OPA689M
GAIN +4 STABLE WIDEBAND VOLTAGE-LIMITING AMPLIFIER

SGLS146B – MARCH 2003 – REVISED DECEMBER 2006

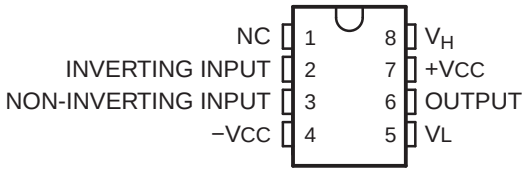
FEATURES

- **High Linearity Near Limiting**
- **Fast Recovery From Overdrive: 2.4 ns**
- **Limiting Voltage Accuracy: ±15 mV**
- **–3-dB Bandwidth (G = 6): 260 MHz**
- **Stable for G ≥ 4**
- **Slew Rate: 1400 V/μs**
- **±5-V and 5-V Supply Operation**
- **High-Gain Version of OPA688**

APPLICATIONS

- **Transimpedance With Fast Overdrive Recovery**
- **Fast Limiting ADC Input Buffers**
- **Low Propagation Delay Comparator**
- **Non-Linear Analog Signal Processing**
- **Difference Amplifier**
- **IF Limiting Amplifier**
- **AM Signal Generation**

JD PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The OPA689 is a wideband, voltage-feedback operational amplifier that offers bipolar output voltage limiting, and is stable for gains ≥4. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15 mV. The operational amplifier operates linearly to within 30 mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100 mV of the desired linear output range. A fast 2.4-ns recovery from limiting ensures that overdrive signals are transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA689 to be used in all standard operational amplifier applications.

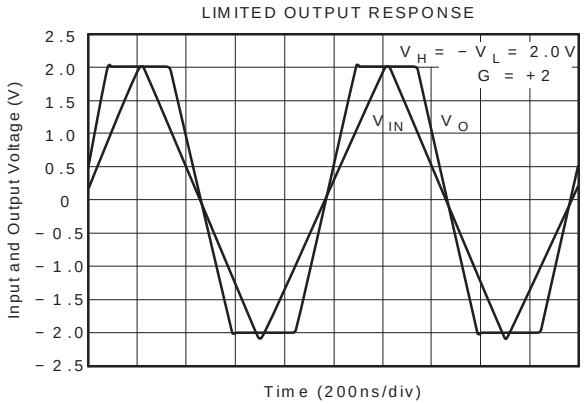
Nonlinear analog signal processing circuits benefit from the OPA689's sharp transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

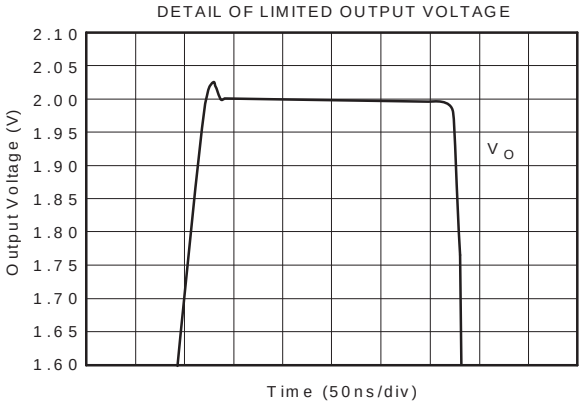
The OPA689M is available in an industry-standard pinout in a CDIP-8 package. For lower gain applications requiring output limiting with fast recovery, consider the OPA688M.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – JD	Tube	OPA689MJD	OPA689MJD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.





Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

		OPA698M	UNIT
	Power supply	–6.5 to 6.5	V
V_{IC}	Common-mode input voltage	$-V_{CC}$ to V_{CC}	V
V_{ID}	Differential input voltage	$-V_{CC}$ to V_{CC}	V
	Limiter voltage range	$-(V_S - 0.7\ V)$ to $(V_S - 0.7\ V)$	V
T_A	Operating free-air temperature range	–55 to 125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s	300	°C
	Case temperature for 10 s	260	°C
T_J	Junction temperature	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Operating voltage	Split-rail operation		±5	±6	V
	Single-supply operation		5	12	
Operating free-air temperature		–55		125	°C

Electrical Characteristics[1]

V_{CC} = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC Performance (See Figure 1)							
	Small signal bandwidth	V_O < 0.5 Vp-p,	G = 6		260		MHz
			G = 12		86		
			G = –6		220		
	Gain bandwidth product (G ≥ 20)	V_O < 0.5 Vp-p			720		MHz
	Gain peaking	V_O = 0.5 V, G = 4			8		dB
	Bandwidth for 0.1-dB gain flatness	V_O = 0.5 V			30		MHz
	Large signal bandwidth	V_O = 2 Vp-p			290		MHz
	Slew rate	V_O = 2 V step			1400		V/µs
	Rise and fall time	V_O = 0.5 V step			1.6		ns
	Settling time to 0.05%	V_O = 2 V step			8		ns
	Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz			61		dB
	Differential gain	R_L = 500 Ω, NTSC, PAL			0.02		%
	Differential phase	R_L = 500 Ω, NTSC, PAL			0.01		°
	Input noise, voltage noise density	f ≥ 1 MHz			4.6		nV/√Hz
	Input noise, current noise density	f ≥ 1 MHz			2		pA/√Hz
DC Performance							
A_{VOL}	Open-loop voltage gain	V_O = ±0.5 V	T_A = 25°C	50	56		dB
			T_A = Full range	47			
V_{IO}	Input offset voltage	T_A = 25°C			±1	±7	mV
		T_A = Full range				±10	
I_{IB}	Input bias current[2]	T_A = 25°C			±8	±12	µA
		T_A = Full range				±20	
I_{IO}	Input offset current	T_A = 25°C			±0.3	±2	µA
		T_A = Full range				±4	
Input							
CMRR	Common-mode rejection ratio	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	53	60		dB
			T_A = Full range	50			
V_{ICR}	Common-mode input voltage range[3]	T_A = 25°C		±3.2	±3.3		V
		T_A = Full range		±3.1			
	Input impedance, differential mode				0.4 1		MΩ pF
	Input impedance, common mode				1 1		MΩ pF
Output							
V_{OH}, V_{OL}	Output voltage range	V_H = 4.3 V, V_L = –4.3 V, R_L ≥ 500 Ω	T_A = 25°C	±3.9	±4.1		V
			T_A = Full range	±3.7			
I_{OH}	Current output, sourcing	V_H = 4.3 V, V_L = –4.3 V, R_L ≥ 20 Ω	T_A = 25°C	90	105		mA
			T_A = Full range	80			
I_{OL}	Current output, sinking	V_H = 4.3 V, V_L = –4.3 V, R_L ≥ 20 Ω	T_A = 25°C	–70	–85		mA
			T_A = Full range	–60			
	Closed-loop output impedance	G = 4, f < 100 kHz			0.2		Ω

(1) All typical limits are at T_A = 25°C (unless otherwise specified).
(2) Current is considered positive out of node.
(3) CMIR tested as <3-dB degradation from minimum CMRR at specified limits.

Electrical Characteristics (continued)

V_{CC} = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply							
V_{CC}	Operating voltage				±5	±6	V
I_{CC}	Quiescent current	T_A = 25°C		14	15.8	17	mA
		T_A = Full range		11		20	
PSRR	Power-supply rejection ratio	Input referred, V_S = ±4.5 V to ±5.5 V	T_A = 25°C	58	70		dB
			T_A = Full range	55			
Output Voltage Limiters (Pins 5 and 8)							
	Default output limited voltage	Limiter pins open	T_A = 25°C	±3	±3.3		V
			T_A = Full range	±2.8			
	Limiter output offset voltage	(V_O – V_H) or (V_O – V_L)	T_A = Full range		±15	±50	mV
	Limiter input bias current magnitude(4)	V_O = 0 V	T_A = 25°C	35	54	65	µA
			T_A = Full range	31		70	
	Limiter input impedance				2 1		MΩ pF
	Limiter feedthrough(5)	f = 5 MHz			–60		dB
	Maximum limiter voltage					±4.3	V
	Minimum limiter voltage separation			400			mV
	Operational amplifier bias current shift(6)				3		µA
	Limiter small signal bandwidth	V_I = ±2 V, V_O < 0.02 Vp-p			450		MHz
	Limter slew rate(7)				100		V/µs
	Limiter step response, overshoot	V_I = ±2 V			250		mV
	Limiter step response, recovery time	V_I = ±2 V			2.4		ns
	Linearity guardband(8)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(4) I_{VH} (V_H bias current) is positive and I_{VL} (V_L bias current) is negative under these conditions (see Note 3, Figure 30, and Figure 37).
(5) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
(6) Current is considered positive out of node.
(7) V_H slew rate conditions are V_{IN} = 0.7 V, G = 6, V_L = –2 V, V_H = step between 2 V and 0 V. V_L slew rate conditions are similar.
(8) Linearity guardband is defined for an output sinusoid (f = 1 MHz, V_O = 2 Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 38).

Electrical Characteristics[1]

V_{CC} = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC Performance (See Figure 2)							
	Small signal bandwidth	V_O < 0.5 Vp-p	G = 6		210		MHz
			G = 12		70		
			G = –6		180		
	Gain bandwidth product	V_O < 0.5 Vp-p, G ≥ 20			440		MHz
	Gain peaking	V_O = 0.5 Vp-p, G = 4			8		dB
	Bandwidth for 0.1-dB gain flatness	V_O = 0.5 Vp-p			30		MHz
	Large signal bandwidth	V_O = 2 Vp-p			175		MHz
	Slew rate	V_O = 2-V step			1050		V/µs
	Rise and fall time	V_O = 0.5-V step			1.9		ns
	Settling time to 0.05%	2-V step			7		ns
	Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz			59		dB
	Input noise, voltage noise density	f ≥ 1 MHz			4.6		nV/√Hz
	Input noise, current noise density	f ≥ 1 MHz			2		pA/√Hz
DC Performance							
A_{VOL}	Open-loop voltage gain	V_O = ±0.4 V	T_A = 25°C	50	56		dB
			T_A = Full range	47			
V_{IO}	Input offset voltage	T_A = 25°C			±1	±7	mV
		T_A = Full range				±10	
I_{IB}	Input bias current	T_A = 25°C			±8	±12	µA
		T_A = Full range				±20	
I_{IO}	Input offset current	T_A = 25°C			±0.3	±2	µA
		T_A = Full range				±4	
Input							
CMRR	Common-mode rejection ratio	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	51	58		dB
			T_A = Full range	48			
V_{ICR}	Common-mode input voltage range[2]	T_A = 25°C		V_{ICM} ±0.7	V_{ICM} ± 0.8		V
		T_A = Full range		V_{ICM} ±0.6			
	Input impedance, differential mode				0.4 1		MΩ pF
	Input impedance, common mode				1 1		MΩ pF
Output							
V_{OH}, V_{OL}	Output voltage range	V_H = V_{ICM} + 1.8 V, V_L = V_{ICM} – 1.8 V, R_L ≥ 500 Ω	T_A = 25°C	V_{ICM} ±1.4	V_{ICM} ±1.6		V
			T_A = Full range	V_{ICM} ±1.3			
I_{OH}	Current output, sourcing	V_{CC} = ±2.5 V, R_L ≥ 20 Ω	T_A = 25°C	60	70		mA
			T_A = Full range	50			
I_{OL}	Current output, sinking	V_{CC} = ±2.5 V, R_L ≥ 20 Ω	T_A = 25°C	–50	–60		mA
			T_A = Full range	–40			
	Closed-loop output impedance	G = 4, f < 100 kHz			0.8		Ω

(1) All typical limits are at T_A = 25°C (unless otherwise specified).
(2) CMIR tested as <3-dB degradation from minimum CMRR at specified limits.

Electrical Characteristics (continued)

V_{CC} = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply							
V_{CC}	Operating voltage				5	12	V
I_{CC}	Quiescent current	T_A = 25°C		11	13	15	mA
		T_A = Full range		9		16.5	
PSRR	Power-supply rejection ratio	Input referred, V_{CC} = ±2 V to ±3 V	T_A = Full range	55	70		dB
Output Voltage Limiters (Pins 5 and 8)							
	Default output limited voltage	Limiter pins open	T_A = 25°C	V_{ICM}± 0.6	V_{ICM}± 0.9		V
			T_A = Full range	V_{ICM}± 0.4			
	Limiter output offset voltage	(V_O – V_H) or (V_O – V_L)	T_A = Full range		±15	±50	mV
	Limiter input bias current magnitude(3)	V_O = 2.5 V	T_A = 25°C	0	35	65	µA
			T_A = Full range	0		85	
	Limiter input bias current drift				30		nA/°C
	Limiter input impedance				2 1		MΩ pF
	Limiter feedthrough(4)	f = 5 MHz			–60		dB
	Limiter offset	V_I = ±2 V, limit mode			±15	±40	mV
	Maximum limiter voltage					V_{ICM}± 1.8 V	V
	Minimum limiter voltage separation			400			mV
	Output bias current shift(5)				5		µA
	Limiter small signal bandwidth	V_I = V_{ICM}± 0.4 V, V_O < 0.02 Vp-p			300		MHz
	Limter slew rate(6)				20		V/µs
	Limiter step response, overshoot	V_I = V_{ICM}± 0.4 V			55		mV
	Limiter step response, recovery time	V_I = V_{ICM}± 0.4 V			15		ns
	Linearity guardband(7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(3) I_{VH} (V_H bias current) is positive and I_{VL} (V_L bias current) is negative under these conditions (see Note 3, Figure 31, and Figure 37).
(4) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
(5) Current is considered positive out of node.
(6) V_H slew rate conditions are V_{IN} = 0.7 V, G = 6, V_L = –2 V, V_H = step between 2 V and 0 V. V_L slew rate conditions are similar.
(7) Linearity guardband is defined for an output sinusoid (f = 1 MHz, V_O = 2 Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 38).

TYPICAL CHARACTERISTICS

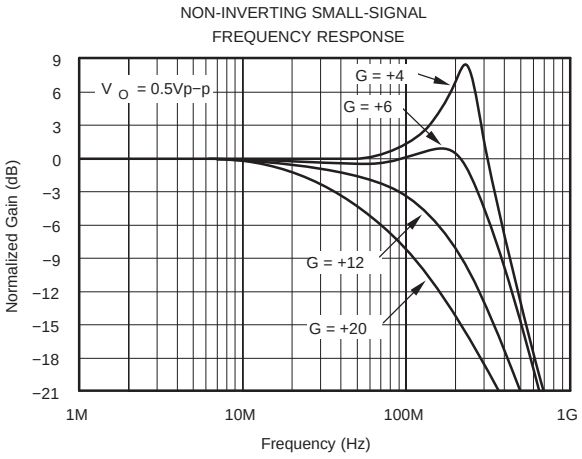


Figure 1.

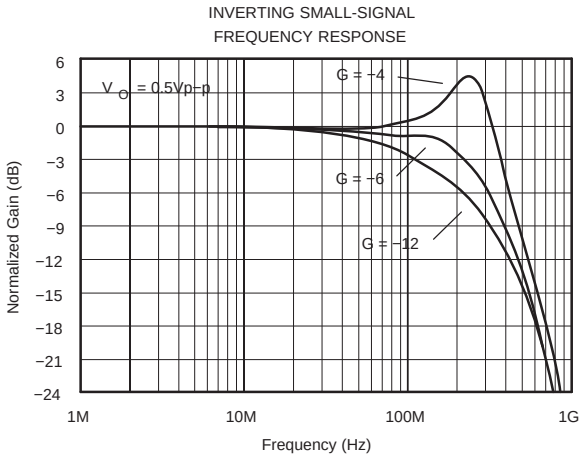


Figure 2.

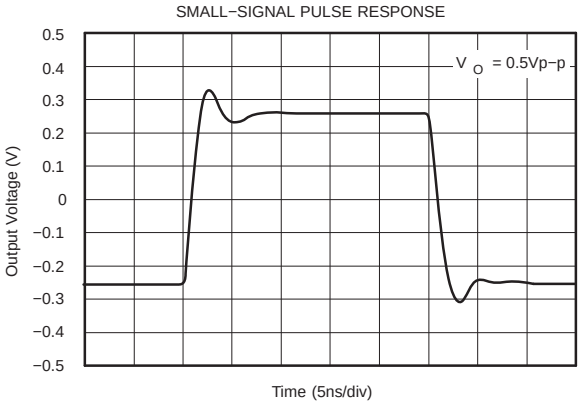


Figure 3.

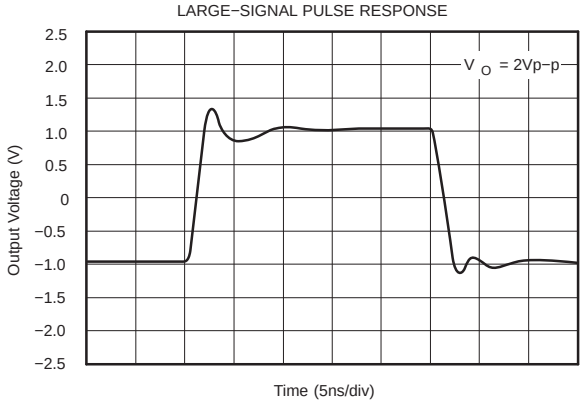


Figure 4.

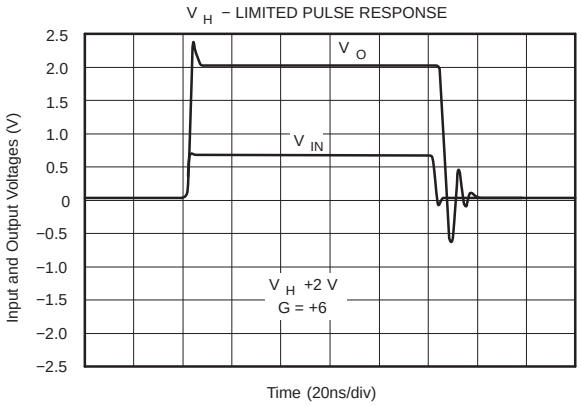


Figure 5.

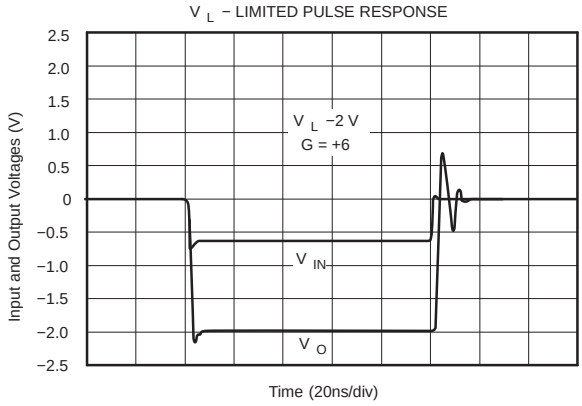


Figure 6.

TYPICAL CHARACTERISTICS (continued)

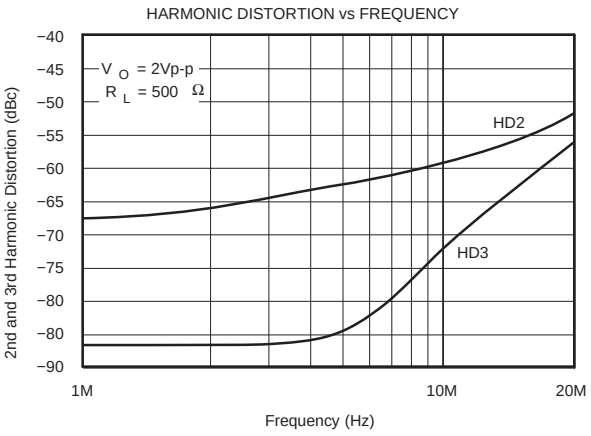


Figure 7.

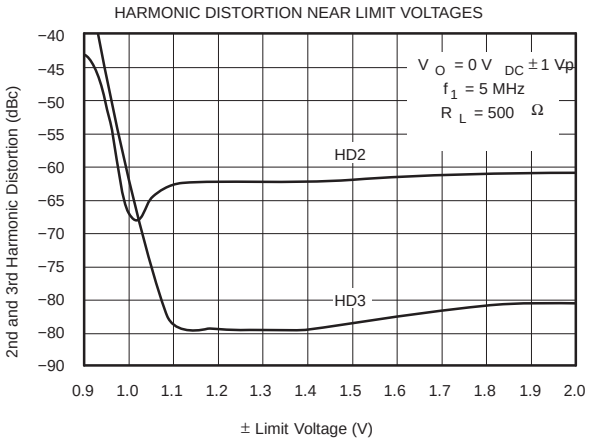
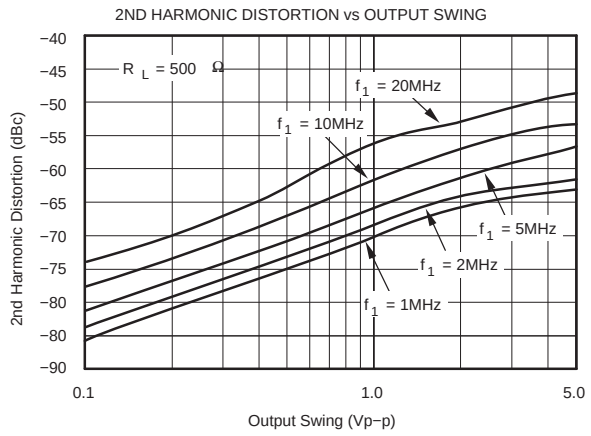


Figure 8.



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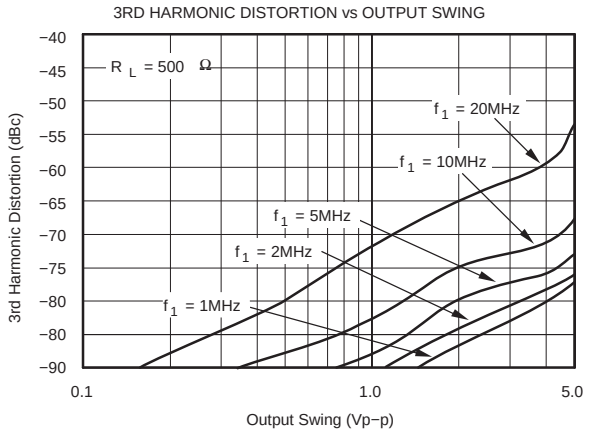

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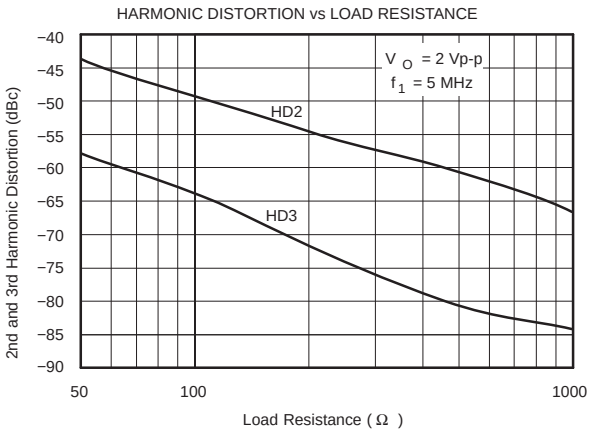

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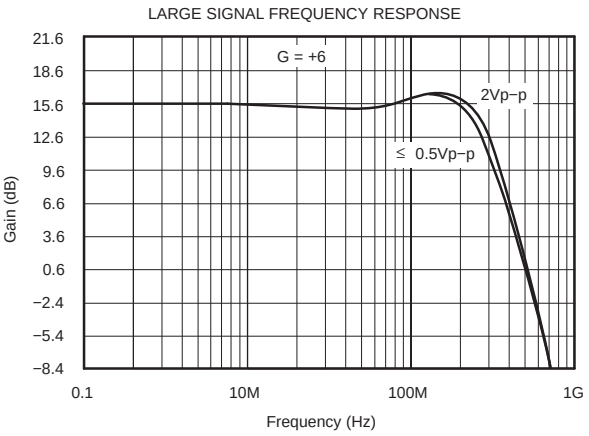
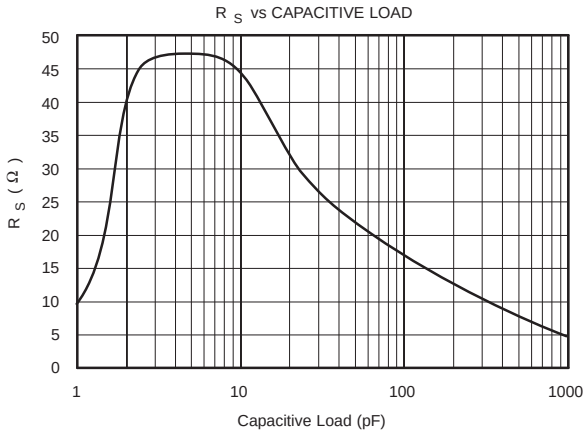


Figure 12.

TYPICAL CHARACTERISTICS (continued)



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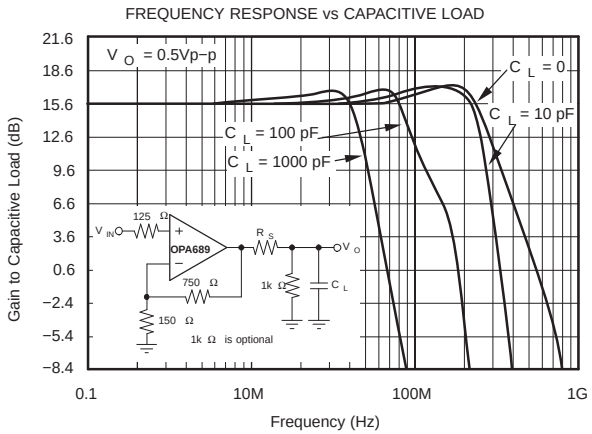

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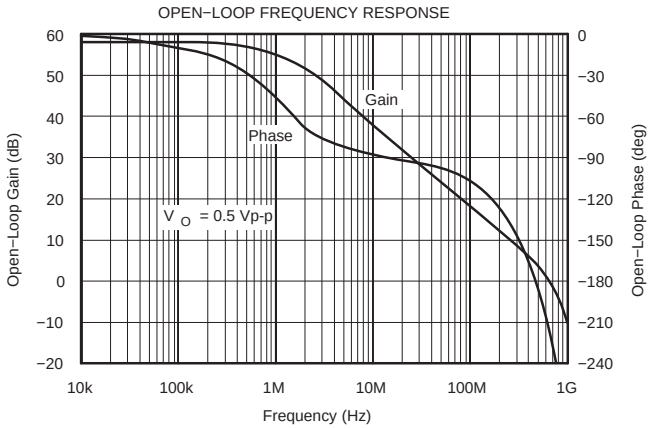

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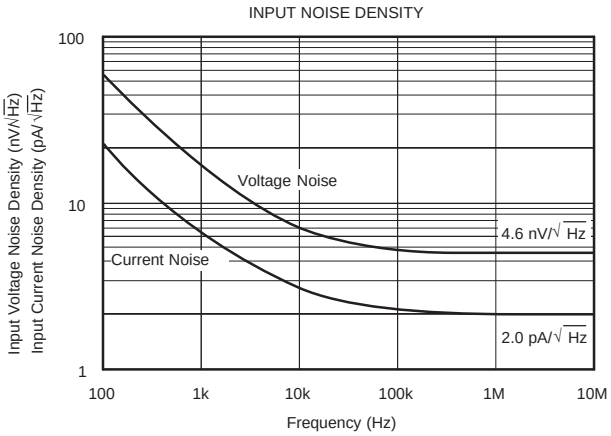

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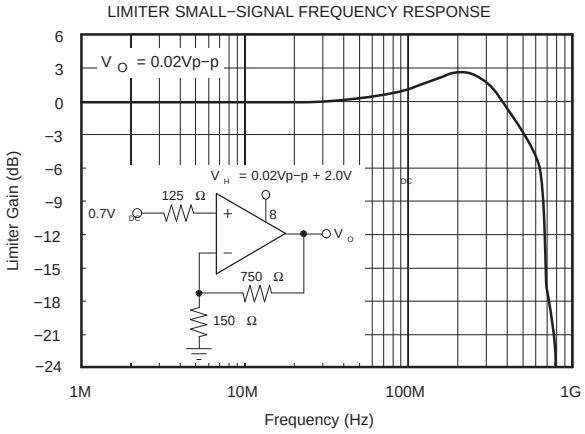


Figure 17.

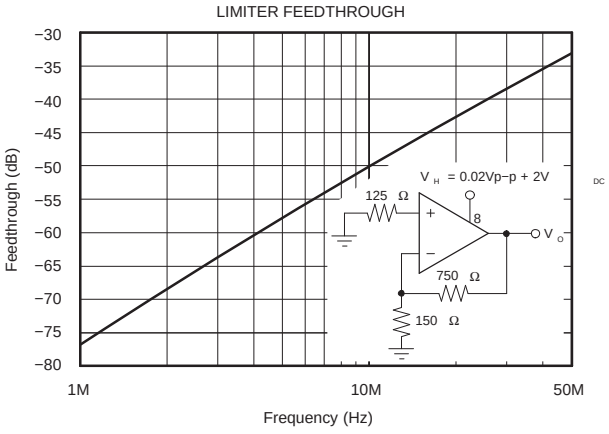
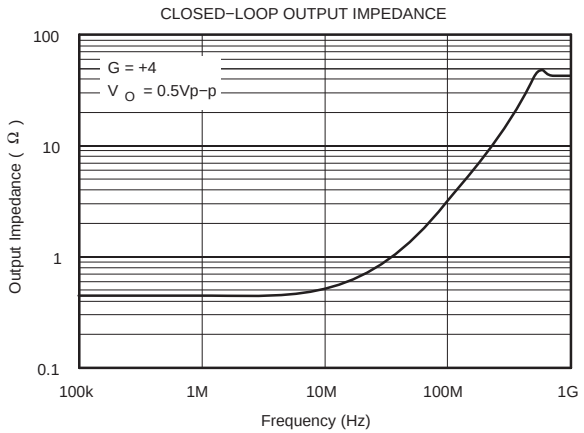


Figure 18.

TYPICAL CHARACTERISTICS (continued)



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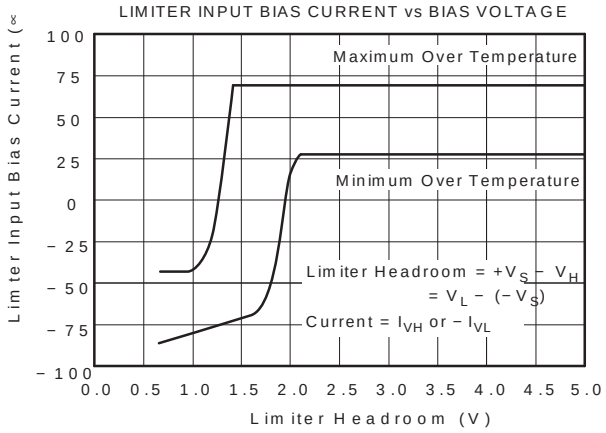


Figure 20.

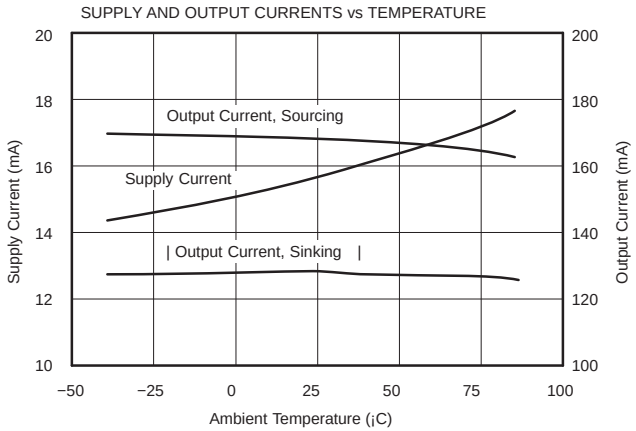
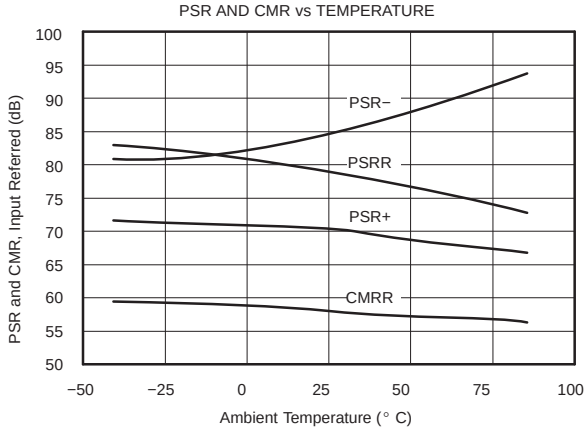


Figure 21.



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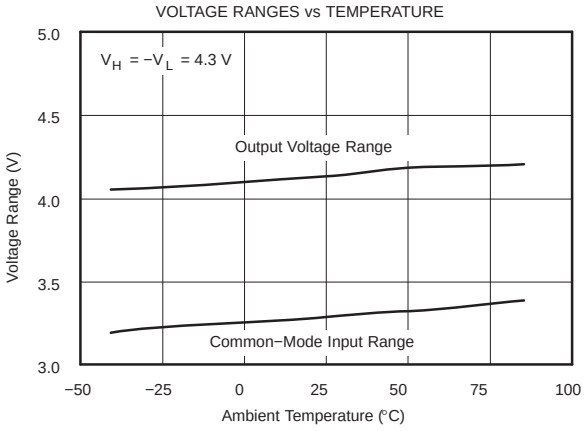

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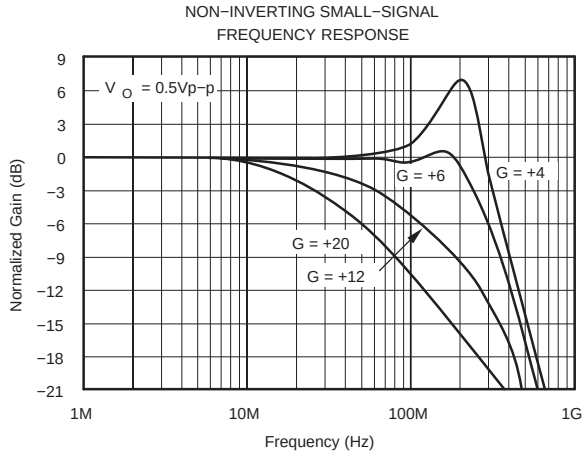


Figure 24.

TYPICAL CHARACTERISTICS (continued)

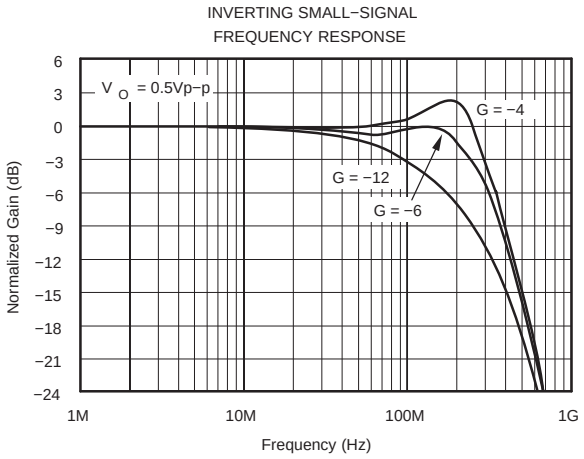


Figure 25.

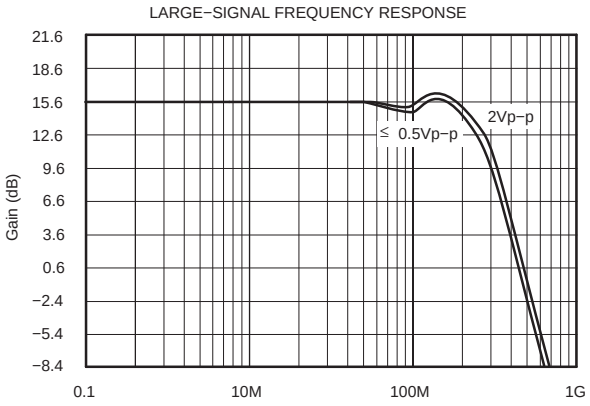


Figure 26.

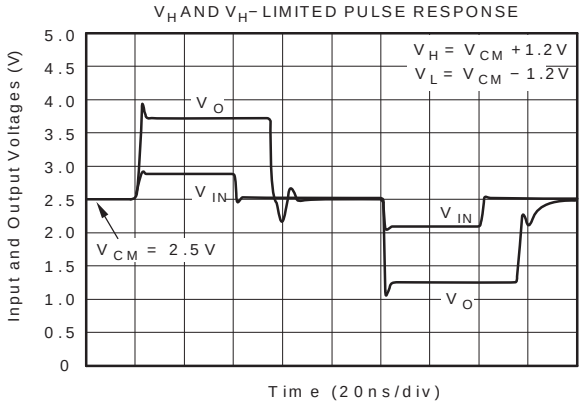


Figure 27.

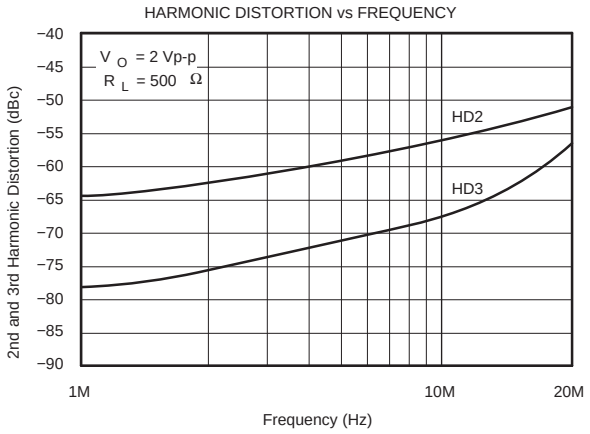


Figure 28.

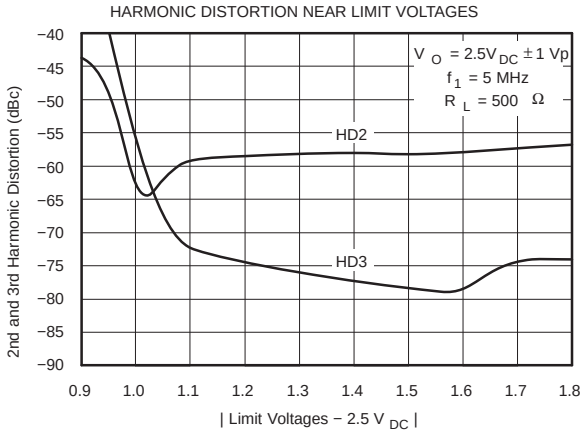


Figure 29.

APPLICATION INFORMATION

Dual-Supply, Non-Inverting Amplifier

Figure 30 shows a non-inverting gain amplifier for dual-supply operation. This circuit was used for AC characterization of the OPA689, with a 50-Ω source, which it matches, and a 500-Ω load. The power-supply bypass capacitors are shown explicitly in Figure 30 and Figure 31, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown.

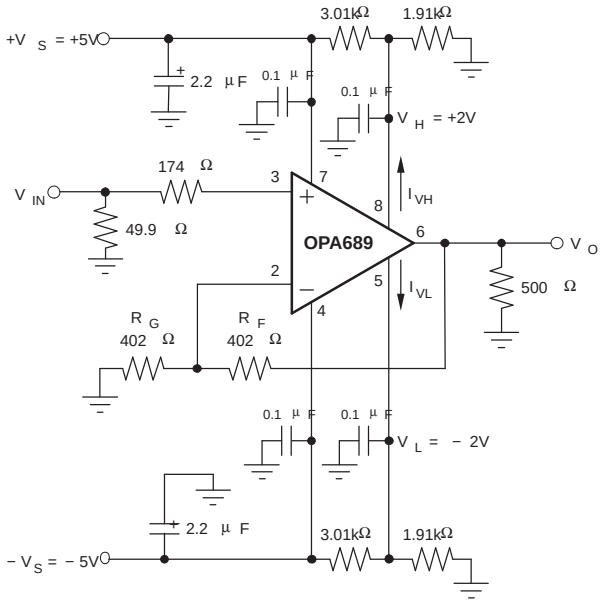


Figure 30. DC-Coupled, Dual Supply Amplifier

Single-Supply, Non-Inverting Amplifier

Figure 31 shows an AC-coupled, non-inverting gain amplifier for single 5-V supply operation. This circuit was used for AC characterization of the OPA689, with a 50-Ω source, which it matches, and a 500-Ω load. The power-supply bypass capacitors are shown explicitly in Figure 30 and Figure 31, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground.

APPLICATION INFORMATION (continued)

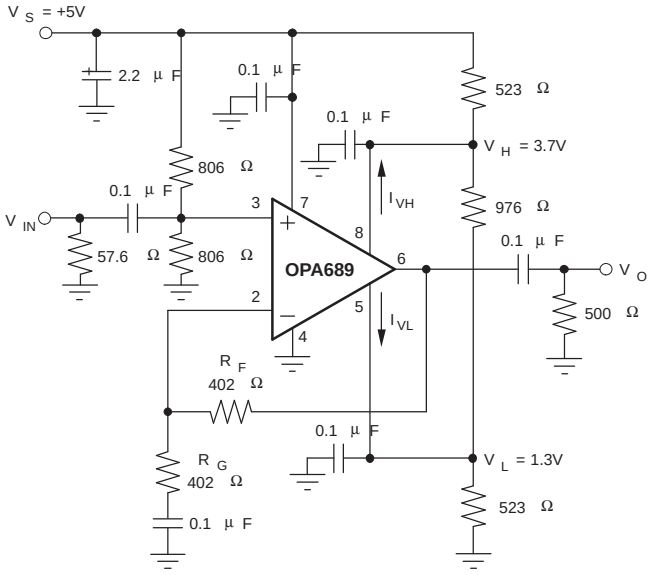


Figure 31. AC-Coupled, Single Supply Amplifier

Limited Output, ADC Input Driver

The circuit in Figure 32 shows an inverting, low distortion ADC driver that operates on a single supply. The converter's internal references bias the op amp input. The 4.0-pF and 18-pF capacitors form a compensation network that allows the OPA689 to have a flat frequency response at a gain of –2. This increases the loop gain of the op amp feedback network, which reduces the distortion products below their specified values.

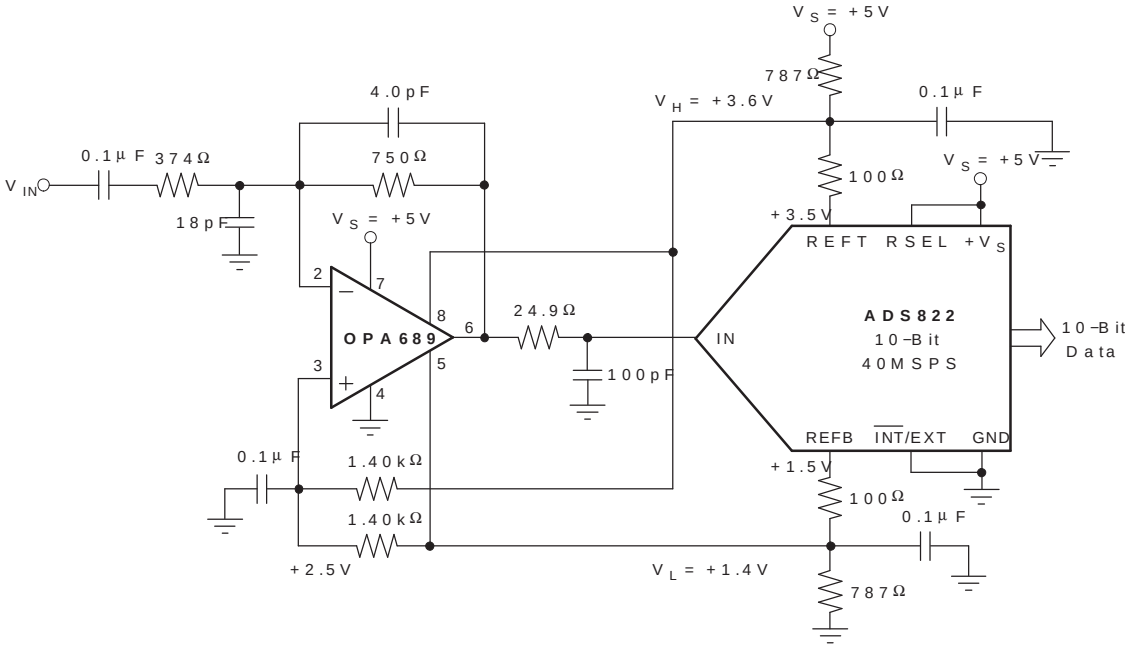


Figure 32. Low Distortion, Limiting ADC Input Driver

APPLICATION INFORMATION (continued)

Precision Half Wave Rectifier

Figure 33 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a voltage between 3.1 and 3.8 V if left open, while the negative limit is set to ground.

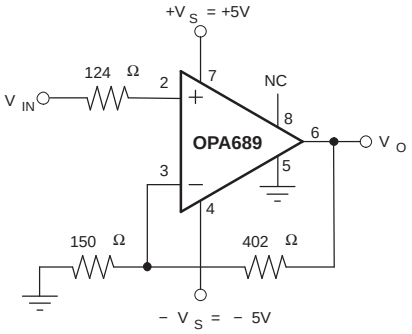


Figure 33. Precision Half Wave Rectifier

Very High Speed Comparator

Figure 34 shows a very high speed comparator with hysterisis. The output level are precisely defined, and the recovery time is exceptional. The output voltage swings between 0.5 V and 3.5 V to provide a logic level output that switches as V_{IN} crosses V_{REF}.

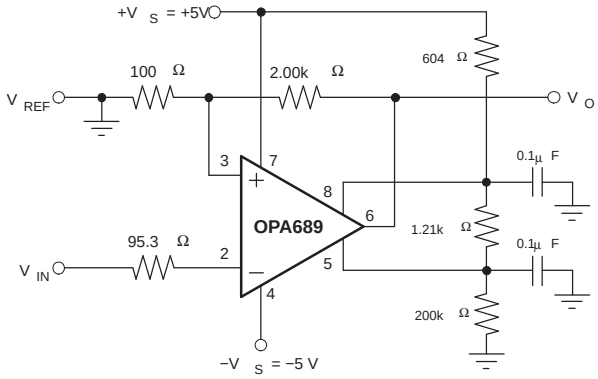


Figure 34. Very High Speed Comparator

Transimpedance Amplifier

Figure 35 shows a transimpedance amplifier that has exceptional overdrive characteristics. The feedback capacitor (C_F) stabilizes the circuit for the assumed diode capacitance (C_D).

APPLICATION INFORMATION (continued)

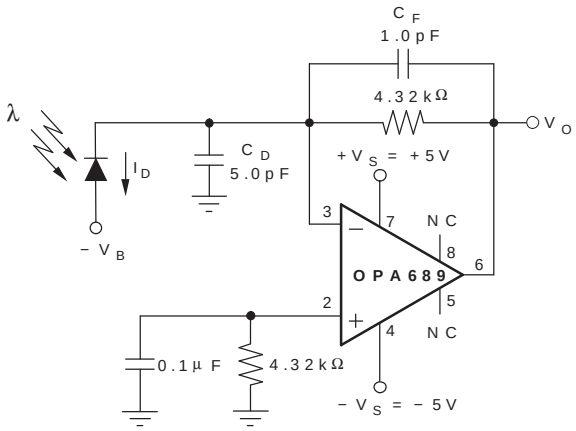


Figure 35. Transimpedance Amplifier

Design-In Tools

Applications Support

The Texas Instruments web site (http://www.ti.com) has the latest data sheets and other design aids.

Demonstration Boards

Two PC boards are available to assist in the initial evaluation of circuit performance of the OPA689 in both package styles. These are available as an unpopulated PCB with descriptive documentation. See the demonstration board literature for more information. The summary information for these boards are shown in Table 1.

Table 1. Evaluation Module Ordering Information

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE NUMBER
OPA689U	SO-8	DEM-OPA-SO-1A	SBOU009

SPICE Models

Computer simulation of circuit performance using SPICE is often useful when analyzing analog circuit or system performance. This is particularly true for high speed amplifier circuits where parasitic capacitance and inductance can have a major effect on frequency response.

SPICE models are available through the Texas Instruments web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion, temperature effects, or different gain and phase characteristics. These models do not distinquish between the AC performance of different package types.

Theory of Operation

The OPA689 is a voltage feedback op amp that is stable for gains ≥4. The output voltage is limited to a range set by the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This avoids saturating any parts in the signal path, gives quick overdrive recovery, and gives consistent limiter accuracy for any gain.

This part is de-compensated (stable for gains ≥4). This gives greater bandwidth, higher slew rate, and lower noise than the unity gain stable companion part OPA689.

The limiters have a very sharp transition from the linear region of operation to output limiting. This allows the limiter voltages to be set very near (<100 mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

Circuit Layout

Achieving optimum performance with the high-frequency OPA689 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

- **Minimize parasitic capacitance to any AC ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.
- **Provide a high quality power supply**. Use linear regulators, ground plane and power planes to provide power. Place high-frequency 0.1 μF decoupling capacitors <0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2 μF to 6.8 μF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.
- **Place external components close** to the OPA689. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.
- **Use high-frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use RF type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2 μF to 6.8 μF) should be tantalum for better high-frequency and pulse performance.
- **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2 pF parasitic parallel capacitance. For resistors >1.5 kΩ, this adds a pole and/or zero below 500 MHz. Make sure that the output loading is not too heavy. The recommended 402-Ω feedback resistor is a good starting point in your design.
- **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve "R_S vs Capacitive Load". Parasitic loads <2 pF may not need the isolation resistor.
- **When long traces are necessary**, use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6 dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded. Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.
- **Do not use sockets** for high-speed parts like the OPA689. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

Power Supplies

The OPA689 is nominally specified for operation using either ±5-V supplies or a single 5-V supply. The maximum specified total supply voltage of 13 V allows reasonable tolerances on the supplies. Higher supply

voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single-supply operation circuits.Figure 31 shows one approach to single-supply operation.

ESD Protection

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high-speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA689.

Output Limiters

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L.

Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is sharp—the desired output signal can safely come to within 30 mV of V_H or V_L. Distortion performance is also good over the same range.

The limiter voltages can be set to within 0.7 V of the supplies ($V_L \geq -V_S + 0.7$ V, $V_H \leq +V_S - 0.7$ V). They must also be at least 400 mV apart ($V_H - V_L \geq 0.4$ V).

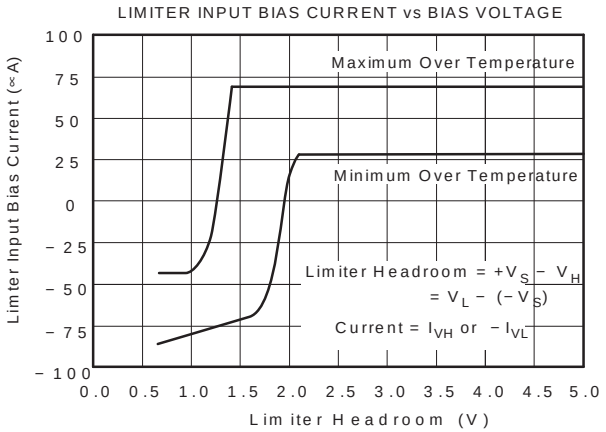


Figure 36. Limiter Bias Current vs Bias Voltage

When pins 5 and 8 are left open, V_H and V_L go to the Default Voltage Limit; the minimum values are in the Specifications. Looking at Figure 37 for the zero bias current case will show the expected range of (V_S– default limit voltages) = headroom.

When the limiter voltages are more than 2.1 V from the supplies ($V_L \geq -V_S + 2.1$ V or $V_H \leq V_S - 2.1$ V), you can use simple resistor dividers to set V_H and V_L (see Figure 30). Make sure you include the Limiter Input Bias Currents (Figure 37) in the calculations (i.e., $I_{VL} \geq -50$ µA out of pin 5, and $I_{VH} \leq 50$ µA out of pin 8). For good limiter voltage accuracy, run at least 1-mA quiescent bias current through these resistors.

When the limiter voltages need to be within 2.1 V of the supplies ($V_L \leq -V_S + 2.1$ V or $V_H \geq V_S - 2.1$ V), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This will typically be the case for single supply operation (V_S = 5 V). Figure 31 runs 2.5 mA through the resistive divider that sets V_H and V_L. This keeps errors due to I_{VH} and I_{VL} <±1% of the target limit voltages.

The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (e.g., 5%). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The Limiter Offset Voltage only slightly degrades limiter accuracy.

Figure 37 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

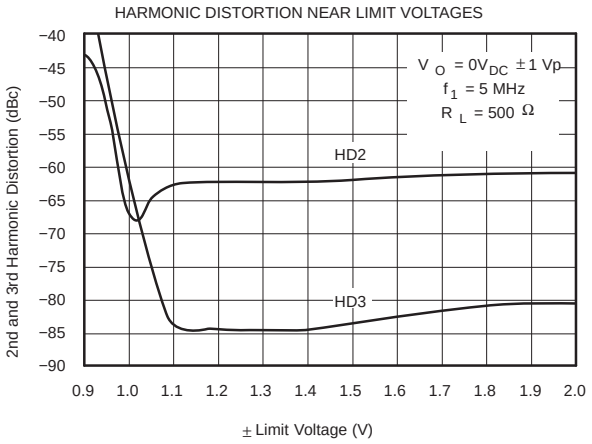
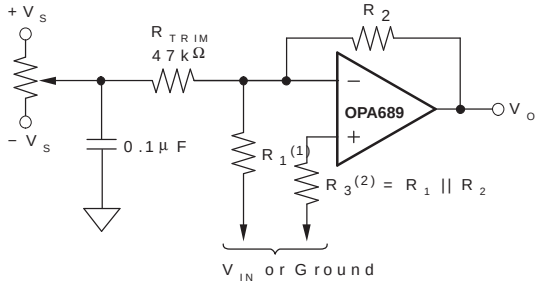


Figure 37. Harmonic Distortion Near Limit Voltages

Offset Voltage Adjustment

The circuit in Figure 38 allows offset adjustment without degrading offset drift with temperature. Use this circuit with caution since power supply noise can inadvertently couple into the op amp.



NOTES: (1) Set R_1 << R_{TRIM}. (2) R_3 is optional and minimizes output offset due to input bias currents.

Figure 38. Offset Voltage Trim

Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both DC input bias currents using R_3. This minimizes the output offset voltage caused by the input bias currents.

Output Drive

The OPA689 has been optimized to drive 500-Ω loads, such as ADCs. It still performs very well driving 100-Ω loads; the specifications are shown for the 500-Ω load. This makes the OPA689 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve "Output Impedance vs Frequency", the OPA689 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

Thermal Considerations

The OPA689 will not require heat-sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at a maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that comprises P_{DL}.

The operating junction temperature is: $T_J = T_A + P_D\theta_{JA}$, where T_A is the ambient temperature.

For example, the maximum T_J for a OPA689M with G = 6, R_{FB} = 750 Ω, R_L = 100 Ω, and $\pm V_S$ = ±5 V at the maximum T_A = 85°C is calculated as:

$$P_{DQ} = (10\ V \times 20\ mA) = 200\ mW$$

$$P_{DL} = \frac{(5\ V)^2}{4 \times (100\ \Omega \parallel 850\ \Omega)}$$

$$P_D = 200\ mW + 70\ mW = 270\ mW$$

$$T_J = 85°C + 270\ mW \times (119°C/W) = 117°C$$

Capacitive Loads

Capacitive loads, such as the input to ADCs, will decrease the amplifier's phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads × 2 pF should be isolated by connecting a small resistor in series with the output as shown in Figure 39. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

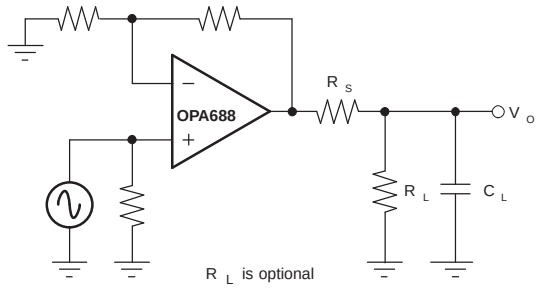


Figure 39. Driving Capacitive Loads

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29 pF/foot for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

Frequency Response Compensation

The OPA689 is internally compensated to be unity-gain stable at a gain of +4, and has a nominal phase margin of 60 degrees at a gain of +6. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –5 is equivalent to a gain of +6 for bandwidth purposes (i.e., noise gain = 6).

Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high gain applications, use a three resistor "Tee" network to reduce the RC time constants set by the parasitic capacitances. Be careful to not increase the noise generated by this feedback network too much.

Pulse Settling Time

The OPA689 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve "R_S vs Capacitive Load". Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics when recovering from overdrive are very good.

Distortion

The OPA689's distortion performance is specified for a 500-Ω load, such as an ADC. Driving loads with smaller resistance will increase the distortion as shown in Figure 40. Remember to include the feedback network in the load resistance calculations.

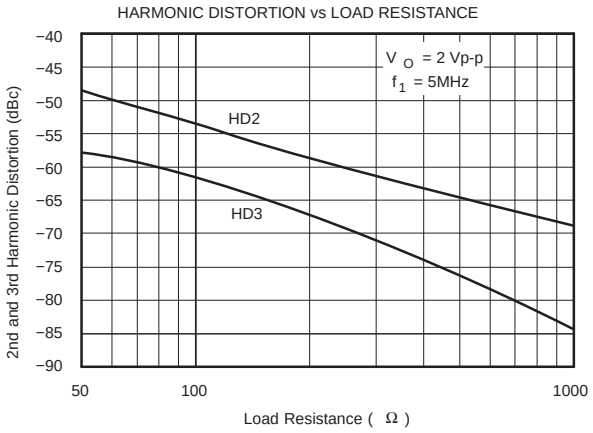


Figure 40. 5-MHz Harmonic Distortion vs Load Resistance

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA689MJD	NRND	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA689MJD
OPA689MJD.A	NRND	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA689MJD

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

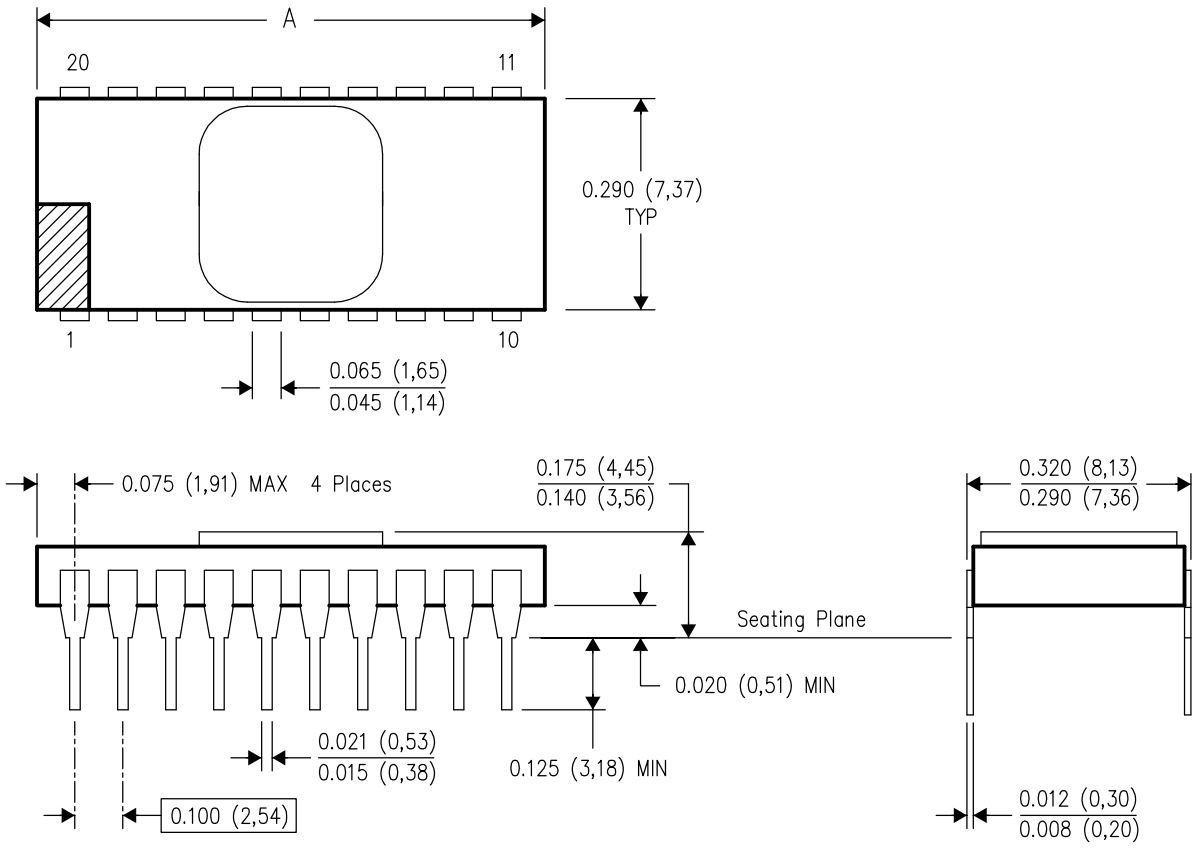
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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