OPA657 1.6-GHz, Low-Noise, FET-Input Operational Amplifier

1 Features

- High Gain Bandwidth Product: 1.6 GHz
- High Bandwidth 275 MHz (G = 10)
- Slew Rate 700 V/µs (G = 10, 1-V Step)
- Available in High Grade With Improved DC Specifications
- Operating Temperature Range: –40°C to 85°C
- Low-Input Offset Voltage: ±250 µV
- Low-Input Bias Current: 2 pA
- Low-Input Voltage Noise: 4.8 nV/$\sqrt{Hz}$
- High-Output Current: 70 mA
- Fast Overdrive Recovery

2 Applications

- Wideband Photodiode Amplifier
- Wafer Scanning Equipment
- ADC Input Amplifier
- Test and Measurement Front End
- High Gain Precision Amplifier
- Optical Time Domain Reflectometry (OTDR)

3 Description

The OPA657 device combines a high-gain bandwidth, low-distortion, voltage-feedback operational amplifier with a low-voltage noise JFET-input stage to offer a very high dynamic range amplifier for high-precision ADC (analog-to-digital converter) driving or wideband transimpedance applications. Photodiode applications see improved noise and bandwidth using this decompensated, high-gain bandwidth amplifier.

Very low level signals can be significantly amplified in a single OPA657 gain stage with exceptional bandwidth and accuracy. Having a high 1.6-GHz gain bandwidth product gives greater than 10-MHz signal bandwidths up to gains of 160 V/V (44 dB). The very low input bias current and capacitance supports this performance even for relatively high source impedances.

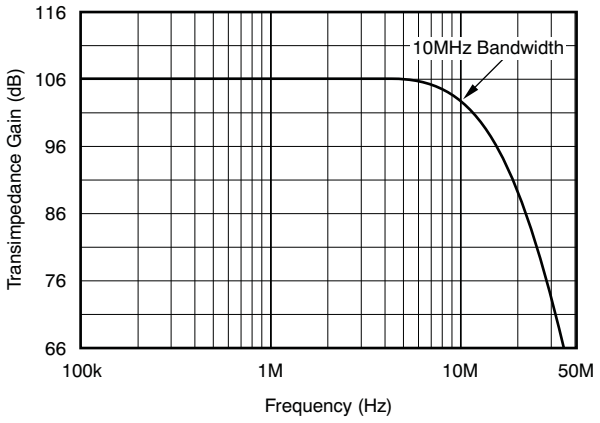
Broadband photodetector applications benefit from the low-voltage noise JFET inputs for the OPA657. The JFET input contributes virtually no current noise while for broadband applications, a low voltage noise is also required. The low 4.8 nV/$\sqrt{Hz}$ input voltage noise provides exceptional input sensitivity for higher bandwidth applications. The example shown below gives a total equivalent input noise current of 1.8 pA/$\sqrt{Hz}$ over a 10-MHz bandwidth.

Device Information(1)

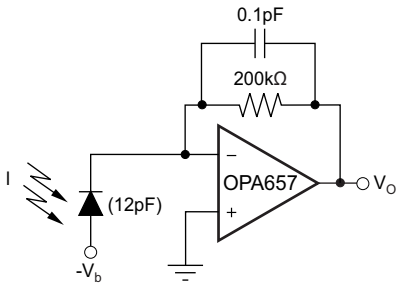
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA657	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Frequency Response of 200-kΩ Transimpedance Amplifier



Wideband Photodiode Transimpedance Amplifier



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2008) to Revision F **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *lead temperature* parameter from *Absolute Maximum Ratings* table ... 4
- Added Power Supply, *Minimum Operating Voltage* specification to ±5V *Electrical Characteristics* table ... 6

Changes from Revision D (March 2006) to Revision E **Page**

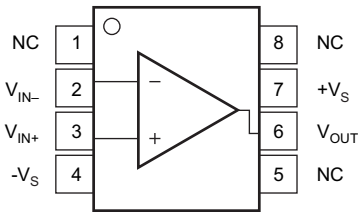
- Changed minimum storage temperature range from –40°C to –65°C ... 4

5 Related Operational Amplifier Products

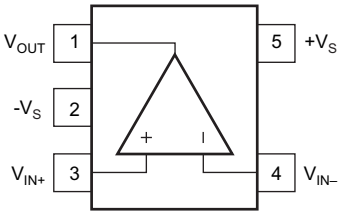
DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA657	±5	1600	700	4.8	Gain of +7 stable FET Input
OPA656	±5	230	290	7	Unity-Gain Stable FET-Input
OPA659	±6	350	2550	8.9	Unity-Gain Stable FET-Input
LMH6629	5	4000	1600	0.69	Gain of +10 stable Bipolar Input
THS4631	±15	210	1000	7	Unity-Gain Stable FET-Input
OPA857	5	4750	220	—	Programmable Gain (5 kΩ / 20 kΩ) Transimpedance Amplifier

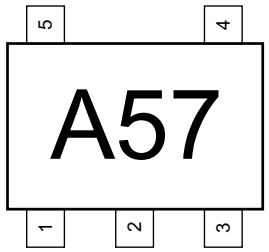
6 Pin Configuration and Functions

D Package
8-Pin SOIC Surface-Mount
Top View



DBV Package
5-Pin SOT-23
Top View





Pin Orientation/Package Marking

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
NC	1	—	—	No Connection
	5			
	8			
V_{IN-}	2	4	I	Inverting Input
V_{IN+}	3	3	I	Noninverting Input
$-V_S$	4	2	POW	Negative Power Supply
V_{OUT}	6	1	O	Output of amplifier
$+V_S$	7	5	POW	Positive Power Supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (Total Bipolar Supplies)		±6.5	V
Internal power dissipation	See *Thermal Information*		
Differential input voltage	$-V_S$	$+V_S$	V
Input voltage	$-V_S$	$+V_S$	V
Junction temperature (T_J)		175	°C
Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
	Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	8	10	12	V
T_A	Ambient temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA657		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.2	140.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.9	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.2	24.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.4	61.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_S = ±5 V

At R_F = +453 Ω, R_L = +100 Ω, and G = +10 V/V, unless otherwise noted. See Figure 29 for AC performance.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE (see Figure 29)							
Small-signal bandwidth	G = +7 V/V, V_O = 200 mV_{PP}	T_J = 25°C		350		MHz	C
	G = +10 V/V, V_O = 200 mV_{PP}	T_J = 25°C		275			
	G = +20 V/V, V_O = 200 mV_{PP}	T_J = 25°C		90			
Gain-bandwidth product	G > +40 V/V	T_J = 25°C		1600		dB	C
Bandwidth for 0.1dB Flatness	G = +10 V/V, 2 V_{PP}	T_J = 25°C		30		MHz	C
Peaking at a Gain of +7		T_J = 25°C		7		dB	C
Large-Signal Bandwidth	G = +10 V/V, 2 V_{PP}	T_J = 25°C		180		MHz	C
Slew Rate	G = +10 V/V, 1-V Step	T_J = 25°C		700		V/µs	C
Rise-and-Fall Time	0.2-V Step	T_J = 25°C		1		ns	C
Settling Time to 0.02%	G = +10 V/V, V_O = 2-V Step	T_J = 25°C		20		ns	C
Harmonic Distortion	G = +10 V/V, f = 5 MHz, V_O = 2 V_{PP}						C
2nd-Harmonic	R_L = 200 Ω	T_J = 25°C		–70		dBc	C
	R_L > 500 Ω	T_J = 25°C		–74		dBc	C
3rd-Harmonic	R_L = 200 Ω	T_J = 25°C		–99		dBc	C
	R_L > 500 Ω	T_J = 25°C		–106		dBc	C
Input Voltage Noise	f > 100 kHz	T_J = 25°C		4.8		nV/√Hz	C
Input Current Noise	f > 100 kHz	T_J = 25°C		1.3		fA/√Hz	C
DC PERFORMANCE(2)							
Open-Loop Voltage Gain (A_{OL})	V_{CM} = 0 V, R_L = 100 Ω	T_J = 25°C	65	70		dB	A
		T_J = 0°C to 70°C(3)	64				
		T_J = –40°C to 85°C(3)	63				
Input Offset Voltage	V_{CM} = 0 V	T_J = 25°C		±0.25	±1.8	mV	A
		T_J = 0°C to 70°C(3)			±2.2		
		T_J = –40°C to 85°C(3)			±2.6		
Average Offset Voltage Drift	V_{CM} = 0 V	T_J = 25°C	±12	±2		µV/°C	A
		T_J = 0°C to 70°C(3)	±12				
		T_J = –40°C to 85°C(3)	±12				
Input Bias Current	V_{CM} = 0 V	T_J = 25°C		±2	±20	pA	A
		T_J = 0°C to 70°C(3)			±1800		
		T_J = –40°C to 85°C(3)			±5000		
Input Offset Current	V_{CM} = 0 V	T_J = 25°C		±1	±10	pA	A
		T_J = 0°C to 70°C(3)			±900		
		T_J = –40°C to 85°C(3)			±2500		
INPUT							
Most Positive Input Voltage(4)		T_J = 25°C	2	2.5		V	A
		T_J = 0°C to 70°C(3)	1.9				
		T_J = –40°C to 85°C(3)	1.8				
Most Negative Input Voltage(4)		T_J = 25°C	–3.5	–4		V	A
		T_J = 0°C to 70°C(3)	–3.4				
		T_J = –40°C to 85°C(3)	–3.3				
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5 V	T_J = 25°C	83	89		dB	A
		T_J = 0°C to 70°C(3)	81				
		T_J = –40°C to 85°C(3)	79				
Input Impendance							

(1) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature specifications.
(4) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

Electrical Characteristics: V_S = ±5 V (continued)

At R_F = +453 Ω, R_L = +100 Ω, and G = +10 V/V, unless otherwise noted. See Figure 29 for AC performance.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Differential		T_J = 25°C		10^{12} || 0.7		Ω || pF	C
Common-Mode		T_J = 25°C		10^{12} || 4.5		Ω || pF	C
OUTPUT							
Voltage Output Swing	No load	T_J = 25°C		±3.9		V	A
		T_J = 0°C to 70°C (3)		±3.7			
	R_L = 100 Ω	T_J = 25°C	±3.3	±3.5		V	B
		T_J = 0°C to 70°C (3)	±3.2				
		T_J = –40°C to 85°C (3)	±3.1				
Current Output, Sourcing		T_J = 25°C	50	70		mA	A
		T_J = 0°C to 70°C (3)	48				
		T_J = –40°C to 85°C (3)	46				
Current Output, Sinking		T_J = 25°C	–50	–70		mA	A
		T_J = 0°C to 70°C (3)	–48				
		T_J = –40°C to 85°C (3)	–46				
Closed-Loop Output Impedance	G = +10 V/V, f = 0.1 MHz	T_J = 25°C		0.02		Ω	A
POWER SUPPLY							
Specified Operating Voltage		T_J = 25°C		±5		V	A
Minimum Operating Voltage		T_J = 25°C		±4		V	C
Maximum Operating Voltage Range		T_J = 25°C			±6	V	A
		T_J = 0°C to 70°C (3)			±6		
		T_J = –40°C to 85°C (3)			±6		
Maximum Quiescent Current		T_J = 25°C		14	16	mA	A
		T_J = 0°C to 70°C (3)			16.2		
		T_J = –40°C to 85°C (3)			16.3		
Minimum Quiescent Current		T_J = 25°C	11.7	14		mA	A
		T_J = 0°C to 70°C (3)	11.4				
		T_J = –40°C to 85°C (3)	11.1				
Power-Supply Rejection Ratio (+PSRR)	+VS = 4.5 V to 5.5 V	T_J = 25°C	76	80		dB	A
		T_J = 0°C to 70°C (3)	74				
		T_J = –40°C to 85°C (3)	72				
Power-Supply Rejection Ratio (–PSRR)	–VS = 4.5 V to 5.5 V	T_J = 25°C	62	68		dB	A
		T_J = 0°C to 70°C (3)	60				
		T_J = –40°C to 85°C (3)	58				
TEMPERATURE RANGE							
Specified Operating Range: U, N Package		T_J = 25°C		–40 to +85		°C	
Thermal Resistance, $R_{\theta JA}$	Junction-to-Ambient						
U: SO-8		T_J = 25°C		125		°C/W	
N: SOT23-5		T_J = 25°C		150		°C/W	

7.6 Electrical Characteristics: V_S - ±5 V, High-Grade DC Specifications

At R_F = 453 Ω, R_L = 100 Ω, and G = +10 V/V, unless otherwise noted. (1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (2)
Input Offset Voltage	V_{CM} = 0 V	T_J = 25°C		±0.1	±0.6 (3)	mV	A
		T_J = 0°C to 70°C (4)			±0.85		
		T_J = –40°C to 85°C (4)			±0.9		
Input Offset Voltage Drift	V_{CM} = 0 V	T_J = 25°C		±2	±6 (3)	µV/°C	A
		T_J = 0°C to 70°C (4)			±6		
		T_J = –40°C to 85°C (4)			±6		
Input Bias Current	V_{CM} = 0 V	T_J = 25°C		±1	±5 (3)	pA	A
		T_J = 0°C to 70°C (4)			±450		
		T_J = –40°C to 85°C (4)			±1250		
Input Offset Current	V_{CM} = 0 V	T_J = 25°C		±0.5	±5 (3)	pA	A
		T_J = 0°C to 70°C (4)			±450		
		T_J = –40°C to 85°C (4)			±1250		
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5 V	T_J = 25°C	91 (3)	98		dB	A
		T_J = 0°C to 70°C (4)	89				
		T_J = –40°C to 85°C (4)	87				
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.5 V to 5.5 V	T_J = 25°C	78 (3)	82		dB	A
		T_J = 0°C to 70°C (4)	76				
		T_J = –40°C to 85°C (4)	74				
Power-Supply Rejection Ratio (–PSRR)	$–V_S$ = –4.5 V to –5.5 V	T_J = 25°C	68 (3)	74		dB	A
		T_J = 0°C to 70°C (4)	66				
		T_J = –40°C to 85°C (4)	64				

(1) All other specifications are the same as the standard-grade.
(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation.
(3) Junction temperature = ambient for +25°C specifications.
(4) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature specifications.

7.7 Typical Characteristics: V_S = ±5 V

At T_A = 25°C, G = 10 V/V, R_F = 453 Ω, and R_L = 100 Ω, unless otherwise noted.

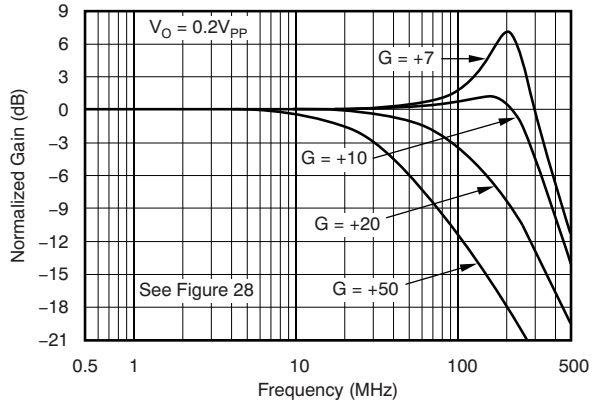


Figure 1. Noninverting Small-Signal Frequency Response

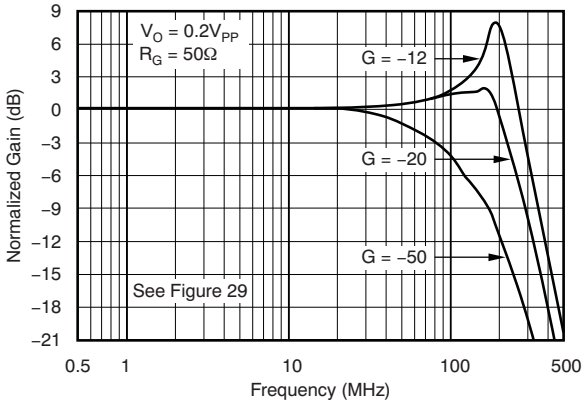


Figure 2. Inverting Small-Signal Frequency Response

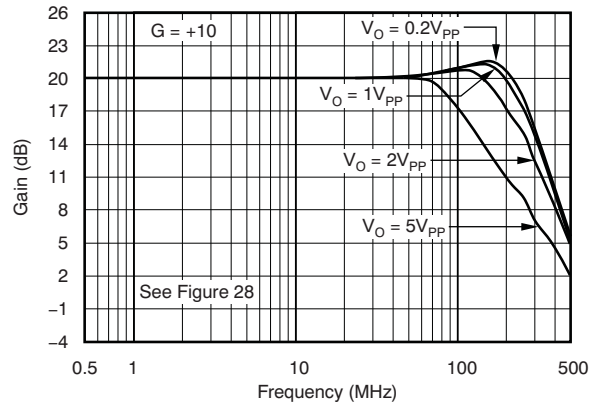


Figure 3. Noninverting Large-Signal Frequency Response

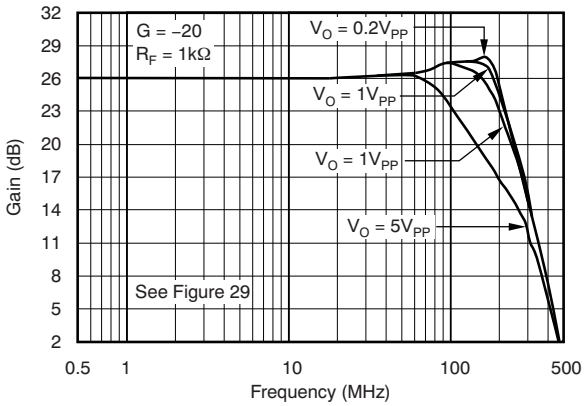


Figure 4. Inverting Large-Signal Frequency Response

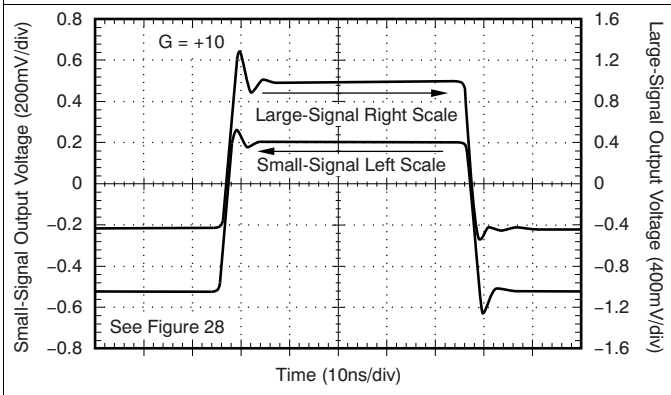


Figure 5. Noninverting Pulse Response

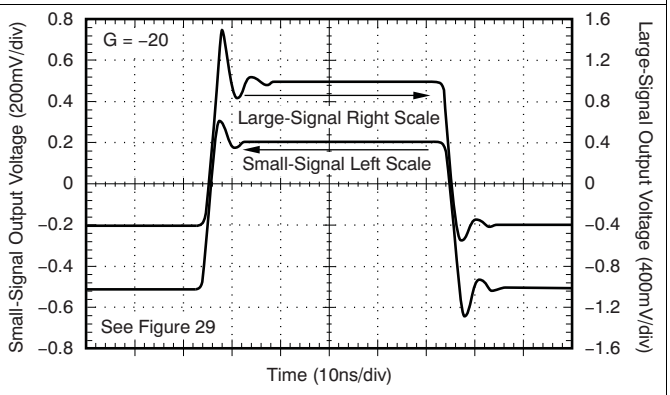


Figure 6. Inverting Pulse Response

Typical Characteristics: V_S = ±5 V (continued)

At T_A = 25°C, G = 10 V/V, R_F = 453 Ω, and R_L = 100 Ω, unless otherwise noted.

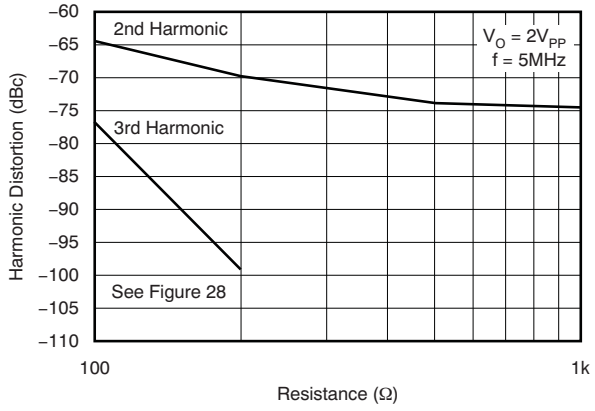


Figure 7. Harmonic Distortion vs Load Resistance

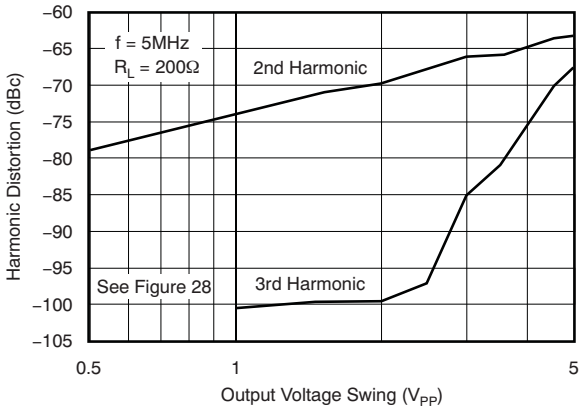


Figure 8. Harmonic Distortion vs Output Voltage (5 MHz)

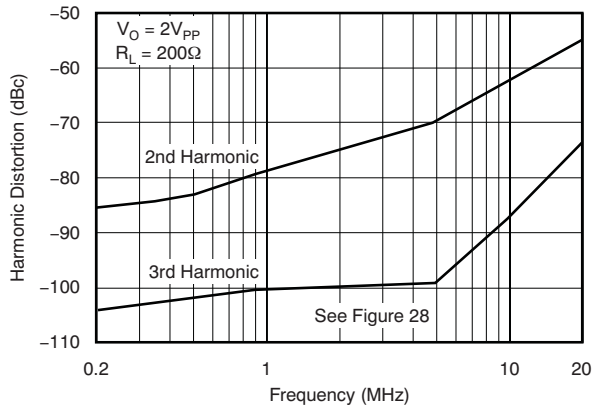


Figure 9. Harmonic Distortion vs Frequency

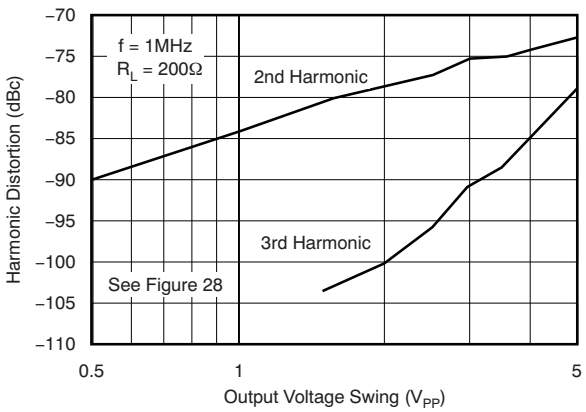


Figure 10. Harmonic Distortion vs Output Voltage (1 MHz)

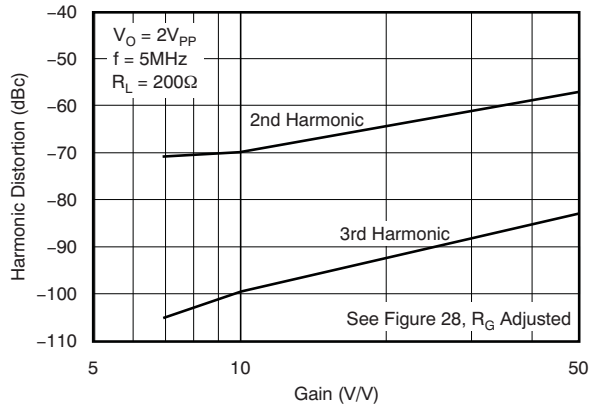


Figure 11. Harmonic Distortion vs Noninverting Gain

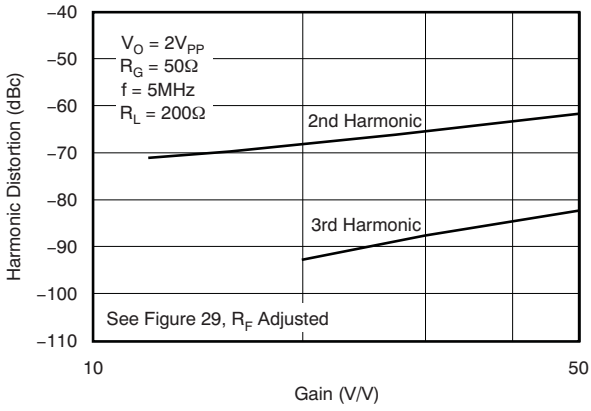


Figure 12. Harmonic Distortion vs Inverting Gain

Typical Characteristics: V_S = ±5 V (continued)

At T_A = 25°C, G = 10 V/V, R_F = 453 Ω, and R_L = 100 Ω, unless otherwise noted.

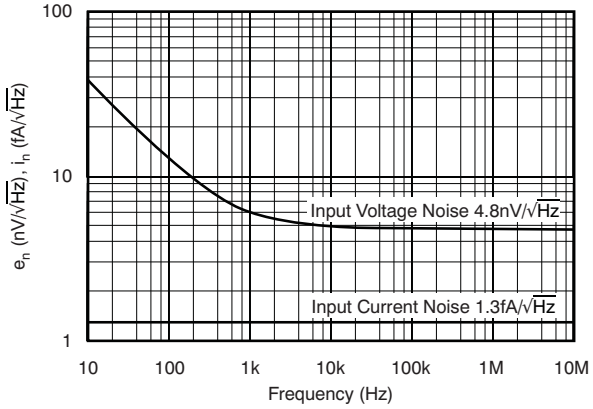


Figure 13. Input Current And Voltage Noise Density

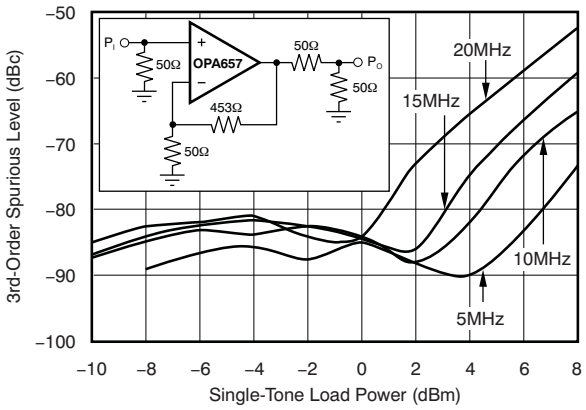


Figure 14. 2-Tone, 3rd-Order IMD Spurious

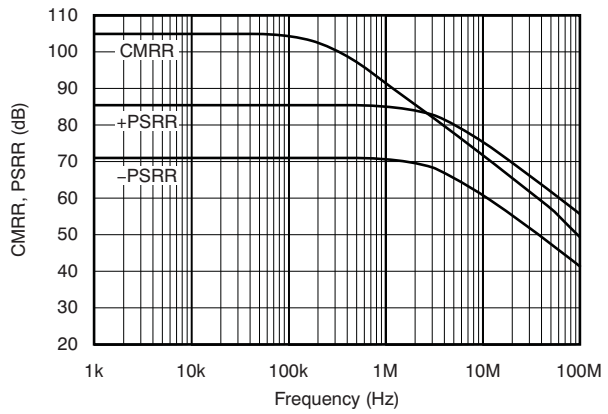


Figure 15. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

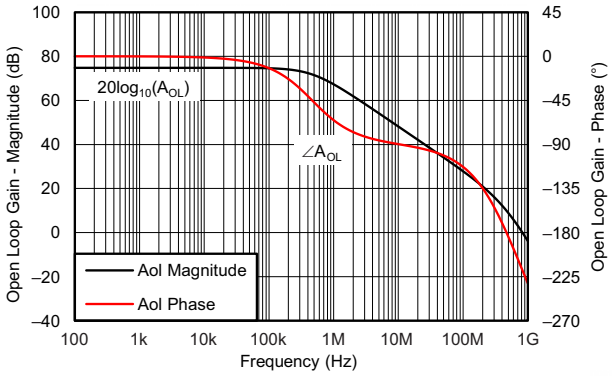


Figure 16. Open-Loop Gain and Phase

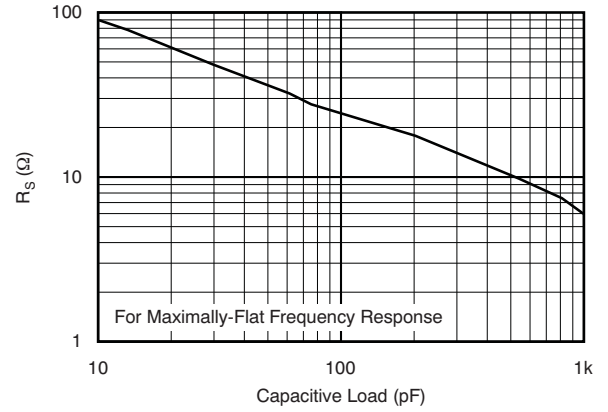


Figure 17. Recommended R_S vs Capacitive Load

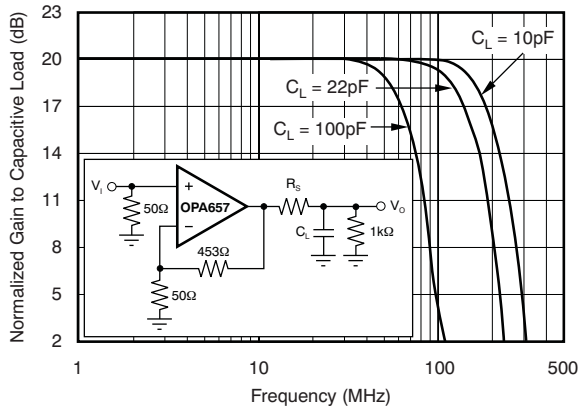


Figure 18. Frequency Response vs Capacitive Load

Typical Characteristics: V_S = ±5 V (continued)

At T_A = 25°C, G = 10 V/V, R_F = 453 Ω, and R_L = 100 Ω, unless otherwise noted.

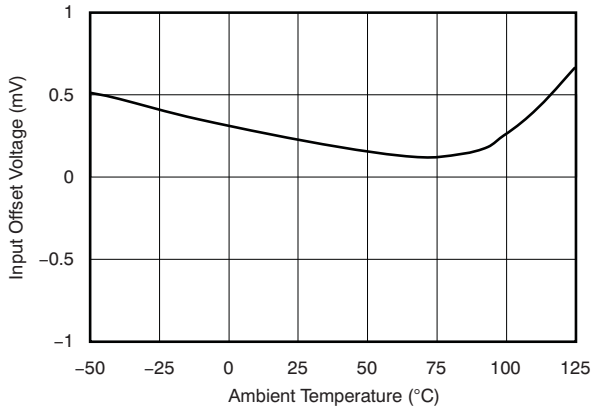


Figure 19. Typical Input Offset Voltage Over Temperature

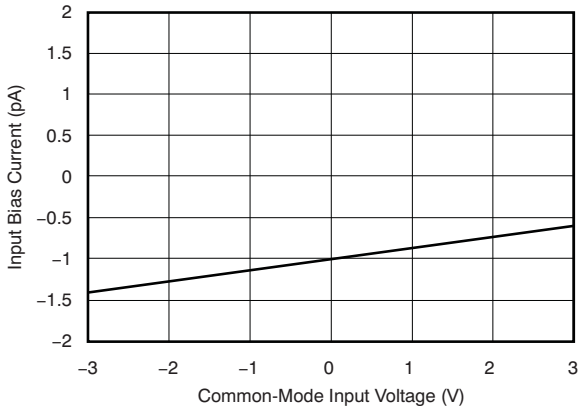


Figure 20. Typical Input Bias Current vs Common-Mode Input Voltage

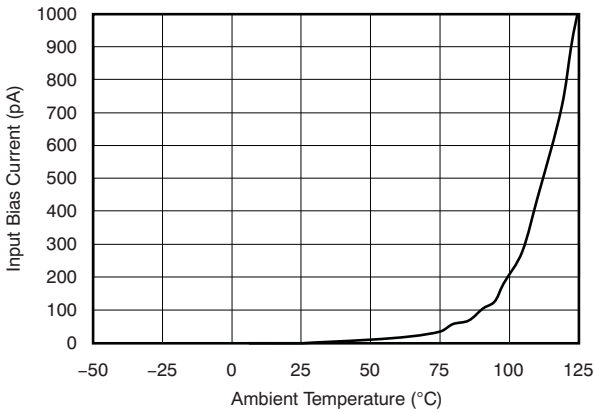


Figure 21. Typical Input Bias Current Over Temperature

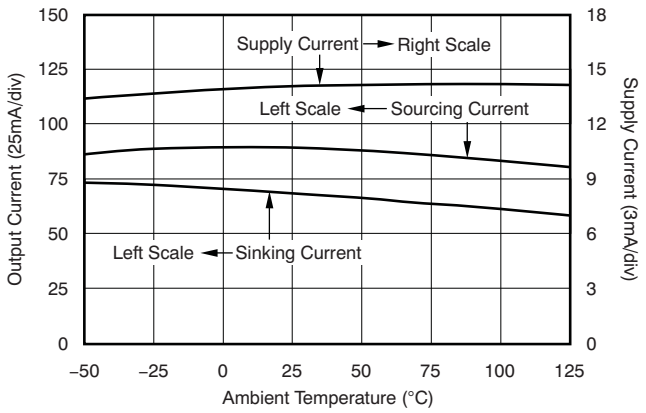


Figure 22. Supply And Output Current vs Temperature

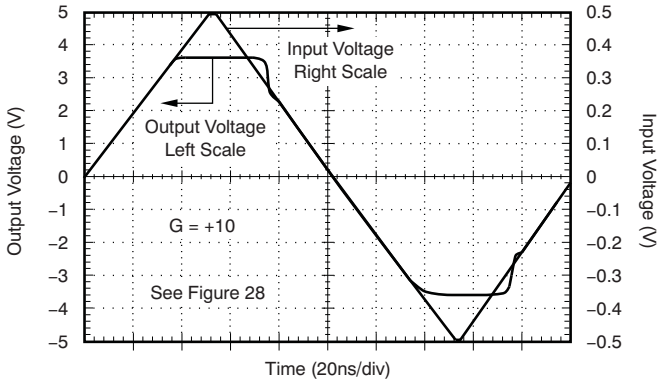


Figure 23. Noninverting Input Overdrive Recovery

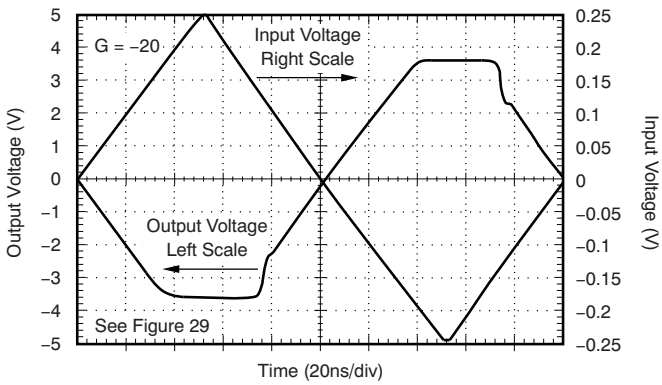


Figure 24. Inverting Input Overdrive Recovery

Typical Characteristics: V_S = ±5 V (continued)

At T_A = 25°C, G = 10 V/V, R_F = 453 Ω, and R_L = 100 Ω, unless otherwise noted.

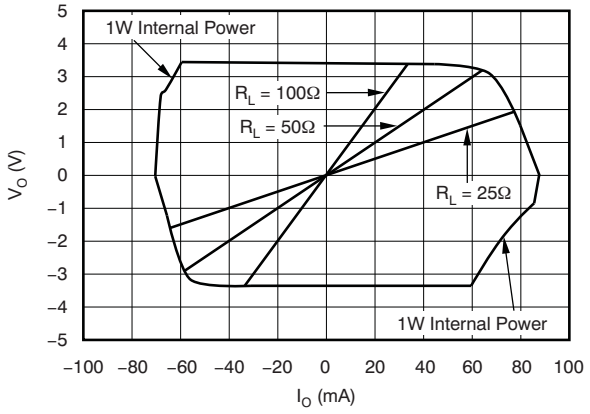


Figure 25. Output Voltage and Current Limitations

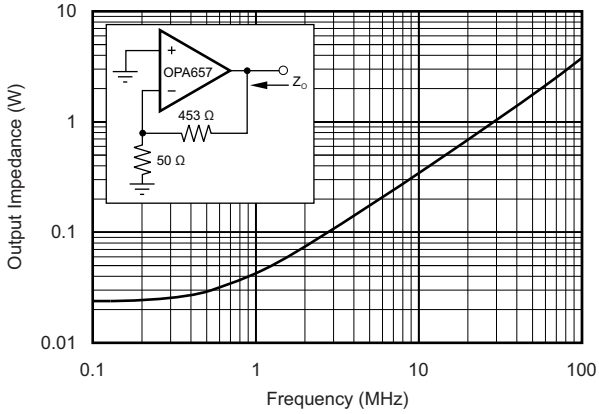


Figure 26. Closed-Loop Output Impedance vs Frequency

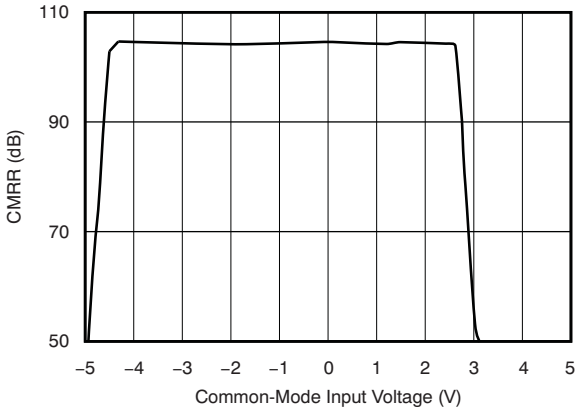


Figure 27. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

8 Detailed Description

8.1 Overview

The OPA657 is high gain-bandwidth, voltage feedback operational amplifier featuring a low noise JFET input stage. The OPA657 has been decompensated to allow for optimized Bandwidth to Quiescent current performance and better optimize its voltage noise performance. The OPA657 finds wide use in optical front-end applications and in test and measurement systems that require high input impedance. It is built using a very high speed complementary bipolar process.

8.2 Feature Description

8.2.1 Input and ESD Protection

The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 28.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (that is, in systems with ±12-V supply parts driving into the OPA657), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

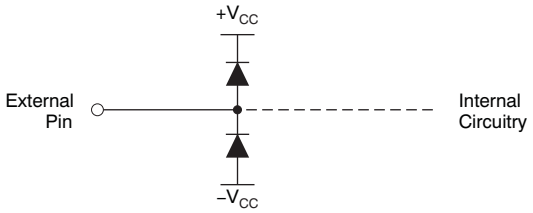


Figure 28. Internal ESD Protection

8.3 Device Functional Modes

8.3.1 Split-Supply Operation (±4-V to ±6-V)

To facilitate testing with common lab equipment, the OPA657 may be configured to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground. Figure 29 and Figure 30 show the OPA657 configured in a simple noninverting and inverting configuration respectively with ±5-V supplies. The input and output will swing symmetrically around ground. Due to its ease of use, split-supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.

8.3.2 Single-Supply Operation (8-V to 12-V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA657 is designed for use with split-supply configuration; however, it can be used with a single-supply with no change in performance, as long as the input and output are biased within the linear operation of the device. To change the circuit from split supply to single supply, level shift all the voltages by 1/2 the difference between the power supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of -PSRR will be minimized because the low supply rail has been grounded.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Wideband, Noninverting Operation

The OPA657 provides a unique combination of low-input voltage noise, very high-gain bandwidth, and the DC precision of a trimmed JFET-input stage to give an exceptional high input impedance, high-gain stage amplifier. Its very high gain bandwidth product (GBP) can be used to either deliver high-signal bandwidths at high gains, or to extend the achievable bandwidth or gain in photodiode-transimpedance applications. To achieve the full performance of the OPA657, careful attention to printed circuit board (PCB) layout and component selection is required as discussed in the following sections of this data sheet.

Figure 29 shows the noninverting gain of +10-V/V circuit used as the basis for most of the *Typical Characteristics: V_S = ±5 V*. Most of the curves are characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 29, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 29) while output power specifications are at the matched 50-Ω load. The total 100-Ω load at the output combined with the 500-Ω total feedback network load presents the OPA657 with an effective output load of 83 Ω for the circuit of Figure 29.

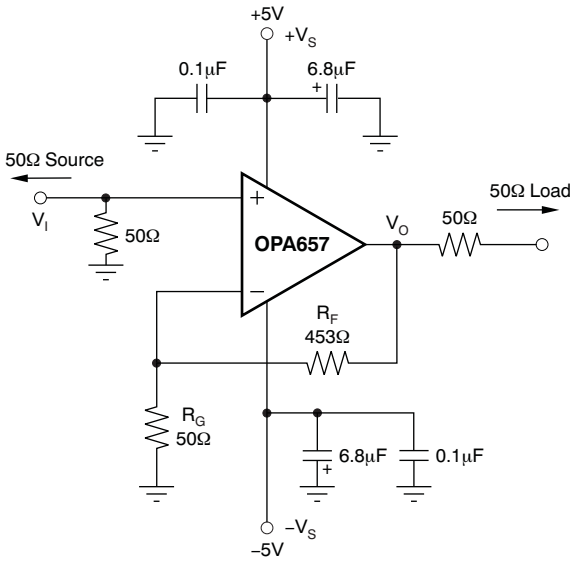


Figure 29. Noninverting G = +10 V/V Specifications and Test Circuit

Voltage-feedback operational amplifiers, unlike current-feedback amplifiers, can use a wide range of resistor values to set the gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 29, the parallel combination of R_F || R_G should always be less than 150 Ω. In the noninverting configuration, the parallel combination of R_F || R_G forms a pole with the parasitic input capacitance at the inverting node of the OPA657 (including layout parasitics). For best performance, this pole should be at a frequency greater than the closed-loop bandwidth for the OPA657. For lower noninverting gains than the minimum recommended gain of +7 for the OPA657, consider the unity-gain stable JFET input OPA656 or high slew rate, low gain stable OPA659.

Application Information (continued)

9.1.2 Wideband, Inverting Gain Operation

There can be significant benefits to operating the OPA657 as an inverting amplifier. This is particularly true when a matched input impedance is required. Figure 30 shows the inverting gain circuit used as a starting point for the Typical Characteristics showing inverting-mode performance.

Driving this circuit from a 50-Ω source, and constraining the gain resistor (R_G) to equal 50 Ω gives both a signal bandwidth and noise advantage. R_G in this case is acting as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain for the circuit of Figure 30 is double that for Figure 29, the noise gains are equal when the 50-Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP for the amplifier. This can be seen in comparing the G = +10 V/V and G = –20 V/V small-signal frequency response curves. Both show about 250-MHz bandwidth, but the inverting configuration of Figure 30 is giving 6-dB higher signal gain. If the signal source is actually the low-impedance output of another amplifier, R_G should be increased to the minimum value allowed at the output of that amplifier and R_F adjusted to get the desired gain. It is critical for stable operation of the OPA657 that this driving amplifier show a very low output impedance through frequencies exceeding the expected closed-loop bandwidth for the OPA657.

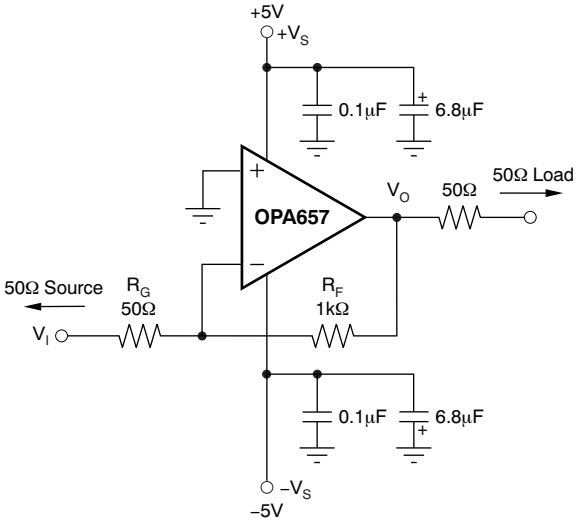


Figure 30. Inverting G = –20 V/V Specifications and Test Circuit

Figure 30 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the DC errors caused by the input bias currents. This is only useful when the input bias currents are matched. For a JFET part like the OPA657, the input bias currents do not match but are so low to begin with (< 5 pA) that DC errors as a result of input bias currents are negligible. Hence, no resistor is recommended at the noninverting input for the inverting signal gain condition.

9.1.3 Low-Gain Compensation

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA657 while maintaining the increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability while giving an easily-controlled second-order low-pass frequency response. Considering only the noise gain for the circuit of Figure 31, the low-frequency noise gain, (NG_1) is set by the resistor ratios while the high frequency noise gain (NG_2) is set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the operational amplifier and the noise gain pole, set by $1/R_FC_F$, is placed correctly, a very well controlled second-order low-pass frequency response results.

Application Information (continued)

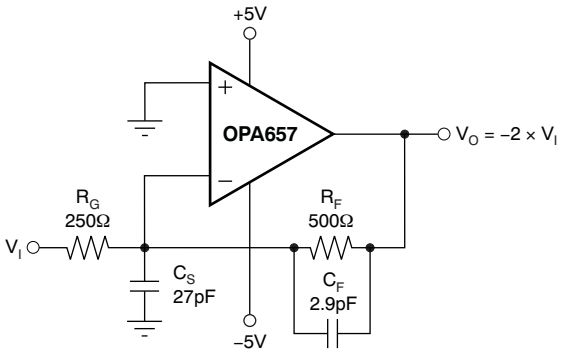


Figure 31. Broadband Low-Gain Inverting External Compensation

To choose the values for both C_S and C_F, two parameters and only three equations must be solved. The first parameter is the target high-frequency noise gain NG_2, which should be greater than the minimum stable gain for the OPA657. Here, a target NG_2 of 10.5 V/V is used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain NG_1. To simplify this discussion, target a maximally-flat second-order low-pass Butterworth frequency response (Q = 0.707). The signal gain of –2 V/V shown in Figure 31 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 3 in this example). Then, using only these two gains and the GBP for the OPA657 (1600 MHz), the key frequency in the compensation can be determined as:

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1 - \frac{NG_1}{NG_2}\right) - \sqrt{1 - 2\frac{NG_1}{NG_2}}\right] \quad (1)$$

Physically, this Z_O (10.6 MHz for the values shown above) is set by $1/(2\pi \times R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0-dB gain. The actual zero in the noise gain occurs at $NG_1 \times Z_O$ and the pole in the noise gain occurs at $NG_2 \times Z_O$. Because GBP is expressed in Hz, multiply Z_O by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi \times R_F Z_O NG_2} \qquad (= 2.86pF) \quad (2)$$

Finally, because C_S and C_F set the high-frequency noise gain, determine C_S by using [$NG_2 = 10.5$]:

$$C_S = (NG_2 - 1)C_F \qquad (= 27.2pF) \quad (3)$$

The resulting closed-loop bandwidth is approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_O\, GBP} \qquad (= 130MHz) \quad (4)$$

For the values shown in Figure 31, the $f_{-3\ dB}$ is approximately 130 MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \times Z_O$. The capacitor values shown in Figure 31 are calculated for $NG_1 = 3$ and $NG_2 = 10.5$ with no adjustment for parasitics.

Figure 32 shows the gain of –2 V/V (6 dB) measured frequency response for the circuit of Figure 31. The amplifier displays exceptional gain flatness through 70 MHz and a –3-dB bandwidth of 170 MHz.

Application Information (continued)

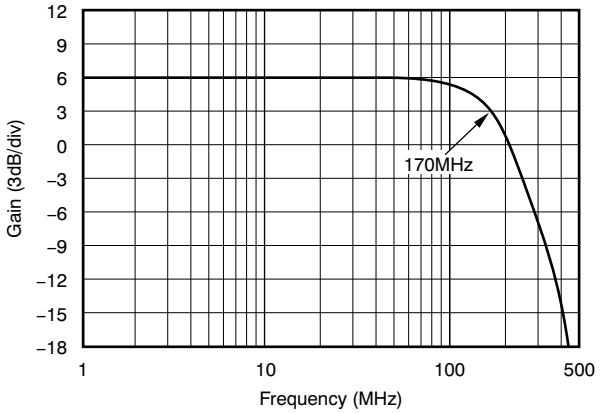


Figure 32. G = –2 Frequency Response With External Compensation

The real benefit to this compensation is to allow a high slew rate, exceptional DC precision operational amplifier to provide a low overshoot, fast settling pulse response. For a 1-V output step, the 700-V/µs slew rate of the OPA657 allows a rise time limited edge rate (2ns for a 170-MHz bandwidth). While unity-gain stable operational amplifiers may offer comparable bandwidths, the lower slew rates extend the settling time for larger steps. For instance, the OPA656 can also provide a 150-MHz gain of –2-V/V bandwidth implying a 2.3-ns transition time. However, the lower slew rate of this unity-gain stable amplifier (290 V/µs) limits a 1-V step transition to 3.5 ns and delays the settling time as the slewing transition is recovered. The combination of higher slew rate and exceptional DC precision for the OPA657 can yield one of the fastest, most precise, pulse amplifiers using the circuit of Figure 31.

An added benefit to the compensation of Figure 31 is to increase the loop gain above that achievable at comparable gains by internally-compensated amplifiers. The circuit of Figure 31 has lower harmonic distortion through 10 MHz than the OPA656 operated at a gain of –2 V/V.

9.1.4 Operating Suggestions

9.1.4.1 Setting Resistor Values to Minimize Noise

The OPA657 provides a very low input noise voltage while requiring a low 14 mA of quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 33 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

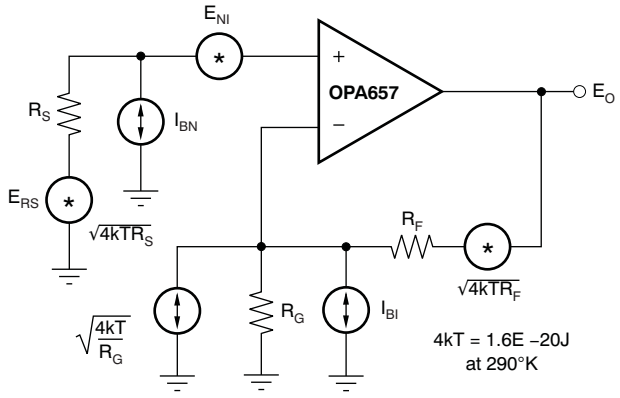


Figure 33. Operational Amplifier Noise Analysis Model

Application Information (continued)

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 5 shows the general form for this output noise voltage using the terms shown in Figure 28:

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right] NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (5)$$

Dividing this expression by the noise gain ($G_N = 1 + R_F/R_G$) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 6:

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Putting high resistor values into Equation 6 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 1.6 kΩ adds a Johnson voltage noise term equal to just that for the amplifier itself (5 nV/√Hz). While the JFET input of the OPA657 is ideal for high source impedance applications, both the overall bandwidth and noise may be limited by these higher source impedances in the noninverting configuration of Figure 29.

9.1.4.2 Frequency Response Control

Voltage-feedback operational amplifiers exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the *Electrical Characteristics: V_S = ±5 V*. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most high-speed amplifiers exhibit a more complex response with lower phase margin. The OPA657 is compensated to give a maximally-flat, second-order, Butterworth, closed-loop response at a noninverting gain of +10 V/V (see Figure 29). This results in a typical gain of +10-V/V bandwidth of 275 MHz, far exceeding that predicted by dividing the 1600-MHz GBP by 10. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +50 V/V the OPA657 shows the 32-MHz bandwidth predicted using the simple formula and the typical GBP of 1600 MHz. Inverting operation offers some interesting opportunities to increase the available gain-bandwidth product. When the source impedance is matched by the gain resistor (see Figure 30), the signal gain is $-(R_F/R_G)$ while the noise gain for bandwidth purposes is $(1 + R_F/R_G)$. This cuts the noise gain in half, increasing the minimum stable gain for inverting operation under these conditions to –12 V/V and the equivalent gain bandwidth product to 3.2 GHz.

9.1.4.3 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an operational amplifier is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier such as the OPA657 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

Application Information (continued)

The Typical Characteristics illustrate the Recommended R_S vs Capacitive Load (Figure 17) and the resulting frequency response at the load. In this case, a design target of a maximally-flat frequency response is used. Lower values of R_S may be used if some peaking can be tolerated. Also, operating at higher gains (than the +10 V/V used in the Typical Characteristics) require lower values of R_S for a minimally-peaked frequency response. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA657. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA657 output pin (see the *Layout Guidelines* section).

9.1.4.4 Distortion Performance

The OPA657 is capable of delivering a low-distortion signal at high frequencies over a wide range of gains. The distortion plots in the *Typical Characteristics: V_S = ±5 V* show the typical distortion under a wide variety of conditions.

Generally, until the fundamental signal reaches very high frequencies or powers, the second-harmonic dominates the distortion with a negligible third-harmonic component. Focusing then on the second-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is sum of R_F + R_G, while in the inverting configuration this is just R_F (see Figure 29). Increasing output voltage swing increases harmonic distortion directly. A 6-dB increase in output swing generally increases the second-harmonic 12 dB and the third-harmonic 18 dB. Increasing the signal gain also increases the second-harmonic distortion. Again, a 6-dB increase in gain increases the second- and third-harmonic by approximately 6 dB, even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the roll-off in the loop gain with frequency. Conversely, the distortion improves going to lower frequencies down to the dominant open-loop pole at approximately 100 kHz. Starting from the –70-dBc second-harmonic for a 5-MHz, 2 V_{PP} fundamental into a 200-Ω load at G = +10 V/V (from the *Typical Characteristics: V_S = ±5 V*), the second-harmonic distortion for frequencies lower than 100 kHz is approximately less than –90 dBc.

The OPA657 has an extremely low third-order harmonic distortion. This also shows up in the two-tone, third-order, intermodulation spurious (IM3) response curves. The third-order spurious levels are extremely low (< –80 dBc) at low output power levels. The output stage continues to hold them low even as the fundamental power reaches higher levels. As shown in *Typical Characteristics: V_S = ±5 V*, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 10 MHz, with 4 dBm/tone into a matched 50-Ω load (that is, 1 V_{PP} for each tone at the load, which requires 4 V_{PP} for the overall two-tone envelope at the output pin), the *Typical Characteristics: V_S = ±5 V* show a 82-dBc difference between the test tone and the third-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies and/or higher load impedances.

9.1.4.5 DC Accuracy and Offset Control

The OPA657 can provide excellent DC accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and its trimmed input offset voltage (and drift) along with the negligible errors introduced by the low input bias current. For the best DC precision, a high-grade version (OPA657UB or OPA657NB) screens the key DC parameters to an even tighter limit. Both standard- and high-grade versions take advantage of a new final test technique to 100% test input offset voltage drift over temperature. This discussion uses the high-grade typical and min/max *Electrical Characteristics: V_S = ±5 V* for illustration; however, an identical analysis applies to the standard-grade version.

The total output DC offset voltage in any configuration and temperature is the combination of a number of possible error terms. In a JFET part such as the OPA657, the input bias current terms are typically quite low but are unmatched. Using bias-current cancellation techniques, more typical in bipolar input amplifiers, does not improve output DC offset errors. Errors due to the input bias current only become dominant at elevated temperatures. The OPA657 shows the typical 2× increase in every 10°C common to JFET-input stage amplifiers. Using the 5-pA maximum tested value at +25°C, and a +20°C internal self heating (see thermal analysis), the maximum input bias current at +85°C ambient is 5 pA × $2^{(105 - 25)/10}$ = 1280 pA. For noninverting configurations,

Application Information (continued)

this term only begins to be a significant term versus the input offset voltage for source impedances greater than 750 kΩ. This would also be the feedback resistor value for transimpedance applications (see Figure 34) where the output DC error due to inverting input bias current is on the order of that contributed by the input offset voltage. In general, except for these extremely high-impedance values, the output DC errors due to the input bias current may be neglected.

After the input offset voltage itself, the most significant term contributing to output offset voltage is the PSRR for the negative supply. This term is modeled as an input offset voltage shift due to changes in the negative power-supply voltage (and similarly for the +PSRR). The high-grade test limit for –PSRR is 68 dB. This translates into 0.4-mV/V input offset voltage shift = $10^{(-68/20)}$. This low sensitivity to the negative supply voltage requires a 1.5-V change in the negative supply to match the ±0.6mV input offset voltage error. The +PSRR is tested to a minimum value of 78 dB. This translates into $10^{(-78/20)}$ = 0.125 mV/V sensitivity for the input offset voltage to positive power-supply changes.

As an example, compute the worst-case output DC error for the transimpedance circuit of Figure 34 at 25°C and then the shift over the 0°C to 70°C range given the following assumptions.

Negative Power Supply

= –5 V ±0.2 V with a ±5 mV/°C worst-case shift

Positive Power Supply

= +5 V ±0.2 V with a ±5 mV/°C worst-case shift

Initial 25°C Output DC Error Band

= ±0.6 mV (OPA657 high-grade input offset voltage limit)

±0.08 mV (due to the –PSRR = 0.4 mV/V × ±0.2 V)

±0.04 mV (due to the +PSRR = 0.2 mV/V × ±0.2 V)

Total = ±0.72mV

This would be the worst-case error band in volume production at 25°C acceptance testing given the conditions stated. Over the temperature range (0°C to 70°C), expect the following worst-case shifting from initial value. A 20°C internal junction self-heating is assumed here.

±0.36 mV (OPA657 high-grade input offset drift)

= ±6 µV/°C × (70°C + 20°C – 25°C)

±0.11 mV (–PSRR of 66dB with 5mV × (70°C – 25°C) supply shift)

±0.04 mV (+PSRR of 76dB with 5mV × (70°C – 25°C) supply shift)

Total = ±0.51mV

This would be the worst-case shift from an initial offset over a 0°C to 70°C ambient for the conditions stated. Typical initial output DC error bands and shifts over temperature are much lower than these worst-case estimates.

In the transimpedance configuration, the CMRR errors can be neglected because the input common-mode voltage is held at ground. For noninverting gain configurations (see Figure 29), the CMRR term needs to be considered but is typically far lower than the input offset voltage term. With a tested minimum of 91 dB (28 µV/V), the added apparent DC error is no more than ±0.06 mV for a ±2-V input swing to the circuit of Figure 29.

9.2 Typical Application

The high GBP and low input voltage and current noise for the OPA657 make it an ideal wideband transimpedance amplifier for moderate to high transimpedance gains. Unity-gain stability in the operational amplifier is not required for application as a transimpedance amplifier.

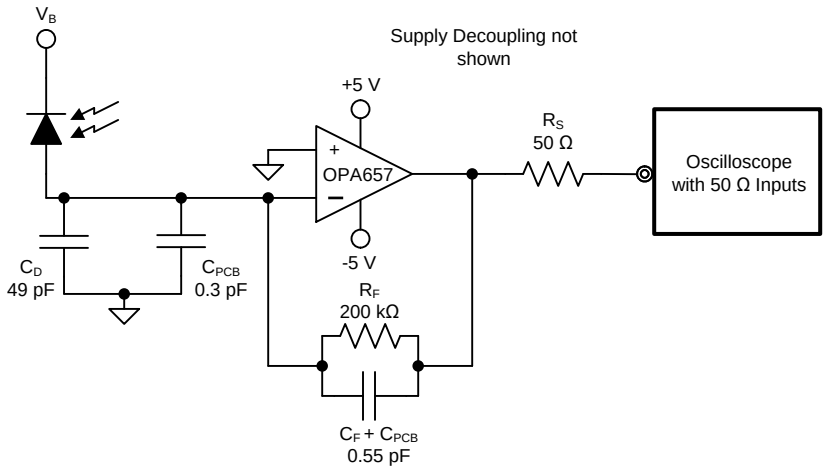


Figure 34. Wideband, High-Sensitivity, Transimpedance Amplifier Diagram

9.2.1 Design Requirements

Design a high-bandwidth, high-gain transimpedance amplifier with the design requirements shown in Table 1.

Table 1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)
1	200	49

9.2.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA657. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_B) applied, the desired transimpedance gain, R_F, and the GBP for the OPA657 (1600 MHz). Figure 34 shows a transimpedance circuit with the parameters as described in Table 1. With these three variables set (and including the parasitic input capacitance for the OPA657 and the PCB added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response. To achieve a maximally-flat second-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{7}$$

Adding the common-mode and differential mode input capacitance (0.7 + 4.5) pF and the trace PCB capacitance of approximately 0.3 pF to the 49-pF diode source capacitance of Figure 34, and targeting a 200-kΩ transimpedance gain using the 1600-MHz GBP for the OPA657 requires a feedback pole set to 3.5 MHz. This requires a total feedback capacitance of 0.2 pF. Such low capacitance values are difficult to achieve due to parasitics from the PCB and the surface mount components.

Equation 8 gives the approximate closed loop bandwidth of the system to be 4.8 MHz. Because the target bandwidth is only 1 MHz, the feedback capacitance can be increased to a more practical value while maintaining the bandwidth requirements of the design. A feedback capacitance of 0.550 pf was chosen. This includes the physical 0.4-pF feedback capacitor in addition to the 0.1-pF parasitic capacitance from the feedback resistor and around 50-fF capacitance from the PCB traces. Removing the ground and power planes from under the surface mount components helps to minimize this parasitic capacitance. The simulated closed loop bandwidth of Figure 34 was 1.7 MHz. The phase margin was close to 82°. This design should result in a system with negligible overshoot to a pulsed input.

$$f_{-3dB} = \sqrt{GBP / (2\pi R_F C_D)}\ Hz \tag{8}$$

Figure 35 shows the measured output noise of the system which matches the simulated output noise in Figure 36 very closely. The low-frequency output noise of 60 nV/√Hz gets input-referred to 0.3 pA/√Hz. The transimpedance gain resistor is the dominant noise source with the operational amplifier itself contributing a negligible amount, reflecting one of the main benefits in using a JFET input amplifier in a high-gain transimpedance application. If the total output noise of the TIA is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent output noise voltage can be derived as: see Equation 9. Figure 37 shows the measured pulse response to a 5-µA input current pulse. The output voltage measured on the scope is 0.5 V because of the 50-Ω termination to the scope.

$$V_{OUTN} = \sqrt{(I_N R_F)^2 + 4kTR_F + {E_N}^2 + \frac{(E_N 2\pi C_D R_F F)^2}{3}} \tag{9}$$

where

- V_{OUTN} = Equivalent output noise when band limited to F < 1 / (2ΩRfCf)
- I_N = Input current noise for the operational amplifier inverting input
- E_N = Input voltage noise for the operational amplifier
- C_D = Diode capacitance including operational amplifier and PCB parasitic capacitance
- F = Band-limiting frequency in Hz (usually a postfilter before further signal processing)
- 4 kT = 1.6 e – 20 J at T = 290°K

9.2.3 Application Curves

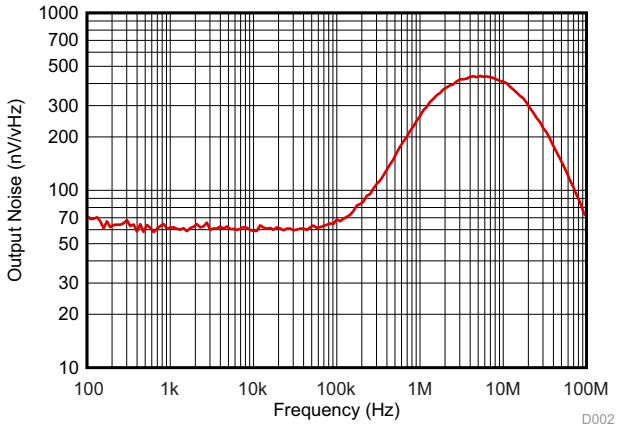


Figure 35. Measured Total TIA Noise

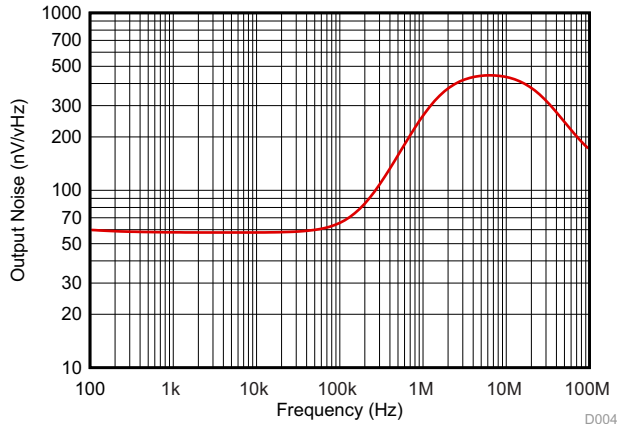


Figure 36. Simulated TIA Output Noise

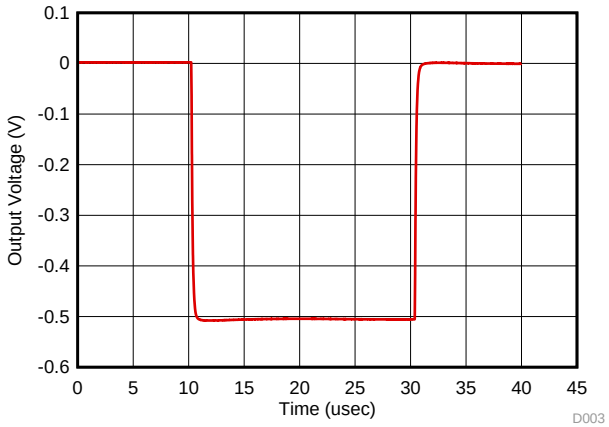


Figure 37. Transient Pulse Response to 5-µA Input Current Pulse

10 Power Supply Recommendations

The OPA657 is principally intended to work in a supply range of ±4 V to ±6 V. Good power-supply bypassing is required. Minimize the distance (<0.1 inch) from the power-supply pins to high frequency, 0.1-µF decoupling capacitors. Often a larger capacitor (2.2 µF is typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second harmonic distortion performance.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA657 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high-frequency performance of the OPA657.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 1.5 kΩ, this parasitic capacitance can add a pole and/or zero below 500 MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be to keep $R_F \parallel R_G < 150\ \Omega$ for voltage amplifier applications. Doing this automatically keeps the resistor noise terms low, and minimizes the effect of the parasitic capacitance. Transimpedance applications (see Figure 34) can use whatever feedback resistor is required by the application as long as the feedback-compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 17). Low parasitic capacitive loads (< 5 pF) may not need an R_S because the OPA657 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques

Layout Guidelines (continued)

(consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA657 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device—this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high-speed part like the OPA657 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA657 onto the board.

11.1.1 Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA657 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 2.

Table 2. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA657U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA657N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments website (www.ti.com) through the OPA657 product folder.

11.2 Layout Example

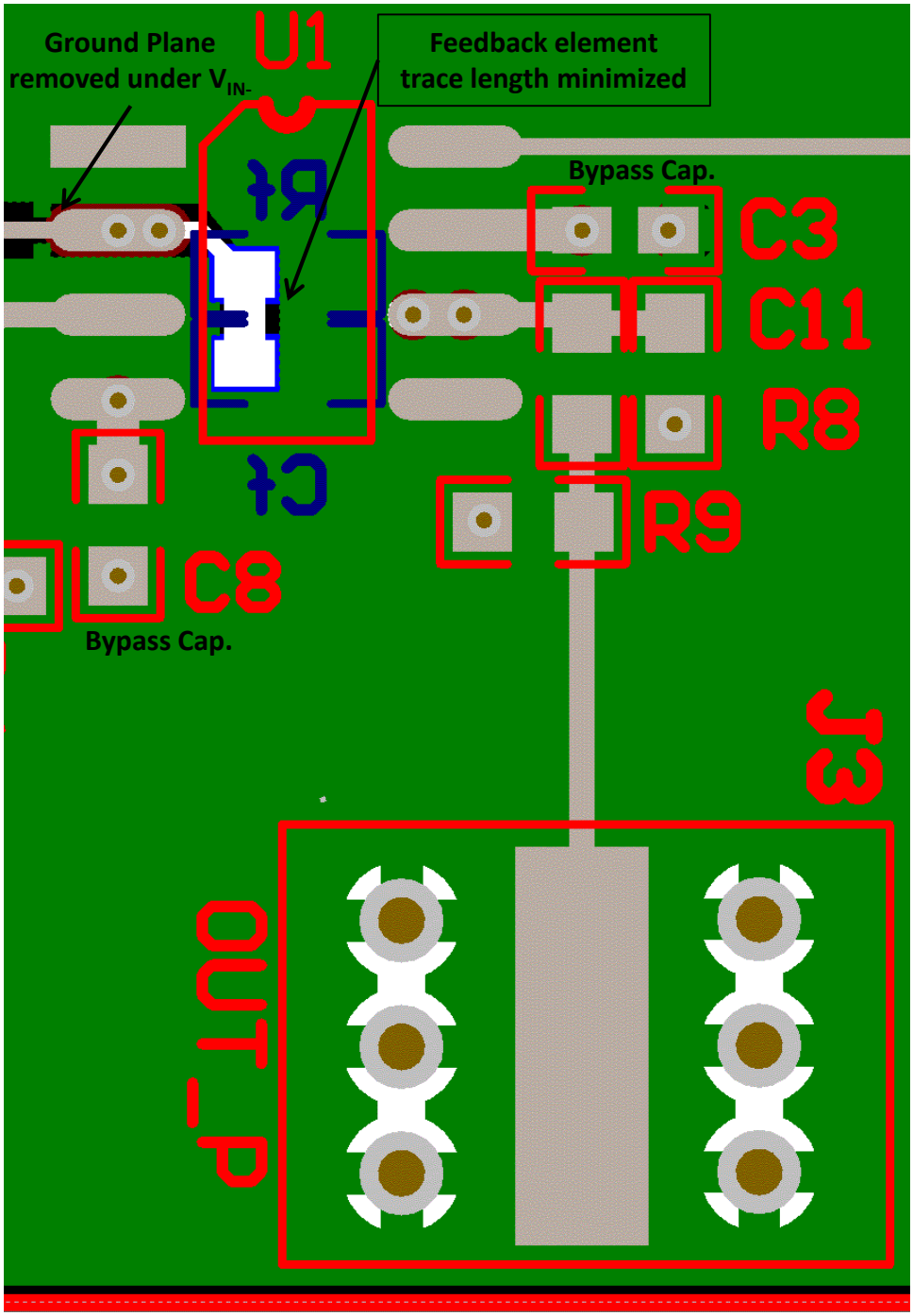


Figure 38. Layout Recommendation

11.3 Thermal Considerations

The OPA657 does not require heatsinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Thermal Considerations (continued)

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but will—for a grounded resistive load—be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S\ 2\ /\ (4 \times R_L)$ where R_L includes feedback network loading.

It is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA657N (SOT23-5 package) in the circuit of Figure 29 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100-Ω load.

$$P_D = 10V \times 16.1mA + 5^2/(4 \times (100\Omega||500\Omega)) = 236mW \quad (10)$$

$$\text{Maximum } T_J = +85°C + (0.25W \times 150°C/W) = 121°C \quad (11)$$

All actual applications are operating at lower internal power and junction temperature.

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA657N/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A57
OPA657N/250.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A57
OPA657NB/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A57
OPA657NB/250.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A57
OPA657NB/250G4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
OPA657U	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U
OPA657U.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U
OPA657U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U
OPA657U/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U
OPA657UB	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U B
OPA657UB.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 657U B
OPA657UBG4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA657UG4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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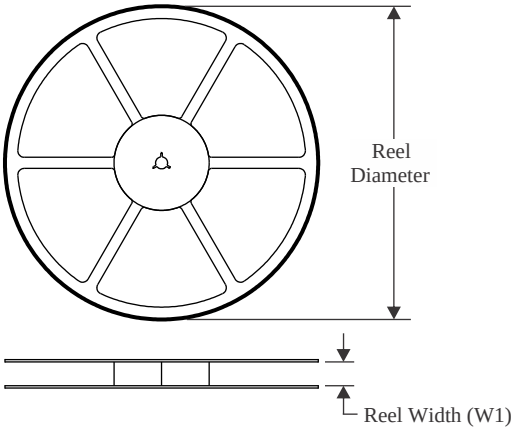
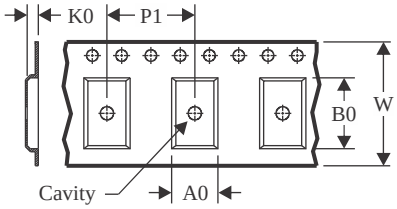
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

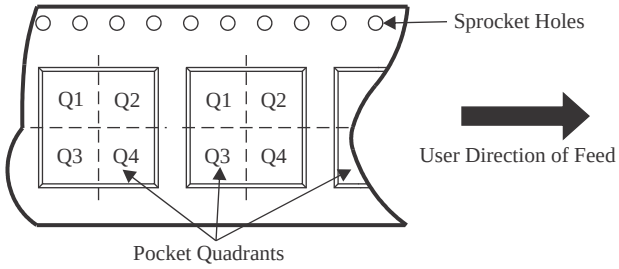


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

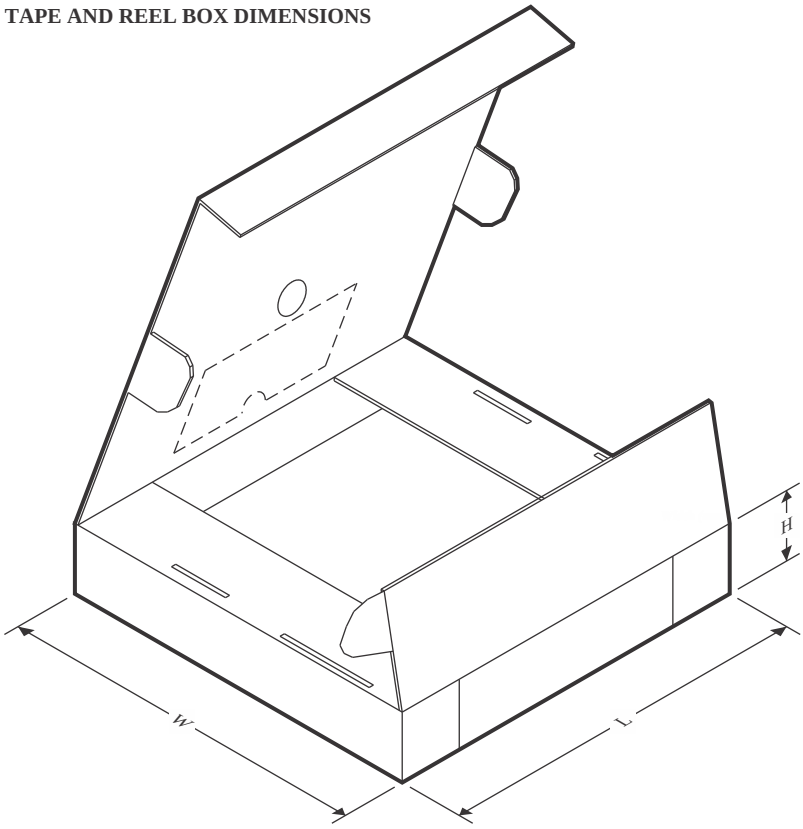
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA657N/250	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA657NB/250	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA657U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

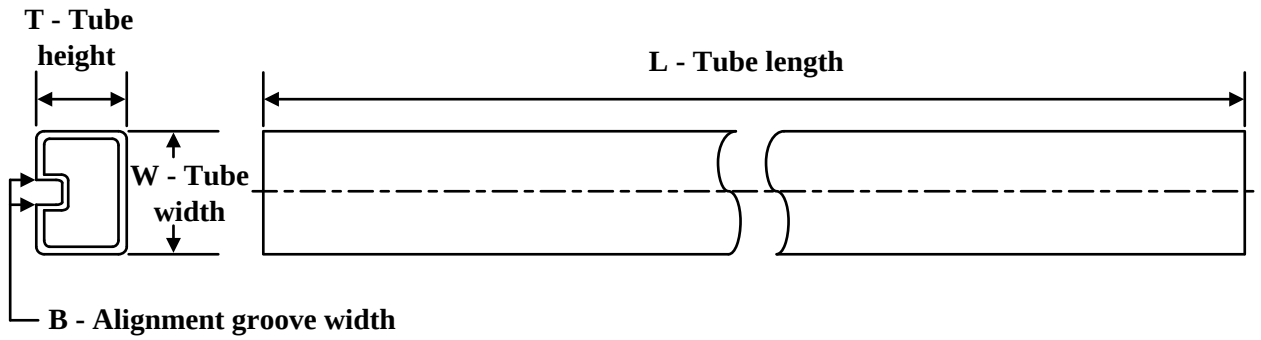
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA657N/250	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA657NB/250	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA657U/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

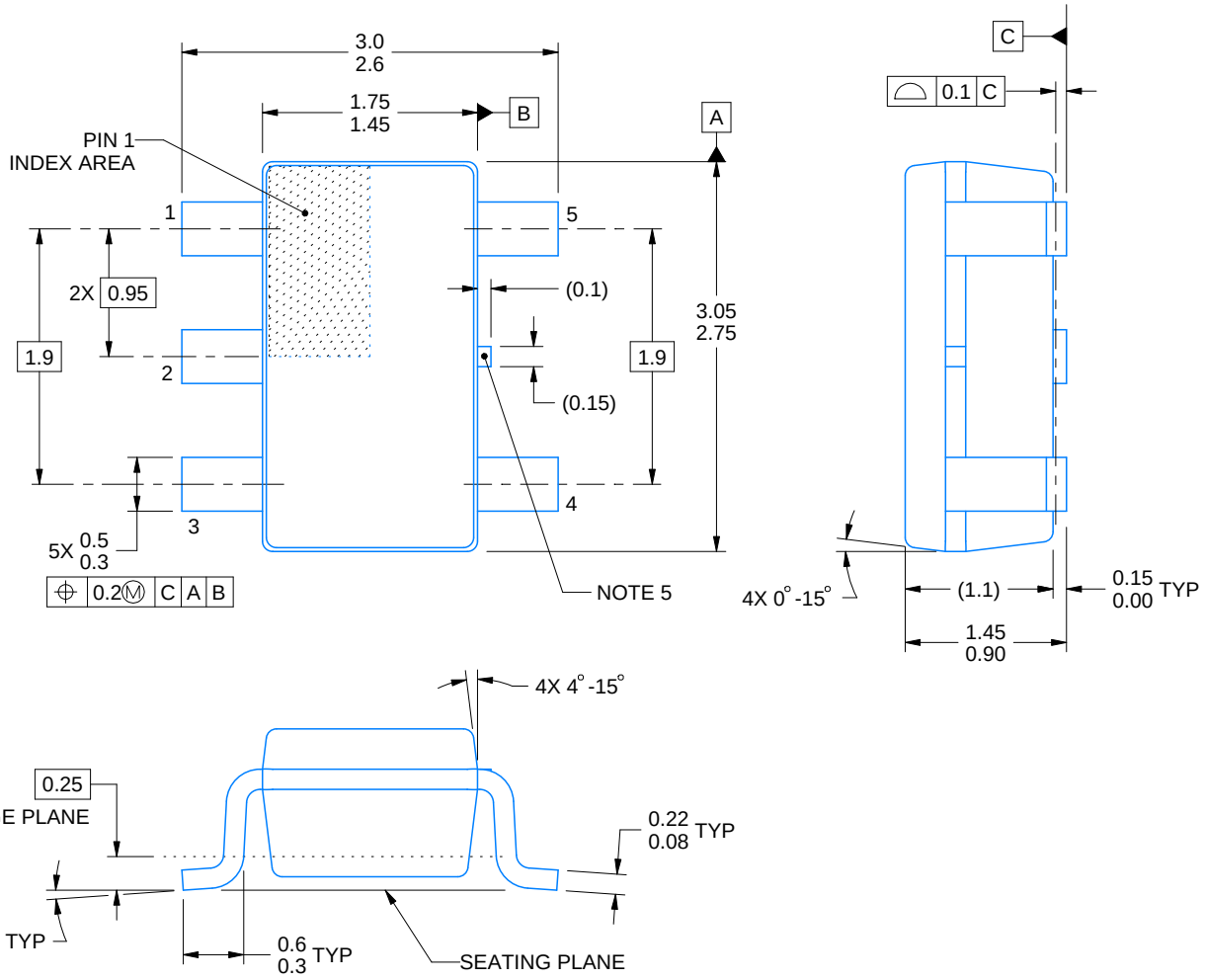
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA657U	D	SOIC	8	75	506.6	8	3940	4.32
OPA657U.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA657UB	D	SOIC	8	75	506.6	8	3940	4.32
OPA657UB.A	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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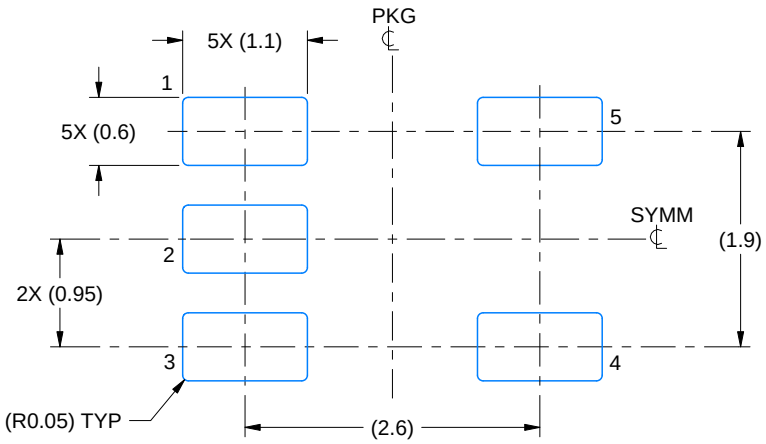
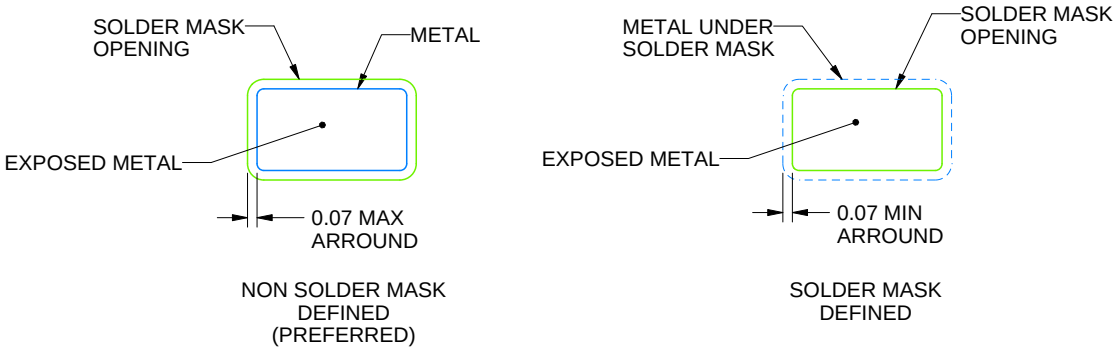
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

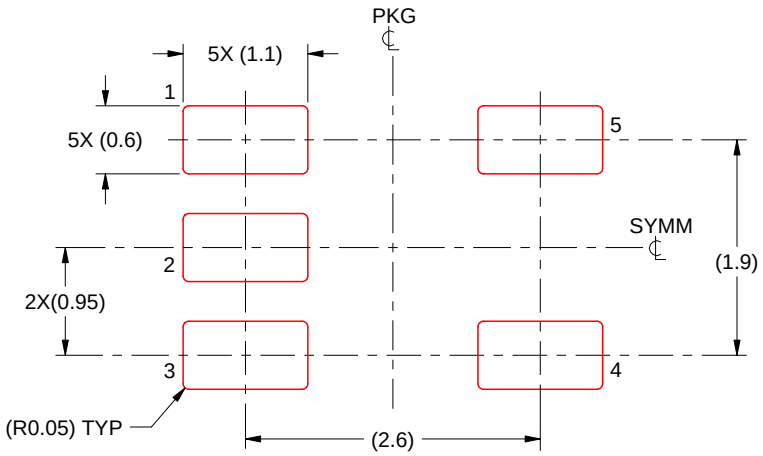


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

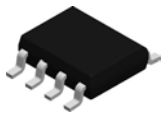


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

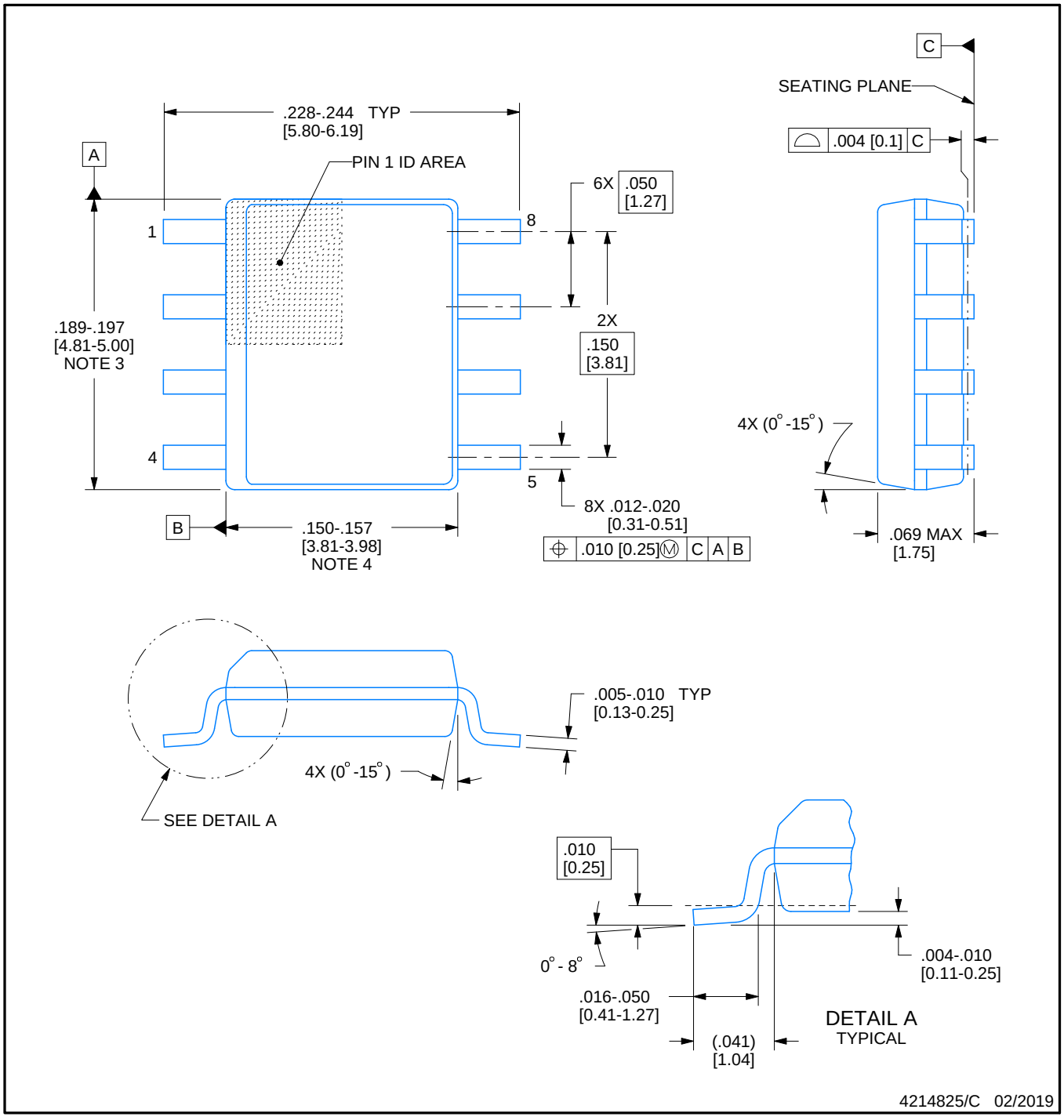


PACKAGE OUTLINE

D0008A

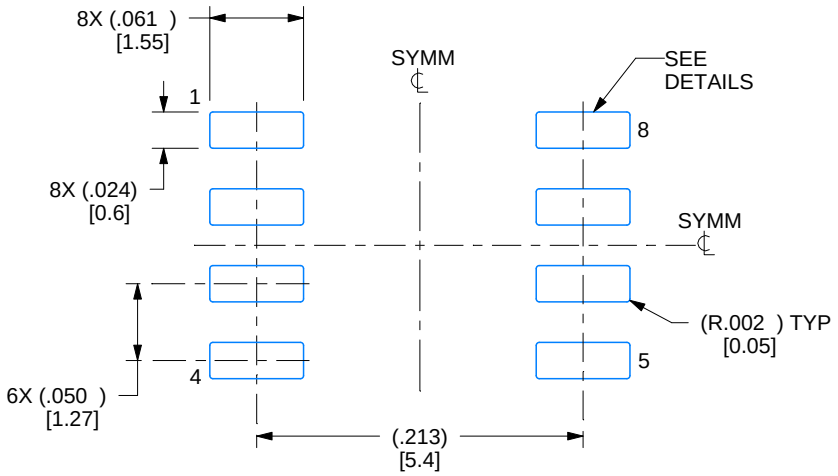
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

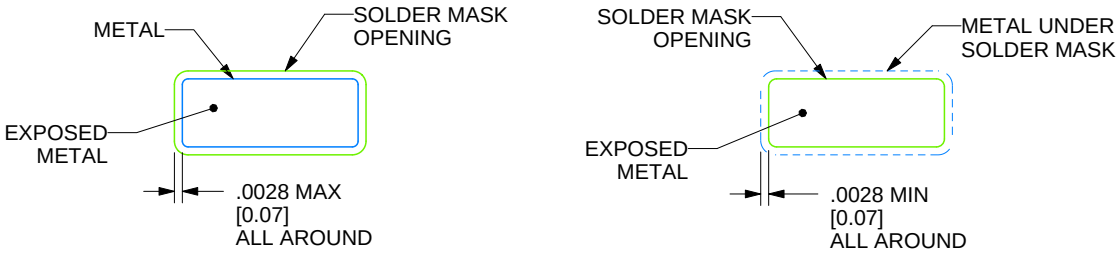


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

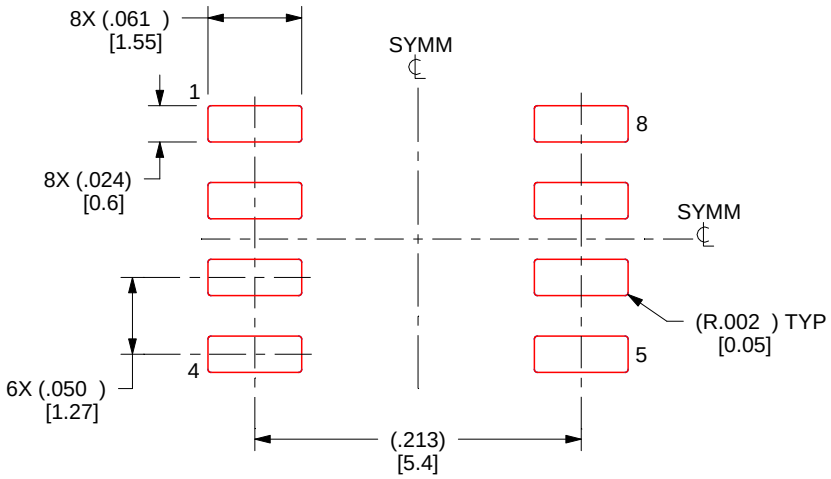
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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