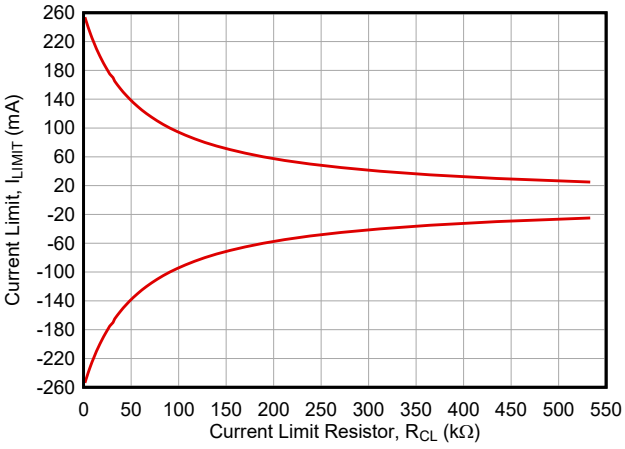
OPA593 85V、出力電流 250mA、高精度パワー・オペアンプ

1 特長

- 広い電源電圧範囲:
  - 8V (±4V) から 85V (±42.5V)
- 低いオフセット電圧:±20µV
- 低い入力オフセット電圧ドリフト:±0.4µV/℃
- 大出力電流:250mA
- 広いゲイン帯域幅:10MHz
- 高いスルーレート:45V/µs、立ち上がり
- 低ノイズ:10kHz において 7nV/√Hz
- MUX 対応入力
- レール・ツー・レール出力
- 静止電流:
  - イネーブル時:3.25mA
  - ディスエーブル時:250µA
- 指定可能な電流制限精度
- 過熱フラグおよび過電流フラグ
- 温度範囲:-40℃～+125℃
- パッケージ:12 ピン WSON

2 アプリケーション

- 半導体テスト
- 半導体製造
- プログラマブル DC 電源
- LCD テスト
- CT および PET スキャナ



出力電流と電流制限抵抗の構成

3 概要

OPA593 は高電圧 (85V)、高精度、広帯域 (10MHz)、大出力電流 (250mA) の、安定したユニティ・ゲインを持つパワー・オペアンプです。

OPA593 では、レーザー・トリミング技術によりオフセット電圧 (20µV、標準値) とオフセット電圧ドリフト (0.4µV/℃、標準値) を改善することで、キャリブレーションを不要にしています。このデバイスは、電源レールまでの差動入力電圧範囲を可能にし、マルチチャネル・システムでのセトリング性能の向上に役立つ、マルチプレクサ対応入力を備えています。

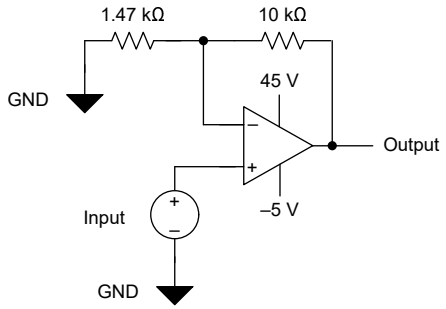
外部抵抗を使用することで、特定の精度で電流を制限できるため、より正確な測定が可能です。過電流状態または過熱状態の場合、デバイスが誤動作をステータス・フラグを使用して示します。内蔵のディスエーブル機能は、デバイスをシャットダウンするために使用し、これにより電力が抑制され、出力は高インピーダンス状態に設定されます。

このデバイスは安定したユニティ・ゲインを持つため、高インピーダンスのバッファとしての動作が可能です。広い帯域幅と高いスルーレートにより、高い信号ゲインを実現できます。このデバイスの大きな出力電流と容量駆動能力は、外付けの電界効果トランジスタ (FET) の駆動を可能にしており、これにより、デジタル電源などの内部でシステムに大電流を供給するために使用できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
OPA593	DNT (WSON, 12)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



8 倍のゲイン構成の出力ドライバ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2022) to Revision C (November 2022)	Page
• 事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

5 Pin Configuration and Functions

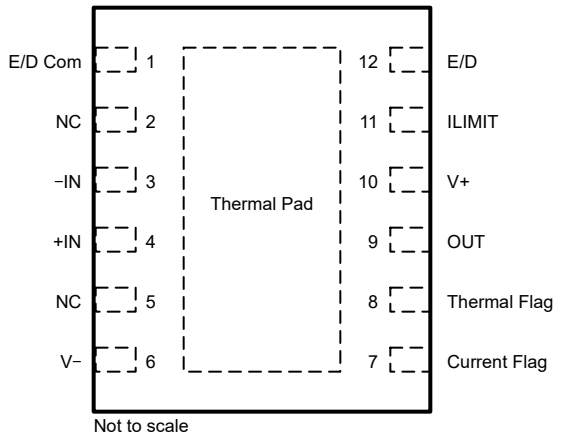


図 5-1. DNT (12-Pin WSON) Package, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Current Flag	7	Output	Overcurrent status flag
E/D	12	Input	Enable and disable
E/D Com	1	Input	Enable and disable common
ILIMIT	11	Input	Current limit
+IN	4	Input	Noninverting input
–IN	3	Input	Inverting input
NC	2, 5	—	No internal connection
OUT	9	Output	Output
Thermal Flag	8	Output	Overtemperature status flag
Thermal Pad	Thermal pad	—	The thermal pad is internally connected to V–. The thermal pad must be soldered to a printed-circuit board (PCB) connected to V–, even with applications that have low power dissipation.
V+	10	Power	Positive (highest) power supply
V–	6	Power	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		93	V
	Signal input pin voltage(2)	(V–) – 0.3	(V+) + 0.3	V
	Status flag and E/D pin voltage(3)		E/D Com + 7	V
	ILIMIT pin voltage	V–	(V–) + 3.35	V
	Status flag pins current(3)		3	mA
	Input current, all pins(2)		±10	mA
	Output short circuit current(4)		Continuous	
T_J	Junction temperature	–55	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input, E/D Com, and output pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to less 10 mA.
(3) Status flag and E/D pins are diode clamped to E/D Com – 0.3 V and E/D Com + 7 V. Pullup signals must be current-limited to < 3 mA.
(4) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply voltage	8		85	V
		Dual supply voltage	±4		±42.5	
$V_{E/D}$	E/D pin voltage(1)				5.5	V
	Status flag pin voltage(1)				5.5	V
I_{LIMIT}	Current limit set		±25		±250	mA
T_A	Operating temperature		–40		125	°C

(1) Recommended voltage must be current limited to below the listed value in the *Absolute Maximum Ratings*.

6.4 Thermal Information

THERMAL METRIC(1)		OPA593 DNT (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For information on traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = 85 V, T_A = 25°C, R_L = 10 kΩ to mid-supply, I_{OUT} limit set to 100 mA, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±20	±100	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.4	±2	µV/°C
PSRR	Power supply rejection ratio	V_S = ±4 V to ±42.5 V			0.1	1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±10	pA
		T_A = –40°C to +85°C				±350	
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±1	±5	pA
		T_A = –40°C to +85°C				±250	
		T_A = –40°C to +125°C				±1	nA
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.9		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			75		nV/√Hz
		f = 1 kHz			10		
		f = 10 kHz			7		
i_n	Current noise density	f = 1 kHz			12		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	Linear operation		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection	(V–) ≤ V_{CM} ≤ (V+) – 3.5 V		124	140		dB
			T_A = –40°C to +125°C	108	124		
INPUT IMPEDANCE							
	Differential				10^{13} || 0.3		Ω || pF
	Common-mode				10^{13} || 9.4		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		134	140		dB
			T_A = –40°C to +125°C	130	140		
		(V–) + 1 V < V_O < (V+) – 1 V, R_L = 2 kΩ		132	140		
			T_A = –40°C to +125°C	130	135		
		(V–) + 2.5 V < V_O < (V+) – 2.5 V, R_L = 600 Ω		130	135		
			T_A = –40°C to +125°C	125	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10		MHz
SR	Slew rate	Gain = ±1, V_{OUT} = 70-V step	Rising		45		V/µs
			Falling		35		
t_S	Settling time	To ±0.01%, gain = –1, V_{OUT} = 70-V step, C_L = 100 pF			2.9		µs
THD+N	Total harmonic distortion + noise	Gain = +1, V_{OUT} = 70 V_{PP}, f = 1 kHz	R_L = 600 Ω		–105		dB
			R_L = 2 kΩ		–110		
OUTPUT							
V_O	Voltage output swing from rail	R_{CL} = 0 Ω connected to V–	No load		10	25	mV
			I_{OUT} = 50 mA		50	125	
			I_{OUT} = 100 mA		400	750	
			I_{OUT} = 250 mA		1.2	2	V

6.5 Electrical Characteristics (continued)

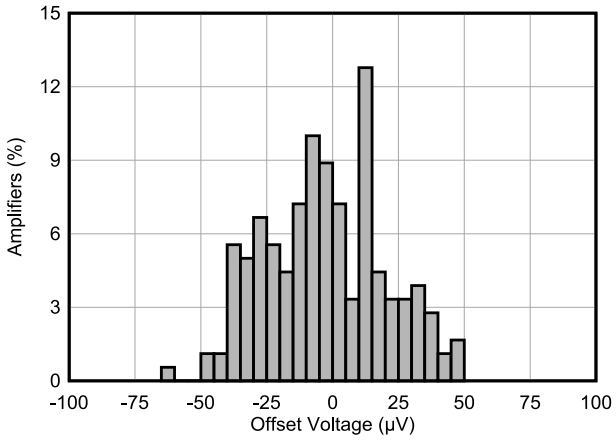
at V_S = 85 V, T_A = 25°C, R_L = 10 kΩ to mid-supply, I_{OUT} limit set to 100 mA, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Continuous output current, dc	V_S = 85 V, R_{CL} = 2.29 kΩ, I_{LIMIT} = 250 mA			±250		mA
C_{LOAD}	Capacitive load drive				See typical curves		pF
Z_O	Open-loop output impedance				See typical curves		Ω
	Output impedance	Output disabled, V– < V_{OUT} < V+			100		MΩ
	Output capacitance	Output disabled			56		pF
CURRENT LIMIT							
I_{LIMIT}	Current limit			±25		±250	mA
	Current limit accuracy(3)	Sourcing, R_L = 10 Ω to mid-supply	I_{LIMIT} = 25 mA, V_{LIMIT} = 3.33 V	17		29	mA
			I_{LIMIT} = 50 mA, V_{LIMIT} = 2.98 V	42		55	
			I_{LIMIT} = 100 mA, V_{LIMIT} = 2.27V	94		107	
			I_{LIMIT} = 250 mA, V_{LIMIT} = 0.14 V	237		263	
		Sinking, R_L = 10 Ω to mid-supply	I_{LIMIT} = 25 mA, V_{LIMIT} = 3.33 V	10		45	
			I_{LIMIT} = 50 mA, V_{LIMIT} = 2.98 V	35		68	
			I_{LIMIT} = 100 mA, V_{LIMIT} = 2.27 V	85		115	
			I_{LIMIT} = 250 mA, V_{LIMIT} = 0.14 V	235		275	
	Current limit equation	Resistor set, R_{CL} connected between ILIMIT pin and V–		(3.687 V × 4000) / (56.7 kΩ + R_{CL})			mA
		Voltage set, V_{LIMIT} connected to ILIMIT pin and referenced to V–		4000 × (3.687 V – V_{LIMIT}) / 56.7 kΩ			
STATUS FLAG PIN (Referenced to E/D Com)							
	Status flag delay	Overcurrent delay			10		µs
		Overcurrent recovery delay			10		
	Thermal shutdown	Alarm (status flag high)			170		°C
		Return to normal operation (status flag low)			150		
	Status flag output voltage	Normal operation			See typical curves		
E/D PIN							
$V_{E/D}$	E/D voltage(1)	Enable, pin open or forced high(2)		E/D Com + 1.5		E/D Com + 5.5	V
		Disable, pin forced low(2)		E/D Com		E/D Com + 0.5	
$I_{E/D}$	E/D input current				50		µA
	Output disable time				12		µs
	Output enable time				18		µs
E/D COM PIN							
	E/D Com voltage			(V–)		(V+) – 6	V
POWER SUPPLY							
I_Q	Quiescent current				3.25	3.75	mA
		T_A = –40°C to +125°C				4	
		Output disabled			0.25		

(1) For information on the output enable and disable feature see セクション 7.3.4.
(2) Enable and disable voltage thresholds can vary near the maximum temperature range; see 図 6-67.
(3) Proper output swing headroom is necessary to maintain current limit accuracy; see 図 6-19. to 図 6-34.

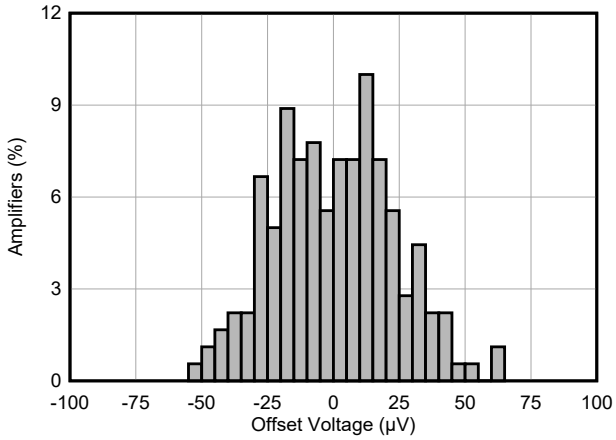
6.6 Typical Characteristics

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



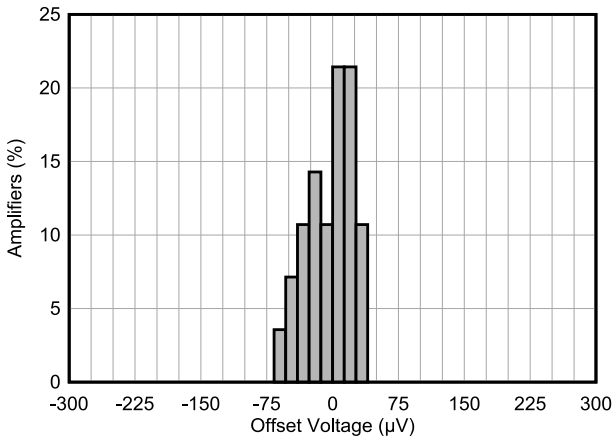
V_S = 85 V, 160 typical units

図 6-1. Input Offset Production Distribution



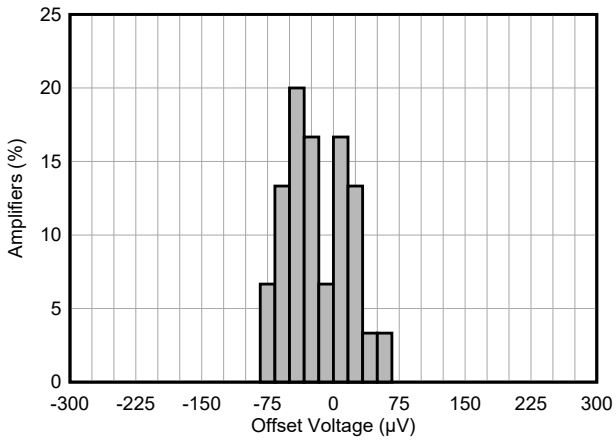
V_S = 8 V, 160 typical units

図 6-2. Input Offset Production Distribution



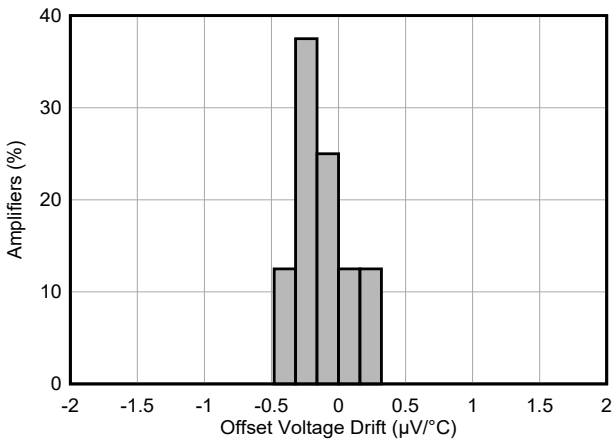
T_A = −40ºC, 30 typical units

図 6-3. Input Offset Production Distribution



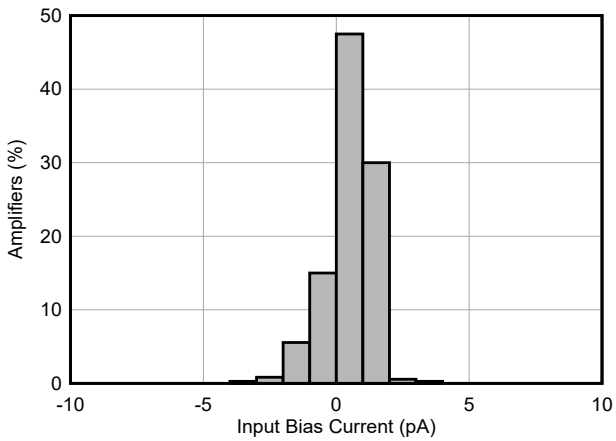
T_A = 125ºC, 30 typical units

図 6-4. Input Offset Production Distribution



T_A = –40ºC to +125ºC

図 6-5. Input Offset Voltage Drift Distribution



360 typical units

図 6-6. Input Bias Current Production Distribution

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

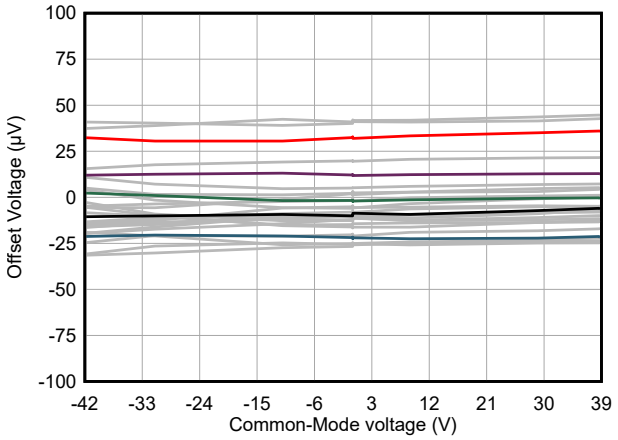


図 6-7. Input Offset Voltage vs Common-Mode Voltage

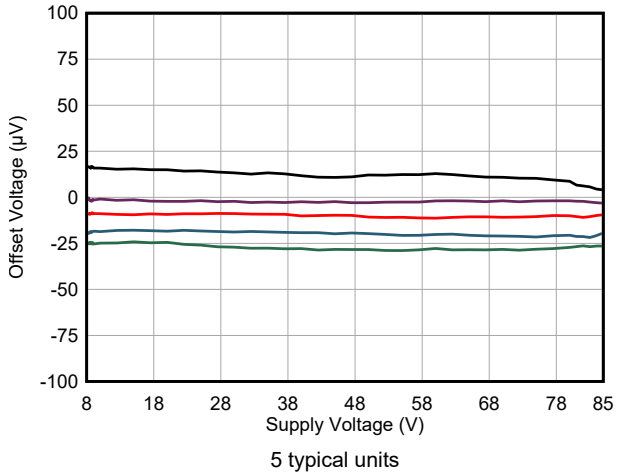


図 6-8. Input Offset Voltage vs Supply Voltage

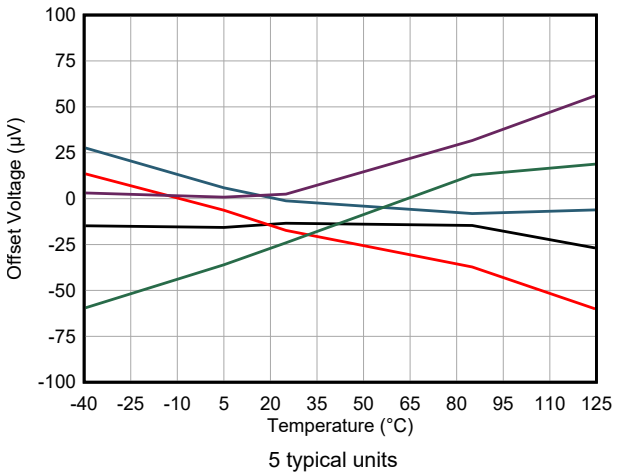


図 6-9. Input Offset Voltage vs Temperature

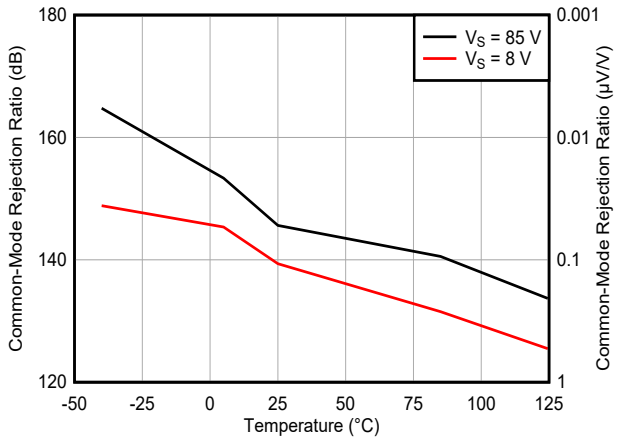


図 6-10. CMRR vs Temperature

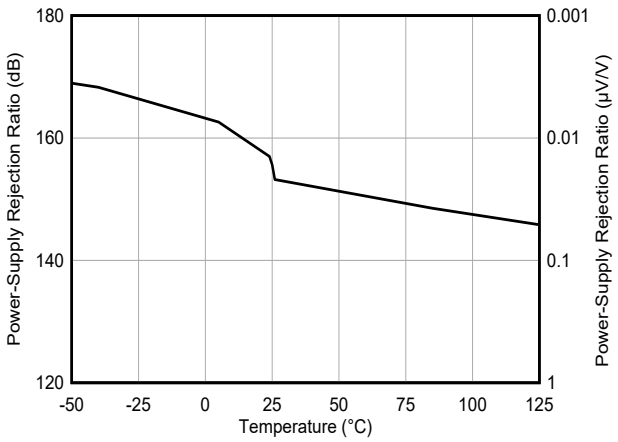


図 6-11. PSRR vs Temperature

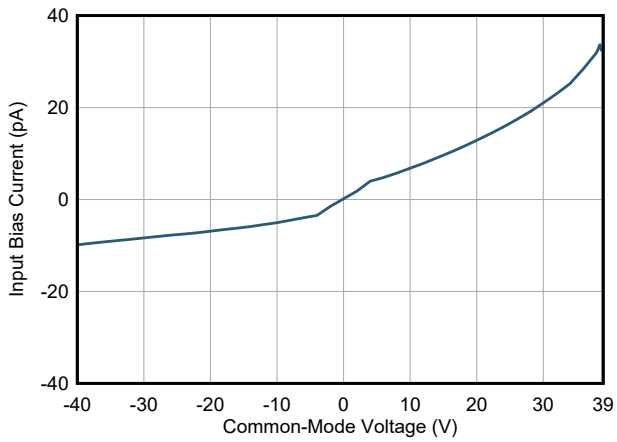


図 6-12. Input Bias Current vs Common-Mode Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

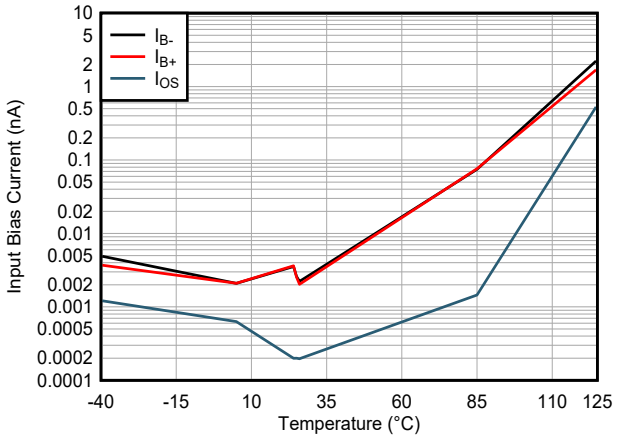


図 6-13. Input Bias Current and Current Offset vs Temperature

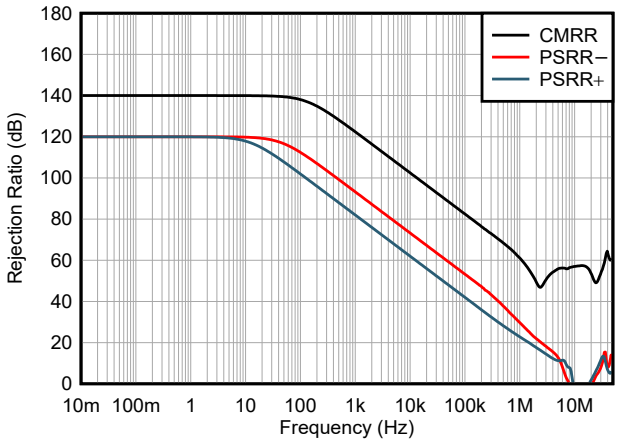


図 6-14. PSRR and CMRR vs Frequency

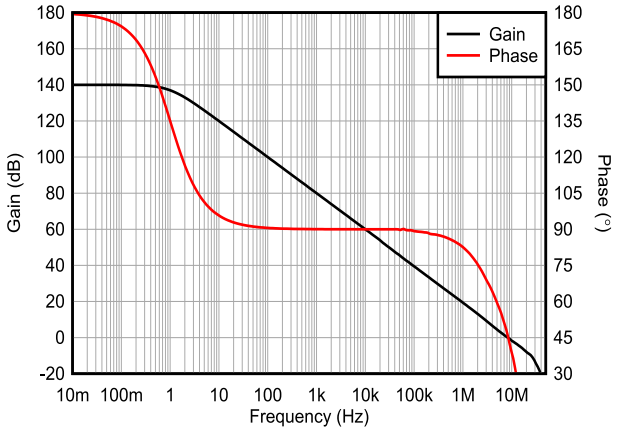


図 6-15. Open-Loop Gain and Phase vs Frequency

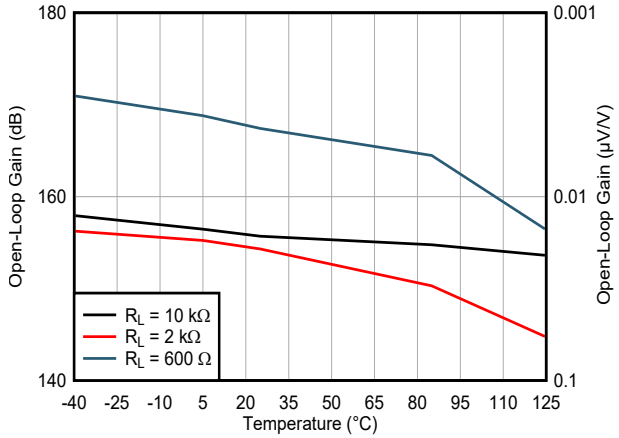


図 6-16. Open Loop Gain vs Temperature

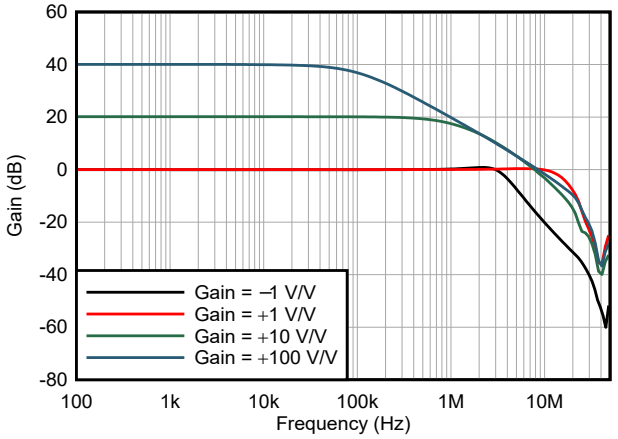


図 6-17. Closed-Loop Gain vs Frequency

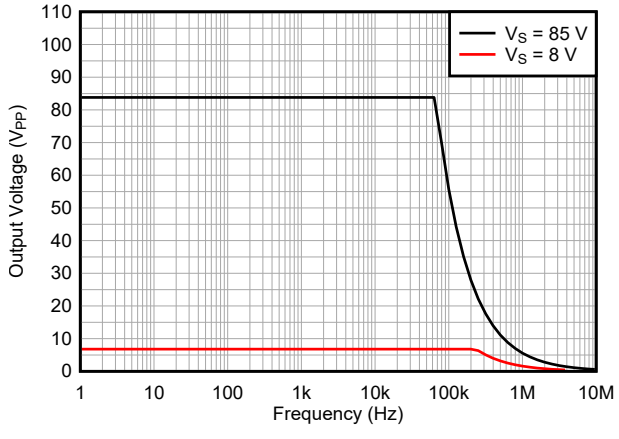
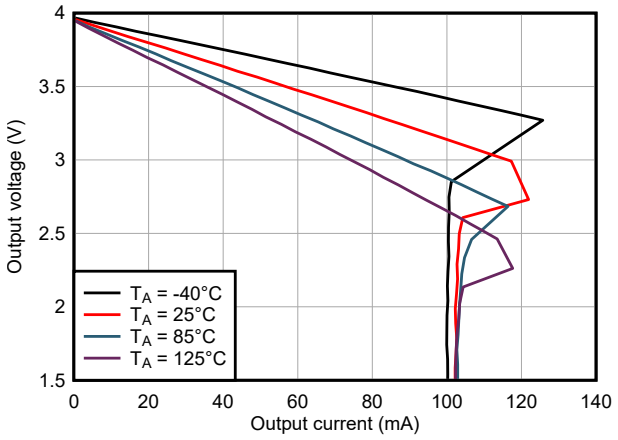


図 6-18. Maximum Output Voltage vs Frequency

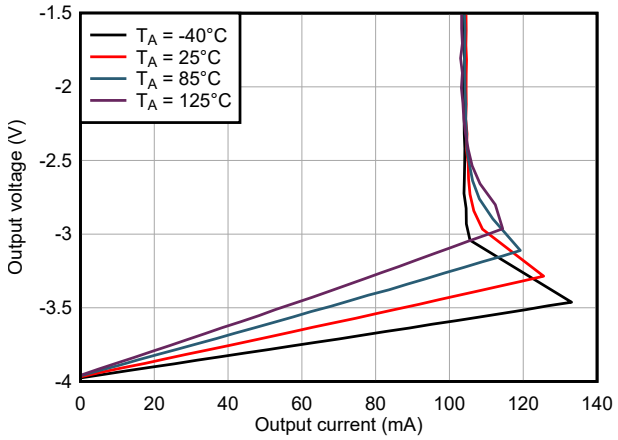
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



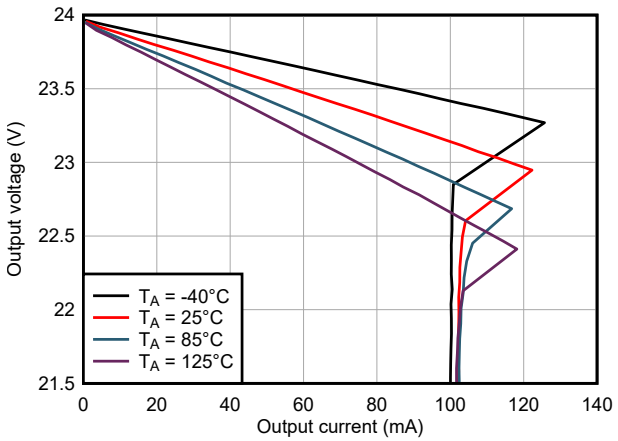
V_S = 8 V, I_{LIMIT} = 100 mA

図 6-19. Output Voltage vs Output Sourcing Current



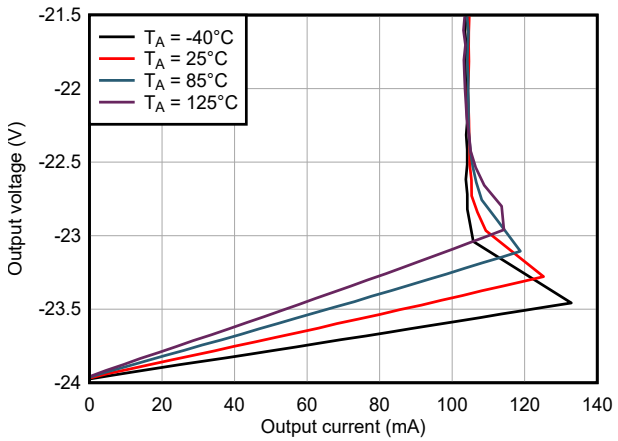
V_S = 8 V, I_{LIMIT} = 100 mA

図 6-20. Output Voltage vs Output Sinking Current



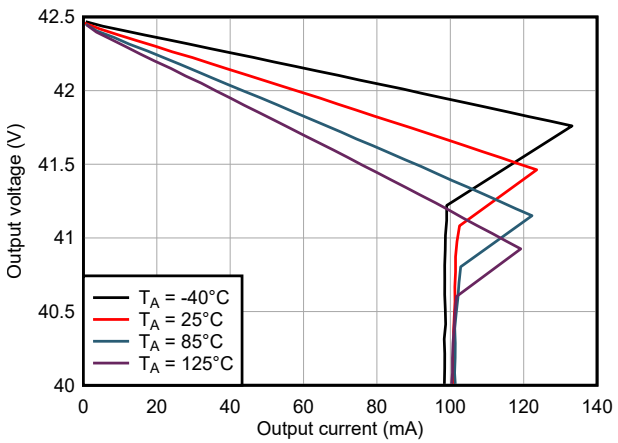
V_S = 48 V, I_{LIMIT} = 100 mA

図 6-21. Output Voltage vs Output Sourcing Current



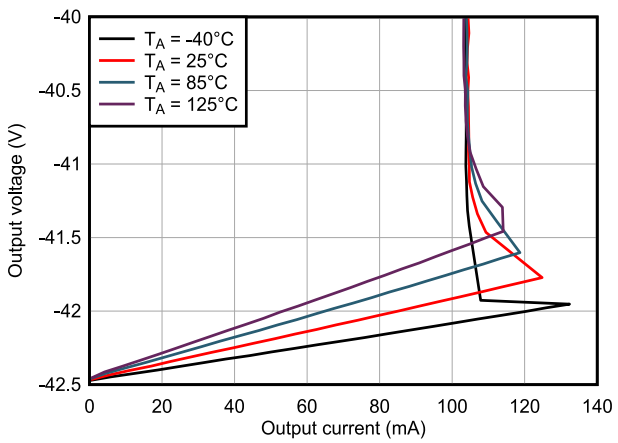
V_S = 48 V, I_{LIMIT} = 100 mA

図 6-22. Output Voltage vs Output Sinking Current



V_S = 85 V, I_{LIMIT} = 100 mA

図 6-23. Output Voltage vs Output Sourcing Current

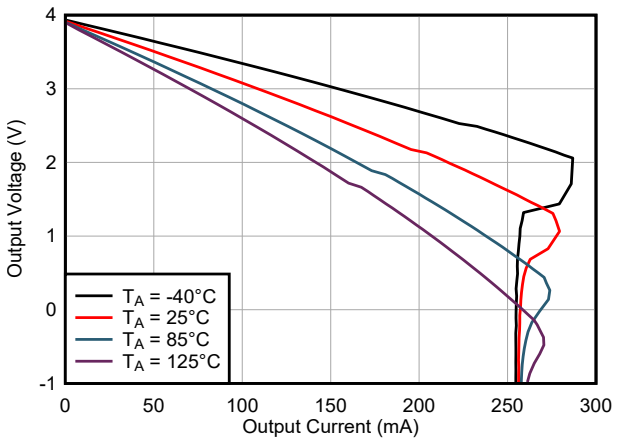


V_S = 85 V, I_{LIMIT} = 100 mA

図 6-24. Output Voltage vs Output Sinking Current

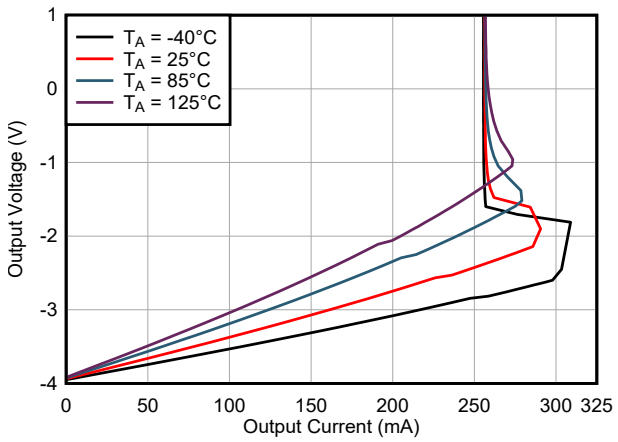
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



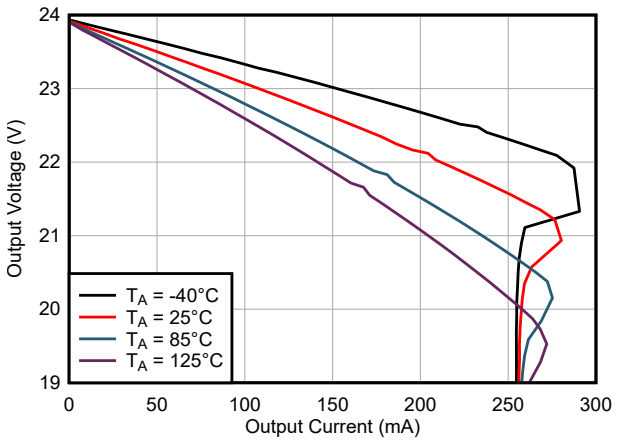
V_S = 8 V, I_{LIMIT} = 250 mA

図 6-25. Output Voltage vs Output Sourcing Current



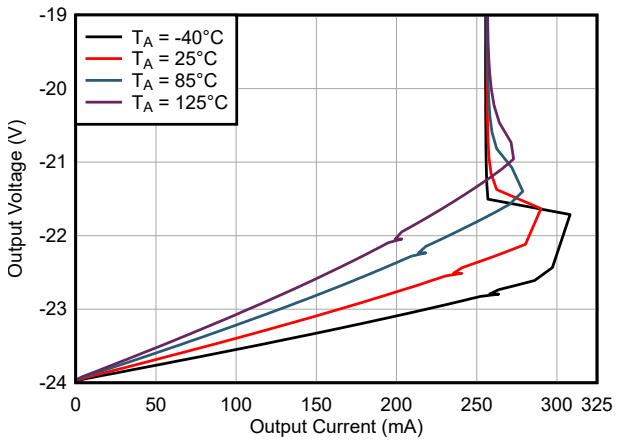
V_S = 8 V, I_{LIMIT} = 250 mA

図 6-26. Output Voltage vs Output Sinking Current



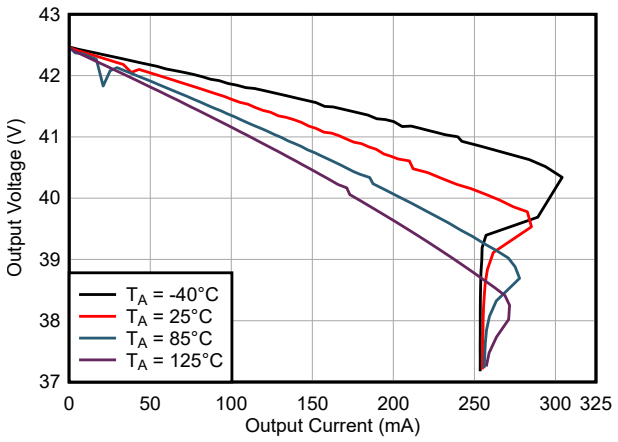
V_S = 48 V, I_{LIMIT} = 250 mA

図 6-27. Output Voltage vs Output Sourcing Current



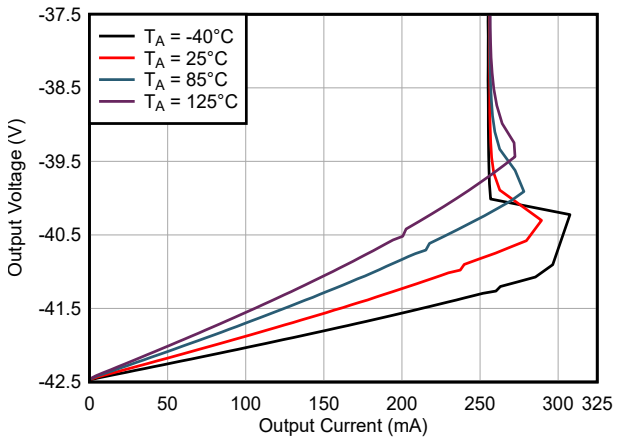
V_S = 48 V, I_{LIMIT} = 250 mA

図 6-28. Output Voltage vs Output Sinking Current



V_S = 85 V, I_{LIMIT} = 250 mA

図 6-29. Output Voltage vs Output Sourcing Current

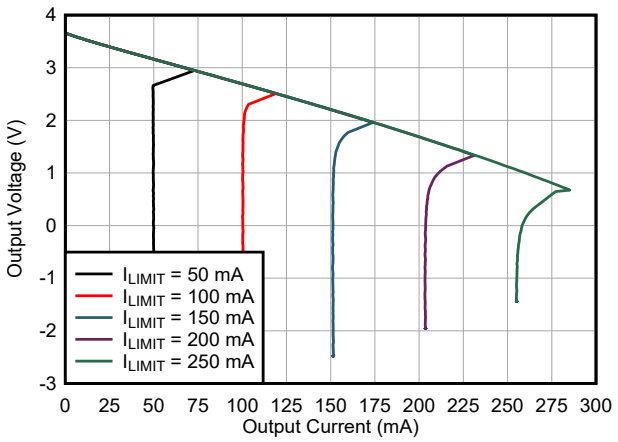


V_S = 85 V, I_{LIMIT} = 250 mA

図 6-30. Output Voltage vs Output Sinking Current

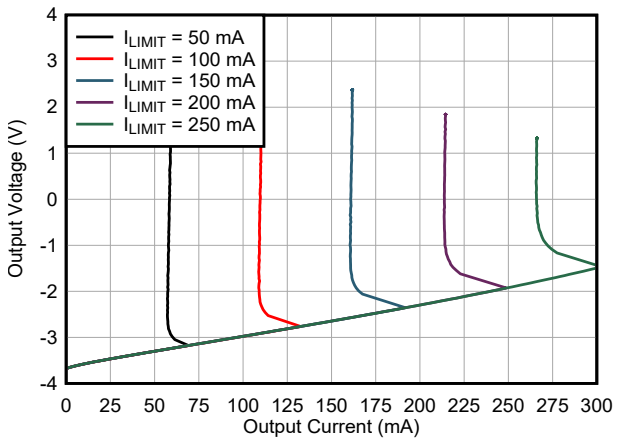
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



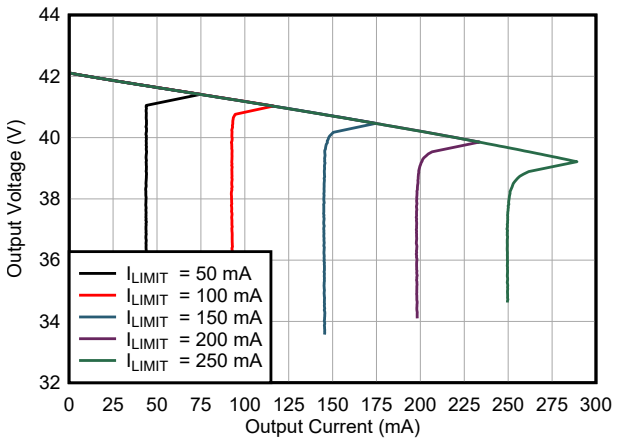
V_S = 8 V, R_L = 10 Ω to mid-supply

図 6-31. Output Voltage vs Current Limit Set



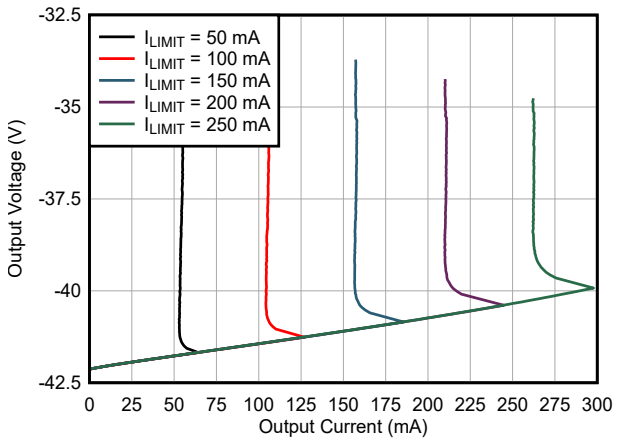
V_S = 8 V, R_L = 10 Ω to mid-supply

図 6-32. Output Voltage vs Current Limit Set



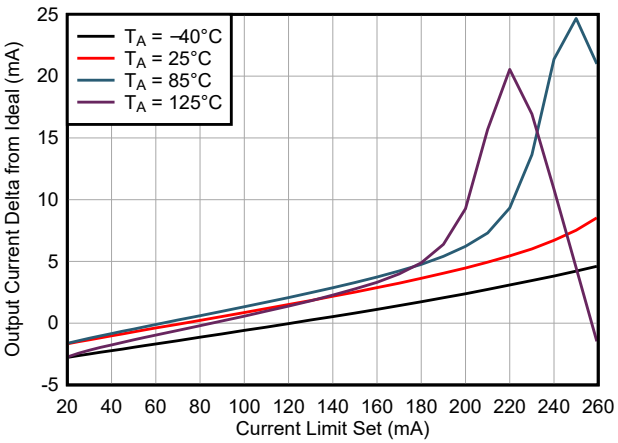
V_S = 85 V, R_L = 10 Ω to mid-supply

図 6-33. Output Voltage vs Output Sourcing Current



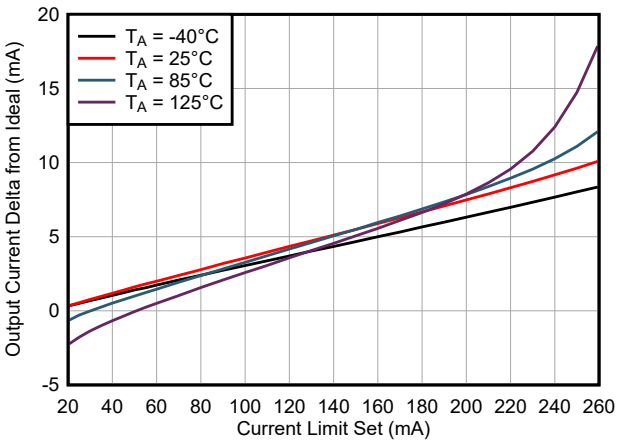
V_S = 85 V, R_L = 10 Ω to mid-supply

図 6-34. Output Voltage vs Output Sinking Current



V_S = 8 V, R_L = 10 Ω to mid-supply

図 6-35. Output Sourcing Current Error vs Current Limit Set

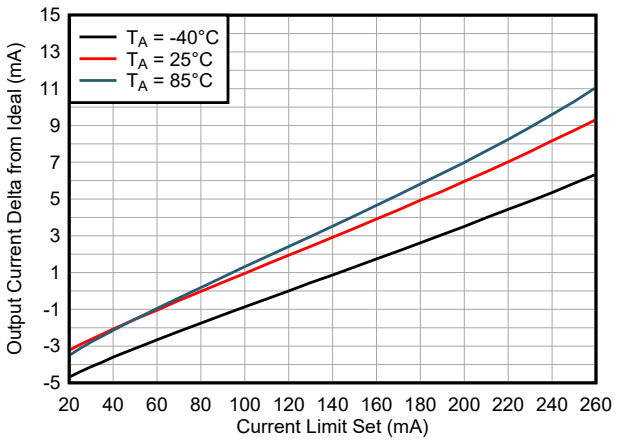


V_S = 8 V, R_L = 10 Ω to mid-supply

図 6-36. Output Sinking Current Error vs Current Limit Set

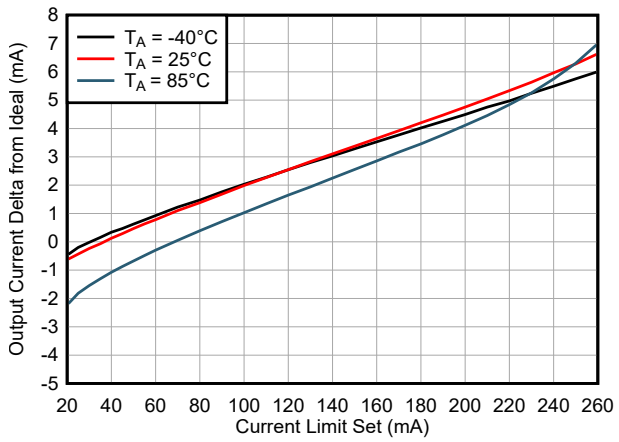
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



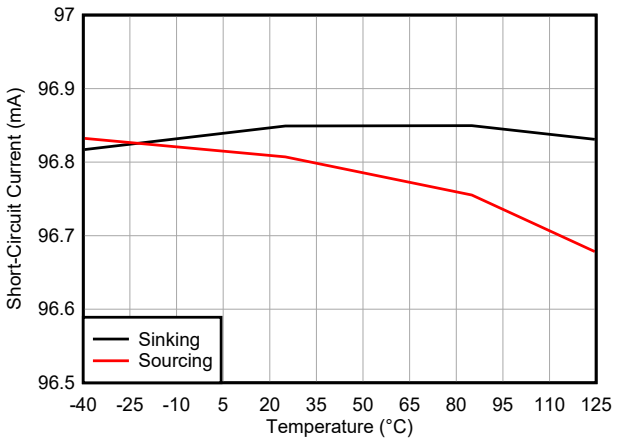
V_S = 85 V, R_L = 10 Ω to mid-supply

図 6-37. Output Sourcing Current Error vs Current Limit Set



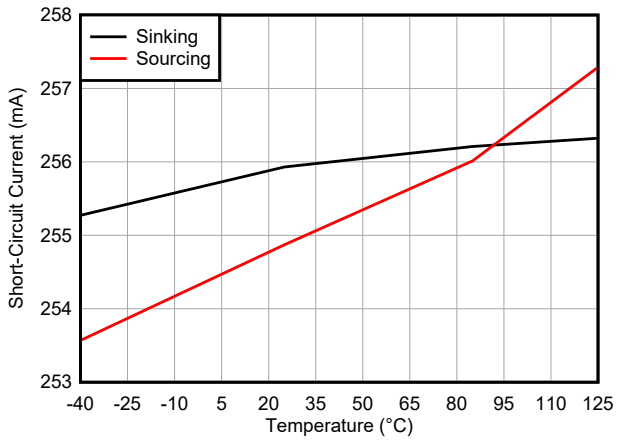
V_S = 85 V, R_L = 10 Ω to mid-supply

図 6-38. Output Sinking Current Error vs Current Limit Set



I_{LIMIT} = 100 mA

図 6-39. Short Circuit Current vs Temperature



I_{LIMIT} = 250 mA

図 6-40. Short Circuit Current vs Temperature

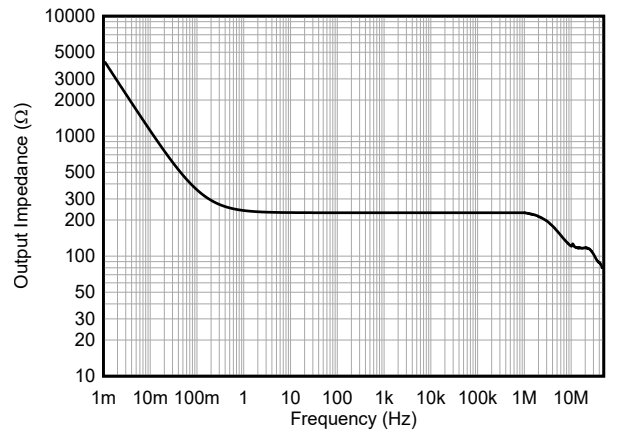


図 6-41. Open-Loop Output Impedance vs Frequency

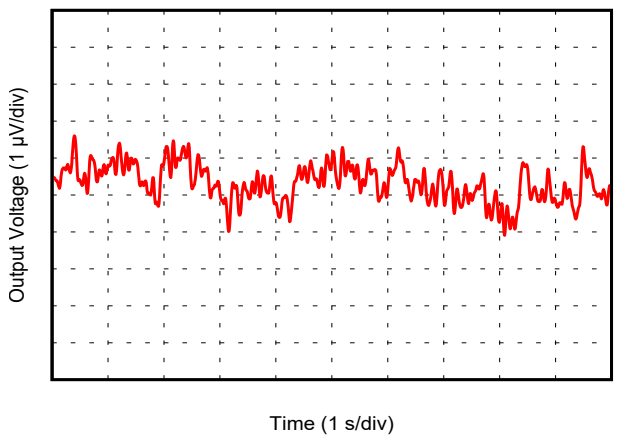


図 6-42. 0.1-Hz to 10-Hz Noise

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

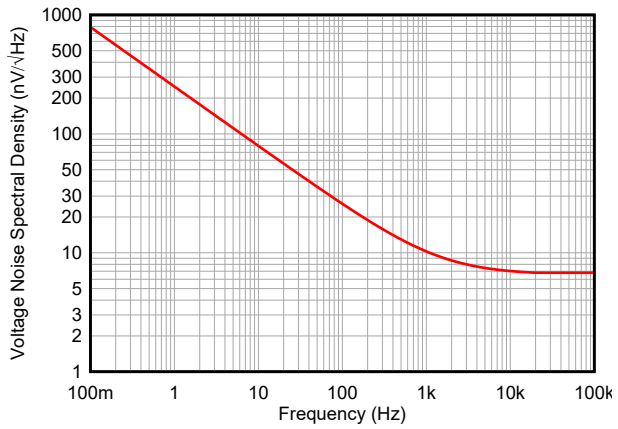


図 6-43. Input Voltage Noise Spectral Density

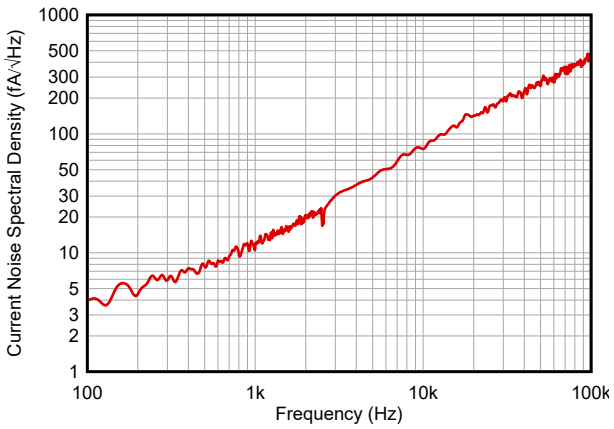
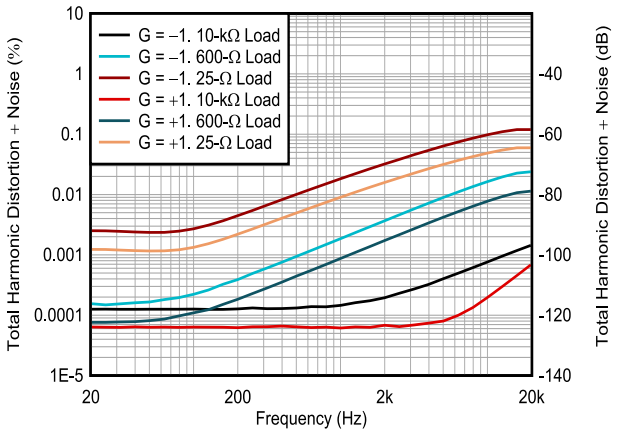
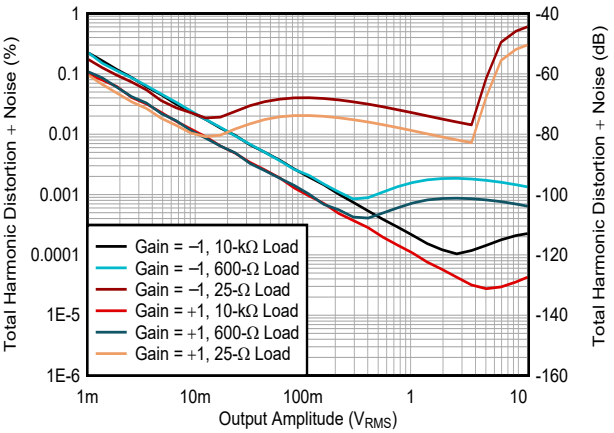


図 6-44. Input Current Noise Spectral Density



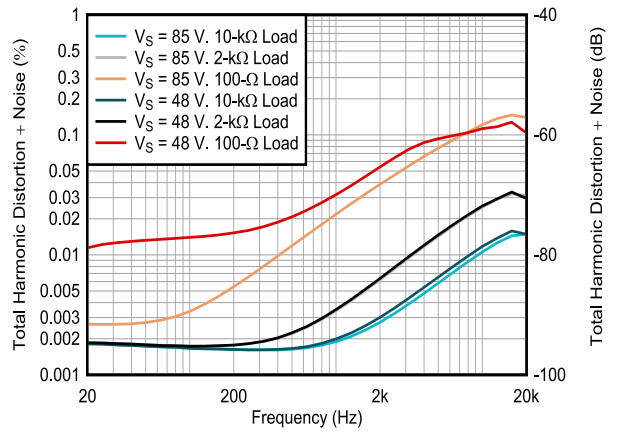
V_{OUT} = 3 V_{RMS}

図 6-45. Total Harmonic Distortion + Noise vs Frequency



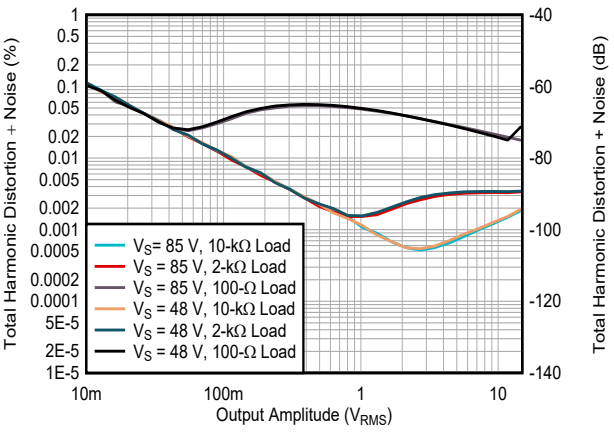
V_{OUT} = 3 V_{RMS}

図 6-46. Total Harmonic Distortion + Noise vs Amplitude



Gain = 10 V/V, V_{OUT} = 15 V_{RMS}

図 6-47. Total Harmonic Distortion + Noise vs Frequency



Gain = 10 V/V, V_{OUT} = 15 V_{RMS}

図 6-48. Total Harmonic Distortion + Noise vs Amplitude

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

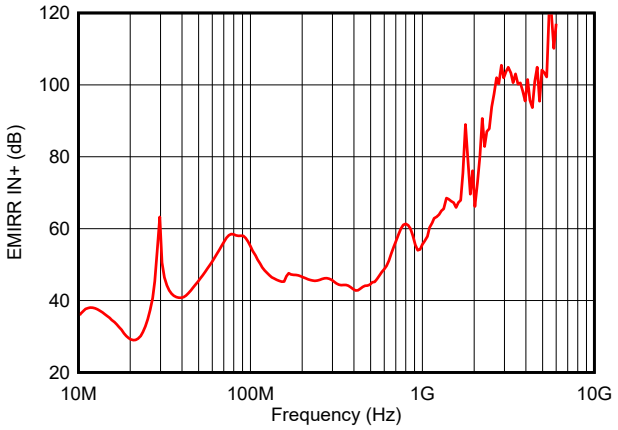


図 6-49. EMIRR vs Frequency

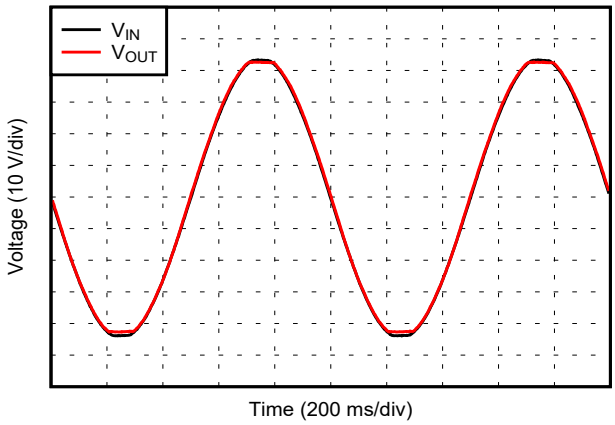


図 6-50. No Phase Reversal

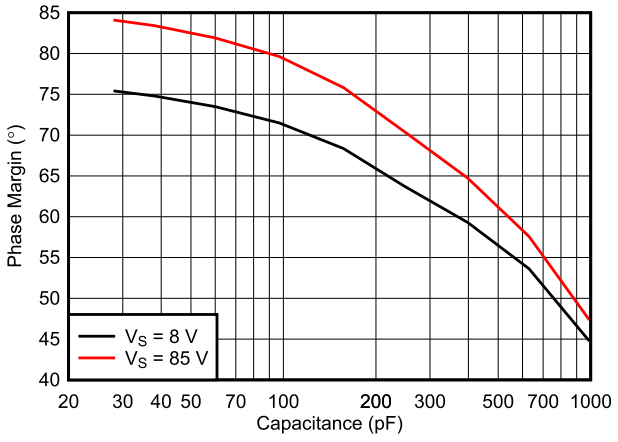


図 6-51. Phase Margin vs Capacitive Load

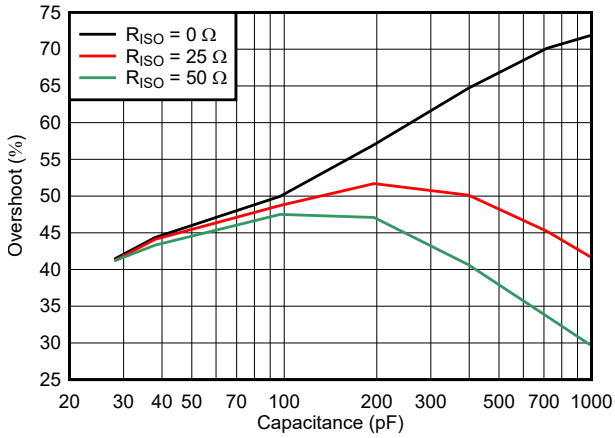


図 6-52. Small-Signal Overshoot vs Capacitive Load

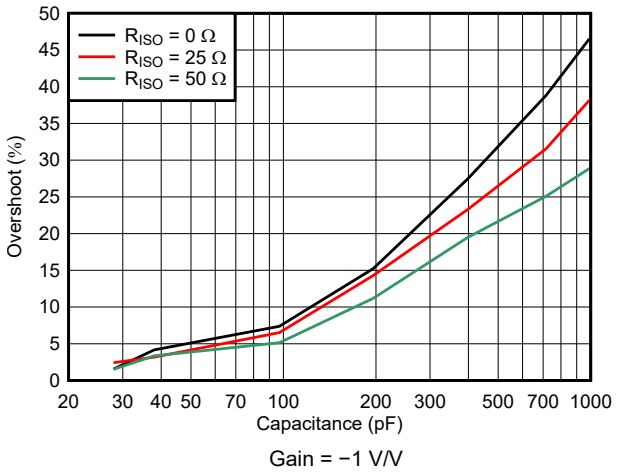


図 6-53. Small-Signal Overshoot vs Capacitive Load

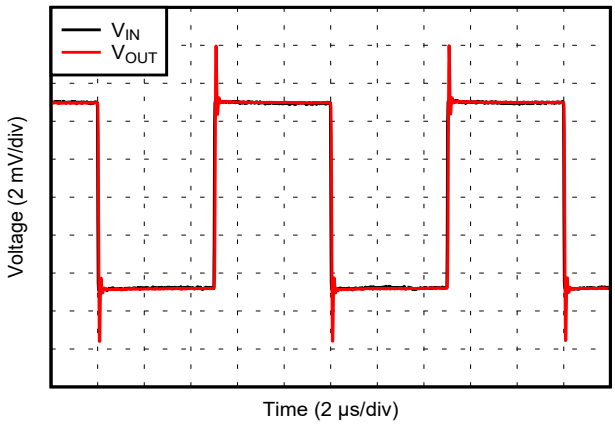
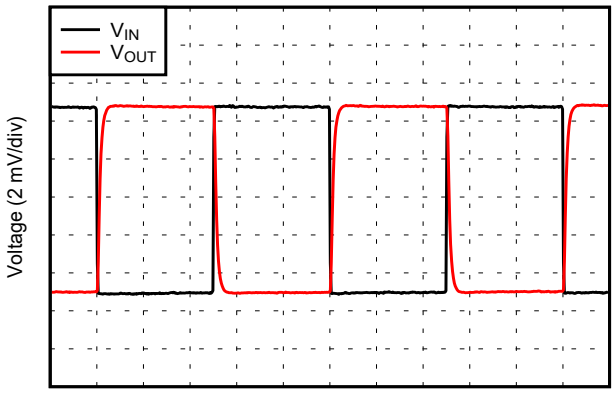


図 6-54. Small-Signal Step Response

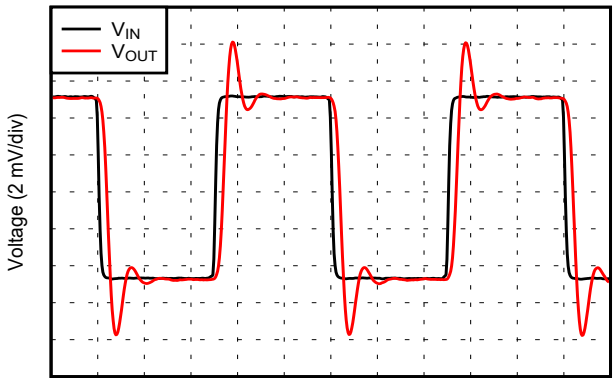
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



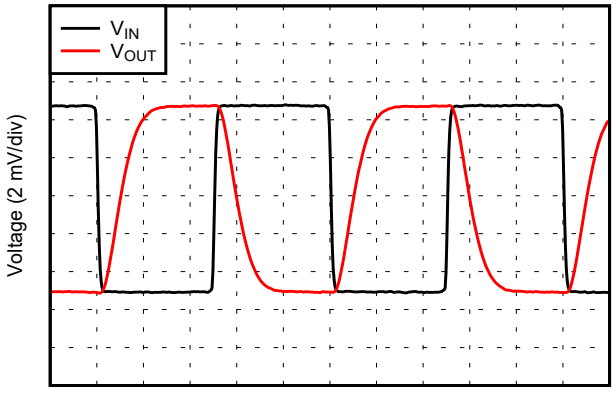
10-mV step, f = 100 kHz, gain = −1 V/V

図 6-55. Small-Signal Step Response



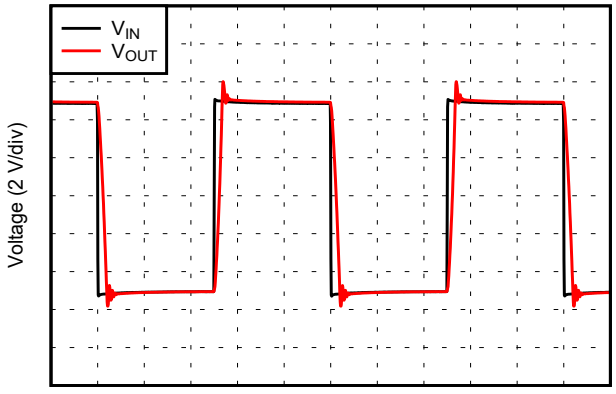
10-mV step, f = 1 MHz, gain = 1 V/V

図 6-56. Small-Signal Step Response



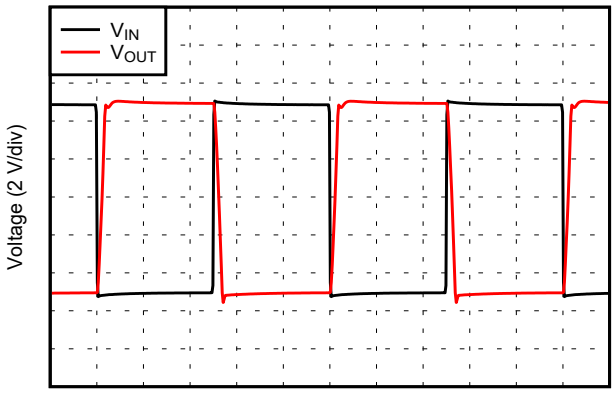
10-mV step, f = 1 MHz, gain = −1 V/V

図 6-57. Small-Signal Step Response



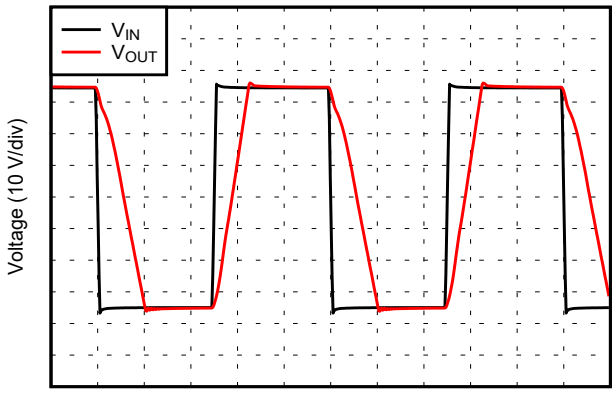
10-V step, f = 100 kHz, gain = 1 V/V

図 6-58. Large-Signal Step Response



10-V step, f = 100 kHz, gain = −1 V/V

図 6-59. Large-Signal Step Response

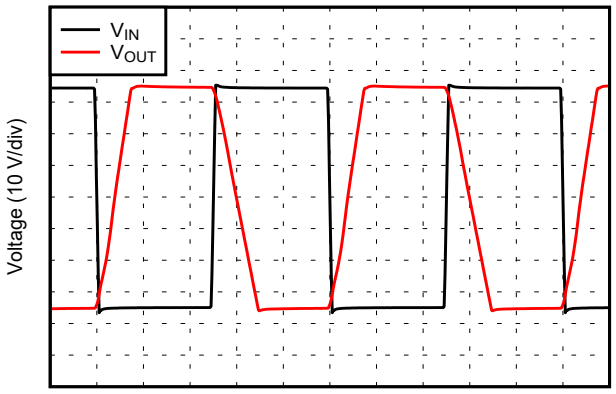


70-V step, f = 100 kHz, gain = 1 V/V

図 6-60. Large-Signal Step Response

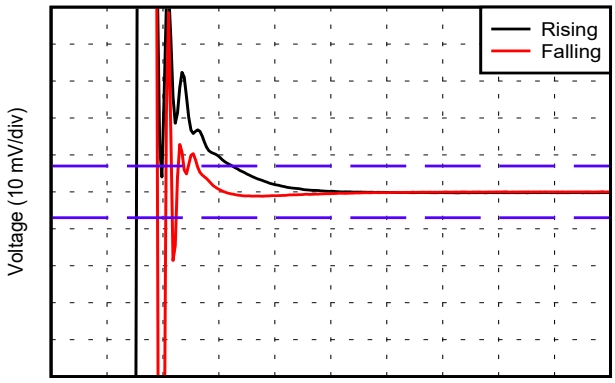
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



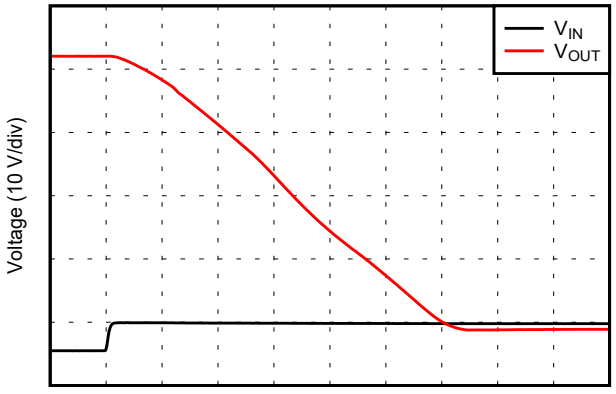
70-V step, f = 100 kHz, gain = −1 V/V

図 6-61. Large-Signal Step Response



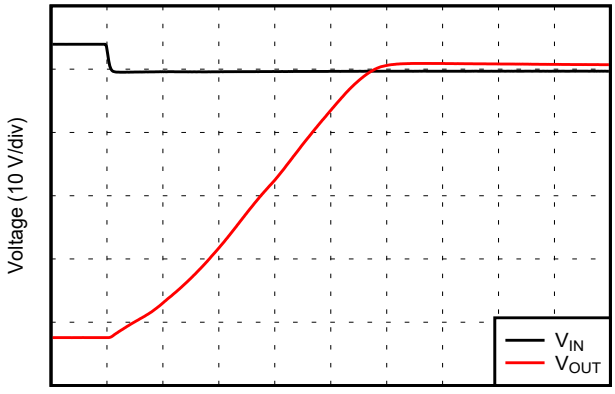
12-bit settling (0.01%), 70-V step

図 6-62. Settling Time



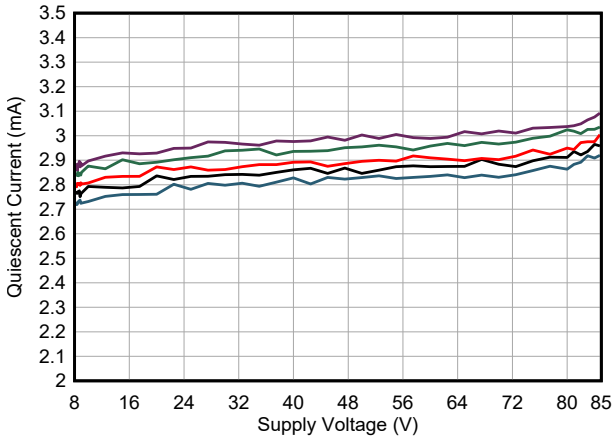
Gain = −10 V/V

図 6-63. Positive Overload Recovery



Gain = −10 V/V

図 6-64. Negative Overload Recovery



5 typical units

図 6-65. Quiescent Current vs Supply Voltage

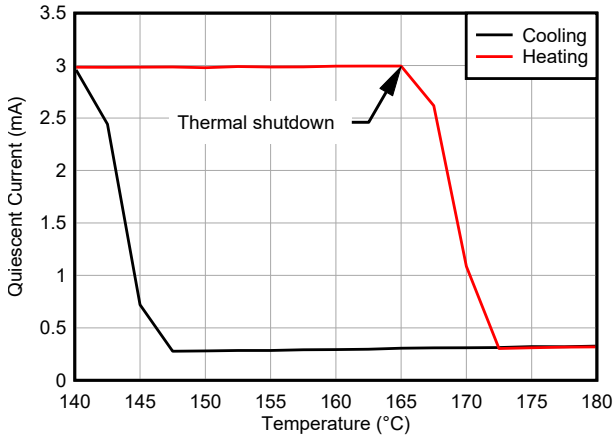


図 6-66. Quiescent Current Temperature Response

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

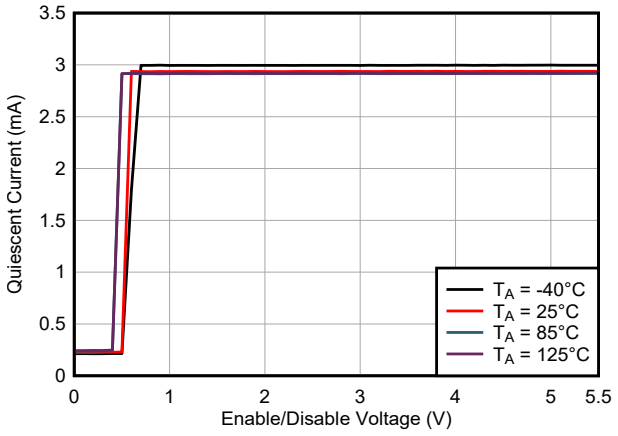
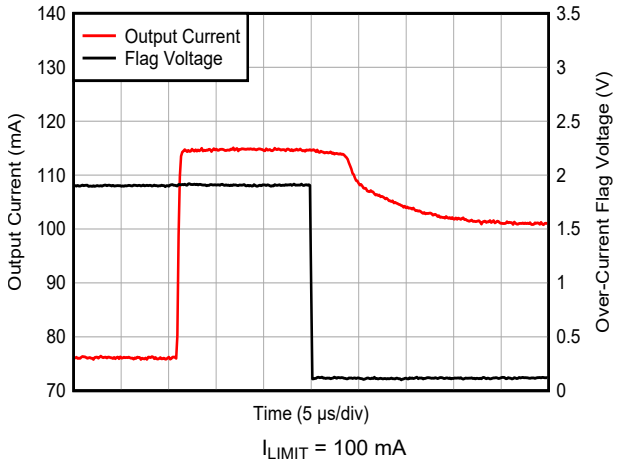
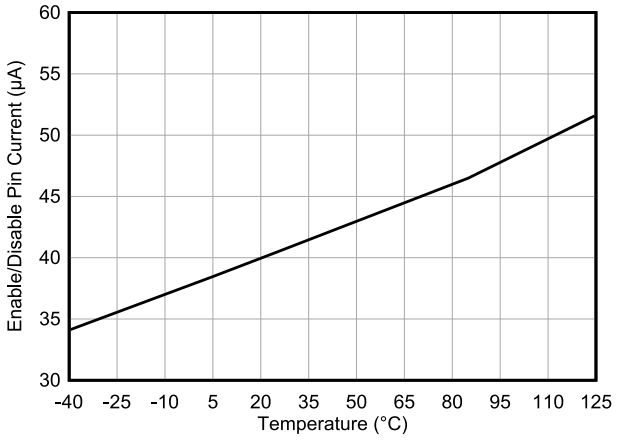


図 6-67. Quiescent Current vs Enable Voltage



I_{LIMIT} = 100 mA

図 6-68. Current Limit Response



$V_{E/D}$ = 5 V

図 6-69. Enable/Disable Pin Current vs Temperature

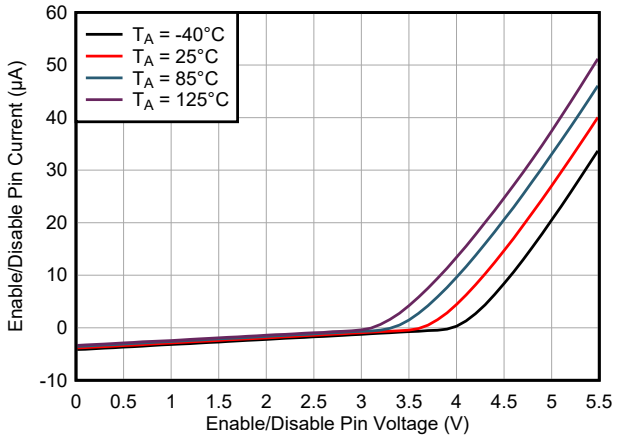


図 6-70. Enable Pin Current vs Enable Pin Voltage

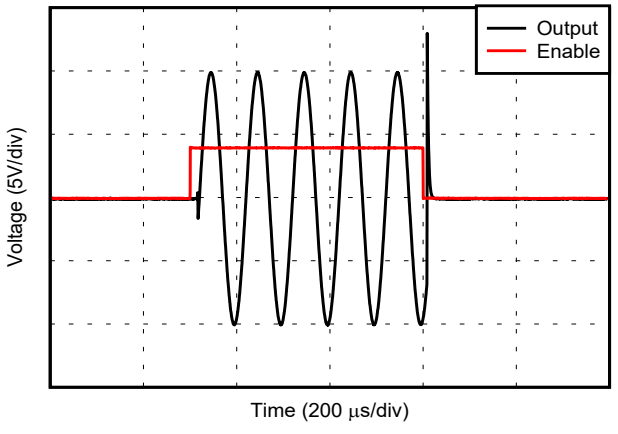
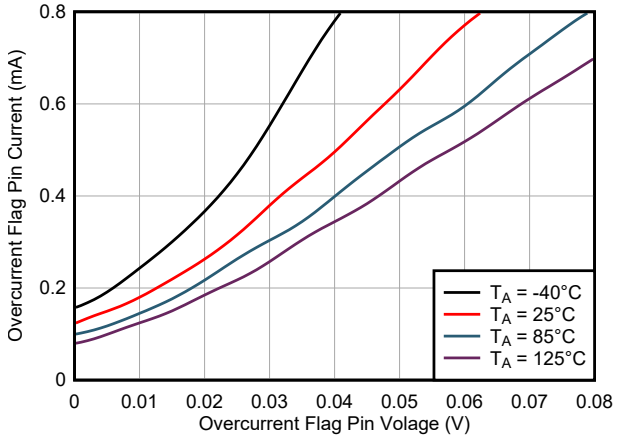


図 6-71. Enable Response

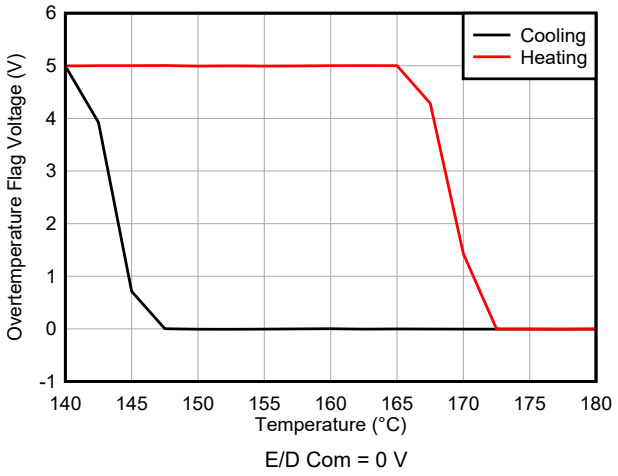


Flag is asserted

図 6-72. Current-Limit Flag Pin vs Current-Limit Flag Pin Voltage

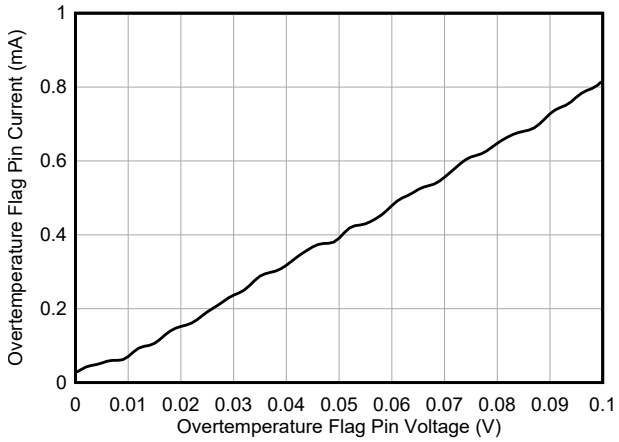
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) − (V−) = 85 V, I_{LIMIT} = 100 mA, V_{CM} = V_{OUT} = V_S/2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)



E/D Com = 0 V

図 6-73. Overtemperature Flag Pin Voltage vs Temperature



Flag is asserted

図 6-74. Overtemperature Flag Pin Current vs Overtemperature Flag Pin Voltage

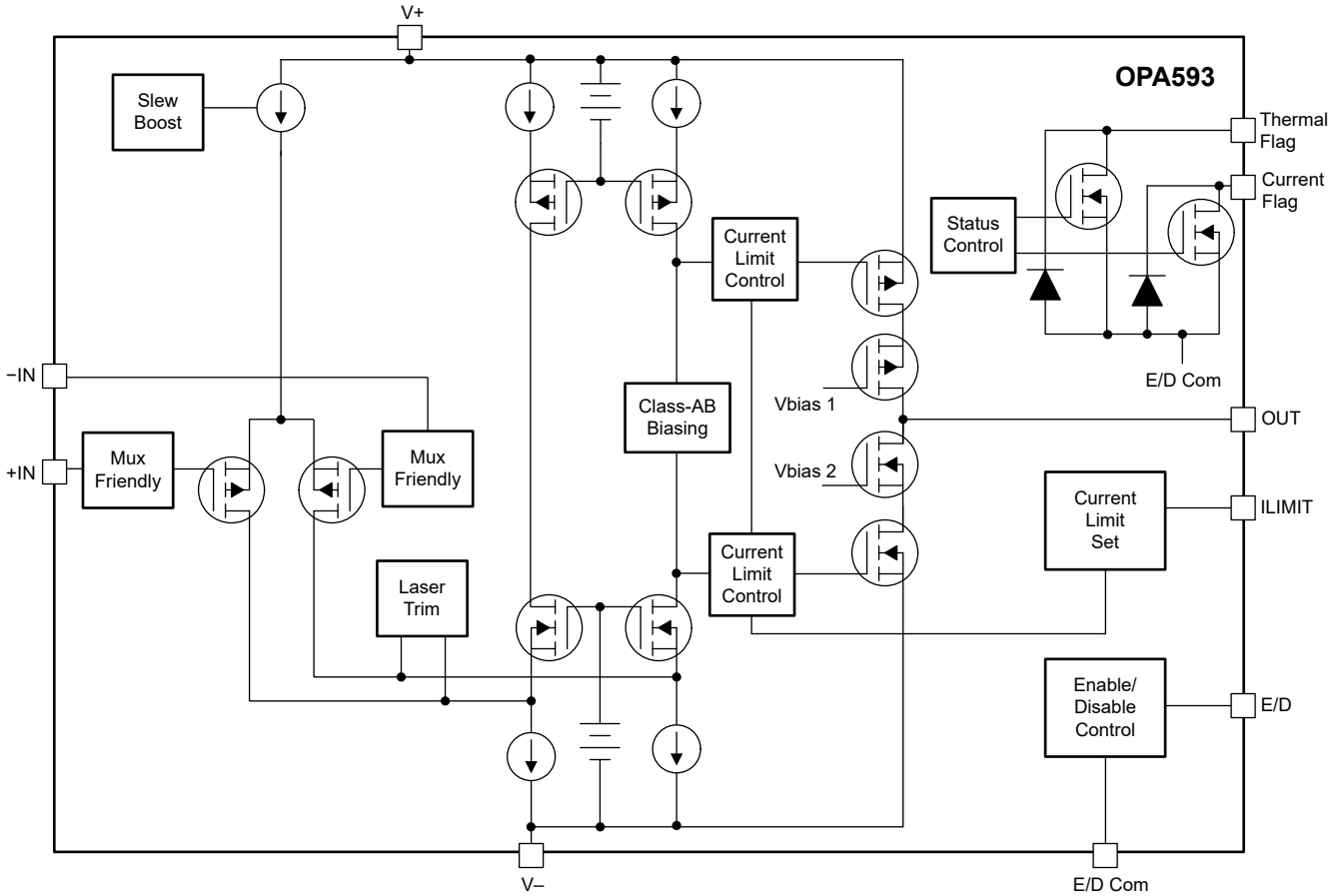
7 Detailed Description

7.1 Overview

The OPA593 is a precision, high-voltage (85 V), wide bandwidth (10 MHz), power operational amplifier (op amp) with a high output current drive of ±250 mA. The device features a current limit that helps protect the system in the event of an output short to ground. Unlike other power op amps, the current limit is specified for specific current ranges from ±25 mA to ±250 mA. Additionally, the device has two flags that indicate an overcurrent fault condition (beyond the configured limit) and an overtemperature fault condition (when the output stage shuts down to protect the device from overheating). Lastly, the output can be disabled to save system power and reduce thermal dissipation.

The unity-gain stable OPA593 has no phase inversion, a common-mode voltage range that includes the negative rail, a wide output swing range, and high dc precision. All these features make the OPA593 an excellent choice as an output driver for a device under test (DUT) in automated test equipment (ATE) systems, or for signal processing in industrial systems using signals greater than 36 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Limit

The OPA593 current limit is set through the ILIMIT pin and is programmable from ±25 mA to ±250 mA, typical. The device is specified and tested for current limits of ±25 mA, ±50 mA, ±100 mA, ±250 mA. A resistor can be used to limit the current to a fixed value or a digital-to-analog converter (DAC) can be used to vary the current limit during operation. 図 7-1 shows a simplified diagram of the current-limit mirror configurations, as well as common resistor or DAC settings and the respective output current limit.

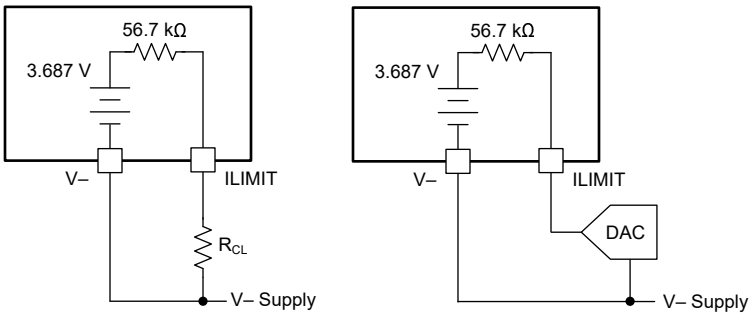


図 7-1. OPA593 Internal Current Limit Configurations

The most common configuration is to set the current limit using a resistor (R_{CL}) connected between the ILIMIT pin and the negative supply (V–). With this configuration, 式 1 and 式 2 are used to calculate the current limit based on the external resistor value or the resistor needed given the desired current limit value:

$$I_{LIMIT} = \frac{3.687\,V \times 4000}{56.7\,k\Omega + R_{CL}} \quad (1)$$

$$R_{CL} = \frac{3.687\,V \times 4000}{I_{LIMIT}} - 56.7\,k\Omega \quad (2)$$

An alternative to fixing the current limit to a single value using an external resistor is to use a source measure unit (SMU) or digital-to-analog converter (DAC), which enables a variable current limit.

> **注意**
> With this configuration, the output of the SMU or DAC must not exceed the I_{LIMIT} specification in セクション 6.1 to avoid reverse biasing the internal current limit circuitry and potentially damaging the device.

Use 式 3 to set the current limit when a DAC is used (V_{LIMIT} = DAC output voltage):

$$V_{LIMIT} = 3.687\,V - \frac{I_{LIMIT} \times 56.7\,k\Omega}{4000} \quad (3)$$

Be aware that the SMU or DAC output voltage must be referenced to the negative supply of the OPA593. Several nominal current-limit values along with the respective external resistor values and DAC output voltages are listed in 表 7-1.

表 7-1. Nominal Current-Limit Values

CURRENT LIMIT, I_{LIMIT}(mA)	RESISTOR, R_{CL} (kΩ)	DAC VOLTAGE, V_{LIMIT} (V)(1)
25	536	3.33
50	237	2.98
100	90.9	2.27
200	16.9	0.85

表 7-1. Nominal Current-Limit Values (continued)

CURRENT LIMIT, I_{LIMIT}(mA)	RESISTOR, R_{CL} (kΩ)	DAC VOLTAGE, V_{LIMIT} (V)(1)
250	2.29	0.14

(1) Voltages are referenced to the negative supply, V−

While the current limit tolerance of the OPA593 is specified for specific current limit levels, any resistor, SMU, or DAC inaccuracies add to the listed tolerance. To achieve the desired system level accuracy, take care when selecting these external components. 図 7-2 shows a correlation between the ideal or calculated output current limit and the actual current limit as measured on the OPA593.

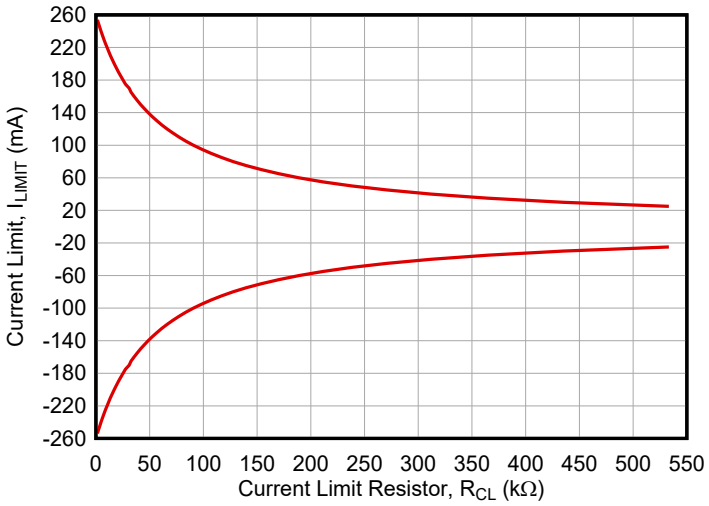


図 7-2. Typical Output Current vs Current-Limit Resistor Value

7.3.2 Overcurrent Flag

The OPA593 features an overcurrent flag (Current Flag pin) that indicates a condition where the output current exceeds the limit established by the ILIMIT pin. For example, in an output short-to-ground fault condition, the overcurrent flag asserts, which pulls the flag pin low to E/D Com, and the output current is limited to the value set by ILIMIT. This flag is an open-drain output compatible with standard low-voltage logic circuitry, such as a microcontroller (MCU). Use a 5-kΩ to 10-kΩ pullup resistor to limit the input current when the flag is asserted. If this feature is not used, leave this pin floating.

7.3.3 Overtemperature Flag

The OPA593 has internal thermal protection. When the junction temperature reaches approximately 170°C, the op amp output stage disables and the overtemperature flag (Thermal Flag pin) is asserted, which pulls the flag pin low to E/D Com. When the junction temperature cools to a safe operating temperature, approximately 150°C, the output stage is enabled, and the op amp resumes normal operation. This flag is an open-drain output compatible with standard low-voltage logic circuitry, such as an MCU. Use a 5-kΩ to 10-kΩ pullup resistor to limit the input current when the flag is asserted. If this feature is not used, leave this pin floating.

7.3.4 Output Enable and Disable

The OPA593 incorporates an enable and disable feature that uses the E/D pin to disable the output stage of the amplifier, which reduces the power consumption of the op amp and switches the output to a high-impedance state.

The E/D pin is referenced to the E/D Com pin. If left floating, the E/D pin is internally pulled up to enable the device. If externally controlled, the E/D pin must be supplied with a voltage between 1.5 V and 5.5 V greater than the E/D Com pin voltage. Even though the OPA593 output is enabled with a floating E/D pin, a moderately fast, negative-going signal capacitively coupled to the E/D pin can overpower the internal pullup and cause device shutdown. If the enable function is not used, a conservative and recommended approach is to connect E/D through a 47-pF capacitor to E/D Com. 図 7-3 shows different ways to connect the E/D and E/D Com pins.

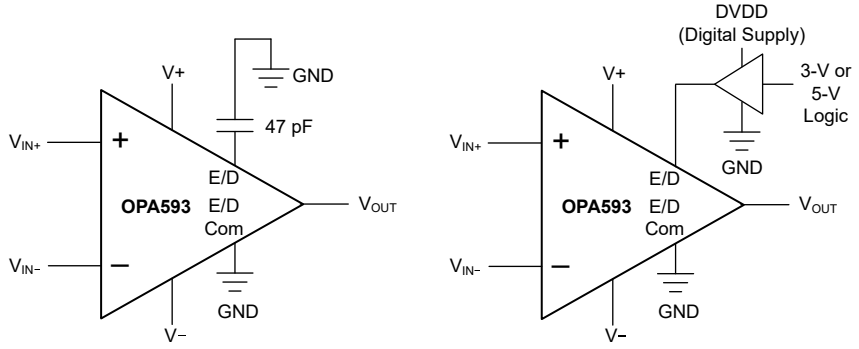


図 7-3. E/D and E/D Com Pin Connections

When the E/D pin is dropped to a voltage between 0 V and 0.5 V greater than the E/D Com pin voltage, the output of the OPA593 is disabled. When disabled, the output of the OPA593 is set to a high-impedance state.

7.3.5 Mux-Friendly Inputs

The OPA593 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in 図 7-4 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in 図 7-5. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.

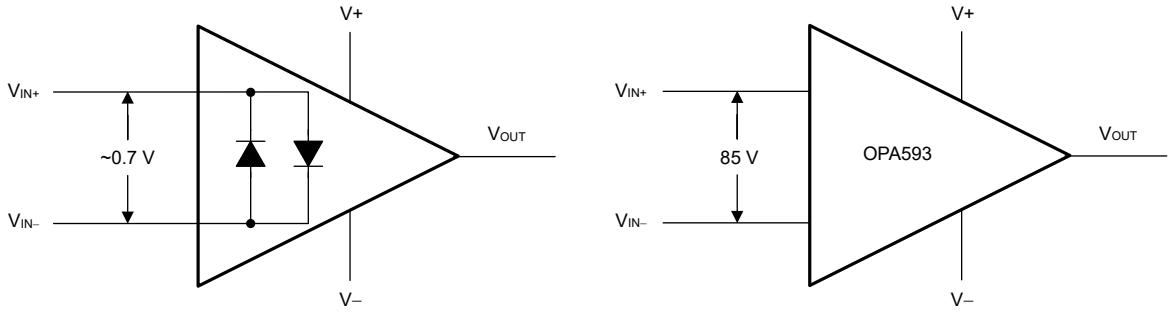


図 7-4. OPA593 Input Protection Does Not Limit Differential Input Capability

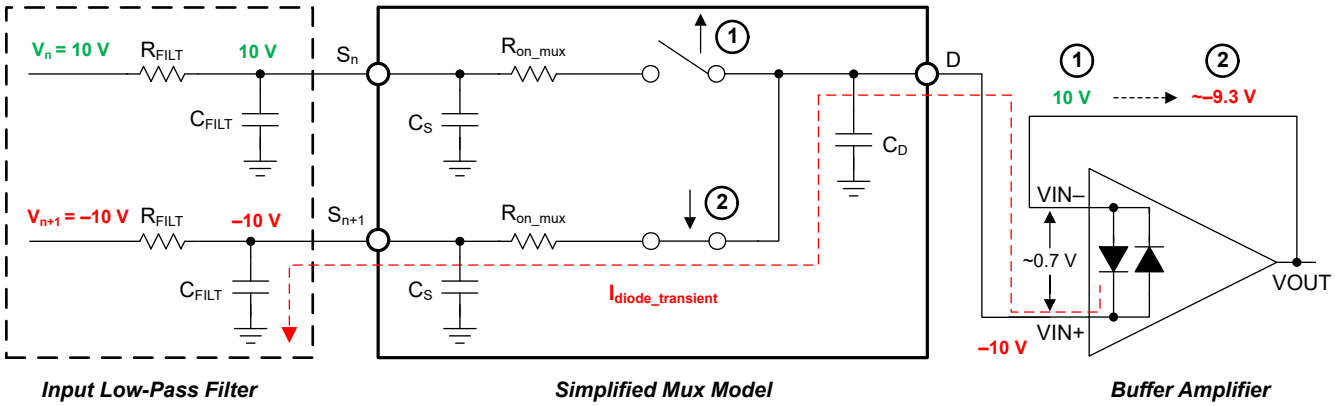


図 7-5. Back-to-Back Diodes Create Settling Issues

The OPA593 a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making this device an excellent choice for multichannel, high-switched, input applications. The OPA593 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85 V, making this device a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

7.4 Device Functional Modes

The OPA593 has two modes of operation. The first mode is normal operation where the amplifier is enabled, either by supplying a voltage to the enable-disable (E/D) pin that is between 2.5 V and 5 V greater than the E/D Com pin or by leaving the E/D pin floating. The second mode of operation is a low-power, disabled state where the E/D pin is driven between 0 V and 0.65 V greater than the E/D Com pin. In this state, the amplifier output is disabled and enters a high-output-impedance state.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPA593 is a precision, high-voltage, high-output-current op amp. The device is capable of operating with supplies as low as ±4 V (8 V) and as high as ±42.5 V (85 V). The current limit feature limits the output current, up to ±250 mA, to a specified accuracy. With a small size, high operating voltage range, output current, and high dc precision, the device is designed to operate as a high-gain stage, capable of driving heavy loads and condition large signals. The additional features of the OPA593, including the current limit, overcurrent and overtemperature flags, thermal protection, output disable, and mux-friendly inputs, help protect both the op amp and the system from potential damage due to various fault conditions.

8.2 Typical Application

8.2.1 Output Driver

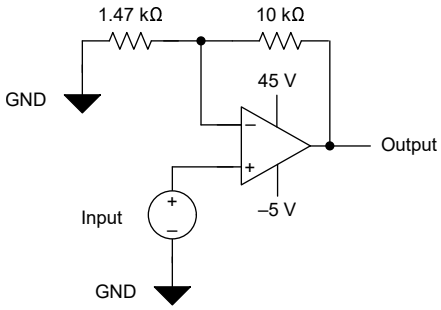


図 8-1. Output Driver Configured With a Gain of 8

8.2.1.1 Design Requirements

The OPA593 is designed for use as an output driver stage with gain and provides a wide supply voltage and high output current with programmable current limit. Combined with the small size of the 4-mm × 4-mm WSON package, these features make this device a great choice for high-channel density systems, such as semiconductor test and manufacturing platforms where many channels are present. In this design example, the OPA593 is configured for a gain of 8 V/V. A small negative supply is provided if the application requires a small output voltage. For example, in the case of a device under test (DUT) continuity check, the amplifier is able to provide the output without being limited by the negative rail (that is, saturating the output).

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	+45 V, –5 V
Input voltage	0 V to 5 V
Output voltage	0 V to 40 V
System gain	8
Output current	Up to 250 mA

8.2.1.2 Detailed Design Procedure

In this design example, the OPA593 is configured as both a gain stage and output driver. The input signal to the amplifier is 0 V to 5 V, and the device is configured with a positive gain of 8. This configuration results in an output voltage of 0 V to 40 V. Select supply voltages that provide adequate headroom so that the amplifier can sink or source up to 250 mA without *slamming* the output into the rail. Minimize the swing from the supply to the output to minimize the thermal dissipation of the device.

This simple design example is common in many systems that use a DAC to provide the input signal and require a wide output signal with high output current. Such systems include test and measurement platforms and power supplies.

図 8-2 shows the input and output signal of this OPA593 circuit.

8.2.1.3 Application Curve

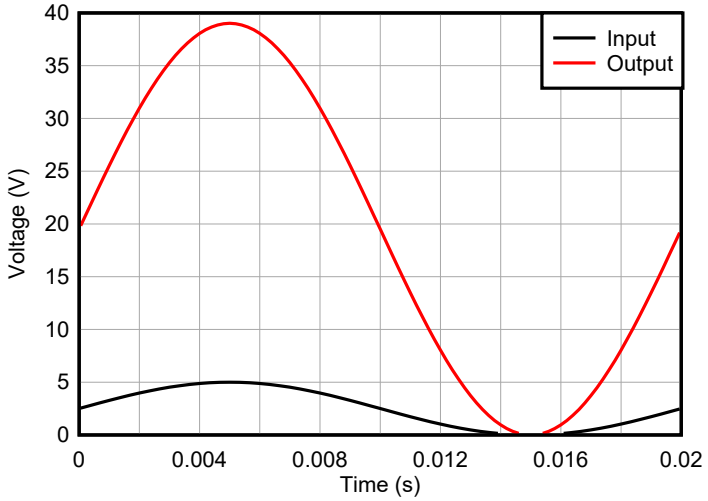


図 8-2. OPA593 Output Driver Circuit, Input and Output Signals

8.2.2 High Voltage 2:1 Multiplexer With Unity Gain

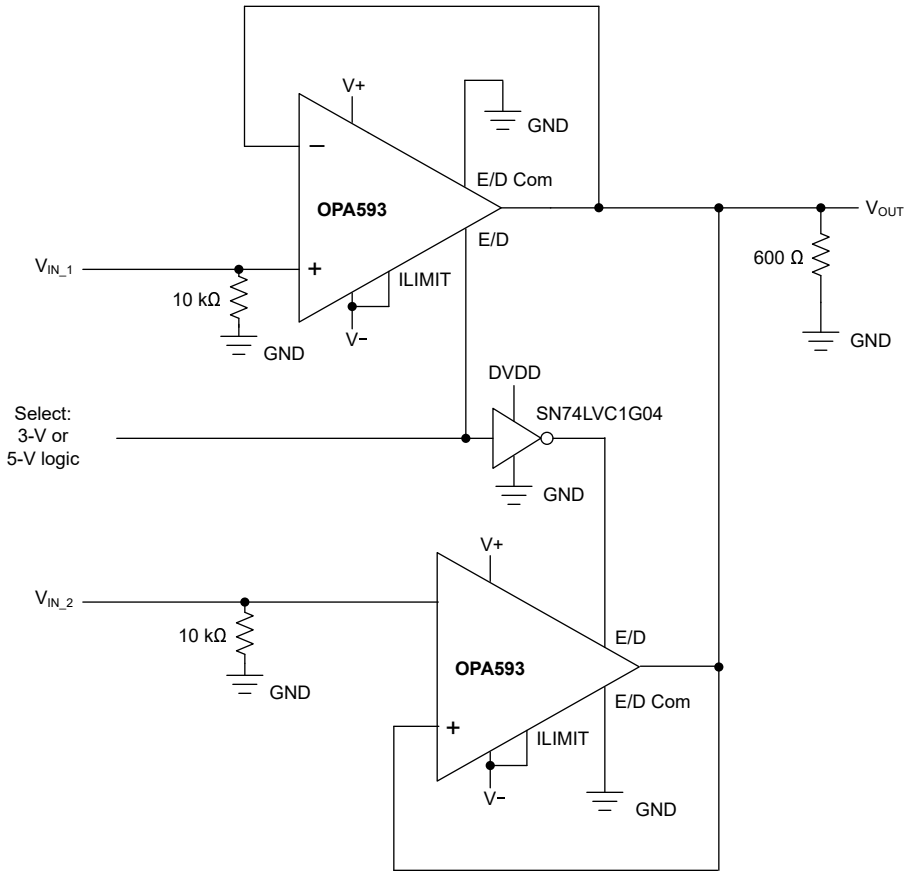


図 8-3. High Voltage 2:1 Multiplexer With Unity Gain

8.2.2.1 Design Requirements

The OPA593 operates on high-voltage supplies up to 85 V and is used to create a high voltage multiplexer (MUX) with a gain of 1 or higher. This design example uses two OPA593 op amps and makes use of the disable function. The high-impedance state of the output while the amplifier is disabled allows for the outputs of two OPA593 op amps to be connected together.

8.2.2.2 Detailed Design Procedure

In this design example, two OPA593 precision op amps are configured as a unity gain buffers powered with a ±42.5-V dual supply. The input signal to either amplifier can range from –40 V to +39 V to remain in linear operation. The output of the amplifiers are connected together and a 3-V or 5-V logic signal, serving as the output select, is used to toggle between the enable and disable modes of operation. The logic control signal is directly applied to one OPA593 E/D pin, and an inverter gate is used to drive the other OPA593 E/D pin. 図 8-3 shows a simplified representation of this circuit.

A clear benefit of this design is the high-voltage capability, along with the thermal protection, overcurrent protection, and current-limit features. The *mux-friendly* input of the OPA593 provides a full input differential range, avoiding the pitfalls of other amplifiers with traditional back-to-back diodes in this configuration. This design can also be reconfigured to include signal gain, but careful selection of the input and feedback resistors is required to minimize current leakage paths.

8.3 Power Supply Recommendations

The OPA593 operates from power supplies up to ±42.5 V, or a total of 85 V, with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. Parameters that vary significantly with operating voltage are shown in セクション 6.6.

Some applications do not require an equal positive and negative output voltage swing. Power-supply voltages do not have to be equal. The OPA593 operates with as little as 8 V between the supplies, and with up to 85 V between the supplies.

8.4 Layout

8.4.1 Layout Guidelines

During the surface-mount solder operation (when the pins are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into a V− plane. Always solder the thermal pad to the PCB, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. Connect the thermal pad to the most negative supply voltage on the device, V–.
2. Prepare the PCB with a top-side pattern. There must be patterning for the pins and thermal pad.
3. Thermal vias improve heat dissipation, but are not required.
4. Place recommended vias in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SON-12 DNT package are shown in the thermal land pattern mechanical drawing appended at the end of this document. Keep the vias small, so that solder wicking through the vias is not a problem during reflow. Use a 0.2-mm size via with a minimum of five connected directly below the thermal pad.
5. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA593 device. These additional vias can be larger than the vias directly under the thermal pad because the additional vias are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all vias to the internal power plane of the correct voltage potential, V–.
7. When connecting these vias to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the OPA593 WSON package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the vias of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the device pins.
10. With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component.

8.4.1.1 Thermal Considerations

Through normal operation, the OPA593 self-heats. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. The maximum allowed junction temperature sets the maximum allowed internal power dissipation (P_D) as described in the following paragraph. Design efforts should be made to prevent T_J from exceedeing the maximum temperature listed in the *Absolute Maximum Ratings* table.

Operating junction temperature (T_J) is determined by the ambient temperature (T_A), the internal P_D under the operating conditions, and the junction-to-ambient thermal resistance ($R_{\theta JA}$). This relationship is given by $T_A + (P_D \times R_{\theta JA})$. P_D is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) when delivering power to the load. P_{DQ} is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load the P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies, V+ and V−). Under this condition $P_{DL} = (V+)^2 / (4 \times R_L)$, where R_L includes feedback network loading.

The power in the output stage and not into the load determines internal power dissipation.

As a worst-case example, compute the maximum T_J using the OPA593 in the circuit of 図 8-1 operating at a maximum specified temperature of 125°C and driving a grounded 600-Ω load.

$$P_D = P_{DQ} + P_{DL} \tag{4}$$

$$P_D = (50\,V \times 4\,mA) + \frac{22.5^2\,V}{(4 \times 600\,\Omega \,||\, 11.47\,k\Omega)} \tag{5}$$

$$T_J(max) = 125°C + \left(0.422\,W \times 40.8°C/W\right) = 142.2°C \tag{6}$$

To enhance semiconductor long-term operating life, minimize T_J. Take proper measures to provide maximum heat removal through both heat conduction and radiation to help keep T_J to the lowest possible level. These proper measures include maximizing the PCB copper area to which the package thermal pad is soldered. The copper area serves as the traditional heat sink. The top layer copper is often easiest to route and is most often exposed to open air. PCB internal planes and the exposed bottom plane can also be used as heat sinks, but the connections are made with vias having higher thermal resistance. The OPA593EVM uses a board design that provides a highly effective thermal layout. The board design encompasses a large top-side copper area, and has heat conduction paths to other planes on the board. Additionally, other higher power-dissipating components are kept physically distant from the OPA593 to better accommodate heat removal by radiation.

8.4.2 Layout Example

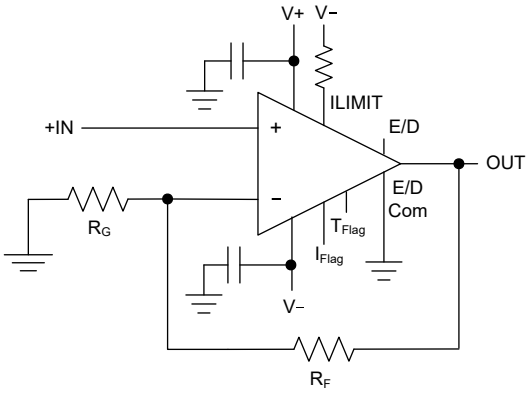


図 8-4. Schematic Representation

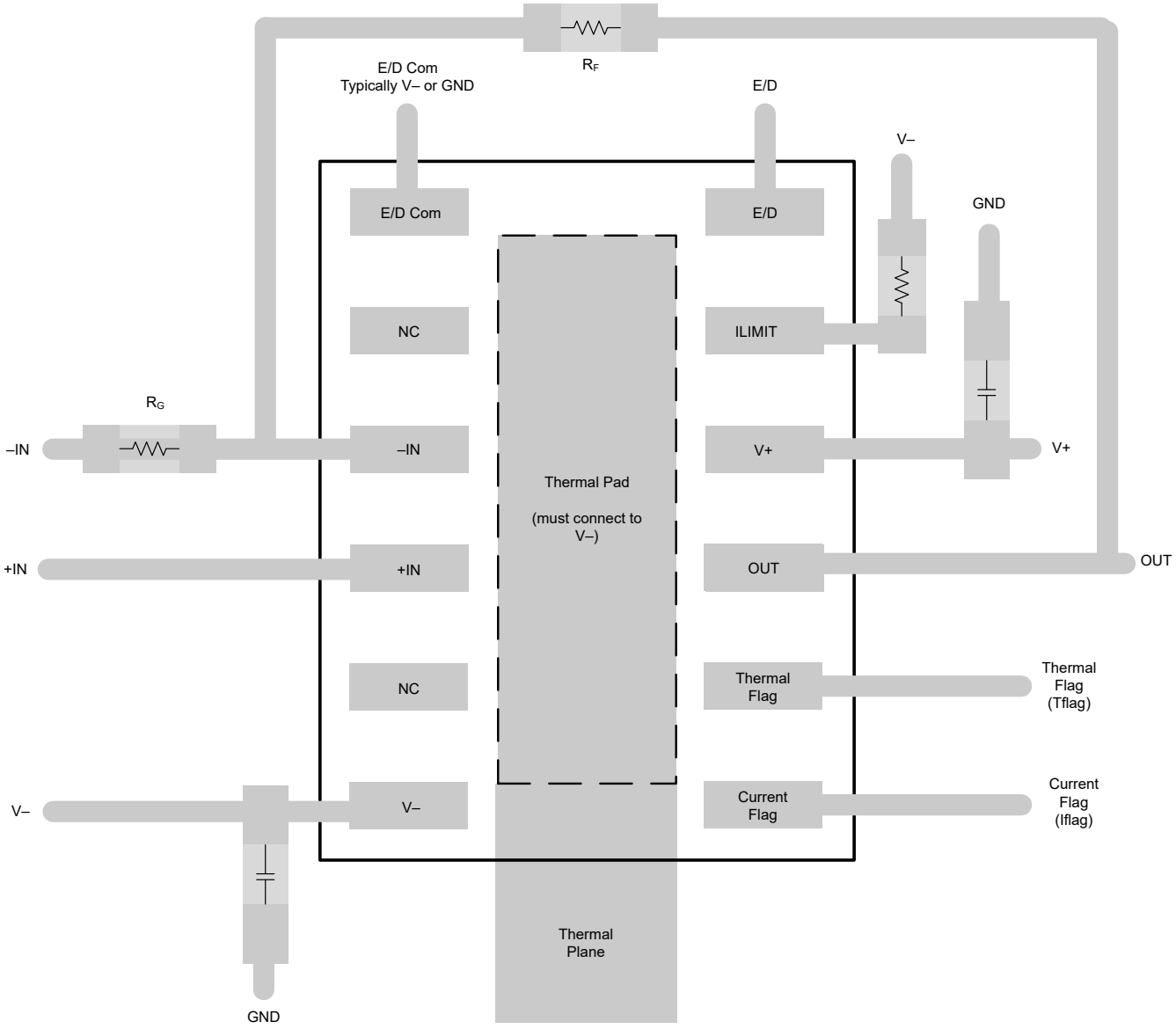


図 8-5. OPA593 Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

9.1.1.2 TINA-TI™ シミュレーション・ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア・フォルダから、無償の TINA-TI シミュレーション・ソフトウェアをダウンロードしてください。

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA593DNTR	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTR.A	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTRG4	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTRG4.A	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTT	Active	Production	WSON (DNT) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTT.A	Active	Production	WSON (DNT) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

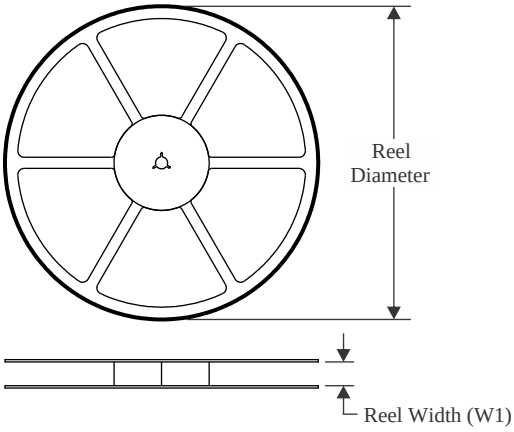
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

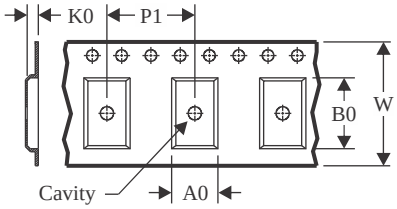
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

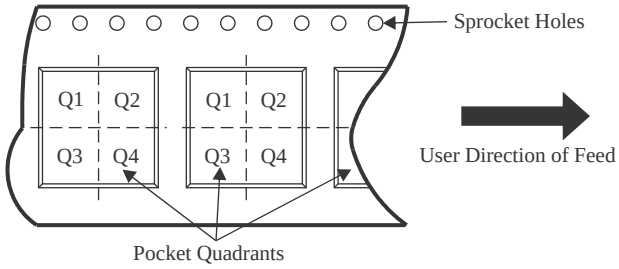


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

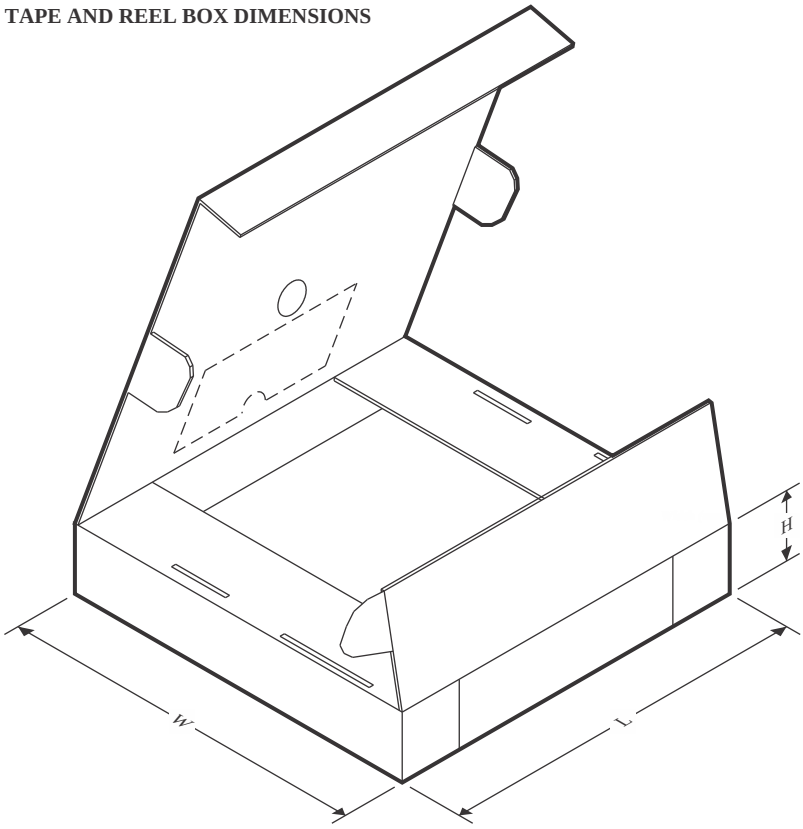
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA593DNTR	WSON	DNT	12	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA593DNTRG4	WSON	DNT	12	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA593DNTT	WSON	DNT	12	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

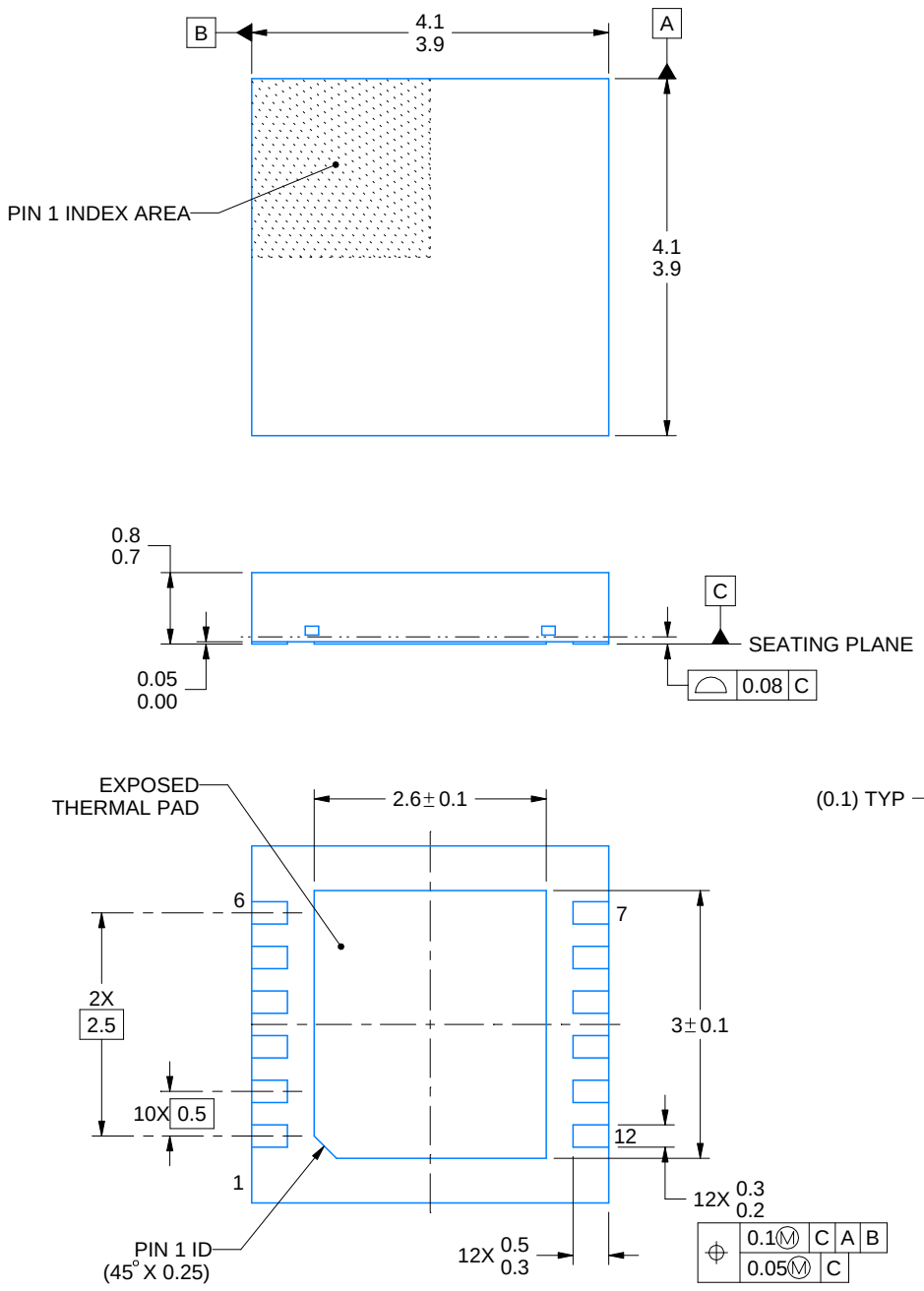
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA593DNTR	WSON	DNT	12	5000	367.0	367.0	35.0
OPA593DNTRG4	WSON	DNT	12	5000	367.0	367.0	35.0
OPA593DNTT	WSON	DNT	12	250	210.0	185.0	35.0

DNT0012B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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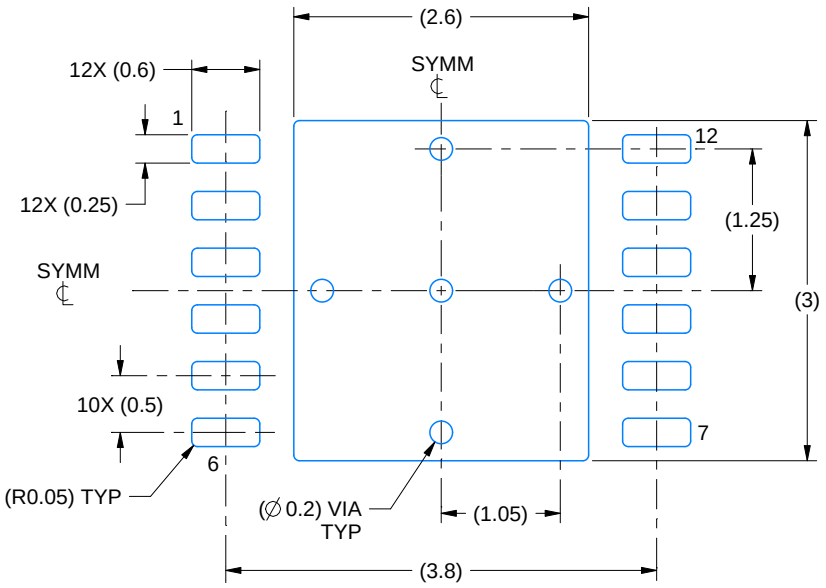
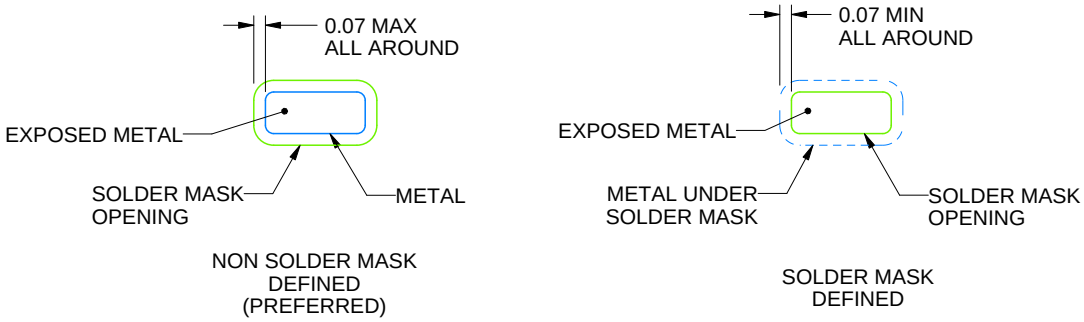
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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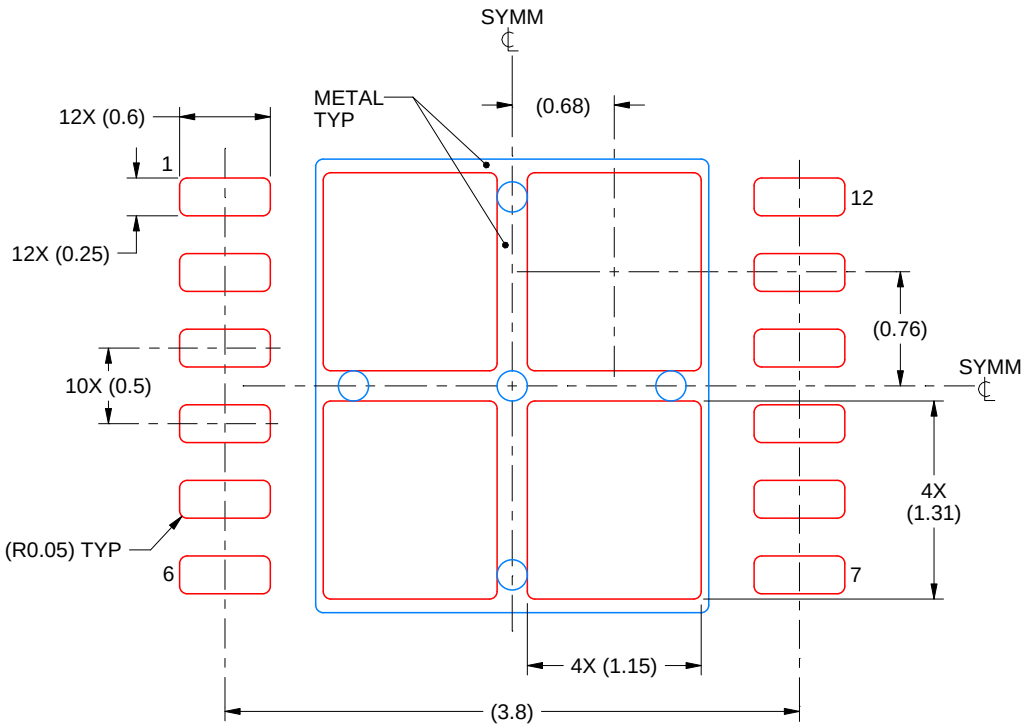
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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