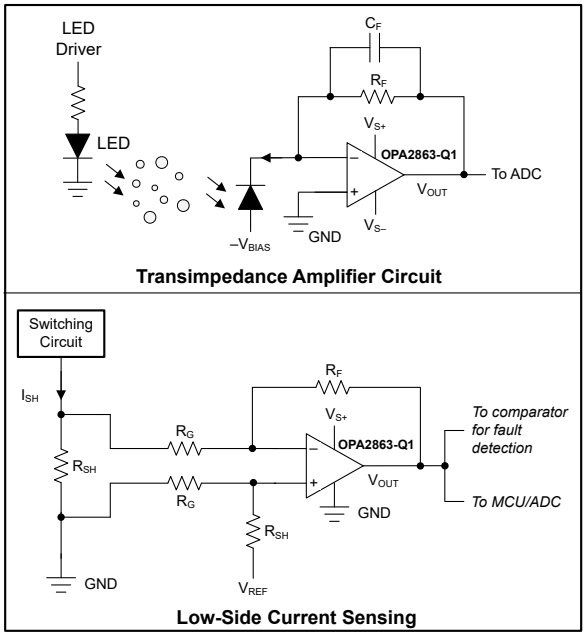
OPA2863-Q1 車載用、低消費電力、110MHz、レール・ツー・レール入出力アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 広い帯域幅
  - ユニティ・ゲイン帯域幅:110MHz
  - ゲイン帯域幅積:50MHz
- 低い消費電力
  - 静止電流:700µA/チャネル (代表値)
  - 電源電圧:2.7V～12.6V
- 入力電圧ノイズ:5.9nV/√Hz
- スルーレート:105V/µs
- レール・ツー・レール入出力
- HD_2/HD_3:-129dBc/-138dBc (20kHz、$2V_{PP}$ 時)
- その他の機能:
  - 過負荷電力制限
  - 出力短絡保護

2 アプリケーション

- ローサイド電流センシング
- DC/DC コンバータ
- インバータおよびモータ制御
- オンボード・チャージャとワイヤレス・チャージャ
- HVAC 用コンプレッサ
- フォトダイオード TIA インターフェイス
- ヘッド・アップ・ディスプレイ (HUD)



以下のデバイスを使用したアプリケーション回路：OPA2863-Q1

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

3 概要

OPA2863-Q1 は、2.7V～12.6V の電源電圧範囲で動作するように設計された低消費電力、ユニティ・ゲイン安定、レール・ツー・レール入出力の電圧帰還型オペアンプです。OPA2863-Q1 のチャネルあたりの消費電流はわずか 700µA であり、ゲイン帯域幅積は 50MHz、スルーレートは 105V/µs、電圧ノイズ密度は 5.9nV/√Hz です。

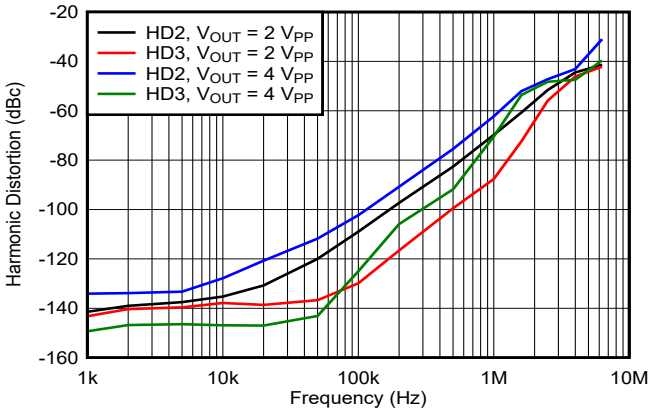
レール・ツー・レール入力段により OPA2863-Q1 は、電流センシングやフォトダイオード・インターフェイスなどの汎用アプリケーションに適しています。レール・ツー・レール入力段は、全入力同相電圧範囲にわたってゲイン帯域幅積とノイズに対してよく調整されているため、広い入力ダイナミック・レンジで優れた性能を実現します。

OPA2863-Q1 は、飽和出力での静止電流 I_Q の増加を抑えるために、過負荷電力制限機能を備えており、電力が問題となるバッテリ駆動システムでの過剰な電力消費を防止できます。出力段は短絡保護されており、これらのデバイスは耐久性が求められる環境に対応しています。

パッケージ情報

部品番号(1)	パッケージ(2)	パッケージ・サイズ(3)
OPA2863-Q1	D (SOIC、8)	4.9mm × 6mm

(1) 関連製品については、「製品比較表」を参照してください。
(2) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(3) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



歪み性能 (G = 1V/V)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2023) to Revision A (July 2023)	Page
• データシートのステータスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	2

5 Device Comparison Table

DEVICE	±V_S (V)	I_Q/CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA2863-Q1	±6.3	0.70	50	105	5.9	Unity-gain-stable. RRIO bipolar amplifier
OPA2365-Q1	±2.75	4.6	50	25	4.5	Unity-gain-stable, zero-crossover, RRIO CMOS amplifier
OPA2607-Q1	±2.75	0.9	50	24	3.8	Gain of 6 V/V stable, NRI/RRO CMOS amplifier
OPA2836-Q1	±2.75	1	110	560	4.6	Unity-gain stable, low-power, NRI/RRO bipolar amplifier

6 Pin Configuration and Functions

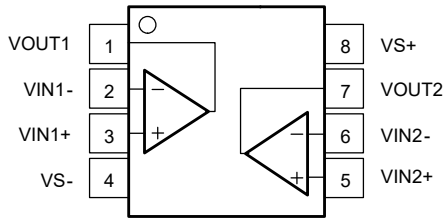

図 6-1. D Package, 8-Pin SOIC (Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2–	6	I	Amplifier 2 inverting input pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	7	O	Amplifier 2 output pin
VS–	4	P	Negative power-supply pin
VS+	8	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt		1	V/µs
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current[2]		±10	mA
I_O	Continuous output current[3]		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Continuous input current limit for both the ESD diodes to the supply pins and amplifier differential input clamp diode. The differential input clamp diodes limit the voltage between the two inputs to 1 V with this continuous input current flowing through these diodes.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{S+} – V_{S–}$	Total supply voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA2863-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	62.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		110		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2-V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		9		ns
	Settling time	To 0.1%, V_{OUT} = 2-V step		57		ns
		To 0.01%, V_{OUT} = 2-V step		70		
	Overshoot/undershoot	V_{OUT} = 2-V step		1		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		70		ns
		G = 1, 0.5-V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–138		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–125		dBc
e_N	Input voltage noise	1/f corner at 25 Hz		5.9		nV/√Hz
i_N	Input current noise	1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}		–124		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–1.5	±0.4	1.5	mV
	Input offset voltage drift	T_A = –40°C to +125°C	–4	±1	4	µV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.6	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	100	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		$V_{S–}$+0.14	$V_{S–}$+0.2	V
		T_A = –40°C to +125°C		$V_{S–}$+0.15	$V_{S–}$+0.22	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.2	V_{S+}–0.14		V
		T_A = –40°C to +125°C	V_{S+}–0.2	V_{S+}–0.15		
	Linear output drive (sourcing and sinking)	V_{OUT} = ±2.5 V, ΔV_{OS} < 1 mV[(1)]	25	30		mA
	Short-circuit current			45		mA

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7.5 Electrical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		700	970	µA
		T_A = –40°C to +125°C			1280	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(2)	100	120		dB
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.5	±0.15	1.5	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C			1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	120		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

7.6 Electrical Characteristics: V_S = 3 V

at G = 1 V/V, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		97		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		26		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1-V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		10		ns
	Settling time	To 0.1%, V_{OUT} = 1-V step		58		ns
		To 0.01%, V_{OUT} = 1-V step		90		
	Overshoot	V_{OUT} = 1-V step		2		%
	Undershoot	V_{OUT} = 1-V step		16		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		95		ns
		G = 1, 0.5-V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–123		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–132		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–109		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–129		dBc
e_N	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
i_N	Input current noise	1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}		–127		dBc

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7.6 Electrical Characteristics: V_S = 3 V (continued)

at G = 1 V/V, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		–1.5	±0.4	1.5	mV
	Input offset voltage drift	T_A = –40°C to +125°C	–4	±1	4	μV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	μA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.4	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		V_{S-}–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} – 0.2 V to V_{S+} – 1.6 V	94	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		V_{S-}+ 0.13	V_{S-}+ 0.15	V
		T_A = –40°C to +125°C		V_{S-}+ 0.13	V_{S-}+ 0.16	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.15	V_{S+}–0.13		V
		T_A = –40°C to +125°C	V_{S+}–0.15	V_{S+}–0.13		
	Linear output drive (sourcing and sinking)	V_{OUT} = ±0.7 V, ΔV_{OS} < 1 mV(1)	23	33		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		690	910	μA
		T_A = –40°C to +125°C			1180	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(2)	100	120		dB
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.5	±0.15	1.5	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	μA
		T_A = –40°C to +125°C			1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	115		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

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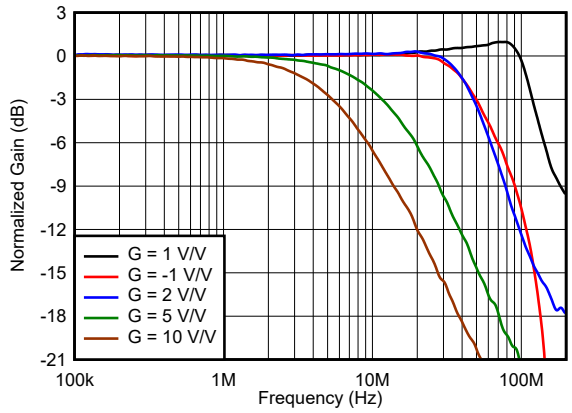
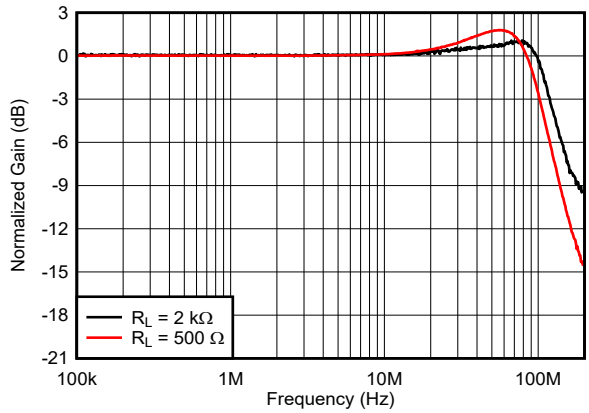
7.7 Typical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



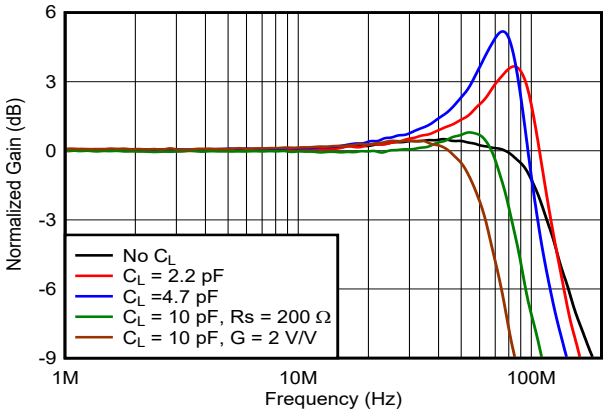
V_{OUT} = 20 mV_{PP}

図 7-1. Small-Signal Frequency Response vs Gain



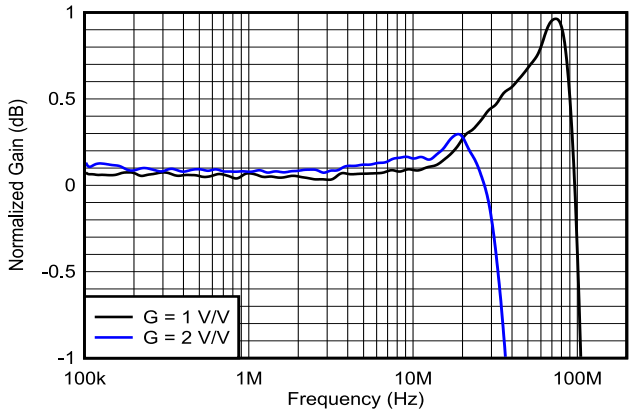
V_{OUT} = 20 mV_{PP}

図 7-2. Small-Signal Frequency Response vs Output Load



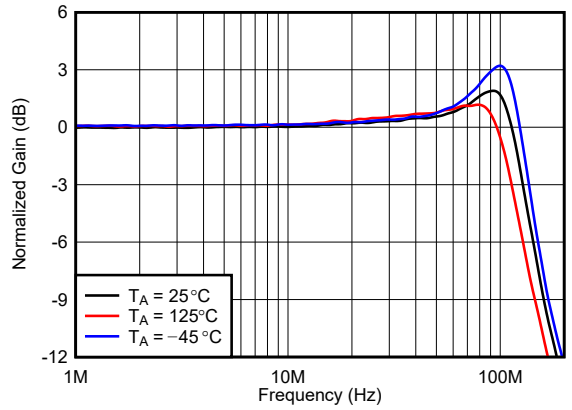
V_{OUT} = 20 mV_{PP}

図 7-3. Frequency Response vs Load Capacitance



V_{OUT} = 20 mV_{PP}

図 7-4. Small-Signal Response Flatness vs Gain



V_{OUT} = 20 mV_{PP}

図 7-5. Frequency Response vs Ambient Temperature

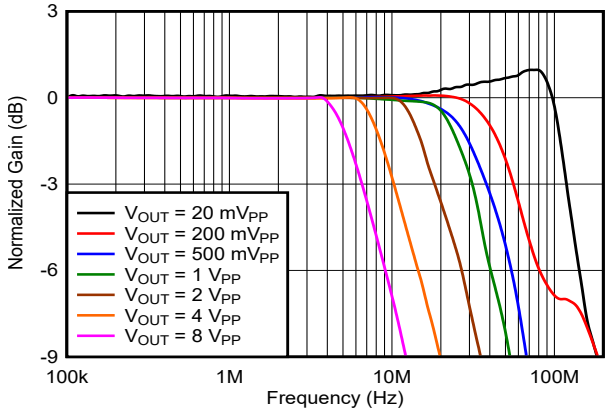


図 7-6. Frequency Response vs Output Voltage

7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

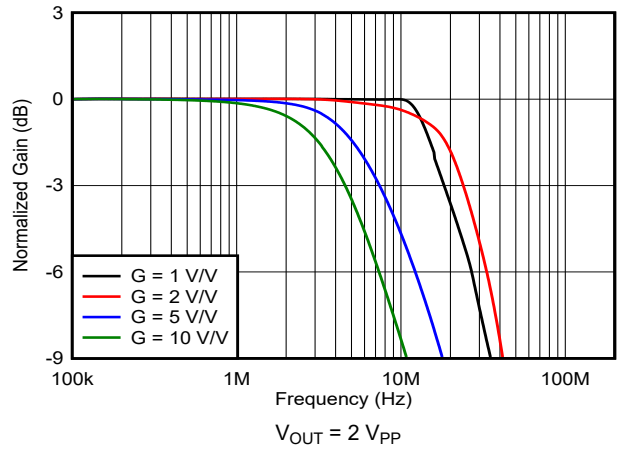


図 7-7. Large-Signal Frequency Response vs Gain

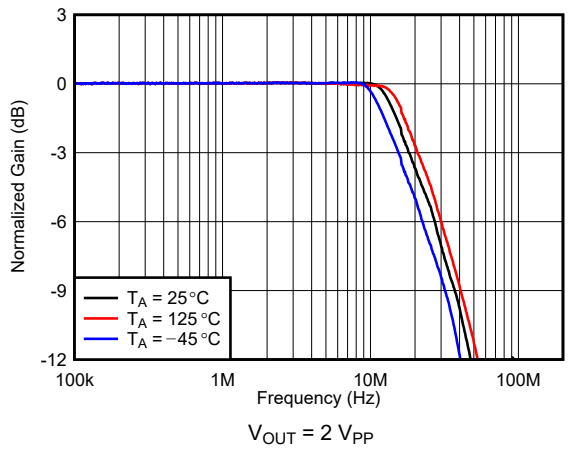


図 7-8. Frequency Response vs Ambient Temperature

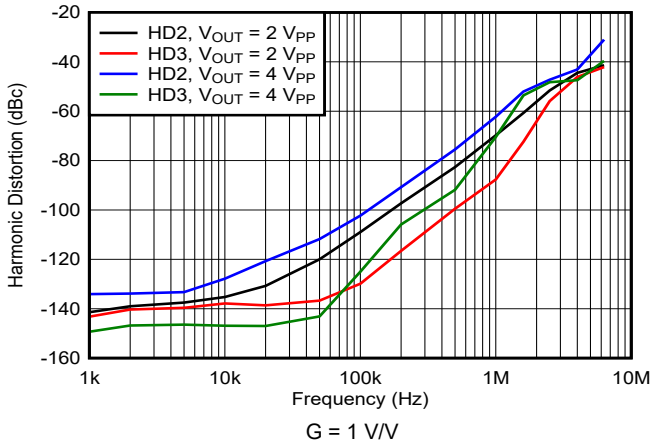


図 7-9. Harmonic Distortion vs Frequency

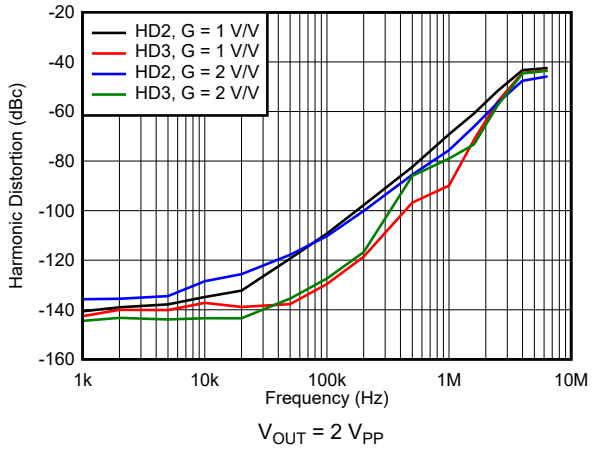


図 7-10. Harmonic Distortion vs Gain

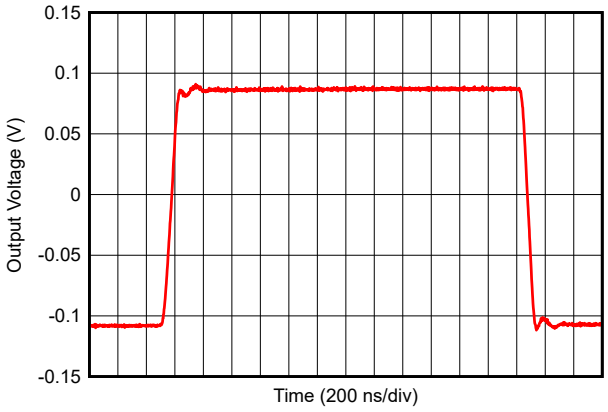


図 7-11. Small-Signal Transient Response

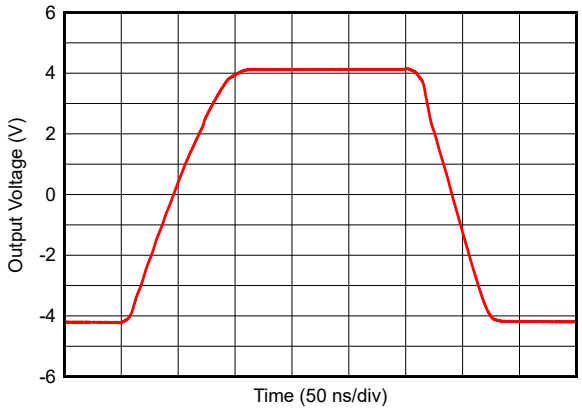


図 7-12. Large-Signal Transient Response

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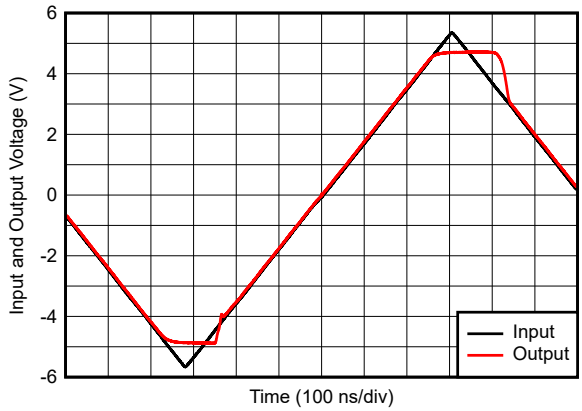
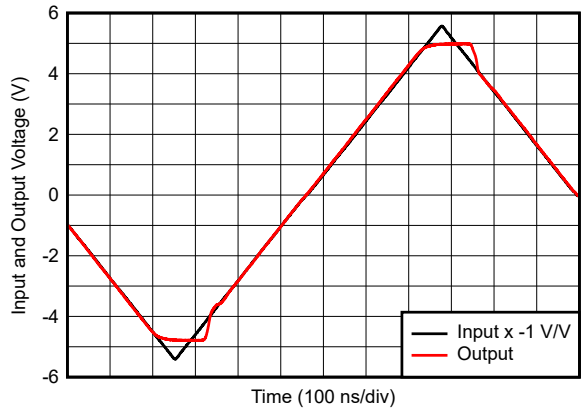
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



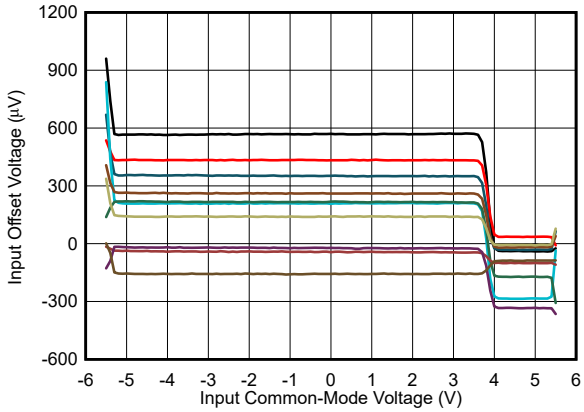
G = 1 V/V

図 7-13. Input Overdrive Recovery



G = –1 V/V

図 7-14. Output Overdrive Recovery



Measured for 10 units

図 7-15. Input Offset Voltage vs Input Common-Mode Voltage

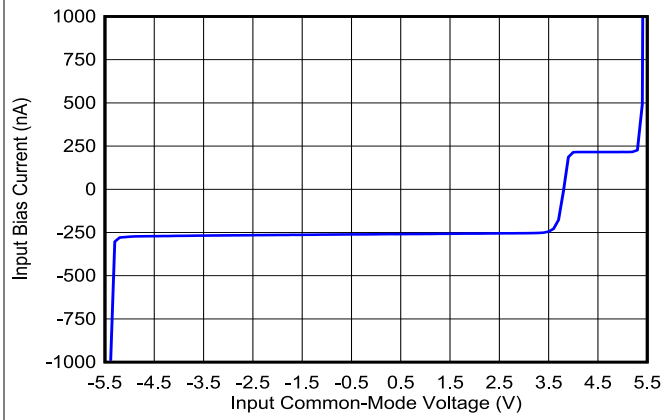


図 7-16. Input Bias Current vs Input Common-Mode Voltage

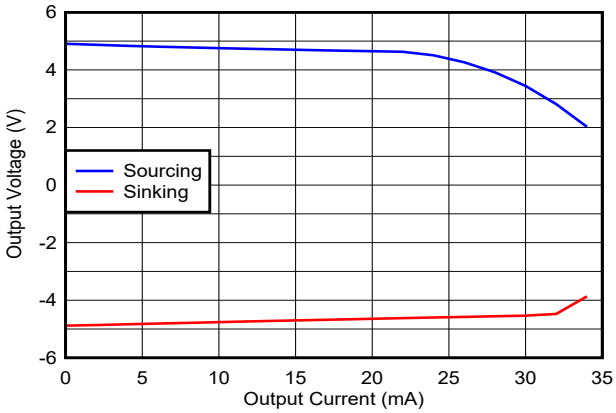
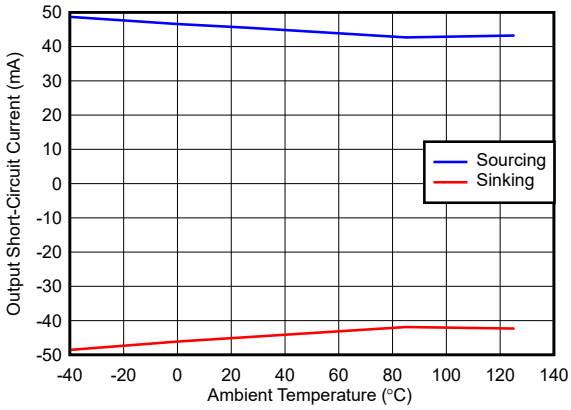


図 7-17. Output Voltage vs Load Current

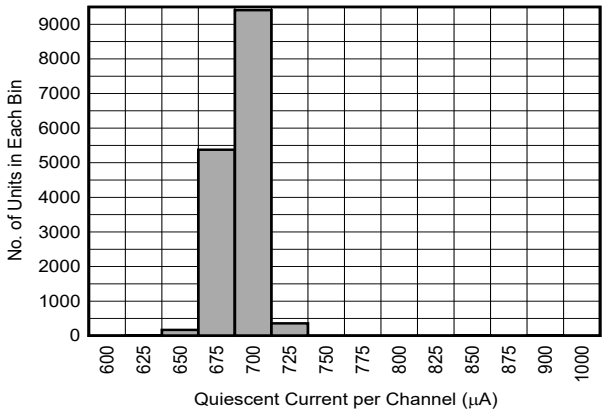


Output saturated and then short-circuited to opposite supply

図 7-18. Output Short-Circuit Current vs Ambient Temperature

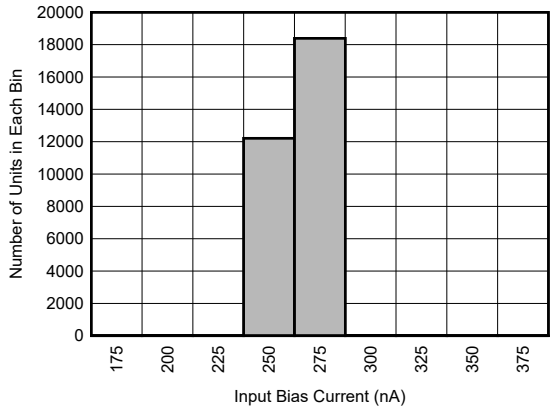
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



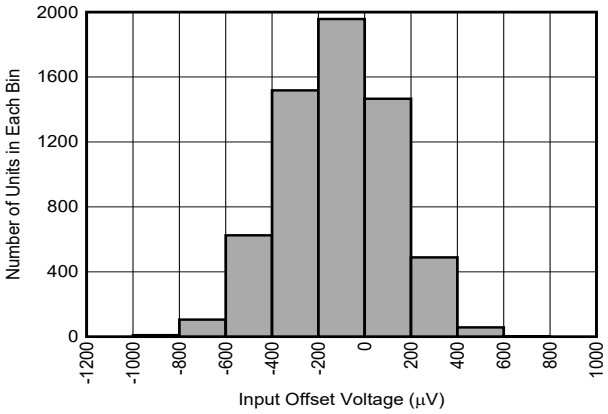
μ = 678 µA, σ = 13 µA

図 7-19. Quiescent Current Distribution



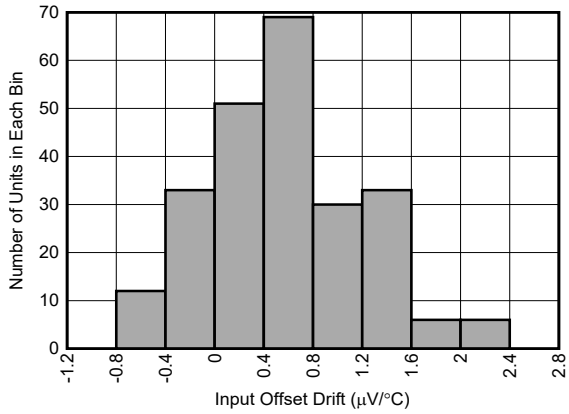
μ = 251 nA, σ = 5.6 nA

図 7-20. Input Bias Current Distribution



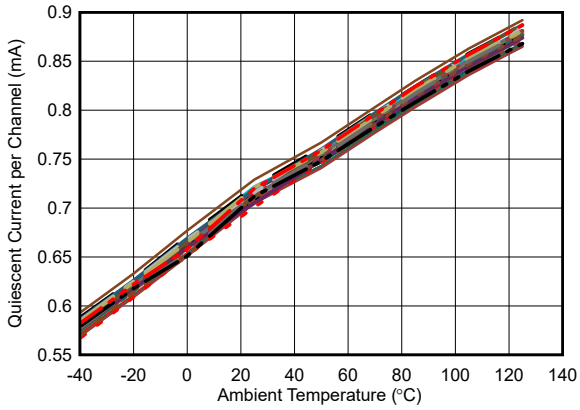
μ = –116 µV, σ = 234 µV

図 7-21. Input Offset Voltage Distribution



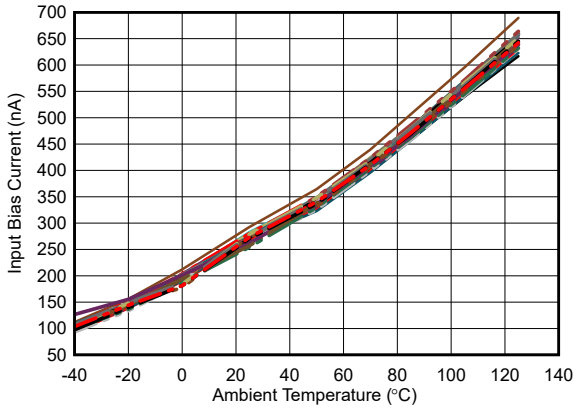
μ = 0.57 µV/°C, σ = 0.64 µV/°C

図 7-22. Input Offset Voltage Drift Distribution



35 units

図 7-23. Quiescent Current vs Ambient Temperature



35 units

図 7-24. Input Bias Current vs Ambient Temperature

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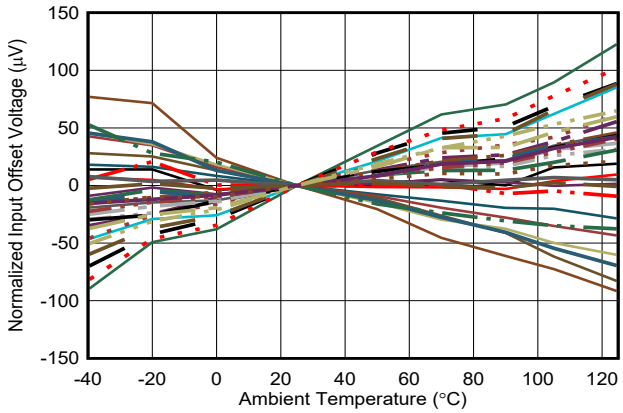
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

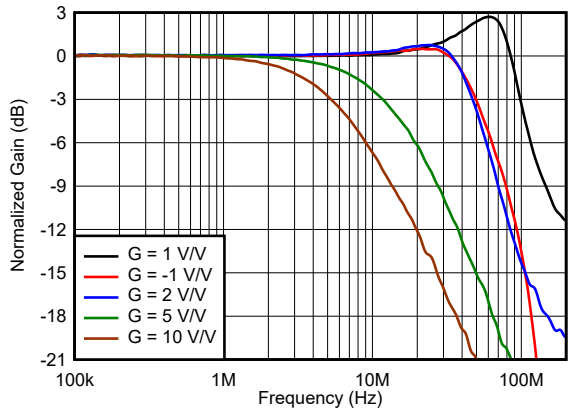


Normalized to 25°C values, 32 units

図 7-25. Input Offset Voltage vs Ambient Temperature

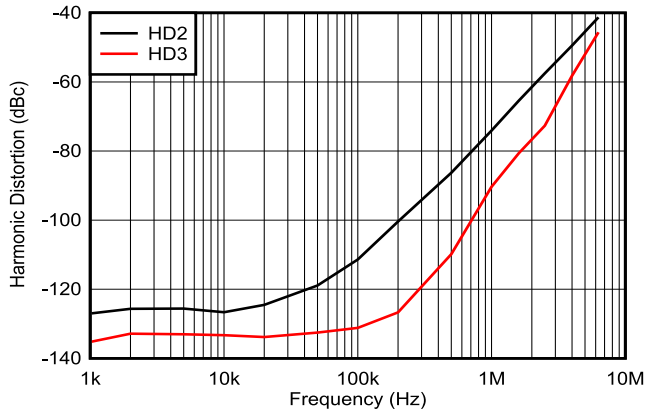
7.8 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, V_{S-} = 0 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

図 7-26. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

図 7-27. Harmonic Distortion vs Frequency

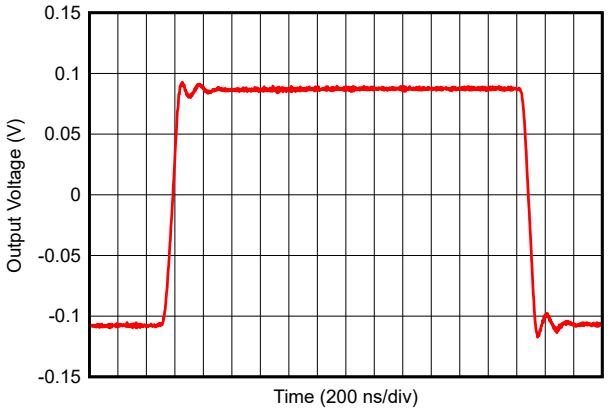


図 7-28. Small-Signal Transient Response

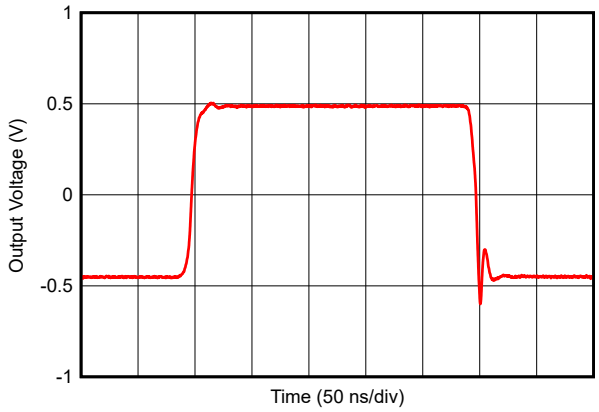
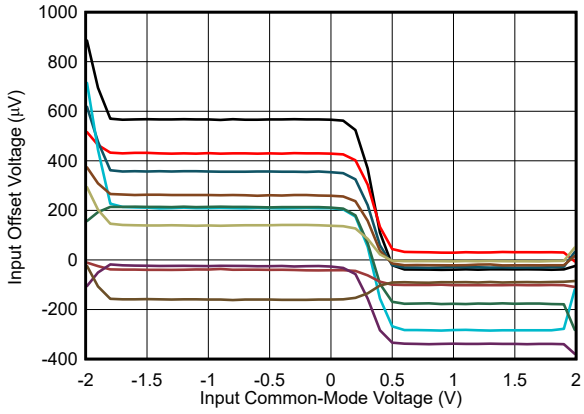


図 7-29. Large-Signal Transient Response



Measured for 10 units

図 7-30. Input Offset Voltage vs Input Common-Mode Voltage

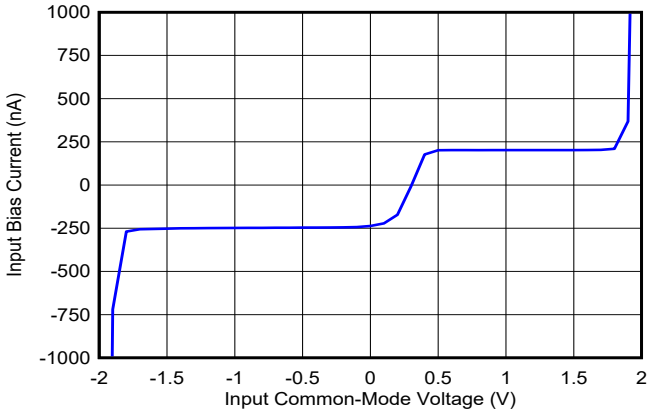


図 7-31. Input Bias Current vs Input Common-Mode Voltage

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7.8 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, V_{S-} = 0 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

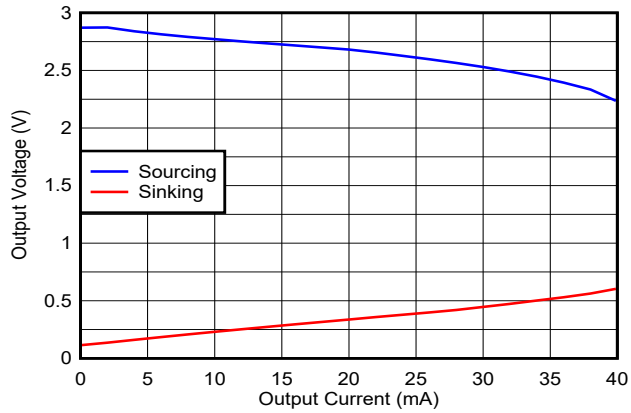
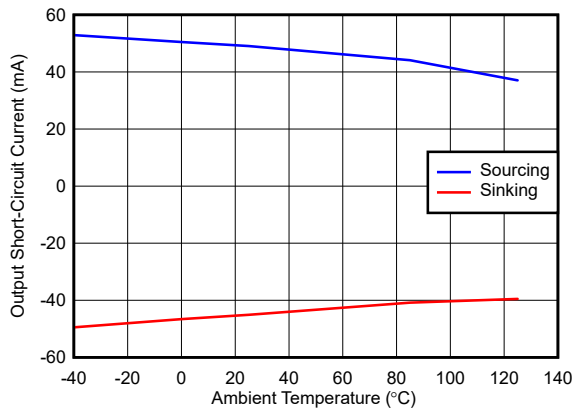


図 7-32. Output Voltage vs Load Current

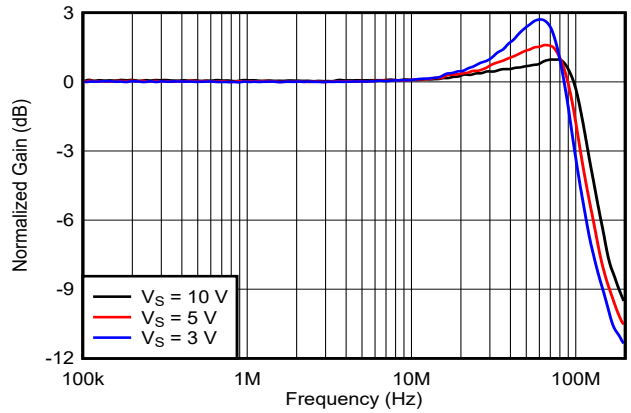


Output saturated and then short-circuited to other supply

図 7-33. Output Short-Circuit Current vs Ambient Temperature

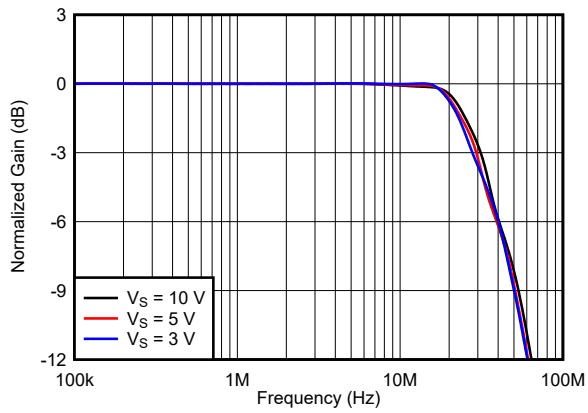
7.9 Typical Characteristics: V_S = 3 V to 10 V

at G = 1 V/V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

図 7-34. Frequency Response vs Supply Voltage



V_{OUT} = 1 V_{PP}

図 7-35. Frequency Response vs Supply Voltage

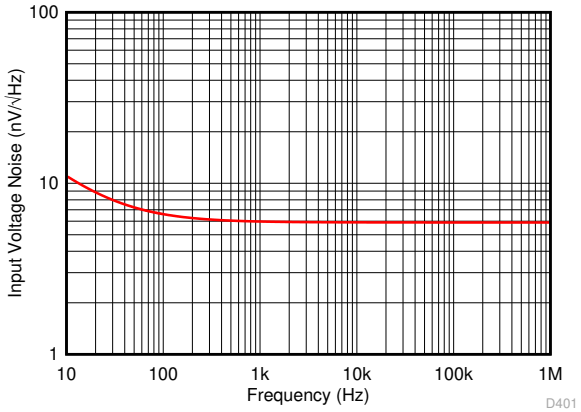


図 7-36. Input Voltage Noise Density vs Frequency

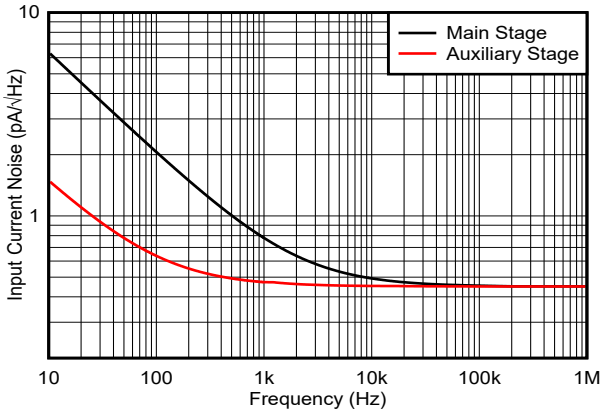


図 7-37. Input Current Noise Density vs Frequency

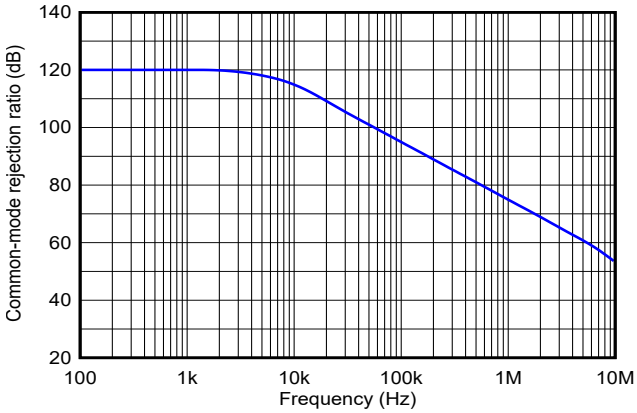


図 7-38. Common-Mode Rejection Ratio vs Frequency

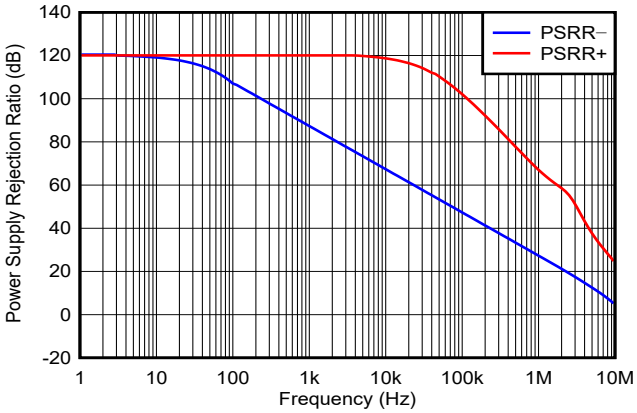


図 7-39. Power Supply Rejection Ratio vs Frequency

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7.9 Typical Characteristics: V_S = 3 V to 10 V (continued)

at G = 1 V/V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

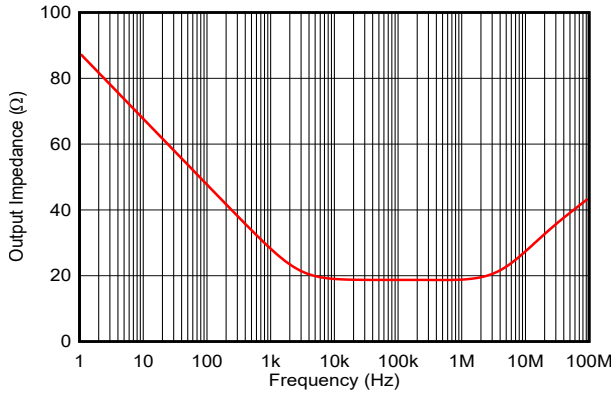
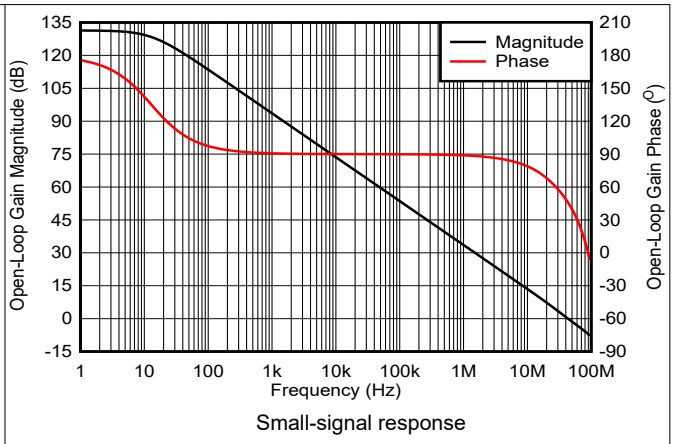
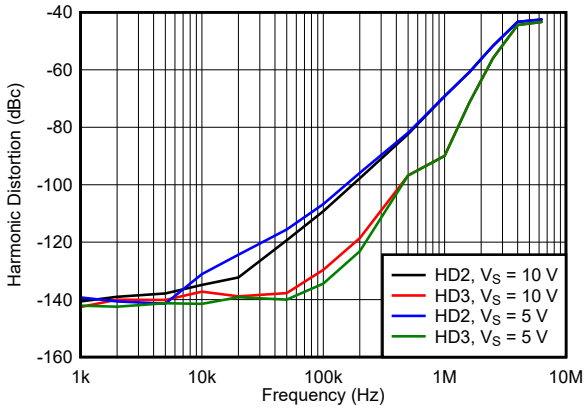


図 7-40. Open-Loop Output Impedance vs Frequency



Small-signal response

図 7-41. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 2 V_{PP}

図 7-42. Harmonic Distortion vs Supply Voltage

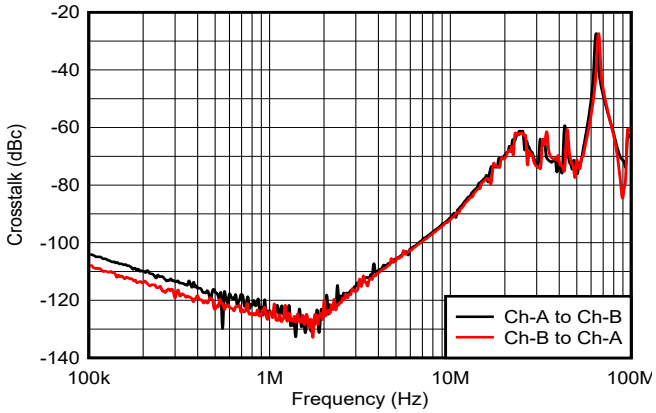


図 7-43. Crosstalk vs Frequency

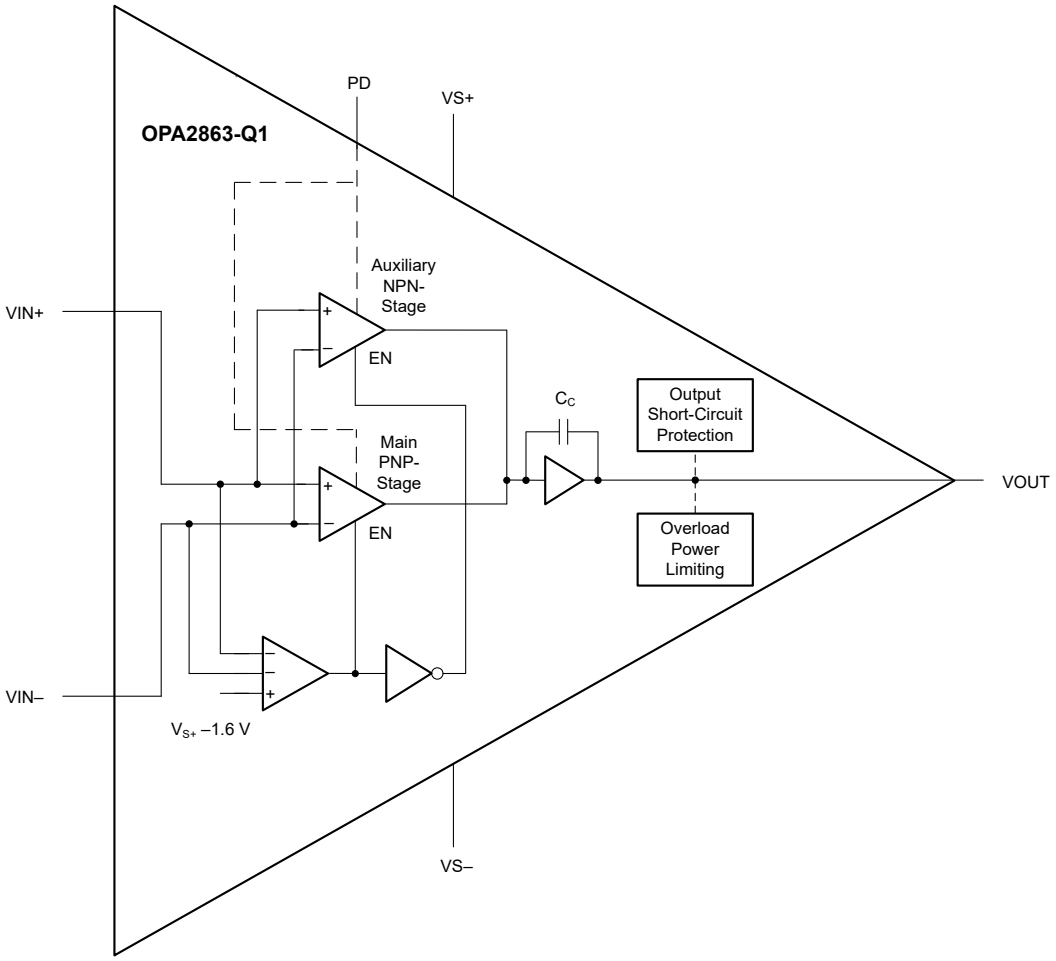
8 Detailed Description

8.1 Overview

The OPA2863-Q1 is a low-power, 50-MHz, rail-to-rail input and output (RRIO), bipolar, voltage-feedback operational amplifier with a voltage noise density of 5.9 nV/√Hz and 1/f noise corner at 25 Hz. The OPA2863-Q1 works with a wide-supply voltage range of 2.7 V to 12.6 V, and consume only 700 µA quiescent current. The OPA2863-Q1 operates with a 2.7 V supply, is RRIO capable, consumes low-power, which makes this a great amplifier for 3.3-V or lower-voltage applications that require excellent ac performance. The main and auxiliary input stages of the amplifier are matched for gain bandwidth product (GBW), noise, and offset voltage and designed for applications that require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. For more details of this overload power limit feature, see セクション 8.3.2.1. The output of the amplifier is protected against short-circuit fault conditions.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Stage

The OPA2863-Q1 includes a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from V_{S-} – 0.2 V to V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 5.9 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The auxiliary NPN input stage does not use the slew-boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages causes a crossover distortion that must be considered in high-frequency applications requiring excellent linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

The OPA2863-Q1 is a bipolar amplifier; therefore, the two inputs are protected with antiparallel back-to-back diodes between them, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the antiparallel diodes begin to conduct in very fast input or output transient conditions. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPA2863-Q1 features a rail-to-rail output stage with possible signal swing from V_{S-} + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom to either of the supplies causes output signal clipping and introduces distortion.

The OPA2863-Q1 integrates an output short-circuit protection circuit, which makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPA2863-Q1 includes overload power limiting that limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier output saturates, the two inputs are pulled apart, which can enable the slew-boost circuit. The input differential voltage is an error voltage in negative feedback that the amplifier core nullifies by engaging the slew-boost circuit and driving the output stage deeper into saturation. After the input to an amplifier attains a value large enough to saturate the output, any further increase in this input excitation results in a finite input differential voltage. As the output stage transistor is pushed deeper into saturation, the base-to-collector current gain (h_{FE}) drops with an increase in the base and collector current, and an increase in the device quiescent current. This increase in quiescent current can cause a catastrophic failure in multichannel, high-gain, high-density front-end designs, and reduce operating lifetime in portable, battery-powered systems.

The OPA2863-Q1 overload power limiting includes an intelligent output saturation-detection circuit that limits the device quiescent current to 2.2-mA per channel under dc overload conditions. This increase in quiescent current is smaller with ac input or output and output saturation duration for only a fraction of the overall signal time period. 表 8-1 compares the increase in quiescent current with 50-mV input overdrive for OPA2863-Q1 and other voltage-feedback amplifiers without overload power limit.

表 8-1. Quiescent Current with Saturated Outputs

DEVICE	INPUT DIFFERENTIAL VOLTAGE	QUIESCENT CURRENT DURING OVERLOAD	INCREASE IN I_Q FROM STEADY-STATE CONDITION
OPA2863-Q1 with overload power limit	50 mV	1.1 mA	1.57 ×
Competitor amplifier without overload power limit	50 mV	1.96 mA	3.43 ×

8.3.3 ESD Protection

図 8-1 shows that all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which makes sure that the current through the ESD diodes remains within the rated value. OPA2863-Q1 is a bipolar amplifier; therefore, the two inputs are protected with antiparallel, back-to-back diodes between the inputs that limits the maximum input differential voltage to approximately 1 V. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

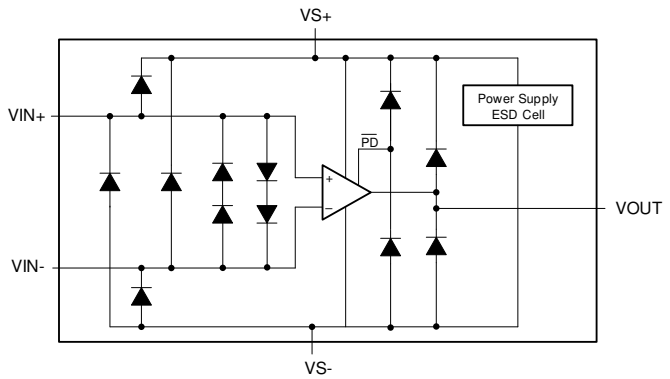

図 8-1. Internal ESD Protection

8.4 Device Functional Modes

The OPAx863-Q1 is operational with a supply voltage greater than 2.7 V (±1.35 V). The maximum recommended supply voltage is 12.6 V (±6.3 V). The OPAx863-Q1 can be used with unipolar, bipolar or asymmetric supplies.

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9 Application and Implementation

注

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9.1 Application Information

The OPA2863-Q1 is a classic voltage-feedback amplifier with two high-impedance inputs and a low-impedance output. This device has a GBW of 50 MHz, 5.9 nV/√Hz of noise, RRIO capability, and precision performance, consuming only 700 µA quiescent current per channel. These features make the OPA2863-Q1 an excellent choice for use in low-side current sensing, ADC input driver, and reference buffering with fast settling, buffers, high gain and filter circuits. The overload power limit makes the OPA2863-Q1 truly low-power in high-gain, multichannel systems, limiting any increase in quiescent current during output overload conditions.

9.2 Typical Applications

9.2.1 Low-Side Current Sensing

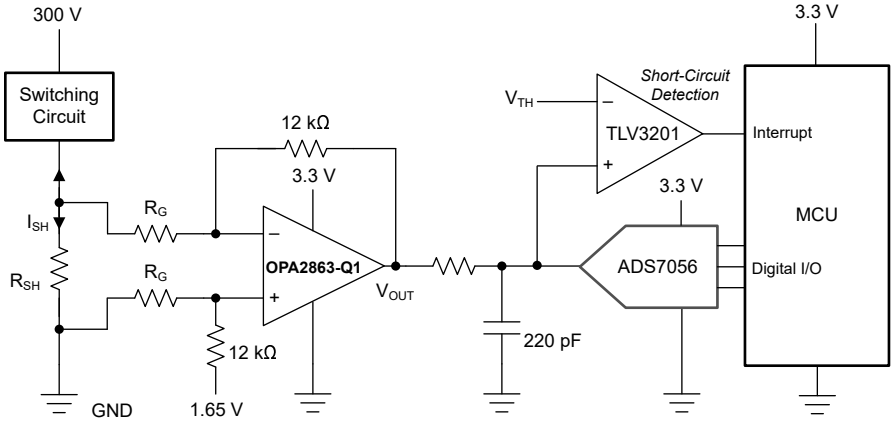

図 9-1. Low-Side Current Sensing in Power Converters

Power converters use current-mode feedback control for excellent transient response and multiphase load sharing. Inverter stages control the phase currents for torque control in motor drives. As a result of the simplicity and low-cost, many of these topologies use difference-amplifier-based, low-side current sensing. 図 9-1 shows the use of the OPA2863-Q1 in a difference amplifier circuit for low-side current sensing.

9.2.1.1 Design Requirements

表 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

9.2.1.2 Detailed Design Procedure

In a difference amplifier circuit, the output voltage is given by:

$$V_0 = \frac{R_F}{R_G} I_{SH} R_{SH} + V_{REF} \tag{1}$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10 V here) seen by the circuit, and is given by:

$$R_G = \frac{V_{IN}\,(max) - V_D - V_S}{I_D\,(max)} \tag{2}$$

where

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit
- V_D is the forward voltage drop of ESD diodes at the amplifier input
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input

For a difference amplifier gain of 20 V/V, an R_F of 12 kΩ and R_G of 600 Ω are used. With a clock frequency of 40 MHz and ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. 表 9-1 shows the simulation results for the circuit in 図 9-1. The worst-case peak-to-peak input transient condition is simulated. The output of the OPA2863-Q1 settles to within 0.1% accuracy within 543 ns. If using a slower clock frequency with the ADC is desired, then the acquisition time reduces with the same sampling rate, which degrades measurement accuracy. Alternatively, the sampling rate can be reduced to recover the required acquisition time and 0.1% accuracy.

9.2.1.3 Application Curve

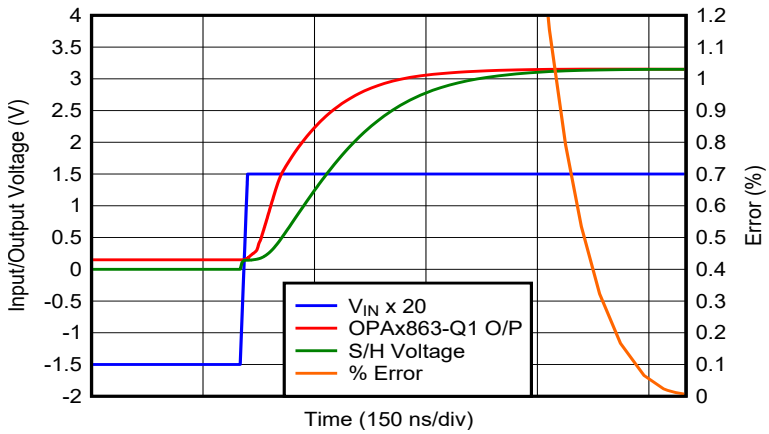

図 9-2. 0.1% Settling Performance

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9.2.2 Front-End Gain and Filtering

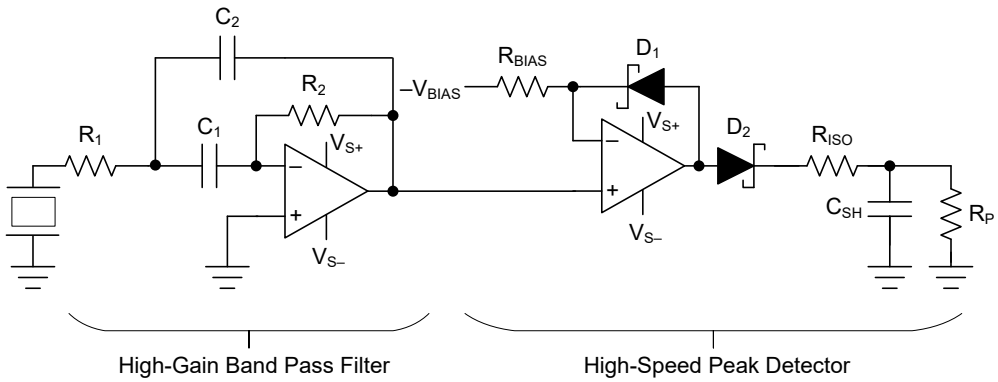

図 9-3. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. 図 9-3 shows a high-gain narrow bandpass filter and peak detector circuit using the OPA2863-Q1. The signal at the frequency of interest is filtered out, gained, and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPA2863-Q1 is used with the 50-MHz GBW to add a single-stage gain, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

9.3 Power Supply Recommendations

The OPA2863-Q1 is intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPA2863-Q1 operates on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply has numerous advantages. The dc errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, ac performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPA2863-Q1) requires careful attention to board layout parasitics and external component types. The *DEM-OPA-SO-2A Demonstration Fixture* user's guide can be used as a reference when designing the circuit board. Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA2863-Q1.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Keep resistor values as low as possible and consistent with load-driving considerations. Lowering the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. Lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifier output load network.

9.4.2 Layout Example

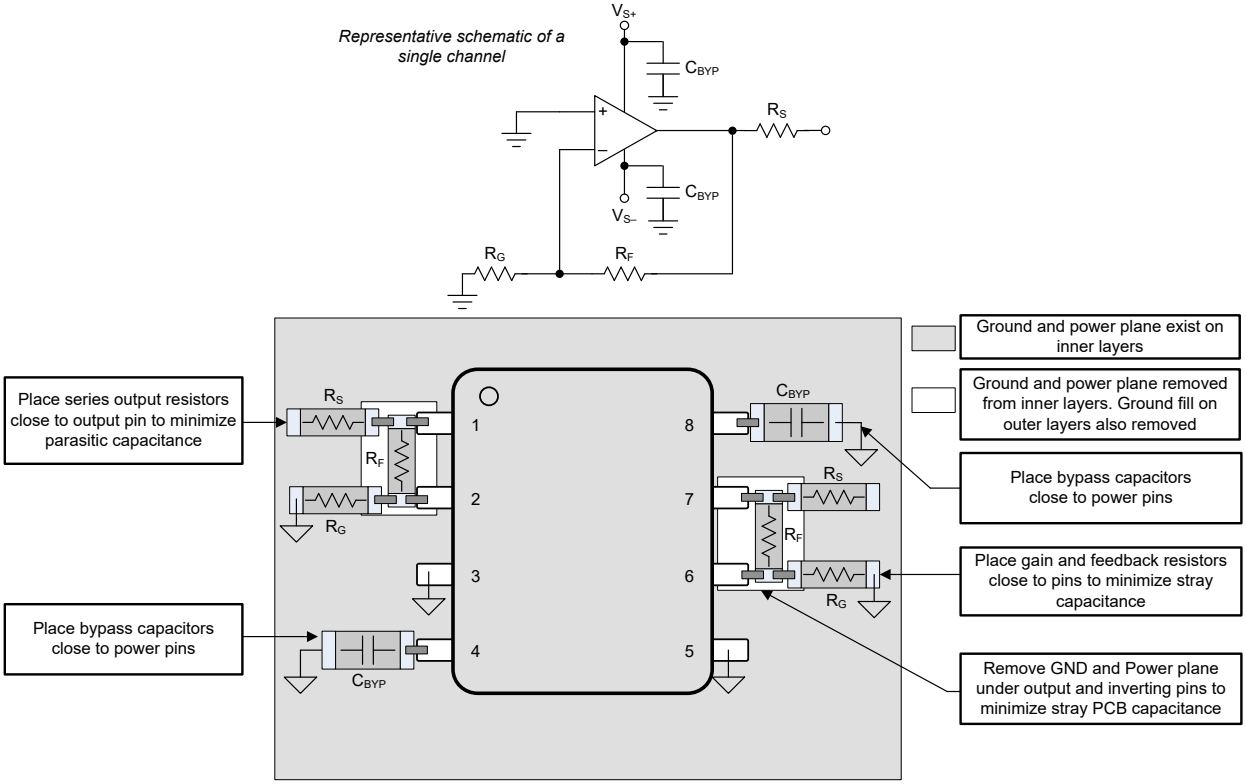

図 9-4. Layout Recommendation for Dual-Channel D Package

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DEM-OPA-SO-2A Demonstration Fixture* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2863QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2863Q
OPA2863QDRQ1.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2863Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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OTHER QUALIFIED VERSIONS OF OPA2863-Q1 :

- Catalog : OPA2863

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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