SBOS274C – JUNE 2003 – REVISED AUGUST 2008

Dual, Wideband, Low-Noise, Voltage-Feedback Operational Amplifier

FEATURES

- HIGH BANDWIDTH: 300MHz (G = +10)
- LOW INPUT VOLTAGE NOISE: 1.2nV/√Hz
- VERY LOW DISTORTION: –100dBc (5MHz)
- HIGH SLEW RATE: 600V/µs
- HIGH DC ACCURACY: V_{IO} = 150µV
- LOW SUPPLY CURRENT: 12.6mA/ch
- HIGH GAIN BANDWIDTH PRODUCT: 1650MHz
- STABLE FOR GAINS ≥ +7V/V

APPLICATIONS

- HIGH DYNAMIC RANGE ADC PREAMPS
- LOW-NOISE, WIDEBAND, TRANSIMPEDANCE AMPLIFIERS
- WIDEBAND, HIGH GAIN AMPLIFIERS
- LOW-NOISE DIFFERENTIAL RECEIVERS
- VDSL LINE RECEIVERS
- ULTRASOUND CHANNEL AMPLIFIERS
- SECURITY SENSOR FRONT ENDS

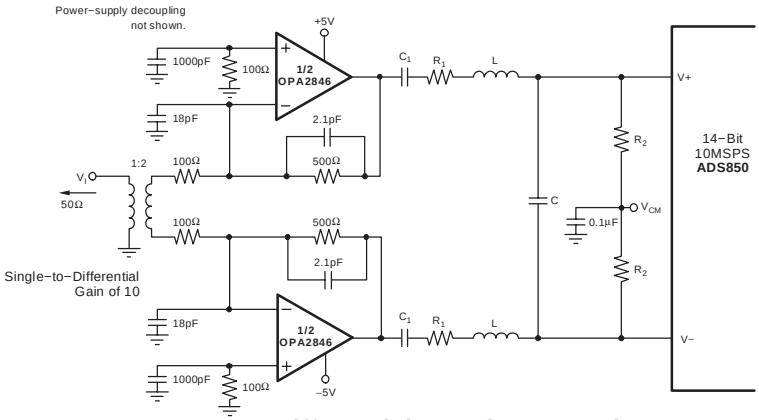
DESCRIPTION

The OPA2846 provides two very low-noise, high gain bandwidth, voltage-feedback op amps in a single package. Operating from a low 12.6mA/channel quiescent current, each channel provides a 1.2nV/√Hz input voltage noise with a 1.65GHz gain bandwidth product. Minimum stable gain is specified at +7V/V while exceptional flatness is ensured at a gain of +10V/V.

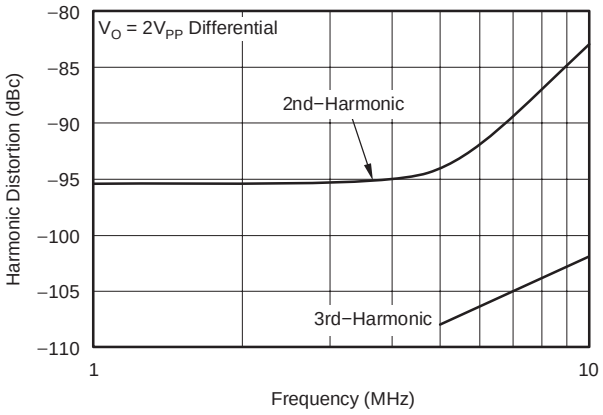
The combination of low noise, high slew rate (600V/µs) and broad bandwidth allow very high SFDR differential receivers to be implemented. Additionally, decompensated, low-noise, voltage-feedback op amps are ideal for broadband transimpedance requirements. The dual channel OPA2846 provides matched channels for high-speed transimpedance requirements. With over 200MHz bandwidth at a gain of 20dB, excellent gain and phase matching are provided at IF frequencies for matched I and Q channel amplifiers.

OPA2846 RELATED PRODUCTS

SINGLES	INPUT NOISE VOLTAGE (nV/√Hz)	GAIN BANDWIDTH PRODUCT (MHz)
OPA842	2.6	200
OPA843	2.0	800
OPA846	1.2	1750
OPA847	0.85	3900



Differential, 14-Bit, ADC Driver



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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range: D	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Charge Device Model)	1500V
(Machine Model)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

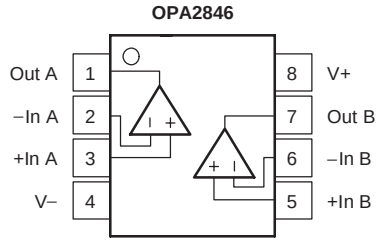
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2846	SO-8	D	−40°C to +85°C	OPA2846	OPA2846ID OPA2846IDR	Rails, 100 Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TOP VIEW **SO**



ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are 100% tested at **+25°C.**

R_F = 453Ω, R_L = 100Ω, and G = +10, unless otherwise noted. See Figure 1 for AC performance.

PARAMETER	TEST CONDITIONS	OPA2846ID						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
AC Performance (see Figure 1)								
Closed-Loop Bandwidth	G = +7, R_G = 50Ω, V_O = 200mV_{PP}	425				MHz	typ	C
	G = +10, R_G = 50Ω, V_O = 200mV_{PP}	300	250	225	200	MHz	min	B
	G = +20, R_G = 50Ω, V_O = 200mV_{PP}	100	80	76	70	MHz	min	B
Gain Bandwidth Product	G ≥ +40	1650	1250	1225	1200	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +10, R_L = 100Ω, V_O = 200mV_{PP}	100	40	35	30	MHz	min	B
Peaking at a Gain of +7		3				dB	typ	C
Harmonic Distortion	G = +10, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	−76	−70	−68	−66	dBc	max	B
	R_L = 500Ω	−100	−89	−87	−85	dBc	max	B
3rd-Harmonic	R_L = 100Ω	−109	−95	−92	−90	dBc	max	B
	R_L = 500Ω	−112	−105	−101	−96	dBc	max	B
2-Tone, 3rd-Order Intercept	G = +10, f = 10MHz	44	41	40	38	dBm	min	B
Input Voltage Noise	f > 1MHz	1.2	1.3	1.4	1.5	nV/√Hz	max	B
Input Current Noise	f > 1MHz	2.8	3.5	3.6	3.6	pA/√Hz	max	B
Rise-and-Fall Time	0.2V Step	1.3	1.6	1.7	1.9	ns	max	B
Slew Rate	2V Step	600	500	400	350	V/µs	min	B
Settling Time to 0.01%	2V Step	18				ns	typ	C
0.1%	2V Step	12	14	16	18	ns	max	B
1%	2V Step	8	10	12	14	ns	max	B
Differential Gain	G = +10, NTSC, R_L = 150Ω	0.02				%	typ	C
Differential Phase	G = +10, NTSC, R_L = 150Ω	0.02				deg	typ	C
Channel-to-Channel Crosstalk	Input Referrred, f = 5MHz	−60				dBc	typ	C
DC Performance(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	90	**82**	81	80	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.15	**±0.65**	±0.73	±0.76	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V	±0.5	±1.6	±1.6	±1.6	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	−10	**−20**	−20.8	−21.2	µA	max	A
Input Bias Current Drift	V_{CM} = 0V	±1	±20	±20	±35	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±0.4**	±0.5	±0.6	µA	max	A
Input Offset Current Drift	V_{CM} = 0V	±0.7	±3.0	±3.0	±3.5	nA/°C	max	B
Input								
Common-Mode Input Range (CMIR)(5)		±3.2	**±3.0**	±2.9	±2.8	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V, Input Referred	110	**95**	93	90	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0V	6.6 ‖2.0				kΩ ‖pF	typ	C
Common-Mode	V_{CM} = 0V	4.7 ‖1.8				MΩ ‖pF	typ	C
Output								
Output Voltage Swing	≥ 400Ω Load	±3.4	**±3.3**	±3.2	±3.1	V	min	A
	100Ω Load	±3.3	**±3.2**	±3.0	±2.9	V	min	A
Current Output, Sourcing	V_O = 0V	80	**65**	61	60	mA	min	A
Current Output, Sinking	V_O = 0V	−80	**−65**	−61	−60	mA	min	A
Closed-Loop Output Impedance	G = +10, f = 100kHz	0.008				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are 100% tested at **+25°C.**

R_F = 453Ω, R_L = 100Ω, and G = +10, unless otherwise noted. See Figure 1 for AC performance.

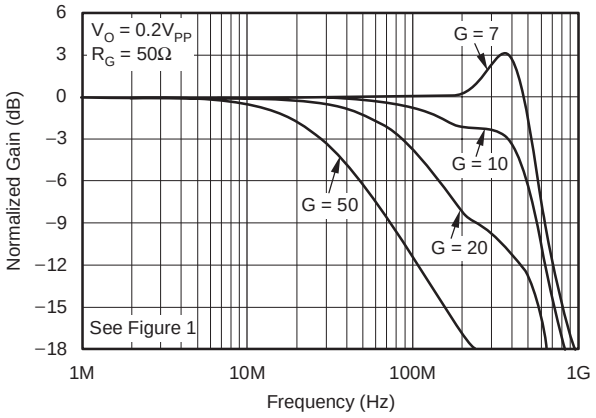
PARAMETER	TEST CONDITIONS	OPA2846ID						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
Power Supply								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Maximum Quiescent Current	V_S = ±5V, Both Channels	25.2	**25.9**	26.3	26.7	mA	max	A
Minimum Quiescent Current	V_S = ±5V, Both Channels	25.2	**24.5**	23.9	23.3	mA	min	A
Power-Supply Rejection Ratio (−PSRR)	$-V_S$ = −4.5 to 5.5 (Input Referred)	95	**90**	88	85	dB	min	A
Thermal Characteristics								
Specified Operating Range: D Package		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

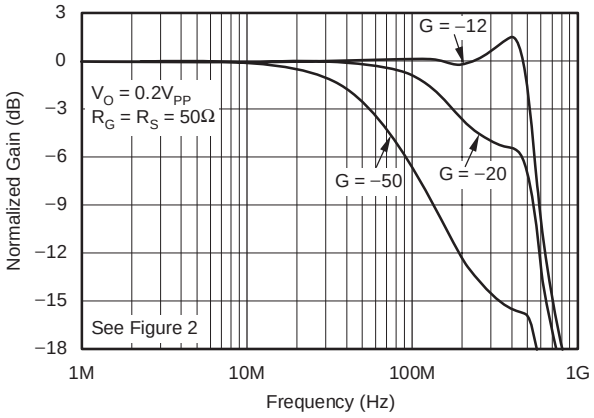
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$T_A = 25°C$, G = +10, $R_F = 453\Omega$, $R_G = 50\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

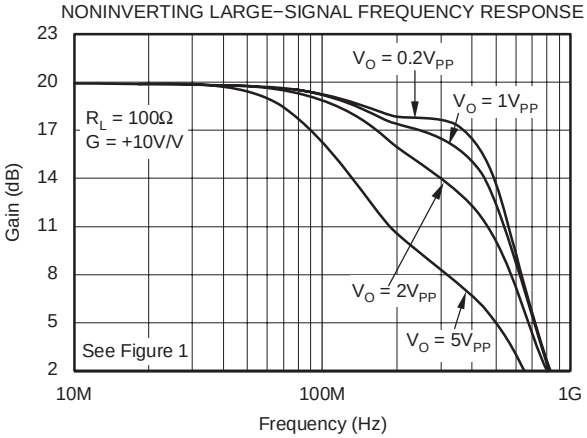
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



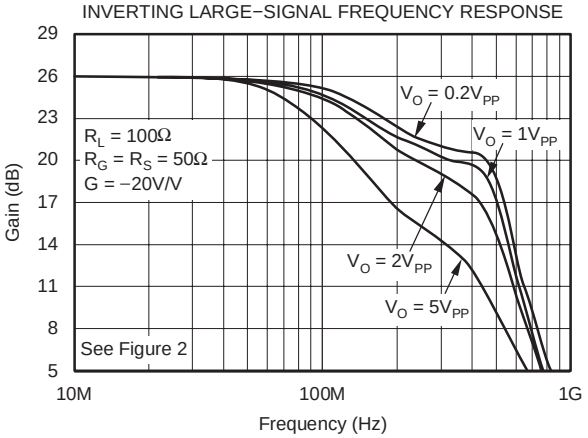
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



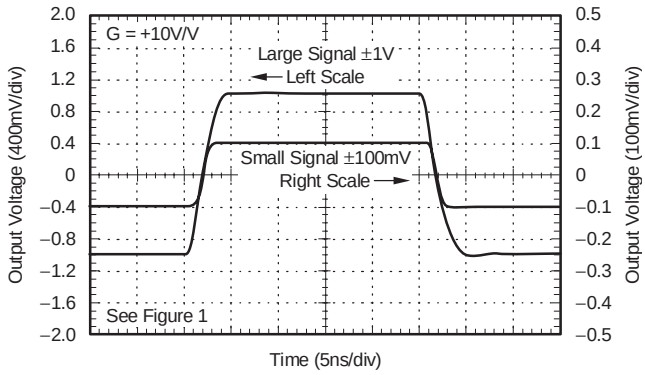
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



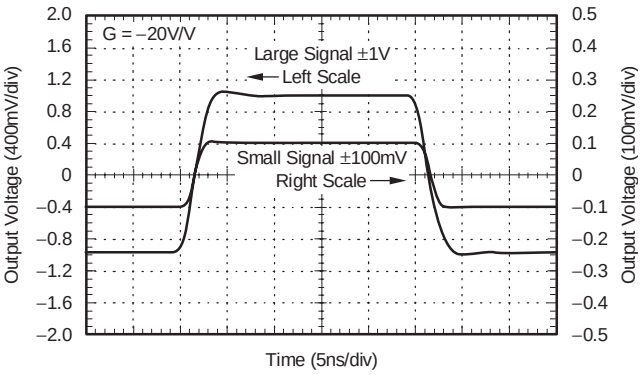
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



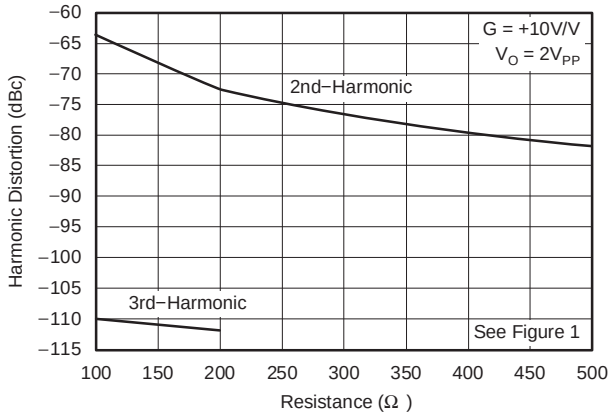
INVERTING PULSE RESPONSE



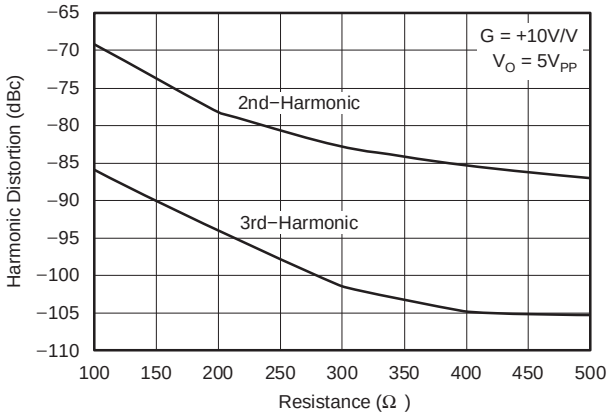
TYPICAL CHARACTERISTICS: $V_S = \pm5V$ (continued)

$T_A = 25°C$, G = +10, $R_F = 453\Omega$, $R_G = 50\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

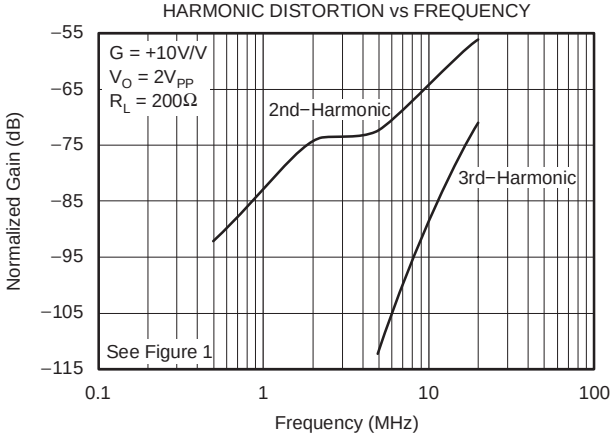
5MHz HARMONIC DISTORTION vs LOAD RESISTANCE



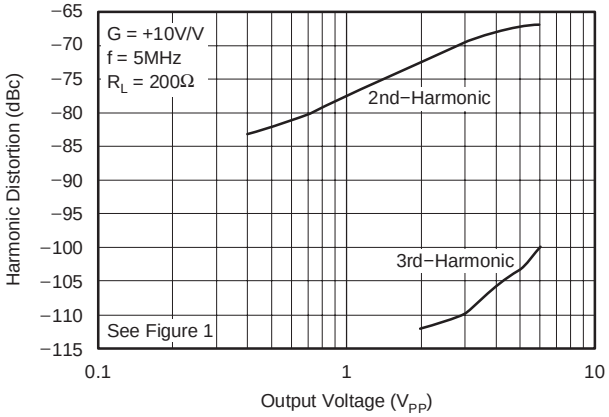
1MHz HARMONIC DISTORTION vs LOAD RESISTANCE



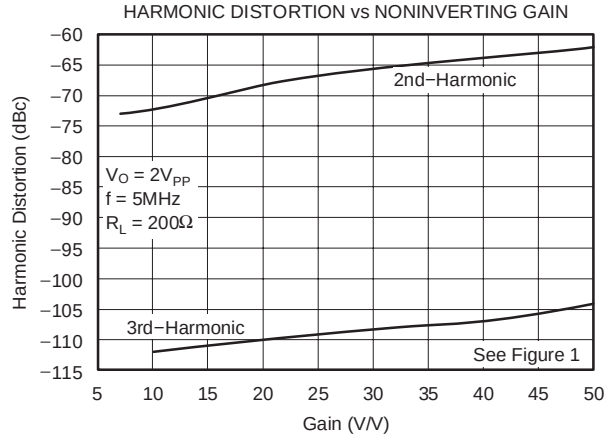
HARMONIC DISTORTION vs FREQUENCY



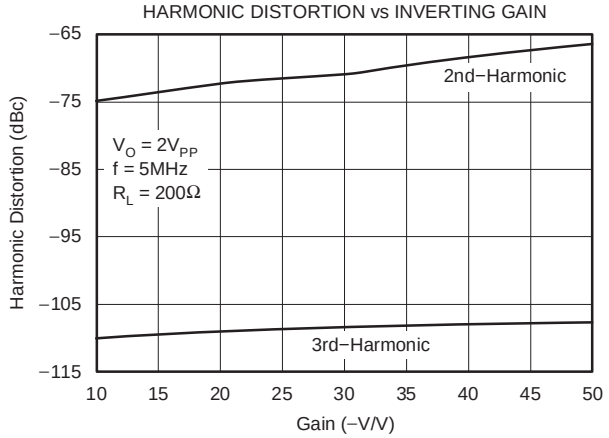
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



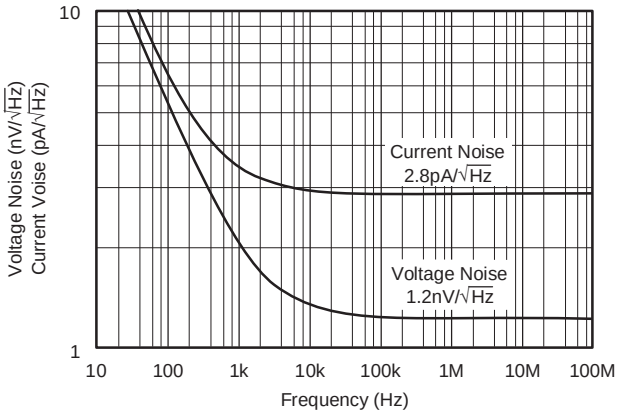
HARMONIC DISTORTION vs INVERTING GAIN



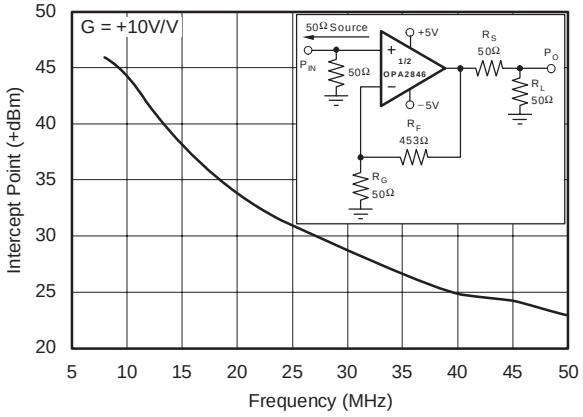
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$T_A = 25°C$, G = +10, $R_F = 453\Omega$, $R_G = 50\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

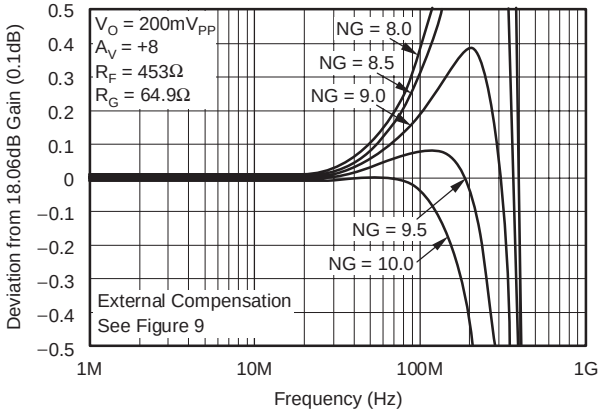
INPUT VOLTAGE AND CURRENT NOISE



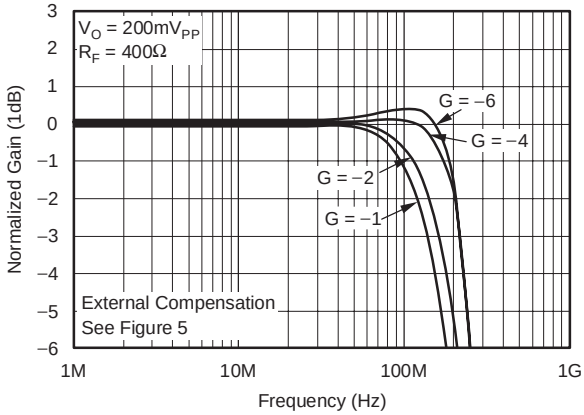
2−TONE, 3RD−ORDER INTERMODULATION INTERCEPT



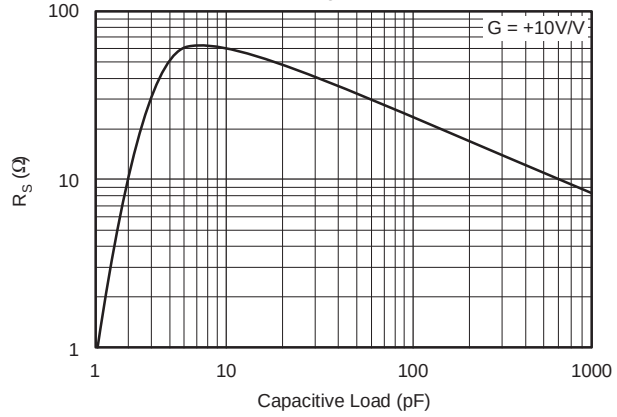
NONINVERTING GAIN FLATNESS TUNE



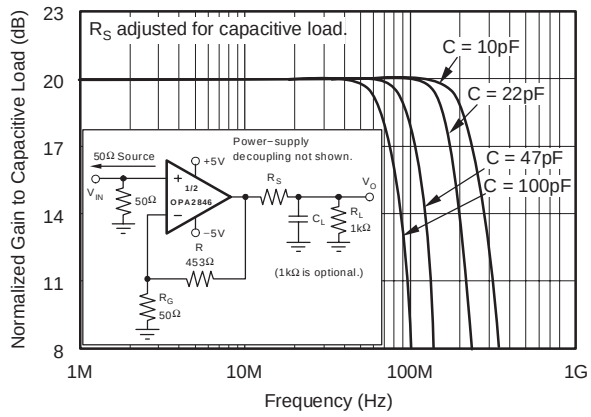
LOW GAIN INVERTING BANDWIDTH



RECOMMENDED R_S vs CAPACITIVE LOAD



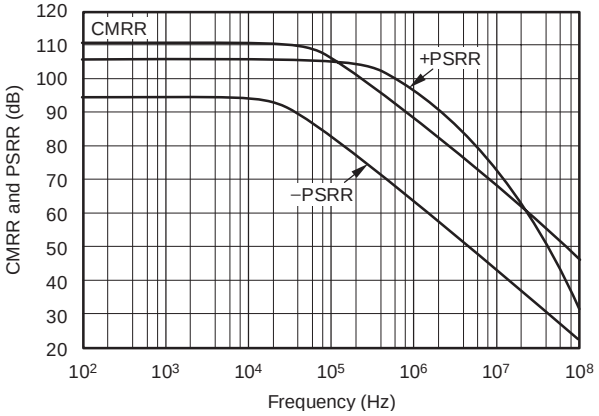
FREQUENCY RESPONSE vs CAPACITIVE LOAD



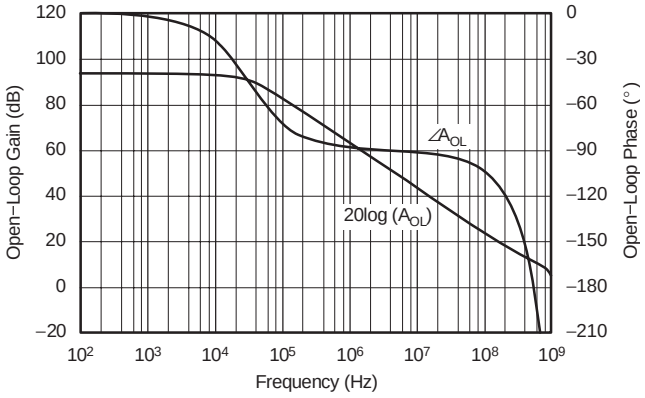
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$T_A = 25°C$, G = +10, $R_F = 453\Omega$, $R_G = 50\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

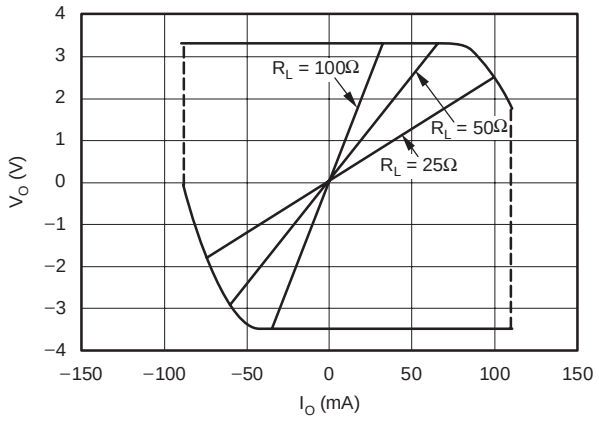
COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs FREQUENCY



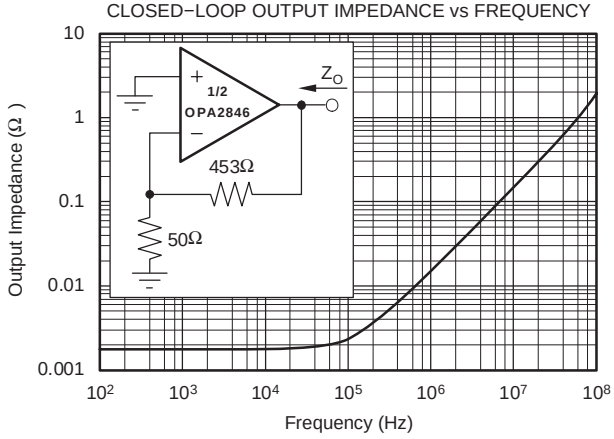
OPEN−LOOP GAIN AND PHASE



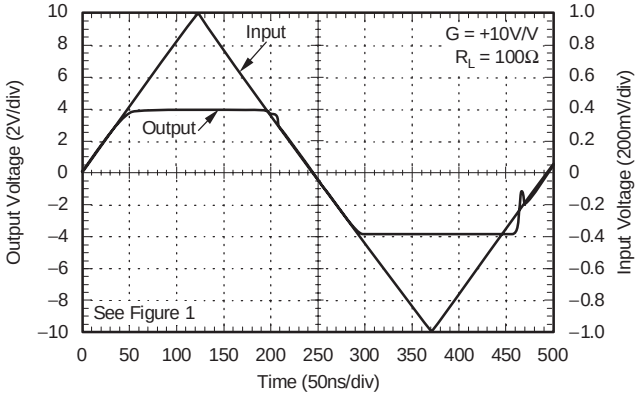
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



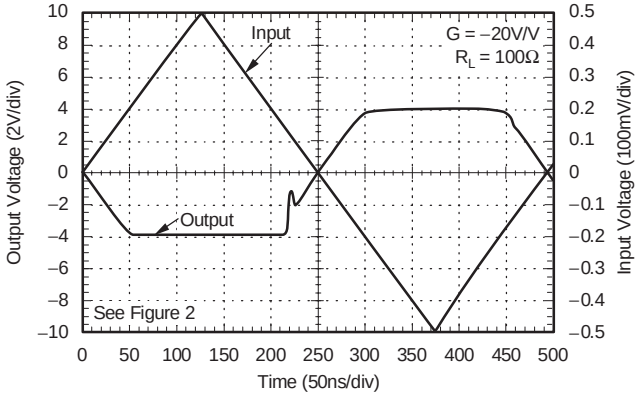
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



NONINVERTING OVERDRIVE RECOVERY



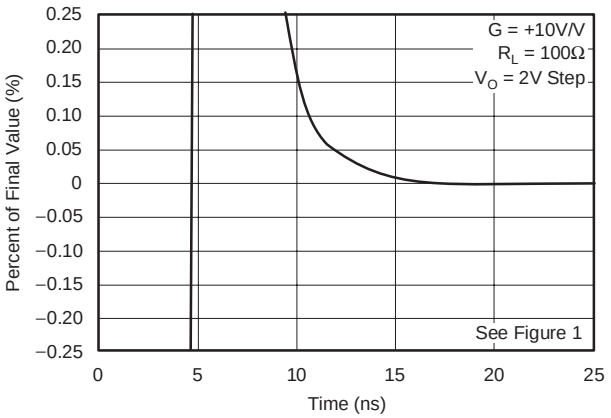
INVERTING OVERDRIVE RECOVERY



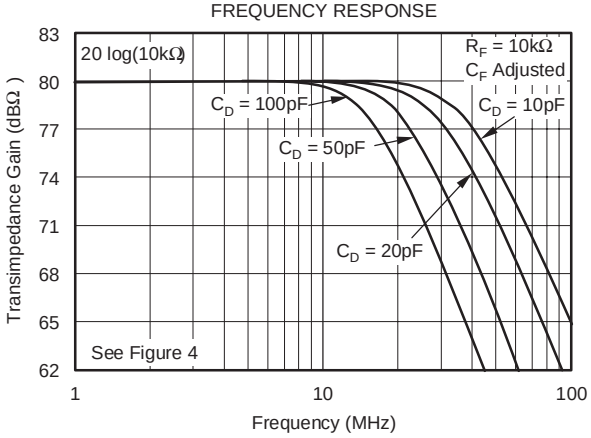
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$T_A = 25°C$, G = +10, $R_F = 453\Omega$, $R_G = 50\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

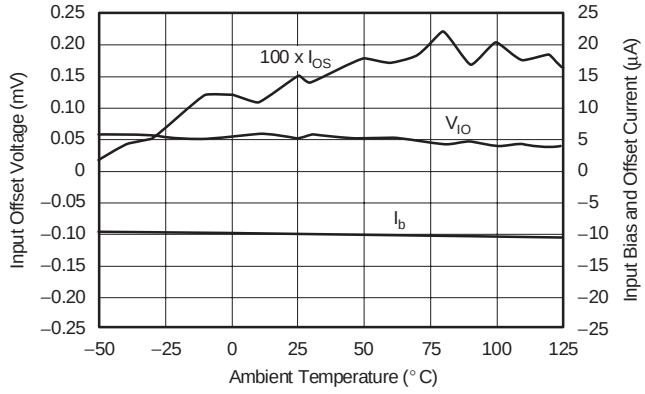
SETTLING TIME



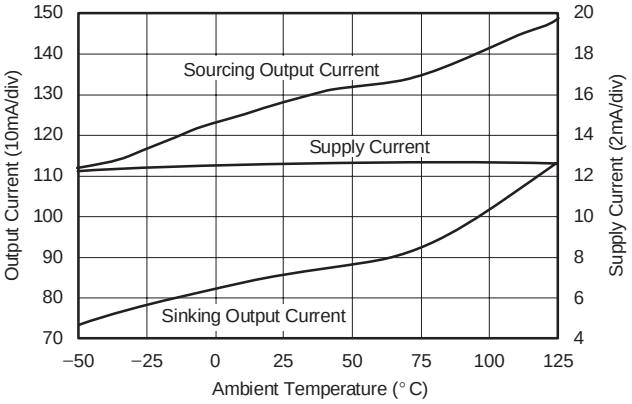
PHOTODIODE TRANSIMPEDANCE FREQUENCY RESPONSE



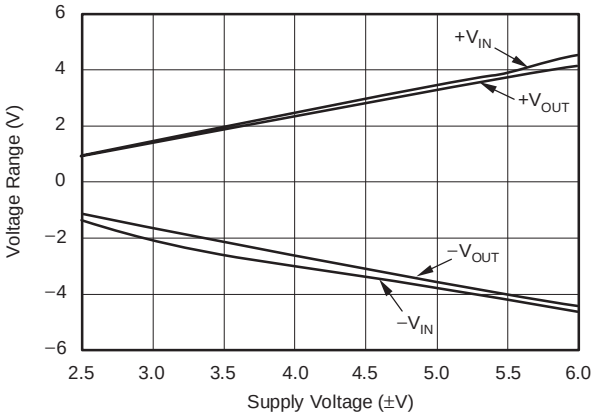
TYPICAL DC DRIFT OVER TEMPERATURE



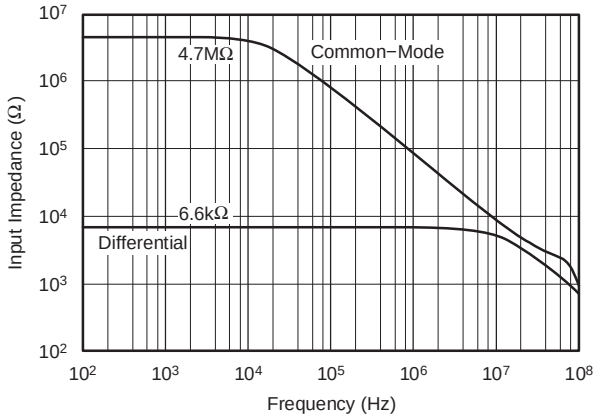
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON−MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



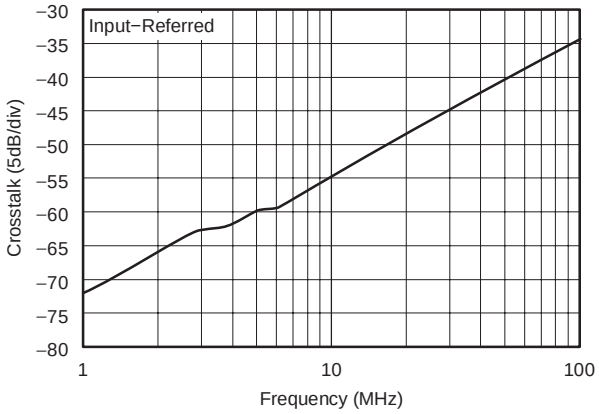
COMMON−MODE AND DIFFERENTIAL INPUT IMPEDANCE



TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

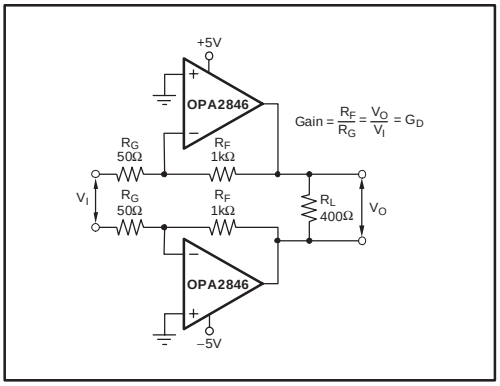
CHANNEL−TO−CHANNEL CROSSTALK



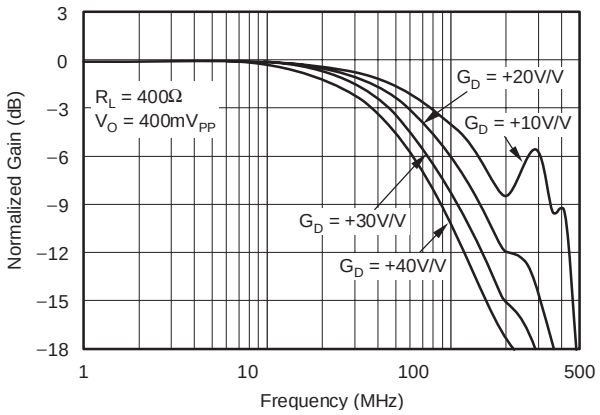
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$, DIFFERENTIAL CONFIGURATION

$T_A = 25°C$, G = +10, $R_F = 1k\Omega$, $R_G = 50\Omega$, and $R_L = 400\Omega$, unless otherwise noted.

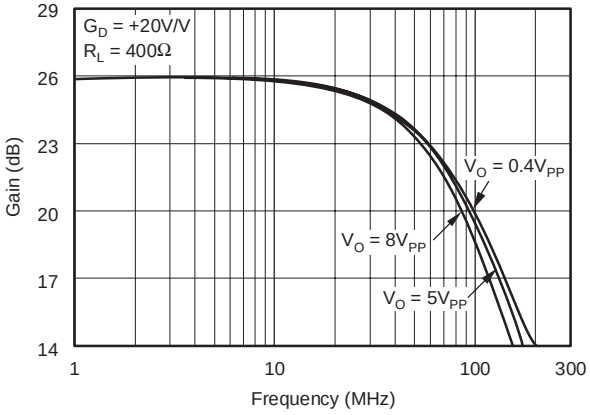
DIFFERENTIAL PERFORMANCE TEST CIRCUIT



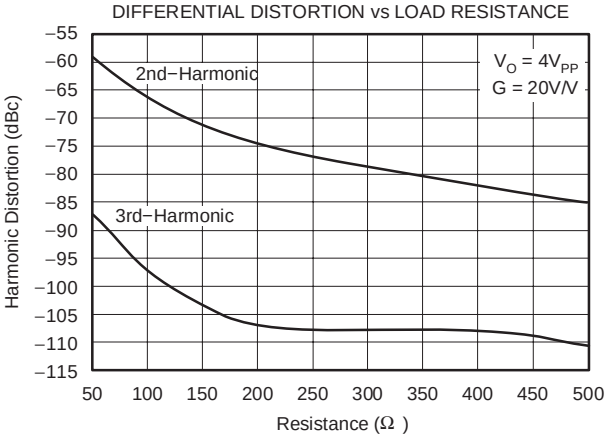
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



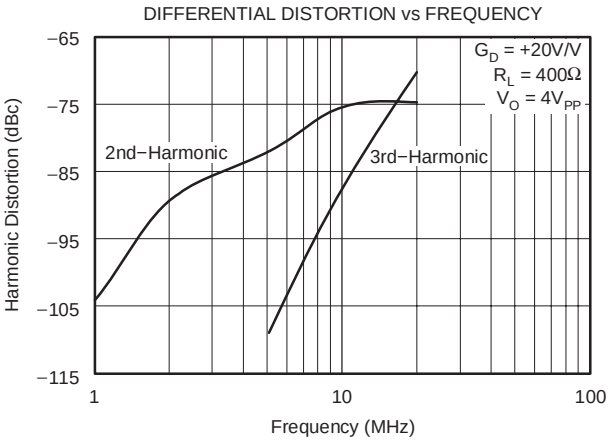
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



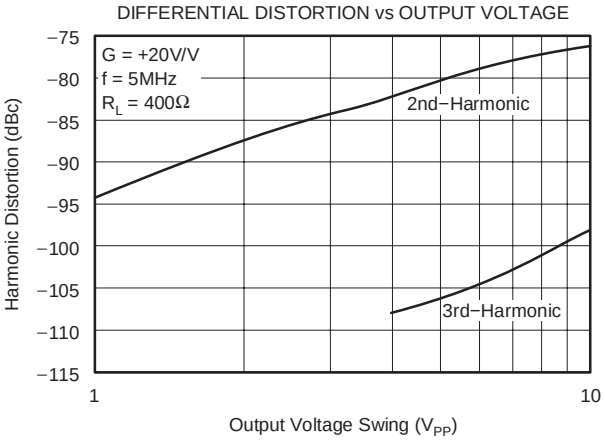
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND, NONINVERTING OPERATION

The OPA2846 provides a unique combination of features—low input voltage noise along with a very low distortion output stage—to give one of the highest dynamic range dual op amps available. Its very high Gain Bandwidth Product (GBP) can be used either to deliver high signal bandwidths at high gains, or to deliver very low distortion signals at moderate frequencies and lower gains. To achieve the full performance of the OPA2846, careful attention to printed circuit board (PCB) layout and component selection is required, as discussed in the remaining sections of this data sheet.

Figure 1 shows the noninverting gain of +10 circuit used as the basis of the Electrical Characteristics and most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1), while output power (dBm) specifications are at the matched 50Ω load. The total 100Ω load at the output, combined with the 503Ω total feedback network load, presents the OPA2846 with an effective output load of 83Ω for the circuit of Figure 1.

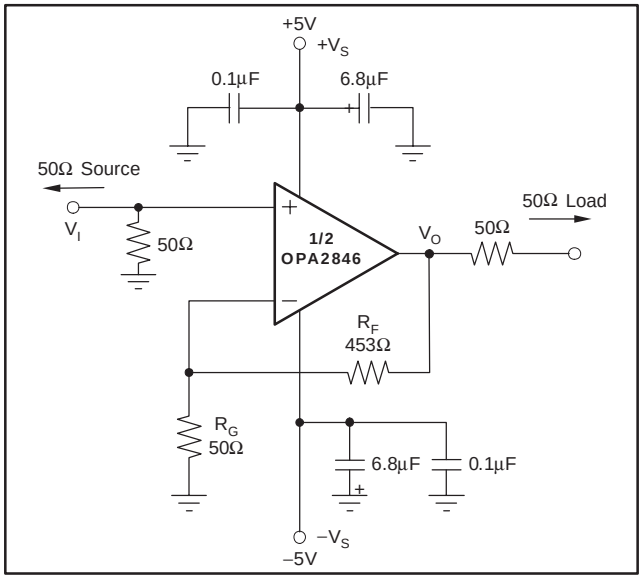


Figure 1. Noninverting, G = +10 Specification and Test Circuit

Voltage-feedback op amps, unlike current-feedback designs, can use a wide range of resistor values to set their gains. The circuit of Figure 1, and the specifications at other gains, uses the constraint that R_G should always be set to 50Ω and R_F adjusted to get the desired gain. Observing this guideline will ensure that the thermal noise contribution of the feedback network is insignificant compared to the 1.2nV/$\sqrt{Hz}$ input voltage noise for the op amp itself.

WIDEBAND, INVERTING GAIN OPERATION

Operating the OPA2846 as an inverting amplifier has several benefits and is particularly appropriate when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as the basis of the inverting mode Typical Characteristics.

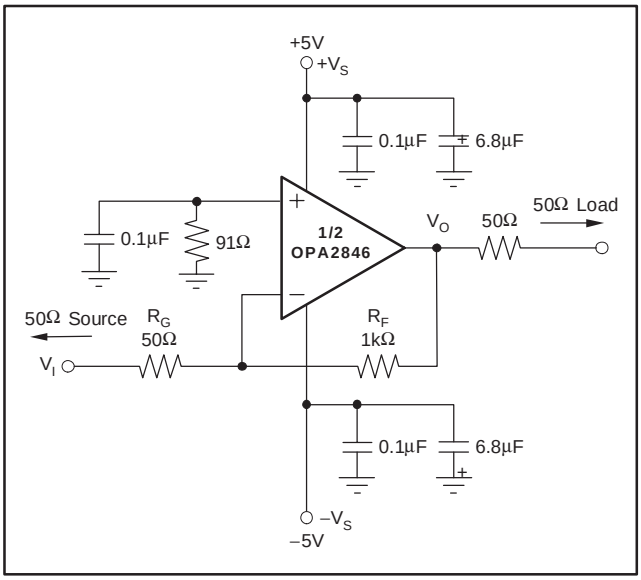


Figure 2. Inverting, G = −20 Characterization Circuit

Driving this circuit from a 50Ω source, and constraining the gain resistor (R_G) to equal 50Ω, will give both a signal bandwidth and noise advantage. R_G acts as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain (V_O/V_I) for the circuit of Figure 2 is double that for Figure 1, the noise gains are in fact equal when the 50Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP of the amplifier. This can be seen in comparing the G = +10 and G = −20 small-signal frequency response curves. Both show approximately 250MHz bandwidth, but the inverting configuration of Figure 2 gives 6dB higher signal gain. If the signal source is actually the low impedance output of another amplifier, R_G should be increased to the minimum load resistance value allowed for that amplifier and R_F should be adjusted to achieve the desired gain. For stable operation of the OPA2846, it is critical that this driving amplifier show a very low output impedance at frequencies beyond the expected closed-loop bandwidth for the OPA2846.

LOW-NOISE VDSL RECEIVER

Most xDSL transceiver channels are differential for both the driver and the receiver. The low-noise, high-gain bandwidth, and low distortion for the dual OPA2846 make it an ideal receiver channel element for the demanding requirements emerging in VDSL. One possible implementation is shown in Figure 3. This circuit presumes full duplex communication using frequency division multiplexing, with send-and-receive isolation improved through the use of a diplexer line interface. The differential receive signal is brought into the inverting channel gain resistors to get both noise and distortion improvement for a given desired gain setting. To get impedance matching, set $2R_G$ equal to the required load looking out of the diplexer. The signal gain is then set by adjusting feedback resistors, R_F. Using the OPA2846 in the inverting mode will give you a reduced noise gain as described in the *Wideband, Inverting Gain Operation* section of this data sheet. This will improve both the SNR and distortion performance. If the noise gain for a particular application drops below the minimum recommended stable gain (+7), consider using the Low-Gain Compensation technique described later in this data sheet.

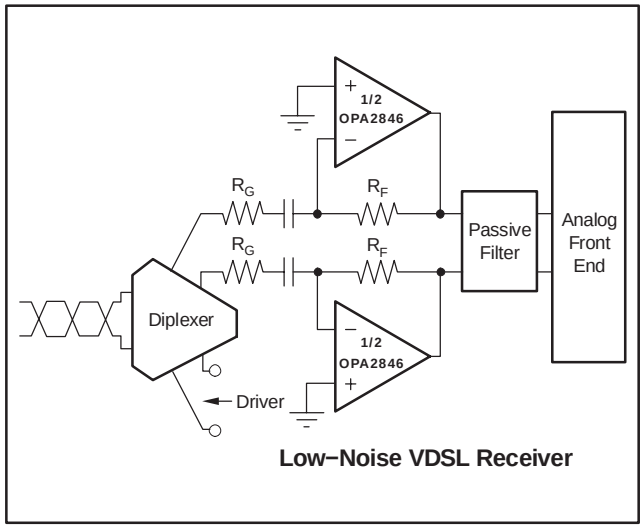


Figure 3. Low-Noise VDSL Receiver

SINGLE-STAGE TRANSIMPEDANCE DESIGN

When setting up either one or both stages as a broadband photodiode amplifier, the key elements in the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain R_F, and the GBP of the OPA2846 (1650MHz). Figure 4 shows a design using a 10pF source capacitance diode and a 10kΩ transimpedance gain. With these three variables set (and including the parasitic input capacitance for the OPA2846 added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response.

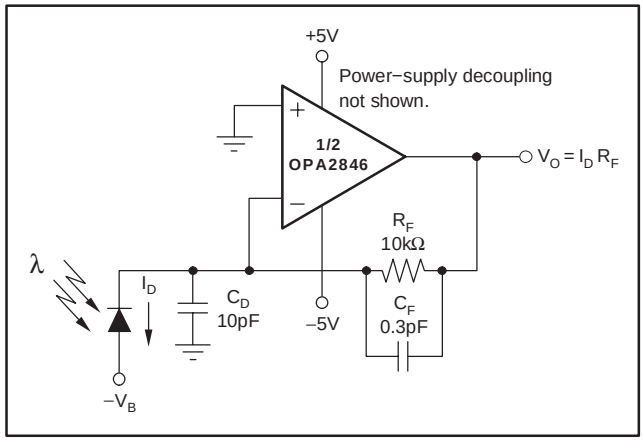


Figure 4. Wideband, Low-Noise, Transimpedance Amplifier

To achieve a maximally-flat, 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$1/(2\pi R_F C_F) = \sqrt{(GBP/(4\pi R_F C_D))} \quad (1)$$

Adding the common-mode and differential mode input capacitance (1.8 + 2.0)pF to the 10pF diode source capacitance of Figure 4, and targeting a 10kΩ transimpedance gain using the 1650MHz GBP for the OPA2846, will require a feedback pole set to 31MHz. This will require a total feedback capacitance of 0.5pF. Typical surface-mount resistors have a parasitic capacitance of 0.2pF, leaving the required 0.3pF value shown in Figure 4 to get the required feedback pole.

This will give a −3dB bandwidth approximately equal to:

$$f_{-3dB} = \sqrt{(GBP/2\pi R_F C_D)Hz} \quad (2)$$

The example of Figure 4 will give approximately 44MHz flat bandwidth using the 0.3pF feedback compensation.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent input noise current can be derived as:

$$I_{EQ} = \sqrt{I_N^2 + \frac{4kT}{R_F} + \left(\frac{E_N}{R_F}\right)^2 + \frac{(E_N 2\pi C_D F)^2}{3}} \quad (3)$$

Where:

I_{EQ} = Equivalent input noise current if the output noise is bandlimited to $F < 1/(2\pi R_F C_F)$

I_N = Input current noise for the op amp inverting input

E_N = Input voltage noise for the op amp

C_D = Diode capacitance

F = Bandlimiting frequency in Hz (usually a post filter prior to further signal processing)

Evaluating this expression up to the feedback pole frequency at 31MHz for the circuit of Figure 4 gives an equivalent input noise current of 3.1pA/$\sqrt{Hz}$. This is only slightly higher than the current noise of the op amp itself.

TWO-STAGE TRANSIMPEDANCE DESIGN

The dual OPA2846 may be used as either a dual transimpedance channel from two photodetectors, or as a very high gain stage by using one amplifier as the transimpedance stage with the second used as a post gain amplifier. See Figure 5 for an example of using one channel as a transimpedance front end from a large area detector, with the second amplifier used as a voltage gain stage to get a 100kΩ total gain (Z_T) from a large 50pF detector (C_D in Figure 5).

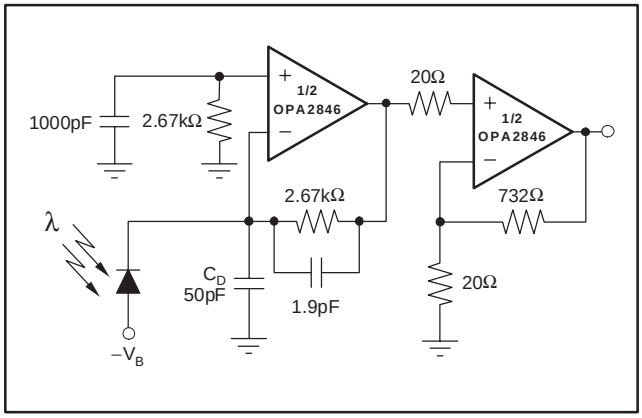


Figure 5. High-Gain, Wideband Transimpedance Amplifier

One key question in this design is how best to split up the first and second stage gains. If bandwidth optimization from a given photodetector capacitance (C_D in Figure 5) is the primary goal, Equation 4 gives a solution for R_F in the input stage that will provide an equal bandwidth in the first and second stages, giving the maximum overall channel bandwidth.

$$R_F = \left(\frac{Z_T^2}{2\pi C_D\, GBP}\right) \quad (4)$$

Where:

Z_T = Desired total transimpedance gain

C_D = Diode capacitance at reverse bias

GBP = Amplifier Gain Bandwidth Product (MHz)

This equation is used to calculate the required input stage feedback resistor in Figure 5. The remaining total signal gain is provided by the second stage; in the example of Figure 5, setting G = 37.5 gives the same bandwidth (approximately 44MHz) as the bandwidth achieved by the input stage. To set this first stage bandwidth to its maximally flat values, use Equation 5 to set the feedback capacitor value:

$$C_F = \sqrt{\left(\frac{C_D}{\pi R_F\, GBP}\right)} \quad (5)$$

$$f_{-3dB} = \frac{1}{\sqrt{2}} \times \frac{(GBP)^{2/3}}{(2\pi C_D)^{1/3}\,(Z_T)^{1/3}} \quad (6)$$

The approximate achievable bandwidth in the two stages is given by Equation 6, which gives approximately 30MHz for Figure 5.

LOW-GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA2846 while giving increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability while giving an easily-controlled, 2nd-order, low-pass frequency response. Considering only the noise gain (noninverting signal gain, which is also called the Noise Gain or NG) for the circuit of Figure 6, the low-frequency noise gain, (NG_1) will be set by the resistor ratios while the high-frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain (determined by $NG_2 = 1 + C_S/C_F$) is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole (set by $1/R_F C_F$) is placed correctly, a very well-controlled, 2nd-order, low-pass frequency response will result.

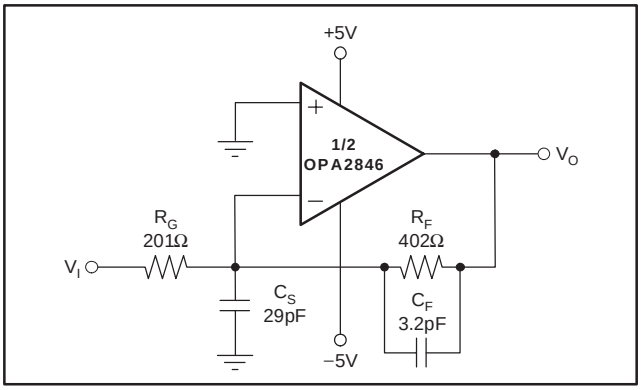


Figure 6. Broadband Low-Gain Inverting External Compensation

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain NG_2, which should be greater than the minimum stable gain for the OPA2846. Here, a target NG_2 of 10 will be used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain NG_1. To simplify this discussion, we will target a maximally-flat, 2nd-order, low-pass Butterworth frequency response (Q = 0.707). The signal gain of −2 shown in Figure 6 will set the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ ($NG_1 = 3$ in this example). Then, using only these two gains and the GBP for the OPA2846 (1650MHz), the key frequency in the compensation can be determined as:

$$Z_0 = \frac{GBP}{NG_1^2}\left[\left(1 - \frac{NG_1}{NG_2}\right) - \sqrt{1 - 2\frac{NG_1}{NG_2}}\right] \quad (7)$$

Physically, this Z_0 (12.4MHz for the values shown above) is set by $1/[2\pi \times R_F(C_F + C_S)]$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0dB gain. The actual zero in the noise gain occurs at $NG_1 \times Z_0$, and the pole in the noise gain occurs at $NG_2 \times Z_0$. Since GBP is expressed in Hz, multiply Z_0 by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi \times R_F Z_0 NG_2} \quad (= 3.2pF) \quad (8)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S by:

$$C_S = (NG_2 - 1)C_F \quad (= 28.8pF) \quad (9)$$

The resulting closed-loop bandwidth will be approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_0\, GBP} \quad (= 143MHz) \quad (10)$$

For the values of Figure 6, the f_{-3dB} will be approximately 130MHz. This is less than that predicted by simply dividing the GBP by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \times Z_0$. The capacitor values of Figure 6 are calculated for $NG_1 = 3$ and $NG_2 = 10$ with no adjustment for parasitics.

Figure 7 shows the measured frequency response for the circuit of Figure 6. This shows the expected gain of −2 (6dB) with exceptional flatness through 70MHz and a −3dB bandwidth of 170MHz. Measured distortion into a 100Ω load shows > 5dB improvement through 20MHz over the performance shown in the Typical Characteristics. Into a 500Ω load, the 5MHz, $2V_{PP}$, 2nd-harmonic improves from −85dBc to −92dBc.

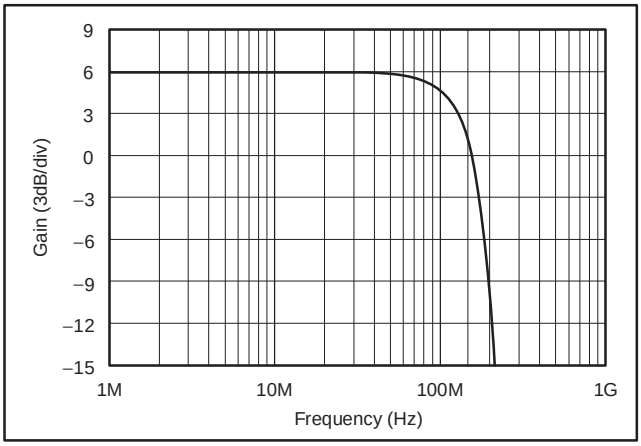


Figure 7. Low Gain Inverting Frequency Response

DC-COUPLED, SINGLE-TO-DIFFERENTIAL ADC DRIVER

Many very high performance CMOS ADCs are intended to operate with a differential input signal. Translating a single-ended source to this differential input while controlling the common-mode operating voltage can present a considerable challenge where high SFDR is required. See Figure 8 for one way to do this, where very low harmonic distortion is required, and good common-mode control and DC precision is desired.

This particular example is set for a signal gain of 16 from the single-ended input to the differential output voltage. Since the common-mode control signal (from the output of the OPA820) is fed into the midpoint of the two gain resistors (93.8Ω), this DC control path requires a very low source impedance through high frequencies to maintain the desired signal path gain. A wideband, unity-gain stable, voltage-feedback op amp like the OPA820 makes an ideal choice to provide this low output impedance DC control signal. This op amp also compares the output common-mode voltage to the desired V_{CM}, and servos the OPA2846 common-mode output voltage to that value, using an integrator loop. This holds the output common-mode voltage precisely at V_{CM} while giving the low output impedance required of the circuit.

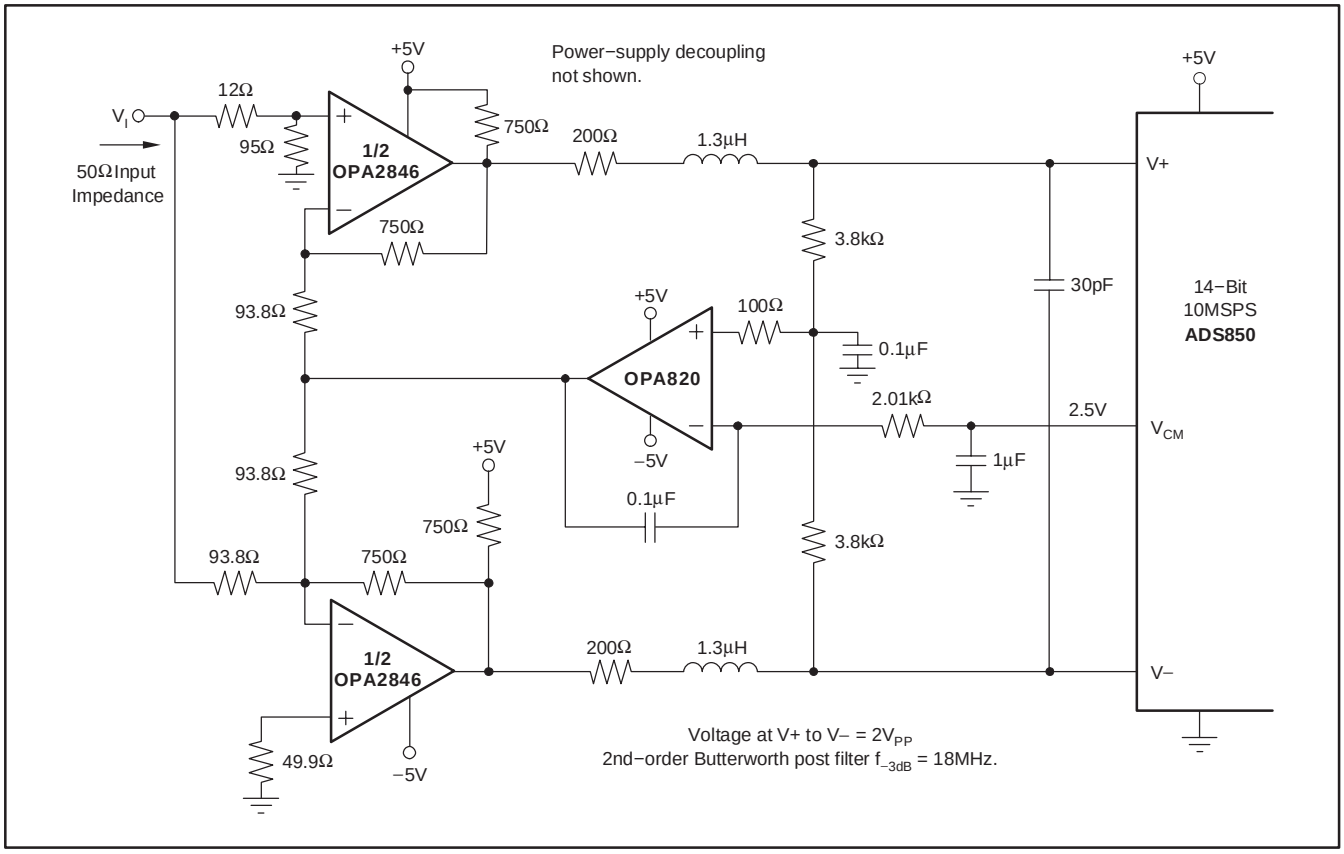


Figure 8. DC-Coupled, Single-to-Differential High SFDR ADC Driver

Operating at +2.5V output common-mode requires a DC level shifting current through the feedback resistors. Since this current is to the supply midpoint, pull-up resistors equal to the feedback resistors are connected to the positive supply to keep the output stage signal currents equal and bipolar. This significantly improves 2nd-harmonic distortion.

One side of the OPA2846 is operating at a gain of +9 with some attenuation of the input signal to have an equivalent +8 gain. The other side of the OPA2846 is operating at a gain of −8.

To deliver a $2V_{PP}$ differential input signal on a 2.5V common-mode voltage, each output must swing between 2.0V and 3.0V. Tested harmonic distortion performance for this condition from 1MHz to 10MHz is shown in Figure 9.

In this case, the 2nd-harmonic distortion is still dominant due to slight signal path imbalances. The distortion levels, however, are very low. Thus, narrowband applications which are impacted by only 3rd-order terms will see very low single- and two-tone distortion levels.

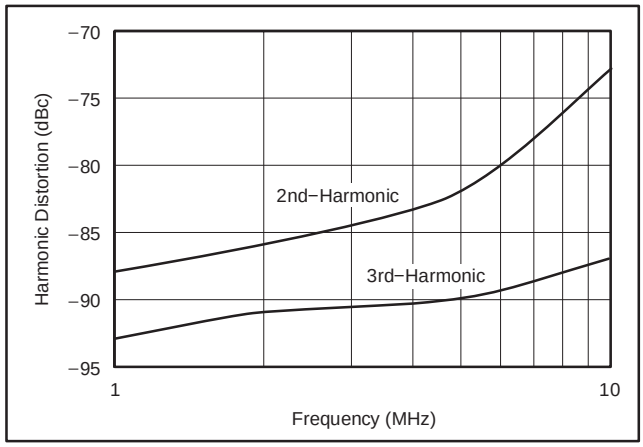


Figure 9. Harmonic Distortion vs Frequency for the Circuit of Figure 8

For more information on the 2nd-order post filter, refer to *RLC Filter Design for ADC Interface Applications* (SBAA108), available for download at www.ti.com.

AC-COUPLED, SINGLE-TO-DIFFERENTIAL ADC DRIVER

Where the signal path may be AC-coupled, a very balanced, high SFDR dual op amp interface circuit can easily be provided by the OPA2846. Figure 10 shows a specific example of this application, where the input single-to-differential conversion is provided by an input transformer. Once the signal source is purely differential, the circuit of Figure 10 provides low harmonic distortion with a common-mode control path that does not interact with the signal path gain. If the source is already differential, such as at the output of a balanced mixer, the input transformer could be replaced by blocking capacitors.

In the example of Figure 10, the secondary of the transformer is connected into the two inverting path gain resistors (100Ω). These resistors provide both an input impedance match (assuming a 50Ω source on the primary of this 1:2 step-up transformer) and set the signal gain for each amplifier along with the 500Ω feedback resistors. Although relatively high signal gain is provided by this circuit (10 in this case), each amplifier is operating at a relatively low noise gain (3.5V/V). This low-noise gain at low frequencies gives high loop gain for distortion suppression in the baseband. External compensation capacitors (18pF and 2.1pF) are included to hold the frequency response flat, as described in the *Low-Gain Compensation For Improved SFDR* section of this data sheet. The common-mode operating voltage is fed into each amplifier's noninverting input. Since these are equal, and will appear at each inverting input as well, no DC current is produced through the transformer secondary due to this common-mode operating voltage. Since no current flows due to V_{CM}, the output will operate at V_{CM} as well. This is one of the few common-mode operating point control techniques that requires no current to flow. This makes the common-mode control aspect of this circuit essentially non-interactive with the signal path. To provide a $2V_{PP}$ differential signal operating at a 2.5V output common-mode requires a 2.0V to 3.0V output swing on each output. Tested performance over frequency for the circuit of Figure 10 is shown in Figure 11.

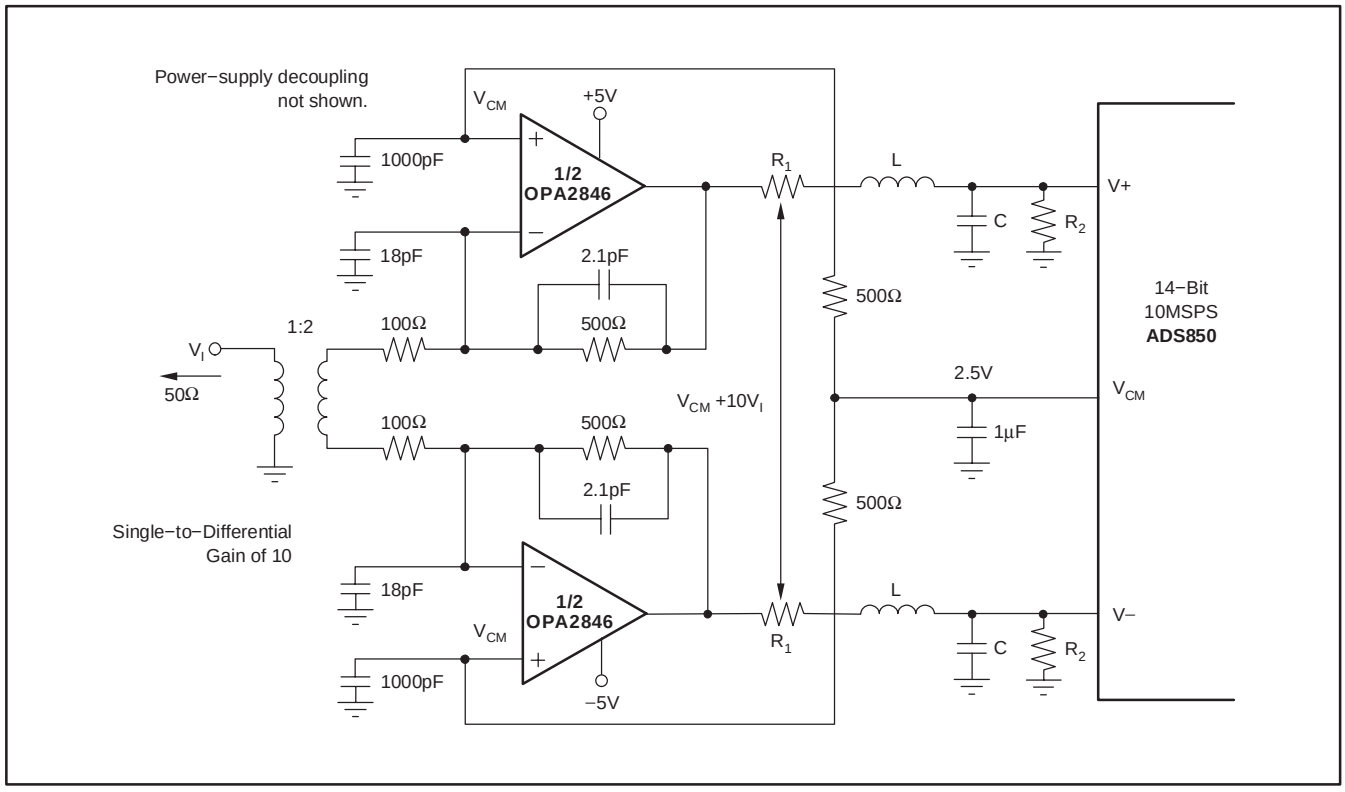


Figure 10. AC-Coupled, Single-to-Differential High SFDR ADC Driver

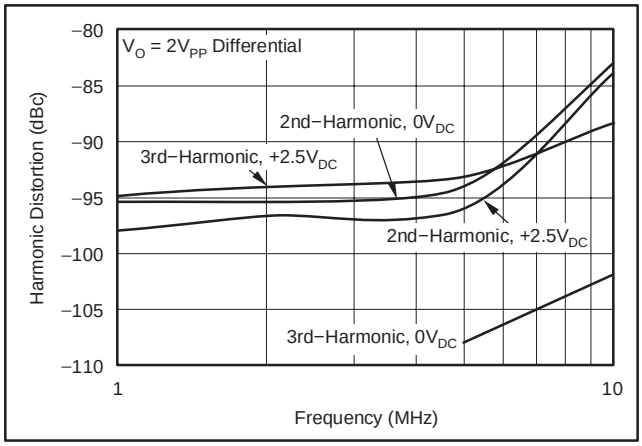


Figure 11. Harmonic Distortion for Figure 10

Figure 11 shows 2nd- and 3rd-harmonic distortion for a 2V_{PP} differential output swing at both 0V output common-mode voltage and +2.5V common-mode voltage. Since there is no DC current required from the output to level shift to +2.5V in this circuit, no pull-up resistors to the power supply were used as in the circuit of Figure 8. The 2nd harmonic remains the dominant distortion mechanism, but shows little sensitivity to the common-mode operating voltage (improved 2nd-harmonic distortion results were achieved with this circuit using two individual OPA846s with an extremely symmetrical layout). The 3rd harmonic is essentially unmeasureable for the ground-centered output swing, but increases as the output is shifted to a +2.5V DC output. Narrowband systems, where a bandpass filter less than an octave wide can be inserted between the amplifier and the converter, will only be concerned about 2-tone, 3rd-order intermodulation distortion. Since this bandpass filter is also AC-coupled, the outputs of Figure 10 may be operated ground-centered, giving the extremely low 3rd-order distortions of Figure 11.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA2846. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this board is shown in Table 1.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2846ID	SO-8 Surface-Mount	DEM-OPA-SO-2A	SBOU003

Table 1. Evaluation Module Ordering Information

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA2846 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2846 is available through the Texas Instruments web page (http://www.ti.com).

These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion characteristics.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA2846 provides a very low input noise voltage while requiring a low 12.6mA/channel quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

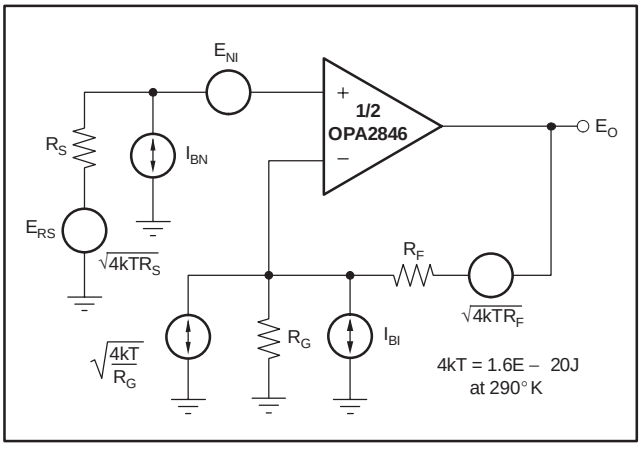


Figure 12. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then takes the square root to get back to a spot noise voltage. Equation 11 shows the general form for this output noise voltage using the terms shown in Figure 12.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (11)$$

Dividing this expression by the noise gain ($NG = 1 + R_F/R_G$) will give the equivalent input-referred spot noise voltage at the noninverting input as shown in Equation 12.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (12)$$

Inserting high resistor values into Equation 12 can quickly dominate the total equivalent input-referred noise. A 105Ω source impedance on the noninverting input will add a thermal voltage noise term equal to that of the amplifier itself. As a simplifying constraint, set $R_G = R_S$ in Equation 12 and assume an $R_S/2$ source impedance at the noninverting input (where R_S is the signal source impedance with another matching R_S to ground on the noninverting input). This results in Equation 13, where NG > 10 has been assumed to further simplify the expression.

$$E_N = \sqrt{(E_{NI})^2 + \frac{5}{4}\left(I_BR_S\right)^2 + 4kT\left(\frac{3R_S}{2}\right)} \quad (13)$$

Evaluating this expression for $R_S = 50\Omega$ will give a total equivalent input noise of $1.64nV/\sqrt{Hz}$. Note that the NG has dropped out of this expression. This is valid only for NG > 10.

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the noninverting signal gain will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (with an increased feedback factor), most high-speed amplifiers will exhibit a more complex response with lower phase margin. The OPA2846 is compensated to give a maximally-flat, 2nd-order, Butterworth, closed-loop response at a noninverting gain of +10 (see Figure 1). This results in a typical gain of +10 bandwidth of 300MHz, far exceeding that predicted by dividing the 1650MHz GBP by 10. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +40, the OPA2846 will show the 41MHz bandwidth predicted using the simple formula and the typical GBP of 1650MHz.

Inverting operation offers some interesting opportunities to increase the available GBP. When the source impedance is matched by the gain resistor (see Figure 2), the signal gain is $(1 + R_F/R_G)$ while the noise gain for bandwidth purposes is $(1 + R_F/2R_G)$. This cuts the noise gain almost in half, increasing the minimum stable gain for inverting operation under these condition to −12 and the equivalent GBP to 3.2GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2846 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended *R_S vs Capacitive Load* and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2846. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2846 output pin (see the *Board Layout* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA2846 operating in a gain of +10, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads. As the signal gain is increased, the unloaded phase margin will also increase. Driving capacitive loads at higher gains will require lower R_S values than those shown for a gain of +10.

DISTORTION PERFORMANCE

The OPA2846 is capable of delivering an exceptionally low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 110dB dynamic range.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration, this is sum of ($R_F + R_G$), while in the inverting configuration, it is just R_F (see Figure 1 and Figure 2). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the 2nd-harmonic to 12dB and the 3rd-harmonic to 18dB. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again, a 6dB increase in gain will increase the 2nd and 3rd harmonic by approximately 6dB each, even with constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases, due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 100kHz. Starting from the −82dBc 2nd-harmonic for a 5MHz, $2V_{PP}$ fundamental into a 200Ω load at G = +10 (from the Typical Characteristics), the 2nd-harmonic distortion for frequencies lower than 100kHz will approximately be:

$$-82dBc - 20 \log(5MHz/100kHz) = -116dBc$$

The OPA2846 has extremely low 3rd-order harmonic distortion. This also gives a high 2-tone, 3rd-order intermodulation intercept as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices. This matching network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA2846 drives directly into the input of a high impedance device, such as an A/D converter, the 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm. The intercept is used to predict the intermodulation spurious for two, closely-spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $f = |f_2 - f_1|/2$, the two 3rd-order, close-in spurious tones will appear at $f_O \pm 3 \times \Delta f$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $dBc = 2 \times (IM3 - P_O)$ where IM3 is the intercept taken from the Typical Characteristic and P_O is the power level, in dBm, at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 10MHz, the OPA2846 at a gain of +10 has an intercept of 44dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be $2 \times (48 - 4) = 88dBc$ below the test-tone power level (−84dBm). If this same $2V_{PP}$, 2-tone envelope were delivered directly into the input of an ADC—without the matching loss or the loading of the 50Ω network—the intercept would increase to at least 50dBm. With the same signal and gain conditions, but now driving directly into a light load, the spurious tones will then be at least $2 \times (54 - 4) = 100dBc$ below the 4dBm test-tone power levels centered on 10MHz.

DC ACCURACY AND OFFSET CONTROL

The OPA2846 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of its low ±0.65mV input offset voltage, careful attention to input bias current cancellation is also required. The low noise input stage of the OPA2846 has a relatively high input bias current (10μA typical into the pins), but with a very close match between the two input currents—typically ±100nA input offset current. The total output offset voltage may be reduced considerably by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 (page 12) would be to insert a 20Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this will increase the source resistances for the noninverting input bias current to 45Ω. Since this is now equal to the resistance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the gains for the bias currents to the output, leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using the 453Ω feedback resistor, this output error will now be less than $\pm 0.6\mu A \times 453\Omega = \pm 0.27mV$ over the full temperature range.

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to insure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal will set up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness.

Figure 13 shows one example of an offset adjustment for a DC-coupled signal path that will have minimum impact on the signal frequency response. In this case, the input is brought into an inverting gain resistor with the DC adjustment an additional current summed into the inverting node. The resistor values setting this offset adjustment are much larger than the signal path resistors. This will insure that this adjustment has minimal impact on the loop gain and hence, the frequency response as well.

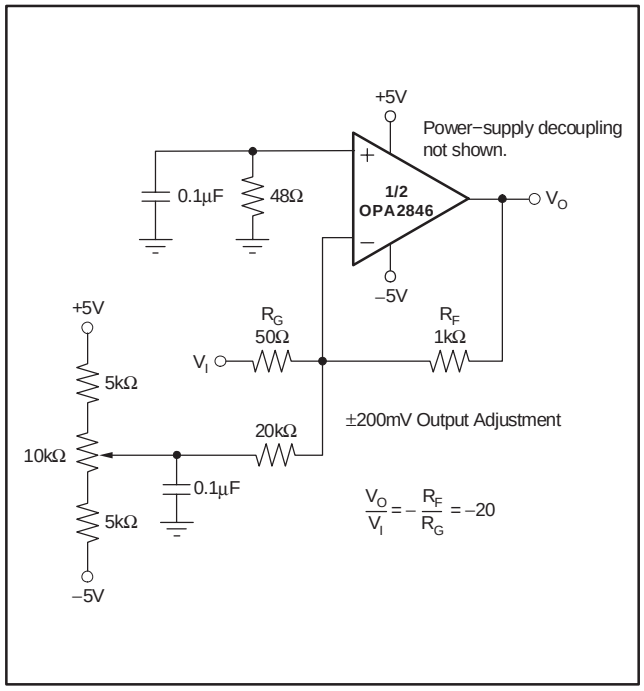


Figure 13. DC-Coupled, Inverting Gain of −20, with Output Offset Adjustment

THERMAL ANALYSIS

The OPA2846 will not require heatsinking or airflow in most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using both channels of the OPA2846ID in the circuit of Figure 1 (page 12) operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load at $+2.5V_{DC}$:

$P_D = 10V \times (26.6mA) + 2 \times [5^2/(4 \times (100\Omega \parallel 500\Omega))] = 416mW$

Maximum $T_J = +85°C + (0.416\Omega \times 125°C/\Omega) = 137°C$

This absolute worst-case example will never be encountered in practice. Therefore, 137°C sets an upper limit to maximum operating junction temperature.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the OPA2846 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2846. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback

resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. It has been suggested here that a good starting point for design would be to set R_G to 50Ω. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2846 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2846 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot, *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2846 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2846 onto the board.

INPUT AND ESD PROTECTION

The OPA2846 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 13.

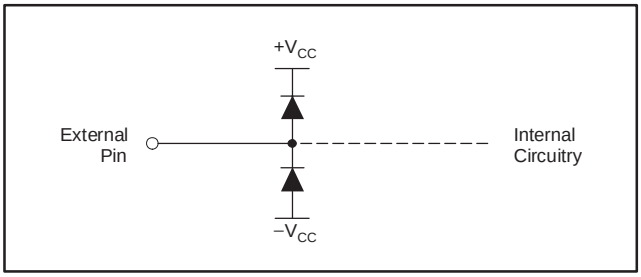


Figure 14. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2846), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	C	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
5/06	B	18	Design-In Tools	Demonstration fixture number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2846ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2846
OPA2846ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2846
OPA2846IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2846
OPA2846IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2846

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

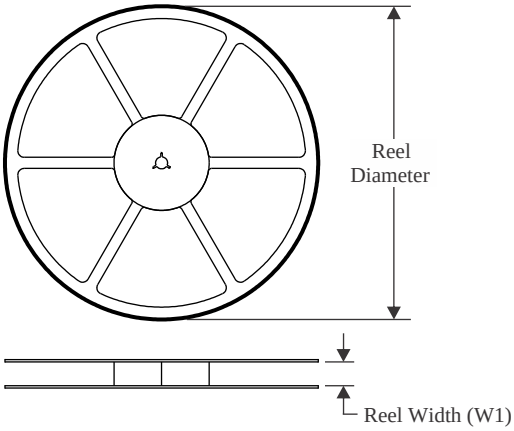
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

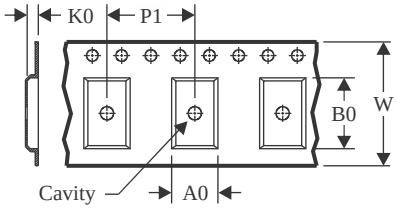
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

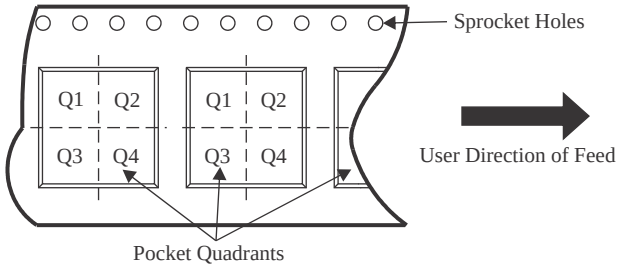


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

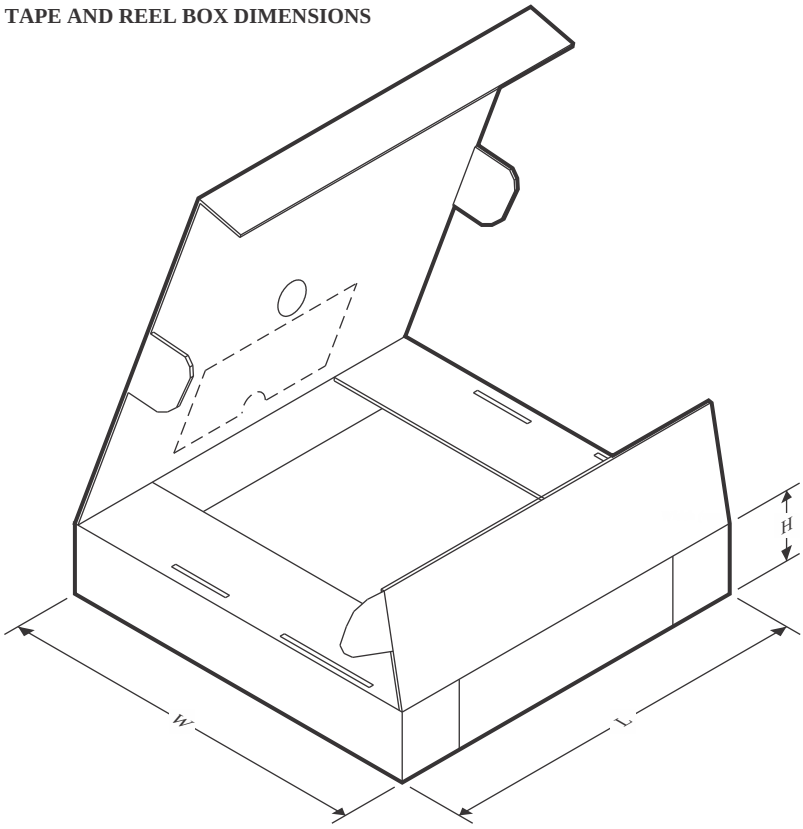
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2846IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

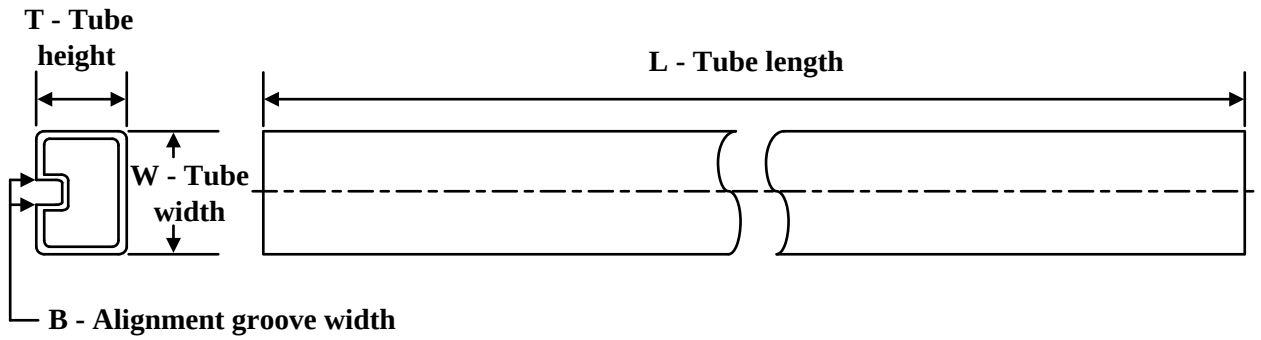
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

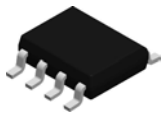
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2846IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2846ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2846ID.A	D	SOIC	8	75	506.6	8	3940	4.32

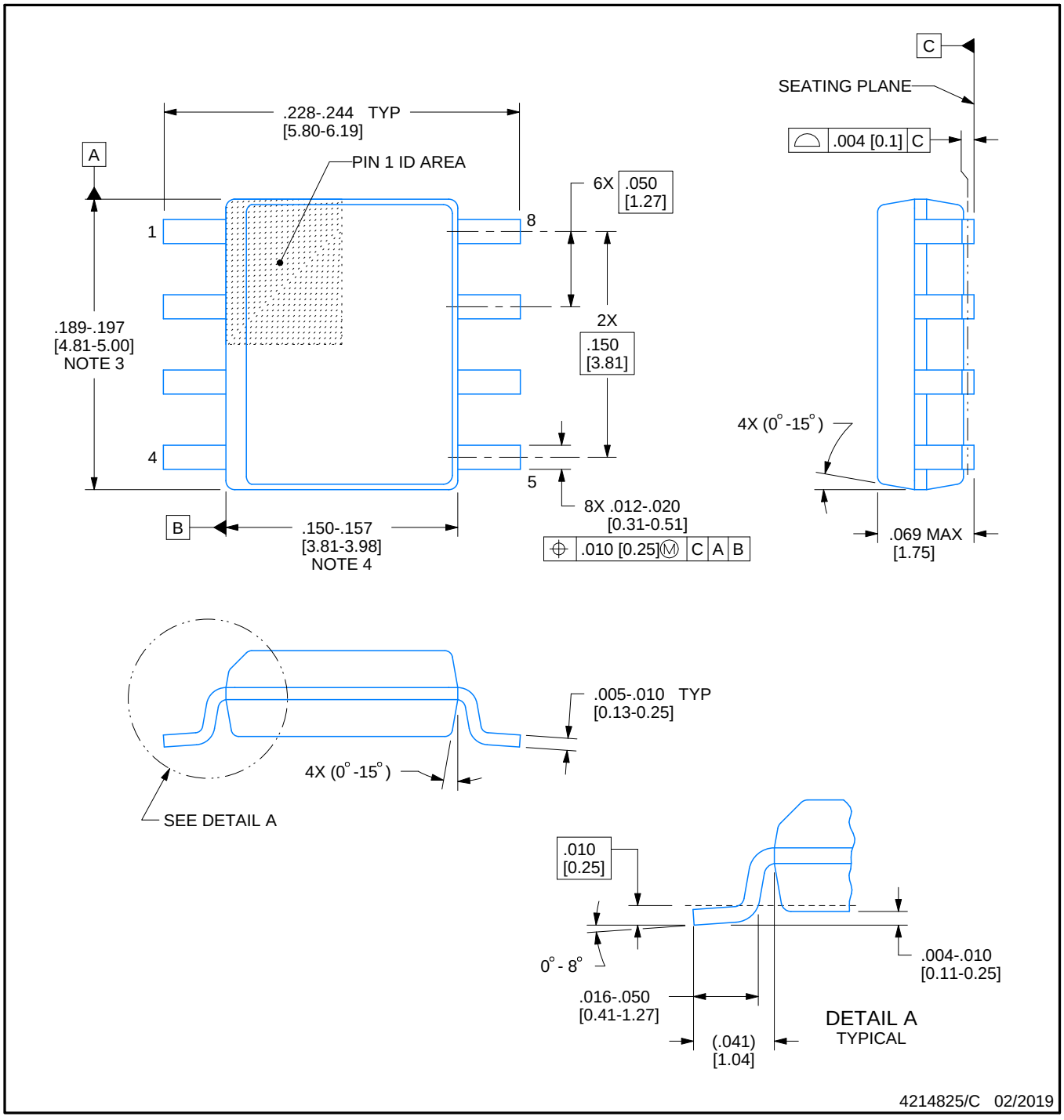


PACKAGE OUTLINE

D0008A

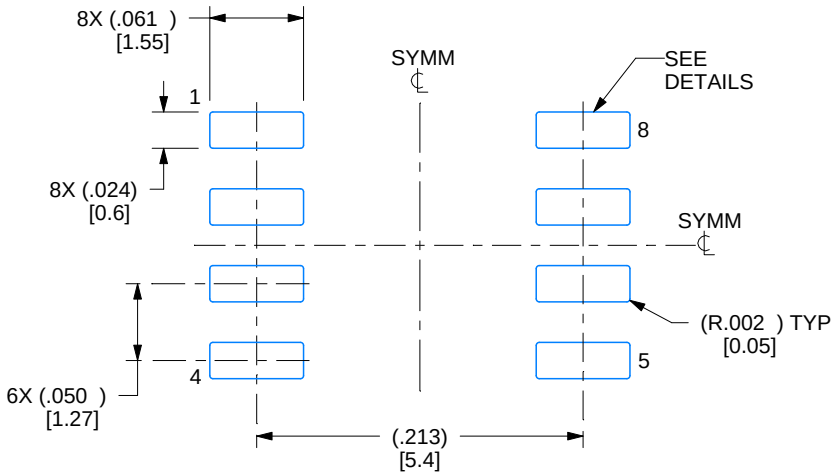
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

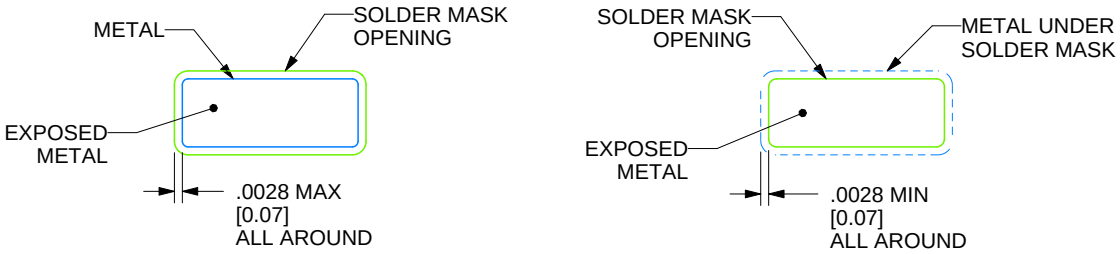


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

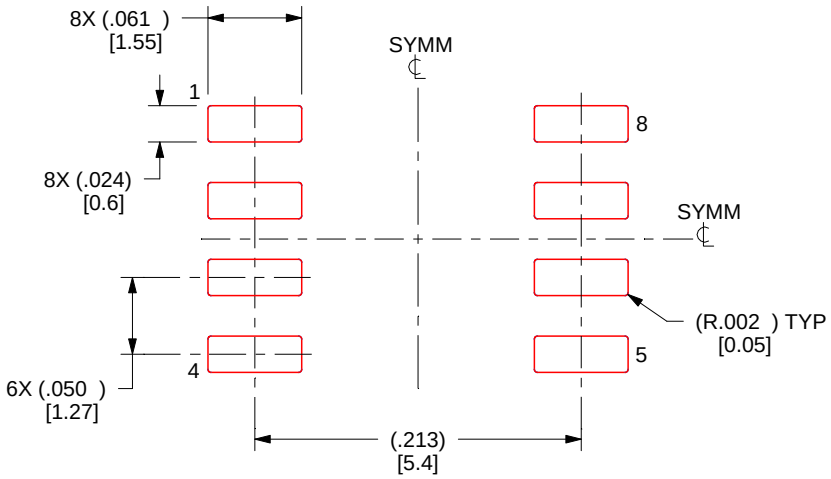
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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