参考資料

OPA2836-Q1 超低消費電力、レール・ツー・レール出力、負レール入力、電圧帰還型オペアンプ

1 特長

- **車載アプリケーションに対応**
- **下記内容でAEC-Q100認定済み：**
  - デバイス温度グレード1: 動作時周囲温度範囲 −40°C～125°C
  - デバイスHBM分類レベル2
  - デバイスCDM分類レベルC6
- **低消費電力**
  - 電源電圧: 2.5V～5.5V
  - 静止電流: 1mA (標準値)
  - パワーダウン･モード: 0.5µA (標準値)
- **帯域幅**: 205MHz
- **スルーレート**: 560V/µs
- **立ち上がり時間**: 3ns (2V_{STEP})
- **セトリング時間**(0.1%): 22ns (2V_{STEP})
- **オーバードライブ回復時間**: 60ns
- **SN比**: 0.00013% (–117.6dBc) (1kHz (1V_{RMS}) **時**)
- **全高周波歪み率**: 0.00003% (–130dBc) (1kHz (1V_{RMS}) **時**)
- HD_2, HD_3: –85dBc、–105dBc (1MHz、2V_{PP}**時**)
- **入力電圧ノイズ**: 4.6 nV/√Hz (f = 100 kHz)
- **入力オフセット電圧**: 65µV (±400µV**最大**)
- CMRR: 116dB
- **出力電流ドライブ**: 50mA
- RRO: **レール・ツー・レール出力**
- **入力電圧範囲**: −0.2V～＋3.9V (5V**電源使用時**)

2 アプリケーション

- 低消費電力のシグナル・コンディショニング
- オーディオ用A/Dコンバータの入力バッファ
- 低消費電力SARおよびΔΣ A/Dコンバータのドライバ
- ポータブル・システム
- 低消費電力システム
- 高密度システム

3 概要

OPA2836-Q1デバイスは、電圧範囲が2.5V～5.5Vの単一電源、または±1.25V～±2.75Vのデュアル電源で動作するように設計された、デュアル･チャネル、レール･ツー･レール出力、負レール入力、超低消費電力の電圧帰還型オペアンプです。このアンプは、1チャネルの消費電力がわずか1mA、単位利得帯域幅が205MHzであり、レール･ツー･レール･アンプの分野では業界トップの電力性能比を実現しています。

OPA2836-Q1は低消費電力で高周波性能が優れているため、電力性能がきわめて重要な意味を持つ電池駆動の携帯アプリケーションに適し、他のデバイスでは不可能な電力性能比を設計者に提供します。

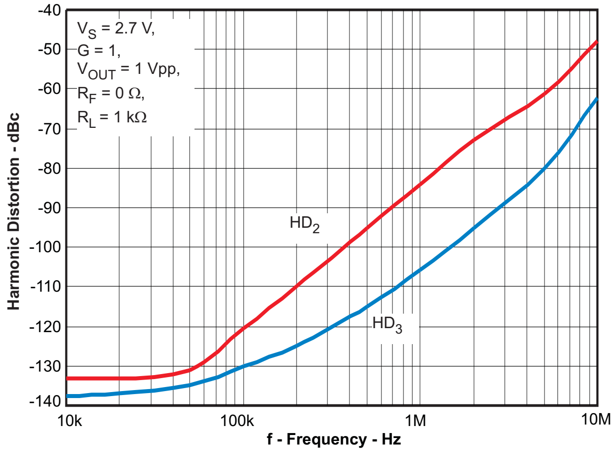
OPA2836-Q1は動作温度範囲が広く、産業用途に適する−40°C～＋125°Cとなっています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA2836-Q1	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

高調波歪みと周波数との関係



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4 改訂履歴

日付	改訂内容	注
2016年12月	*	初版

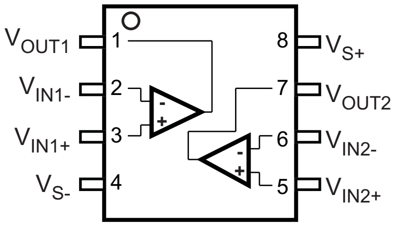
5 OPA2836-Q1 Related Devices

DEVICE	BW (A_V = 1) (MHz)	SLEW RATE (V/µs)	I_Q (5 V) (mA)	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL IN/OUT	DUALS
OPA836	205	560	1	4.6	–VS/Out	OPA2836
OPA835	30	110	0.25	9.3	–VS/Out	OPA2835
OPA365	50	25	5	4.5	In/Out	OPA2365
THS4281	95	35	0.75	12.5	In/Out	—
LMH6618	140	45	1.25	10	In/Out	LMH6619
OPA830	310	600	3.9	9.5	–VS/Out	OPA2830

For a complete selection of TI high-speed amplifiers, visit www.ti.com.

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

NAME	PIN	I/O	DESCRIPTION
V_{IN1+}	3	Input	Amplifier 1 noninverting input
$V_{IN1–}$	2	Input	Amplifier 1 inverting input
V_{IN2+}	5	Input	Amplifier 2 noninverting input
$V_{IN2–}$	6	Input	Amplifier 2 inverting input
V_{OUT1}	1	Output	Amplifier 1 output
V_{OUT2}	7	Output	Amplifier 2 output
V_{S+}	8	Power	Positive power supply input
$V_{S–}$	4	Power	Negative power supply input

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		5.5	V
V_I	Input voltage	V_{S-} – 0.7	V_{S+} + 0.7	V
V_{ID}	Differential input voltage		1	V
I_I	Continuous input current		0.85	mA
I_O	Continuous output current		60	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±6000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single supply voltage	2.5	5	5.5	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA2836-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	69.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_S = 2.7 V

test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V; T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV$_{PP}$, G = 1		200		MHz	C
	V_{OUT} = 100 mV$_{PP}$, G = 2		100			C
	V_{OUT} = 100 mV$_{PP}$, G = 5		26			C
	V_{OUT} = 100 mV$_{PP}$, G = 10		11			C
Gain-bandwidth product	V_{OUT} = 100 mV$_{PP}$, G = 10		110		MHz	C
Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 2		60		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 1 V_{PP}, G = 2		25		MHz	C
Slew rate, rise	V_{OUT} = 1 V_{STEP}, G = 2		260		V/µs	C
Slew rate, fall	V_{OUT} = 1 V_{STEP}, G = 2		240		V/µs	C
Rise time	V_{OUT} = 1 V_{STEP}, G = 2		4		ns	C
Fall time	V_{OUT} = 1 V_{STEP}, G = 2		4.5		ns	C
Settling time to 1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		15		ns	C
Settling time to 1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		15		ns	C
Settling time to 0.1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		30		ns	C
Settling time to 0.1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		25		ns	C
Settling time to 0.01%, rise	V_{OUT} = 1 V_{STEP}, G = 2		50		ns	C
Settling time to 0.01%, fall	V_{OUT} = 1 V_{STEP}, G = 2		45		ns	C
Overshoot	V_{OUT} = 1 V_{STEP}, G = 2		5%			C
Undershoot	V_{OUT} = 1 V_{STEP}, G = 2		3%			C
Second-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–133		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–120			C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–84			C
Third-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–137		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–130			C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–105			C
Second-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5 V		–90		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5 V		–90		dBc	C
Input voltage noise	f = 100 kHz		4.6		nV/√Hz	C
Voltage noise 1/f corner frequency			215		Hz	C
Input current noise	f = 1 MHz		0.75		pA/√Hz	C
Current noise 1/f corner frequency			31.7		kHz	C
Overdrive recovery time	Overdrive = 0.5 V		55		ns	C
Underdrive recovery time	Underdrive = 0.5 V		60		ns	C
Closed-loop output impedance	f = 100 kHz		0.02		Ω	C
Channel-to-channel crosstalk	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	125		dB	A
Input-referred offset voltage	T_A = 25°C	–400	±65	400	µV	A
	T_A = –40°C to +85°C	–760		760		B
	T_A = –40°C to +125°C	–1060		1060		B
Input offset voltage drift(2)	T_A = –40°C to +85°C	–6	±1	6	µV/°C	B
	T_A = –40°C to +125°C	–6.6	±1.1	6.6		B

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

(2) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

Electrical Characteristics: V_S = 2.7 V (continued)

test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V; T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
DC PERFORMANCE (continued)						
Input bias current(3)	T_A = 25°C	200	650	1000	nA	A
	T_A = –40°C to +85°C	120		1500		B
	T_A = –40°C to +125°C	100		1800		B
Input bias current drift(2)	T_A = –40°C to +85°C	–1.9	±0.32	1.9	nA/°C	B
	T_A = –40°C to +125°C	–3.5	±0.37	2.1		B
Input offset current	T_A = 25°C	–180	±30	180	nA	A
	T_A = –40°C to +85°C	–215	±30	215		B
	T_A = –40°C to +125°C	–240	±30	240		B
Input offset current drift(2)	T_A = –40°C to +85°C	–575	±95	575	pA/°C	B
	T_A = –40°C to +125°C	–600	±100	600		B
INPUT						
Common-mode input range, low	T_A = 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range, high	T_A = 25°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	B
Input linear operating voltage range	T_A = 25°C, < 6-dB degradation in THD		–0.3 to 1.75		V	C
Common-mode rejection ratio		91	114		dB	A
Input impedance common-mode			200 || 1.2		kΩ || pF	C
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Output voltage, low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to +125°C, G = 5		0.15	0.2	V	B
Output voltage, high	T_A = 25°C, G = 5	2.45	2.5		V	A
	T_A = –40°C to +125°C, G = 5	2.45	2.5		V	B
Output saturation voltage, high	T_A = 25°C, G = 5		80		mV	C
Output saturation voltage, low	T_A = 25°C, G = 5		40		mV	C
Output current drive	T_A = 25°C	±40	±45		mA	A
	T_A = –40°C to +125°C	±40	±45		mA	B
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	0.7	0.95	1.15	mA	A
	T_A = –40°C to +125°C	0.6		1.6	mA	B
Power-supply rejection ratio (±PSRR)		91	108		dB	A

(3) Current is considered positive out of the pin.

7.6 Electrical Characteristics: V_S = 5 V

test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply; T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[1]
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		205		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		100			C
	V_{OUT} = 100 mV_{PP}, G = 5		28			C
	V_{OUT} = 100 mV_{PP}, G = 10		11.8			C
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		118		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 2		87		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 2		29		MHz	C
Slew rate, rise	V_{OUT} = 2-V step, G = 2		560		V/µs	C
Slew rate, fall	V_{OUT} = 2-V step, G = 2		580		V/µs	C
Rise time	V_{OUT} = 2-V step, G = 2		3		ns	C
Fall time	V_{OUT} = 2-V Step, G = 2		3		ns	C
Settling time to 1%, rise	V_{OUT} = 2-V step, G = 2		22		ns	C
Settling time to 1%, fall	V_{OUT} = 2-V step, G = 2		22		ns	C
Settling time to 0.1%, rise	V_{OUT} = 2-V step, G = 2		30		ns	C
Settling time to 0.1%, fall	V_{OUT} = 2-V step, G = 2		30		ns	C
Settling time to 0.01%, rise	V_{OUT} = 2-V step, G = 2		40		ns	C
Settling time to 0.01%, fall	V_{OUT} = 2-V step, G = 2		45		ns	C
Overshoot	V_{OUT} = 2-V step, G = 2		7.5%			C
Undershoot	V_{OUT} = 2-V step, G = 2		5%			C
Second-order harmonic distortion	f = 10 kHz		–133		dBc	C
	f = 100 kHz		–120			C
	f = 1 MHz		–85			C
Third-order harmonic distortion	f = 10 kHz		–140		dBc	C
	f = 100 kHz		–130			C
	f = 1 MHz		–105			C
Second-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} envelope = 2 V_{PP}		–79		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} envelope = 2 V_{PP}		–91		dBc	C
Signal-to-noise ratio (SNR)	f = 1 kHz, V_{OUT} = 1 V_{RMS}, 22-kHz bandwidth		0.00013%			C
			–117.6		dBc	C
Total harmonic distortion (THD)	f = 1 kHz, V_{OUT} = 1 V_{RMS}		0.00003%			C
			–130		dBc	C
Input voltage noise	f = 100 KHz		4.6		nV/√Hz	C
Voltage noise 1/f corner frequency			215		Hz	C
Input current noise	f > 1 MHz		0.75		pA/√Hz	C
Current noise 1/f corner frequency			31.7		kHz	C
Overdrive recovery time	Overdrive = 0.5 V		55		ns	C
Underdrive recovery time	Underdrive = 0.5 V		60		ns	C
Closed-loop output impedance	f = 100 kHz		0.02		Ω	C
Channel-to-channel crosstalk	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	122		dB	A
Input-referred offset voltage	T_A = 25°C	–400	±65	400	µV	A
	T_A = –40°C to +85°C	–765		765		B
	T_A = –40°C to +125°C	–1080		1080		B

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

Electrical Characteristics: V_S = 5 V (continued)

test conditions unless otherwise noted: V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply; T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
DC PERFORMANCE (continued)						
Input offset voltage drift(2)	T_A = –40°C to +85°C	–6.1	±1	6.1	µV/°C	B
	T_A = –40°C to +125°C	–6.8	±1.1	6.8		B
Input bias current(3)	T_A = 25°C	200	650	1000	nA	A
	T_A = –40°C to +85°C	120		1550		B
	T_A = –40°C to +125°C	100		1850		B
Input bias current drift(2)	T_A = –40°C to +85°C		±0.34	±2	nA/°C	B
	T_A = –40°C to +125°C		±0.38	±3.8		B
Input offset current	T_A = 25°C		±30	±180	nA	A
	T_A = –40°C to +85°C		±30	±215		B
	T_A = –40°C to +125°C		±30	±250		B
Input offset current drift(2)	T_A = –40°C to +85°C		±100	±600	pA/°C	B
	T_A = –40°C to +125°C		±110	±660		B
INPUT						
Common-mode input range low	T_A = 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	B
Input linear operating voltage range	T_A = 25°C, < 6-dB degradation in THD		–0.3 to 4.05		V	C
Common-mode rejection ratio		94	116		dB	A
Input impedance common mode			200 || 1.2		kΩ || pF	C
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to +125°C, G = 5		0.15	0.2	V	B
Output voltage high	T_A = 25°C, G = 5	4.75	4.8		V	A
	T_A = –40°C to +125°C, G = 5	4.75	4.8		V	B
Output saturation voltage, high	T_A = 25°C, G = 5		100		mV	C
Output saturation voltage, low	T_A = 25°C, G = 5		50		mV	C
Output current drive	T_A = 25°C	±40	±50		mA	A
	T_A = –40°C to +125°C	±40	±50		mA	B
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	0.8	1.0	1.2	mA	A
	T_A = –40°C to +125°C	0.65		1.7	mA	B
Power-supply rejection ratio (±PSRR)		94	108		dB	A

(2) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

(3) Current is considered positive out of the pin.

7.7 Typical Characteristics

7.7.1 Typical Characteristics: V_S = 2.7 V

test conditions unless otherwise noted: V_{S+} = 2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V; T_A = 25°C (unless otherwise noted)

Table 1. Table of Graphs

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Input Offset Voltage Drift	Figure 46
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Input Offset Current vs Free-Air Temperature	Figure 24
Input Offset Current Drift	Figure 25

test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V; T_A = 25°C (unless otherwise noted)

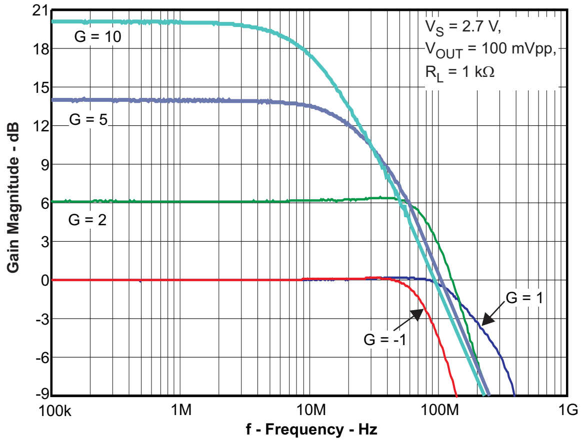


Figure 1. Small-Signal Frequency Response

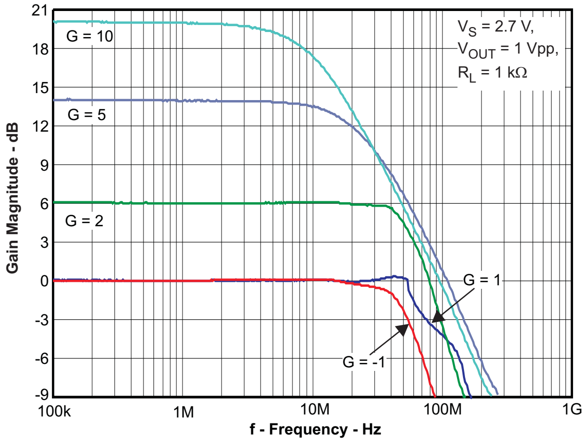


Figure 2. Large-Signal Frequency Response

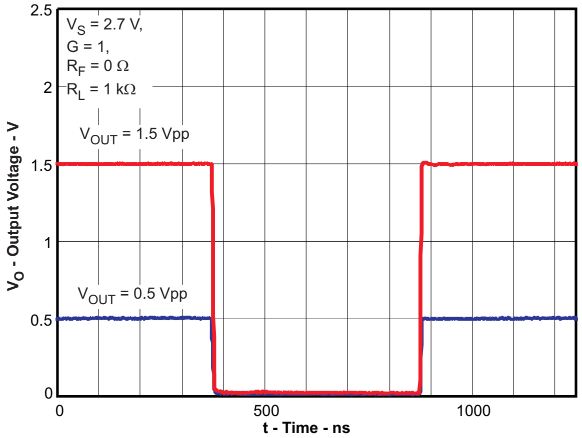


Figure 3. Noninverting Pulse Response

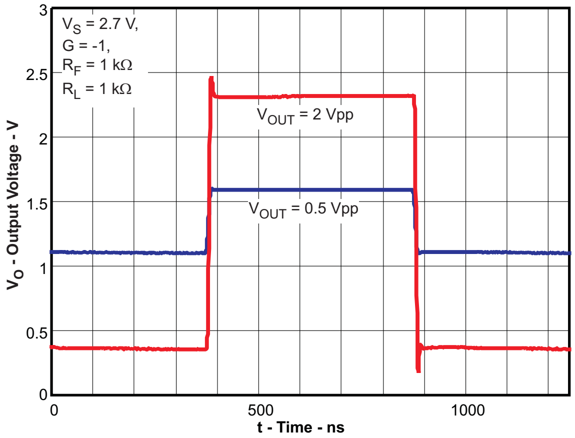


Figure 4. Inverting Pulse Response

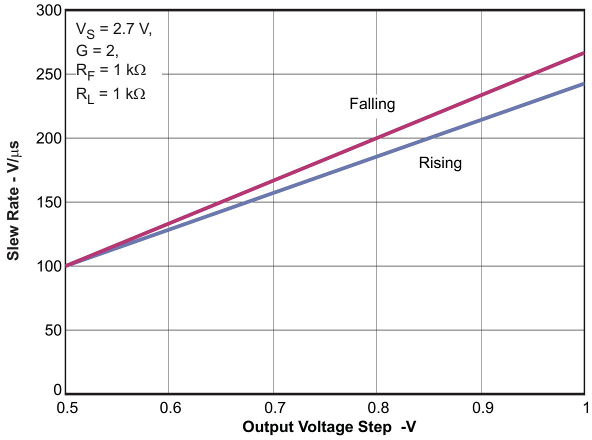


Figure 5. Slew Rate vs Output Voltage Step

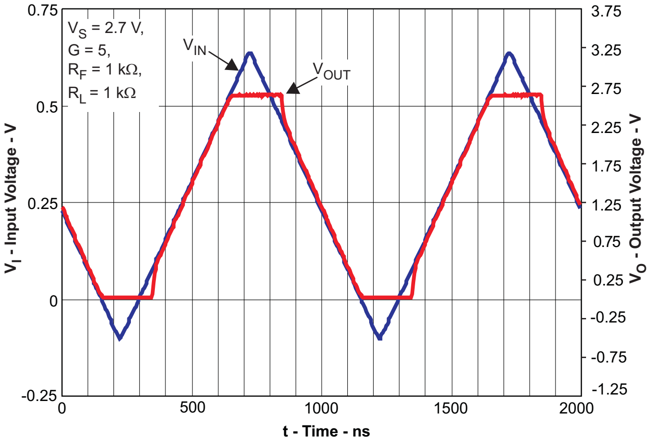


Figure 6. Output Overdrive Recovery

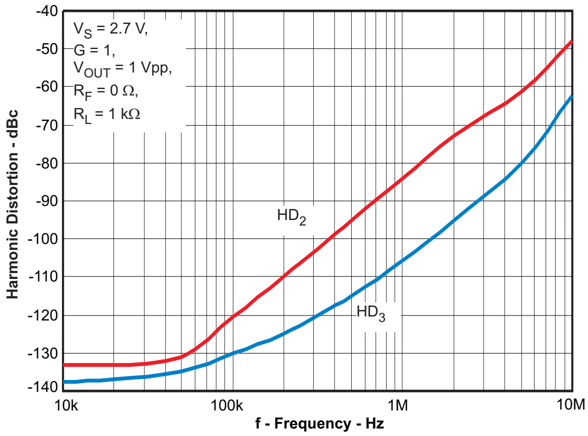


Figure 7. Harmonic Distortion vs Frequency

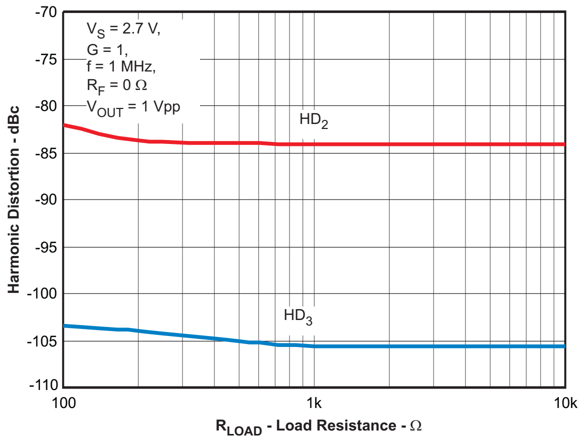


Figure 8. Harmonic Distortion vs Load Resistance

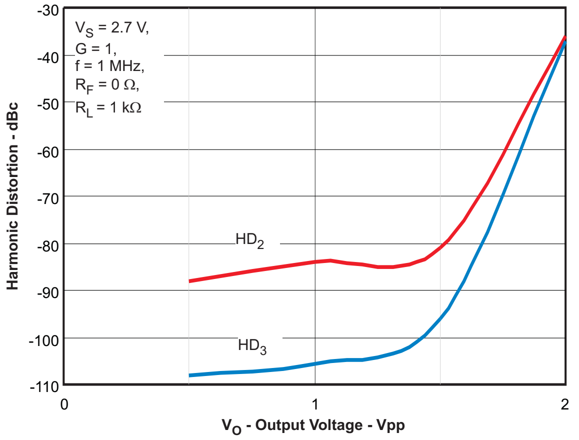


Figure 9. Harmonic Distortion vs Output Voltage

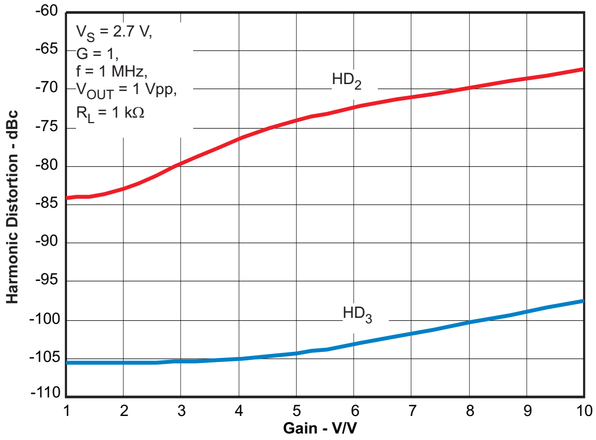


Figure 10. Harmonic Distortion vs Gain

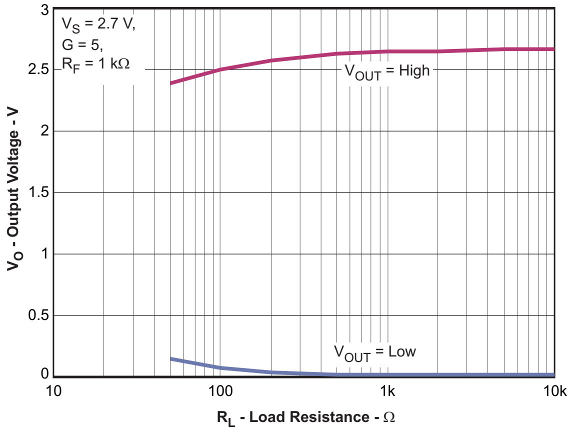


Figure 11. Output Voltage Swing vs Load Resistance

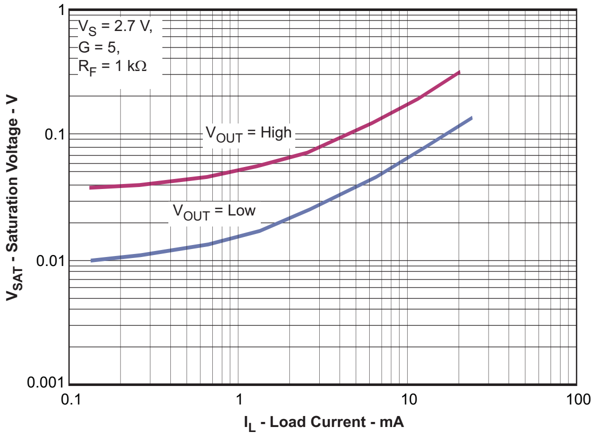


Figure 12. Output Saturation Voltage vs Load Current

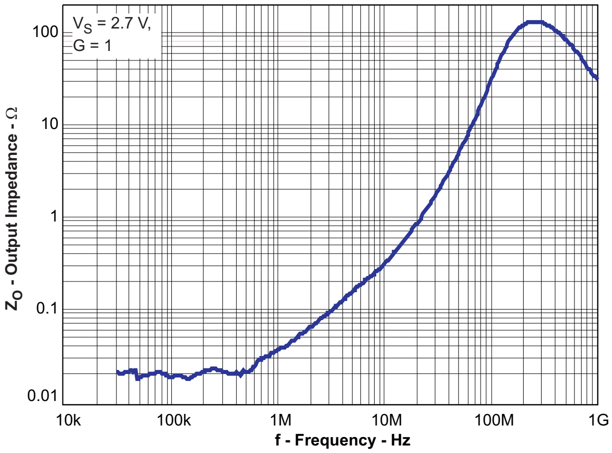


Figure 13. Output Impedance vs Frequency

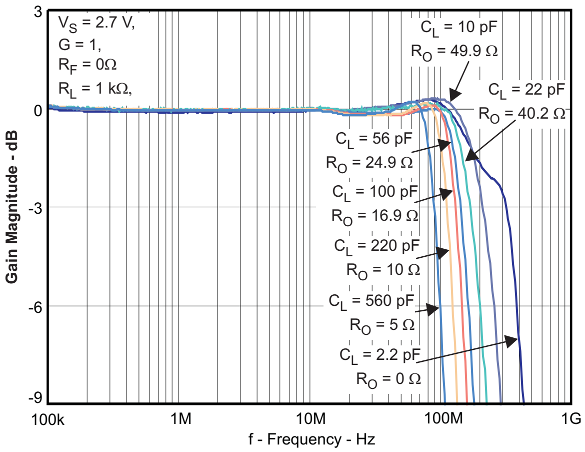
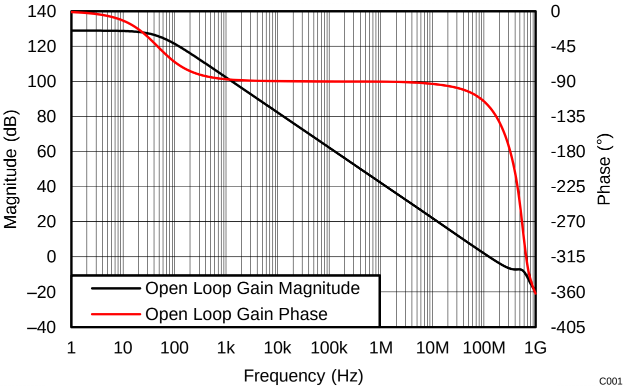
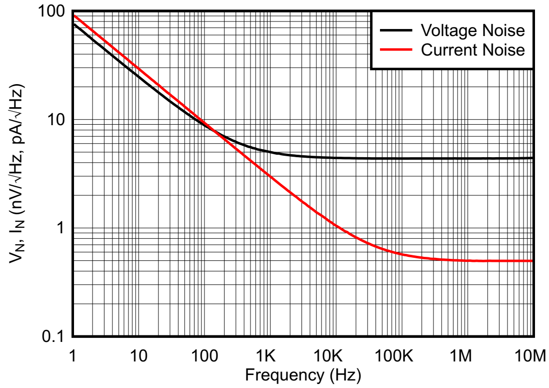


Figure 14. Frequency Response With Capacitive Load



V_S = 2.7 V

Figure 15. Open-Loop Gain vs Frequency



V_S = 2.7 V

Figure 16. Input-Referred Noise vs Frequency

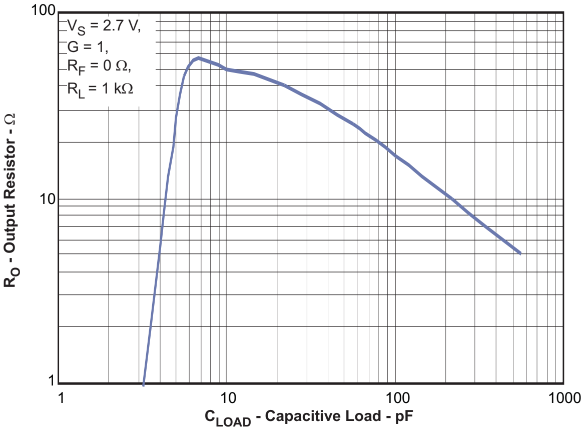


Figure 17. Series Output Resistor vs Capacitive Load

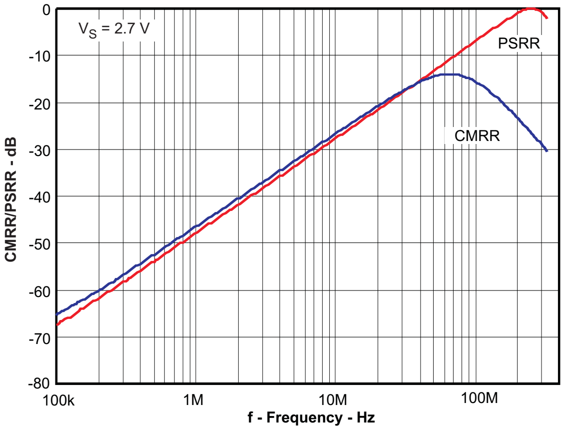


Figure 18. Common-Mode, Power-Supply Rejection Ratios vs Frequency

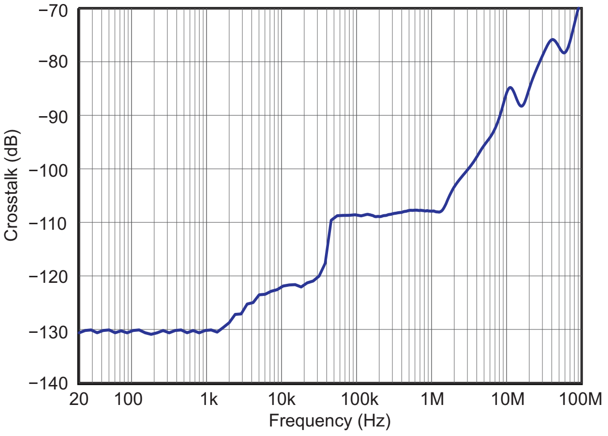


Figure 19. Crosstalk vs Frequency

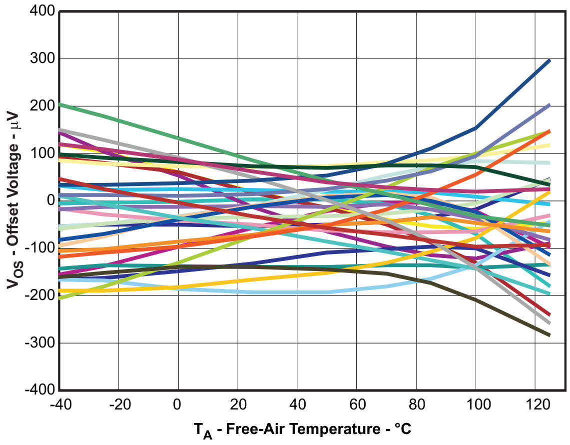


Figure 20. Input Offset Voltage vs Free-Air Temperature

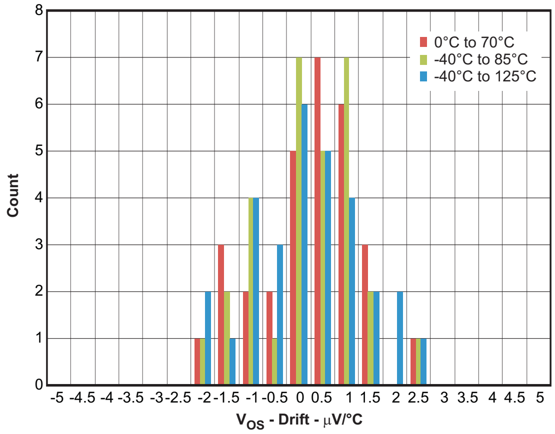


Figure 21. Input Offset Voltage Drift

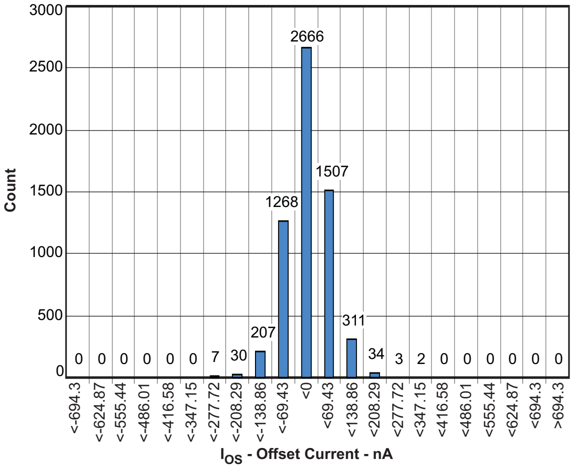


Figure 22. Input Offset Voltage

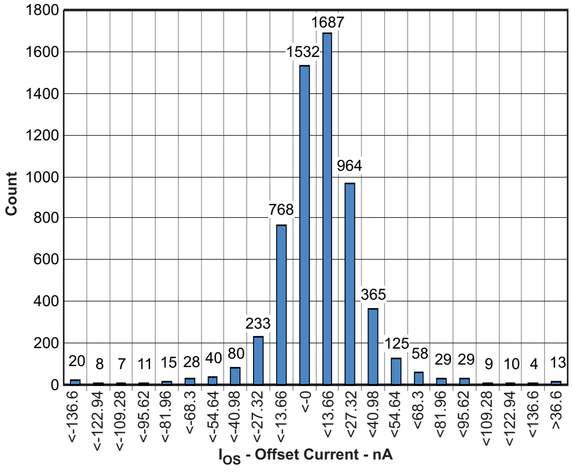


Figure 23. Input Offset Current

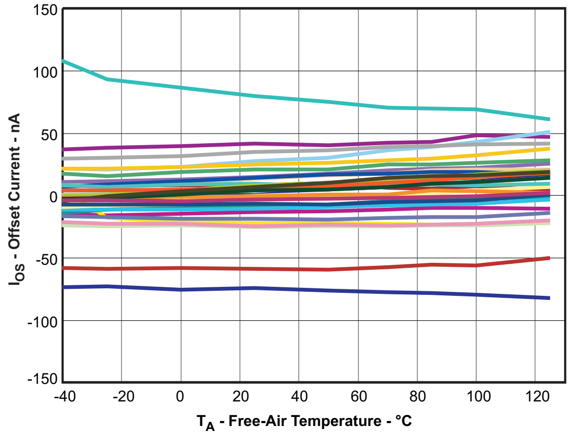


Figure 24. Input Offset Current vs Free-Air Temperature

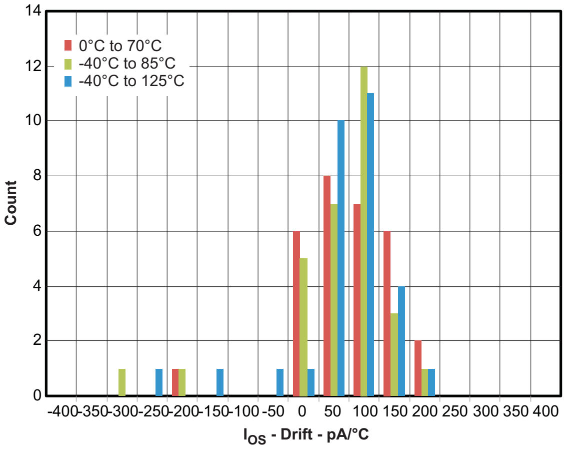


Figure 25. Input Offset Current Drift

7.7.2 Typical Characteristics: V_S = 5 V

test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply; T_A = 25°C (unless otherwise noted)

Table 2. Table of Graphs

FIGURE TITLE	FIGURE LOCATION
Small-Signal Frequency Response	Figure 26
Large-Signal Frequency Response	Figure 27
Noninverting Pulse Response	Figure 28
Inverting Pulse Response	Figure 29
Slew Rate vs Output Voltage Step	Figure 30
Output Overdrive Recovery	Figure 31
Harmonic Distortion vs Frequency	Figure 32
Harmonic Distortion vs Load Resistance	Figure 33
Harmonic Distortion vs Output Voltage	Figure 34
Harmonic Distortion vs Gain	Figure 35
Output Voltage Swing vs Load Resistance	Figure 36
Output Saturation Voltage vs Load Current	Figure 37
Output Impedance vs Frequency	Figure 38
Frequency Response With Capacitive Load	Figure 39
Series Output Resistor vs Capacitive Load	Figure 42
Input-Referred Noise vs Frequency	Figure 40
Open-Loop Gain vs Frequency	Figure 41
Common-Mode, Power-Supply Rejection Ratios vs Frequency	Figure 43
Crosstalk vs Frequency	Figure 44
Input Offset Voltage	Figure 47
Input Offset Voltage vs Free-Air Temperature	Figure 45
Input Offset Voltage Drift	Figure 46
Input Offset Current	Figure 48
Input Offset Current vs Free-Air Temperature	Figure 49
Input Offset Current Drift	Figure 50

test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply; T_A = 25°C (unless otherwise noted)

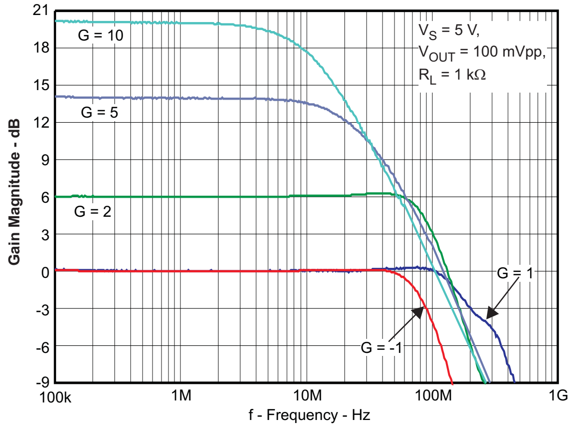


Figure 26. Small-Signal Frequency Response

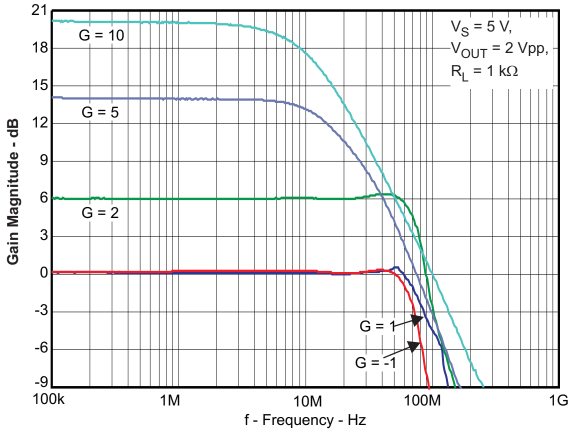


Figure 27. Large-Signal Frequency Response

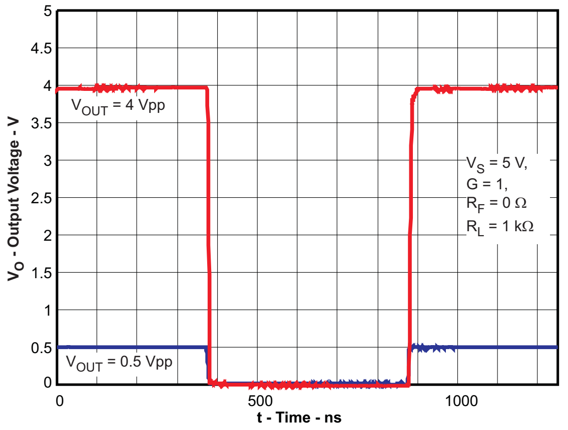


Figure 28. Noninverting Pulse Response

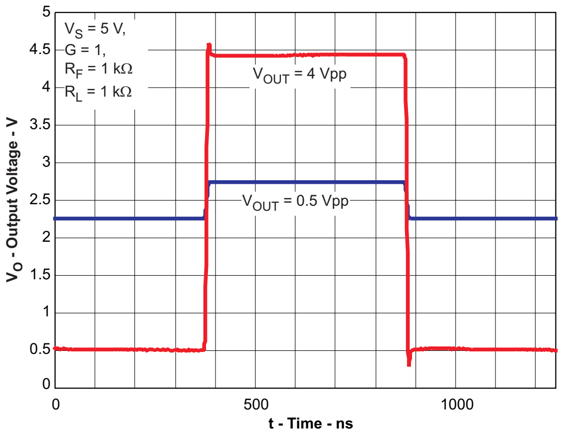


Figure 29. Inverting Pulse Response

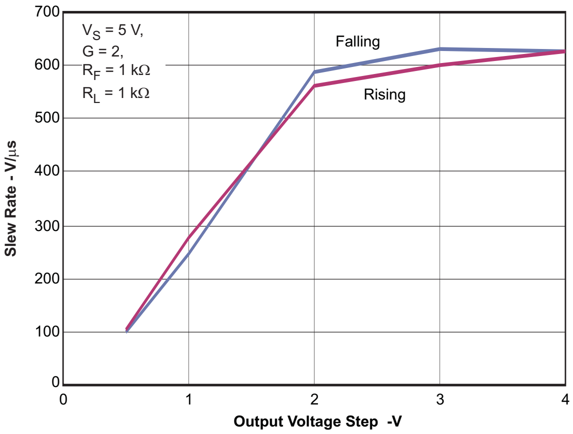


Figure 30. Slew Rate vs Output Voltage Step

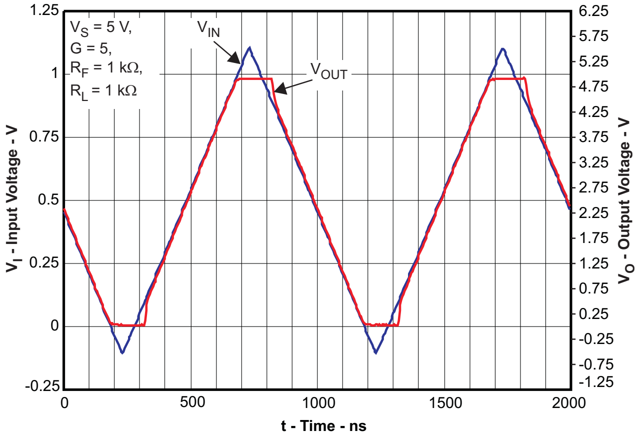


Figure 31. Output Overdrive Recovery

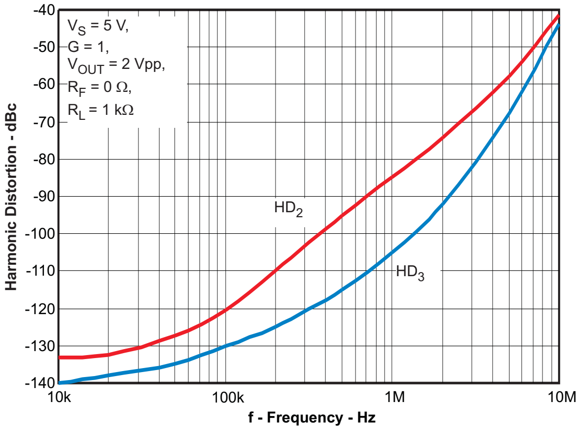


Figure 32. Harmonic Distortion vs Frequency

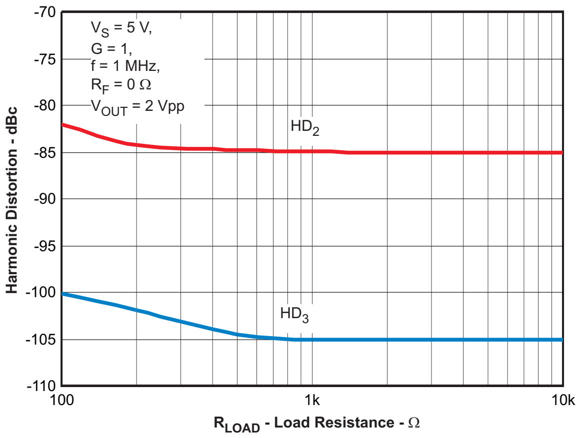


Figure 33. Harmonic Distortion vs Load Resistance

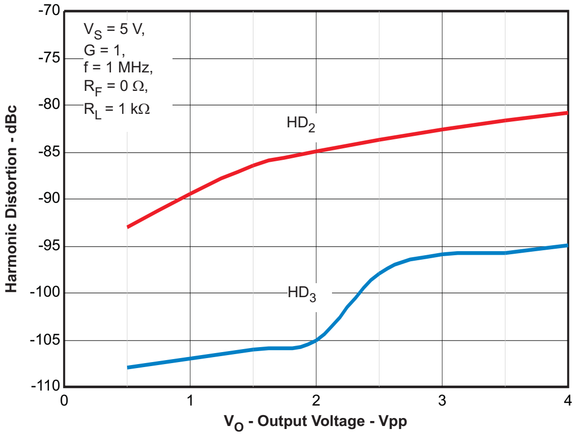


Figure 34. Harmonic Distortion vs Output Voltage

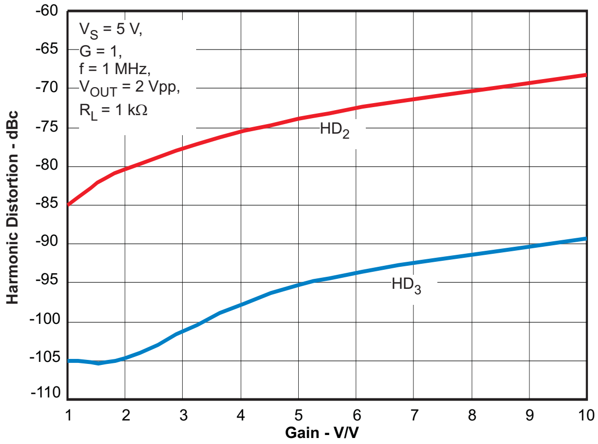


Figure 35. Harmonic Distortion vs Gain

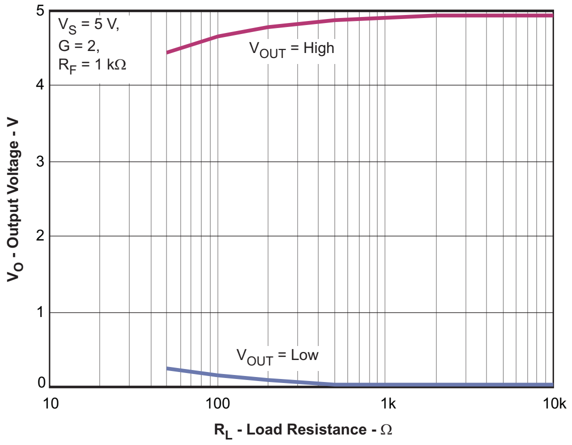


Figure 36. Output Voltage Swing vs Load Resistance

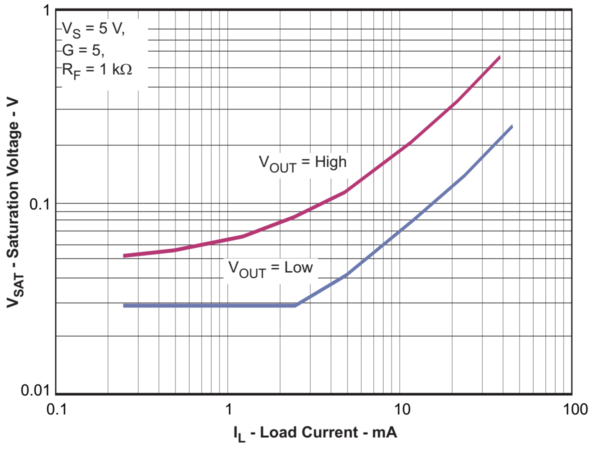


Figure 37. Output Saturation Voltage vs Load Current

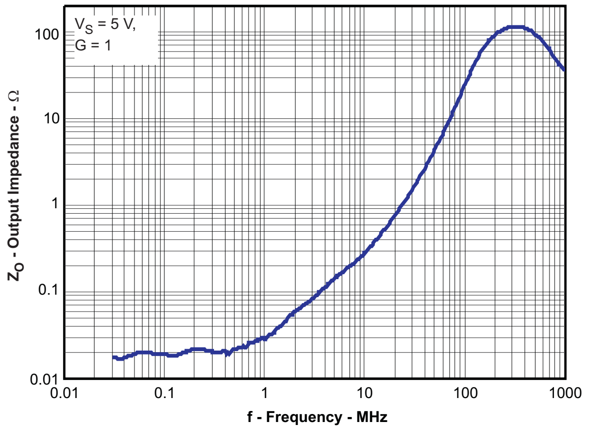


Figure 38. Output Impedance vs Frequency

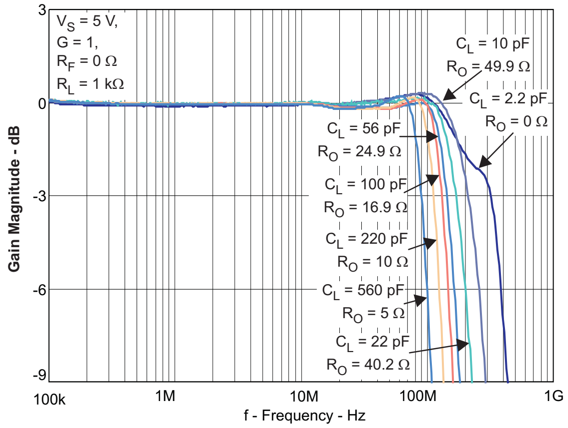
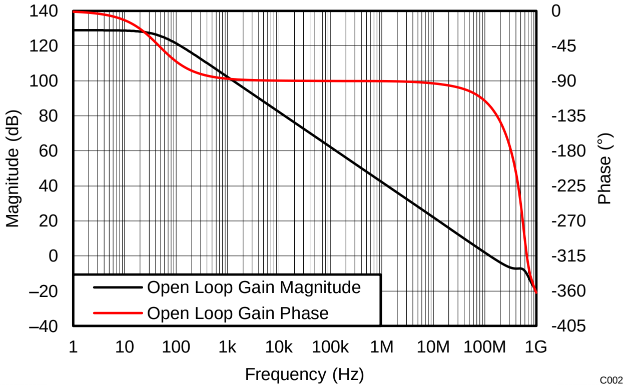
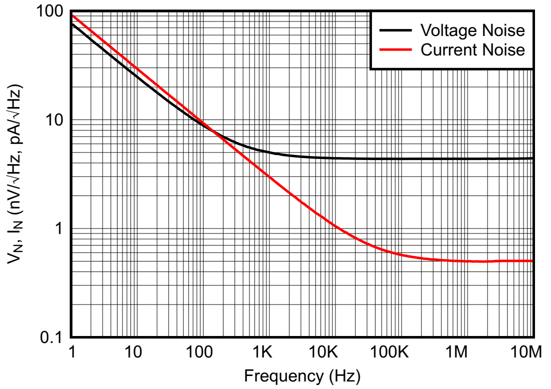


Figure 39. Frequency Response With Capacitive Load



V_S = 5.0 V

Figure 40. Open-Loop Gain vs Frequency



V_S = 5.0 V

Figure 41. Input-Referred Noise vs Frequency

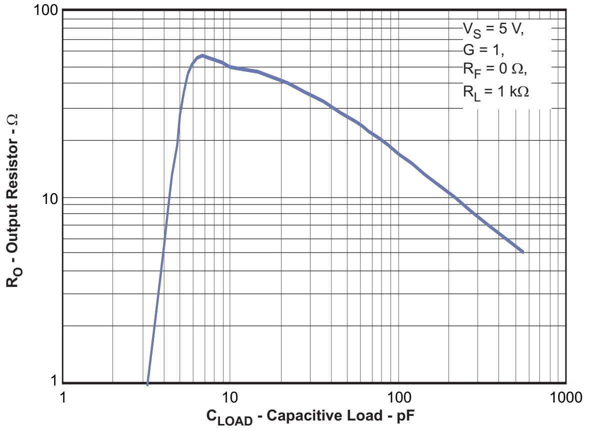


Figure 42. Series Output Resistor vs Capacitive Load

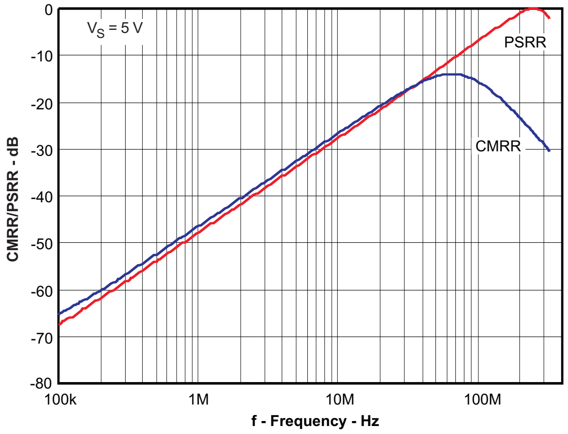


Figure 43. Common-Mode, Power-Supply Rejection Ratios vs Frequency

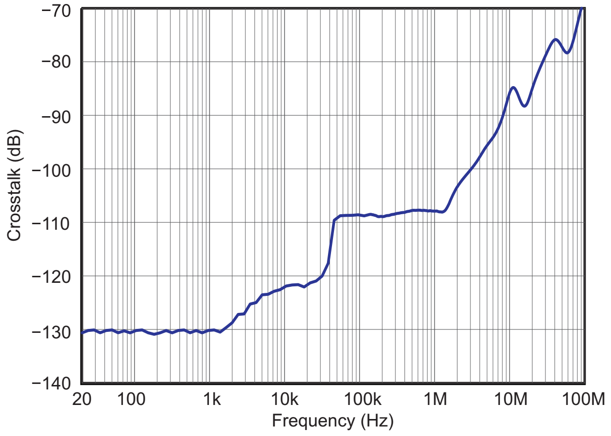


Figure 44. Crosstalk vs Frequency

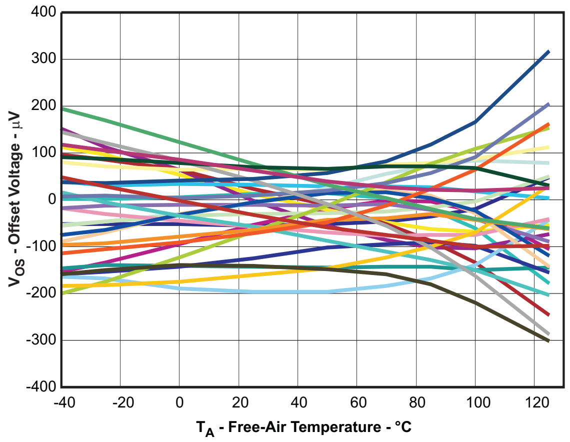


Figure 45. Input Offset Voltage vs Free-Air Temperature

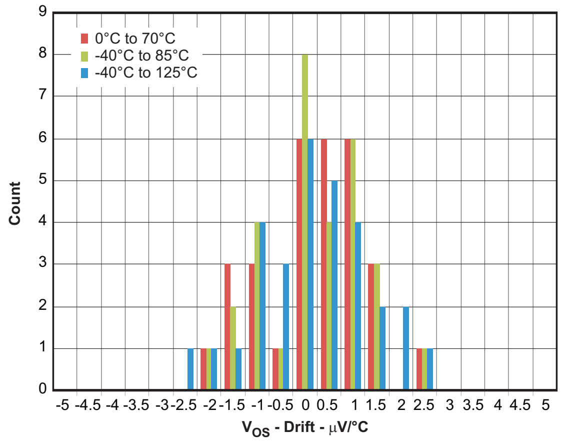


Figure 46. Input Offset Voltage Drift

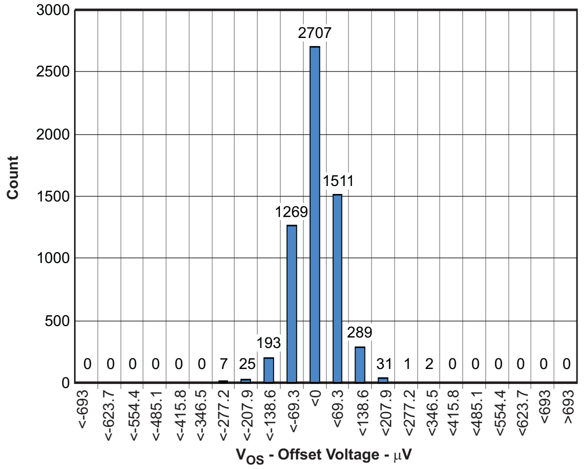


Figure 47. Input Offset Voltage

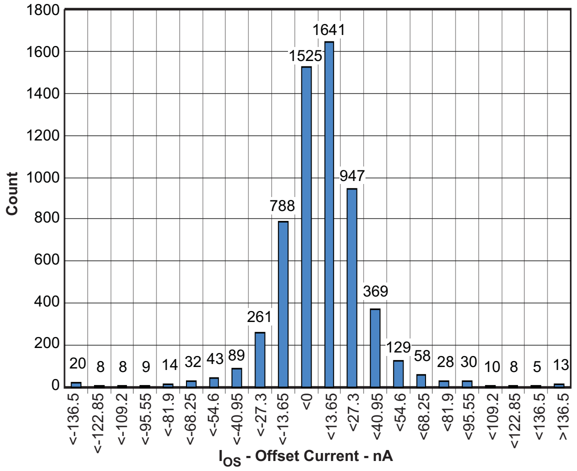


Figure 48. Input Offset Current

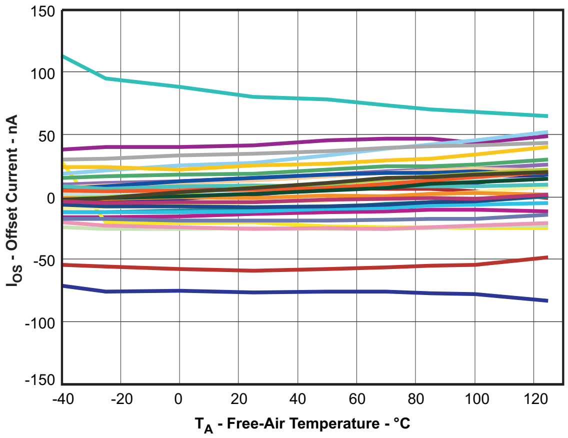


Figure 49. Input Offset Current vs Free-Air Temperature

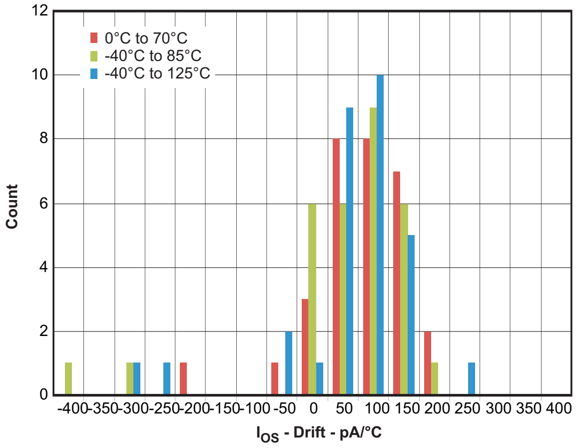


Figure 50. Input Offset Current Drift

8 Detailed Description

8.1 Overview

The OPA2836-Q1 bipolar input operational amplifier offers an excellent bandwidth of 205 MHz with ultra-low THD of 0.00003% at 1 kHz. The OPA2836-Q1 can swing to within 200 mV of the supply rails when driving a 1-kΩ load. The input common-mode of the amplifier can swing to 200 mV below the negative supply rail. This level of performance is achieved at 1 mA of quiescent current per amplifier channel.

8.2 Functional Block Diagrams

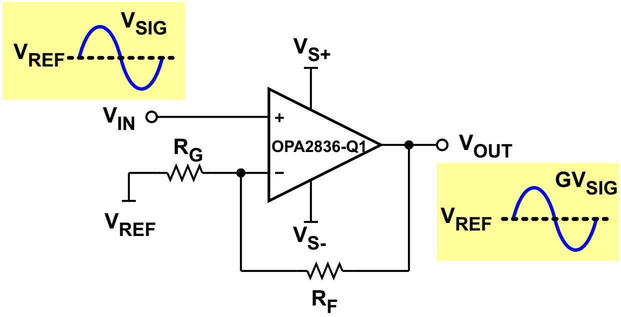


Figure 51. Noninverting Amplifier

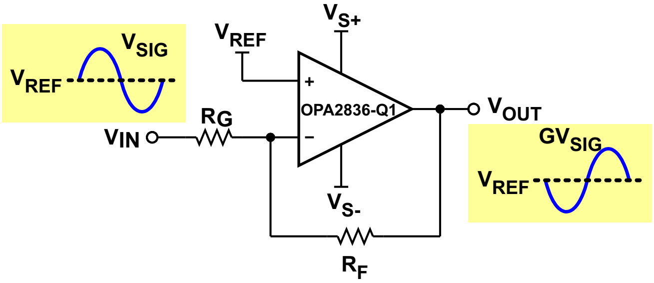


Figure 52. Inverting Amplifier

8.3 Feature Description

8.3.1 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier with high CMRR, the input common-mode voltage range (V_{ICR}) of the amplifier must not be violated.

The common-mode input range low and high specifications are based on CMRR. The specification limits are chosen to ensure CMRR does not degrade more than 3 dB below the mid-supply limit if the input voltage is kept within the specified range. The limits cover all process variations and most parts are better than specified. The typical specifications are from 0.2 V below the negative rail to 1.1 V below the positive rail.

Given that the operational amplifier is in linear operation, the voltage difference between the input pins is very small (ideally 0 V), and input common-mode voltage can be analyzed at either input pin with the other input pin assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In the noninverting configuration, Figure 51, the input signal V_{IN} must not violate V_{ICR}. In the inverting configuration, Figure 52, the reference voltage V_{REF} must be within V_{ICR}.

Feature Description (continued)

The input voltage limits have a fixed headroom to the power rails and track the power-supply voltages. For one 5-V supply, the linear input voltage range is –0.2 V to 3.9 V, and with a 2.7-V supply this range is –0.2 V to 1.6 V. The delta from each power-supply rail is the same in either case: –0.2 V and 1.1 V.

8.3.2 Output Voltage Range

The OPA2836-Q1 is a rail-to-rail output (RRO) operational amplifier. Rail-to-rail output typically means the output voltage can swing to within a couple hundred millivolts of the supply rails. There are two different ways to specify this: with the output still in linear operation and with the output saturated. Saturated output voltages are closer to the power-supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Both saturation and linear operation limits are affected by the current in the output, where higher currents lead to more loss in the output transistors.

Data in the *Electrical Characteristics* tables list both linear and saturated output voltage specifications with a 1-kΩ load. Figure 11 and Figure 36 illustrate saturated voltage-swing limits versus output load resistance, and Figure 12 and Figure 37 illustrate the output saturation voltage versus load current. Given a light load, the output voltage limits have a nearly constant headroom to the power rails and track the power-supply voltages. For example, with a 2-kΩ load and a single 5-V supply, the linear output voltage range is 0.15 V to 4.8 V, and with a 2.7-V supply this range is 0.15 V to 2.5 V. The delta from each power-supply rail is the same in either case: 0.15 V and 0.2 V.

With devices such as the OPA2836-Q1 where the input range is lower than the output range, the input typically limits the available signal swing only in the noninverting gain of 1. Signal swings in noninverting configurations in gains greater than +1 and in inverting configurations in any gain are generally limited by the output voltage limits of the operational amplifier.

8.3.3 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The OPA2836-Q1 is designed for the nominal value of R_F to be 1 kΩ in gains other than +1 V/V. This value of R_F = 1 kΩ gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. This value also loads the amplifier. For example, in a gain of 2 with $R_F = R_G$ = 1 kΩ, R_G to ground, and V_{OUT} = 4 V, 2 mA of current flows through the feedback path to ground. In s gain of +1, R_G is open and no current flows to ground. In low-power applications, reducing this current by increasing the gain-setting resistors values is desirable. Using larger value gain resistors has two primary side effects (other than lower power) because of the interaction with parasitic circuit capacitance:

- Lowers the bandwidth
- Lowers the phase margin
  - Causes peaking in the frequency response
  - Also causes overshoot and ringing in the pulse response

Feature Description (continued)

Figure 53 shows the small-signal frequency response for a noninverting gain of 2 with R_F and R_G equal to 1 kΩ, 10 kΩ, and 100 kΩ. The test was done with R_L = 1 kΩ. Lower values can reduce the peaking because of loading effects of R_L, but higher values do not have a significant effect.

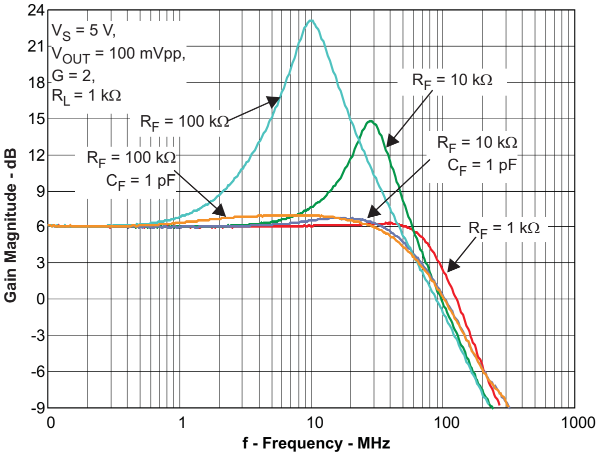


Figure 53. Frequency Response With Various Gain-Setting Resistor Values

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in the frequency response is synonymous with overshoot and ringing in pulse response). Adding 1-pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. Figure 54 shows the test circuit used.

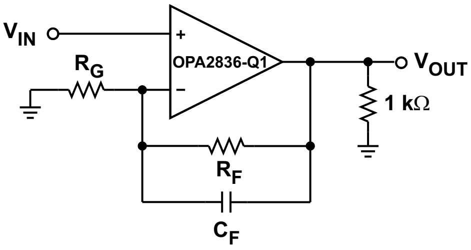


Figure 54. G = 2 Test Circuit for Various Gain-Setting Resistor Values

8.3.4 Driving Capacitive Loads

The OPA2836-Q1 can drive up to a nominal capacitive load of 2.2 pF on the output with no special consideration. When driving capacitive loads greater than this load, using a small resister (R_O) in series with the output as close to the device as possible is recommended. Without R_O, the capacitance on the output interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that reduces the phase margin. This scenario causes peaking in the frequency response and overshoot and ringing in the pulse responses. Interaction with other parasitic elements can lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop-gain path and restores the phase margin; however, the bandwidth is also limited.

Feature Description (continued)

Figure 55 shows the test circuit and Figure 42 illustrates the recommended values of R_O versus capacitive loads, C_L. See Figure 39 for frequency responses with various values.

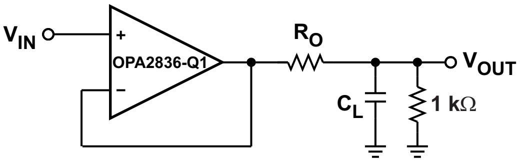


Figure 55. R_O versus C_L Test Circuit

8.4 Device Functional Modes

8.4.1 Split-Supply Operation (±1.25 V to ±2.75 V)

To facilitate testing with common lab equipment, the OPA2836-Q1 EVM (see the *OPA835DBV, OPA836DBV EVM*, SLOU314) is built to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference inputs and outputs to ground.

Figure 56 shows a simple noninverting configuration analogous to Figure 51 with a ±2.5-V supply and V_{REF} equal to ground. The input and output swing symmetrically around ground. Split-supply operation is preferred because of the ease of use in systems where signals swing around ground, but two supply rails still must be generated.

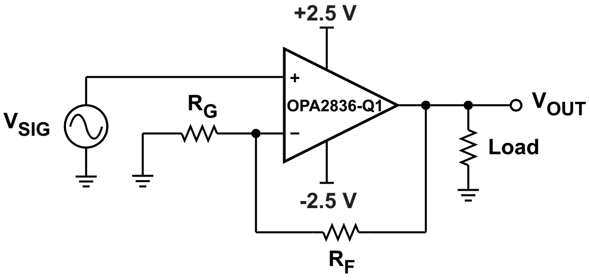


Figure 56. Split-Supply Operation

Device Functional Modes (continued)

8.4.2 Single-Supply Operation (2.5 V to 5.5 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the power supply. The OPA2836-Q1 is designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single supply, level shift all voltages by half the difference between the power-supply rails. For example, changing from a ±2.5-V split supply to a 5-V single supply is shown conceptually in Figure 57.

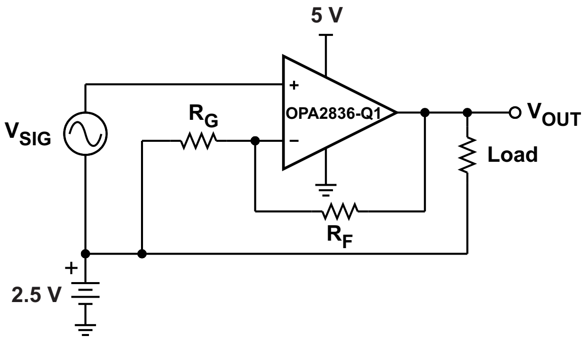


Figure 57. Single Supply Concept

A more practical circuit has a prior amplifier or another circuit to provide the bias voltage for the input with the output providing the bias for the next stage.

Figure 58 shows a typical noninverting amplifier situation. With a 5-V single supply, a mid-supply reference generator is needed to bias the negative side through R_G. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example, if a gain of 2 is required and R_F = 1 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 499 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise.

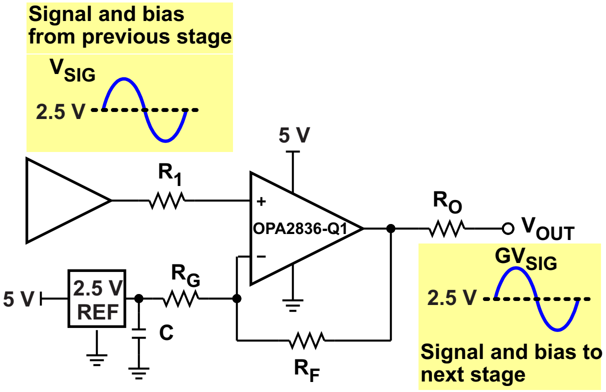


Figure 58. Noninverting Single Supply With Reference

Device Functional Modes (continued)

Figure 59 shows a similar noninverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G’ and R_G” form a resistor divider from the 5-V supply and are used to bias the negative side with the parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G’ in parallel with R_G” (R_1= R_F || R_G’ || R_G”). For example, if a gain of 2 is required and R_F = 1 kΩ, selecting R_G’ = R_G” = 2 kΩ gives an equivalent parallel sum of 1 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is then set to 499 Ω for bias current cancellation, which can be lower cost compared to Figure 59 but requires extra current in the resistor divider.

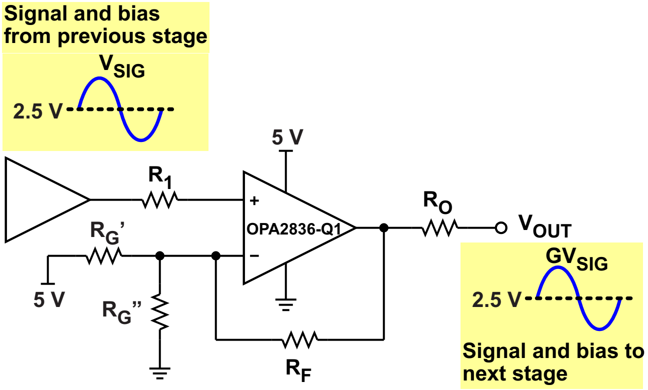


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Figure 59. Noninverting Single Supply With Resistors

Figure 60 shows a typical inverting amplifier situation. With a 5-V single supply, a mid-supply reference generator is needed to bias the positive side via R_1. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example, if a gain of –2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain and R_1 = 332 Ω for bias-current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise into the operational amplifier.

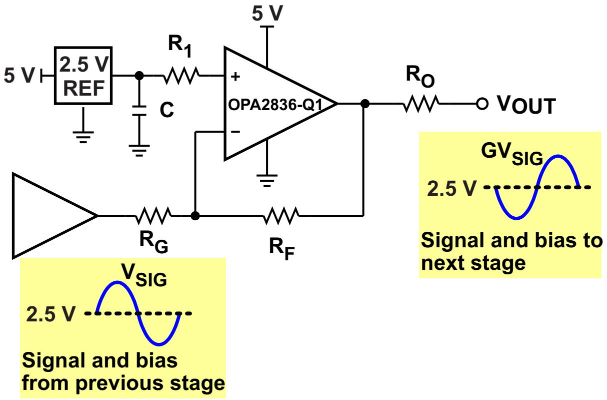

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Figure 60. Inverting Single Supply With Reference

Device Functional Modes (continued)

Figure 61 shows a similar inverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5-V supply and are used to bias the positive side. To cancel the voltage offset that is otherwise caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C must be added to limit coupling of noise into the positive input. For example, if a gain of –2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain. $R_1 = R_2$ = 665 Ω for mid-supply voltage bias and for operational amplifier input bias current cancellation. A good value for C is 0.1 µF and can be a lower cost compared to Figure 61, but requires extra current in the resistor divider.

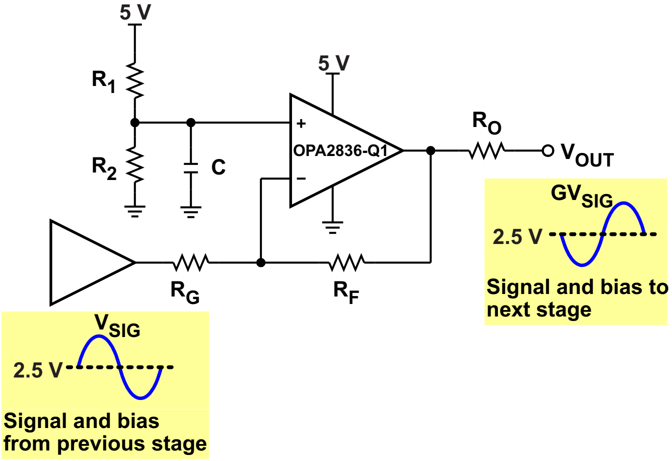


Figure 61. Inverting Single Supply With Resistors

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Noninverting Amplifier

The OPA2836-Q1 can be used as a noninverting amplifier with a signal input to the noninverting input, V_{IN+} . A basic block diagram of the circuit is illustrated in Figure 51.

If $V_{IN} = V_{REF} + V_{SIG}$, then the output of the amplifier can be calculated according to Equation 1.

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \tag{1}$$

The signal gain of the circuit is set by $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA2836-Q1 is designed for the nominal value of R_F to be 1 kΩ in gains other than +1. This value gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 1 kΩ must be used as a default unless other design goals require changing to other values. All test circuits used to collect data for this document have R_F = 1 kΩ for all gains other than +1. Gain of +1 is a special case where R_F is shorted and R_G is left open.

9.1.2 Inverting Amplifier

The OPA2836-Q1 can be used as an inverting amplifier with a signal input to the inverting input, V_{IN-} , through the gain setting resistor R_G. A basic block diagram of the circuit is illustrated in Figure 52.

If $V_{IN} = V_{REF} + V_{SIG}$, then the output of the amplifier may be calculated according to Equation 2.

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \tag{2}$$

The signal gain of the circuit is set by: $G = \frac{-R_F}{R_G}$, and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F must be 1 kΩ for inverting gains.

9.1.3 Instrumentation Amplifier

Figure 62 is an instrumentation amplifier that combines the high input impedance of the differential-to-differential amplifier circuit and the common-mode rejection of the differential-to-single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required (such as taps from a differential line or in cases where the signal source has a high output impedance).

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then the output of the amplifier can be calculated according to Equation 3.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \tag{3}$$

Application Information (continued)

The signal gain of the circuit is set by $G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$. V_{CM} is rejected and V_{REF} provides a level shift around which the output signal swings. The single-ended output signal is in-phase with the differential input signal.

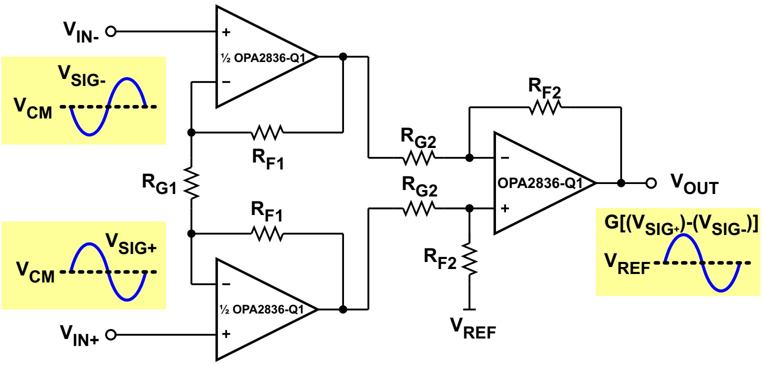


Figure 62. Instrumentation Amplifier

Integrated solutions are available, but the OPA2836-Q1 provides a much lower-power, high-frequency solution. For best CMRR performance, resistors must be matched. Given that CMRR ≈ the resistor tolerance, a 0.1% tolerance provides apprximately 60-dB CMRR.

9.1.4 Attenuators

The noninverting circuit of Figure 51 has a minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier can be set for a gain of 1 by shorting V_{OUT} to V_{IN-} and removing R_G. Because the operational amplifier input has high input impedance, the attenuation is set by the resistor divider.

The inverting circuit of Figure 52 can be used as an attenuator by making R_G larger than R_F. The attenuation is simply the resistor ratio. For example, a 10:1 attenuator can be implemented with R_F = 1 kΩ and R_G = 10 kΩ.

9.1.5 Single-Ended-to-Differential Amplifier

Figure 63 illustrates an amplifier circuit that is used to convert single-ended signals to differential and that provides gain and level shifting. This circuit can be used for converting signals to differential in applications (such as line drivers for Cat5 cabling or for driving differential-input SAR and ΔΣ ADCs).

With $V_{IN} = V_{REF} + V_{SIG}$, the output of the amplifier can be calculated according to Equation 4.

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and} \quad V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \tag{4}$$

The differential-signal gain of the circuit is 2 × G, and V_{REF} provides a reference around which the output signal swings. The differential output signal is in-phase with the single-ended input signal.

Application Information (continued)

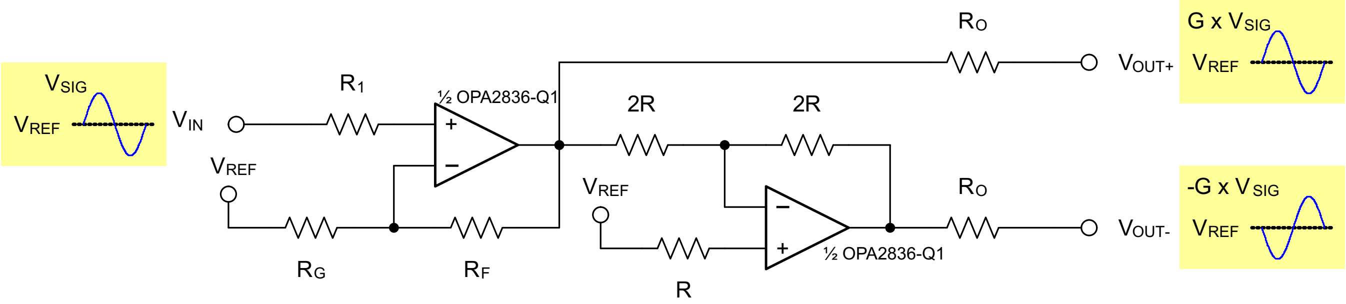


Figure 63. Single-Ended-to-Differential Amplifier

Line termination on the output can be accomplished with resistors R_O. The differential input impedance of the circuit is 2 × R_O. For example, if a 100-Ω Cat5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with R_F = 0 Ω (short), R_G = open, 2R = 1 kΩ, R1 = 0 Ω, R = 499 Ω to balance the input bias currents, and R_O = 49.9 Ω for output line termination. This configuration is shown in Figure 64.

For driving a differential-input ADC, the situation is similar but the output resistors (R_O) are typically chosen along with a capacitor across the ADC input for optimum filtering and settling-time performance.

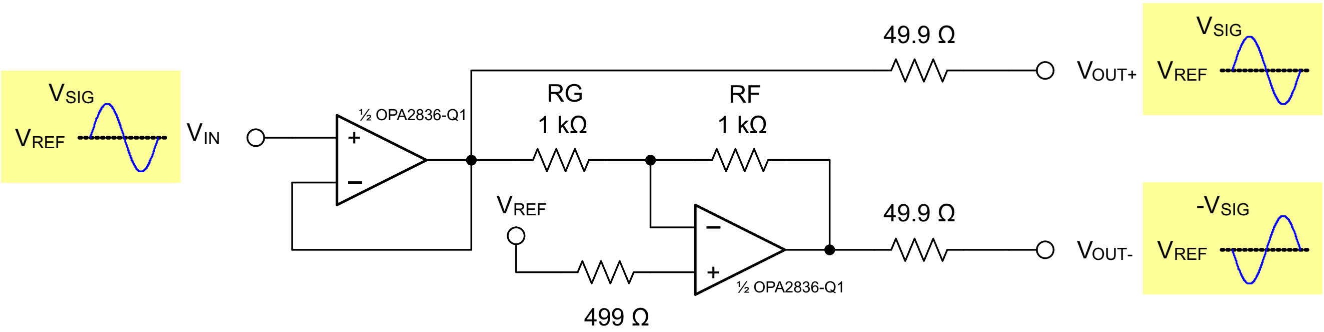


Figure 64. Cat5 Line Driver With Gain = 2 V/V (6 dB)

9.1.6 Differential-to-Signal-Ended Amplifier

Figure 65 illustrates a differential amplifier that converts differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications such as a line receiver for converting a differential signal from a Cat5 cable to single ended.

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then the output of the amplifier can be calculated according to Equation 5.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_F}{R_G} \right) + V_{REF} \tag{5}$$

The signal gain of the circuit is set by $G = \frac{R_F}{R_G}$. V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single-ended output signal is in-phase with the differential input signal.

Application Information (continued)

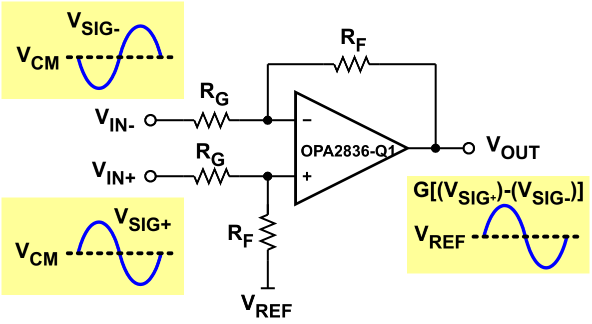


Figure 65. Differential to Single Ended Amplifier

Line termination can be accomplished with a resistor shunt across the input. The differential input impedance of the circuit is the resistor value in parallel with the amplifier circuit. For low-gain and low-line impedance, the resistor value to add is approximately the impedance of the line. For example, if a 100-Ω Cat5 cable is used with a gain of 1 amplifier and $R_F = R_G = 1\ k\Omega$, adding a 100-Ω shunt across the input gives a differential impedance of 98 Ω that is adequate for most applications.

For best CMRR performance, resistors must be matched. A rule of thumb is CMRR ≈ the resistor tolerance; so a 0.1% tolerance provides approximately 60-dB CMRR.

9.1.7 Differential-to-Differential Amplifier

Figure 66 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is often used in differential line driver applications where the signal source is a high-impedance driver (for example, a differential DAC) that must drive a line.

If $V_{IN\pm} = V_{CM} + V_{SIG\pm}$, then the output of the amplifier can be calculated according to Equation 6.

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \tag{6}$$

The signal gain of the circuit is set by $G = 1 + \frac{2R_F}{R_G}$, and V_{CM} passes with unity gain. The amplifier in essence combines two noninverting amplifiers into one differential amplifier with the R_G resistor shared, which makes R_G effectively half the value when calculating the gain. The output signals are in-phase with the input signals.

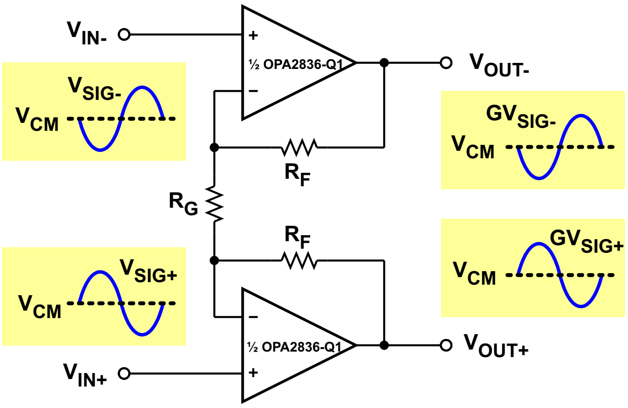


Figure 66. Differential to Differential Amplifier

Application Information (continued)

9.1.8 Pulse Application With Single-Supply

For pulsed applications, where the signal is at ground and pulses to some positive or negative voltage, the circuit bias-voltage considerations are different than with a signal that swings symmetrical about a reference point. Figure 67 shows a pulsed situation where the signal is at ground (0 V) and pulses to a positive value.

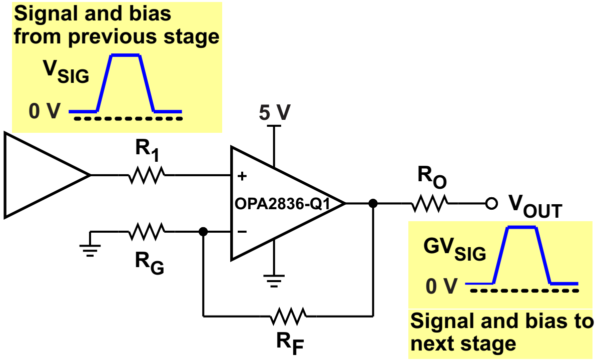


Figure 67. Noninverting Single Supply With Pulse

If the input signal pulses negatively from ground, an inverting amplifier is more appropriate, as shown in Figure 68. A key consideration in both noninverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier; because the V_{ICR} of the OPA2836-Q1 includes the negative supply rail, the OPA2836-Q1 lends itself to this application.

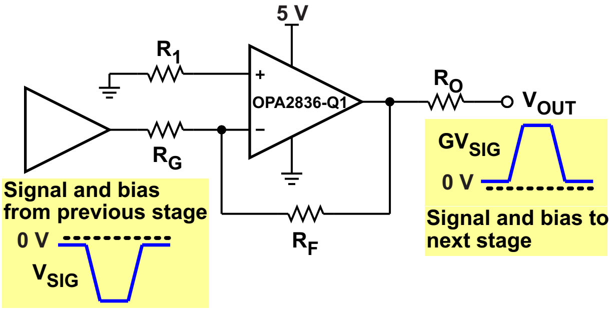


Figure 68. Inverting Single Supply With Pulse

9.1.9 ADC Driver Performance

The OPA2836-Q1 provides excellent performance when driving high-performance, delta-sigma (ΔΣ), and successive approximation register (SAR) ADCs in low-power audio and industrial applications.

To show achievable performance, the OPA2836-Q1 is tested as the drive amplifier for the ADS8326. The ADS8326 is a 16-bit, micro power, SAR ADC with pseudo-differential inputs and sample rates up to 250 kSPS. The ADS8326 offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA2836-Q1 devices an ideal solution for portable and battery-operated systems, for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

Application Information (continued)

The circuit shown in Figure 69 is used to test the performance. Figure 70 is the FFT plot showing the spectral performance with a 10-kHz input frequency, and Table 3 shows the tabulated ac analysis results.

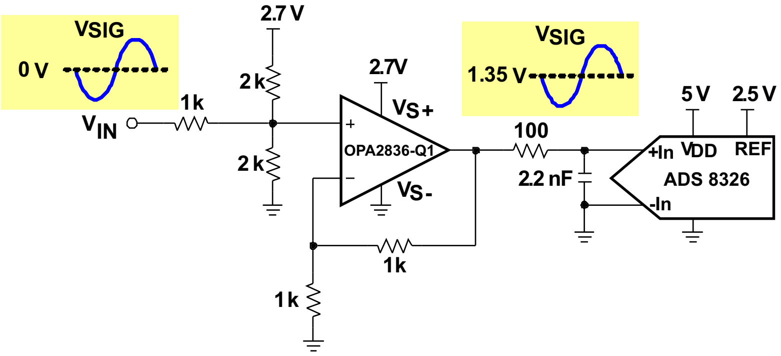


Figure 69. OPA2836-Q1 and ADS8326 Test Circuit

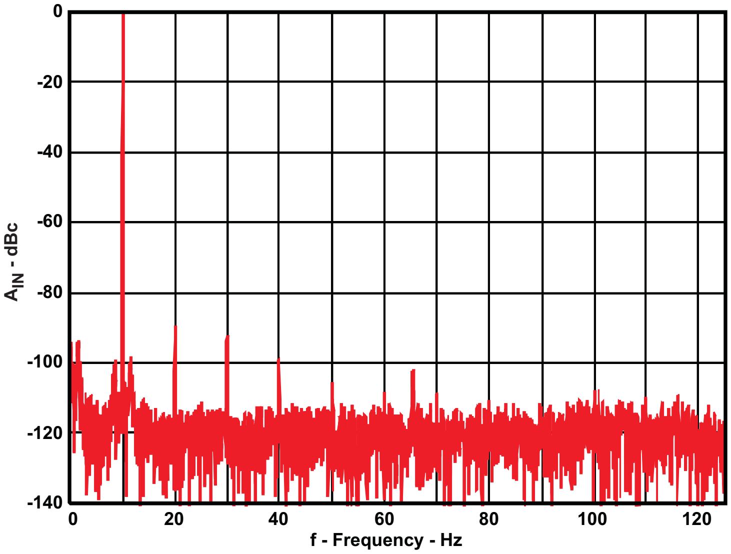


Figure 70. ADS8326 and OPA2836-Q1 10-kHz FFT

Table 3. AC Analysis

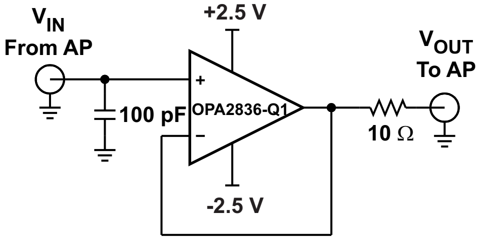
TONE (kHz)	SIGNAL (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
10	–0.85	83.3	–86.6	81.65	88.9

9.2 Typical Applications

9.2.1 Audio-Frequency Performance

The OPA2836-Q1 provides excellent audio performance with very low quiescent power. To show performance in the audio band, a 2700 series audio analyzer from Audio Precision is used to test THD+N and FFT at 1-V_{RMS} output voltage.

Figure 71 shows the test circuit used for the audio-frequency performance application.



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The 100-pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

Figure 71. OPA2836-Q1 Audio Precision Analyzer Test Circuit

9.2.1.1 Design Requirements

Design a low distortion, single-ended input to single-ended output audio amplifier using the OPA2836-Q1. The 2700 series audio analyzer from Audio Precision is used as the signal source and also as the measurement system.

Table 4. Design Requirements

CONFIGURATION	INPUT EXCITATION	PERFORMANCE TARGET	R_{Load}
OPA2836-Q1 unity-gain configuration	1-kHz tone frequency	> 110 dBc SFDR	300 Ω and 100 kΩ

9.2.1.2 Detailed Design Procedure

The OPA2836-Q1 is tested in this application in a unity-gain buffer configuration. A buffer configuration is chosen because this configuration maximizes the loop gain of the amplifier configuration. At higher closed-loop gains, the loop gain of the circuit reduces, resulting in degraded harmonic distortion. The relationship between distortion and closed-loop gain at a fixed input frequency is illustrated in Figure 35 in the *Typical Characteristics* section. The test was performed under varying output load conditions using a resistive load of 300 Ω and 100 kΩ. Figure 33 illustrates the distortion performance of the amplifier versus output resistive load. Output loading, output swing, and closed-loop gain play a key role in determining the distortion performance of the amplifier.

NOTE

The 100-pF capacitor to ground on the input helped to decouple noise pickup in the lab and improved noise performance.

The Audio Precision was configured as a single-ended output in this application circuit. In applications where a differential output is available, the OPA2836-Q1 device can be configured as a differential-to-single-ended amplifier; see Figure 65. Power-supply bypassing is critical in order to reject noise from the power supplies. A 2.2-µF power-supply decoupling capacitor must be placed within 2 inches of the device and can be shared with other operational amplifiers on the same board. A 0.1-µF power supply decoupling capacitor must be placed as close to the power supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies. A 0.1-µF capacitor placed directly between the supplies is also beneficial for improving system noise performance. If the output load is very heavy, in the order of 16 Ω to 32 Ω, performance of the amplifier can begin to degrade. In order to drive such heavy loads, both channels of the OPA2836-Q1 device can be paralleled with the outputs isolated with 1-Ω resistors to reduce the loading effects.

9.2.1.3 Application Curves

A 10-Ω series resistor can be inserted between the capacitor and the noninverting pin to isolate the capacitance.

Figure 72 shows the THD+N performance with 100-kΩ and 300-Ω loads, with A-weighting and with no weighting. Both loads show similar performance. With no weighting, the THD+N performance is dominated by the noise; whereas, A-weighting provides filtering that improves the noise.

Figure 73 and Figure 74 show FFT outputs with a 1-kHz tone and 100-kΩ and 300-Ω loads. To show relative performance of the device versus the test set, one channel has the OPA2836-Q1 in-line between generator output and analyzer input and the other channel is in *Gen Mon* loopback mode that internally connects the signal generator to the analyzer input. With a 100-kΩ load, Figure 73, the curves are basically indistinguishable from each other except for noise, meaning that the OPA2836-Q1 cannot be directly measured. With a 300-Ω load, Figure 74, the main difference between the curves is that the OPA2836-Q1 shows slightly higher even-order harmonics, but odd-order harmonics are masked by the test-set performance.

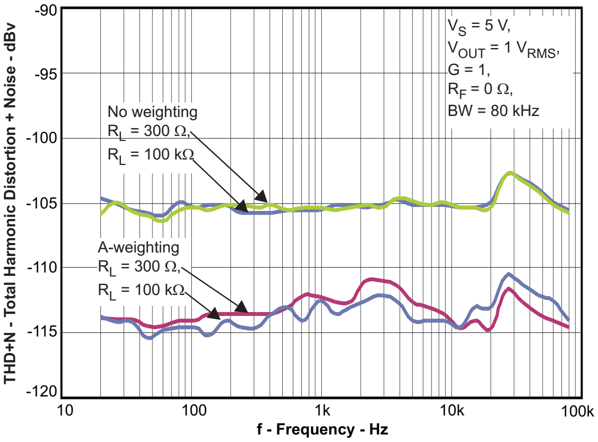

Figure 72. OPA2836-Q1 1 V_{RMS}, 20-Hz to 80-kHz THD+N

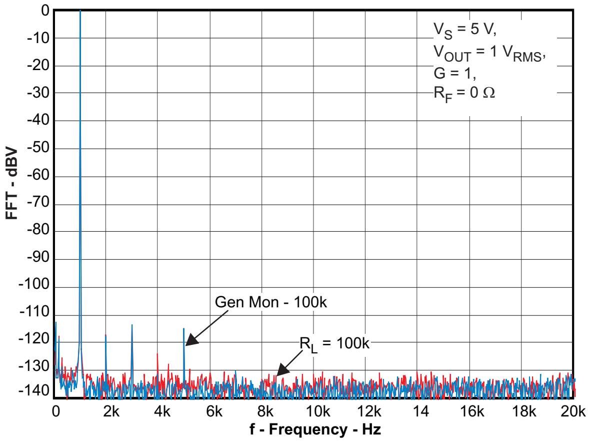

Figure 73. OPA2836-Q1 and AP Gen Mon 10-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 100 kΩ

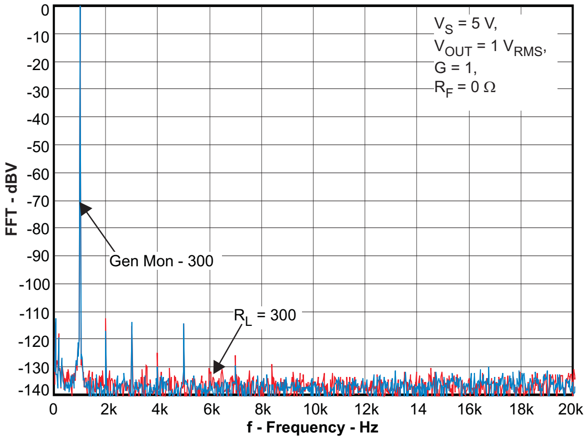

Figure 74. OPA2836-Q1 and AP Gen Mon 10-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 300 Ω

9.2.2 Active Filters

The OPA2836-Q1 can be used to design active filters. Figure 75 and Figure 76 show MFB and Sallen-Key circuits designed using the WEBENCH® filter designer to implement second-order low-pass Butterworth filter circuits. Figure 77 shows the frequency response.

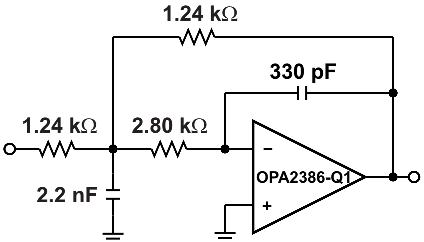

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Figure 75. MFB 100-kHz Second Order Low-Pass Butterworth Filter Circuit

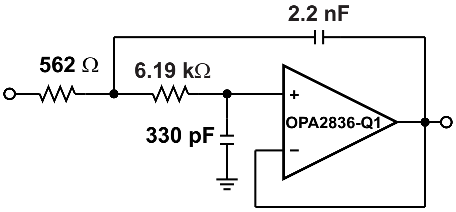

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Figure 76. Sallen-Key 100-kHz Second Order Low-Pass Butterworth Filter Circuit

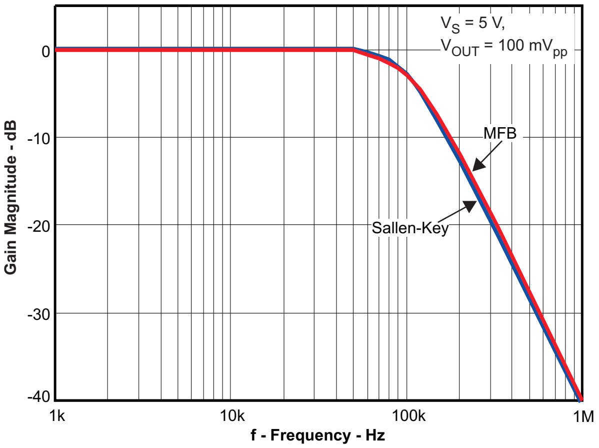


Figure 77. MFB and Sallen-Key Second Order Low-Pass Butterworth Filter Response

MFB and Sallen-Key filter circuits offer similar performance. The main difference is the MFB uses an inverting amplifier in the pass-band and the Sallen-Key uses an noninverting amplifier. The primary advantage for each is the Sallen-Key in unity gain has no resistor gain-error term, and thus no sensitivity to gain error, whereas the MFB has inherently better attenuation properties beyond the bandwidth of the operational amplifier.

10 Power Supply Recommendations

The OPA2836-Q1 is principally intended to work in a supply range of 2.7 V to 5 V. Supply voltage tolerances are supported with the specified operating range of 2.5 V (7% on a 2.7-V supply) and 5.5 V (10% on a 5-V supply). Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. Often a larger capacitor (2.2 µF, typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance.

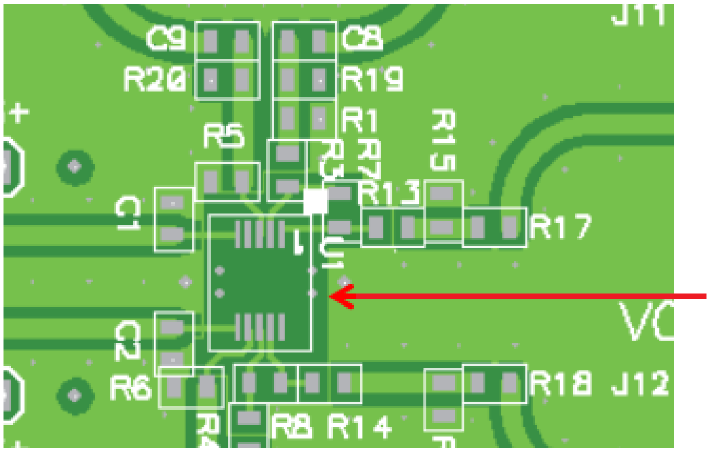
11 Layout

11.1 Layout Guidelines

The *OPA835DBV, OPA836DBV EVM* (SLOU314) must be used as a reference when designing the circuit board. Follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

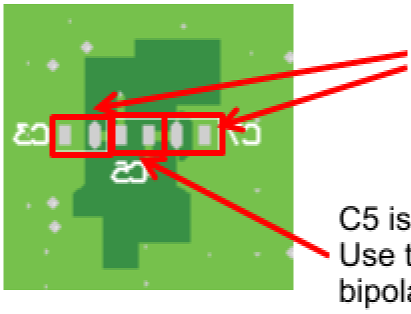
1. Signal routing must be direct and as short as possible into an out of the operational amplifier.
2. The feedback path must be short and direct avoiding vias if possible especially with G = +1.
3. Ground or power planes must be removed from directly under the negative input and output pins of the amplifier.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See Figure 17 for recommended values given expected capacitive load of design.
5. A 2.2-µF power-supply decoupling capacitor must be placed within 2 inches of the device and can be shared with other operational amplifiers. For spit supply, a capacitor is required for both supplies.
6. A 0.1-µF power-supply decoupling capacitor must be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.

11.2 Layout Example



Dark green areas indicate regions of the PCB where the underlying Ground and Power Planes have been removed in order to minimize parasitic capacitance on the sensitive input and output nodes.

Figure 78. Top Layer



C3 and C7 are 0.1-µF bypass capacitors placed directly underneath the device power supply pins.

C5 is a bypass capacitor between the supply pins. Use this when configuring the amplifier with bipolar supplies to improve HD2 performance.

Figure 79. Bottom Layer

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

WEBENCH® filter designer

12.1.2 関連資料

関連資料については、以下を参照してください。

- *『OPA835DBV、OPA836DBV EVM』* (SLOU314)
- *『ADS8326 16ビット、高速、2.7V～5.5V、マイクロパワー・サンプリングA/Dコンバータ』* (SBAS343)

12.2 関連リンク

表 5 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA2836-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.5 商標

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2836QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2836Q
OPA2836QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2836Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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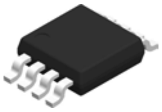
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2836-Q1 :

- Catalog : OPA2836

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

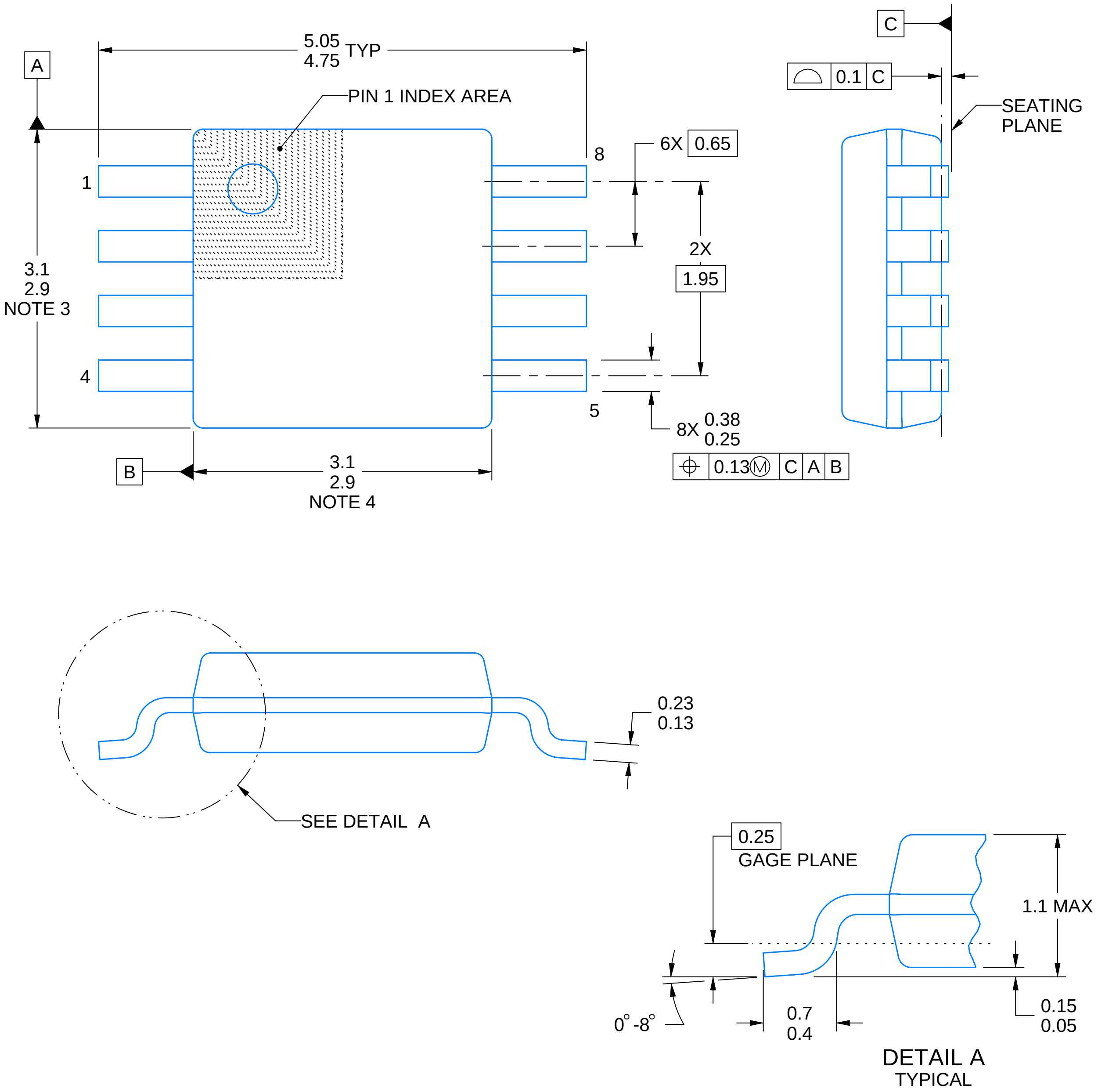


PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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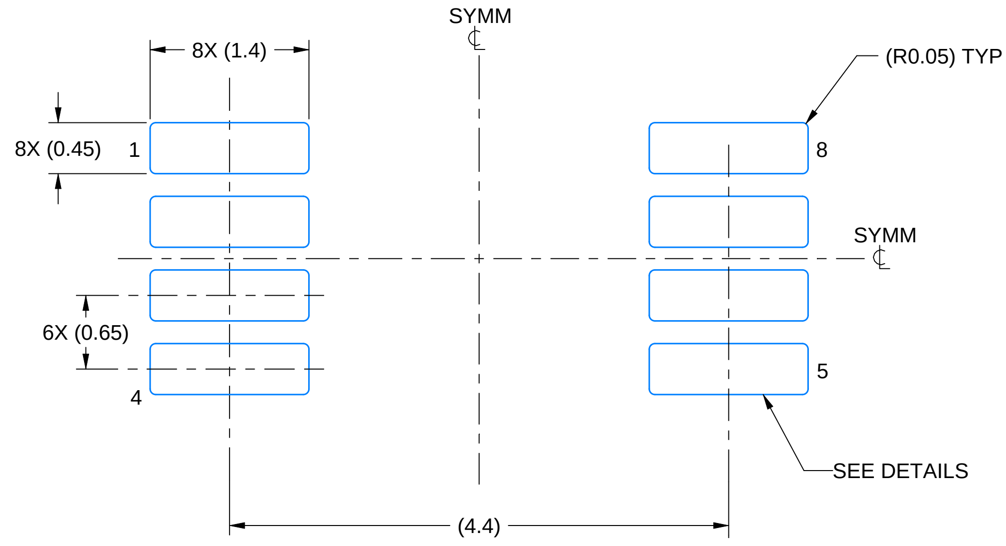
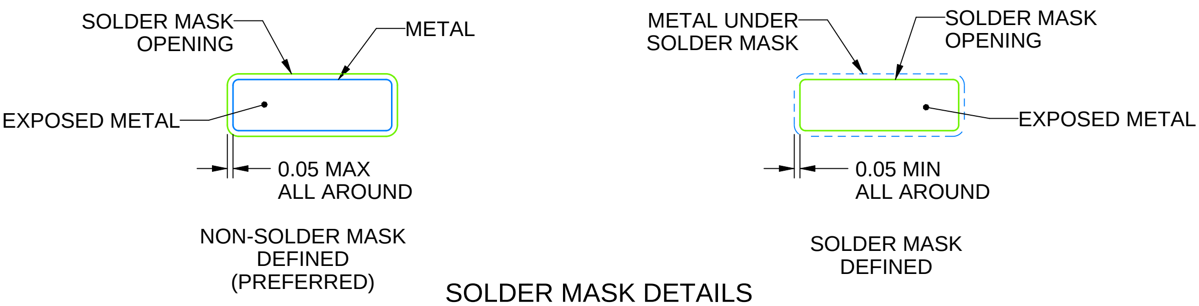
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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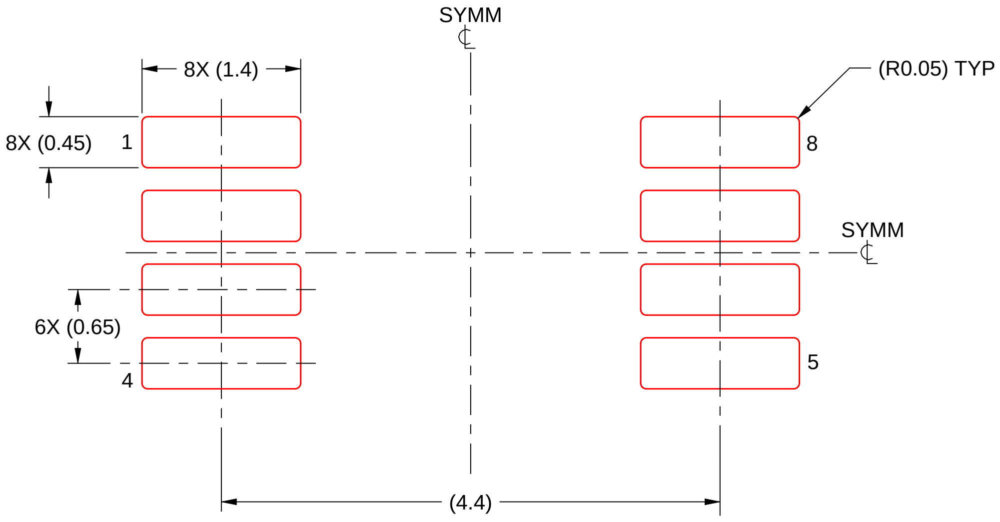
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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