



# OPA2810 デュアル・チャネル、27V、レール・ツー・レール入出力、 FET入力のおペアンプ

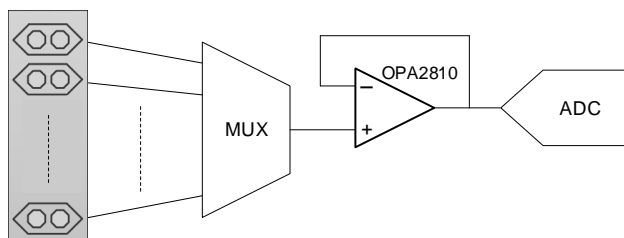
## 1 特長

- ゲイン帯域幅積: 70MHz
- 小信号帯域幅: 105MHz
- スルーレート: 192V/μs
- 広い電源電圧範囲: 4.75V~27V
- 低ノイズ
  - 入力電圧ノイズ:  $6\text{nV}/\sqrt{\text{Hz}}$  ( $f=500\text{kHz}$ )
  - 入力電流ノイズ:  $5\text{fA}/\sqrt{\text{Hz}}$  ( $f=10\text{kHz}$ )
- レール・ツー・レール入出力
  - FET入力段: 2pAの入力バイアス電流(標準値)
  - 高リニア出力電流: 75mA
- 入力オフセット:  $\pm 1.5\text{mV}$  (最大値)
- オフセット・ドリフト係数:  $\pm 2\mu\text{V}/^\circ\text{C}$  (標準値)
- 低消費電流: 3.6mA/チャネル
- 拡張温度範囲で動作:  $-40^\circ\text{C} \sim +125^\circ\text{C}$

## 2 アプリケーション

- 広帯域フォトダイオード・トランスインピーダンス・アンプ
- High-Zフロントエンド
- インピーダンス測定
- 電力分析
- マルチチャネル・センサ・インターフェイス
- レベル・シフト/バッファリング
- オプトエレクトロニクス・ドライバ

### マルチチャネル・センサ・インターフェイス



## 3 概要

OPA2810は、入力バイアス電流の小さい、デュアル・チャネル、FET入力の電圧帰還オペアンプです。ユニティ・ゲイン安定で、105MHzの小信号ユニティ・ゲイン帯域幅を提供し、チャネルあたり3.6mA (標準値)の低い静止電流( $I_Q$ )で優れたDC精度と動的AC性能を実現します。テキサス・インスツルメンツ独自の高速SiGe BiCMOSプロセスで製造されており、静止電流が同等である他のFET入力アンプに比べて大幅に性能が向上しています。70MHzのゲイン帯域幅積(GBWP)、192V/μsのスルー・レート、 $6\text{nV}/\sqrt{\text{Hz}}$ の低い電圧ノイズにより、幅広い高忠実度データ収集/信号処理装置に適しています。

OPA2810は4.75V~27Vの広い電源電圧範囲で動作し、レール・ツー・レール入出力を特長としています。また、75mAのリニア出力電流を提供できることから、オプトエレクトロニクス部品およびアナログ/デジタル・コンバータ(ADC)入力の駆動や、重負荷へのDAC出力のバッファリングにも最適です。

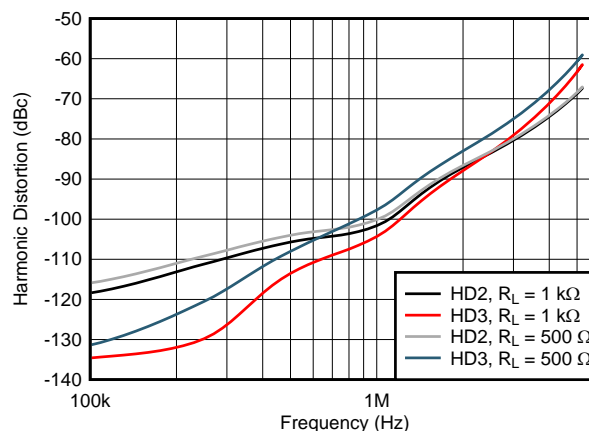
OPA2810は8ピンのSOIC、SOT23、VSSOPパッケージで供給され、拡張産業用温度範囲の $-40^\circ\text{C} \sim +125^\circ\text{C}$ で動作が規定されています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
OPA2810	SOIC (8)	4.90mm×3.91mm
	SOT-23 (8)	2.90mm×1.60mm
	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

### 高調波歪みと周波数との関係



D048



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## 4 改訂履歴

### Revision A (June 2018) から Revision B に変更

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•	ドキュメントにD (SOIC)パッケージを 追加 .....	1
•	Changed value of minimum linear output drive at $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ in 10 V, 24 V and 5 V Electrical Characteristics tables .....	6
•	Changed test condition for linear output drive at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ in 10 V, 24 V and 5 V Electrical Characteristics tables. ....	6
•	Deleted specification for minimum output short-circuit current in 10 V, 24 V and 5 V Electrical Characteristics tables.....	6
•	Deleted '±' sign from the test condition for PSRR at $25^\circ\text{C}$ in 10 V, 24 V and 5 V Electrical Characteristics tables.....	7
•	Changed footnote for PSRR in 10 V, 24 V and 5 V Electrical Characteristics tables. ....	7
•	Added $V_{CM} = 0.5\text{ V}$ to the test condition for PSRR at $25^\circ\text{C}$ in 5 V Electrical Characteristics table. ....	12
•	Changed changed test condition for open-loop voltage gain in auxiliary CMOS input stage section in 5 V Electrical Characteristics table. ....	13

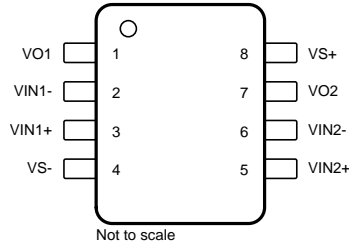
### 2017年8月発行のものから更新

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•	デバイスのステータスを「事前情報」から「量産データ」に 変更 .....	1
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## 5 Pin Configuration and Functions

**D, DCN, and DGK Packages  
8-Pin SOIC, SOT-23, and VSSOP  
Top View**



**Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VO1	1	O	Amplifier 1 output pin
VIN1-	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VS-	4	P	Negative power supply pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VIN2-	6	I	Amplifier 2 inverting input pin
VO2	7	O	Amplifier 2 output pin
VS+	8	P	Positive power supply pin

(1) I = input, O = output, and P = power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_S$	Supply voltage (total bipolar supplies) <sup>(2)</sup>			±14	V
$V_{IN}$	Input voltage		$V_{S-} - 0.5$	$V_{S+} + 0.5$	V
$V_{IN,Diff}$	Differential input voltage <sup>(3)</sup>			±7	V
$I_I$	Continuous input current			±10	mA
$I_O$	Continuous output current <sup>(4)</sup>	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		±40	mA
		$T_A = 125^{\circ}\text{C}$		±12	mA
$P_D$	Continuous power dissipation		See <a href="#">Thermal Information</a>		
$T_J$	Junction temperature			150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature		-65	125	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2)  $V_S$  is the total supply voltage given by  $V_S = V_{S+} - V_{S-}$ .
- (3) Equal to the lower of ±7 V or total supply voltage.
- (4) Long-term continuous output current for electromigration limits.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_S$	Total supply voltage	4.75		27	V
$T_A$	Ambient temperature	-40	25	125	$^{\circ}\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		OPA2810			UNIT
		D (SOIC)	DCN (SOT-23)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.9	130.9	177.2	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	86.6	64.6	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	69.4	42.3	99.0	$^{\circ}\text{C}/\text{W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	13.5	25.9	9.7	$^{\circ}\text{C}/\text{W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	68.1	42.3	97.3	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	$^{\circ}\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics: 10 V

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
<b>AC PERFORMANCE</b>							
SSBW	Small-signal bandwidth	$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\ \Omega$		75		MHz	C
		$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\ \Omega$ , $C_L = 33\text{ pF}$		105		MHz	C
		$G = -1$ , $V_o = 20\text{ mV}_{PP}$		50		MHz	C
		$G = 2$ , $V_o = 20\text{ mV}_{PP}$		49		MHz	C
		$G = 5$ , $V_o = 20\text{ mV}_{PP}$		15		MHz	C
LSBW	Large-signal bandwidth	$G = 2$ , $V_o = 2\text{ V}_{PP}$		38		MHz	C
		$G = 2$ , $V_o = 4\text{ V}_{PP}$		26		MHz	C
GBWP	Gain-bandwidth product	$G = 11$ , $V_o = 20\text{ mV}_{PP}$		70		MHz	C
	Bandwidth for 0.1dB flatness	$G = 2$ , $V_o = 20\text{ mV}_{PP}$		13		MHz	C
SR	Slew rate (20%-80%) <sup>(3)</sup>	$G = 2$ , $V_o = -2\text{ V}$ to $2\text{ V}$ step		192		V/ $\mu\text{s}$	C
		$G = -1$ , $V_o = -2\text{ V}$ to $2\text{ V}$ step		187		V/ $\mu\text{s}$	C
		$G = 2$ , $V_o = -4.5\text{ V}$ to $3.5\text{ V}$ step		193		V/ $\mu\text{s}$	C
	Rise time	$V_o = 200\text{-mV}$ step		4		ns	C
	Fall time	$V_o = 200\text{-mV}$ step		5		ns	C
	Settling time to 0.1%	$G = 2$ , $V_o = 2\text{-V}$ step		73		ns	C
		$G = 2$ , $V_o = 8\text{-V}$ step		97		ns	C
		$G = -1$ , $V_o = 8\text{-V}$ step		96		ns	C
	Settling time to 0.001%	$G = 2$ , $V_o = 2\text{-V}$ step		374		ns	C
		$G = 2$ , $V_o = 8\text{-V}$ step		213		ns	C
		$G = -1$ , $V_o = 8\text{-V}$ step		163		ns	C
	Overshoot/undershoot	$G = +1$ , $R_F = 0\ \Omega$ , $V_o = 200\text{ mV}_{PP}$		9/10		%	C
		$G = +1$ , $R_F = 0\ \Omega$ , $V_o = 2\text{ V}_{PP}$		4/5		%	C
	Input overdrive recovery	$G = 1$ , $R_F = 0\ \Omega$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input (see <a href="#">Figure 14</a> )		44		ns	C
	Output overdrive recovery	$G = -1$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input (see <a href="#">Figure 15</a> )		55		ns	C
HD2	Second-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-118		dBc	C
		$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 8\text{ V}_{PP}$		-101		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-99		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 8\text{ V}_{PP}$		-82		dBc	C
HD3	Third-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-134		dBc	C
		$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 8\text{ V}_{PP}$		-105		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-104		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 8\text{ V}_{PP}$		-92		dBc	C
$e_n$	Input-referred voltage noise	$f = 500\text{ kHz}$ , flatband		6		nV/ $\sqrt{\text{Hz}}$	C
		$f = 0.1\text{-}10\text{ Hz}$ integrated		0.42		$\mu\text{V}_{rms}$	C
$e_i$	Input-referred current noise	$f = 10\text{ kHz}$		5		fA/ $\sqrt{\text{Hz}}$	C
$z_o$	Close-loop output impedance	$f = 100\text{ kHz}$		0.007		$\Omega$	C

(1) For AC specifications,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$  and  $C_L = 4.7\text{ pF}$  (unless otherwise noted).

(2) Test levels (all values set by characterization and simulation): (A) 100% tested at  $25^\circ\text{C}$ , overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.

(3) Lower of the measured positive and negative slew rate.

**Electrical Characteristics: 10 V (continued)**

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
DC PERFORMANCE							
A <sub>OL</sub>	Open-loop voltage gain	f = DC, V <sub>O</sub> = ±2.5 V	108	120		dB	A
		T <sub>A</sub> = −40°C to +125°C	108				B
V <sub>OS</sub>	Input offset voltage	T <sub>A</sub> = 25°C		0.1	1.5	mV	A
		T <sub>A</sub> = −40°C to +85°C			2.4	mV	B
		T <sub>A</sub> = −40°C to +125°C			2.8	mV	B
	Input offset voltage drift	T = 25°C		1.5		μV/°C	B
		T <sub>A</sub> = −40°C to +125°C			13	μV/°C	B
	Input bias current	T <sub>A</sub> = 25°C		2	20	pA	A
		T <sub>A</sub> = −40°C to +85°C <sup>(4)</sup>		20	60	pA	B
		T <sub>A</sub> = −40°C to +125°C <sup>(4)</sup>		100	350	pA	B
	Input offset current	T <sub>A</sub> = 25°C		1	20	pA	A
		T <sub>A</sub> = −40°C to +85°C		5		pA	B
		T <sub>A</sub> = −40°C to +125°C		50		pA	B
CMRR	Common-mode rejection ratio	f = DC, T <sub>A</sub> = 25°C, V <sub>CM</sub> = −3 V to +1 V	85	100		dB	A
		T <sub>A</sub> = −40°C to +125°C	85			dB	B
INPUT							
	Allowable input differential voltage	See <a href="#">FIG 57</a>		±7		V	C
	Common-mode input impedance	In closed-loop configuration		12    2.5		GΩ  pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S+</sub> + 0.2	V <sub>S+</sub> + 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> + 0.2			V	B
	Most negative input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S−</sub> − 0.2	V <sub>S−</sub> − 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S−</sub> − 0.2			V	B
	Most positive input voltage for main-JFET stage	T = 25°C (see <a href="#">FIG 18</a> )	V <sub>S+</sub> − 2.9	V <sub>S+</sub> − 2.5		V	C
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> − 3			V	C
OUTPUT							
V <sub>OCRH</sub>	Output voltage range high	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S+</sub> − 0.18	V <sub>S+</sub> − 0.11		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>L</sub> = 667 Ω	V <sub>S+</sub> − 0.2			V	B
V <sub>OCRL</sub>	Output voltage range low	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.15	V <sub>S−</sub> + 0.08		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.2			V	B
I <sub>O(max)</sub>	Linear output drive (sourcing and sinking)	T <sub>A</sub> = 25°C, V <sub>O</sub> = 2.65 V, R <sub>L</sub> = 51 Ω, V <sub>OS</sub> < 2 mV	52	75		mA	A
		T <sub>A</sub> = −40°C to +125°C, V <sub>O</sub> = 1.4 V, V <sub>OS</sub> < 2 mV	28			mA	B
I <sub>SC</sub>	Output short-circuit current	T <sub>A</sub> = 25°C, T <sub>Delay</sub> = 5 ms		100		mA	B
C <sub>L</sub>	Capacitive load drive	< 1 dB peaking, R <sub>S</sub> = 0 Ω		35		pF	C

(4) Maximum bias current specification is set using  $\pm 5\sigma$  limits (corresponding to 0.58 DPPM) obtained using the statistical distribution from electrical characterization over temperature of a sample set of 70 units. Maximum specification is not specified by final automated test equipment (ATE) nor by QA sample testing.

(5) Change in input offset from its value when input is biased to midsupply.

## Electrical Characteristics: 10 V (continued)

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
POWER SUPPLY							
V <sub>S</sub>	Operating voltage	T <sub>A</sub> = 25°C	4.75		27	V	A
		T <sub>A</sub> = −40°C to +125°C	4.75		27	V	B
I <sub>Q</sub>	Quiescent current per channel	T <sub>A</sub> = 25°C	3.125	3.6	4.05	mA	A
		T <sub>A</sub> = −40°C to +125°C	2.9		4.4	mA	B
PSRR	Power supply rejection ratio	ΔV <sub>S</sub> = 2 V <sup>(6)</sup>	82	100		dB	A
		T <sub>A</sub> = −40°C to +125°C	82			dB	B
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product	V <sub>CM</sub> = (V <sub>S+</sub> ) − 1 V		35		MHz	C
	Open-loop voltage gain	V <sub>CM</sub> = (V <sub>S+</sub> ) − 1 V, f = DC, V <sub>o</sub> = 2 V to 4 V	80	100		dB	A
	Input-referred voltage noise	V <sub>CM</sub> = V <sub>S+</sub> − 1V, f = 1 MHz		21		nV/√Hz	C
	Input offset voltage	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, no-load			4	mV	A
		V <sub>CM</sub> = V <sub>S+</sub> − 0.5 V, no-load			4.8	mV	A
		V <sub>CM</sub> = V <sub>S+</sub> − 0.5 V, T <sub>A</sub> = −40°C to +125°C, no-load			6.4	mV	B
	Input bias current	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V		2	20	pA	A
		V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, T <sub>A</sub> = −40°C to +125°C		0.15	0.5	nA	B
	Common-mode rejection ratio	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V to V <sub>S+</sub> − 0.5 V		75		dB	B
	Power supply rejection ratio	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, ΔV <sub>S</sub> = ±2 V <sup>(6)</sup>		75		dB	B
CHANNEL MATCHING							
	Channel-to-channel GBWP mismatch	T <sub>A</sub> = 25°C		3		%	C
	Channel-to-channel crosstalk	f = 100 kHz		−93		dBc	C
	Input offset voltage mismatch	T <sub>A</sub> = 25°C		0.1	2.5	mV	A

(6) The supply voltages are  $V_{S+} = 5\text{ V} \pm 1\text{ V}$  and  $V_{S-} = -5\text{ V}$  for +PSRR, and  $V_{S+} = 5\text{ V}$  and  $V_{S-} = -5\text{ V} \pm 1\text{ V}$  for -PSRR.

## 6.6 Electrical Characteristics: 24 V

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
<b>AC PERFORMANCE</b>							
SSBW	Small-signal bandwidth	$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\ \Omega$		75		MHz	C
		$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\ \Omega$ , $C_L = 33\text{ pF}$		105		MHz	C
		$G = -1$ , $V_o = 20\text{ mV}_{PP}$		51		MHz	C
		$G = 2$ , $V_o = 20\text{ mV}_{PP}$		49		MHz	C
		$G = 5$ , $V_o = 20\text{ mV}_{PP}$		15		MHz	C
LSBW	Large-signal bandwidth	$G = 2$ , $V_o = 2\text{ V}_{PP}$		38		MHz	C
		$G = 2$ , $V_o = 10\text{ V}_{PP}$		14		MHz	C
GBWP	Gain-bandwidth product	$G = 11$ , $V_o = 20\text{ mV}_{PP}$		70		MHz	C
	Bandwidth for 0.1dB flatness	$G = 2$ , $V_o = 20\text{ mV}_{PP}$		12		MHz	C
SR	Slew rate (20%-80%) <sup>(3)</sup>	$G = 2$ , $V_o = -2\text{ V}$ to $2\text{ V}$ step		226		V/ $\mu\text{s}$	C
		$G = -1$ , $V_o = -2\text{ V}$ to $2\text{ V}$ step		218		V/ $\mu\text{s}$	C
		$G = 2$ , $V_o = -4.5\text{ V}$ to $3.5\text{ V}$ step		243		V/ $\mu\text{s}$	C
	Rise time	$V_o = 200\text{-mV}$ step		4		ns	C
	Fall time	$V_o = 200\text{-mV}$ step		5		ns	C
	Settling time to 0.1%	$G = 2$ , $V_o = 2\text{-V}$ step		72		ns	C
		$G = 2$ , $V_o = 10\text{-V}$ step		90		ns	C
		$G = -1$ , $V_o = 10\text{-V}$ step		89		ns	C
	Settling time to 0.001%	$G = 2$ , $V_o = 2\text{-V}$ step		370		ns	C
		$G = 2$ , $V_o = 10\text{-V}$ step		210		ns	C
		$G = -1$ , $V_o = 10\text{-V}$ step		150		ns	C
	Overshoot/undershoot	$G = 1$ , $R_F = 0\ \Omega$ , $V_o = 200\text{ mV}_{PP}$		7.5/9		%	C
		$G = 1$ , $R_F = 0\ \Omega$ , $V_o = 2\text{ V}_{PP}$		4/5		%	C
	Input overdrive recovery	$G = 1$ , $R_F = 0\ \Omega$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input (see <a href="#">31</a> )		66		ns	C
	Output overdrive recovery	$G = -1$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input (see <a href="#">32</a> )		30		ns	C
HD2	Second-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-123		dBc	C
		$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 10\text{ V}_{PP}$		-113		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-105		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 10\text{ V}_{PP}$		-92		dBc	C
HD3	Third-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-134		dBc	C
		$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 10\text{ V}_{PP}$		-130		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-103		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 10\text{ V}_{PP}$		-86		dBc	C
$e_n$	Input-referred voltage noise	$f = 500\text{ kHz}$ , flatband		6		nV/ $\sqrt{\text{Hz}}$	C
		$f = 0.1\text{-}10\text{ Hz}$ integrated		0.36		$\mu\text{V}_{rms}$	C
$e_i$	Input-referred current noise	$f = 10\text{ kHz}$		5		fA/ $\sqrt{\text{Hz}}$	C
$z_O$	Close-loop output impedance	$f = 100\text{ kHz}$		0.007		$\Omega$	C

(1) For AC specifications,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$  and  $C_L = 4.7\text{ pF}$  (unless otherwise noted).

(2) Test levels (all values set by characterization and simulation): (A) 100% tested at  $25^\circ\text{C}$ , overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.

(3) Lower of the measured positive and negative slew rate.



## Electrical Characteristics: 24 V (continued)

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
DC PERFORMANCE							
A <sub>OL</sub>	Open-loop voltage gain	f = DC, V <sub>O</sub> = ±8 V	108	120		dB	A
		T <sub>A</sub> = −40°C to +125°C	108			dB	B
V <sub>OS</sub>	Input offset voltage	T <sub>A</sub> = 25°C		0.1	1.5	mV	A
		T <sub>A</sub> = −40°C to +85°C			2.4	mV	B
		T <sub>A</sub> = −40°C to +125°C			2.8	mV	B
	Input offset voltage drift	T <sub>A</sub> = 25°C		1.5		μV/°C	B
		T <sub>A</sub> = −40°C to +125°C			13	μV/°C	B
	Input bias current	T <sub>A</sub> = 25°C		2	20	pA	A
		T <sub>A</sub> = −40°C to +85°C <sup>(4)</sup>		20	60	pA	B
		T <sub>A</sub> = −40°C to +125°C <sup>(4)</sup>		100	460	pA	B
	Input offset current	T <sub>A</sub> = 25°C		1	20	pA	A
		T <sub>A</sub> = −40°C to +85°C		5		pA	B
		T <sub>A</sub> = −40°C to +125°C		50		pA	B
CMRR	Common-mode rejection ratio	f = DC, T <sub>A</sub> = 25°C, V <sub>CM</sub> = ±5 V	90	105		dB	A
		T <sub>A</sub> = −40°C to +125°C	90			dB	B
INPUT							
	Allowable input differential voltage	see <a href="#">Fig 57</a>		±7		V	C
	Common-mode input impedance	In closed-loop configuration		12    2.5		GΩ  pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S+</sub> + 0.2	V <sub>S+</sub> + 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> + 0.1			V	B
	Most negative input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S−</sub> − 0.2	V <sub>S−</sub> − 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S−</sub> − 0.2			V	B
	Most positive input voltage for main-JFET stage	T <sub>A</sub> = 25°C (see <a href="#">Fig 35</a> )	V <sub>S+</sub> − 2.9	V <sub>S+</sub> − 2.5		V	C
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> − 3			V	C
OUTPUT							
V <sub>OCRH</sub>	Output voltage range high	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S+</sub> − 0.33	V <sub>S+</sub> − 0.22		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>L</sub> = 667 Ω	V <sub>S+</sub> − 0.36			V	B
V <sub>OCRL</sub>	Output voltage range low	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.23	V <sub>S−</sub> + 0.15		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.33			V	B
I <sub>O(max)</sub>	Linear output drive (sourcing and sinking)	T <sub>A</sub> = 25°C, V <sub>O</sub> = 7.25 V, R <sub>L</sub> = 151 Ω, V <sub>OS</sub> < 2 mV	48	64		mA	A
		T <sub>A</sub> = −40°C to +90°C, V <sub>O</sub> = 4.35 V, V <sub>OS</sub> < 2 mV	29			mA	B
I <sub>SC</sub>	Output short-circuit current	T <sub>A</sub> = 25°C, T <sub>Delay</sub> = 5 ms		108		mA	B
C <sub>L</sub>	Capacitive load drive	< 1 dB peaking, R <sub>S</sub> = 0 Ω		35		pF	C

(4) Maximum bias current specification is set using  $\pm 5\sigma$  limits (corresponding to 0.58 DPPM) obtained using the statistical distribution from electrical characterization over temperature of a sample set of 70 units. Maximum specification is not specified by final automated test equipment (ATE) nor by QA sample testing.

(5) Change in input offset from its value when input is biased to midsupply.

**Electrical Characteristics: 24 V (continued)**

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
POWER SUPPLY							
VS	Operating voltage	T <sub>A</sub> = 25°C	4.75		27	V	A
		T <sub>A</sub> = −40°C to +125°C	4.75		27	V	B
I <sub>Q</sub>	Quiescent current per channel	T <sub>A</sub> = 25°C	3.2	3.7	4.1	mA	A
		T <sub>A</sub> = −40°C to +125°C	3.0		4.5	mA	B
PSRR	Power supply rejection ratio	ΔV <sub>S</sub> = 2 V <sup>(6)</sup>	90	105		dB	A
		T <sub>A</sub> = −40°C to +125°C	90			dB	B
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product	V <sub>CM</sub> = V <sub>S+</sub> − 1 V		35		MHz	C
	Open-loop voltage gain	V <sub>CM</sub> = V <sub>S+</sub> − 1 V, f = DC, V <sub>O</sub> = 7 V to −7 V	80	95		dB	A
	Input-referred voltage noise	V <sub>CM</sub> = V <sub>S+</sub> − 1 V, f = 1 MHz		21		nV/√Hz	C
	Input offset voltage	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, no-load			4	mV	A
		V <sub>CM</sub> = V <sub>S+</sub> − 0.5 V, no-load			4.8	mV	A
		V <sub>CM</sub> = V <sub>S+</sub> − 0.5 V, T <sub>A</sub> = −40°C to +125°C, no-load			6.4	mV	B
	Input bias current	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V		2	24	pA	A
		V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, T <sub>A</sub> = −40°C to +125°C		0.15	1	nA	B
	Common-mode rejection ratio	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V to V <sub>S+</sub> − 0.5 V		75		dB	B
	Power supply rejection ratio	V <sub>CM</sub> = V <sub>S+</sub> − 1.5 V, ΔV <sub>S</sub> = ±2 V <sup>(6)</sup>		70		dB	B
CHANNEL MATCHING							
	Channel-to-channel GBWP mismatch	T <sub>A</sub> = 25°C		3		%	C
	Channel-to-channel crosstalk	f = 100 kHz		-93		dBc	C
	Input offset voltage mismatch	T <sub>A</sub> = 25°C		0.1	2.5	mV	A

(6) The supply voltages are  $V_{S+} = 12\text{ V} \pm 1\text{ V}$  and  $V_{S-} = -12\text{ V}$  for +PSRR, and  $V_{S+} = 12\text{ V}$  and  $V_{S-} = -12\text{ V} \pm 1\text{ V}$  for -PSRR.

## 6.7 Electrical Characteristics: 5 V

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{CM} = 1.25\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , and output is biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
<b>AC PERFORMANCE</b>							
SSBW	Small-signal bandwidth	$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\text{ }\Omega$		74		MHz	C
		$G = 1$ , $V_o = 20\text{ mV}_{PP}$ , $R_F = 0\text{ }\Omega$ , $C_L = 33\text{ pF}$		103		MHz	C
		$G = -1$ , $V_o = 20\text{ mV}_{PP}$		51		MHz	C
		$G = 2$ , $V_o = 20\text{ mV}_{PP}$		49		MHz	C
		$G = 5$ , $V_o = 20\text{ mV}_{PP}$		15		MHz	C
LSBW	Large-signal bandwidth	$G = 2$ , $V_o = 2\text{ V}_{PP}$		33		MHz	C
GBWP	Gain-bandwidth product	$G = 11$ , $V_o = 20\text{ mV}_{PP}$		70		MHz	C
	Bandwidth for 0.1dB flatness	$G = 2$ , $V_o = 20\text{ mV}_{PP}$		11		MHz	C
SR	Slew rate (20%-80%) <sup>(3)</sup>	$G = 2$ , $V_o = -1\text{ V}$ to $1\text{ V}$ step		119		V/ $\mu\text{s}$	C
		$G = 2$ , $V_o = -2\text{ V}$ to $2\text{ V}$ step, $V_S = \pm 2.5\text{ V}$		88		V/ $\mu\text{s}$	C
	Rise time	$V_o = 200\text{-mV}$ step		4		ns	C
	Fall time	$V_o = 200\text{-mV}$ step		5		ns	C
	Settling time to 0.1%	$G = 2$ , $V_o = -2\text{ V}$ to $0\text{ V}$ step, $V_S = \pm 2.5\text{ V}$		108		ns	C
	Settling time to 0.001%	$G = 2$ , $V_o = -2\text{ V}$ to $0\text{ V}$ step, $V_S = \pm 2.5\text{ V}$		197		ns	C
	Overshoot/undershoot	$G = 1$ , $V_o = 200\text{ mV}_{PP}$		10/11		%	C
		$G = 1$ , $V_o = -1.25\text{ V}$ to $0.75\text{ V}$ step		1/7		%	C
	Input overdrive recovery	$G = 1$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input, $V_S = \pm 2.5\text{ V}$ (see <a href="#">Figure 39</a> )		71		ns	C
	Output overdrive recovery	$G = -1$ , ( $V_{S-} - 0.5\text{ V}$ ) to ( $V_{S+} + 0.5\text{ V}$ ) input, $V_S = \pm 2.5\text{ V}$ (see <a href="#">Figure 40</a> )		91		ns	C
HD2	Second-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-102		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-85		dBc	C
HD3	Third-order harmonic distortion	$f = 100\text{ kHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-113		dBc	C
		$f = 1\text{ MHz}$ , $R_L = 1\text{ k}\Omega$ , $V_o = 2\text{ V}_{PP}$		-97		dBc	C
$e_n$	Input-referred voltage noise	$f = 500\text{ kHz}$ , 1atband		6		nV/ $\sqrt{\text{Hz}}$	C
		$f = 0.1\text{-}10\text{ Hz}$ integrated		0.42		$\mu\text{V}_{rms}$	C
$e_i$	Input-referred current noise	$f = 10\text{ kHz}$		5		fA/ $\sqrt{\text{Hz}}$	C
$z_O$	Close-loop output impedance	$f = 100\text{ kHz}$		0.007		$\Omega$	C
<b>DC PERFORMANCE</b>							
$A_{OL}$	Open-loop voltage gain	$f = \text{DC}$ , $V_o = 1.25\text{ V}$ to $3.25\text{ V}$	104	118		dB	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	104			dB	B
$V_{OS}$	Input offset voltage	$T_A = 25^\circ\text{C}$ , no-load		0.1	1.5	mV	A
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			2.4	mV	B
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2.8	mV	B
	Input offset voltage drift	$T_A = 25^\circ\text{C}$ , no-load		1.5		$\mu\text{V}/^\circ\text{C}$	B
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			13	$\mu\text{V}/^\circ\text{C}$	B

(1) For AC specifications,  $V_{S+} = 3.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ ,  $C_L = 4.7\text{ pF}$ , input and output are biased to  $0\text{ V}$  (unless otherwise noted).

(2) Test levels (all values set by characterization and simulation): (A) 100% tested at  $25^\circ\text{C}$ , overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.

(3) Lower of the measured positive and negative slew rate.

**Electrical Characteristics: 5 V (continued)**

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{CM} = 1.25\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , and output is biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
	Input bias current	T <sub>A</sub> = 25°C		2	20	pA	A
		T <sub>A</sub> = −40°C to +85°C <sup>(4)</sup>		20	50	pA	B
		T <sub>A</sub> = −40°C to +125°C <sup>(4)</sup>		100	340	pA	B
	Input offset current	T <sub>A</sub> = 25°C		1	20	pA	A
		T <sub>A</sub> = −40°C to +85°C		5		pA	B
		T <sub>A</sub> = −40°C to +125°C		50		pA	B
CMRR	Common-mode rejection ratio	f = DC, T <sub>A</sub> = 25°C, V <sub>CM</sub> = 0.75 V to 1.75 V	78	92		dB	A
		T <sub>A</sub> = −40°C to +125°C	75			dB	B
INPUT							
	Allowable input differential voltage	See <a href="#">Figure 57</a>		±5		V	C
	Common-mode input impedance	In closed-loop configuration		12    2.5		GΩ  pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S+</sub> + 0.2	V <sub>S+</sub> + 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> + 0.2			V	B
	Most negative input voltage	ΔV <sub>OS</sub> < 5 mV <sup>(5)</sup>	V <sub>S−</sub> − 0.2	V <sub>S−</sub> − 0.3		V	A
		T <sub>A</sub> = −40°C to +125°C	V <sub>S−</sub> − 0.2			V	B
	Most positive input voltage for main-JFET stage	T = 25°C (see <a href="#">Figure 43</a> )	V <sub>S+</sub> − 2.9	V <sub>S+</sub> − 2.5		V	C
		T <sub>A</sub> = −40°C to +125°C	V <sub>S+</sub> − 3			V	C
OUTPUT							
V <sub>OCRH</sub>	Output voltage range high	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S+</sub> − 0.12	V <sub>S+</sub> − 0.09		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>LOAD</sub> = 667 Ω	V <sub>S+</sub> − 0.15			V	B
V <sub>OCRL</sub>	Output voltage range low	T <sub>A</sub> = 25°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.1	V <sub>S−</sub> + 0.06		V	A
		T <sub>A</sub> = −40°C to +125°C, R <sub>L</sub> = 667 Ω	V <sub>S−</sub> + 0.15			V	B
I <sub>O(max)</sub>	Linear output drive (sourcing and sinking)	T <sub>A</sub> = 25°C, V <sub>O</sub> = 1.4 V, R <sub>L</sub> = 27.5 Ω, V <sub>OS</sub> < 2 mV, V <sub>S+</sub> = 3 V and V <sub>S−</sub> = −2 V	50	64		mA	A
		T <sub>A</sub> = −40°C to 125°C, V <sub>O</sub> = 0.6 V, V <sub>OS</sub> < 2 mV, V <sub>S+</sub> = 3 V and V <sub>S−</sub> = −2 V	22			mA	B
I <sub>SC</sub>	Output short-circuit current	T <sub>A</sub> = 25°C, T <sub>Delay</sub> = 5 ms		96		mA	B
C <sub>L</sub>	Capacitive load drive	< 1 dB peaking, R <sub>S</sub> = 0 Ω		35		pF	C
POWER SUPPLY							
V <sub>S</sub>	Operating voltage	T <sub>A</sub> = 25°C	4.75		27	V	A
		T <sub>A</sub> = −40°C to +125°C	4.75		27	V	B
I <sub>Q</sub>	Quiescent current per channel	T <sub>A</sub> = 25°C	3.05	3.6	4	mA	A
		T <sub>A</sub> = −40°C to +125°C	2.8		4.4	mA	B
PSRR	Power supply rejection ratio	ΔV <sub>S</sub> = 0.5 V, V <sub>CM</sub> = 0.5 V <sup>(6)</sup>	80	100		dB	A
		T <sub>A</sub> = −40°C to +125°C	80			dB	B

(4) Maximum bias current specification is set using  $\pm 5\sigma$  limits (corresponding to 0.58 DPPM) obtained using the statistical distribution from electrical characterization over temperature of a sample set of 70 units. Maximum specification is not specified by final automated test equipment (ATE) nor by QA sample testing.

(5) Change in input offset from its value when input is biased to 0 V.

(6) The supply voltages are  $V_{S+} = 5\text{ V} \pm 0.25\text{ V}$  and  $V_{S-} = 0\text{ V}$  for +PSRR, and  $V_{S+} = 5\text{ V}$  and  $V_{S-} = 0\text{ V} \pm 0.25\text{ V}$  for -PSRR.

## Electrical Characteristics: 5 V (continued)

Test conditions unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{CM} = 1.25\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , and output is biased to midsupply<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level <sup>(2)</sup>
<b>AUXILIARY CMOS INPUT STAGE</b>							
	Gain-bandwidth product	$V_{CM} = V_{S+} - 1\text{ V}$		35		MHz	C
	Open-loop voltage gain	$V_{CM} = V_{S+} - 1\text{ V}$ , $f = \text{DC}$ , $V_o = 1.5\text{ V}$ to $2.5\text{ V}$	80	100		dB	A
	Input-referred voltage noise	$V_{CM} = V_{S+} - 1\text{ V}$ , $f = 1\text{ MHz}$		21		nV/ $\sqrt{\text{Hz}}$	C
	Input offset voltage	$V_{CM} = V_{S+} - 1.5\text{ V}$ , no-load			4	mV	A
		$V_{CM} = V_{S+} - 0.5\text{ V}$ , no-load			4.8	mV	A
		$V_{CM} = V_{S+} - 0.5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , no-load			6.4	mV	B
	Input bias current	$V_{CM} = V_{S+} - 1.5\text{ V}$		2	20	pA	A
		$V_{CM} = V_{S+} - 1.5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.15	0.5	nA	B
	Common-mode rejection ratio	$V_{CM} = V_{S+} - 1.5\text{ V}$ to $V_{S+} - 0.5\text{ V}$		75		dB	B
	Power supply rejection ratio	$V_{CM} = V_{S+} - 1.5\text{ V}$ , $\Delta V_S = \pm 0.5\text{ V}$ <sup>(6)</sup>		75		dB	B
<b>CHANNEL MATCHING</b>							
	Channel-to-channel GBWP mismatch	$T_A = 25^\circ\text{C}$		3		%	C
	Channel-to-channel crosstalk	$f = 100\text{ kHz}$		-93		dBc	C
	Input offset voltage mismatch	$T_A = 25^\circ\text{C}$		0.1	2.5	mV	A

## 6.8 Typical Characteristics: $V_S = 10\text{ V}$

at  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

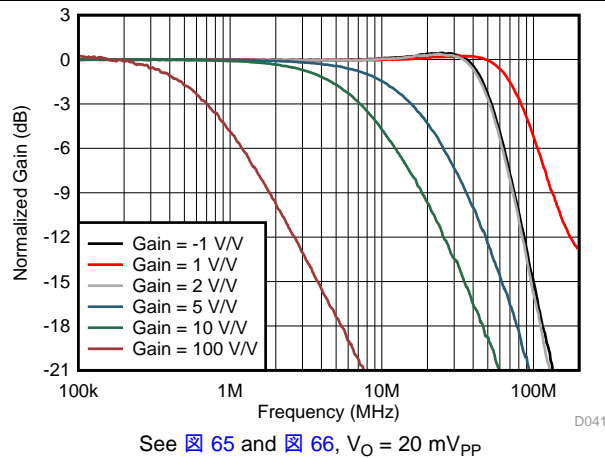


Figure 1. Small-Signal Frequency Response vs Gain

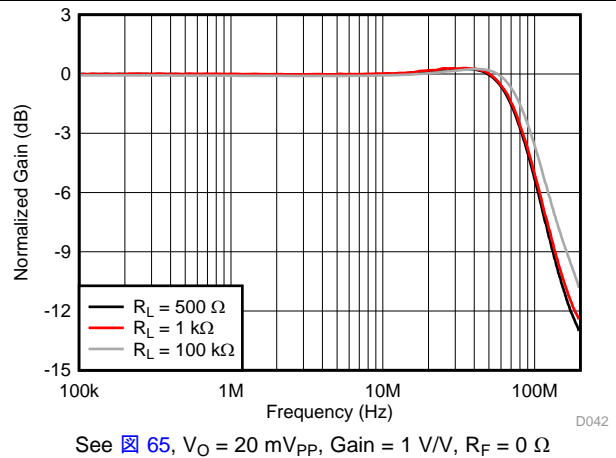


Figure 2. Small-Signal Frequency Response vs Output Load

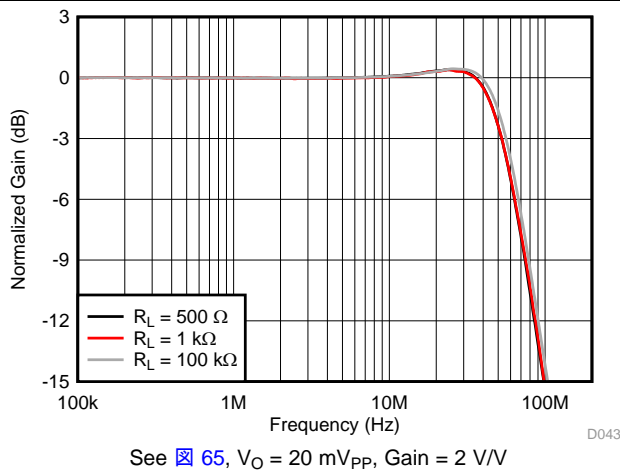


Figure 3. Small-Signal Frequency Response vs Output Load

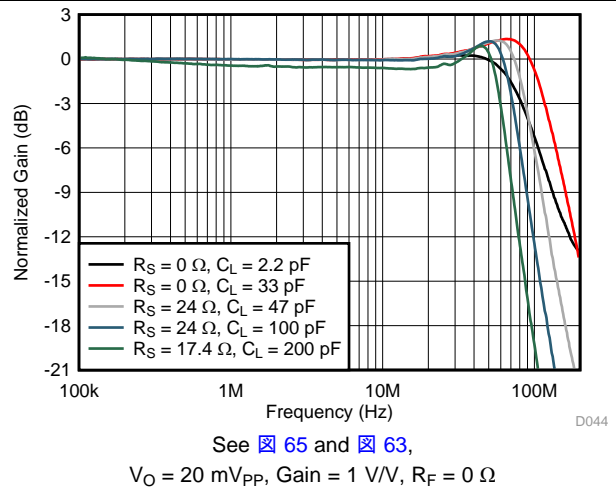


Figure 4. Small-Signal Frequency Response vs  $C_L$

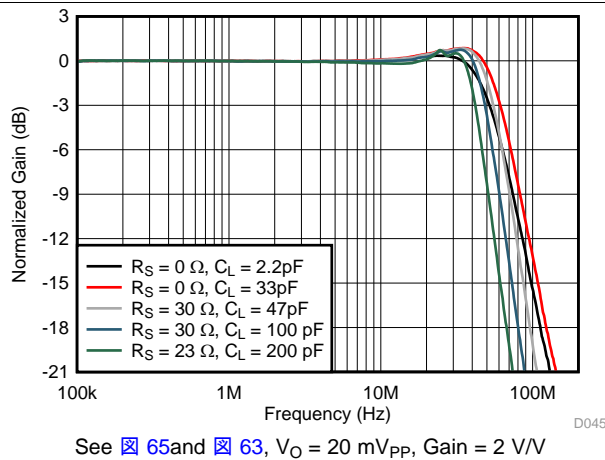


Figure 5. Small-Signal Frequency Response vs  $C_L$

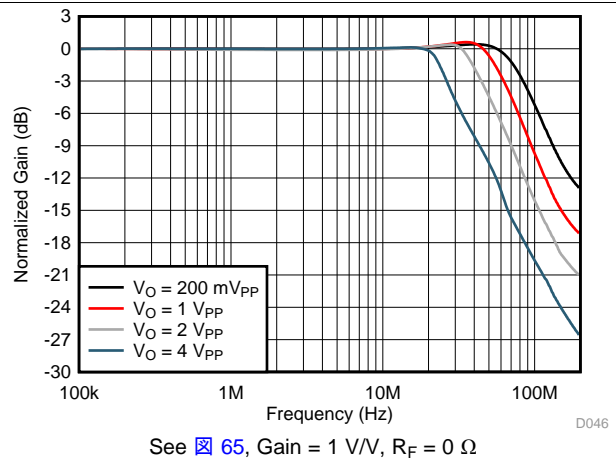
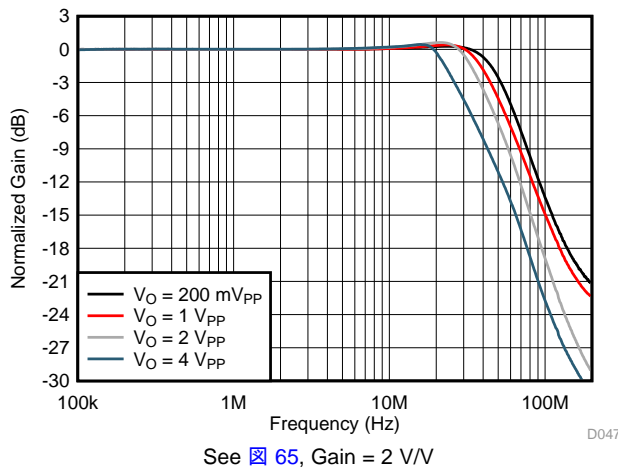


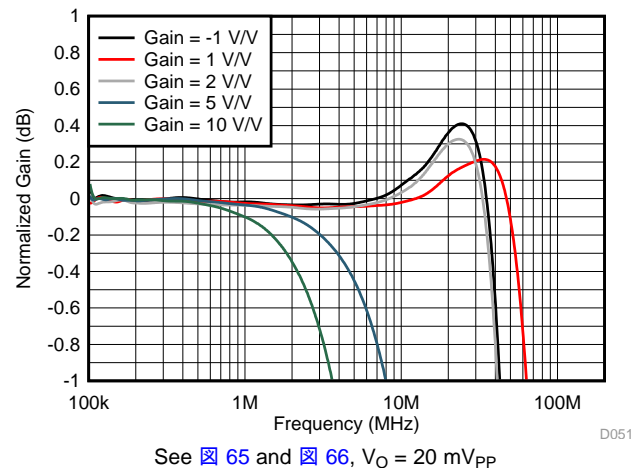
Figure 6. Large-Signal Frequency Response vs Output Voltage

## Typical Characteristics: $V_S = 10\text{ V}$ (continued)

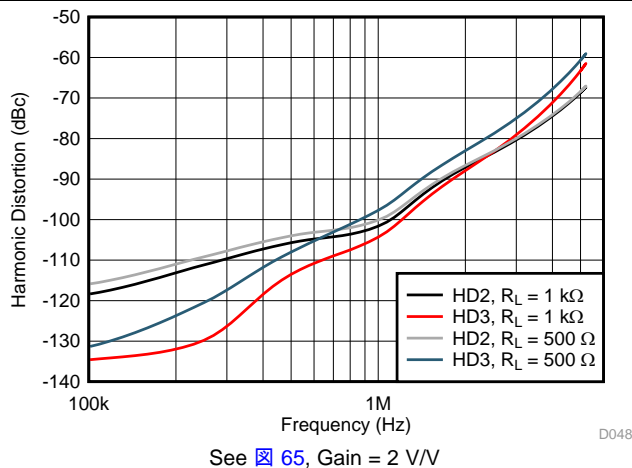
at  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)



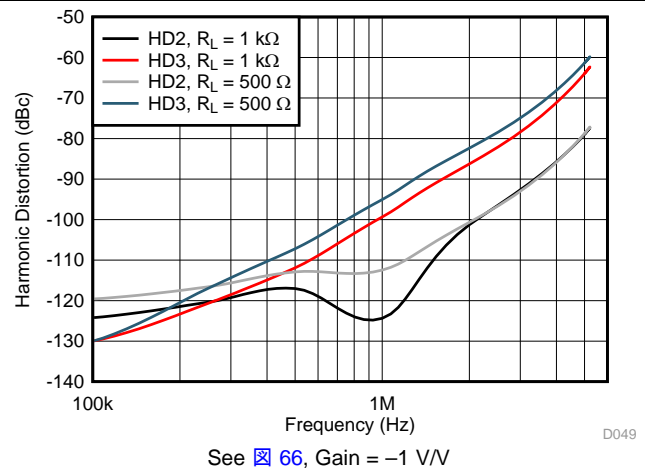
**Figure 7. Large-Signal Frequency Response vs Output Voltage**



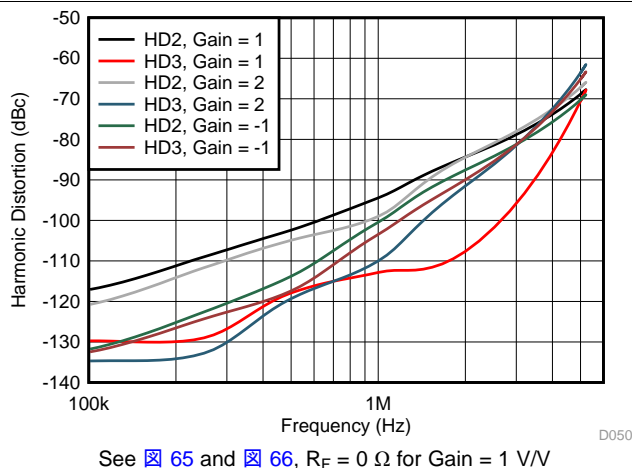
**Figure 8. Small-Signal Response Flatness vs Gain**



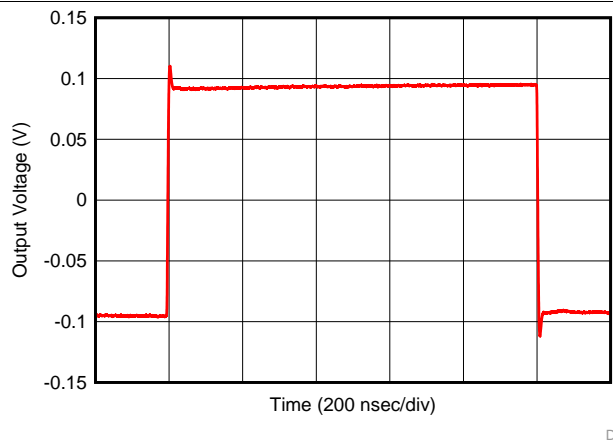
**Figure 9. Harmonic Distortion vs Frequency**



**Figure 10. Harmonic Distortion vs Frequency**



**Figure 11. Harmonic Distortion vs Gain**



**Figure 12. Small-Signal Transient Response**

## Typical Characteristics: $V_S = 10\text{ V}$ (continued)

at  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

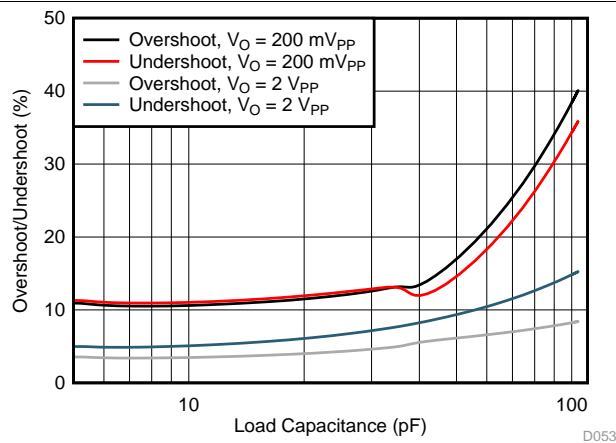


Figure 13. Overshoot and Undershoot vs  $C_L$

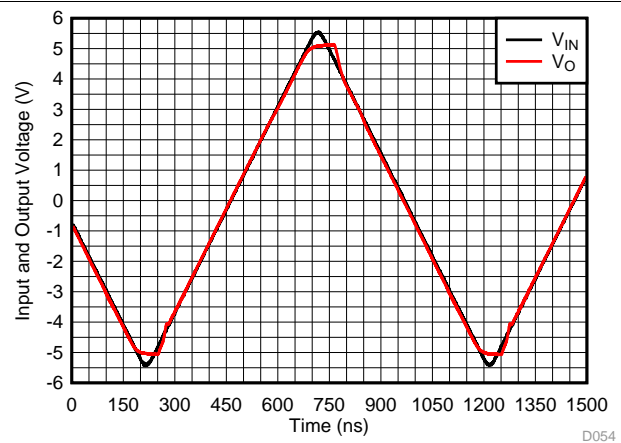


Figure 14. Input Overdrive Recovery

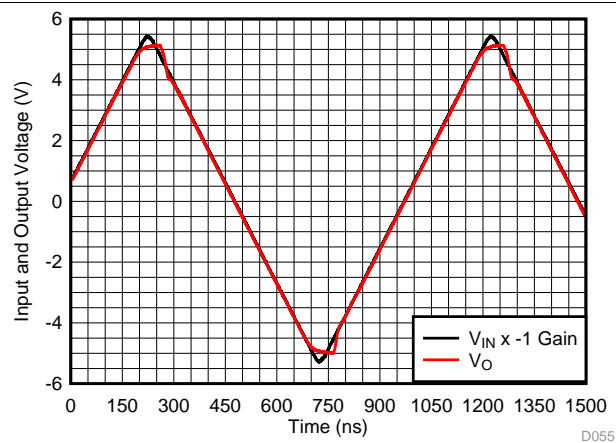


Figure 15. Output Overdrive Recovery

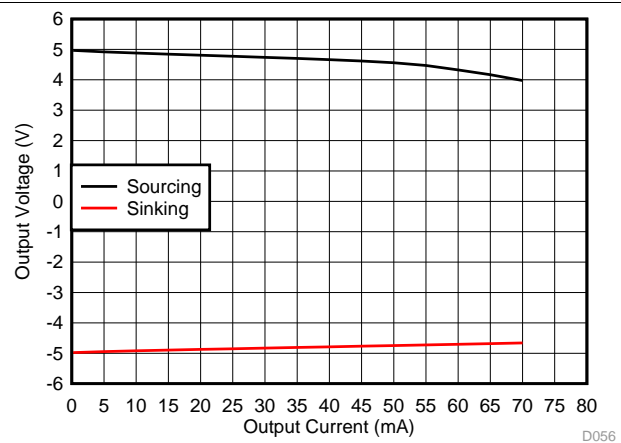


Figure 16. Output Voltage vs Load Current

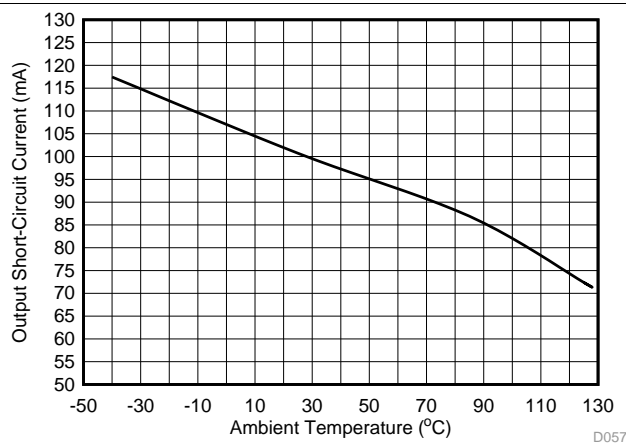


Figure 17. Output Short-Circuit Current vs Ambient Temperature

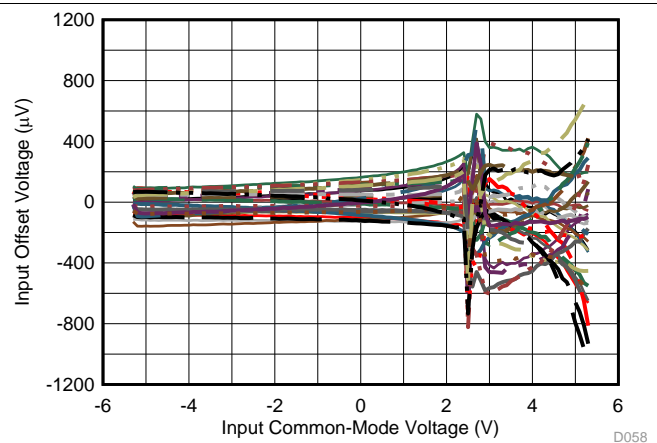
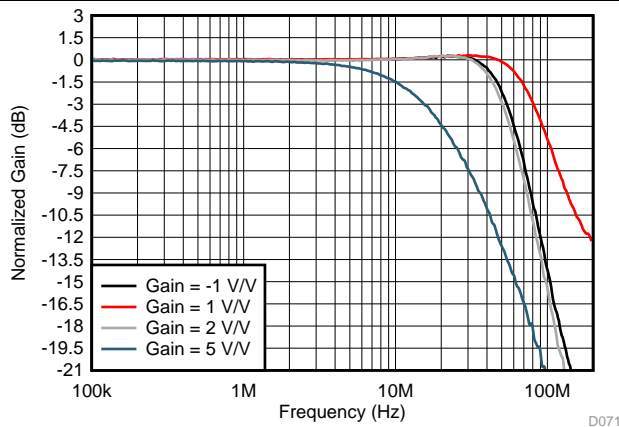


Figure 18. Input Offset Voltage vs Input Common-Mode Voltage

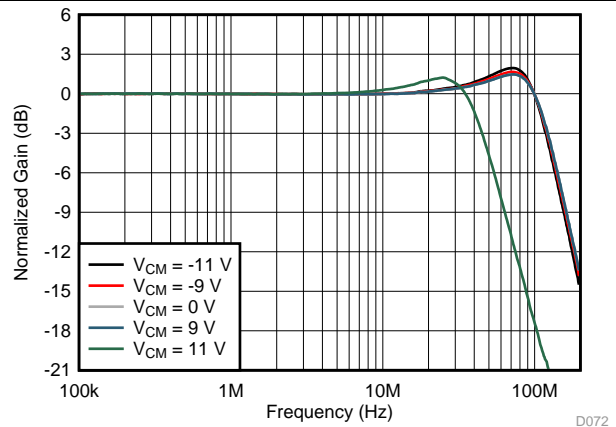


## 6.9 Typical Characteristics: $V_S = 24\text{ V}$

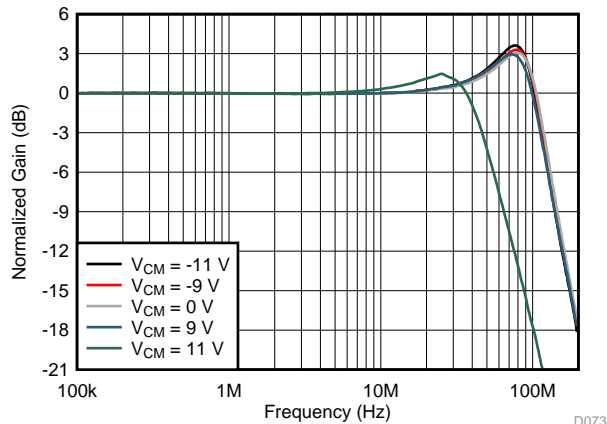
at  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)



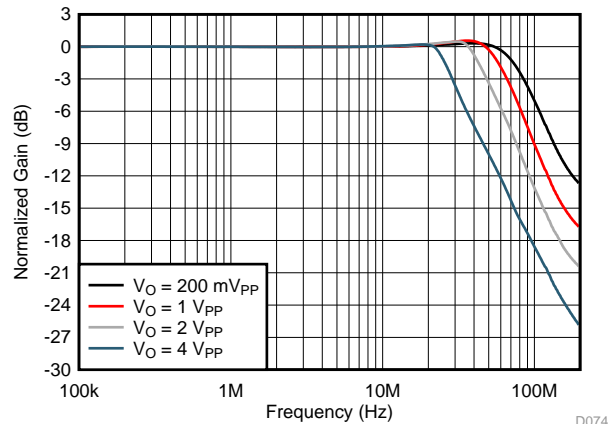
**Figure 19. Noninverting Small-Signal Frequency Response vs Gain**



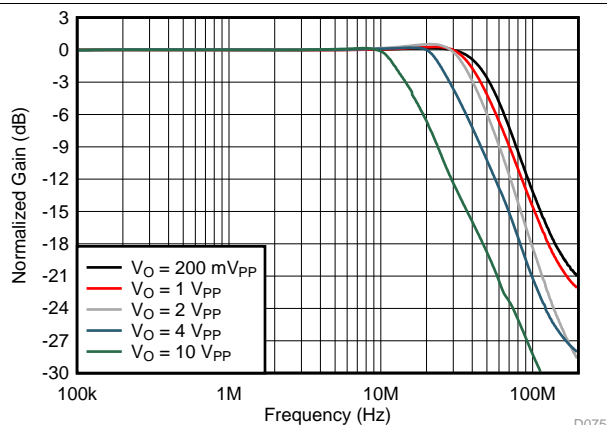
**Figure 20. Small-Signal Frequency Response vs Output Common-Mode Voltage**



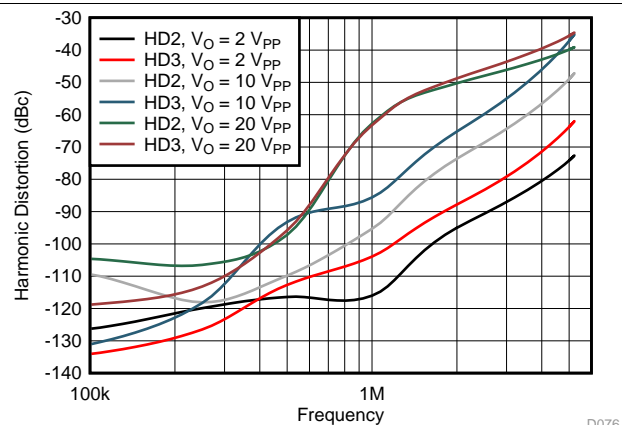
**Figure 21. Small-Signal Frequency Response vs Output Common-Mode Voltage**



**Figure 22. Large-Signal Frequency Response vs Output Voltage**



**Figure 23. Large-Signal Frequency Response vs  $V_O$**



**Figure 24. Harmonic Distortion vs Frequency vs  $V_O$**

## Typical Characteristics: $V_S = 24\text{ V}$ (continued)

at  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

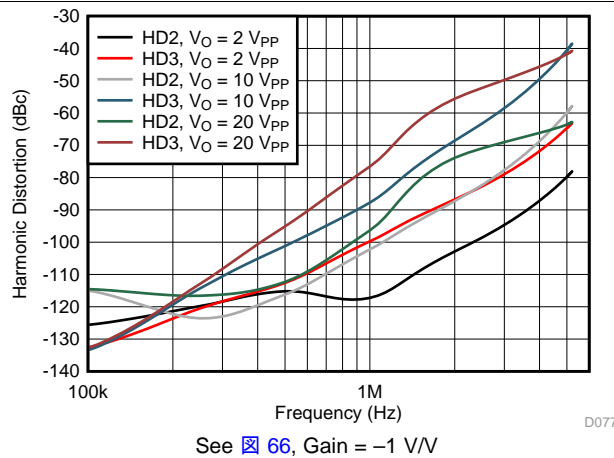


Figure 25. Harmonic Distortion vs Frequency vs  $V_O$

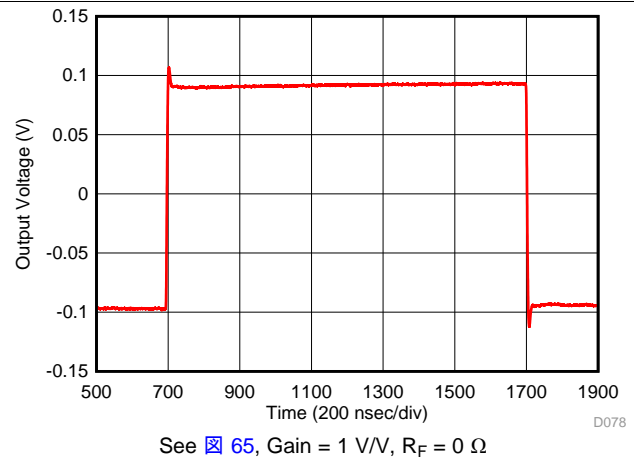


Figure 26. Small-Signal Transient Response

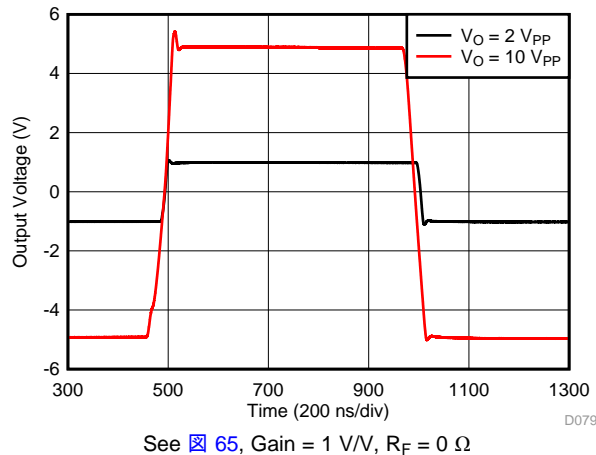


Figure 27. Large-Signal Transient Response

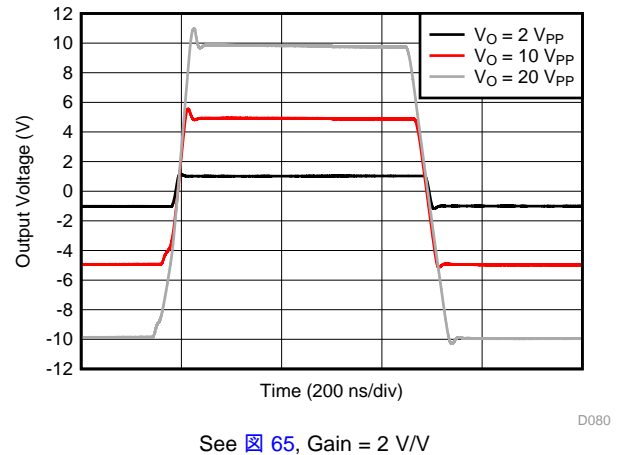


Figure 28. Large-Signal Transient Response

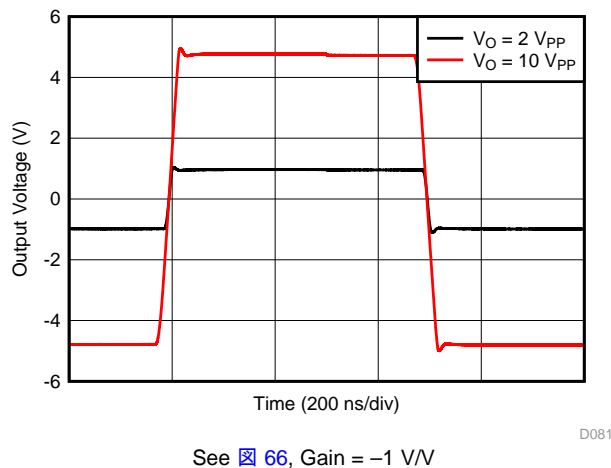


Figure 29. Large-Signal Transient Response

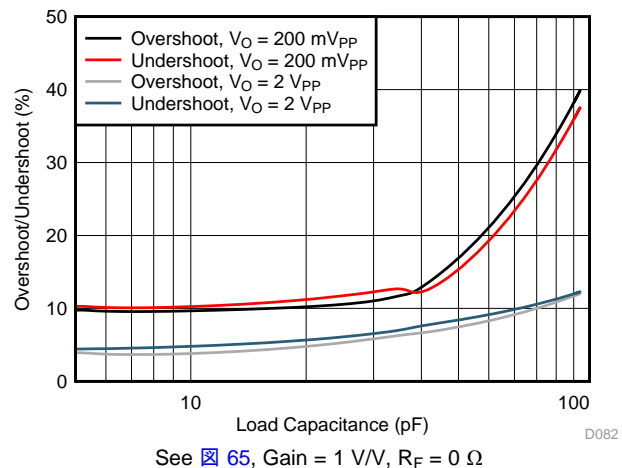


Figure 30. Overshoot and Undershoot vs  $C_L$

## Typical Characteristics: $V_S = 24\text{ V}$ (continued)

at  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = -12\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , input and output are biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

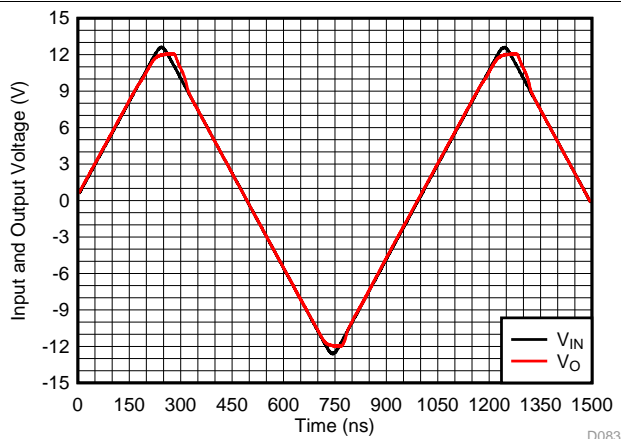


Figure 31. Input Overdrive Recovery

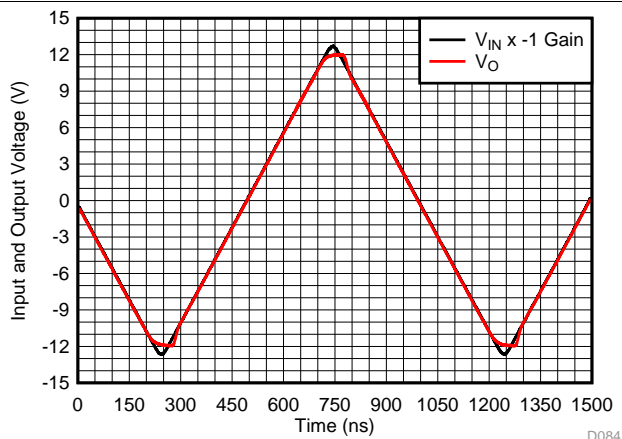


Figure 32. Output Overdrive Recovery

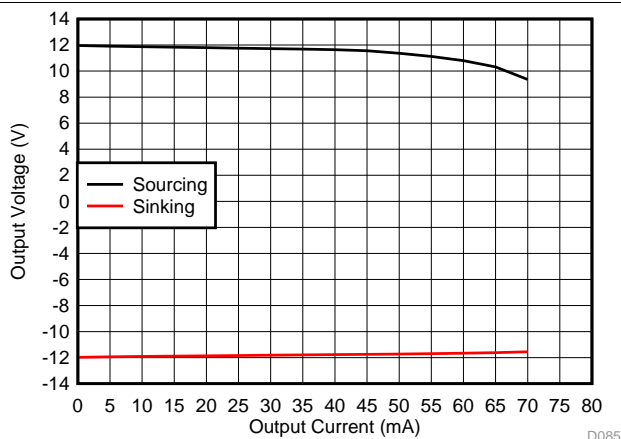


Figure 33. Output Voltage Range vs Load Current

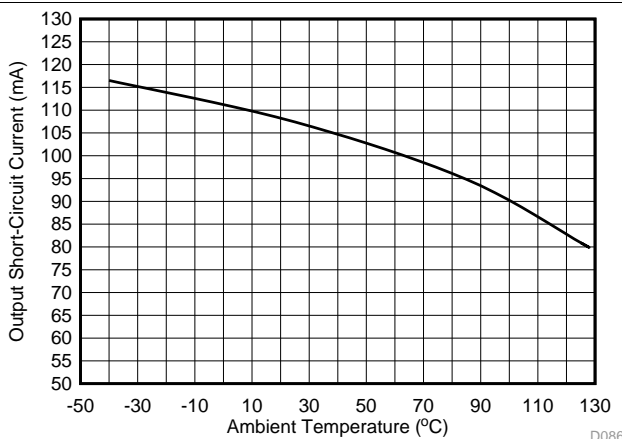


Figure 34. Output Short-Circuit Current vs Ambient Temperature

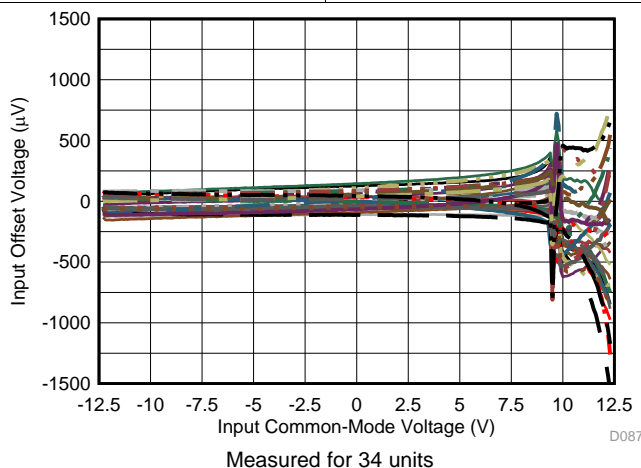


Figure 35. Input Offset Voltage vs Input Common-Mode Voltage

## 6.10 Typical Characteristics: $V_S = 5\text{ V}$

at  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{CM} = 1.25\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , output is biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_{S+} = 3.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

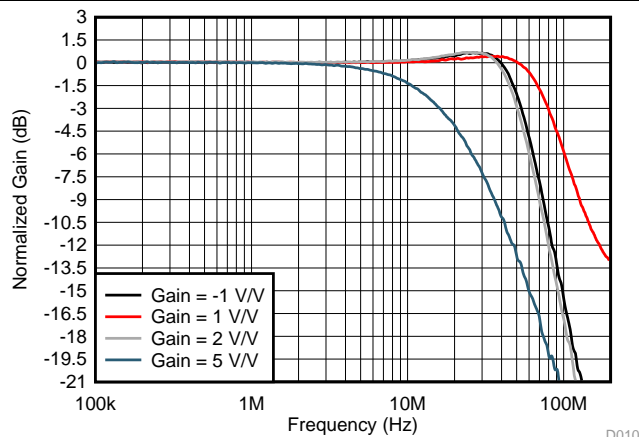


Figure 36. Small-Signal Response vs Gain

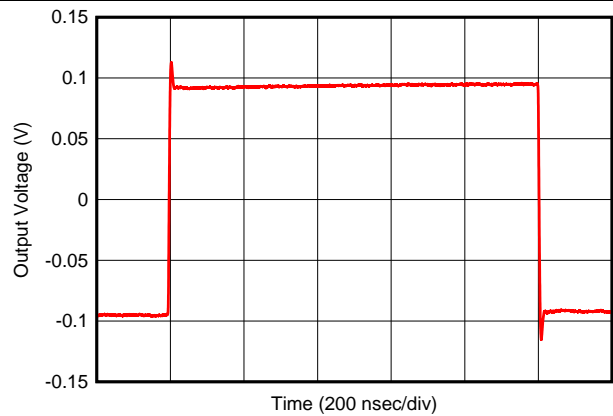


Figure 37. Small-Signal Transient Response

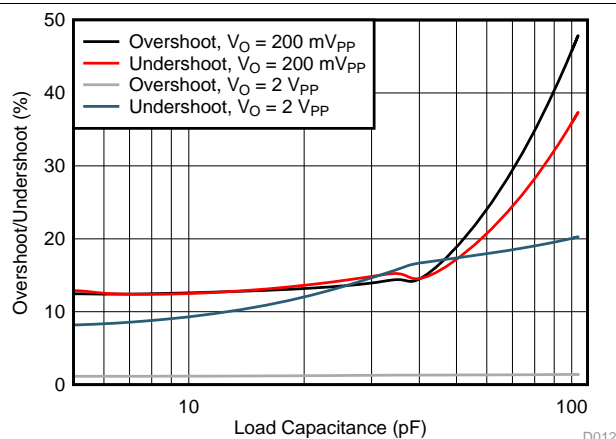


Figure 38. Overshoot and Undershoot vs  $C_L$

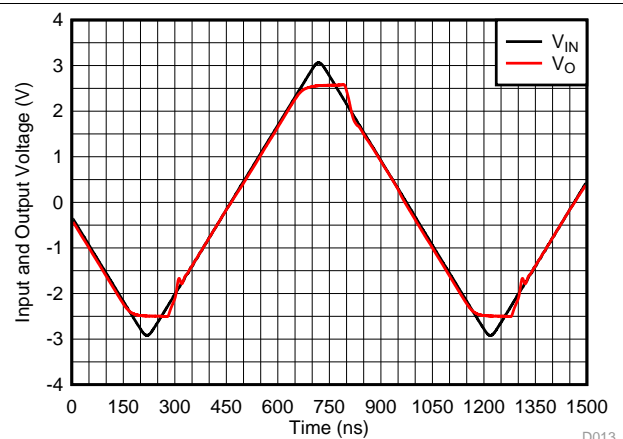


Figure 39. Input Overdrive Recovery

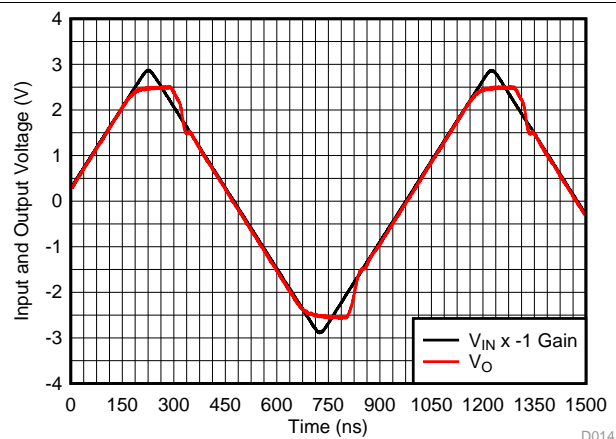


Figure 40. Output Overdrive Recovery

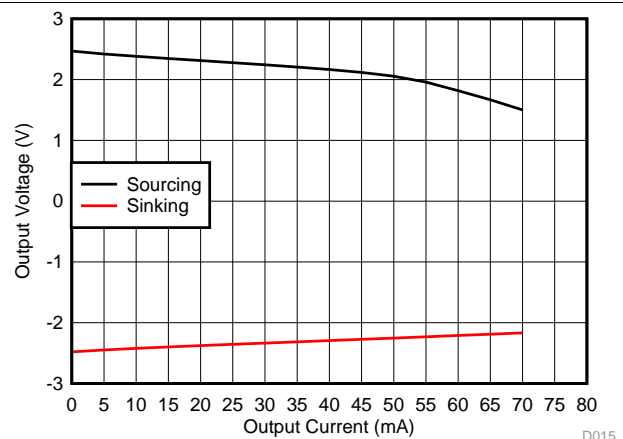


Figure 41. Output Voltage Range vs Output Current

## Typical Characteristics: $V_S = 5\text{ V}$ (continued)

at  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{CM} = 1.25\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , output is biased to midsupply, and  $T_A \approx 25^\circ\text{C}$ . For AC specifications,  $V_{S+} = 3.5\text{ V}$ ,  $V_{S-} = -1.5\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $V_O = 2\text{ V}_{PP}$ ,  $G = 2\text{ V/V}$ ,  $R_F = 1\text{ k}\Omega$ , and  $C_L = 4.7\text{ pF}$  (unless otherwise noted)

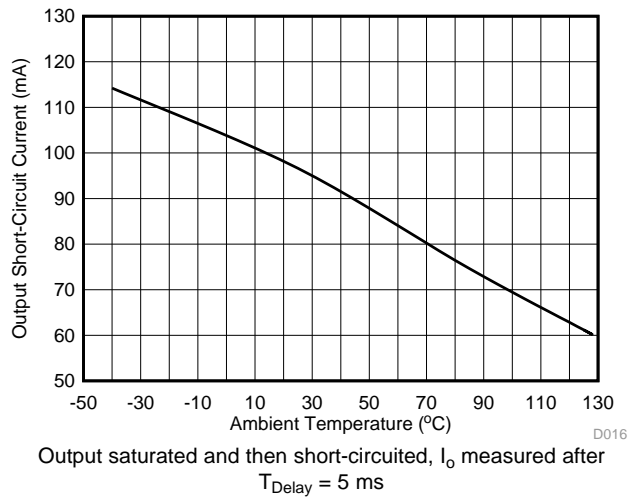


FIG 42. Output Short-Circuit Current vs Ambient Temperature

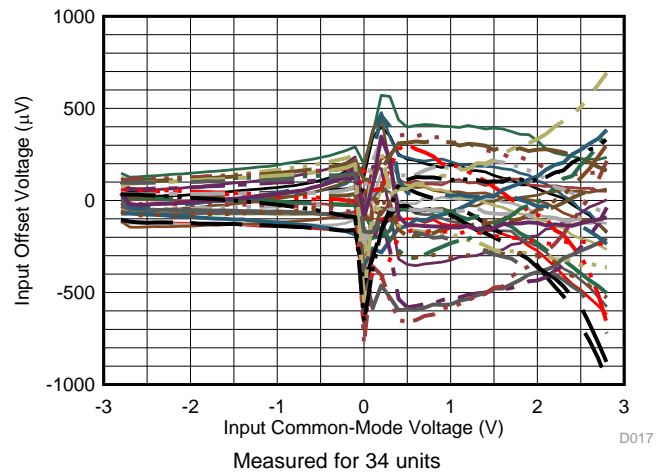


FIG 43. Input Offset Voltage vs Input Common-Mode Voltage

## 6.11 Typical Characteristics: $\pm 2.375$ V to $\pm 12$ V Split Supply

at  $V_O = 2 V_{PP}$ ,  $R_F = 1$  k $\Omega$ ,  $R_L = 1$  k $\Omega$  and  $T_A \approx 25^\circ\text{C}$  (unless otherwise noted)

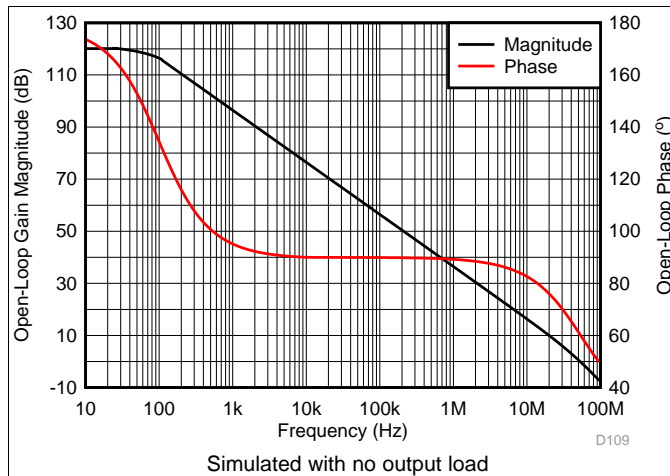


Figure 44. Open-Loop Gain and Phase vs Frequency

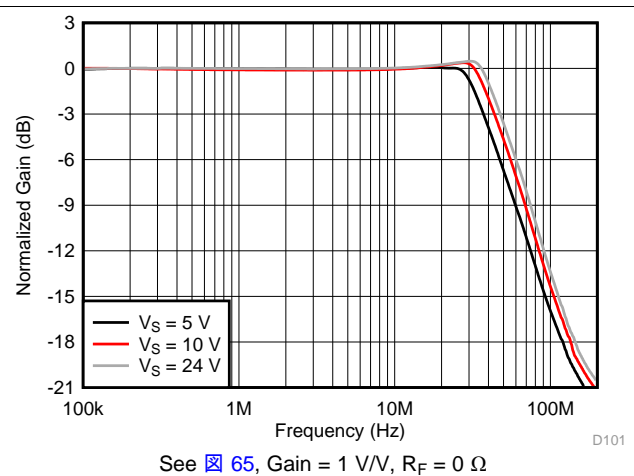


Figure 45. Large-Signal Response vs Supply Voltage

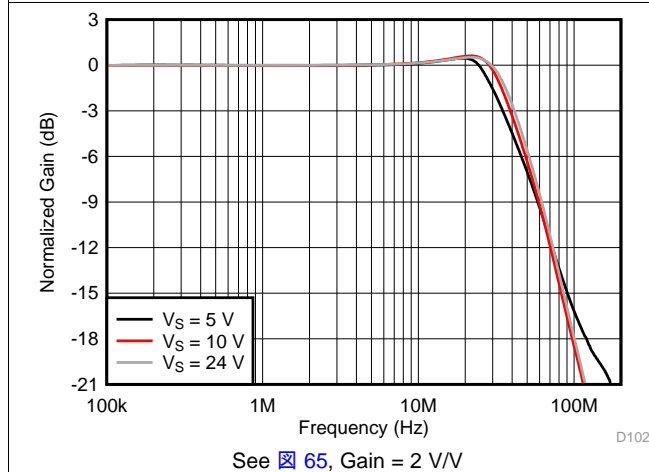


Figure 46. Large-Signal Response vs Supply Voltage

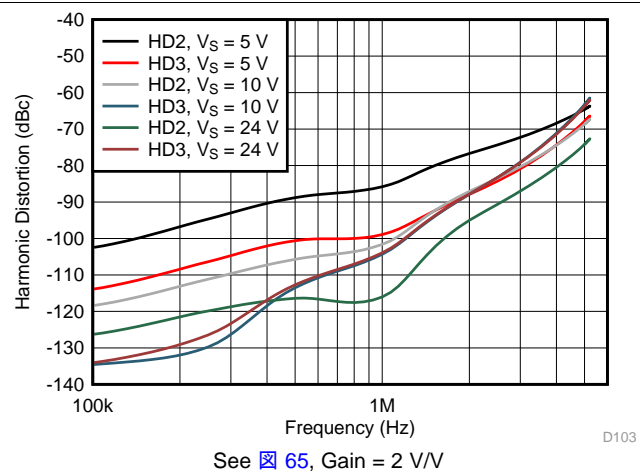


Figure 47. Harmonic Distortion vs Frequency vs Supply Voltage

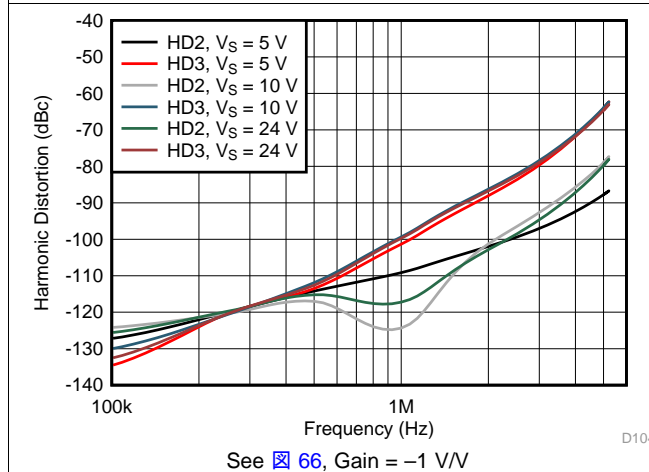


Figure 48. Harmonic Distortion vs Frequency vs Supply Voltage

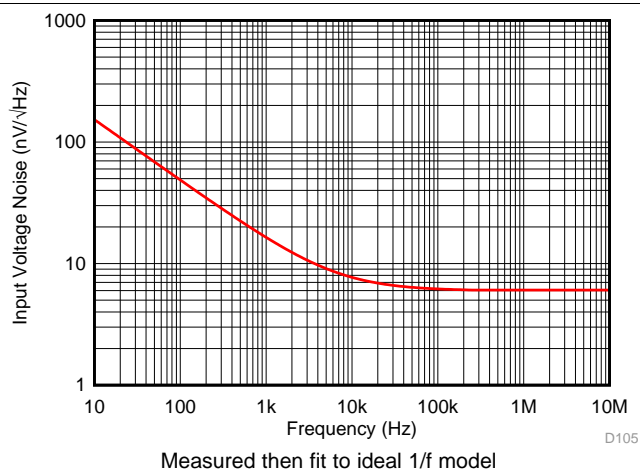
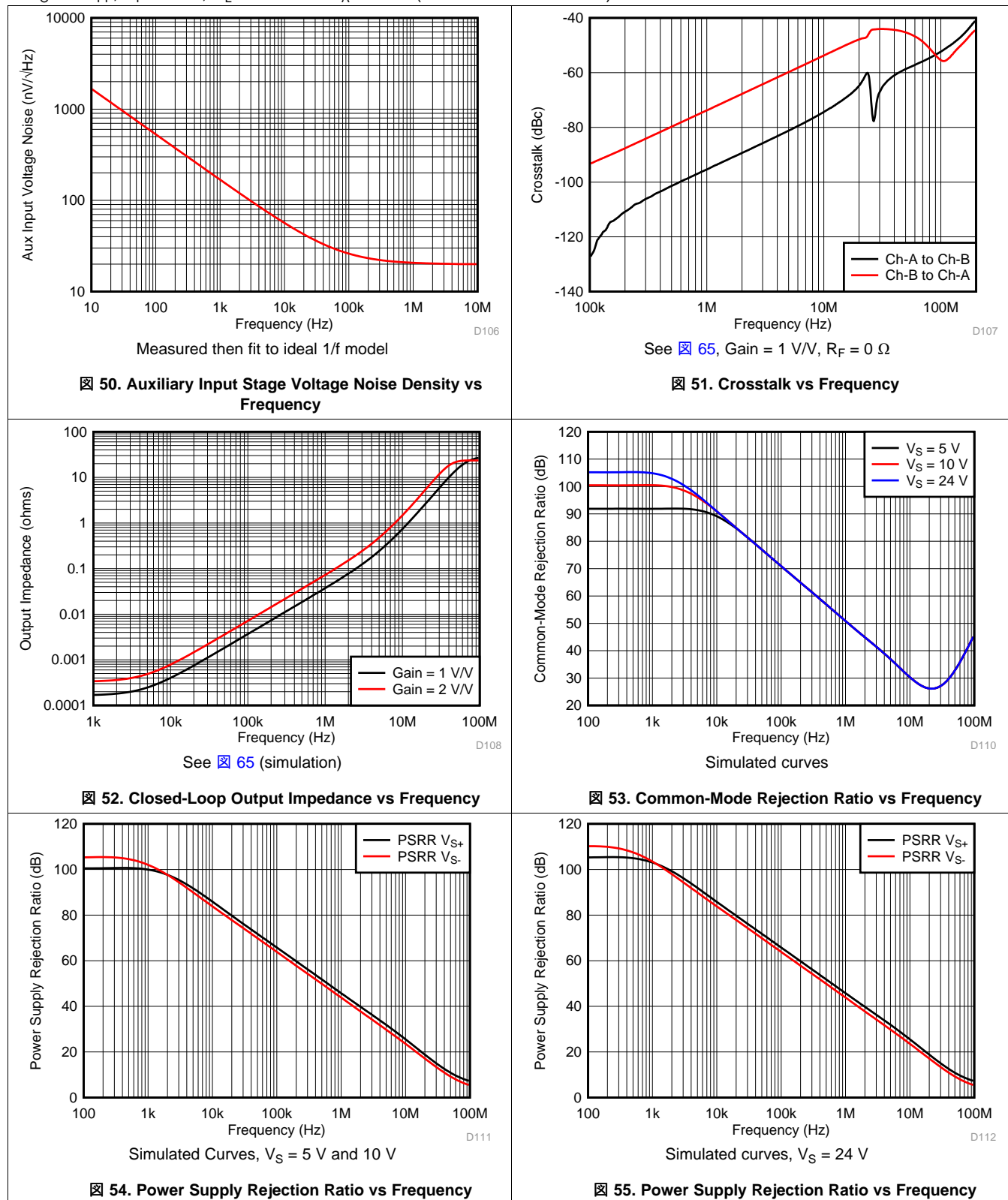


Figure 49. Input Voltage Noise Density vs Frequency

## Typical Characteristics: $\pm 2.375$ V to $\pm 12$ V Split Supply (continued)

at  $V_O = 2 V_{PP}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_L = 1\text{ k}\Omega$  and  $T_A \approx 25^\circ\text{C}$  (unless otherwise noted)



## Typical Characteristics: $\pm 2.375$ V to $\pm 12$ V Split Supply (continued)

at  $V_O = 2 V_{PP}$ ,  $R_F = 1$  k $\Omega$ ,  $R_L = 1$  k $\Omega$  and  $T_A \approx 25^\circ\text{C}$  (unless otherwise noted)

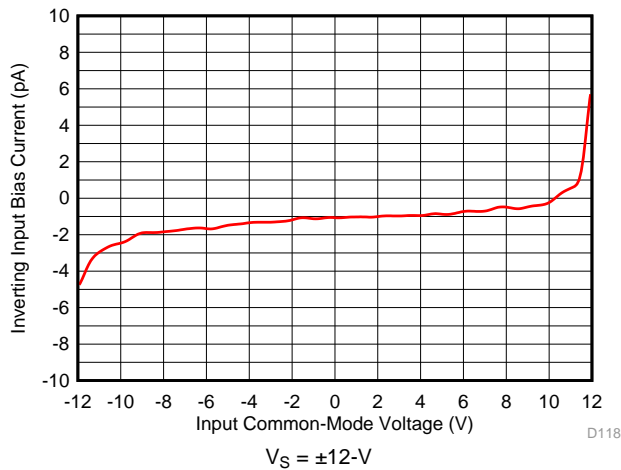


Figure 56. Input Bias Current vs Input Common-Mode Voltage

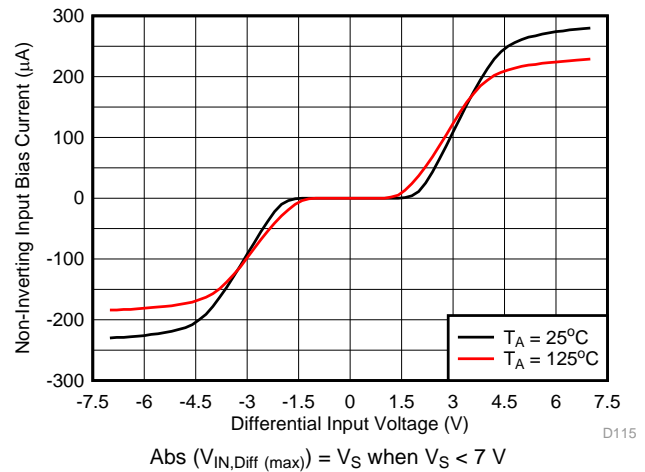


Figure 57. Input Bias Current vs Differential Input Voltage

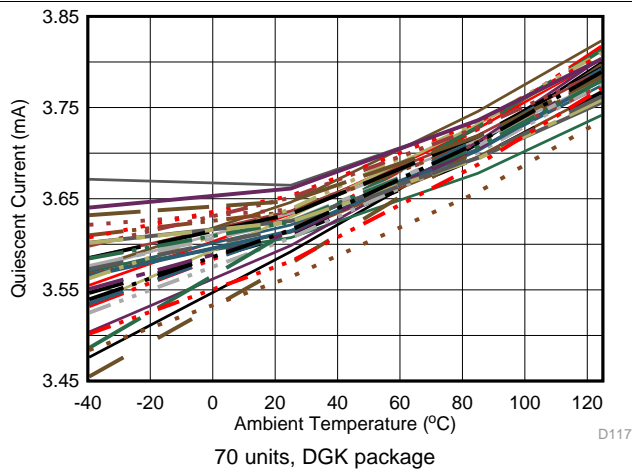


Figure 58. Quiescent Current vs Ambient Temperature

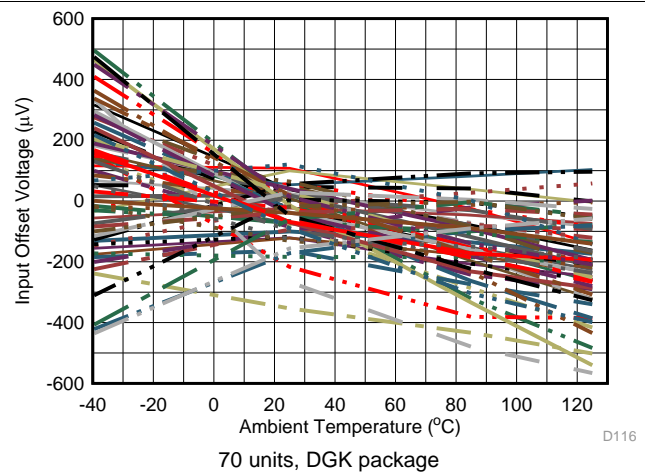


Figure 59. Input Offset Voltage vs Ambient Temperature

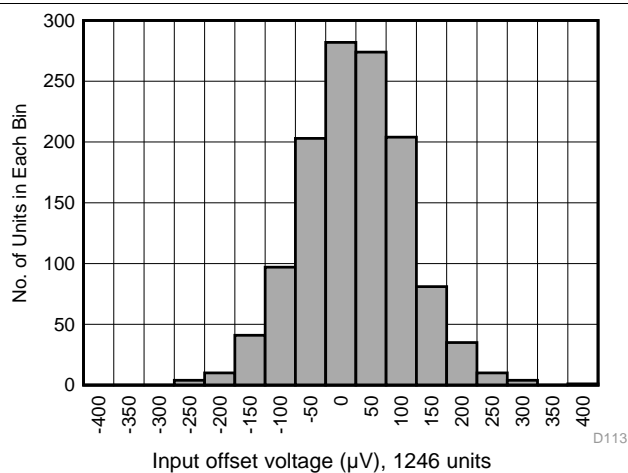
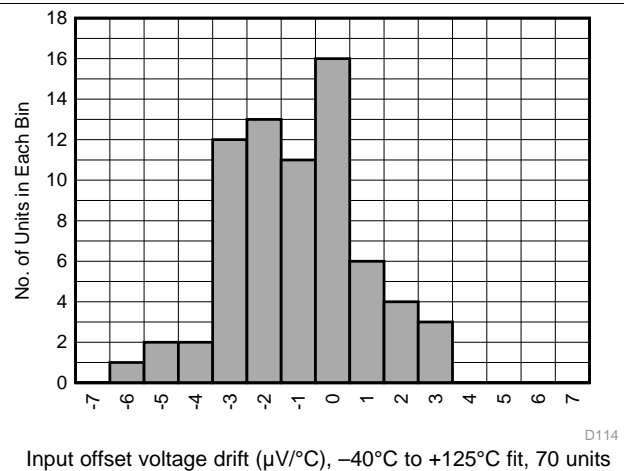


Figure 60. Input Offset Voltage Distribution



Input offset voltage drift ( $\mu\text{V}/^\circ\text{C}$ ),  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  fit, 70 units

Figure 61. Input Offset Voltage Drift Distribution



## 7 Detailed Description

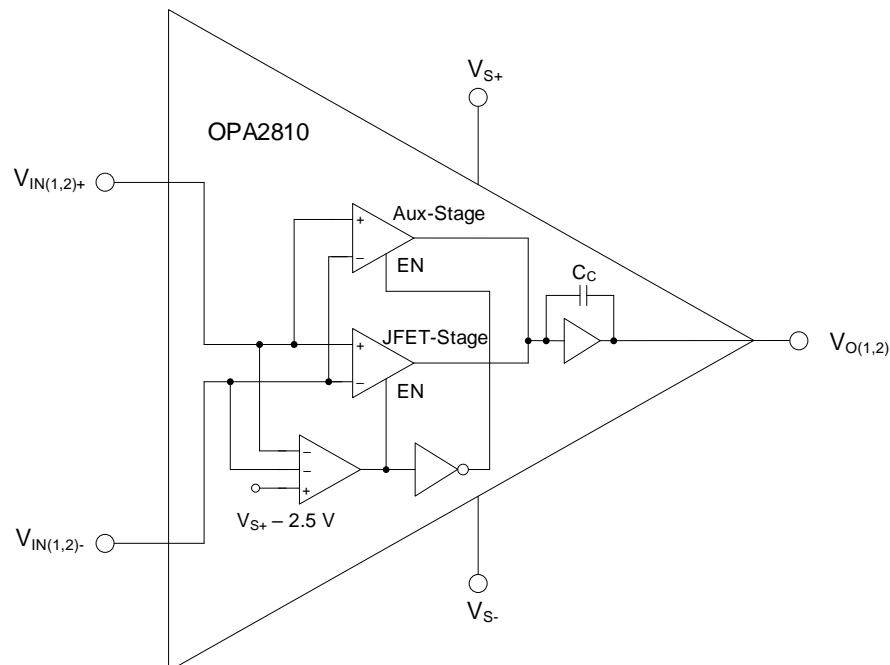
### 7.1 Overview

The OPA2810 is a dual-channel, FET-input, unity-gain stable voltage-feedback operational amplifier with extremely low input bias current across its common-mode input voltage range. The OPA2810, characterized to operate over a wide supply range of 4.75 V to 27 V, has a small-signal unity-gain bandwidth of 105 MHz and offers both excellent DC precision and dynamic AC performance at low quiescent power. The OPA2810 is fabricated on Texas Instrument's proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70MHz, extremely high slew-rate (192 V/ $\mu$ s), and low-noise (6 nV/ $\sqrt{\text{Hz}}$ ) the OPA2810 is ideal in a wide range of data acquisition and signal processing applications. The OPA2810 includes input clamps to allow maximum input differential voltage of up to 7 V, making it suitable for use with multiplexers and processing of signals with fast transients. It achieves these benchmark levels of performance while consuming a typical quiescent current ( $I_Q$ ) of 3.6 mA /channel.

The OPA2810 can source and sink large amounts of current without degradation in its linearity performance. The wide-bandwidth of the OPA2810 implies that the device has low output-impedance across a wide frequency range, thereby allowing the amplifier to drive capacitive loads up to 35 pF without requiring output isolation. This device is suitable for a wide range of data acquisition, test and measurement front-end buffer, impedance measurement, power analyzer, wideband photodiode transimpedance and signal processing applications.

### 7.2 Functional Block Diagram

The OPA2810 features a true high-impedance input stage including a JFET differential-input pair main stage and a CMOS differential-input auxiliary (Aux) stage operational within 2.5 V of the positive supply voltage. The bias current is limited to a maximum of 20 pA throughout the common-mode input range of the amplifier. [Figure 62](#) shows a block diagram representation for the input stage of the OPA2810.



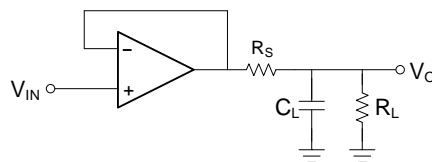
**Figure 62. Input-Stage Block Diagram**

## Functional Block Diagram (continued)

The amplifier exhibits superior performance for high-speed signals (distortion, noise and input offset voltage) while the Aux stage enables rail-to-rail inputs and prevents phase reversal. The OPA2810 also includes input clamps which enable maximum input differential voltage of upto 7 V (lower of 7 V and total supply voltage). This architecture offers significantly greater differential input voltage capability as compared to one to two times the diode forward voltage drop maximum rating in standard amplifiers, and makes this device suitable for use with multiplexers and processing of signals with fast transients. The input bias currents are also clamped to maximum 300  $\mu\text{A}$ , as [Figure 57](#) shows, which does not load the previous driver stage or require current-limiting resistors (except limiting current through the input ESD diodes when input common-mode voltages are greater than the supply voltages). This also enables the use of one of the channels as a comparator in systems which require an amplifier and a comparator for signal-gain and fault-detection, respectively. For the lowest offset, distortion and noise performance, limit the common-mode input voltage to the main JFET-input stage (greater than 2.5 V away from the positive supply).

The OPA2810 is a rail-to-rail output amplifier and swings to either of the rails at the output, as shown in [Figure 16](#) for 10-V supply operation. This is particularly useful for inputs biased near the rails or when the amplifier is configured in a closed-loop gain such that the output approaches the supply voltage. When the output saturates, it recovers with 55 ns when inputs exceed the supply voltages by 0.5 V in an  $G = -1$  V/V inverting gain with a 10-V supply. The outputs are short-circuit protected with the limits of [Figure 17](#).

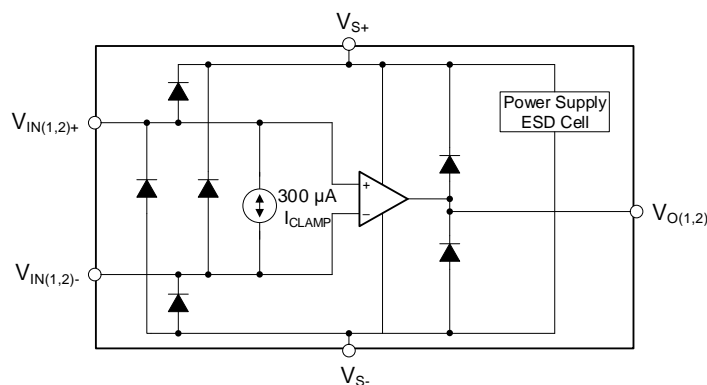
An amplifier phase margin reduces and it becomes unstable when driving a capacitive load ( $C_L$ ) at the output, as [Figure 63](#) shows. Use of a series resistor ( $R_S$ ) between the amplifier output and load capacitance introduces a zero which cancels the pole formed by the amplifier output impedance and  $C_L$  in the open-loop transfer function. The OPA2810 drives capacitive loads of up to 35 pF without causing instability. It is recommended to use a series resistor for larger load capacitance values, as [Figure 4](#) shows for OPA2810 configured as a unity-gain buffer.



**Figure 63. OPA2810 Driving Capacitive Load**

### 7.2.1 ESD Protection

All the device pins are protected with internal ESD protection diodes to the power supplies as [Figure 64](#) shows. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. The differential input clamps only limit the bias current when the input common-mode voltages are within the supply voltage range, whereas current limiting series resistors must be added at the inputs if common-mode voltages higher than the supply voltages are possible. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.



**Figure 64. Internal ESD Protection**

## 7.3 Feature Description

### 7.3.1 OPA2810 Comparison

表 1 lists several members of the device family that includes the OPA2810.

**表 1. Related Operational Amplifier Products**

DEVICE	$V_{S\pm}$ (V)	$I_Q$ / Channel (mA)	GBWP (MHz)	SLEW RATE (V/ $\mu$ s)	VOLTAGE NOISE (nV/ $\sqrt{\text{Hz}}$ )	AMPLIFIER DESCRIPTION
<a href="#">OPA2810</a>	$\pm 12$	3.6	70	192	6	Unity-gain stable FET input (Dual-ch)
<a href="#">THS4631</a>	$\pm 15$	13	210	900	7	Unity-gain stable FET input
<a href="#">OPA656</a>	$\pm 6$	14	230	290	7	Unity-gain stable FET input
<a href="#">OPA657</a>	$\pm 6$	14	1600	700	4.8	Gain of 7 stable FET input
<a href="#">OPA659</a>	$\pm 6$	32	350	2550	8.9	Unity-gain stable FET input

## 7.4 Device Functional Modes

### 7.4.1 Split-Supply Operation ( $\pm 2.375$ V to $\pm 13.5$ V)

To facilitate testing with common lab equipment, the OPA2810 can be configured to allow for split-supply operation (see the [OPA2810DGK Evaluation Module](#)). This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference the inputs and outputs to ground. 图 65 shows the OPA2810 configured as a noninverting amplifier and 图 66 shows the OPA2810 configured as an inverting amplifier. For split-supply operation referenced to ground, the power supplies  $V_{S+}$  and  $V_{S-}$  are symmetrical around ground and  $V_{REF} = \text{GND}$ . Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

### 7.4.2 Single-Supply Operation (4.75 V to 27 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA2810 can be used with a single supply (negative supply set to ground) with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a balanced, single-supply configuration, level shift all the voltages by half the difference between the power-supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the [Single-Supply Op Amp Design Techniques application report](#) for examples of single-supply designs.

## 8 Application and Implementation

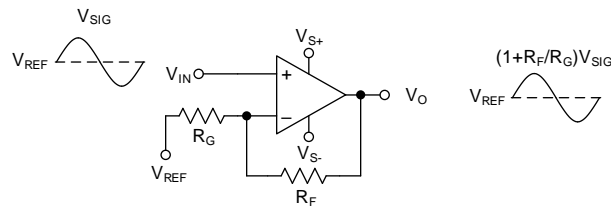
### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

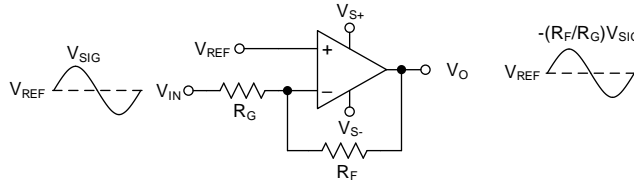
### 8.1 Application Information

#### 8.1.1 Selection of Feedback Resistors

The OPA2810 is a classic voltage feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits include the noninverting and inverting gain configurations as [Figure 65](#) and [Figure 66](#) show. The DC operating point for each configuration is level-shifted by the reference voltage  $V_{REF}$  which is typically set to midsupply in single-supply operation.  $V_{REF}$  is often connected to ground in split-supply applications.



**Figure 65. Noninverting Amplifier**



**Figure 66. Inverting Amplifier**

The closed-loop gain of an amplifier in noninverting configuration is shown in [Equation 1](#).

$$V_O = V_{IN} \left( 1 + \frac{R_F}{R_G} \right) + V_{REF} \quad (1)$$

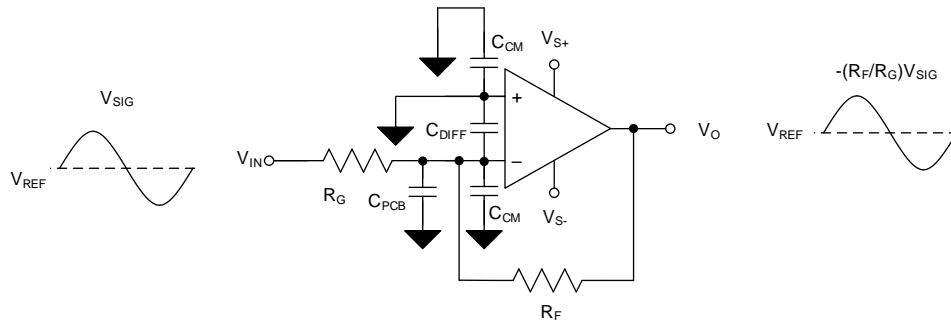
The closed-loop gain of an amplifier in an inverting configuration is shown in [Equation 2](#).

$$V_O = V_{IN} \left( -\frac{R_F}{R_G} \right) + V_{REF} \quad (2)$$

The magnitude of the low-frequency gain is determined by the ratio of the magnitudes of the feedback resistor ( $R_F$ ) and the gain setting resistor  $R_G$ . The order of magnitudes of the individual values of  $R_F$  and  $R_G$  offer a trade-off between amplifier stability, power dissipated in the feedback resistor network, and total output noise. The feedback network increases the loading on the amplifier output. Using large values of the feedback resistors reduces the power dissipated at the amplifier output. On the other hand, this increases the inherent voltage and

## Application Information (continued)

amplifier current noise contribution seen at the output while lowering the frequency at which a pole occurs in the feedback factor ( $\beta$ ). This pole causes a decrease in the phase margin at zero-gain crossover frequency and potential instability. Using small feedback resistors increases power dissipation and also degrades amplifier linearity due to a heavier amplifier output load. [Figure 67](#) shows a representative schematic of the OPA2810 in an inverting configuration with the input capacitors shown.



**Figure 67. Inverting Amplifier with Input Capacitors**

The effective capacitance seen at the amplifier's inverting input pin is shown in [Equation 3](#) which forms a pole in  $\beta$  at a cut-off frequency of [Equation 4](#).

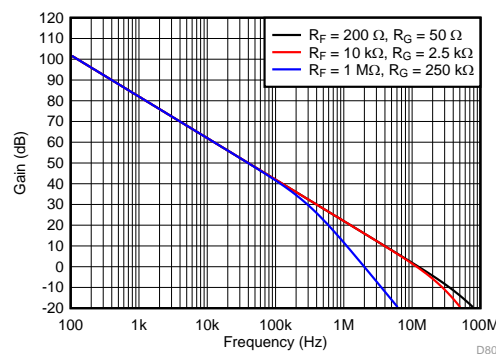
$$C_{IN} = C_{CM} + C_{DIFF} + C_{PCB} \quad (3)$$

$$F_C = \frac{1}{2\pi R_F C_{IN}} \quad (4)$$

where:

- $C_{CM}$  is the amplifier common-mode input capacitance
- $C_{DIFF}$  is the amplifier differential input capacitance
- and,  $C_{PCB}$  is the PCB parasitic capacitance.

For low-power systems, greater the values of the feedback resistors, the earlier in frequency does the phase margin begin to reduce and cause instability. [Figure 68](#) and [Figure 69](#) illustrate the loop gain magnitude and phase plots, respectively, for the OPA2810 simulation in [TINA-TI](#) configured as an inverting amplifier with values of feedback resistors varying by orders of magnitudes.



**Figure 68. Loop-Gain vs. Frequency for Circuit of Figure 67**

## Application Information (continued)

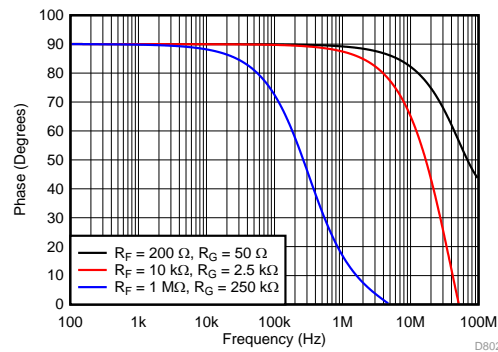


Figure 69. Loop-Gain Phase vs. Frequency for Circuit of Figure 67

A lower phase margin results in peaking in the frequency response and lower bandwidth as Figure 70 shows, which is synonymous with overshoot and ringing in the pulse response results. The OPA2810 offers a flat-band voltage noise density of 6 nV/√Hz. TI recommends selecting an  $R_F$  so the voltage noise contribution does not exceed that of the amplifier. Figure 71 shows the voltage noise density variation with value of resistance at 25°C. A 2-kΩ resistor exhibits a thermal noise density of 5.75 nV/√Hz which is comparable to the flatband noise of the OPA2810. Hence, TI recommends using an  $R_F$  lower than 2 kΩ while being large enough to not dissipate excessive power for the output voltage swing and supply current requirements of the application. The [Noise Analysis and the Effect of Resistor Elements on Total Noise](#) section shows a detailed analysis of the various contributors to noise.

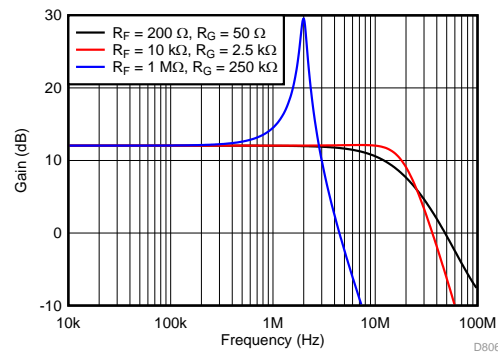


Figure 70. Closed-Loop Gain vs. Frequency for Circuit of Figure 67

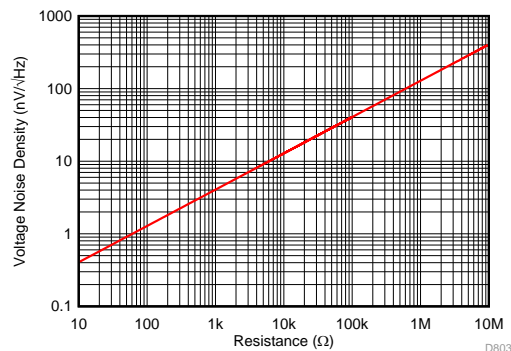
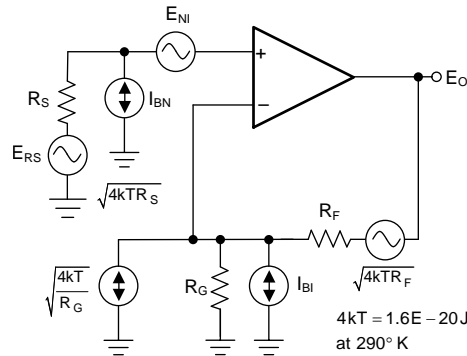


Figure 71. Thermal Noise Density vs Resistance

## Application Information (continued)

### 8.1.2 Noise Analysis and the Effect of Resistor Elements on Total Noise

The OPA2810 provides a low input-referred broadband noise voltage density of 6 nV/√Hz while requiring a low 3.6-mA quiescent supply current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. [Figure 72](#) shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in nV/√Hz or pA/√Hz.



**Figure 72. Operational Amplifier Noise Analysis Model**

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then calculates the square root to get back to a spot noise voltage. [Figure 72](#) shows the general form for this output noise voltage using the terms shown in [Equation 5](#).

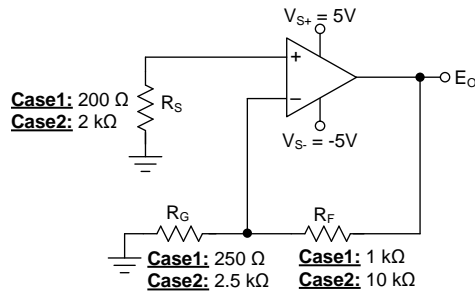
$$E_O = \sqrt{(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (5)$$

Dividing this expression by the noise gain ( $NG = 1 + R_F / R_G$ ) shows the equivalent input referred spot noise voltage at the noninverting input; see [Equation 6](#).

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Substituting large resistor values into [Equation 6](#) can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 2-kΩ adds a Johnson voltage noise term equal to that of the amplifier (6 nV/√Hz).

[Table 2](#) compares the noise contributions from the various terms when the OPA2810 is configured in a noninverting gain of 5V/V as [Figure 73](#) shows. Two cases are considered where the resistor values in case 2 are 10x the resistor values in case 1. The total output noise in case 1 is 31.3 nV/√Hz while the noise in case 2 is 49.7 nV/√Hz. The large value resistors in case 2 dilute the benefits of selecting a low noise amplifier like the OPA2810. To minimize total system noise, reduce the size of the resistor values. This increases the amplifiers output load and results in a degradation of distortion performance. The increased loading increases the dynamic power consumption of the amplifier. The circuit designer must make the appropriate tradeoffs to maximize the overall performance of the amplifier to match the system requirements.

**Application Information (continued)**

**图 73. Comparing Noise Contributors for Two Cases With the Amplifier in a Noninverting Gain of 5 V/V**
**表 2. Comparing Noise Contributions for the Circuit in 图 73**

Noise Source	Output Noise Equation	Case1				Case2			
		Noise Source Value	Voltage Noise Contribution (nV/√Hz)	Noise Power Contribution (nV <sup>2</sup> /Hz)	Contribution (%)	Noise Source Value	Voltage Noise Contribution (nV/√Hz)	Noise Power Contribution (nV <sup>2</sup> /Hz)	Contribution (%)
Source resistor, $R_S$	$E_{RS} (1+R_F/R_G)$	$1.82 \text{ nV}/\sqrt{\text{Hz}}$	9.1	82.81	7.77	$5.76 \text{ nV}/\sqrt{\text{Hz}}$	28.8	829.44	32.41
Gain resistor, $R_G$	$E_{RG} (R_F/R_G)$	$2.04 \text{ nV}/\sqrt{\text{Hz}}$	8.16	66.59	6.24	$6.44 \text{ nV}/\sqrt{\text{Hz}}$	25.76	663.58	25.93
Feedback resistor, $R_F$	$E_{RF}$	$4.07 \text{ nV}/\sqrt{\text{Hz}}$	4.07	16.57	1.55	$12.87 \text{ nV}/\sqrt{\text{Hz}}$	12.87	165.64	6.47
Amplifier voltage noise, $E_{NI}$	$E_{NI} (1+R_F/R_G)$	$6 \text{ nV}/\sqrt{\text{Hz}}$	30	900	84.43	$6 \text{ nV}/\sqrt{\text{Hz}}$	30	900	35.17
Inverting current noise, $I_{BI}$	$I_{BI} (R_F    R_G)$	$5 \text{ fA}/\sqrt{\text{Hz}}$	5.0E-3	—	—	$5 \text{ fA}/\sqrt{\text{Hz}}$	50E-3	—	—
Noninverting current noise, $I_{BN}$	$I_{BN} R_S (1+R_F/R_G)$	$5 \text{ fA}/\sqrt{\text{Hz}}$	1.0E-3	—	—	$5 \text{ fA}/\sqrt{\text{Hz}}$	10E-3	—	—



## 8.2 Typical Applications

### 8.2.1 Transimpedance Amplifier

The high GBWP and low input voltage and current noise for the OPA2810 make it an ideal wideband transimpedance amplifier for moderate to high transimpedance gains.

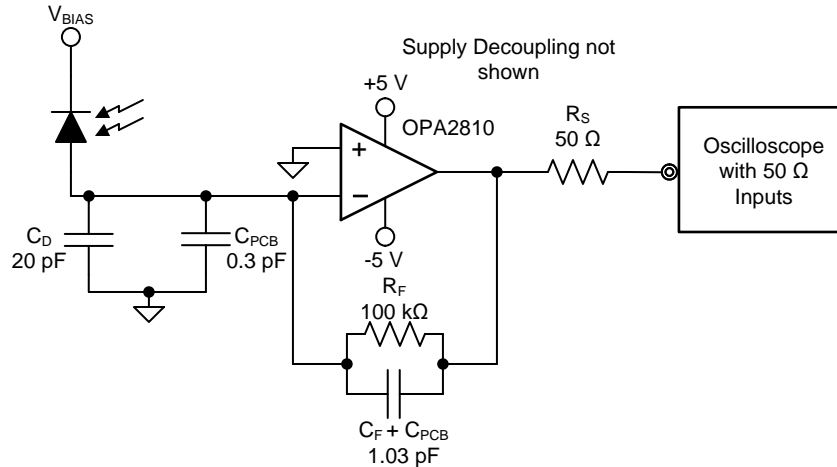


图 74. Wideband, High-Sensitivity, Transimpedance Amplifier

#### 8.2.1.1 Design Requirements

Design a high-bandwidth, high-gain transimpedance amplifier with the design requirements listed in 表 3.

表 3. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (KΩ)	PHOTODIODE CAPACITANCE (pF)
> 2	100	20

#### 8.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA2810. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance ( $C_D$ ) with the reverse bias voltage ( $V_{BIAS}$ ) applied, the desired transimpedance gain,  $R_F$ , and the GBWP for the OPA2810 (70 MHz). 图 74 shows a transimpedance circuit with the parameters as described in 表 3. With these three variables set (and including the parasitic input capacitance for the OPA2810 and the PCB added to  $C_D$ ), the feedback capacitor value ( $C_F$ ) may be set to control the frequency response. [Transimpedance Considerations for High-Speed Amplifiers application report](#) discusses using high-speed amplifiers for transimpedance applications. To achieve a maximally-flat second-order Butterworth frequency response, set the feedback pole to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBWP}{4\pi R_F C_D}} \quad (7)$$

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (2.5 + 0.5) pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3 pF. Using 式 3, this results in a total input capacitance of  $C_D = 23.3$  pF. From 式 7, set the feedback pole at 1.55 MHz. Setting the pole at 1.55 MHz requires a total feedback capacitance of 1.03 pF.

The approximate –3-dB bandwidth of the transimpedance amplifier circuit is shown in:

$$f_{-3dB} = \sqrt{GBWP / (2\pi R_F C_D)} \text{ Hz} \quad (8)$$

式 8 estimates a closed-loop bandwidth of 2.19 MHz. 図 75 and 図 76 show the loop-gain magnitude and phase plots from the TINA-TI simulations of the transimpedance amplifier circuit of 図 74. The  $1/\beta$  gain curve has a zero from  $R_F$  and  $C_{IN}$  at 70 kHz and a pole from  $R_F$  and  $C_F$  cancelling the  $1/\beta$  zero at 1.5 MHz resulting in a 20 dB/decade rate-of-closure at the loop gain crossover frequency (frequency where  $A_{OL} = 1/\beta$ ), ensuring a stable circuit. A phase margin of  $62^\circ$  is obtained with a closed-loop bandwidth of 3 MHz and a 100-k $\Omega$  transimpedance gain.

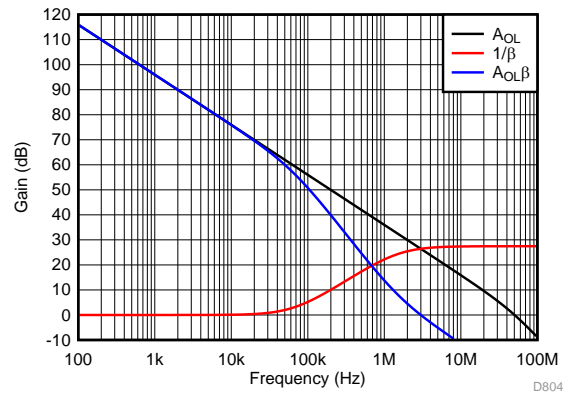


図 75. Loop-Gain Magnitude vs Frequency for Transimpedance Amplifier Circuit of 図 74

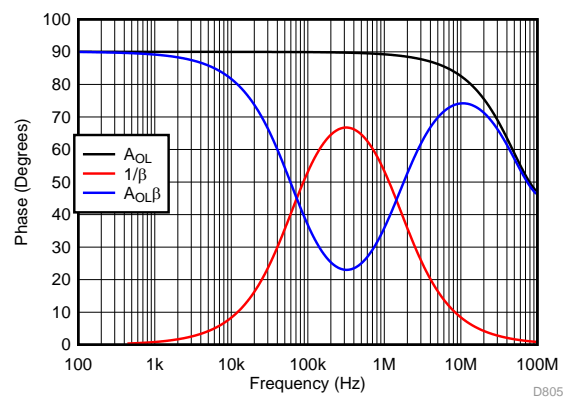
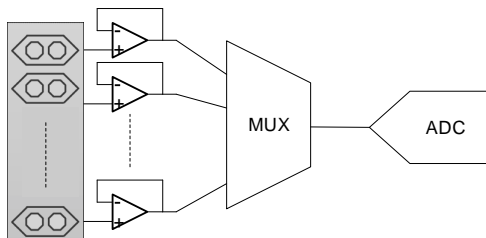


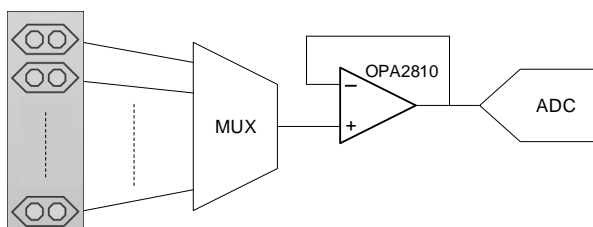
図 76. Loop-Gain Phase vs Frequency for Transimpedance Amplifier Circuit of 図 74

## 8.2.2 Multichannel Sensor Interface

High-Z input amplifiers are particularly useful when interfaced with sensors that have relatively high output impedance. Such multichannel systems usually interface these sensors with the signal chain through a multiplexer. [Figure 77](#) shows one such implementation using an amplifier for interface with each sensor, and driving into an ADC through a multiplexer. An alternate circuit, shown in [Figure 78](#), may use a single higher GBWP and fast-settling amplifier at the output of the multiplexer. This gives rise to large signal transients when switching between channels, where the settling performance of the amplifier and maximum allowed differential input voltage limits signal chain performance and amplifier reliability, respectively.

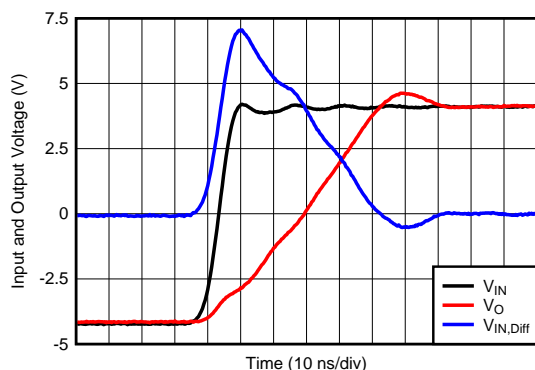


**Figure 77. Multichannel Sensor Interface Using Multiple Amplifiers**



**Figure 78. Multichannel Sensor Interface Using a Single Higher GBWP Amplifier**

[Figure 79](#) shows the output voltage and input differential voltage when a 8-V step is applied at the noninverting terminal of the OPA2810 configured as a unity-gain buffer of [Figure 78](#).



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**Figure 79. Large-Signal Transient Response Using OPA2810**

Because of the fast input transient, the amplifier is slew-limited and the inputs cease to track each other (a maximum  $V_{IN,Diff}$  of 7V is seen in [Figure 79](#)) until the output reaches its final value and the negative feedback loop is closed. For standard amplifiers with a 0.7-1.5V maximum  $V_{IN,Diff}$  rating, it is required to use current-limiting resistors in series with the input pins to protect from irreversible damage, which also limits the device frequency response. The OPA2810 has built-in input clamps that allow the application of as much as 7V of  $V_{IN,Diff}$ , with no external resistors required and no damage to the device or a shift in performance specifications. Such an input-stage architecture coupled, with its fast settling performance, makes the OPA2810 a good fit for multichannel sensor multiplexed systems.

## 9 Power Supply Recommendations

The OPA2810 is intended for operation on supplies ranging from 4.75 V to 27 V. The OPA2810 may be operated on single-sided supplies, split and balanced bipolar supplies or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance ( $< 0.1''$ ) from the power supply pins to high-frequency, 0.01- $\mu\text{F}$  decoupling capacitors. A larger capacitor (2.2  $\mu\text{F}$  typical) is used along with a high-frequency, 0.01- $\mu\text{F}$  supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split-supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

## 10 Layout

### 10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA2810 requires careful attention to board layout parasitics and external component types. The [OPA2810EVM](#) can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** ( $< 0.1''$ ) from the power-supply pins to high-frequency 0.01- $\mu\text{F}$  decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2- $\mu\text{F}$  to 6.8- $\mu\text{F}$ ) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high frequency performance of the OPA2810.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values  $> 10\text{ k}\Omega$ , this parasitic capacitance can add a pole or zero close to the GBWP of 70 MHz and subsequently affects circuit operation. Keep resistor values as low as possible consistent with load driving considerations. Lowering the resistor values keep the resistor noise terms low, and minimize the effect of its parasitic capacitance, however lower resistor values increase the dynamic power consumption because  $R_F$  and  $R_G$  become part of the amplifiers output load network. Transimpedance applications (see the [Transimpedance Amplifier](#) section) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set  $R_S$  for sufficient phase margin and stability. Low parasitic capacitive loads ( $< 35\text{ pF}$ ) may not need an  $R_S$  because the OPA2810 is nominally compensated to operate with a 35-pF parasitic load. Higher parasitic capacitive loads without an  $R_S$  are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is

## Layout Guidelines (continued)

required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and a higher impedance environment improves distortion. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2810 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device— this total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value to obtain sufficient phase margin and stability. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, the signal attenuates because of the voltage divider formed by the series output into the terminating impedance.

5. **Take care to design the PCB layout for optimal thermal dissipation.** For the extreme case of 125°C operating ambient, using the approximate maximum 177.2°C/W for the two packages, and an internal power of 24-V supply × 9-mA 125°C supply current (both amplifiers) gives a maximum internal power dissipation of 216 mW. This power gives a 38°C increase from ambient to junction temperature. Load power adds to this value and this dissipation must also be calculated to determine the worst-case safe operating point.
6. **Socketing a high speed part like the OPA2810 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2810 onto the board.

### 10.1.1 Thermal Considerations

The OPA2810 does not require heat sinking or airflow in most applications. Maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature ( $T_J$ ) is given by  $T_A + P_D \times \theta_{JA}$ . The total internal power dissipation ( $P_D$ ) is the sum of quiescent power ( $P_{DQ}$ ) and additional power dissipated in the output stage ( $P_{DL}$ ) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part.  $P_{DL}$  depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to half of either supply voltage (for equal split-supplies). Under this condition  $P_{DL} = V_S^2 / (4 \times R_L)$  where  $R_L$  includes feedback network loading.

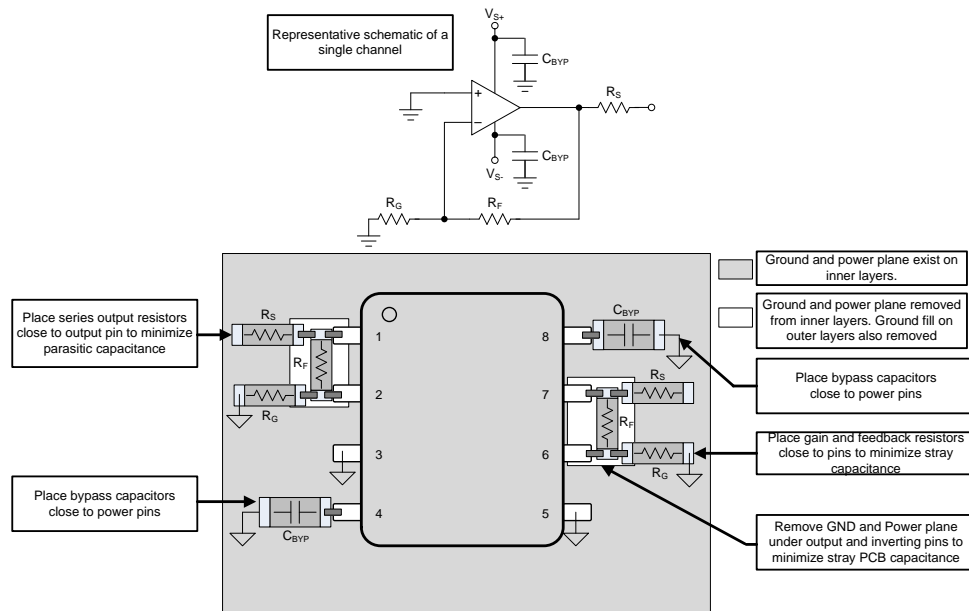
The power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum  $T_J$  using an OPA2810-DGK (VSSOP package) configured as a unity gain buffer, operating on ±12-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$$P_D = 24 \text{ V} \times 9 \text{ mA} + 12^2 / (4 \times 500 \text{ } \Omega) = 288 \text{ mW}$$

Maximum  $T_J = 25^\circ\text{C} + (0.288 \text{ W} \times 177.2^\circ\text{C/W}) = 76^\circ\text{C}$ , which is well below the maximum allowed junction temperature of 150°C.

## 10.2 Layout Example



**80. Layout Recommendation**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[OPA2810DGK 評価モジュール](#)』ユーザー・ガイド
- テキサス・インスツルメンツ、『[単一電源オペアンプの設計テクニック](#)』アプリケーション・レポート
- テキサス・インスツルメンツ、『[高速アンプのトランスインピーダンスに関する考慮事項](#)』アプリケーション・レポート
- テキサス・インスツルメンツ、『[ブログ: トランスインピーダンス・アンプについて知っておくべきこと—第1部](#)』
- テキサス・インスツルメンツ、『[ブログ: トランスインピーダンス・アンプについて知っておくべきこと—第2部](#)』
- テキサス・インスツルメンツ、『[高速オペアンプのノイズ解析](#)』アプリケーション・レポート
- テキサス・インスツルメンツ、[TINAモデルとシミュレーション・ツール](#)

#### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

#### 11.4 商標

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#### 11.5 静電気放電に関する注意事項



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#### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2810IDCNR</a>	Active	Production	SOT-23 (DCN)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2810
OPA2810IDCNR.B	Active	Production	SOT-23 (DCN)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2810
<a href="#">OPA2810IDCNT</a>	Active	Production	SOT-23 (DCN)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2810
OPA2810IDCNT.B	Active	Production	SOT-23 (DCN)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2810
<a href="#">OPA2810IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2810
OPA2810IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2810
<a href="#">OPA2810IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	2810
OPA2810IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2810
<a href="#">OPA2810IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2810
OPA2810IDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2810
<a href="#">OPA2810IDT</a>	Active	Production	SOIC (D)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2810
OPA2810IDT.B	Active	Production	SOIC (D)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2810

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2810IDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA2810IDCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA2810IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2810IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2810IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2810IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2810IDT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

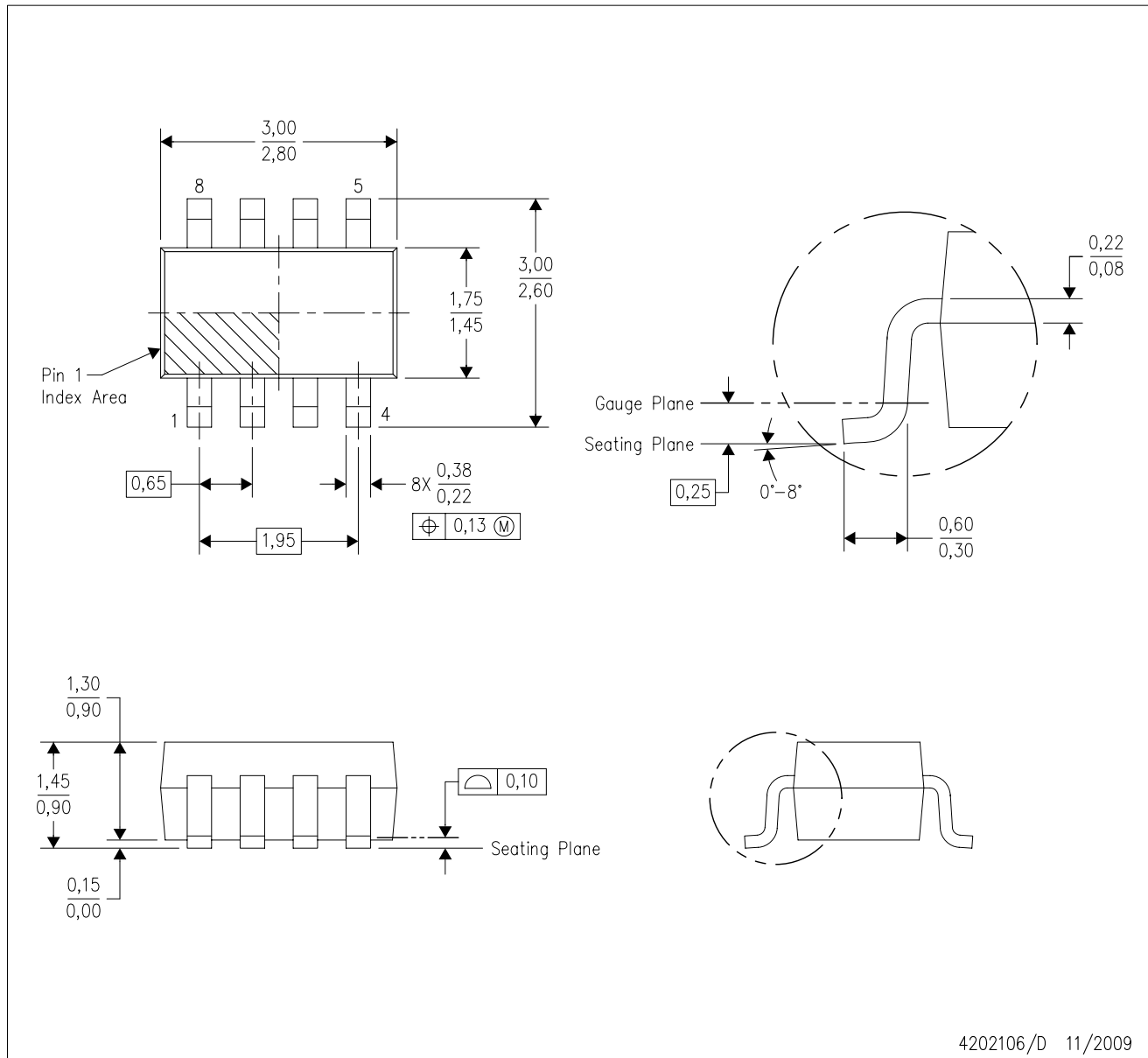


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2810IDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
OPA2810IDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2810IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2810IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2810IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2810IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2810IDT	SOIC	D	8	250	213.0	191.0	35.0

DCN (R-PDSO-G8)

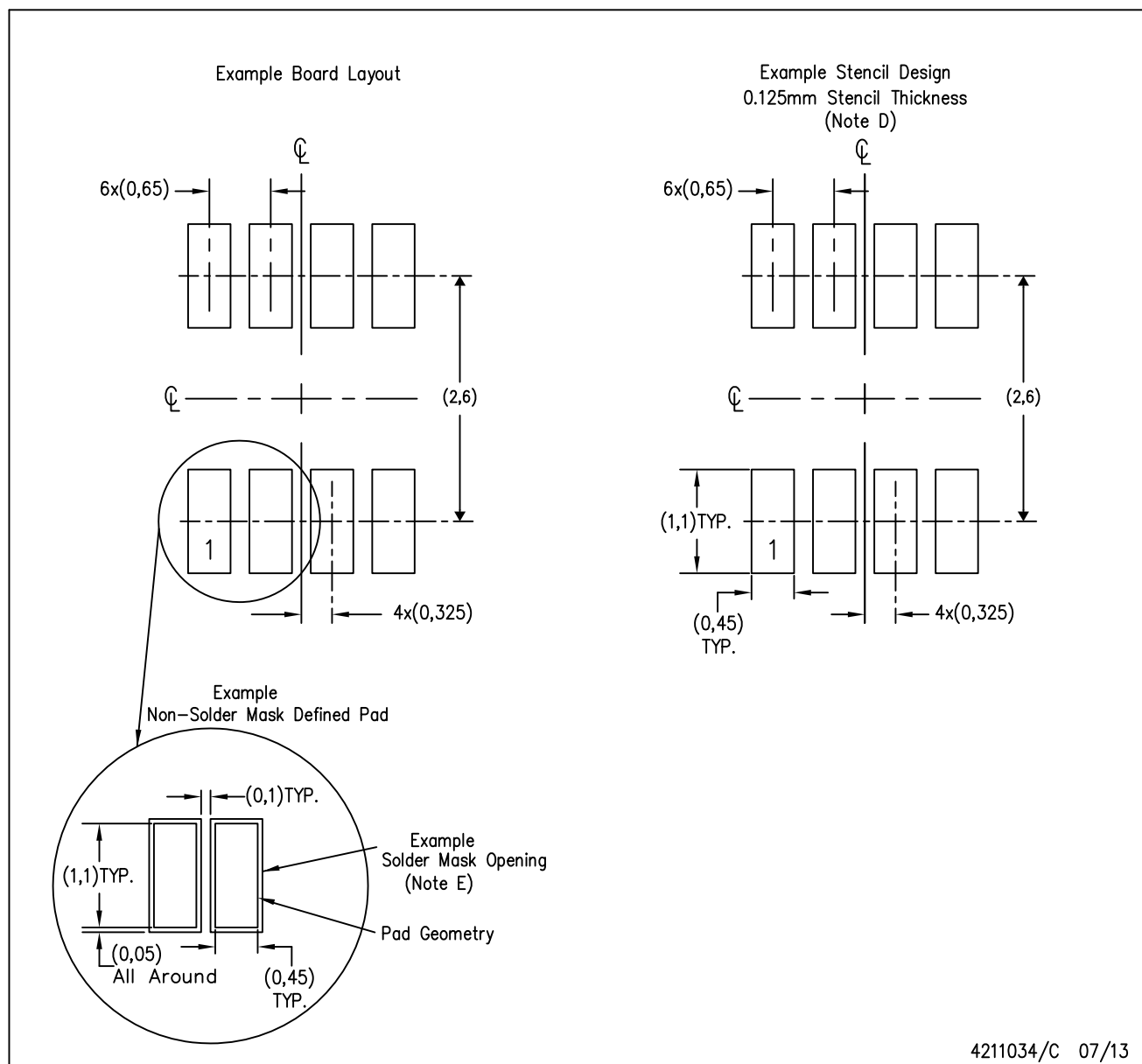
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

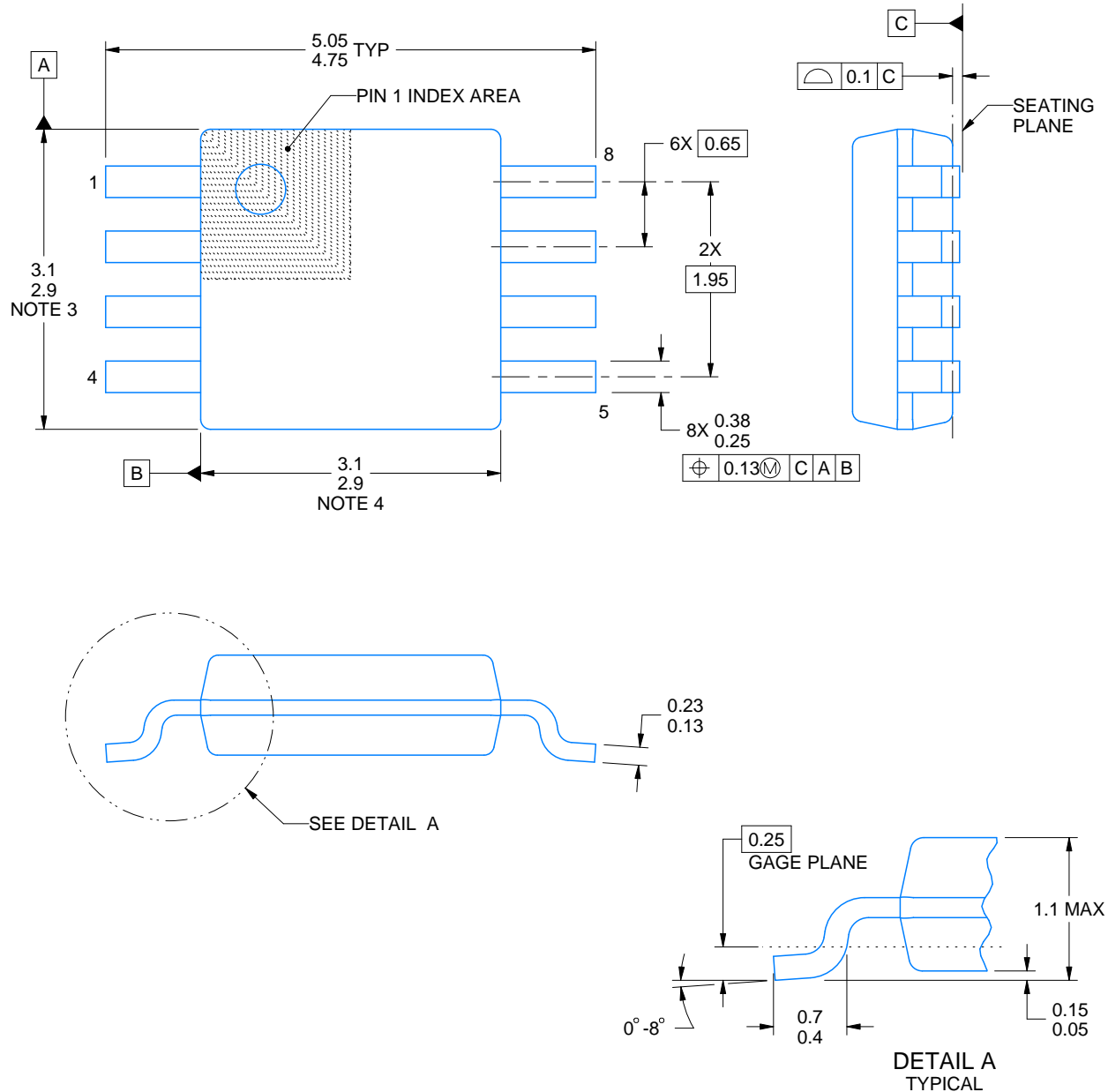
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



**DGK0008A****PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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