OPAx241、OPAx251 単一電源、マイクロパワー オペアンプ

1 特長

- 5V 電源用に最適化された OPAx241 ファミリ
- ±15V 電源用に最適化された OPAx251 ファミリ
- マイクロパワー: I_Q = 25µA
- 単一電源動作
- レール ツー レール出力 (50mV 以内)
- 広い電源電圧範囲
  - シングル電源:2.7V～36V
  - デュアル電源:±1.35V～±18V
- 低いオフセット電圧:±250µV (最大値)
- 大きい同相除去:124dB
- 高いオープン ループ ゲイン:128dB
- シングル、デュアル、クワッド

2 アプリケーション

- バッテリ駆動機器
- 携帯機器
- 医療機器
- 試験用機器

3 概要

OPA241、OPA2241、OPA4241 (OPAx241)、および OPA251、OPA2251、OPA4251 (OPAx251) デバイスは、バッテリ駆動の携帯アプリケーション用に設計されています。これらのアンプは、非常に低い消費電力 (25µA) に加え、低いオフセット電圧、レール ツー レール出力スイング、高い同相除去、高い開ループ ゲインを特長としています。

OPAx241 シリーズは低電源電圧で動作するように最適化されており、OPAx251 シリーズは高電源用に最適化されています。どちらのシリーズにも、単一電源 (2.7V～36V) またはデュアル電源 (±1.35V～±18V) を使用できます。入力同相電圧範囲は、負電源より 200mV 低い電圧まで拡張されており、単一電源アプリケーションに最適です。

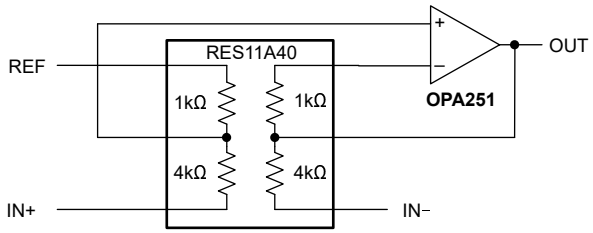
OPAx241 および OPAx251 は、ユニティ ゲイン安定で、大きな容量性負荷を駆動できます。設計上の特別な考慮事項により、これらの製品は使いやすくなっています。アンプが規定された制限までスイングしても、高い性能が維持されます。初期オフセット電圧 (最大 ±250µV) は非常に低いため、ユーザーによる調整は通常必要ありません。ただし、特殊なアプリケーション用に外部トリム ピンが提供されています (シングル バージョンのみ)。

OPAx241 および OPAx251 は、-40℃～+85℃で仕様が規定されており、-55℃～+125℃で動作します。

製品情報

部品番号	チャネル	パッケージ (1)
OPA241	シングル	D (SOIC、8)
		P (PDIP、8)
OPA2241	デュアル	D (SOIC、8)
		P (PDIP、8)
OPA4241	クワッド	N (PDIP、14)
		D (SOIC、14)
OPA251	シングル	D (SOIC、8)
OPA2251	デュアル	P (PDIP、8)
		D (SOIC、8)
OPA4251	クワッド	D (SOIC、14)

(1) 詳細については、セクション 9 を参照してください。



高同相モード、低電力差動アンプ

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4 Pin Configuration and Functions

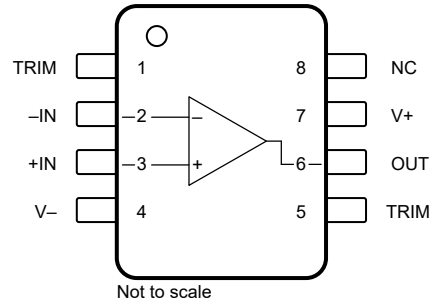


図 4-1. OPA241 and OPA251: D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions: OPA241 and OPA251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	2	Input	Inverting input
NC	8	—	No internal connection (can be left floating)
OUT	6	Output	Output
TRIM	1, 5	—	External offset voltage adjustment. See セクション 6.1.2.
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

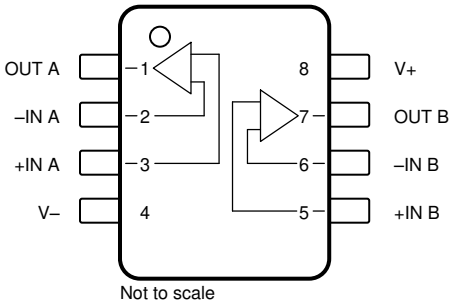


図 4-2. OPA2241 and OPA2251: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

表 4-2. Pin Functions: OPA2241 and OPA2251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

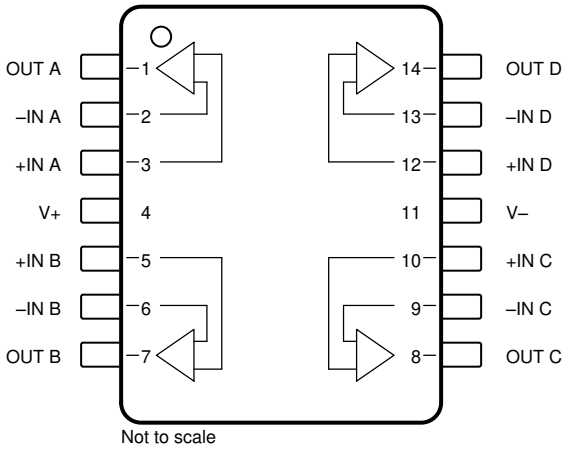


図 4-3. OPA4241 and OPA4251: D Package, 14-Pin SOIC (Top View)

Pin Functions: OPA4241 and OPA4251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply		36	V
		Dual supply		±18	
	Signal input pin voltage	Common-mode(2)	(V–) – 0.5	(V+) + 0.5	V
		Differential(3)		±0.5	
	Output short-circuit(4)		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power supply rails. Current-limit input signals that can swing more that 0.5V beyond the supply rails to 5mA or less.
(3) Input terminals are anti-parallel diode-clamped to each other. Current-limit input signals that cause differential voltage swings of more than ±0.5V to 5mA or less.
(4) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	2.7	30	36	V
		Dual supply	±1.35	±15	±18	
T_A	Operating temperature		–40		+85	°C

5.3 Thermal Information for OPA241 and OPA251

THERMAL METRIC(1)		OPA241 AND OPA251		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.4	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.1	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.2	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information for OPA2241 and OPA2251

THERMAL METRIC(1)		OPA2241 AND OPA2251		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.0	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.3	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.4	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for OPA4241 and OPA4251

THERMAL METRIC(1)		OPA4241 AND OPA4251		UNIT
		D (SOIC)	P (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics for V_S = 2.7V to 5V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx241			±50	±250	µV
			T_A = –40°C to +85°C		±100	±400	
		OPAx251			±100		
			T_A = –40°C to +85°C		±130		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	OPAx241		±0.4		µV/°C
			OPAx251		±0.6		
PSRR	Power supply rejection ratio	V_S = 2.7V to 36V			±3	±30	µV/V
			T_A = –40°C to +85°C			±30	
	Channel separation, (dual, quad)				0.3		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				–4	–20	nA
		T_A = –40°C to +85°C				–25	
I_{OS}	Input offset current				±0.1	±2	nA
		T_A = –40°C to +85°C				±2	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.7		$µV_{PP}$
e_n	Input voltage noise density	f = 1kHz			65		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1kHz			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			–0.2		(V+) – 0.8	V
CMRR	Common-mode rejection ratio	–0.2V < V_{CM} < (V+) – 0.8V		80	106		dB
		0V < V_{CM} < (V+) – 0.8V, T_A = –40°C to +85°C		80			
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			10 || 3.75		MΩ || pF
		Common-mode			1 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 100mV < V_O < (V+) – 100mV		100	120		dB
			T_A = –40°C to +125°C	100			
		(V–) + 200mV < V_O < (V+) – 200mV, R_L = 10kΩ		100	120		
			T_A = –40°C to +125°C	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				35		kHz
SR	Slew rate	V_S = 5V, G = 1V/V			0.01		V/µs
	Overload recovery time	V_S = V_{IN} × G			80		µs

5.6 Electrical Characteristics for V_S = 2.7V to 5V (続き)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail(2)	A_{OL} > 70dB			50		mV
		A_{OL} > 100dB			75	100	
			T_A = –40°C to +85°C			100	
		A_{OL} > 100dB, R_L = 10kΩ,			100	200	
			T_A = –40°C to +85°C			200	
I_{SC}	Short-circuit current	Source, V_S = 5V	Single		4		mA
			Dual and Quad		4		
		Sink, V_S = 5V	Single		–24		
			Dual and Quad		–24		
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			±25	±30	µA
			T_A = –40°C to +85°C			±36	

(1) The negative sign indicates input bias current flows out of the input terminals.
(2) Output voltage swings are measured between the output and power supply rails.

5.7 Electrical Characteristics for V_S = ±15V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx241			±100		µV
			T_A = –40°C to +85°C		±150		
		OPAx251			±50	±250	
			T_A = –40°C to +85°C		±100	±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	OPAx241		±0.6		µV/°C
			OPAx251		±0.5		
PSRR	Power supply rejection ratio	V_S = 2.7V to 36V			±3	±30	µV/V
			T_A = –40°C to +85°C			±30	
	Channel separation, (dual, quad)				0.3		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				–4	–20	nA
		T_A = –40°C to +85°C				–25	
I_{OS}	Input offset current				±0.1	±2	nA
		T_A = –40°C to +85°C				±2	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.7		$µV_{PP}$
e_n	Input voltage noise density	f = 1kHz			65		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1kHz			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 0.8	V
CMRR	Common-mode rejection ratio	–15.2V < V_{CM} < (V+) – 14.2V		100	124		dB
		–15V < V_{CM} < (V+) – 14.2V	T_A = –40°C to +85°C	100			
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			10 || 3.75		MΩ || pF
		Common-mode			1 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 250mV < V_O < (V+) – 250mV		100	128		dB
			T_A = –40°C to +85°C	100			
		(V–) + 300mV < V_O < (V+) – 300mV, R_L = 20kΩ		100	128		
			T_A = –40°C to +85°C	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				30		kHz
SR	Slew rate	V_S = 5V, G = 1V/V			0.01		V/µs
	Overload recovery time	V_S = V_{IN} × G			75		µs

5.7 Electrical Characteristics for V_S = ±15V (続き)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail(2)	A_{OL} > 100dB			50		mV
		A_{OL} > 100dB			75	250	
			T_A = –40°C to +85°C			250	
		A_{OL} > 100dB, R_L = 20kΩ,			100	300	
			T_A = –40°C to +85°C			300	
I_{SC}	Short-circuit current	Source	Single		4		mA
			Dual		4		
		Sink	Single		–21		
			Dual		–27		
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			±27	±38	µA
			T_A = –40°C to +85°C			±45	

(1) The negative sign indicates input bias current flows out of the input terminals.
(2) Output voltage swings are measured between the output and power supply rails.

5.8 Typical Characteristics

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

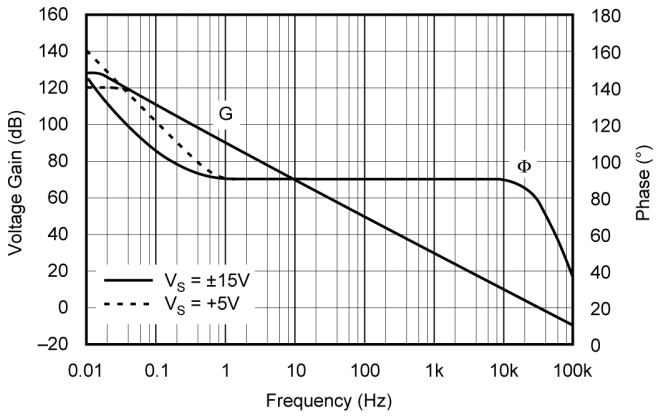


図 5-1. Open-Loop Gain and Phase vs Frequency

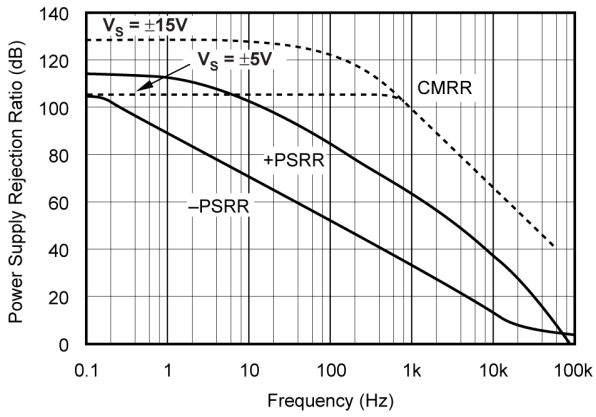


図 5-2. Power Supply and Common-mode Rejection Ratio vs Frequency

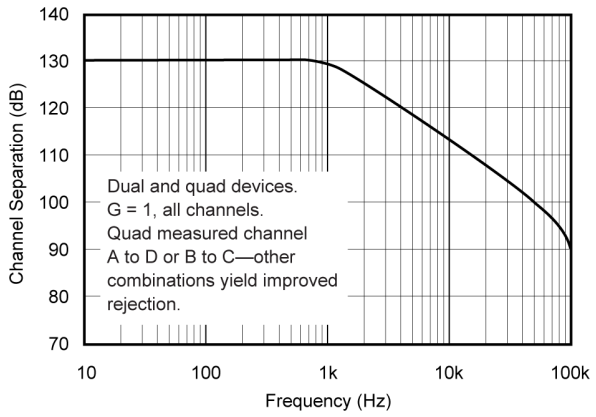


図 5-3. Channel Separation vs Frequency

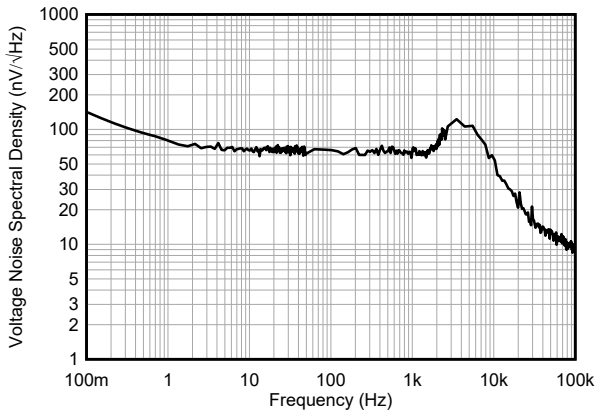


図 5-4. Input Voltage Noise Spectral Density vs Frequency

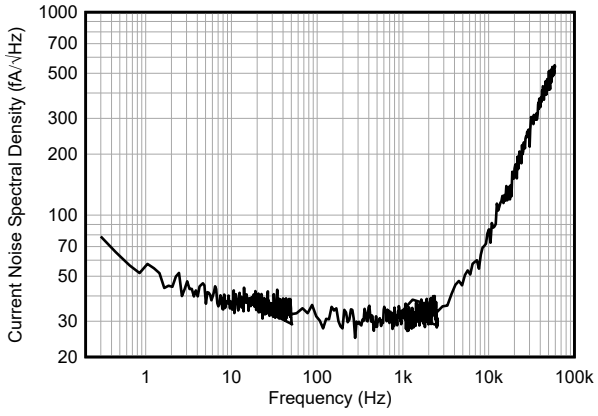


図 5-5. Input Current Noise Spectral Density vs Frequency

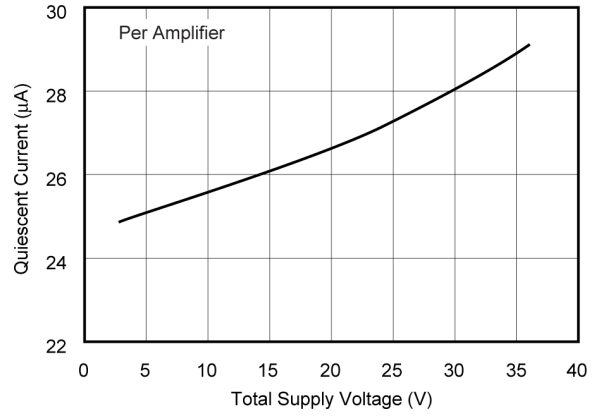


図 5-6. Quiescent Current vs Supply Voltage

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

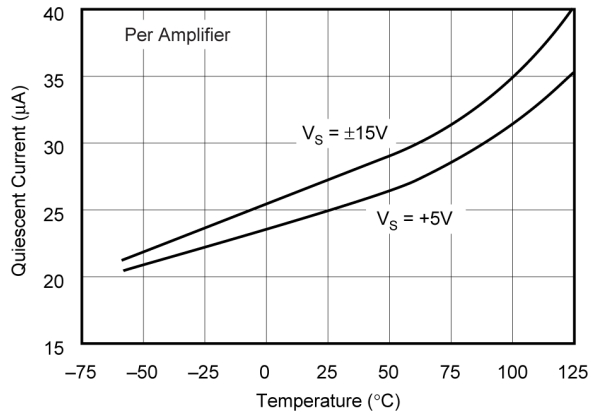


図 5-7. Quiescent Current vs Temperature

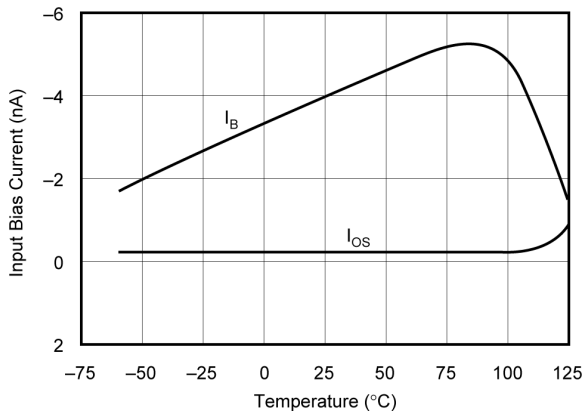


図 5-8. Input Bias Current vs Temperature

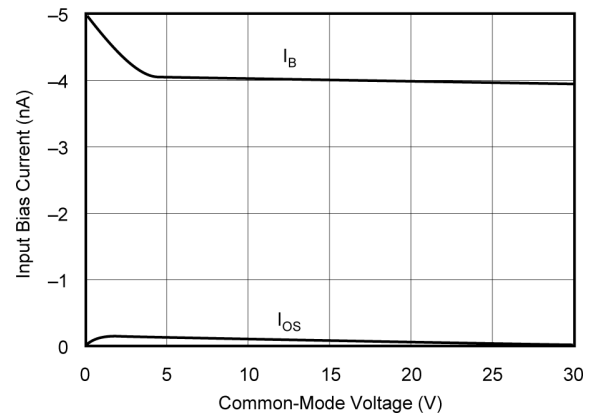


図 5-9. Input Bias Current vs Input Common-mode Voltage

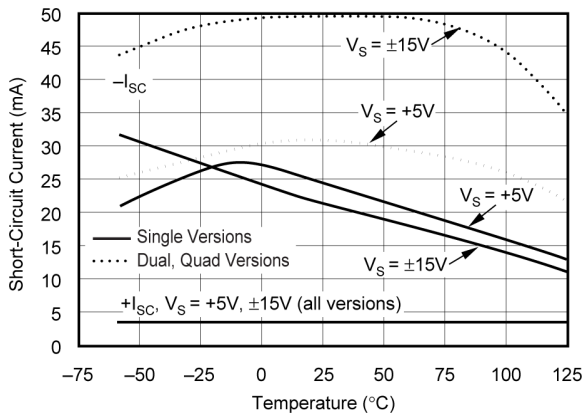


図 5-10. Short-circuit Current vs Temperature

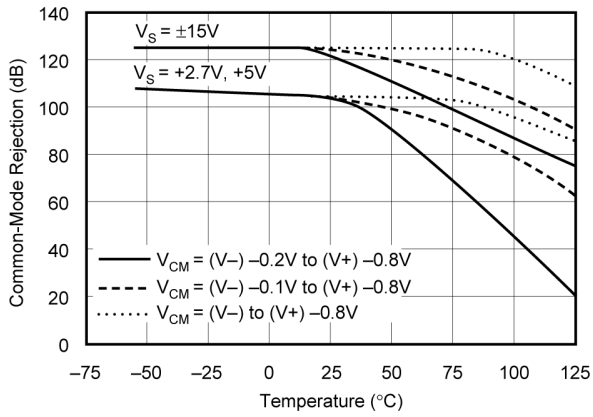


図 5-11. Common-mode Rejection vs Temperature

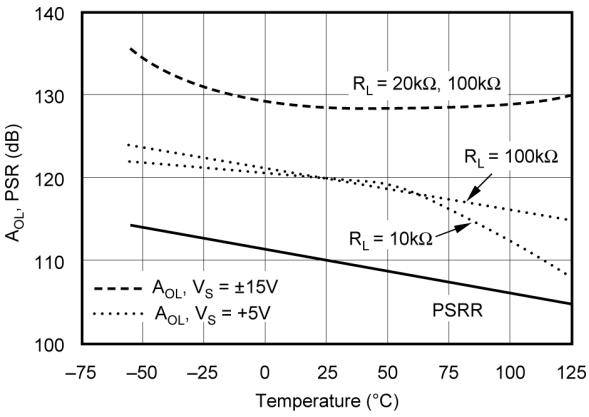


図 5-12. Open-loop Gain and Power Supply Rejection vs Temperature

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

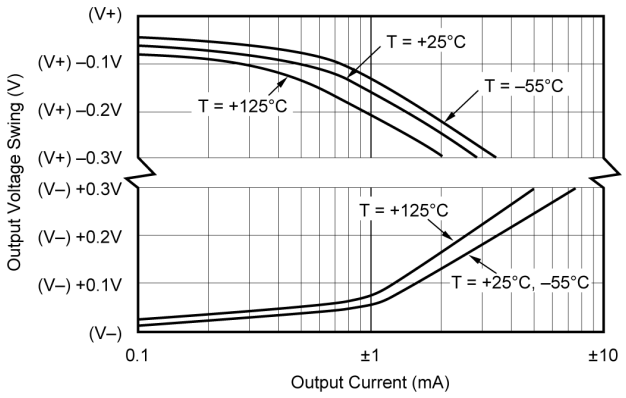


図 5-13. Output Voltage Swing vs Output Current

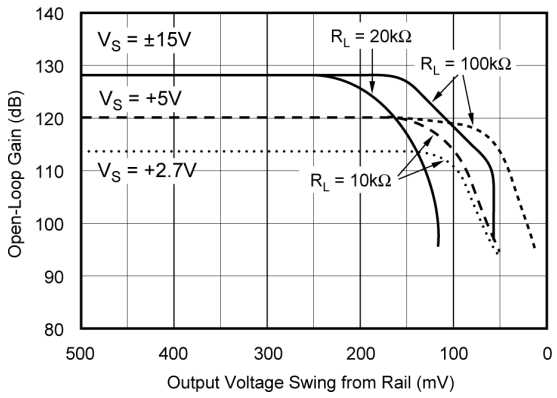


図 5-14. Open-loop Gain vs Output Voltage Swing

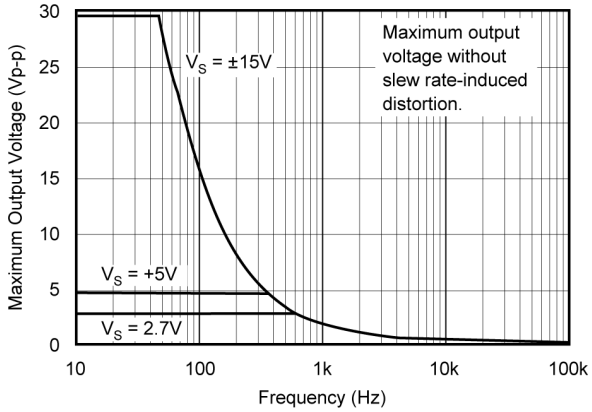


図 5-15. Maximum Output Voltage vs Frequency

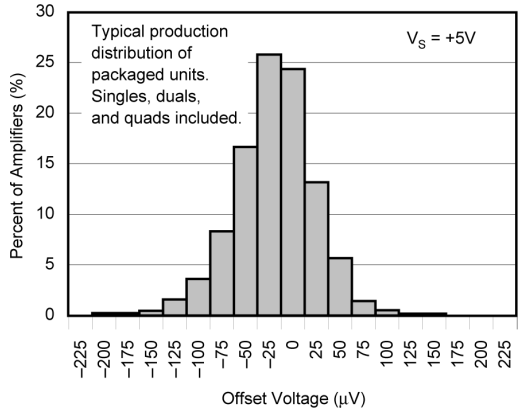


図 5-16. OPA241 Series Offset Voltage Production Distribution

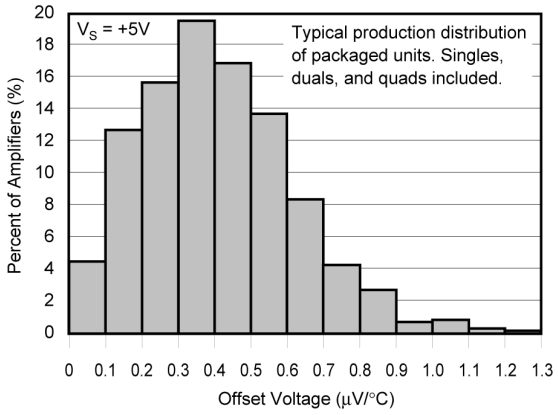


図 5-17. OPA241 Series Offset Voltage Drift Production Distribution

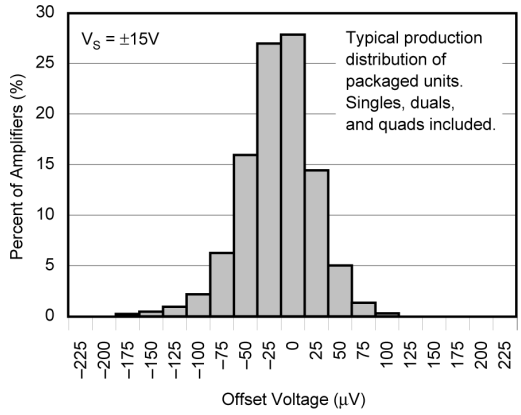


図 5-18. OPA251 Series Offset Voltage Production Distribution

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

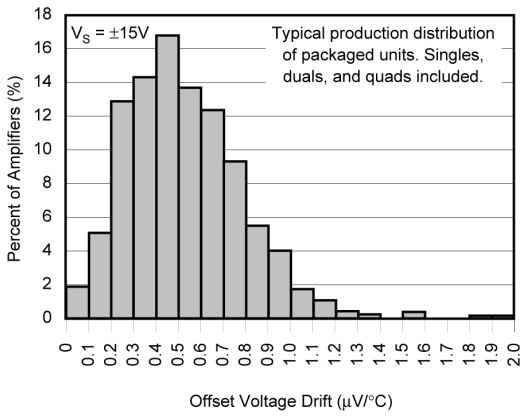


図 5-19. OPA251 Series Offset Voltage Drift Production Distribution

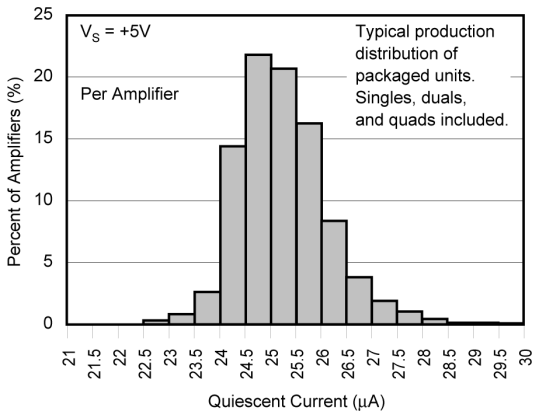


図 5-20. Quiescent Current Product Distribution

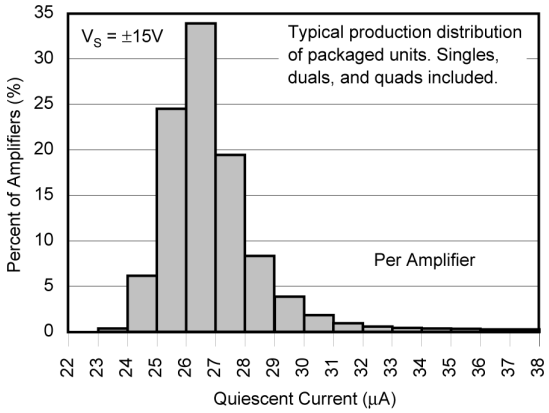
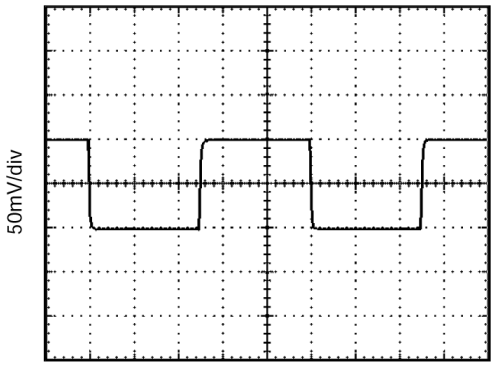
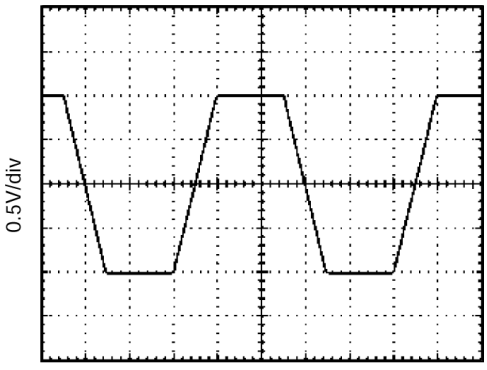


図 5-21. Quiescent Current Production Distribution



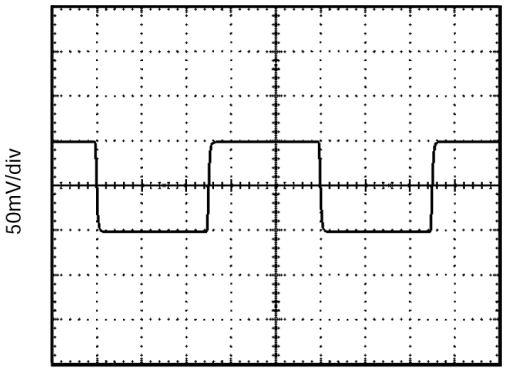
V_S = 5V, G = +1, R_L = 100kΩ, C_L = 100pF

図 5-22. OPA241 Small-Signal Step Response



V_S = 5V, G = + 1, R_L = 100kΩ, C_L = 100pF

図 5-23. OPA241 Large-Signal Step Response

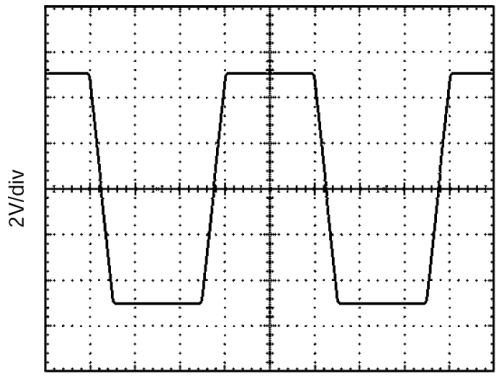


V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF

図 5-24. OPA251 Small-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)



V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF

図 5-25. OPA251 Large-Signal Step Response

6 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

6.1 Applications Information

The OPAx241 and OPAx251 series are unity-gain stable and designed for a wide range of general-purpose applications. Bypass power-supply pins with 0.01µF ceramic capacitors.

6.1.1 Operating Voltage

The OPAx241 series is laser-trimmed for low offset voltage and drift at a low supply voltage (V_S = 5V). The OPAx251 series is trimmed for ±15V operation. Both series operate over the full voltage range (2.7V to 36V or ±1.35V to ±18V) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are production tested over the specified temperature range of −40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. The typical characteristics curves show parameters that vary significantly with operating voltage or temperature.

6.1.2 Offset Voltage Trim

As previously mentioned, the OPAx241 series offset voltage is laser-trimmed at 5V. The OPAx251 series is trimmed at ±15V. The initial offset is so low that user adjustment is usually not required. However, the OPA241 and OPA251 (single op-amp versions) provide offset voltage trim connections on pins 1 and 5. 図 6-1shows how the offset voltage can be adjusted by connecting a potentiometer. Only use this adjustment to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset can degrade the offset drift behavior of the op amp. While predicting the exact change in drift is not possible, the effect is usually small.

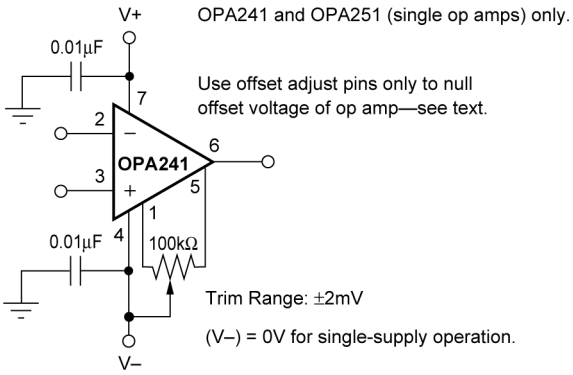


図 6-1. OPA241 and OPA251 Offset Voltage Trim Circuit

6.1.3 Capacitive Load and Stability

The OPAx241 series and OPAx251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions can be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

図 6-2 and 図 6-3 show the regions where the OPAx241 series and OPAx251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With V_S = 5V, G = 1, and I_{OUT} = 0, operation remains stable with load capacitance up to approximately 200pF. Increasing a combination of supply voltage, output current, and gain significantly improves capacitive load drive. For example, increasing the supplies to ±15V and gain to 10 drives approximately 2700pF.

図 6-4 shows one method to improve capacitive load drive in the unity gain configuration by inserting a resistor inside the feedback loop. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with V_S = ±1.35V and R_S = 5kΩ, the OPAx241 series and OPAx251 series perform well with capacitive loads in excess of 1000pF. Without the series resistor, the capacitive load drive is typically 200pF for these conditions. However, this method results in a slight reduction of output voltage swing.

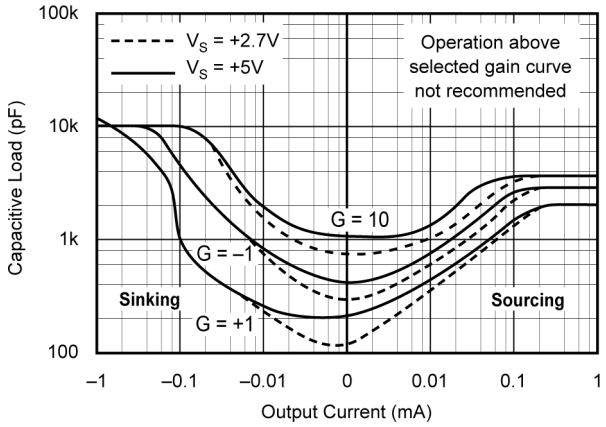


図 6-2. Stability—Capacitive Load vs Output Current for Low Supply Voltage

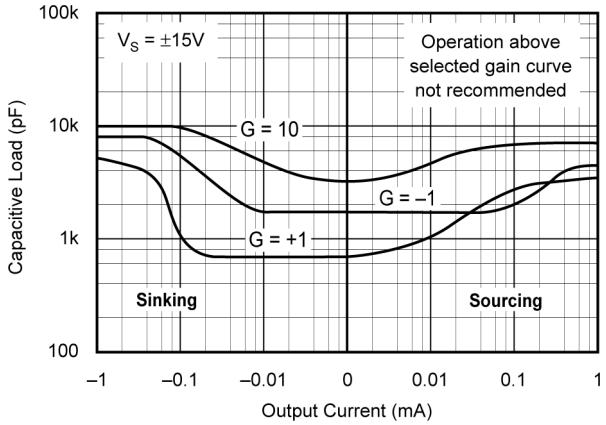


図 6-3. Stability—Capacitive Load vs Output Current for ±15V Supplies

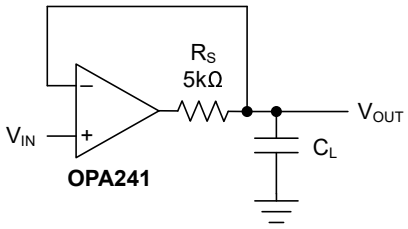
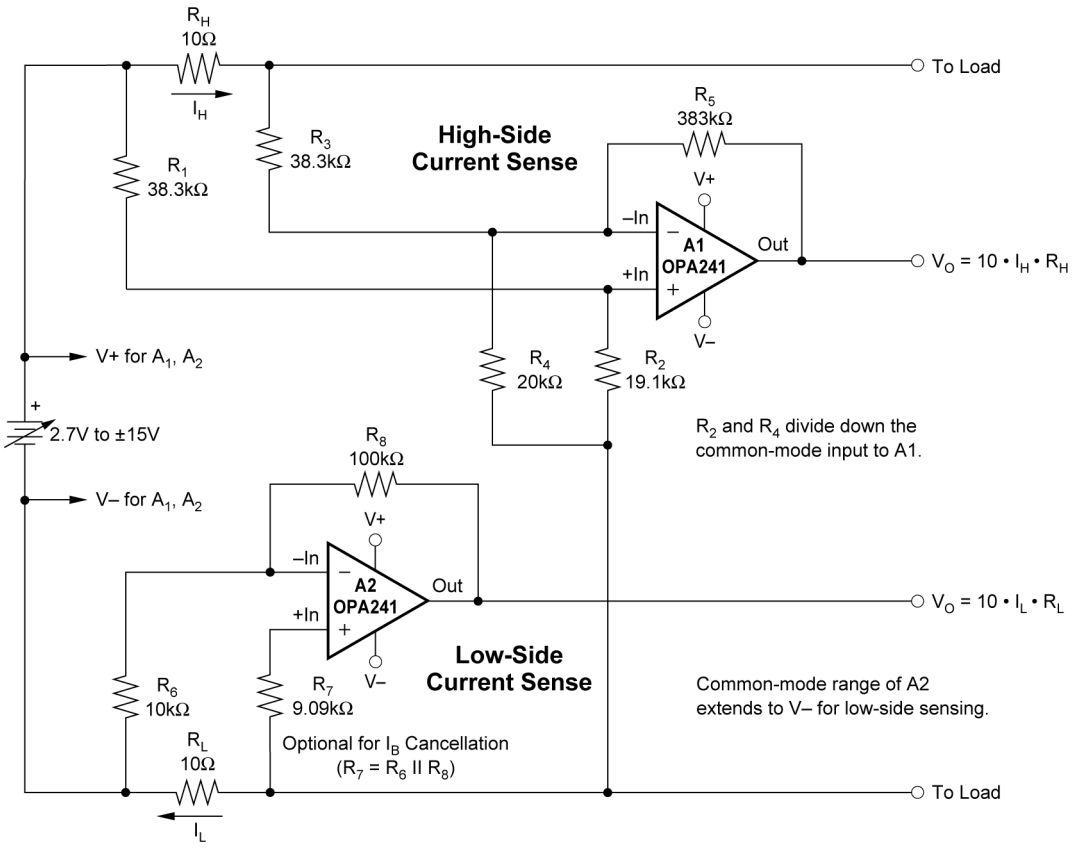


図 6-4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive



NOTE: Low and high-side sensing circuits can be used independently.

図 6-5. Low-Side and High-Side Battery Current Sensing

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

7.2 サポート・リソース

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7.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2000) to Revision A (June 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「製品情報」表、「ピン構成および機能」、「推奨動作条件」、「熱に関する情報」、「電気的特性」、「アプリケーションと実装」、「デバイスおよびドキュメントのサポート」、「改訂履歴」、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「概要」に新しい図を追加	1
• Updated pin names	3
• Changed input voltage noise from 1μV_{PP} to 1.7μV_{PP}	7
• Changed input voltage noise density from 45nV/√Hz to 65nV/√Hz	7
• Changed input impedance differential capacitance from 2pF to 3.75pF	7
• Changed overload recovery from 60μs to 80μs	7
• Changed short-circuit current from –30mA to –24mA for dual and quad	7
• Changed short-circuit current sink from –50mA to –27mA	9
• Deleted *Input Voltage and Current Noise Spectral Density vs Frequency* from *Typical Characteristics*	11
• Added Figure 5-4, *Input Voltage Noise Spectral Density vs Frequency* and Figure 5-5, *Input Current Noise Spectral Density vs Frequency*	11

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2241PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2241PA
OPA2241PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2241PA
OPA2241PAG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2241PA
OPA2241UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 2241UA
OPA2241UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA
OPA2241UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA
OPA2241UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA
OPA2251PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2251PA
OPA2251PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2251PA
OPA2251PAG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2251PA
OPA2251UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 2251UA
OPA2251UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA
OPA2251UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA
OPA2251UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA
OPA241PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	OPA241PA
OPA241PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA241PA
OPA241UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 241UA
OPA241UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA
OPA241UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA
OPA241UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA251UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 251UA
OPA251UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA
OPA251UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA
OPA251UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA
OPA4241PA	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4241PA
OPA4241PA.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA4241PA
OPA4241UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4241UA
OPA4241UA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4241UA
OPA4241UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4241UA
OPA4241UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4241UA
OPA4251UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4251UA
OPA4251UA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4251UA
OPA4251UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4251UA
OPA4251UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4251UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

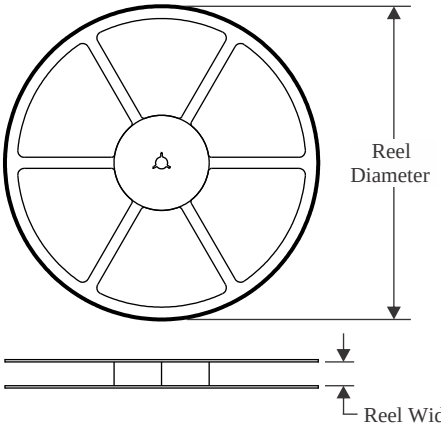
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

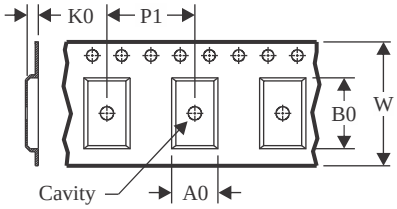
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

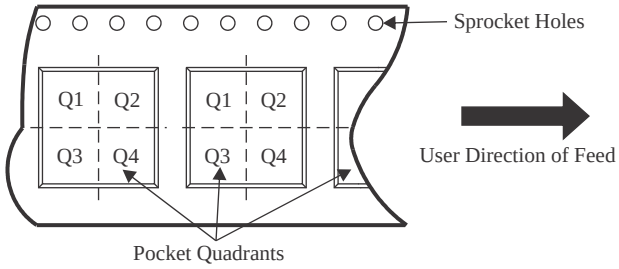


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

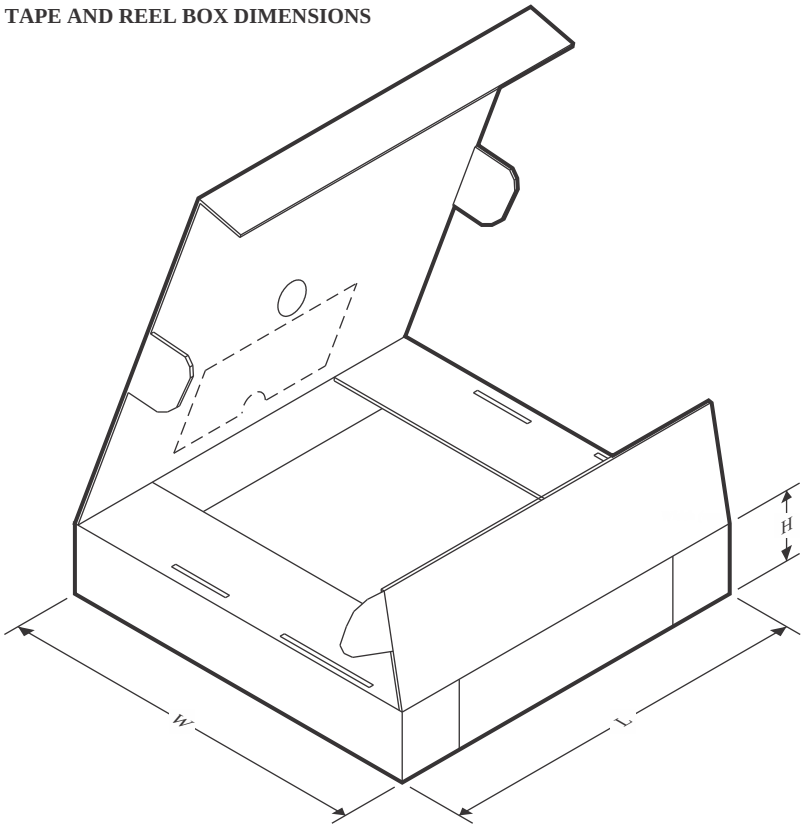
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4241UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4251UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

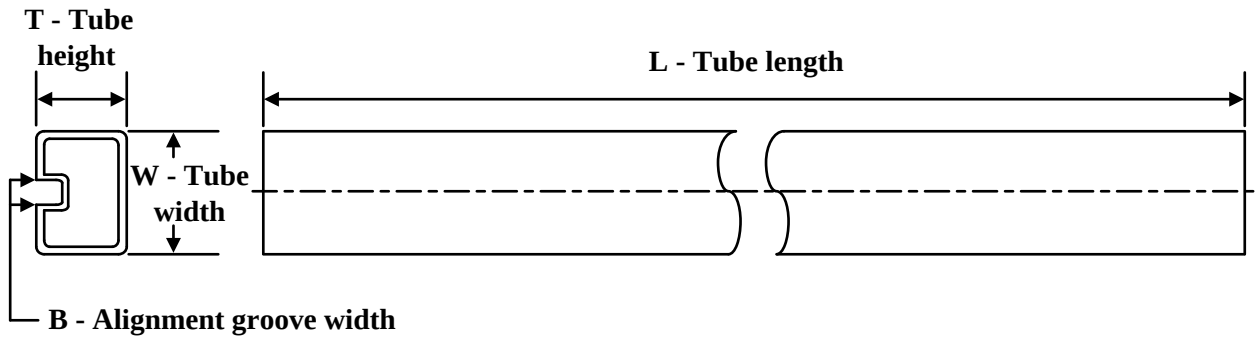
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

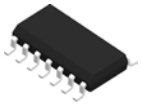
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2241UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2251UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA241UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA251UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4241UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0
OPA4251UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA241PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA4241PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4241PA.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4241UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4241UA.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UA.A	D	SOIC	14	50	506.6	8	3940	4.32

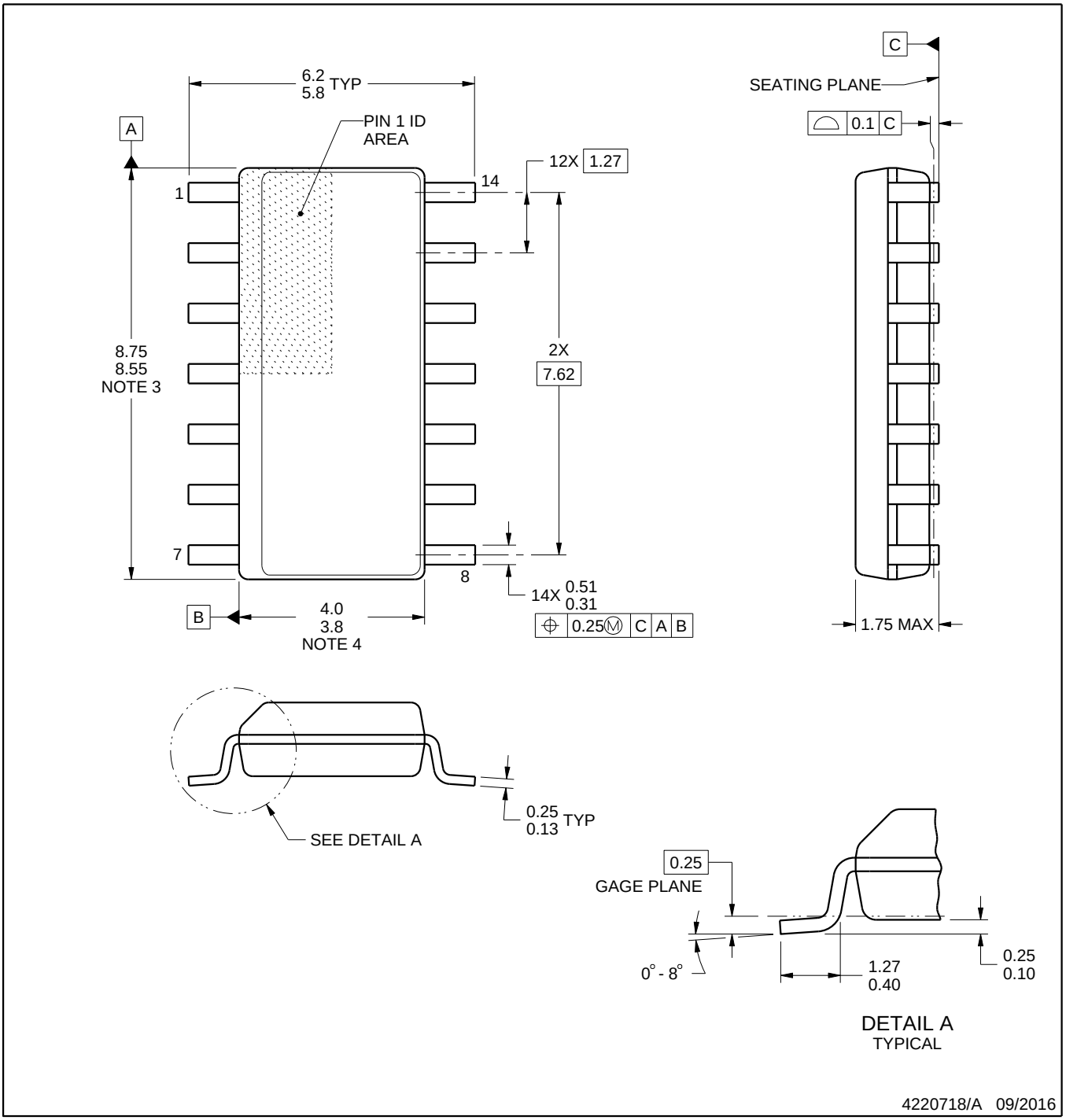


PACKAGE OUTLINE

D0014A

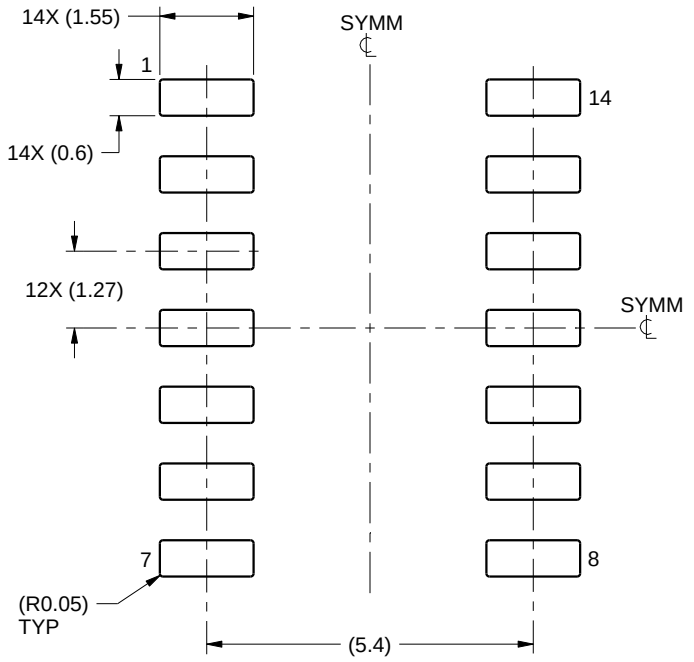
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

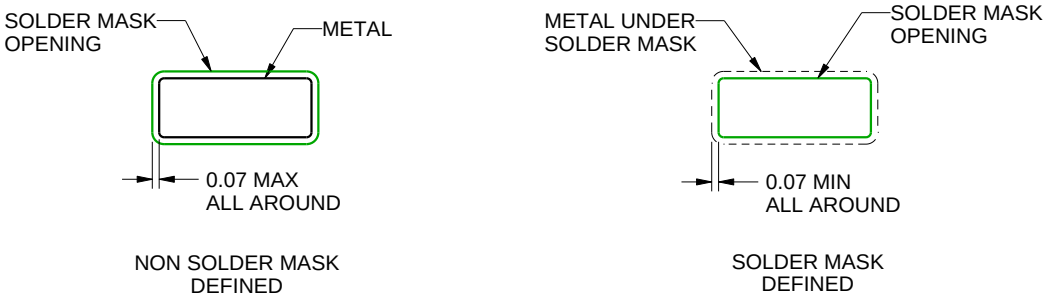


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

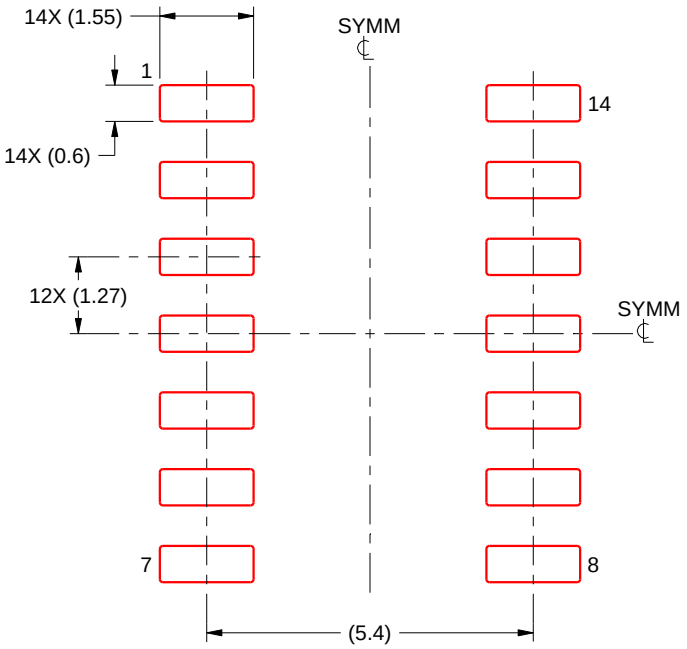
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

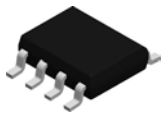


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

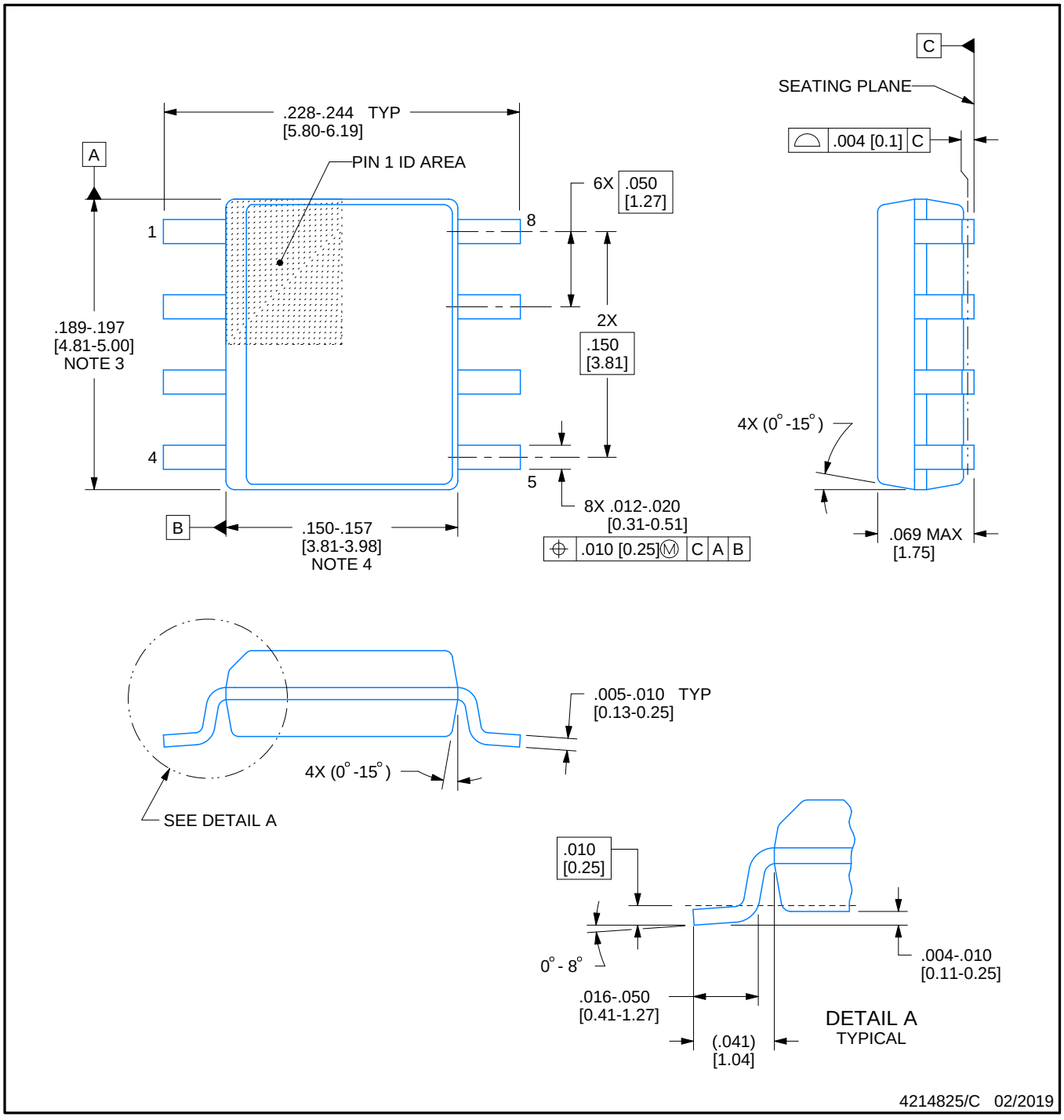


PACKAGE OUTLINE

D0008A

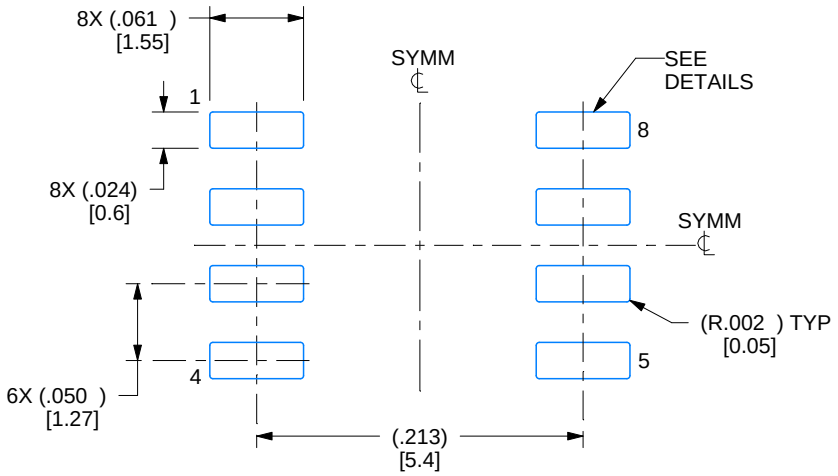
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

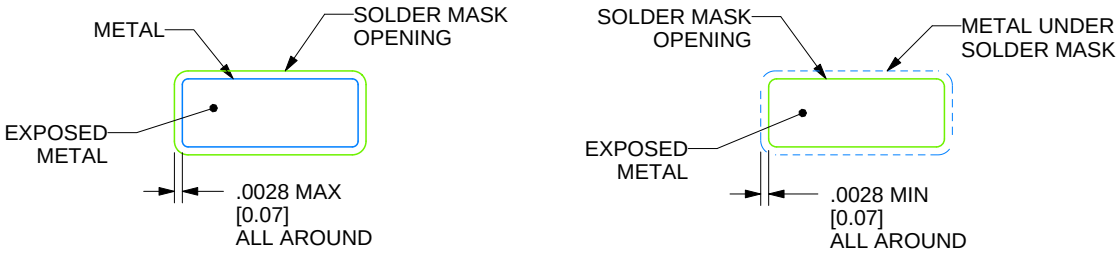


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

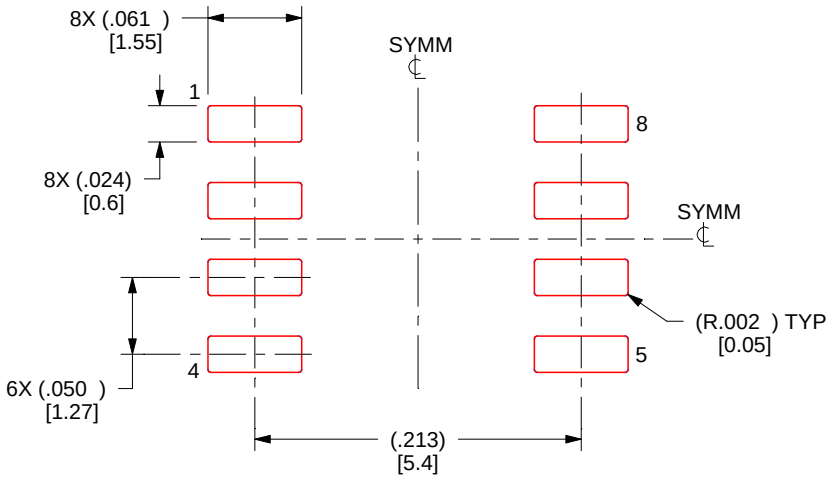
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



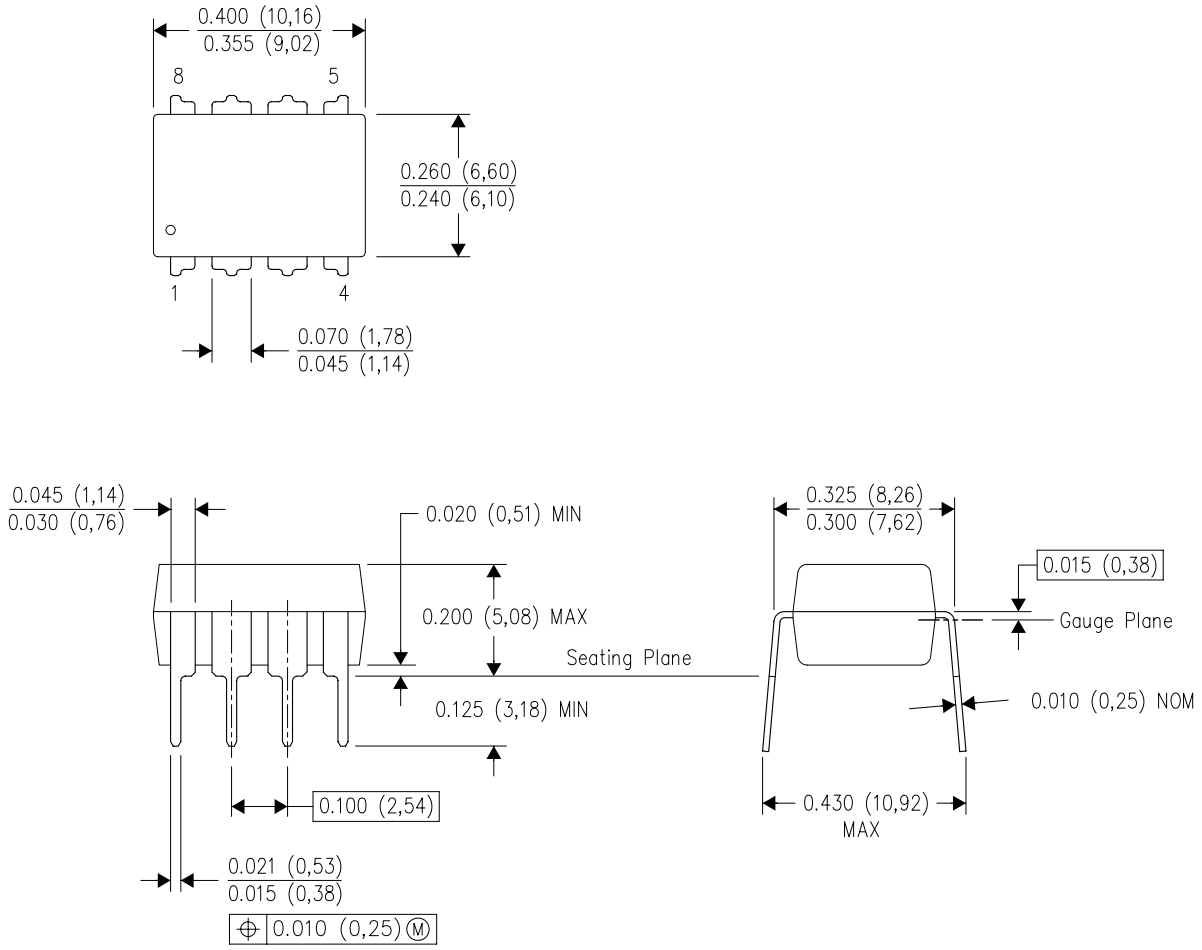
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

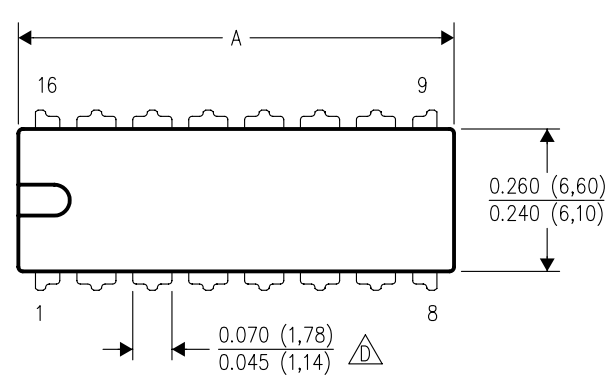


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

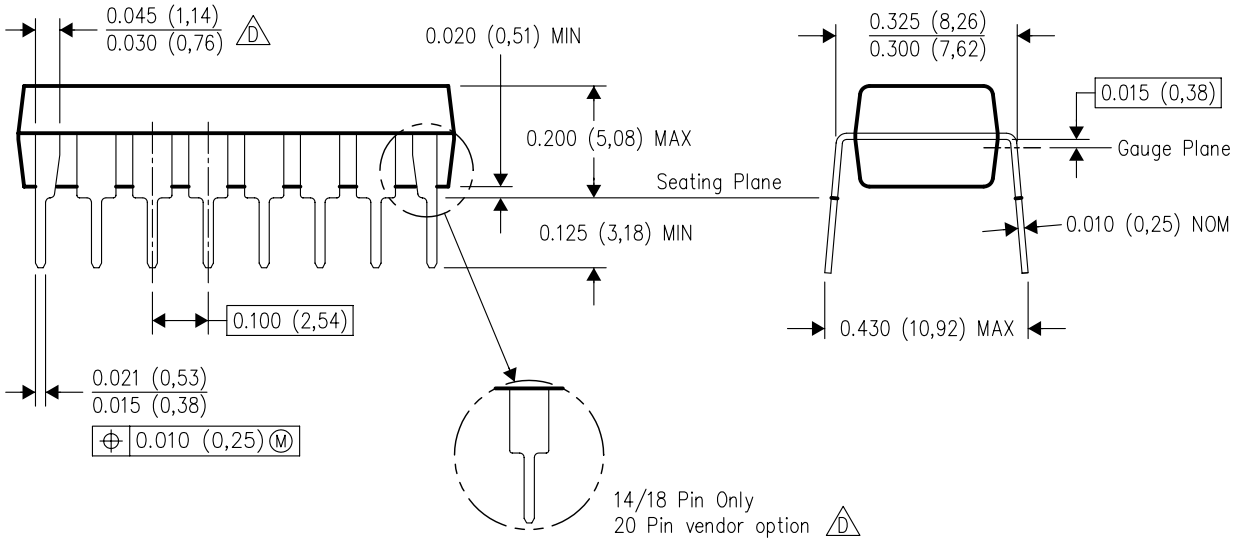
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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