OPAx373、OPAx374 6.5MHz、585μA、レール・ツー・レール入出力 CMOSオペアンプ

1 特長

- 低オフセット: 5mV (最大値)
- 低I_B: 10pA (最大値)
- 高い帯域幅: 6.5MHz
- レール・ツー・レール入出力
- 単一電源: 2.3V～5.5V
- シャットダウン: OPAx373
- 最高125℃での動作
- *Micro*サイズ・パッケージ: 5ピンSOT-23、6ピンSOT-23、8ピンSOT-23、10ピンVSON

2 アプリケーション

- 携帯機器
- バッテリ駆動のデバイス
- アクティブ・フィルタ
- A/Dコンバータの駆動

3 概要

OPA373およびOPA374ファミリは、低消費電力、低コストで非常に優れた帯域幅(6.5MHz)とスルー・レート(5V/μs)を持つオペアンプです。入力範囲はレールよりも200mV上まで対応し、出力範囲はレールから25mV以内です。速度/電力比と、小さなサイズから、携帯およびバッテリ駆動のアプリケーションに最適です。

OPA373ファミリはシャットダウン・モードを備えています。ロジック制御により、アンプを通常の動作からスタンバイに切り替えることができ、この状態での消費電流は1μA未満です。

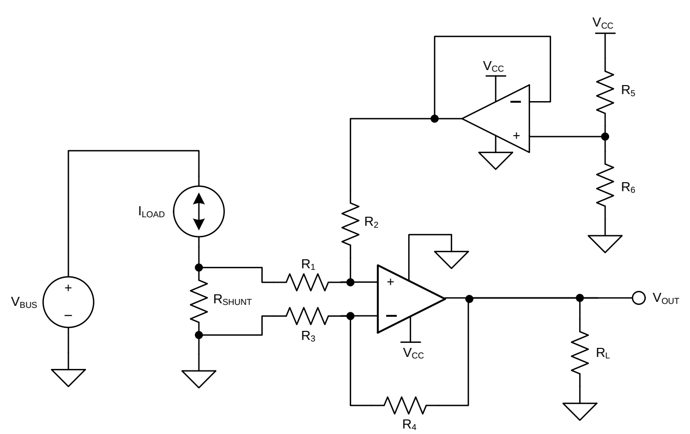
OPA373およびOPA374ファミリのオペアンプは、2.7V～5.5Vの単一またはデュアル電源での使用が規定されており、2.3V～5.5Vで動作します。すべてのモデルは、-40℃ ～ 125℃での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA373	SOIC (8)	4.90mm×3.91mm
	SOT-23 (6)	2.90mm×1.60mm
OPA374	SOIC (8)	4.90mm×3.91mm
	SOT-23 (5)	2.90mm×1.60mm
OPA2373	VSON (10)	3.00mm×3.00mm
	VSSOP (10)	3.00mm×3.00mm
OPA2374	SOIC (8)	4.90mm×3.91mm
	SOT-23 (8)	2.90mm×1.63mm
OPA4374	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



目次

4 改訂履歴

Revision E (May 2008) から **Revision F** に変更 | **Page**

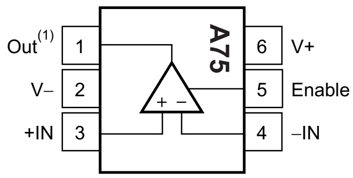
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Deleted *Package/Ordering Information* table; refer to *Package Option Addendum* at the end of this data sheet ... 4
- Deleted *lead temperature* specification from Absolute Maximum Ratings ... 7
- Changed values in the *Thermal Information* tables to align with JEDEC standards ... 7

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	SHUTDOWN	PACKAGE-PIN				
			SOIC	SOT-23	VSON	VSSOP	TSSOP
OPA373	1	Yes	8	6	—	—	—
OPA2373	2	Yes	—	—	10	10	—
OPA374	1	No	8	5	—	—	—
OPA2374	2	No	8	8	—	—	—
OPA4374	4	No	14	—	—	—	14

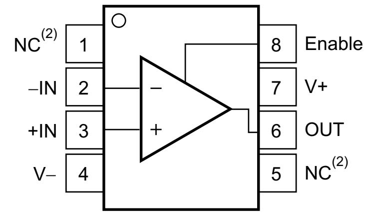
6 Pin Configuration and Functions

OPA373: DBV Package
6-Pin SOT-23
Top View



(1) Pin 1 of the 6-pin SOT-23 is determined by orienting the package marking as shown.

OPA373: D Package
8-Pin SOIC
Top View

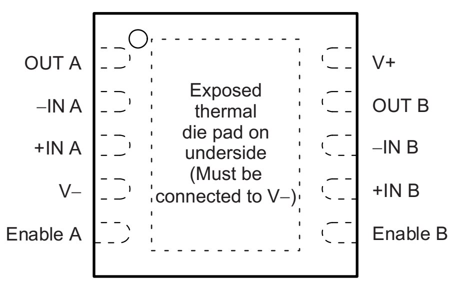


(2) NC indicates no internal connection.

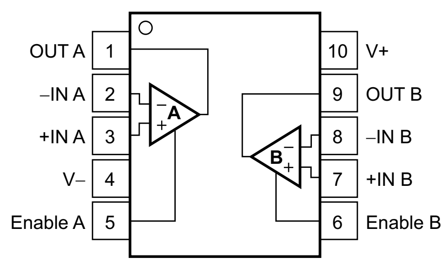
Pin Functions: OPA373

PIN			I/O	DESCRIPTION
NAME	**SOIC**	**SOT-23**		
Enable	8	5	I	Enable
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	6	—	Positive (highest) power supply

OPA2373: DGS Package
10-Pin VSON
Top View



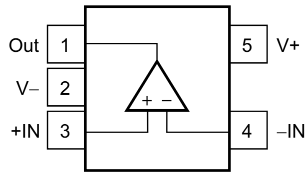
OPA2373: DRC Package
10-Pin VSSOP
Top View



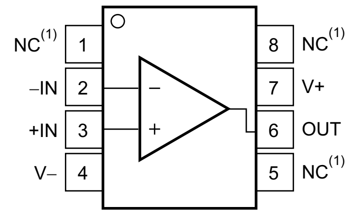
Pin Functions: OPA2373

PIN			I/O	DESCRIPTION
NAME	**VSON**	**VSSOP**		
Enable A	5	5	I	Enable A amplifier
Enable B	6	6	I	Enable B amplifier
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	8	8	I	Inverting input, channel B
+IN B	7	7	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	9	9	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	10	10	—	Positive (highest) power supply

OPA374: DBV Package
5-Pin SOT-23
Top View



OPA374: D Package
8-Pin SOIC
Top View

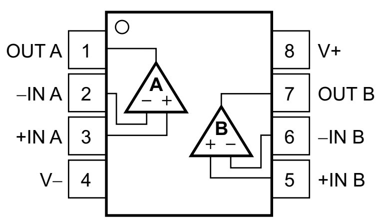


(1) NC indicates no internal connection.

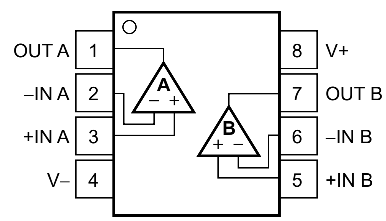
Pin Functions: OPA374

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2374: DCN Package
8-Pin SOT-23
Top View



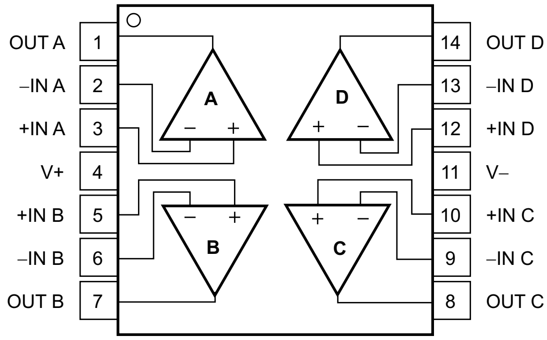
OPA2374: D Package
8-Pin SOIC
Top View



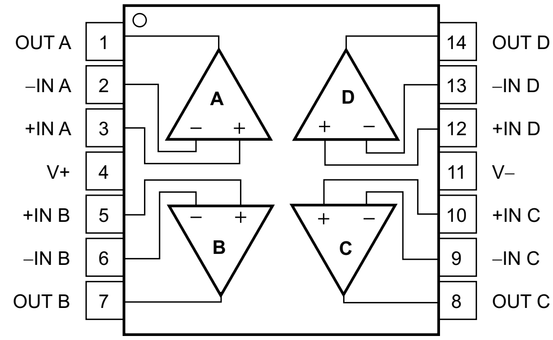
Pin Functions: OPA2374

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

OPA4374: PW Package
14-Pin TSSOP
Top View



OPA4374: D Package
14-Pin SOIC
Top View



Pin Functions: OPA4374

PIN			I/O	DESCRIPTION
NAME	SOIC	TSSOP		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
–IN C	9	9	I	Inverting input, channel C
+IN C	10	10	I	Noninverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage	Supply		7	V
	Signal input pin[(2)]	−0.5	(V+) + 0.5	
Current	Signal input pin[(2)]	–10	10	mA
	Output short-circuit[(3)]	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage	±1.35 (2.7)	±2.75 (5.5)	V
T_A	Operating temperature	–40	125	°C

7.4 Thermal Information: OPA373

THERMAL METRIC[(1)]		OPA373		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.4	184.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.7	146.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.8	36.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.9	33.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.3	35.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA374

THERMAL METRIC (1)		OPA374		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.1	220.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.7	129	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.5	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.2	21	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65	45.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA2373

THERMAL METRIC (1)		OPA2373		UNIT
		DGS (VSON)	DRC (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.6	56.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.8	76.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.6	30.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Thermal Information: OPA2374

THERMAL METRIC (1)		OPA2374		UNIT
		D (SOIC)	DCN (SOT-23)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.8	171.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	73.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.4	106.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.3	15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	105.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.8 Thermal Information: OPA4374

THERMAL METRIC (1)		OPA4374		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	112.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.8	56.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.9 Electrical Characteristics: V_S = 2.7 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			1	5	mV
	Input offset voltage versus temperature	T_A = –40°C to 125°C				6.5	mV
dV_{OS}/dT	Input offset voltage versus drift	T_A = –40°C to +125°C			3		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 2.7 V to 5.5 V, V_{CM} < (V+) – 2 V	T_A = 25°C		25	100	µV/V
			T_A = –40°C to 125°C			150	
	Channel separation, DC				0.4		µV/V
		At f = 1 kHz			128		dB
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 2 V	T_A = 25°C	80	90		dB
			T_A = –40°C to 125°C	70			
		V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V	T_A = 25°C	66			dB
			T_A = –40°C to 125°C	60			dB
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
I_{OS}	Input offset current				±0.5	±10	pA
INPUT IMPEDANCE							
	Differential				10^{13} || 3		Ω || pF
	Common-mode				10^{13} || 6		Ω || pF
NOISE							
	Input voltage noise	V_{CM} < (V+) – 2 V, f = 0.1 Hz to 10 Hz			10		μV_{PP}
e_n	Input voltage noise density	V_{CM} < (V+) – 2 V, f = 10 kHz			15		nV/$\sqrt{Hz}$
i_n	Input current noise density	V_{CM} < (V+) – 2 V, f = 10 kHz			4		fA/$\sqrt{Hz}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V	T_A = 25°C	94	110		dB
			T_A = –40°C to 125°C	80			
		V_S = 5 V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V	T_A = 25°C	94	106		dB
			T_A = –40°C to 125°C	80			
OUTPUT							
	Voltage output swing from rail	R_L = 100 kΩ	T_A = 25°C		18	25	mV
			T_A = –40°C to 125°C			25	mV
		R_L = 5 kΩ	T_A = 25°C		100	125	mV
			T_A = –40°C to 125°C			125	mV
I_{SC}	Short-circuit current			See *Typical Characteristics*			
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
R_O	Open-loop output impedance	f = 1 MHz, I_O = 0 mA			220		Ω

Electrical Characteristics: V_S = 2.7 V to 5.5 V (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF			6.5		MHz
SR	Slew rate	C_L = 100 pF, G = +1			5		V/µs
t_S	Settling time	0.1%, C_L = 100 pF, V_S = 5 V, 2-V step, G = +1			1		µs
		0.01%, C_L = 100 pF, V_S = 5 V, 2-V step, G = +1			1.5		µs
	Overload recovery time	C_L = 100 pF, V_{IN} ● Gain > V_S			0.3		µs
THD+N	Total harmonic distortion + noise	C_L = 100 pF, V_S = 5 V, V_O = 3 V_{PP}, G = +1, f = 1 kHz			0.0013%		
ENABLE OR SHUTDOWN							
t_{OFF}	Turnoff time				3		µs
t_{ON}	Turnon time				12		µs
V_L	Logic low threshold	Shutdown		V–		(V–) + 0.8	V
V_H	Logic high threshold	Amplifier is active		(V–) + 2		V+	V
	Input bias current of Enable pin				0.2		µA
$I_{Q(sd)}$	Quiescent current at shutdown (per amplifier)				< 0.5	1	µA
POWER SUPPLY							
V_S	Specified voltage range			2.7		5.5	V
	Operating voltage range				2.3 to 5.5		V
I_Q	Quiescent current (per amplifier)	I_O = 0 mA	T_A = 25°C		585	750	µA
			T_A = –40°C to 125°C			800	µA
TEMPERATURE							
	Specified range			–40		125	°C
T_A	Operating range			–55		150	°C
T_{stg}	Storage range			–65		150	°C

7.10 Typical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted)

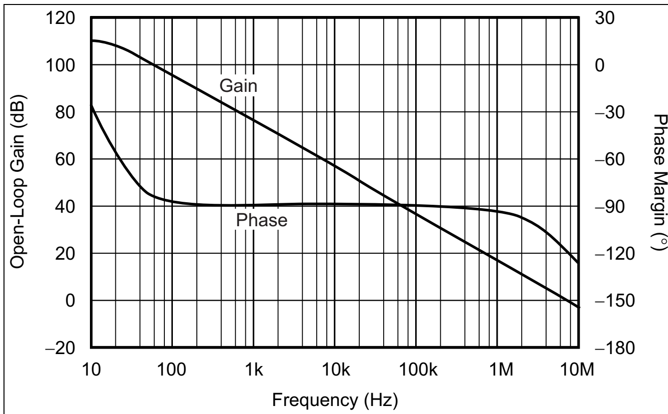


Figure 1. Open-Loop Gain and Phase vs Frequency

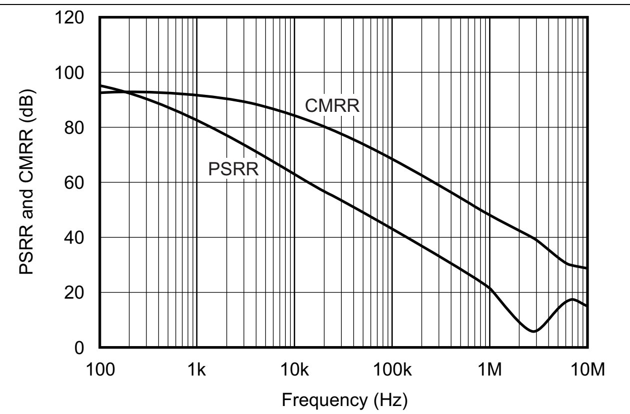


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

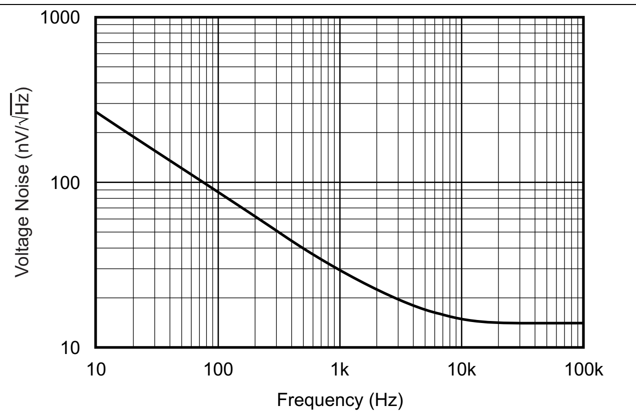


Figure 3. Input Voltage Noise Spectral Density vs Frequency

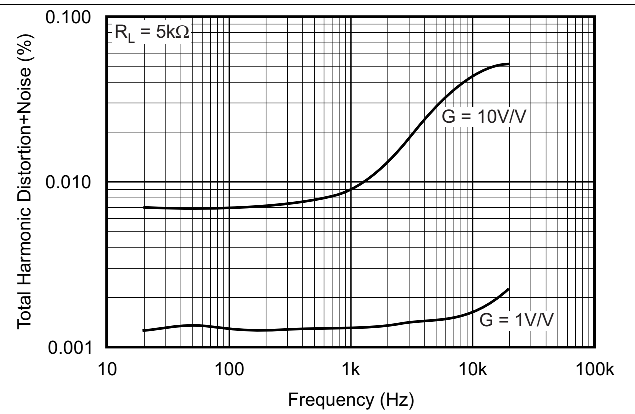


Figure 4. Total Harmonic Distortion + Noise vs Frequency

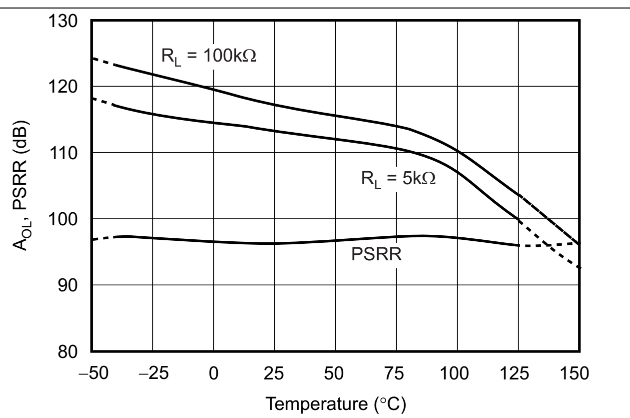


Figure 5. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

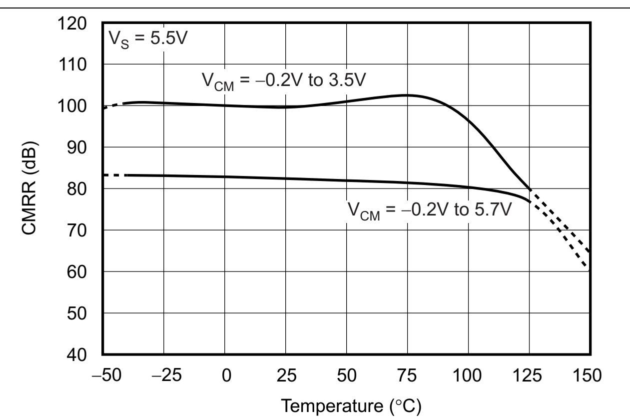


Figure 6. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$ (unless otherwise noted)

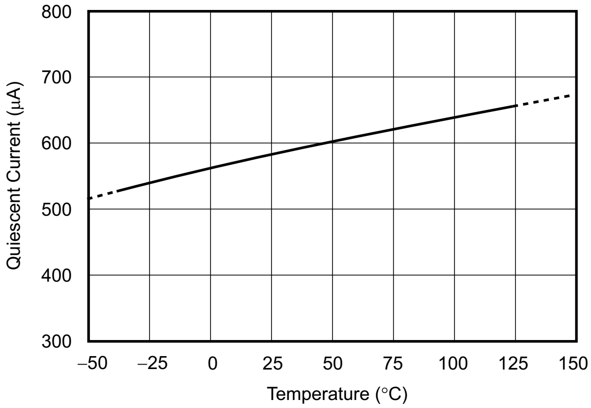


Figure 7. Quiescent Current vs Temperature

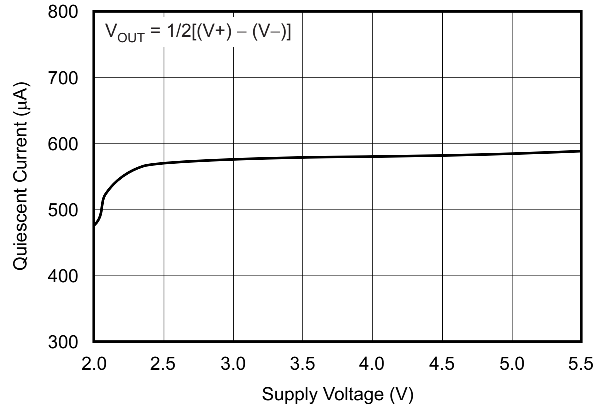


Figure 8. Quiescent Current vs Supply Voltage

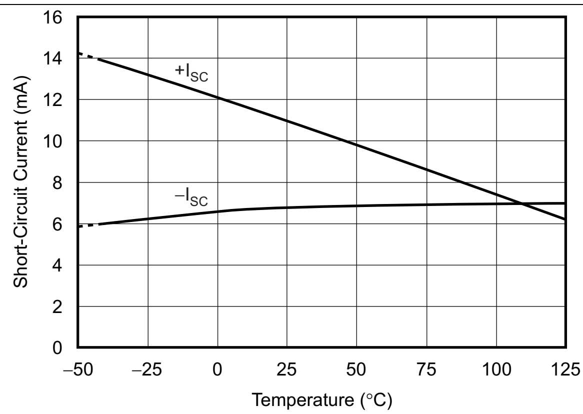


Figure 9. Short-Circuit Current vs Temperature

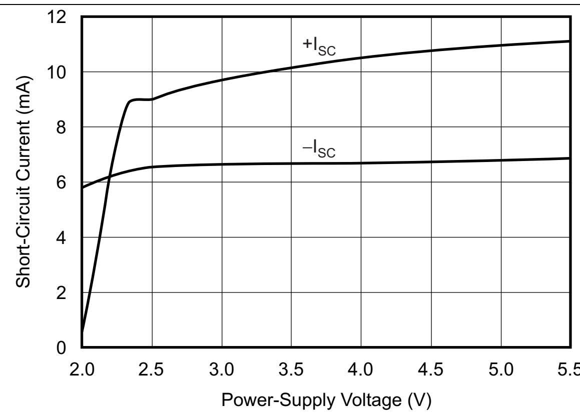


Figure 10. Continuous Short-Circuit Current vs Power-Supply Voltage

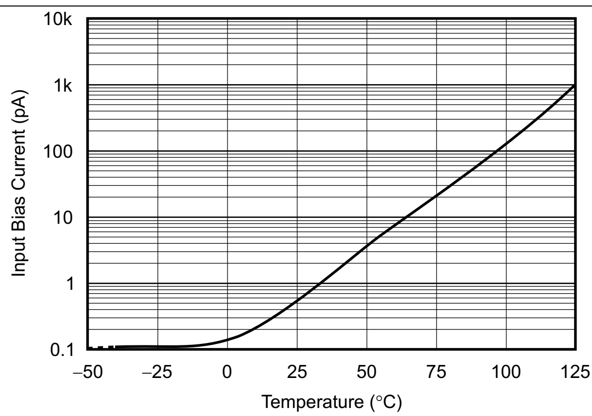


Figure 11. Input Bias Current vs Temperature

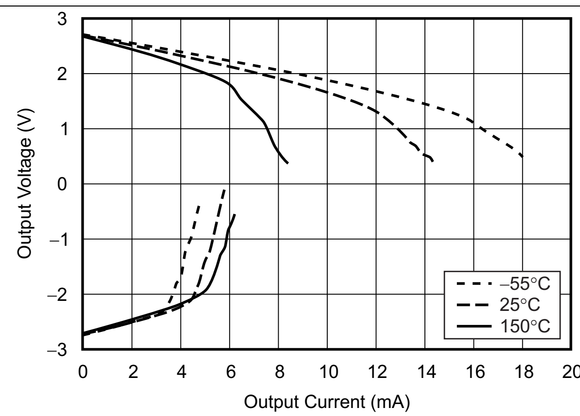


Figure 12. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

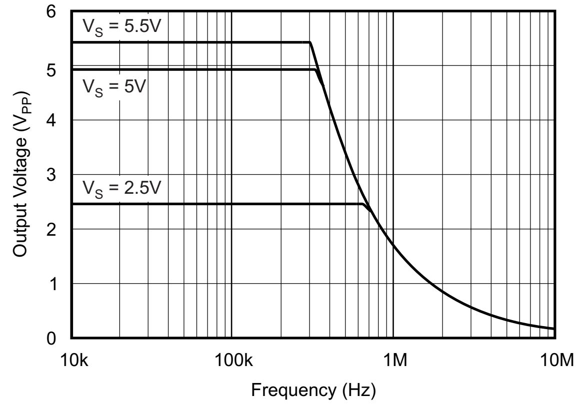


Figure 13. Maximum Output Voltage vs Frequency

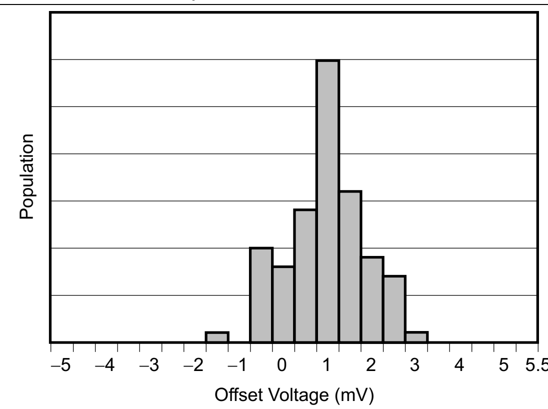


Figure 14. Offset Voltage Production Distribution

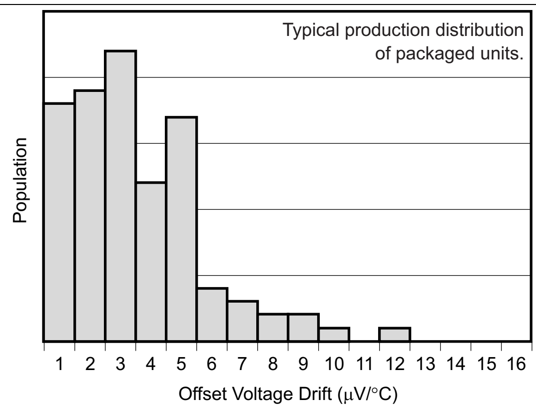


Figure 15. Offset Voltage Drift Magnitude Production Distribution

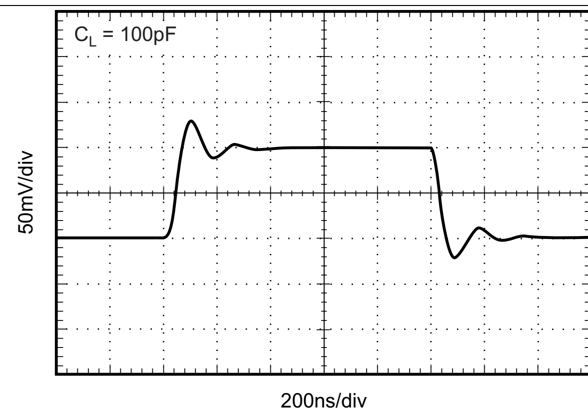


Figure 16. Small-Signal Step Response

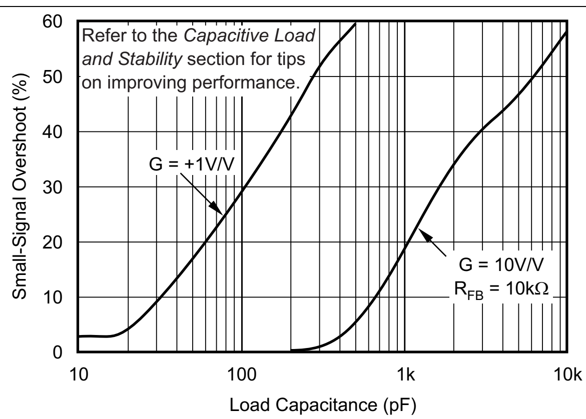


Figure 17. Small-Signal Overshoot vs Load Capacitance

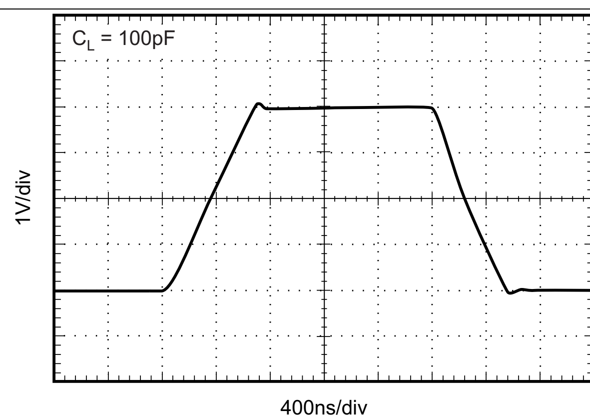


Figure 18. Large-Signal Step Response

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

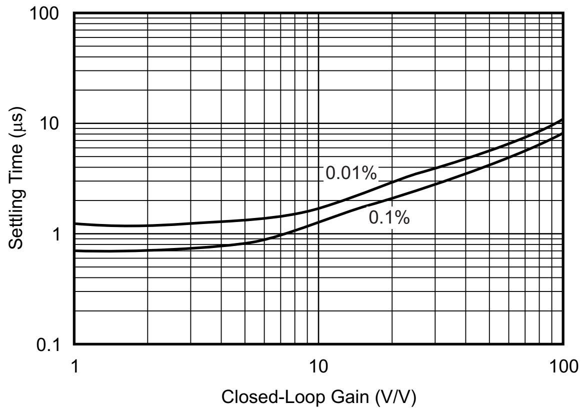


Figure 19. Settling Time vs Closed-Loop Gain

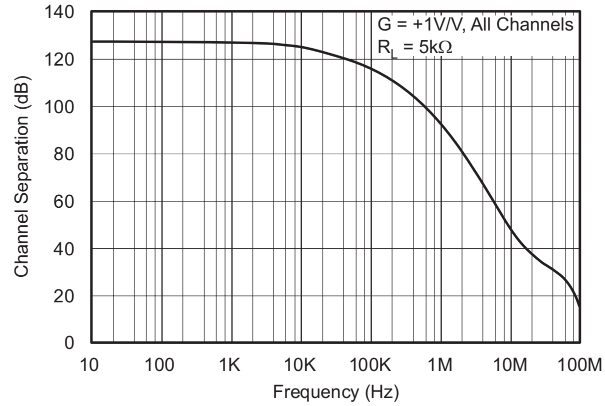


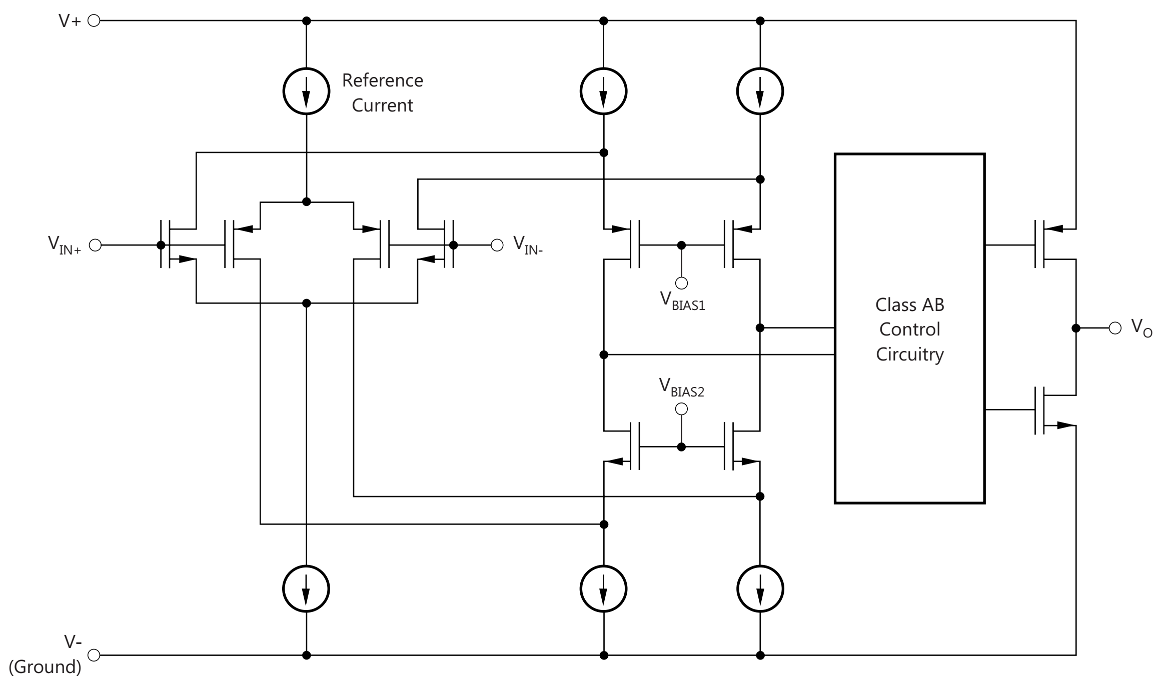
Figure 20. Channel Separation vs Frequency

8 Detailed Description

8.1 Overview

The OPAx373 and OPAx374 operational amplifiers (op amps) are suitable for a broad range of general-purpose applications. As unity-gain stable devices and outstanding AC performance, these op amps are ideal for audio applications. The class AB output stage is capable of driving 100-kΩ loads connected to any point between V+ and ground. These devices are well-suited for nearly any single-supply application up to a supply voltage of 5.5 V because the input common-mode voltage range includes both rails. Rail-to-rail input and output swing significantly increases the overall device dynamic range, especially in low-supply applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPA373 and OPA374 op amps are specified and tested over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.3 V to 5.5 V (±1.15 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics*.

Feature Description (continued)

8.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPA373 and OPA374 series extends 200 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.65 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) − 1.65 V. There is a 500-mV transition region, typically (V+) − 1.9 V to (V+) − 1.4 V, in which both pairs are on. This 500-mV transition region, shown in Figure 21, can vary ±300 mV with process variation. Thus, the transition region (that is, both stages on) can range from (V+) − 2.2 V to (V+) − 1.7 V on the low end, up to (V+) − 1.6 V to (V+) − 1.1 V on the high end. Within the 500-mV transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded, compared to device operation outside this region.

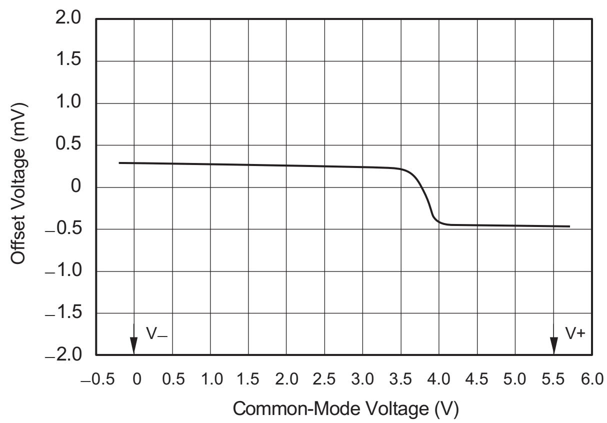


Figure 21. Behavior of Typical Transition Region at Room Temperature

8.3.3 Rail-to-Rail Input

The input common-mode range extends from (V−) − 0.2 V to (V+) + 0.2 V. For normal operation, inputs must be limited to this range. The absolute maximum input voltage is 500 mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, do not cause any damage to the op amp. Unlike some other op amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 22.

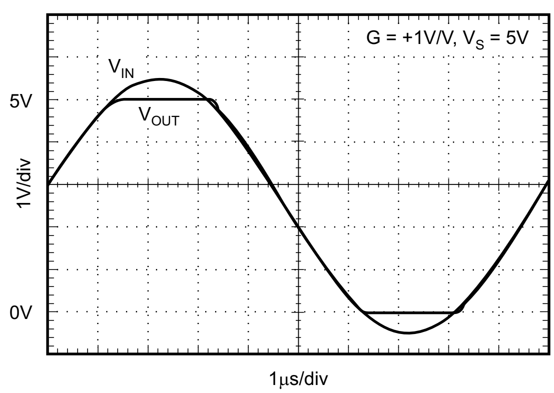


Figure 22. OPA373: No Phase Inversion With Inputs Greater Than the Power-Supply Voltage

Normally, input bias current is approximately 500 fA; however, input voltages exceeding the power supplies by more than 500 mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This limiting is easily accomplished with an input resistor; see Figure 23. Many input signals are inherently current-limited to less than 10 mA, therefore, a limiting resistor is not required.

Feature Description (continued)

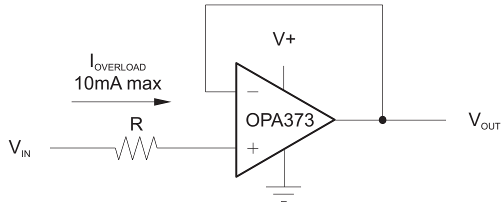


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Figure 23. Input Current Protection for Voltages Exceeding the Supply Voltage

8.3.4 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 100 kΩ), the output voltage can typically swing to within 18 mV from the supply rails. With moderate resistive loads (5 kΩ to 50 kΩ), the output can typically swing to within 100 mV from the supply rails and maintain high open-loop gain. See Figure 12 for more information.

8.3.5 Capacitive Load and Stability

The OPA373 series op amps can drive a wide range of capacitive loads. However, under certain conditions, all op amps may become unstable. Op amp configuration, gain, and load value are some of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. The OPA373 series op amps perform well in unity-gain configuration, with a pure capacitive load up to approximately 250 pF. Increased gains allow the amplifier to drive more capacitance. See Figure 17 for further details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 24. This configuration significantly reduces ringing while maintaining DC performance for purely capacitive loads. When there is a resistive load in parallel with the capacitive load, R_S must be placed within the feedback loop as shown to allow the feedback loop to compensate for the voltage divider created by R_S and R_L.

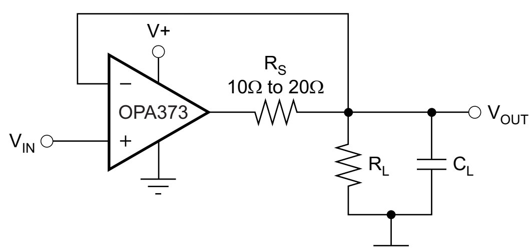

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Figure 24. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

Feature Description (continued)

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small-valued resistors. However, when large-valued resistors cannot be avoided, a small (4-pF to 6-pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 25. This technique significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance and printed-circuit board (PCB) parasitic capacitance.

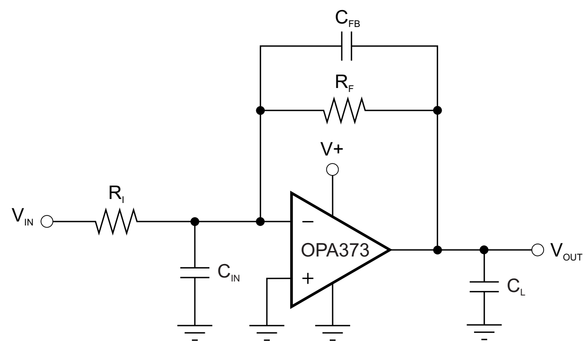

Figure 25. Improving Capacitive Load Drive

For example, when driving a 100-pF load in unity-gain inverter configuration, adding a 6-pF capacitor in parallel with the 10-kΩ feedback resistor decreases overshoot from 57% to 12%, as shown in Figure 26.

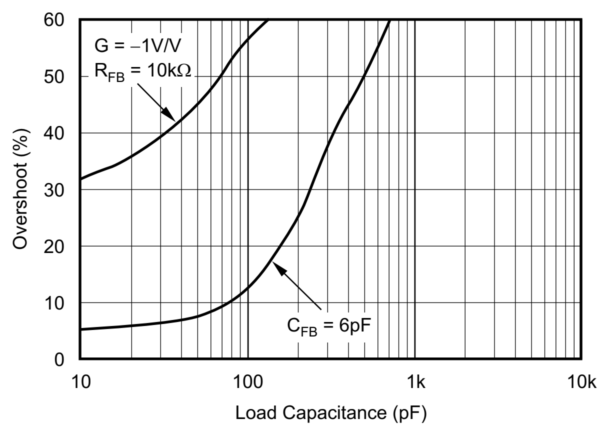

Figure 26. Improving Capacitive Load Drive

8.3.6 Enable or Shutdown

The OPA373 and OPA374 series op amps typically require 585-µA quiescent current. The enable or shutdown feature of the OPA373 allows the op amp to be shut off to reduce this current to less than 1 µA.

8.4 Device Functional Modes

The OPAx374 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx374 is 5.5 V (±2.75 V).

The OPAx373 has two functional modes: active and shutdown. When the voltage at the Enable pin is from V– to (V–) + 0.8 V, the device is in shutdown and consumes less than 0.5 µA of quiescent current (typical). To activate, or enable, the device, the voltage at the Enable pin must be from (V–) + 2 V to V+. When active, the power-supply requirements are the same as the OPAx374.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA373 and OPA374 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input and output make them ideal for driving sampling analog-to-digital converters (ADCs). Excellent AC performance makes them well-suited for audio applications. The class AB output stage is capable of driving 100-kΩ loads connected to any point between V+ and ground.

The input common-mode voltage range includes both rails, allowing the OPA373 and OPA374 series op amps to be used in virtually any single-supply application up to a supply voltage of 5.5 V. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

9.2 Typical Application

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1 A to 1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA2374 because of its rail-to-rail input and output range and cost compared to performance. One of the amplifiers is configured as a difference amplifier, and the other amplifier provides the reference voltage.

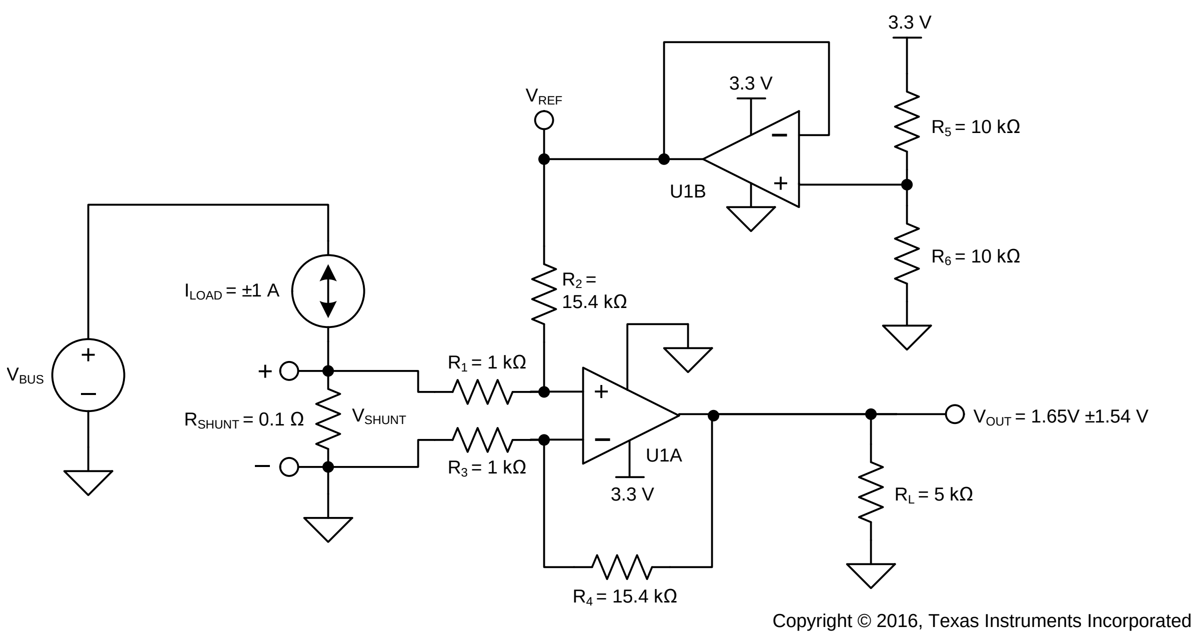

Figure 27. Single-Supply, Low-Side, Bidirectional Current-Sensing Solution

9.2.1 Design Requirements

This design has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

Typical Application (continued)

9.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6}\right)$ (1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches the ratio of R_2/R_1. The ratio of R_2/R_1 impacts the CMRR of the difference amplifier, which ultimately translates to an offset error.

This is a low-side measurement. Therefore, the value of V_{SHUNT} is the ground potential for the system load. Thus, it is important to place a maximum value on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT\_Max} = \frac{|V_{SHUNT\_Max}|}{|I_{LOAD\_Max}|} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

Because the load current is bidirectional, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the op amp, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device.

It is therefore important to use an op amp, such as the OPA374, that has a common-mode range that extends below the negative supply voltage.

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA374 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and output swing of the OPA374, given a 3.3-V supply.

$$-200\ mV < V_{CM} < 3.5\ V \quad (3)$$

$$100\ mV < V_{OUT} < 3.2\ V \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1\ A)]} = 15.5\ \frac{V}{V} \quad (5)$$

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

Because the gain error of the circuit primarily depends on R_1 through R_4, 0.1% resistors were selected. This value reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

Typical Application (continued)

9.2.3 Application Curve

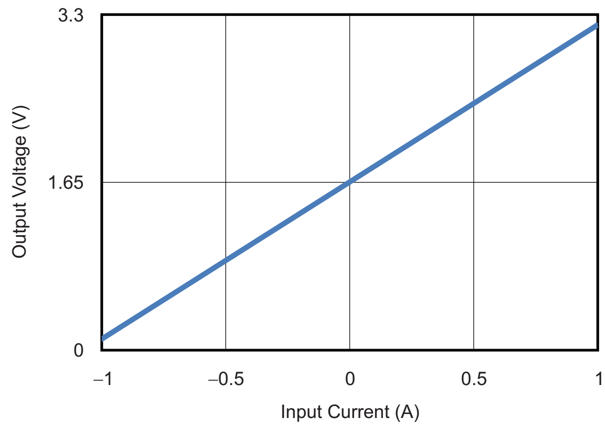

Figure 28. Output Voltage vs Input Current

9.3 System Examples

9.3.1 Driving ADCs

The OPA373 and OPA374 series op amps are optimized for driving medium-speed sampling ADCs. The OPA373 and OPA374 op amps buffer the ADC input capacitance and resulting charge injection, while providing signal gain.

The OPA373 is shown driving the ADS7816 in a basic noninverting configuration, as Figure 29 shows. The ADS7816 is a 12-bit, MicroPower sampling converter in the 8-pin VSSOP package. When used with the low-power, miniature packages of the OPA373, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide anti-aliasing filtering.

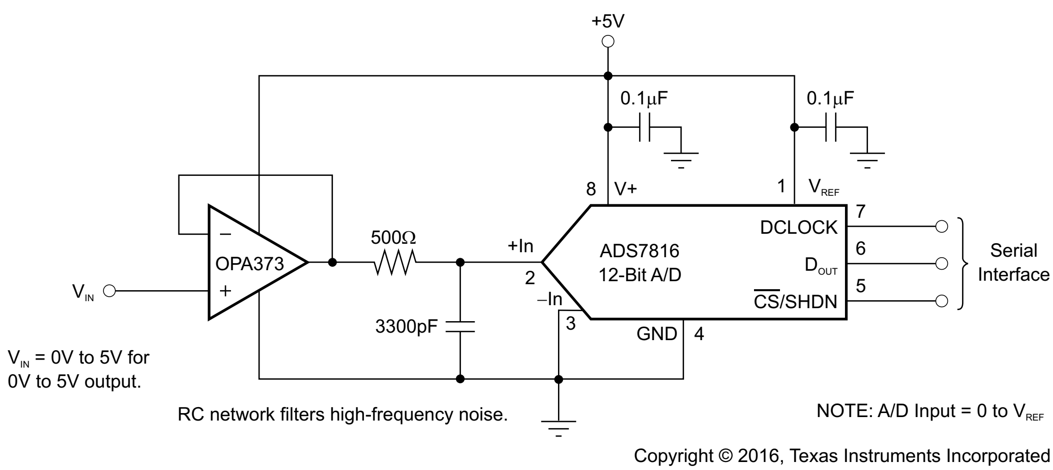

Figure 29. The OPA373 in Noninverting Configuration Driving the ADS7816

System Examples (continued)

Figure 30 shows the OPA373 driving the ADS7816 in a speech bypass-filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit operates with V_S = 2.7 V to 5 V.

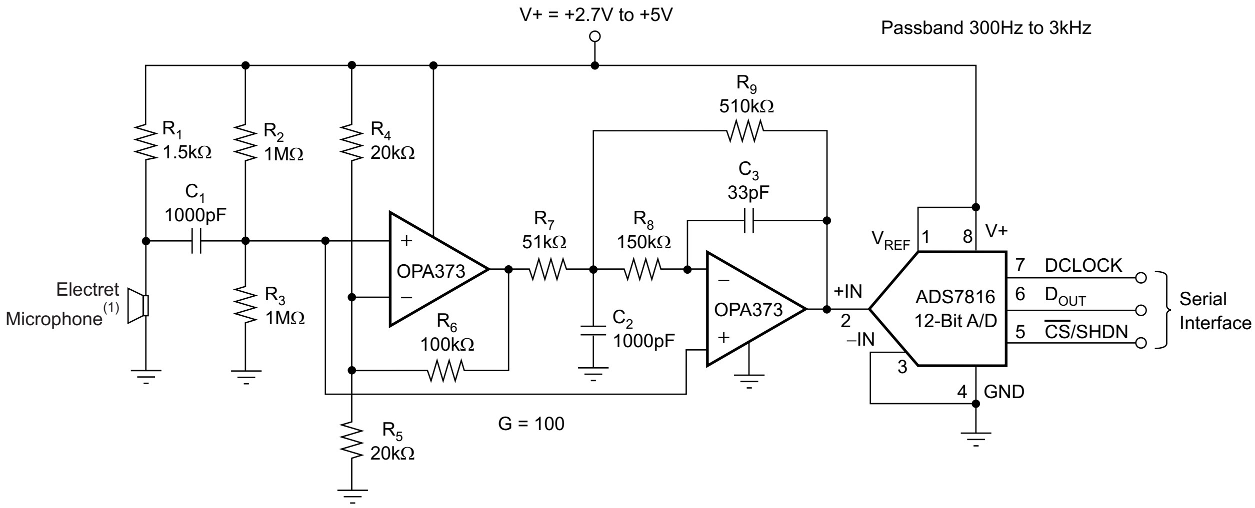

Figure 30. The OPA2373 as a Speech Bypass-Filtered Data Acquisition System

The OPA373 is shown in the inverting configuration described in Figure 31. In this configuration, filtering may be accomplished with the capacitor across the feedback resistor.

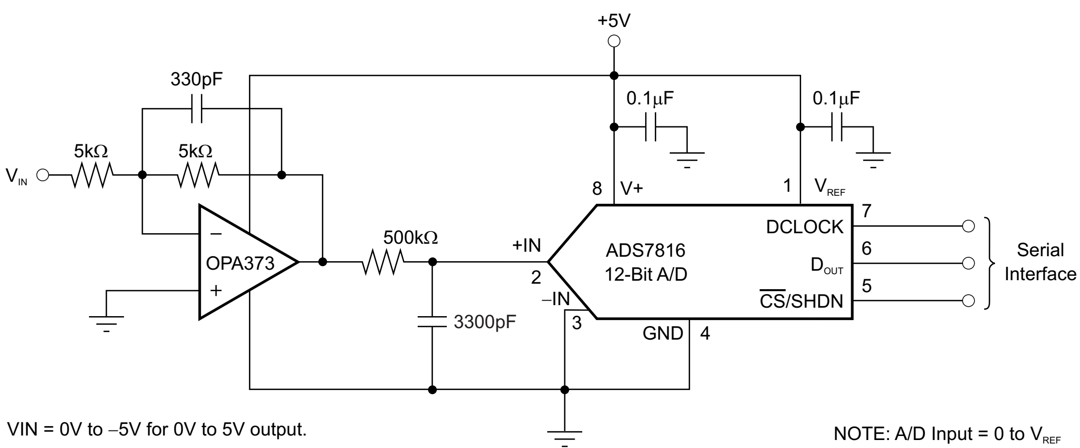

Figure 31. The OPA373 in Inverting Configuration Driving the ADS7816

Figure 32 shows the OPA373 configured as a three-pole, Sallen-Key, Butterworth low-pass filter.

System Examples (continued)

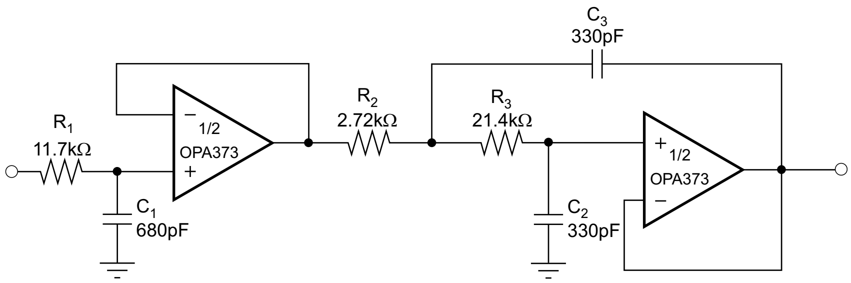

Figure 32. Three-Pole, Sallen-Key, Butterworth Low-Pass Filter

10 Power Supply Recommendations

The OPAx373 and OPAx374 are specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

The leadframe die pad must be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements.

Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat sink area on the PCB. Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests.

Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

11.1.1 VSON Package

The OPA2373 is available in a 10-pin VSON package, which is a VQFN package with lead contacts on only two sides of the bottom of the package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad. VSON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SOIC and VSSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The VSON package can be easily mounted using standard PCP assembly techniques. See *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages*, both available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package must be connected to V−.

11.2 Layout Example

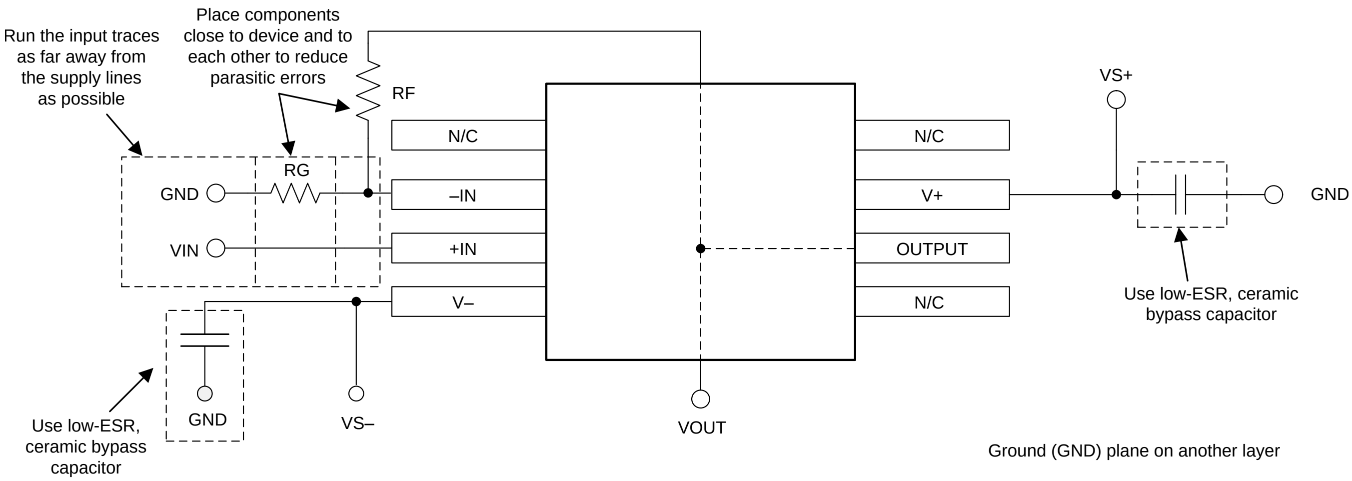

Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

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これらのファイルを使用するには、TINAソフトウェア(DesignSoft™ 製)またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

12.1.1.2 DIPアダプタ評価モジュール

DIPアダプタ評価モジュール・ツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU (8ピンSOIC)、PW (8ピンTSSOP)、DGK (8ピンMSOP)、DBV (6ピンSOT-23、5ピンSOT23、3ピンSOT-23)、DCK (6ピンSC-70および5ピンSC-70)、DRL (6ピンSOT-563)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

12.1.1.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のICパッケージ・タイプ向けの回路のプロトタイプ作成を容易にします。この評価モジュール基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、SOT-23のすべてのパッケージがサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のICを実装する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

12.1.1.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

12.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

12.2 ドキュメントのサポート

12.2.1 関連資料

以下に示すドキュメントはOPAx373およびOPAx374の使用に関連しており、参照用にお勧めします。すべてのドキュメントは、特に記述のない限りwww.ti.comからダウンロードできます。

- *『36V、1kWブラシレスDCモータ・ドライブ、応答時間1μs未満のストール電流制限付き、リファレンス・デザイン』*(TIDU852)
- *『OPA373のEMI耐性特性』*(SBOZ009)
- *『AB-045 オペアンプの性能分析』*(SBOA054)
- *『AB-067 オペアンプの単一電源動作』*(SBOA059)
- *『AB-105 アンプのチューニング』*(SBOA067)
- *『QFN/SONのPCB実装』*(SLUA271)
- *『クワッド・フラットパックの鉛フリー・ロジック・パッケージ』*(SCBA017)

12.3 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA373	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2373	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA374	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2374	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4374	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商標

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2373AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	AYO
OPA2373AIDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	AYO
OPA2373AIDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	AYO
OPA2373AIDGST.B	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	AYO
OPA2373AIDRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ
OPA2373AIDRCR.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ
OPA2373AIDRCRG4.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ
OPA2373AIDRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ
OPA2373AIDRCT.B	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ
OPA2374AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A
OPA2374AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A
OPA2374AIDCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDCNR.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDCNRG4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDCNT	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDCNT.B	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDCNTG4	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP
OPA2374AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A
OPA2374AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	OPA 2374A
OPA2374AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A
OPA373AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A
OPA373AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A
OPA373AIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75
OPA373AIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA373AIDBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75
OPA373AIDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75
OPA373AIDBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75
OPA373AIDBVTG4	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75
OPA373AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A
OPA373AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A
OPA373AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A
OPA374AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A
OPA374AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A
OPA374AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76
OPA374AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A
OPA374AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A
OPA374AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A
OPA4374AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A
OPA4374AID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A
OPA4374AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A
OPA4374AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A
OPA4374AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A
OPA4374AIPWR	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4374AIPWR.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A
OPA4374AIPWRG4	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A
OPA4374AIPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A
OPA4374AIPWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

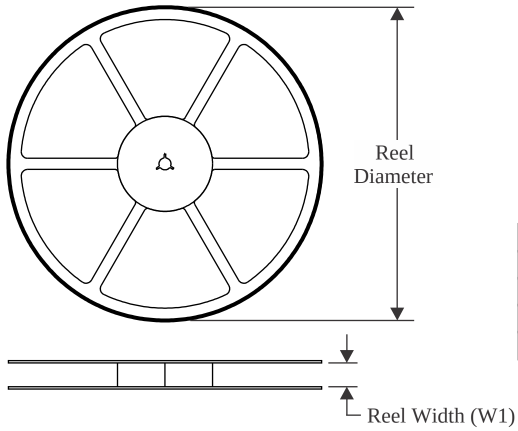
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

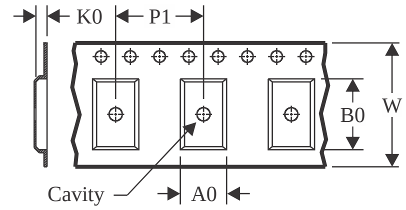
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

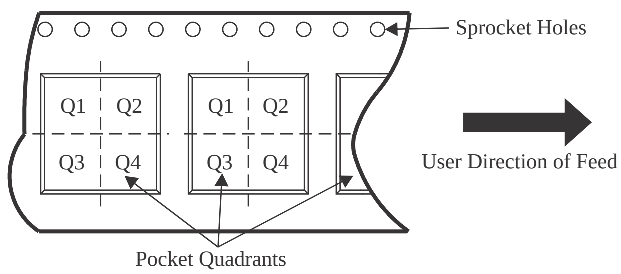


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

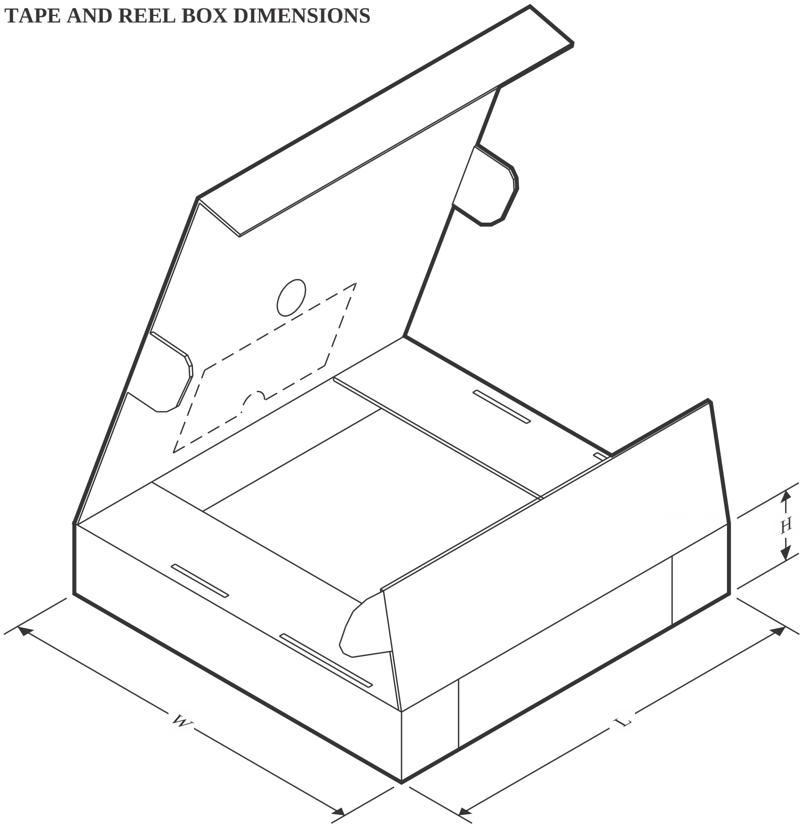
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2373AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2373AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2374AIDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2374AIDCNT	SOT-23	DCN	8	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA373AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA373AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA373AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA374AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4374AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4374AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4374AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4374AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

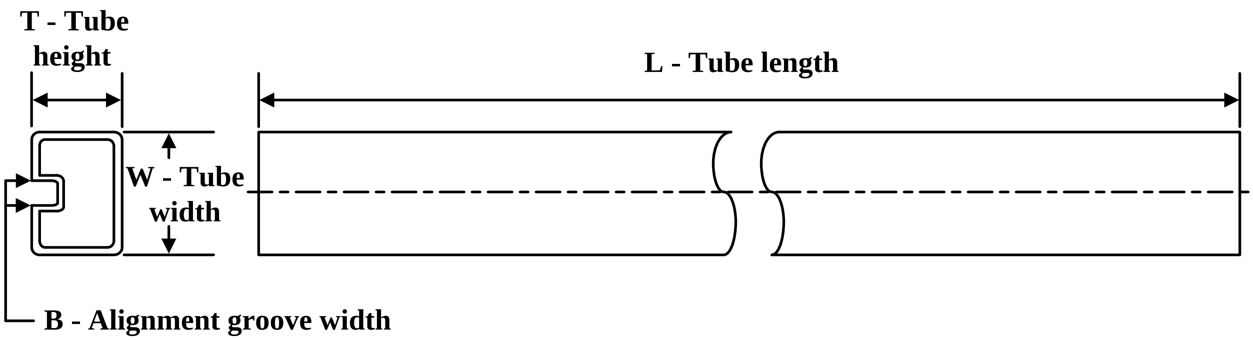
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2373AIDRCR	VSON	DRC	10	3000	356.0	356.0	35.0
OPA2373AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0
OPA2374AIDCNR	SOT-23	DCN	8	3000	210.0	185.0	35.0
OPA2374AIDCNT	SOT-23	DCN	8	250	210.0	185.0	35.0
OPA2374AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA373AIDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
OPA373AIDBVT	SOT-23	DBV	6	250	445.0	220.0	345.0
OPA373AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA374AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA374AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA374AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4374AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4374AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4374AIPWR	TSSOP	PW	14	2500	356.0	356.0	35.0
OPA4374AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

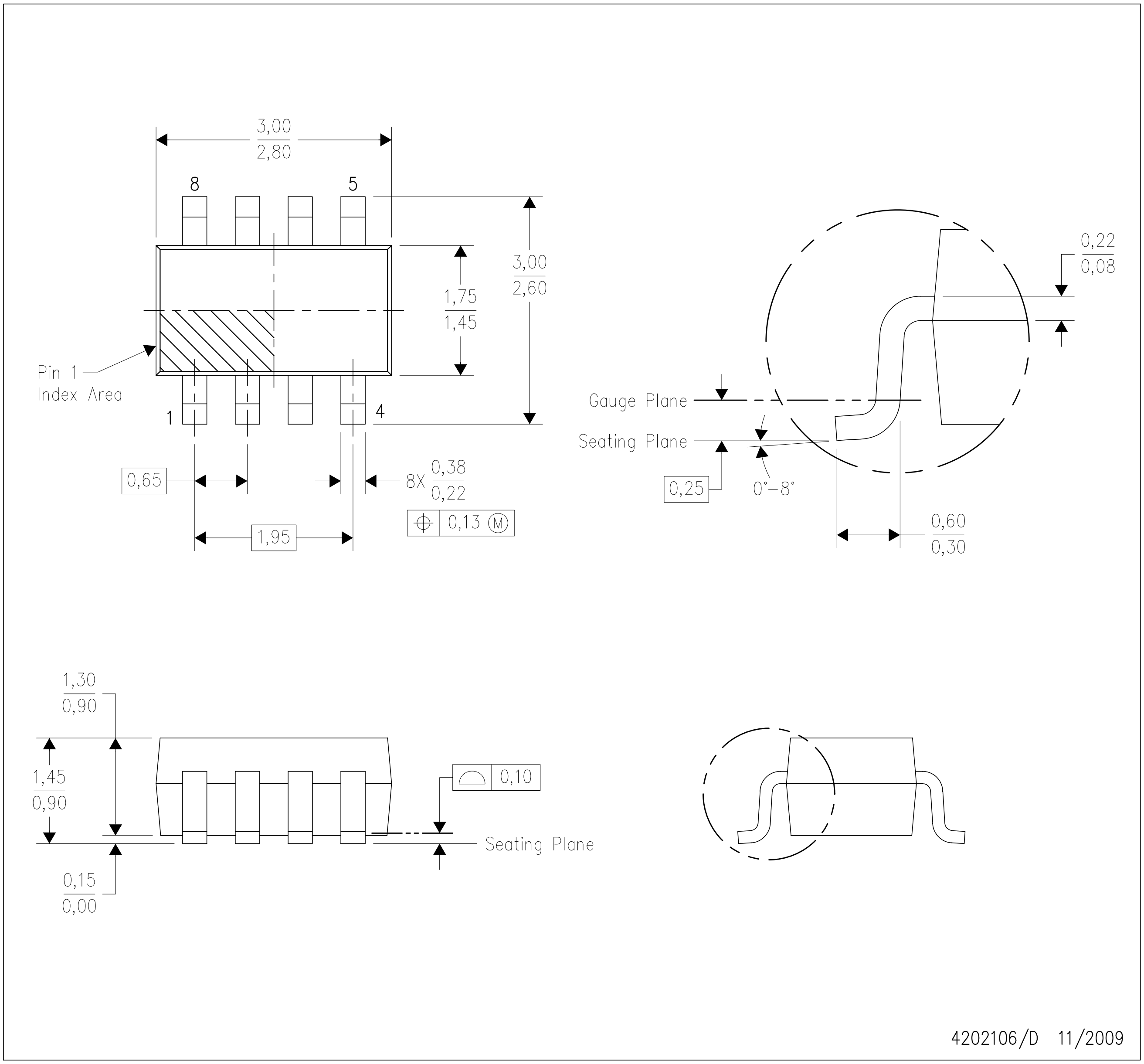
TUBE



*All dimensions are nominal

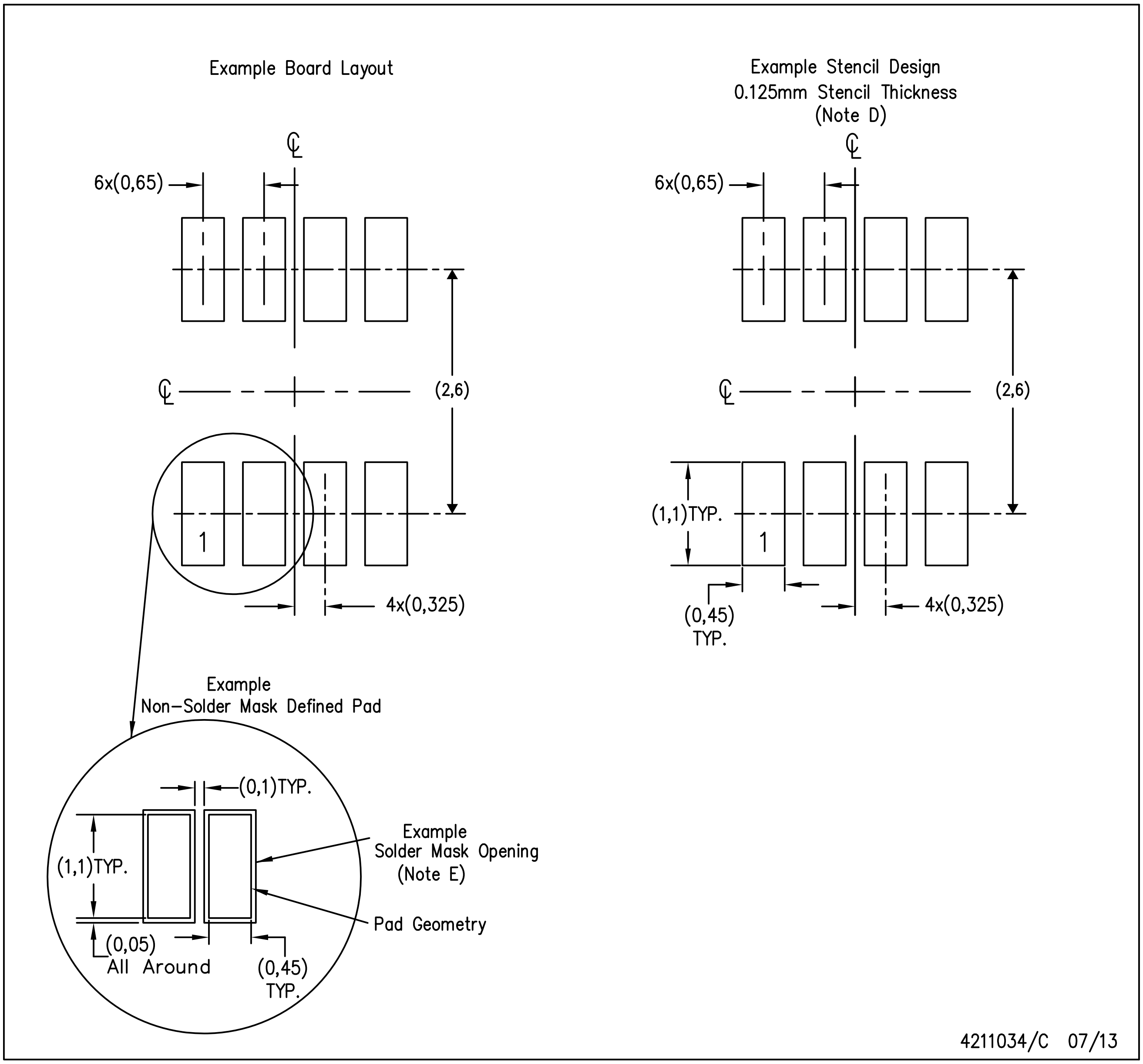
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2374AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2374AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2374AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA373AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA373AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA374AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA374AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4374AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4374AID.B	D	SOIC	14	50	506.6	8	3940	4.32

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

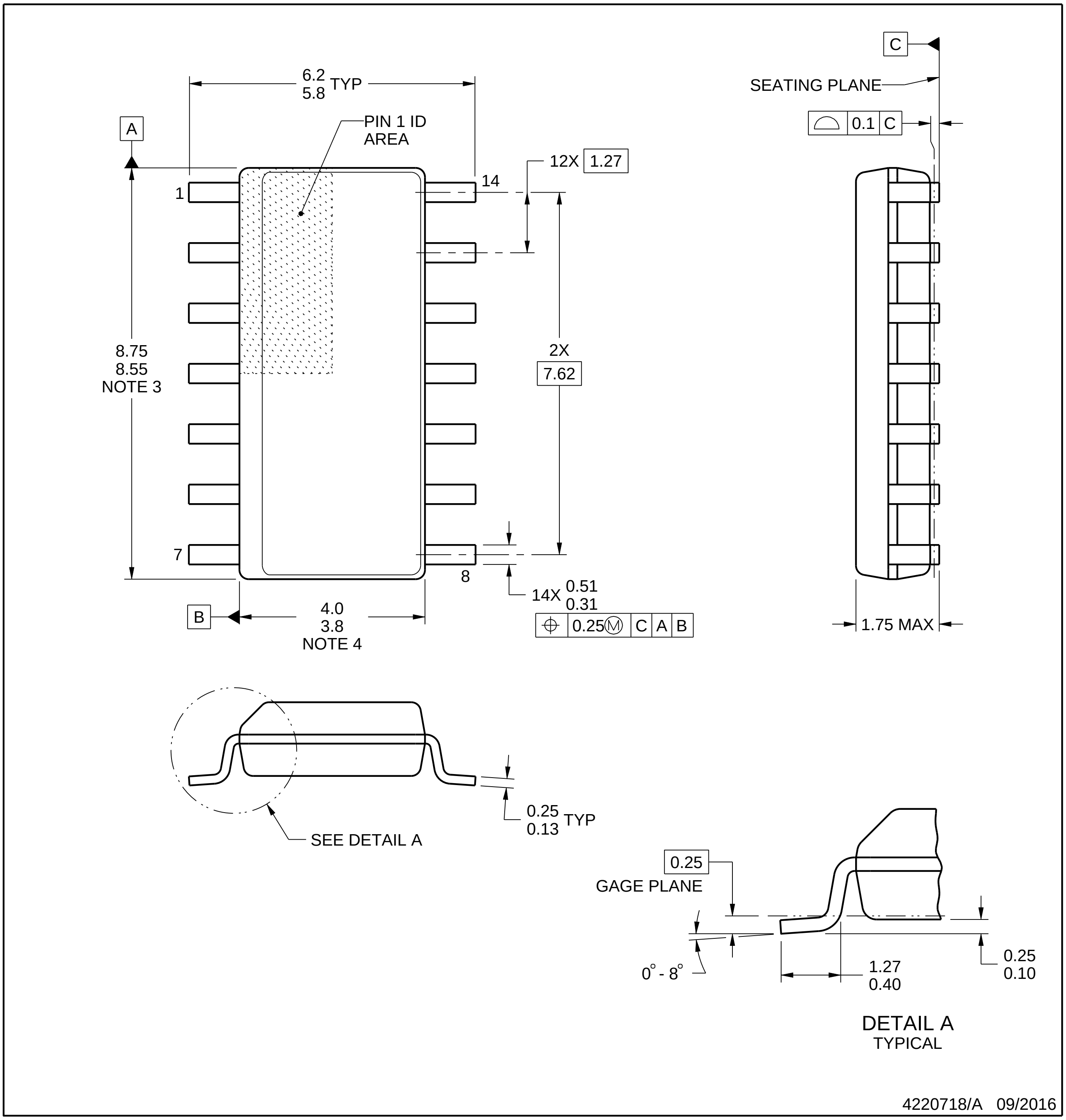


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

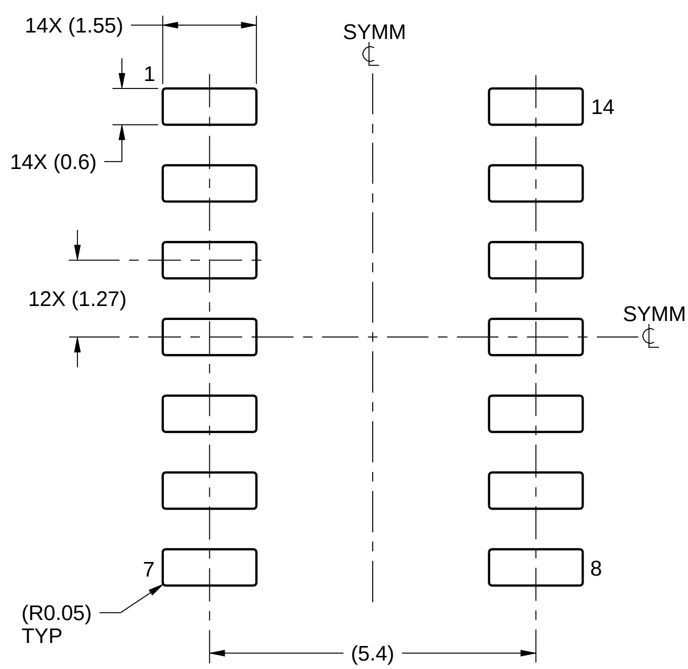


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

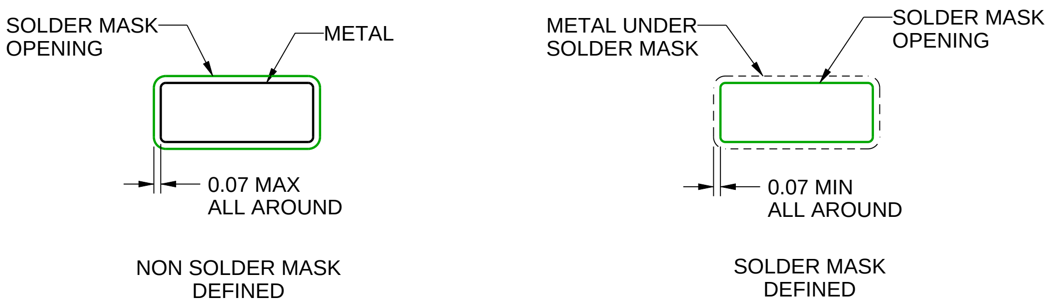


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

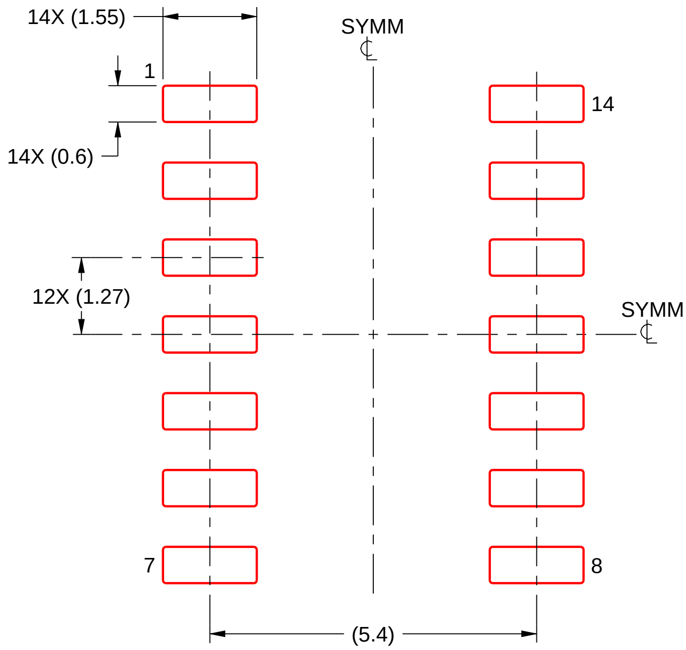


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

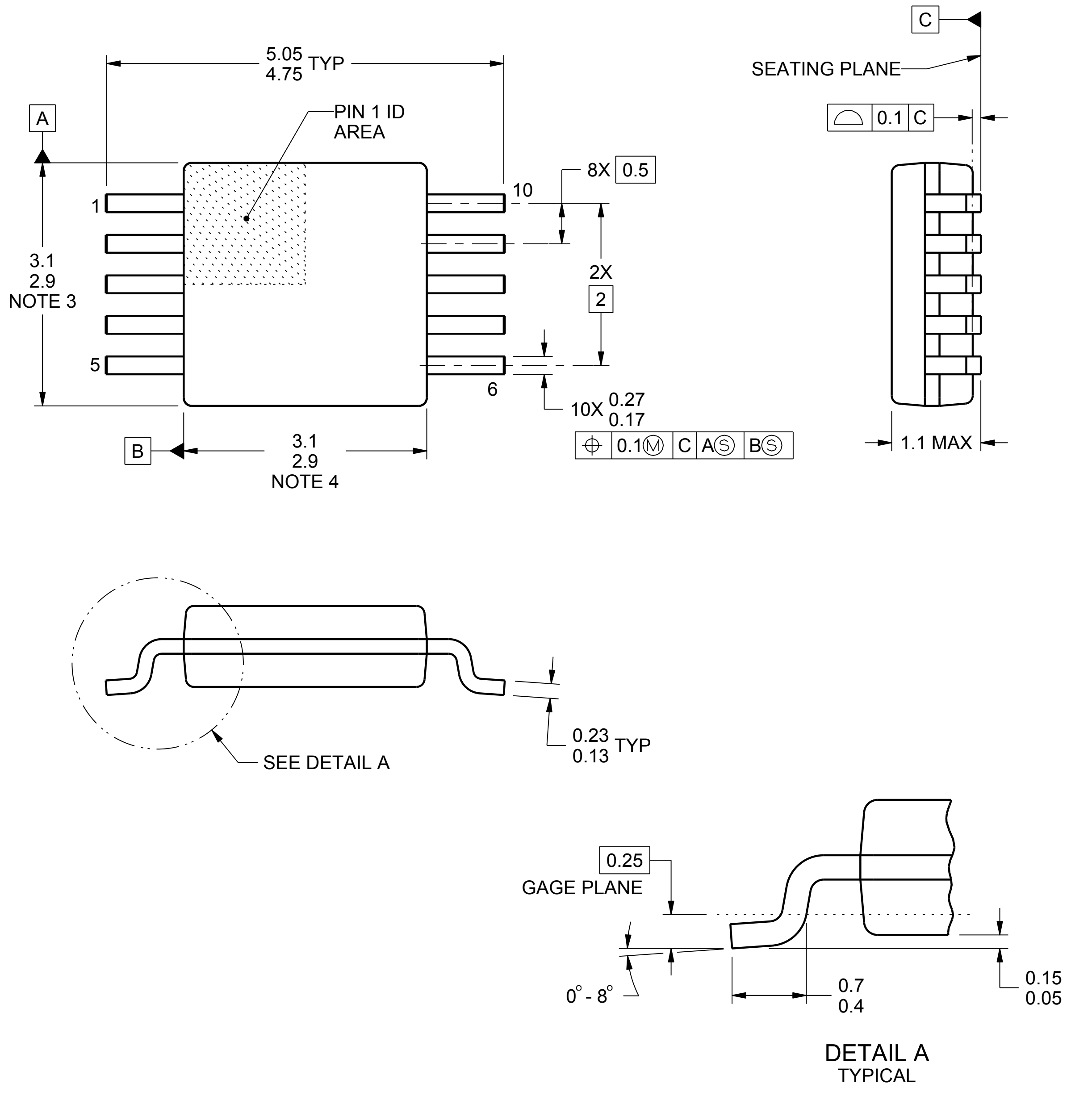


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

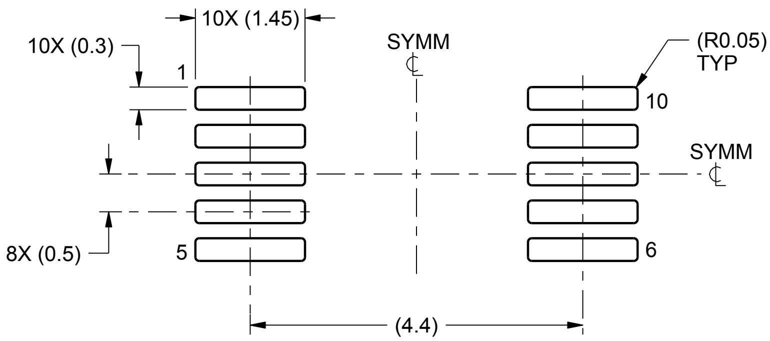
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



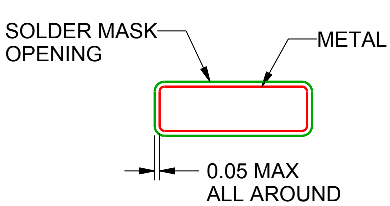
4221984/A 05/2015

NOTES:

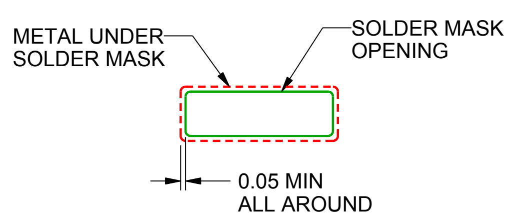
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED



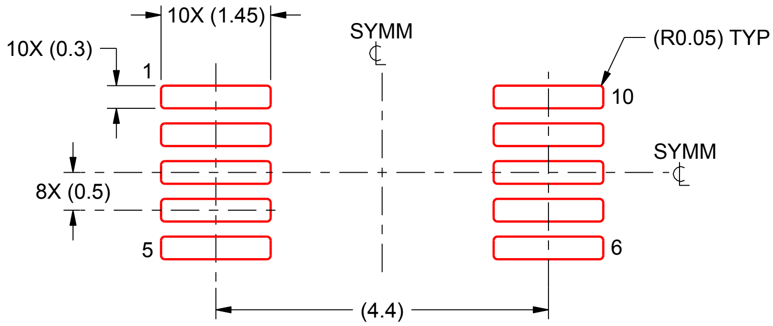
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

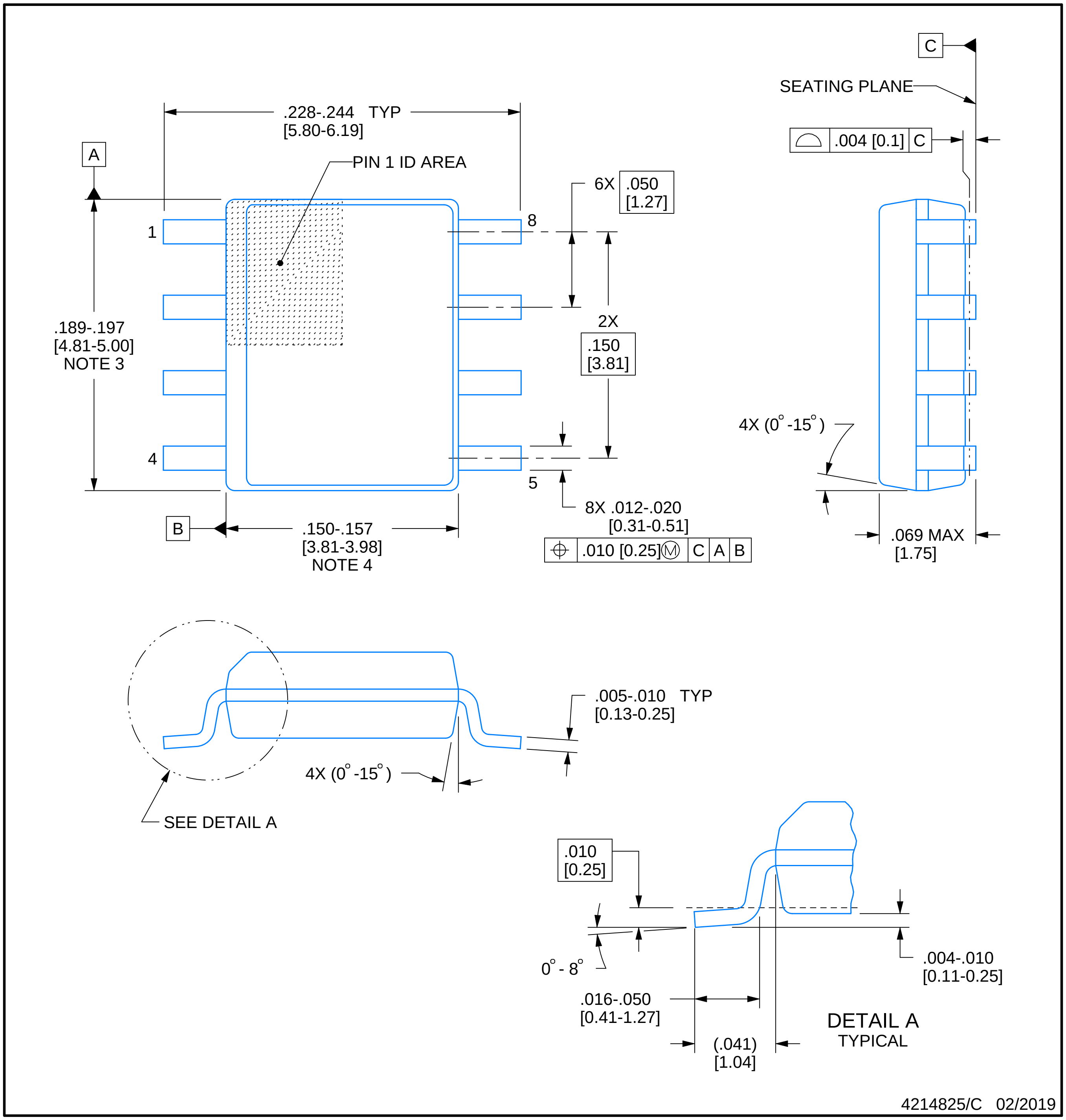


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

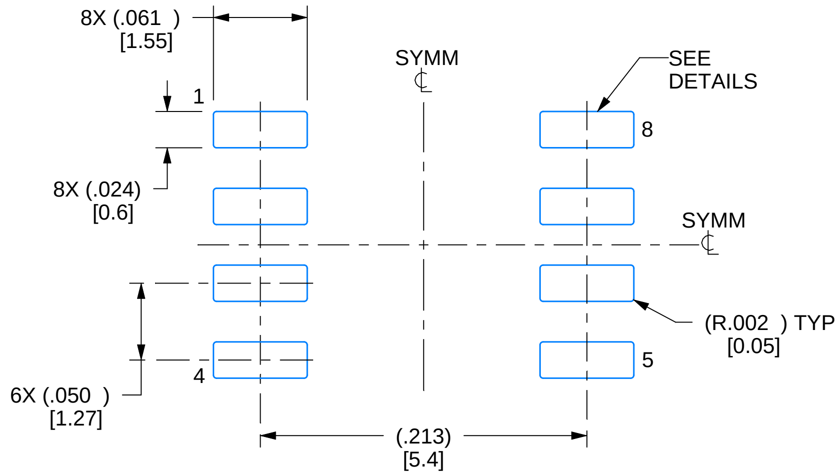
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



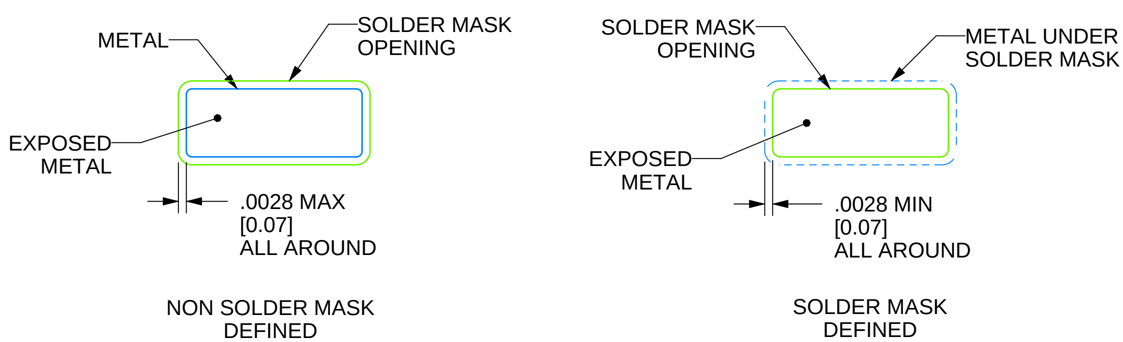
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

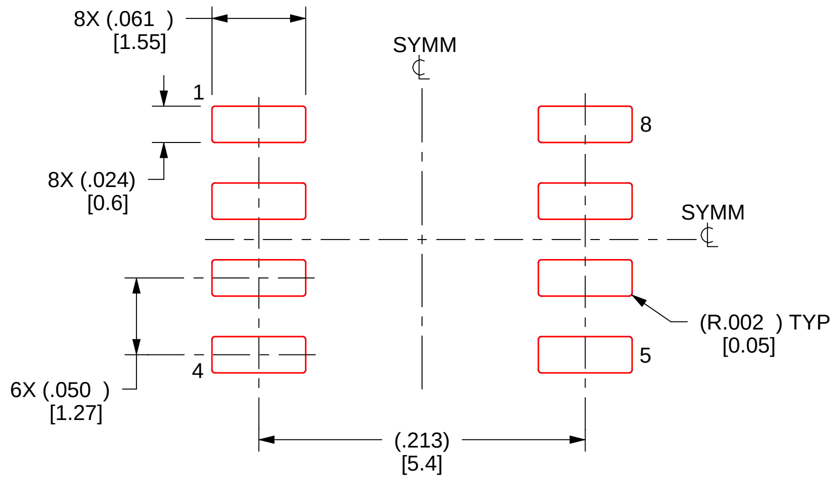


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

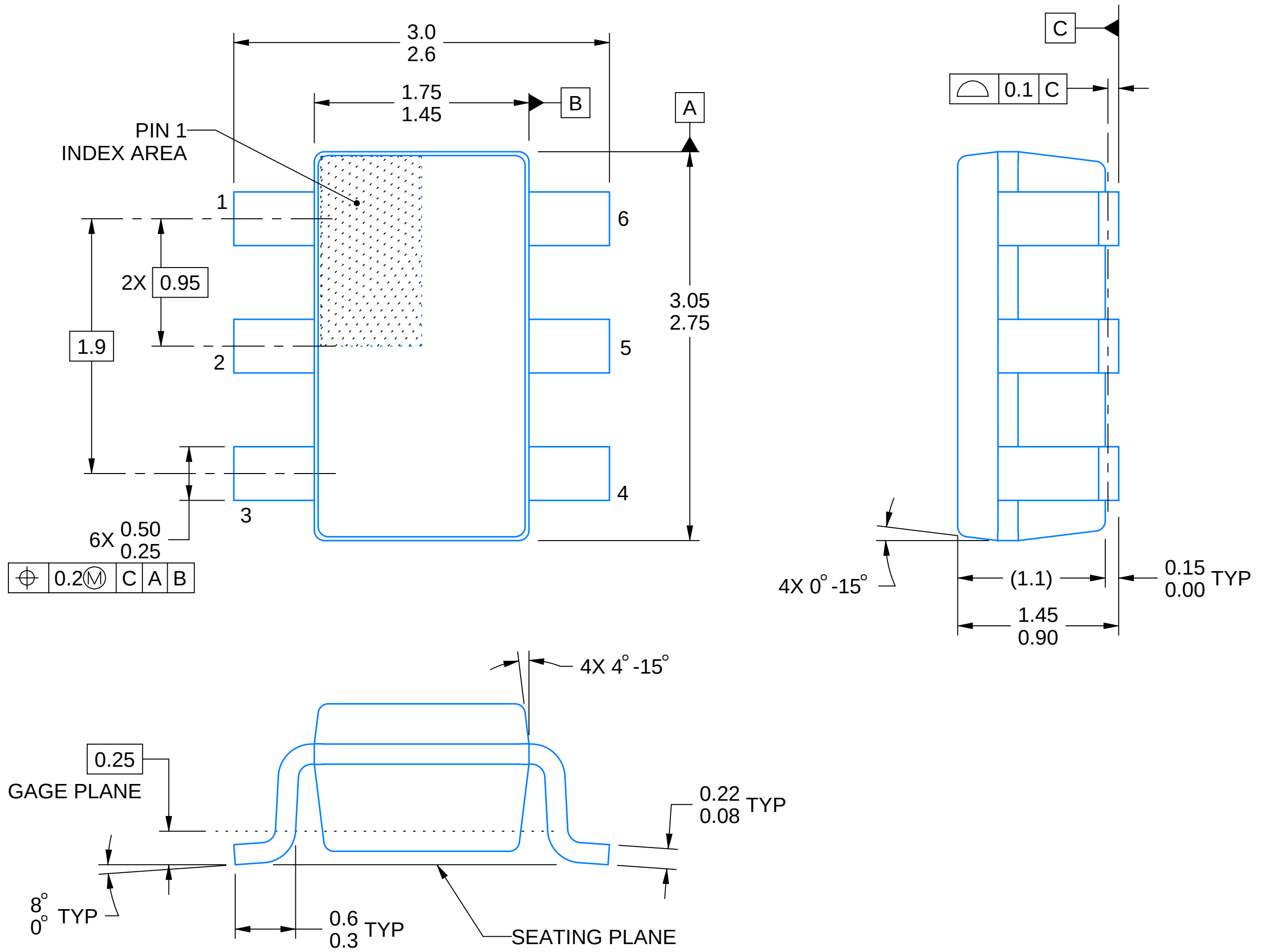


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

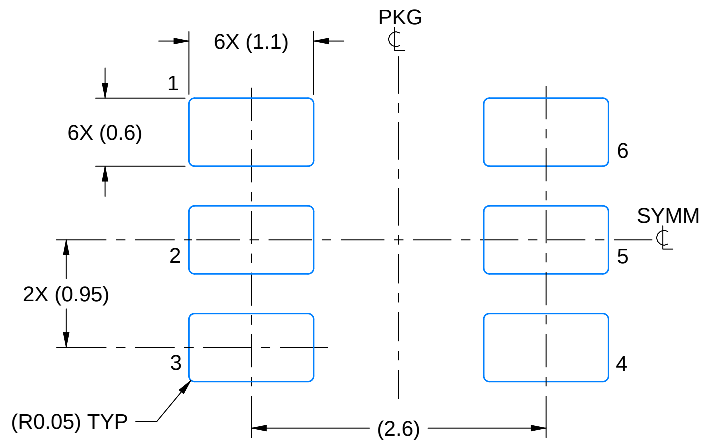
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



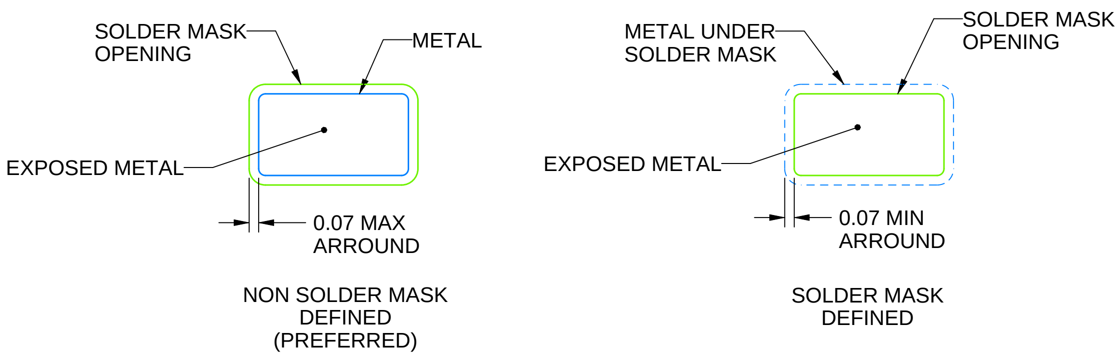
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

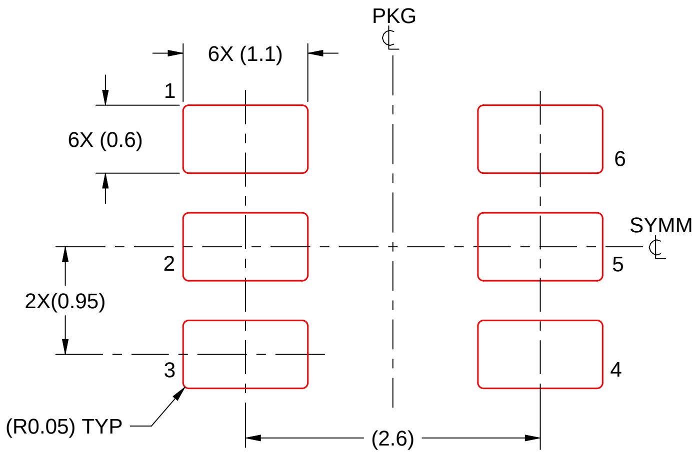


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



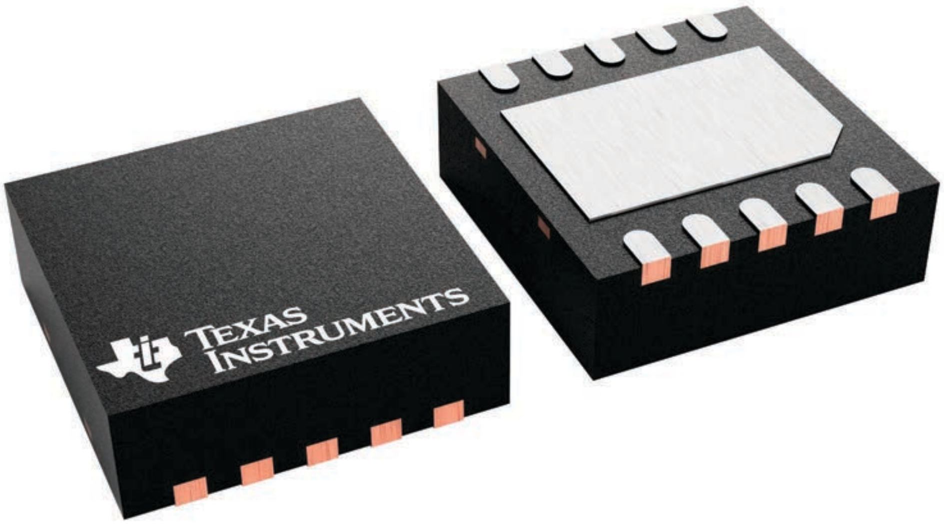
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

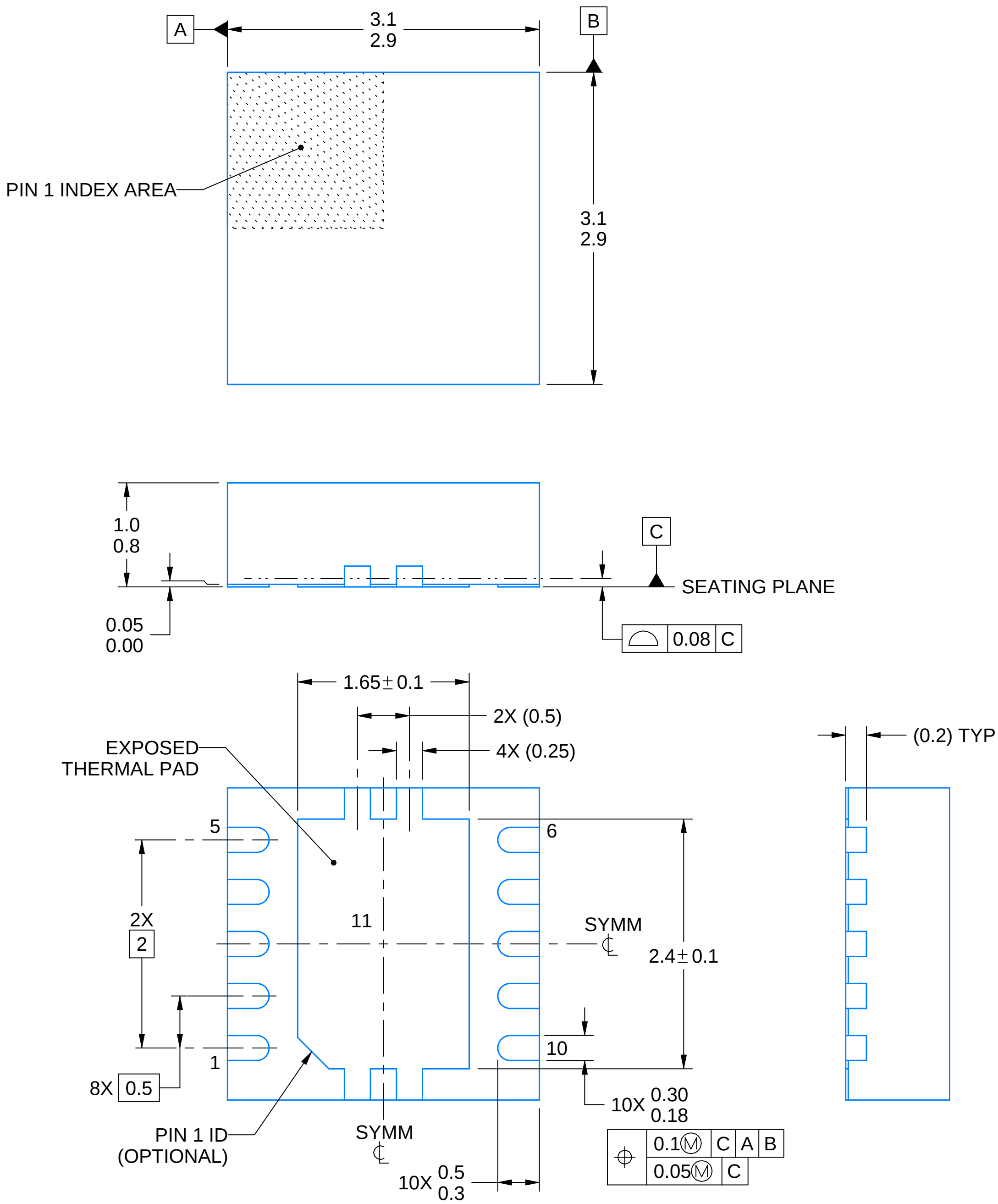
4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

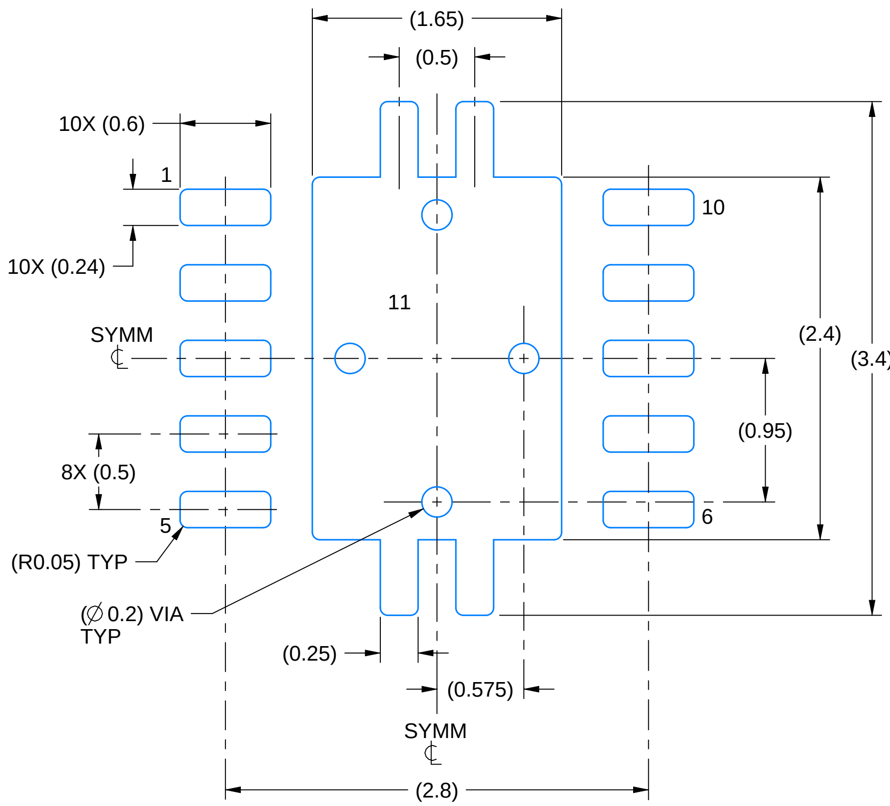




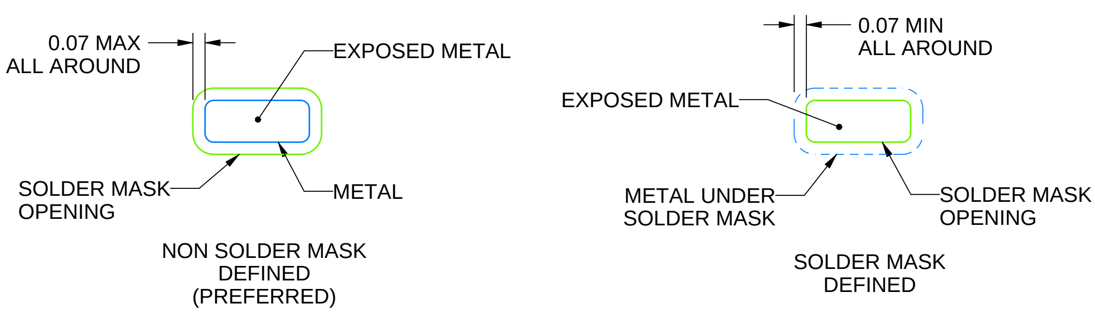
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

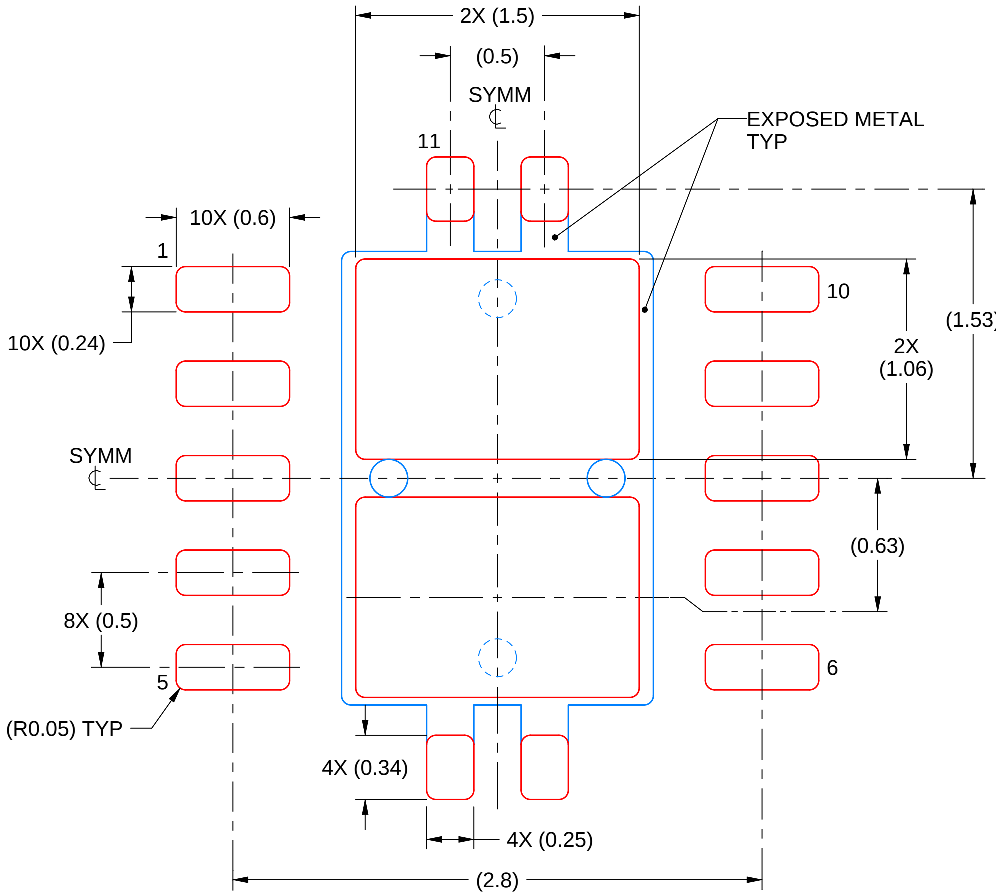


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



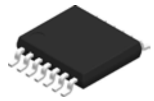
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

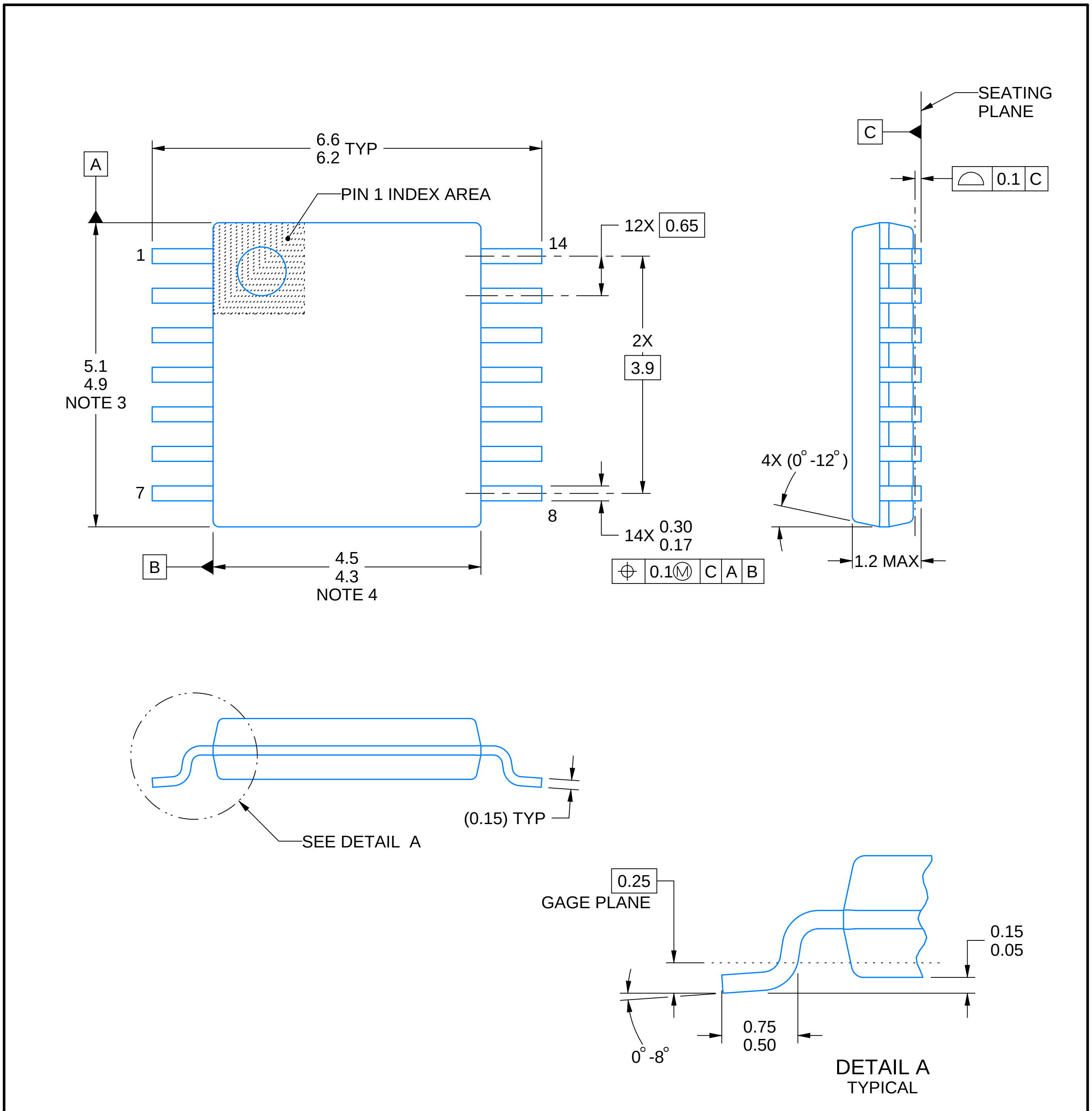
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

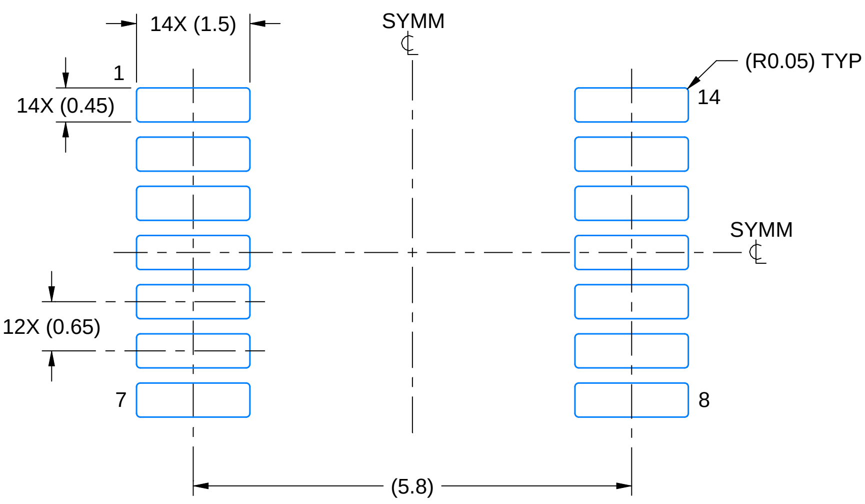
SMALL OUTLINE PACKAGE



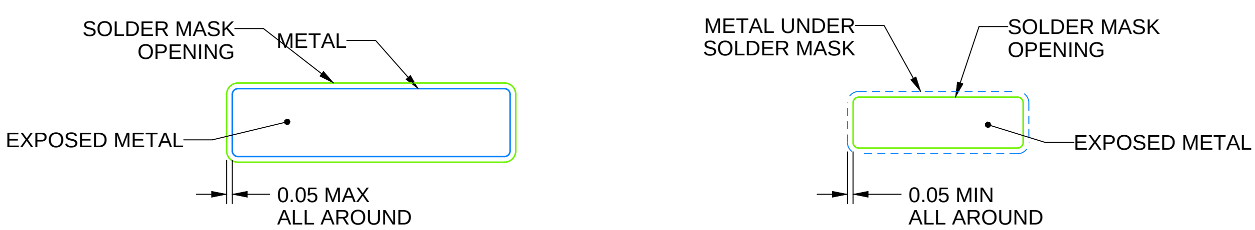
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

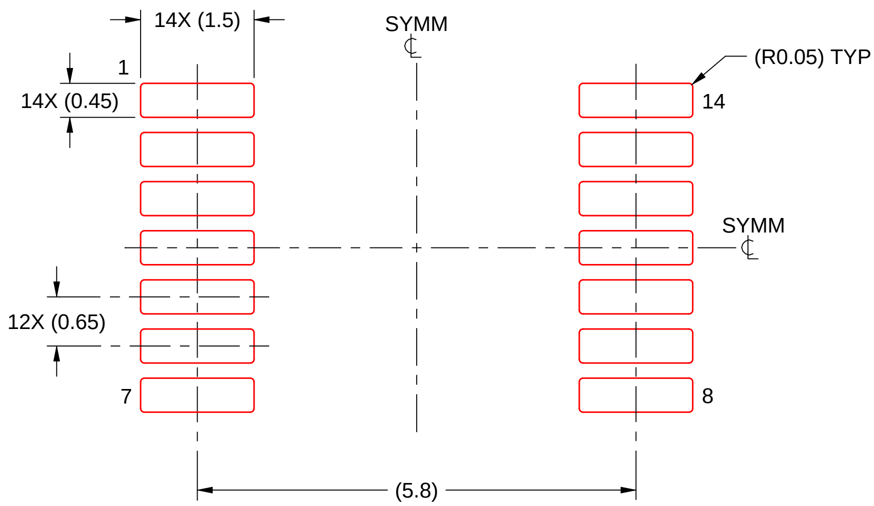
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



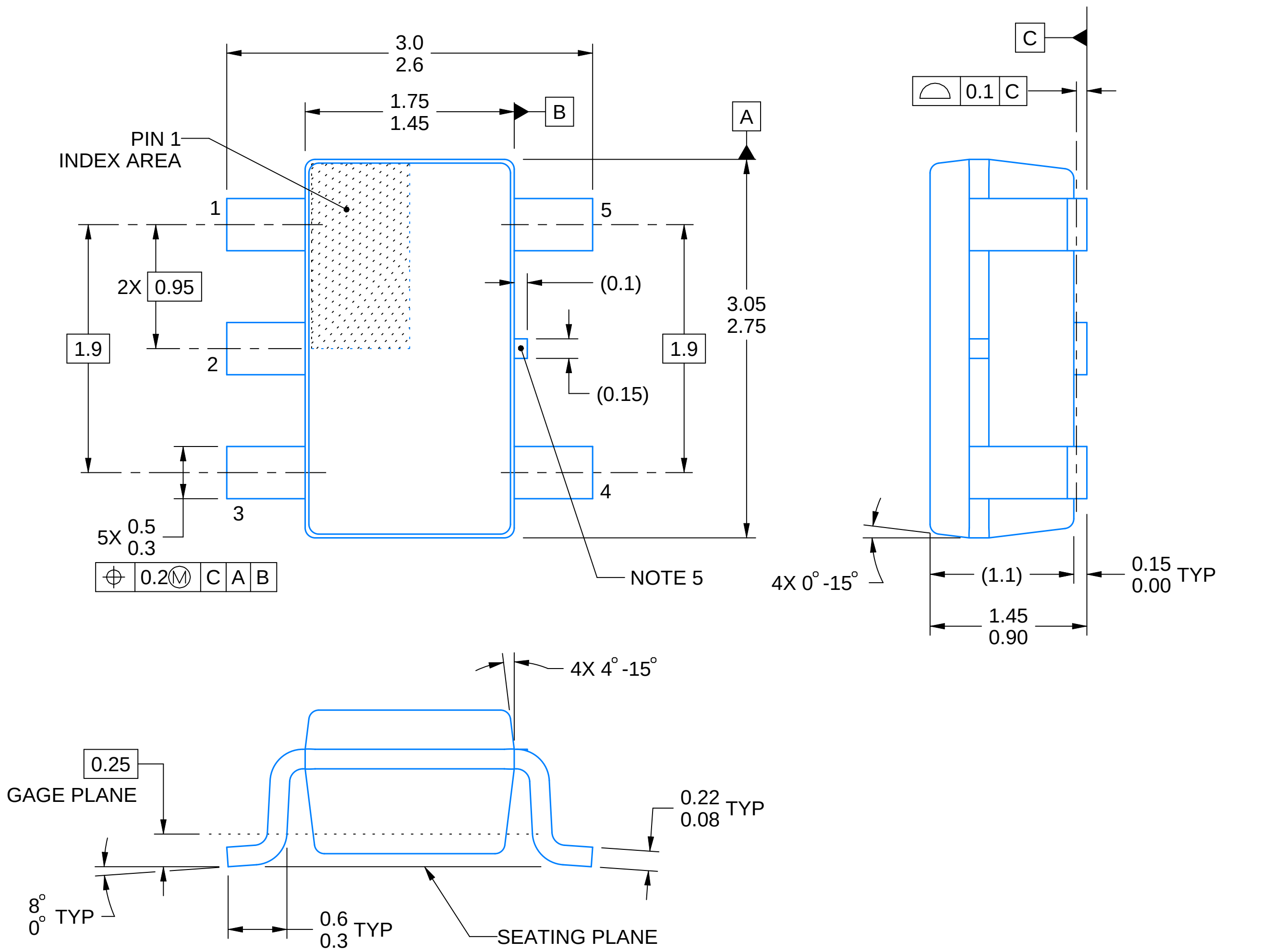
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

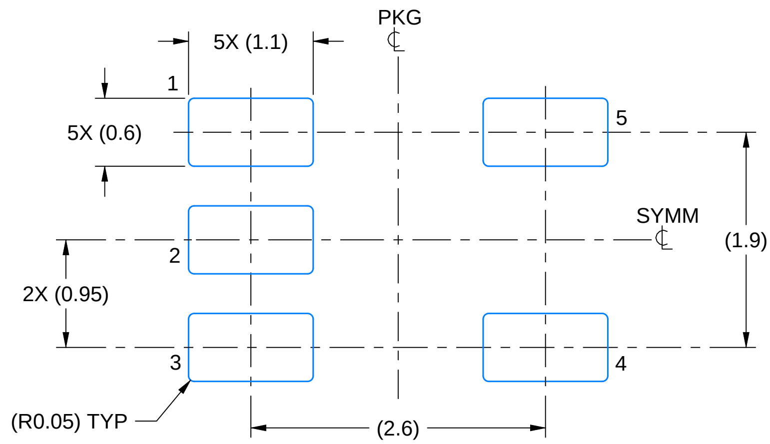
SMALL OUTLINE TRANSISTOR



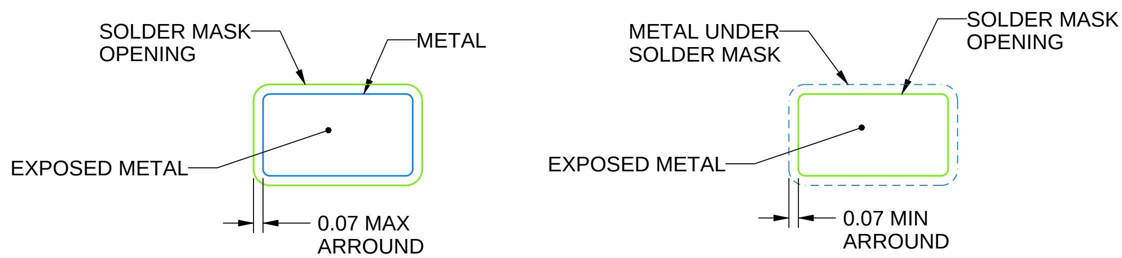
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

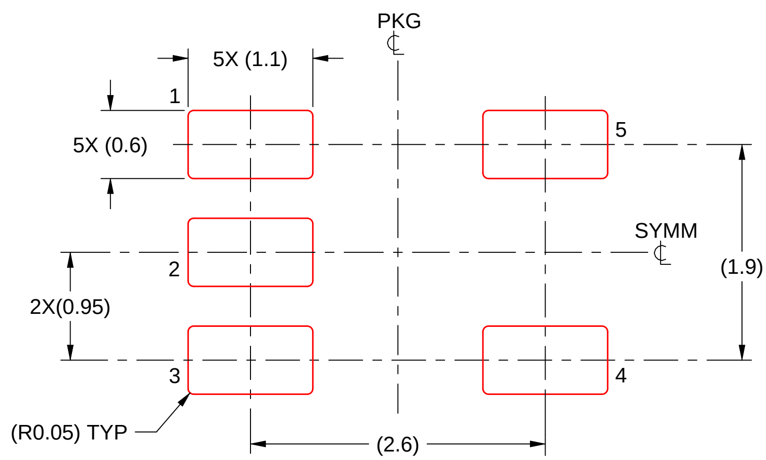


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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