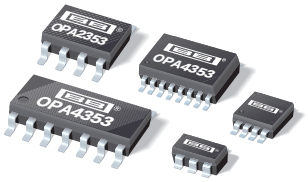
BURR - BROWN®




**OPA353**
**OPA2353**
**OPA4353**

For most current data sheet and other product information, visit www.burr-brown.com

# High-Speed, Single-Supply, Rail-to-Rail OPERATIONAL AMPLIFIERS

## *Micro*Amplifier™ Series

## FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 10mV)
- WIDE BANDWIDTH: 44MHz
- HIGH SLEW RATE: 22V/µs
- LOW NOISE: 5nV/√Hz
- LOW THD+NOISE: 0.0006%
- UNITY-GAIN STABLE
- *Micro*SIZE PACKAGES
- SINGLE, DUAL, AND QUAD

## APPLICATIONS

- CELL PHONE PA CONTROL LOOPS
- DRIVING A/D CONVERTERS
- VIDEO PROCESSING
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

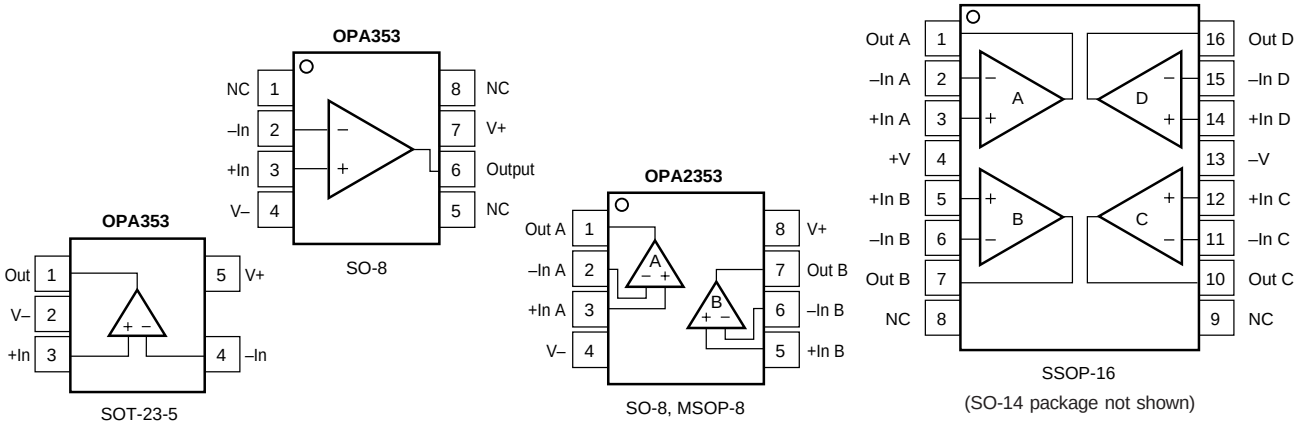
## DESCRIPTION

OPA353 series rail-to-rail CMOS operational amplifiers are designed for low cost, miniature applications. They are optimized for low voltage, single-supply operation. Rail-to-rail input/output, low noise (5nV/√Hz), and high speed operation (44MHz, 22V/µs) make them ideal for driving sampling analog-to-digital converters. They are also well suited for cell phone PA control loops and video processing (75Ω drive capability) as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for design flexibility.

The OPA353 series operates on a single supply as low as 2.5V with an input common-mode voltage range that extends 300mV beyond the supply rails. Output voltage swing is to within 10mV of the supply rails with a 10kΩ load. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The single (OPA353) packages are the tiny 5-lead SOT-23-5 surface mount and SO-8 surface mount. The dual (OPA2353) comes in the miniature MSOP-8 surface mount and SO-8 surface mount. The quad (OPA4353) packages are the space-saving SSOP-16 surface mount and SO-14 surface mount. All are specified from –40°C to +85°C and operate from –55°C to +125°C.

**SPICE Model available at www.burr-brown.com**

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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132


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SBOS103

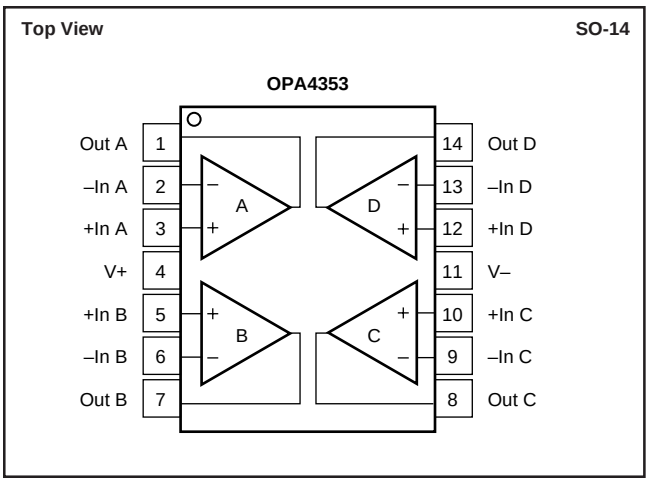
# SPECIFICATIONS: $V_S$ = 2.7V to 5.5V

At $T_A$ = +25°C, $R_L$ = 1kΩ connected to $V_S/2$ and $V_{OUT}$ = $V_S/2$, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C. $V_S$ = 5V.

| PARAMETER | | CONDITION | OPA353NA, UA<br>OPA2353EA, UA<br>OPA4353EA, UA<br>MIN | TYP[1] | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = 5V | | ±3 | ±8 | mV |
| **$T_A$ = –40°C to +85°C** | | | | | **±10** | mV |
| vs Temperature | | **$T_A$ = –40°C to +85°C** | | **±5** | | µV/°C |
| vs Power Supply Rejection Ratio | PSRR | $V_S$ = 2.7V to 5.5V, $V_{CM}$ = 0V | | 40 | 150 | µV/V |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = 2.7V to 5.5V, $V_{CM}$ = 0V | | | **175** | µV/V |
| Channel Separation (dual, quad) | | dc | | 0.15 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.5 | ±10 | pA |
| **$T_A$ = –40°C to +85°C** | | | | See Typical Curve | | |
| Input Offset Current | $I_{OS}$ | | | ±0.5 | ±10 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise, f = 100Hz to 400kHz | | | | 4 | | µVrms |
| Input Voltage Noise Density, f = 10kHz | $e_n$ | | | 7 | | nV/√Hz |
| f = 100kHz | | | | 5 | | nV/√Hz |
| Current Noise Density, f = 10kHz | $i_n$ | | | 4 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.1 | | (V+) + 0.1 | V |
| Common-Mode Rejection Ratio | CMRR | –0.1V < $V_{CM}$ < (V+) – 2.4V | 76 | 86 | | dB |
| | | $V_S$ = 5V, –0.1V < $V_{CM}$ < 5.1V | 60 | 74 | | dB |
| **$T_A$ = –40°C to +85°C** | | $V_S$ = 5V, –0.1V < $V_{CM}$ < 5.1V | **58** | | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 2.5 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 6.5 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 10kΩ, 50mV < $V_O$ < (V+) – 50mV | 100 | 122 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ, 50mV < $V_O$ < (V+) – 50mV | **100** | | | dB |
| | | $R_L$ = 1kΩ, 200mV < $V_O$ < (V+) – 200mV | 100 | 120 | | dB |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 1kΩ, 200mV < $V_O$ < (V+) – 200mV | **100** | | | dB |
| **FREQUENCY RESPONSE** | | $C_L$ = 100pF | | | | |
| Gain-Bandwidth Product | GBW | G = 1 | | 44 | | MHz |
| Slew Rate | SR | G = 1 | | 22 | | V/µs |
| Settling Time, 0.1% | | G = ±1, 2V Step | | 0.22 | | µs |
| 0.01% | | G = ±1, 2V Step | | 0.5 | | µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 0.1 | | µs |
| Total Harmonic Distortion + Noise | THD+N | $R_L$ = 600Ω, $V_O$ = 2.5Vp-p[2], G = 1, f = 1kHz | | 0.0006 | | % |
| Differential Gain Error | | G = 2, $R_L$ = 600Ω, $V_O$ = 1.4V[3] | | 0.17 | | % |
| Differential Phase Error | | G = 2, $R_L$ = 600Ω, $V_O$ = 1.4V[3] | | 0.17 | | deg |
| **OUTPUT** | | | | | | |
| Voltage Output Swing from Rail[4] | $V_{OUT}$ | $R_L$ = 10kΩ, $A_{OL}$ ≥ 100dB | | 10 | 50 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 10kΩ, $A_{OL}$ ≥ 100dB | | | **50** | mV |
| | | $R_L$ = 1kΩ, $A_{OL}$ ≥ 100dB | | 25 | 200 | mV |
| **$T_A$ = –40°C to +85°C** | | $R_L$ = 1kΩ, $A_{OL}$ ≥ 100dB | | | **200** | mV |
| Output Current | $I_{OUT}$ | | | ±40[5] | | mA |
| Short-Circuit Current | $I_{SC}$ | | | ±80 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Operating Voltage Range | $V_S$ | **$T_A$ = –40°C to +85°C** | **2.7** | | **5.5** | V |
| Minimum Operating Voltage | | | | 2.5 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $I_O$ = 0 | | 5.2 | 8 | mA |
| **$T_A$ = –40°C to +85°C** | | $I_O$ = 0 | | | **9** | mA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +85 | °C |
| Operating Range | | | –55 | | +125 | °C |
| Storage Range | | | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SOT-23-5 | | | | 200 | | °C/W |
| MSOP-8 Surface Mount | | | | 150 | | °C/W |
| SO-8 Surface Mount | | | | 150 | | °C/W |
| SSOP-16 Surface Mount | | | | 100 | | °C/W |
| SO-14 Surface Mount | | | | 100 | | °C/W |

NOTES: (1) $V_S$ = +5V. (2) $V_{OUT}$ = 0.25V to 2.75V. (3) NTSC signal generator used. See Figure 6 for test circuit. (4) Output voltage swings are measured between the output and power supply rails. (5) See typical performance curve, "Output Voltage Swing vs Output Swing."

## PIN CONFIGURATION




## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | 5.5V |
| Signal Input Terminals, Voltage[2] | (V–) – 0.3V to (V+) + 0.3V |
| Current[2] | 10mA |
| Output Short-Circuit[3] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short circuit to ground, one amplifier per package.

## PACKAGE/ORDERING INFORMATION

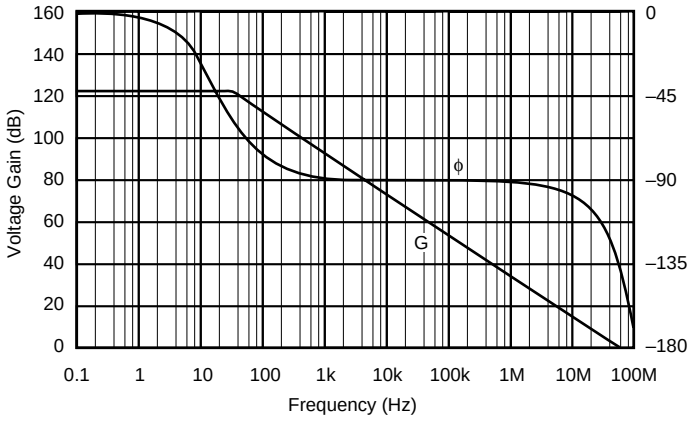
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| **Single** | | | | | | |
| OPA353NA | 5-Lead SOT-23-5 | 331 | –40°C to +85°C | D53 | OPA353NA/250 | Tape and Reel |
| " | " | " | " | " | OPA353NA/3K | Tape and Reel |
| OPA353UA | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA353UA | OPA353UA | Rails |
| " | " | " | " | " | OPA353UA/2K5 | Tape and Reel |
| **Dual** | | | | | | |
| OPA2353EA | MSOP-8 Surface Mount | 337 | –40°C to +85°C | E53 | OPA2353EA/250 | Tape and Reel |
| " | " | " | " | " | OPA2353EA/2K5 | Tape and Reel |
| OPA2353UA | SO-8 Surface Mount | 182 | –40°C to +85°C | OPA2353UA | OPA2353UA | Rails |
| " | " | " | " | " | OPA2353UA/2K5 | Tape and Reel |
| **Quad** | | | | | | |
| OPA4353EA | SSOP-16 Surface Mount | 322 | –40°C to +85°C | OPA4353EA | OPA4353EA/250 | Tape and Reel |
| " | " | " | " | " | OPA4353EA/2K5 | Tape and Reel |
| OPA4353UA | SO-14 Surface Mount | 235 | –40°C to +85°C | OPA4353UA | OPA4353UA | Rails |
| " | " | " | " | " | OPA4353UA/2K5 | Tape and Reel |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA2353EA/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

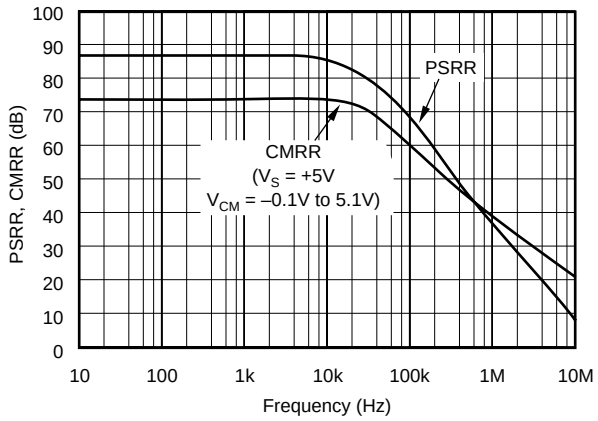
# TYPICAL PERFORMANCE CURVES

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 1kΩ connected to $V_S$/2, unless otherwise noted.

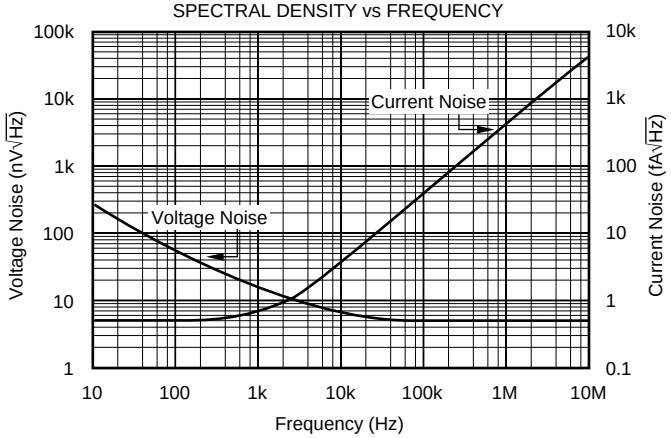
OPEN-LOOP GAIN/PHASE vs FREQUENCY



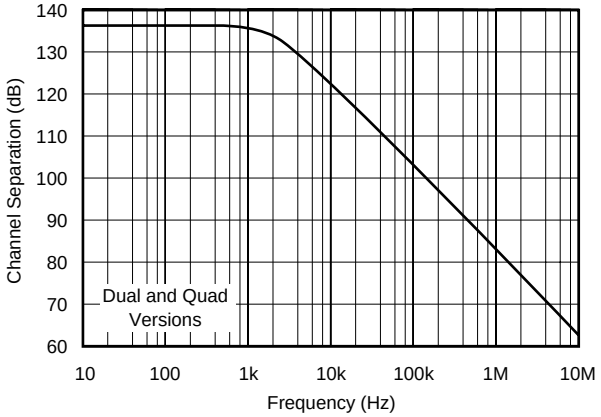

POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



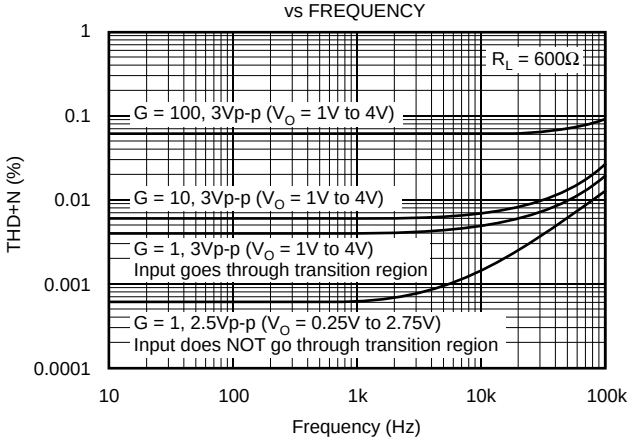

INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



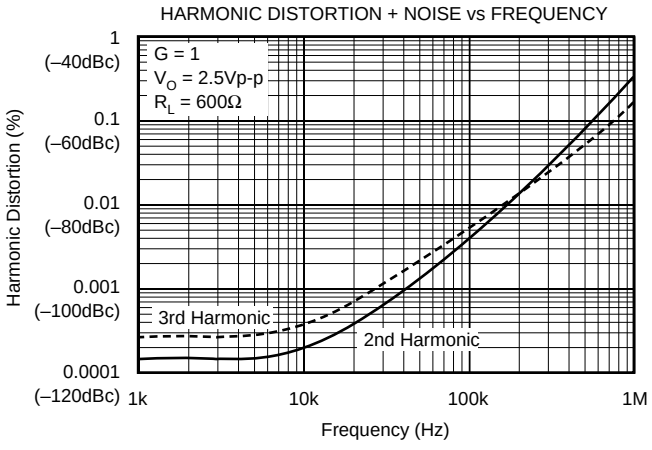

CHANNEL SEPARATION vs FREQUENCY




TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



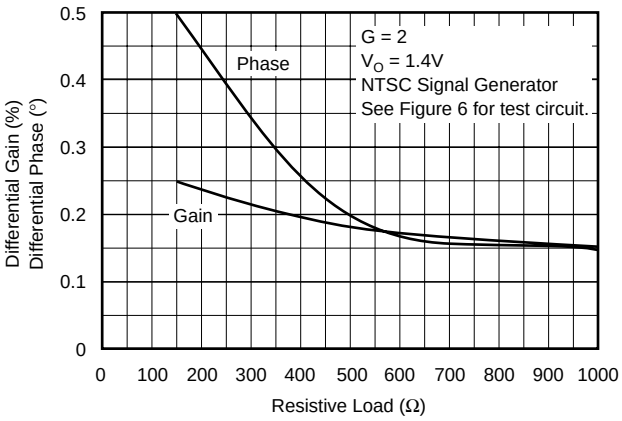

HARMONIC DISTORTION + NOISE vs FREQUENCY



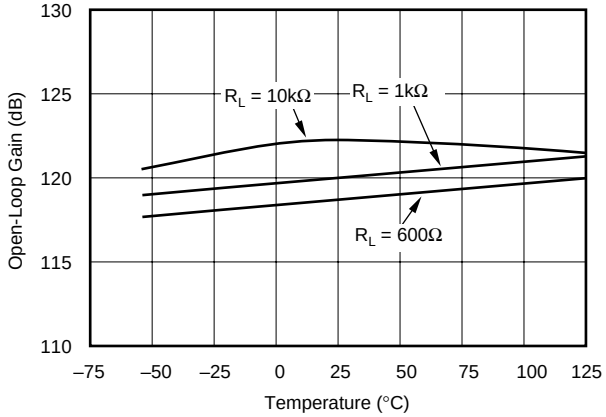
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 1kΩ connected to $V_S$/2, unless otherwise noted.

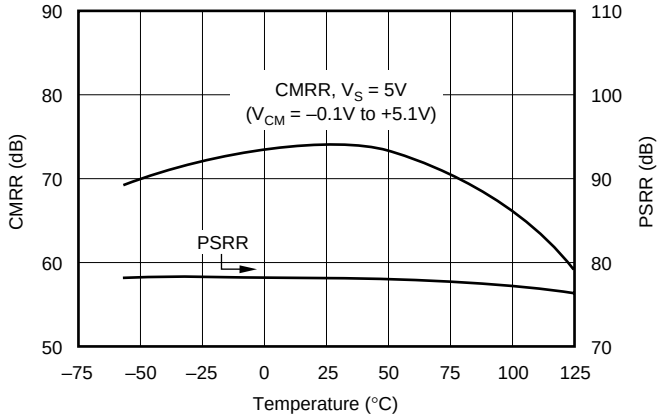
DIFFERENTIAL GAIN/PHASE vs RESISTIVE LOAD



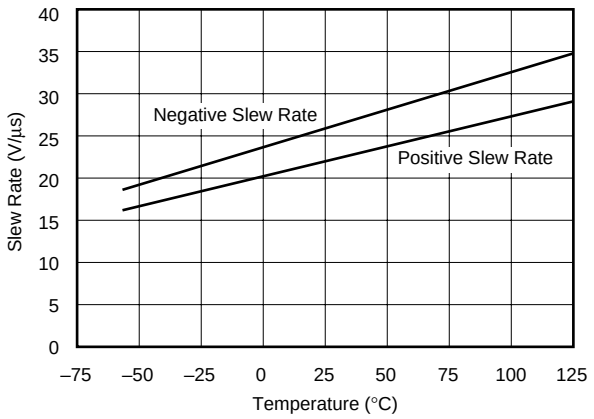

OPEN-LOOP GAIN vs TEMPERATURE



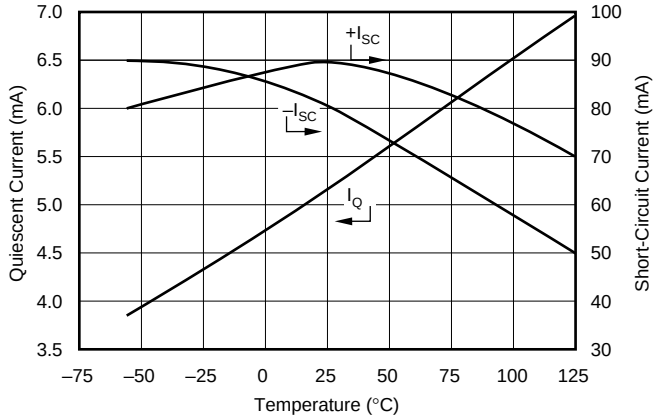

COMMON-MODE AND POWER SUPPLY REJECTION RATIO vs TEMPERATURE



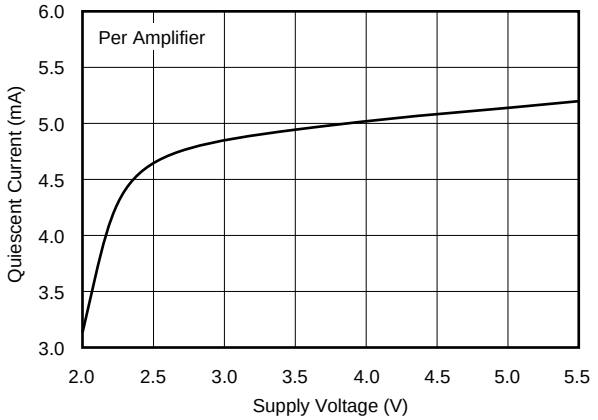

SLEW RATE vs TEMPERATURE




QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



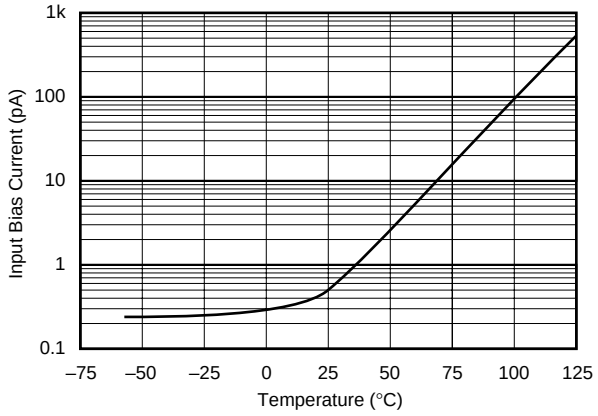

QUIESCENT CURRENT vs SUPPLY VOLTAGE



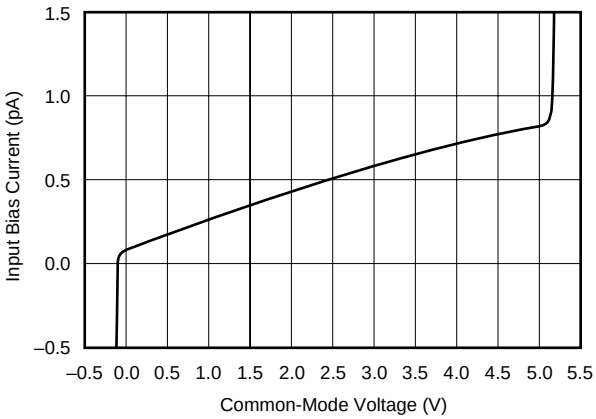
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 1kΩ connected to $V_S$/2, unless otherwise noted.

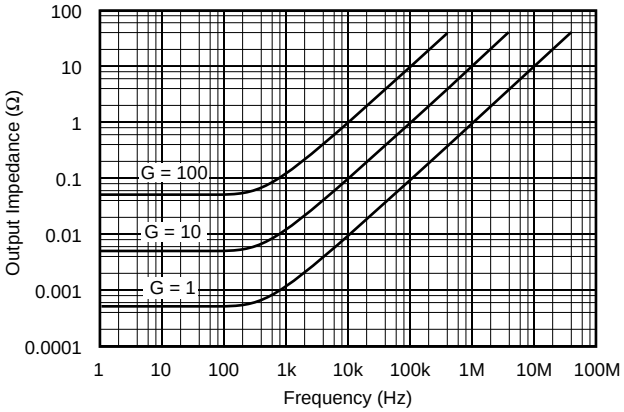
INPUT BIAS CURRENT vs TEMPERATURE



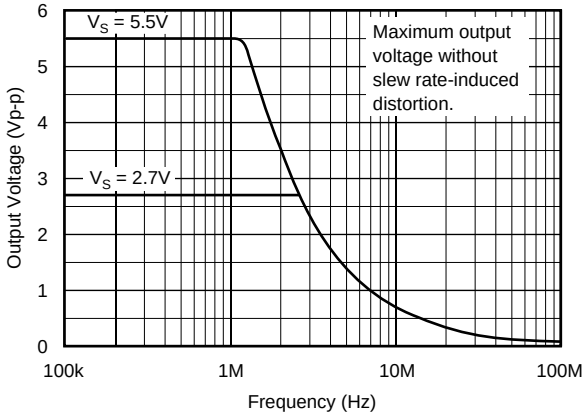

INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



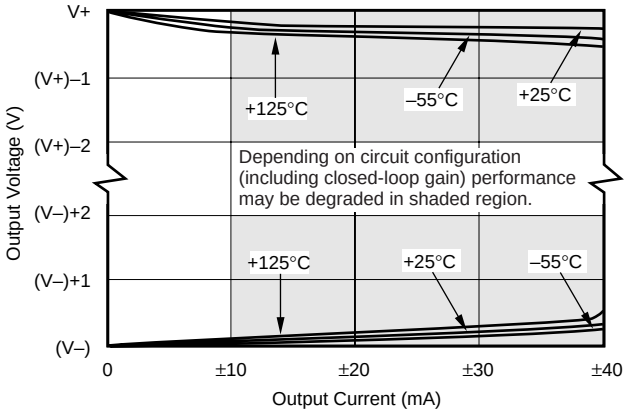

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



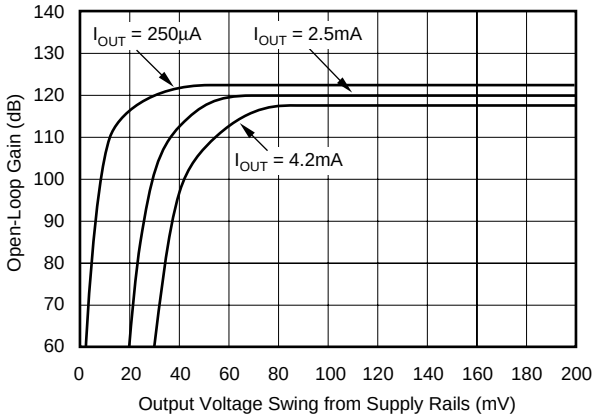

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY




OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



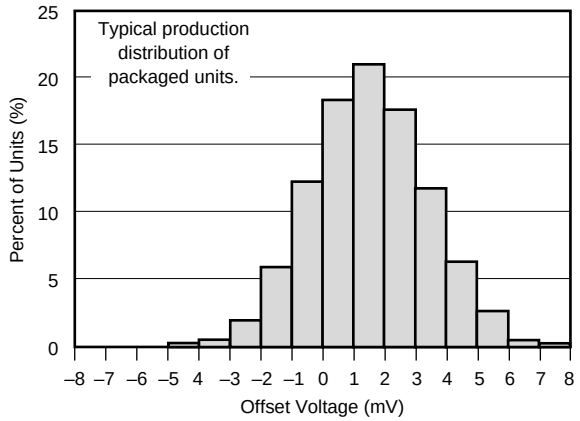

OPEN-LOOP GAIN vs OUTPUT VOLTAGE SWING



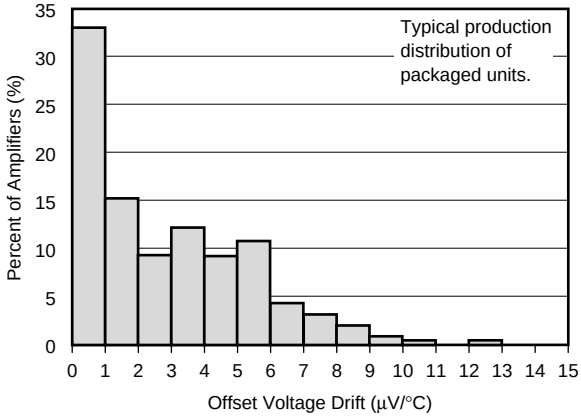
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 1kΩ connected to $V_S$/2, unless otherwise noted.

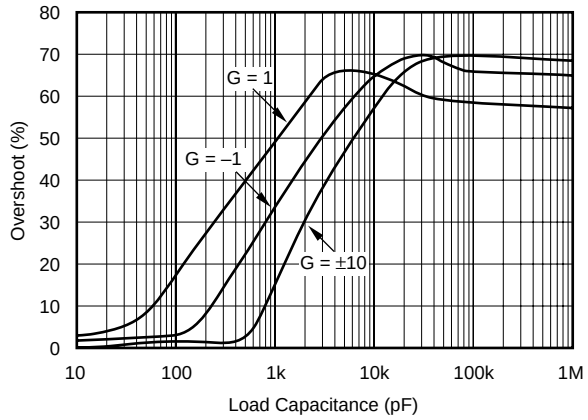
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



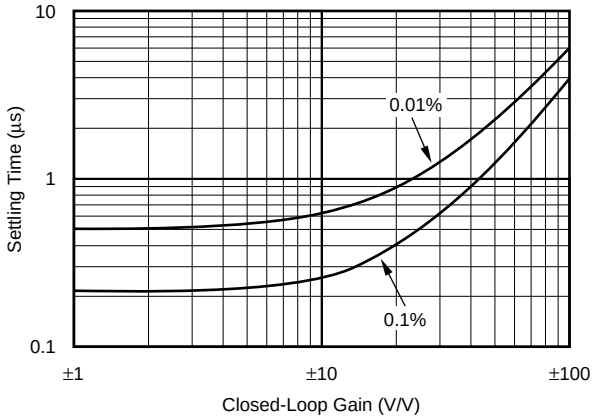

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



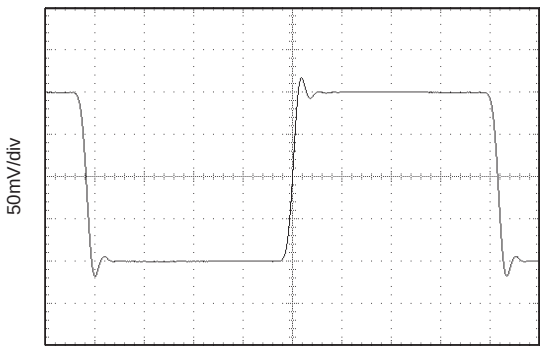

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



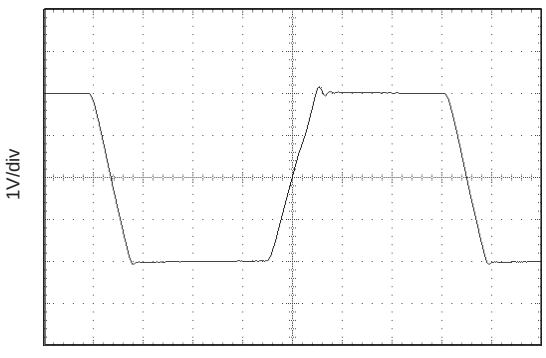

SETTLING TIME vs CLOSED-LOOP GAIN




SMALL-SIGNAL STEP RESPONSE
$C_L$ = 100pF




LARGE-SIGNAL STEP RESPONSE
$C_L$ = 100pF



# APPLICATIONS INFORMATION

OPA353 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general purpose applications. Rail-to-rail input/output make them ideal for driving sampling A/D converters. They are well suited for controlling the output power in cell phones. These applications often require high speed and low noise. In addition, the OPA353 series offers a low cost solution for general purpose and consumer video applications (75Ω drive capability).

Excellent ac performance makes the OPA353 series well suited for audio applications. Their bandwidth, slew rate, low noise ($5nV/\sqrt{Hz}$), low THD (0.0006%), and small package options are ideal for these applications. The class AB output stage is capable of driving 600Ω loads connected to any point between V+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low voltage supply applications. Figure 1 shows the input and output waveforms for the OPA353 in unity-gain configuration. Operation is from a single +5V supply with a 1kΩ load connected to $V_S/2$. The input is a 5Vp-p sinusoid. Output voltage is approximately 4.95Vp-p.

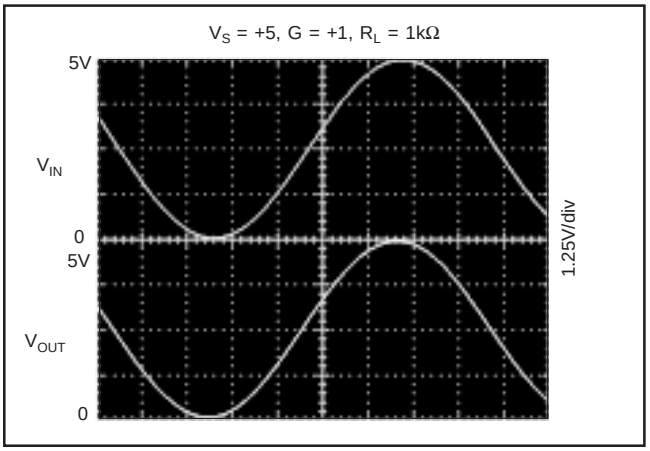



FIGURE 1. Rail-to-Rail Input and Output.

Power supply pins should be bypassed with 0.01µF ceramic capacitors.

## OPERATING VOLTAGE

OPA353 series op amps are fully specified from +2.7V to +5.5V. However, supply voltage may range from +2.5V to +5.5V. Parameters are guaranteed over the specified supply range—a unique feature of the OPA353 series. In addition, many specifications apply from –40°C to +85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltages or temperature are shown in the typical performance curves.

## RAIL-TO-RAIL INPUT

The guaranteed input common-mode voltage range of the OPA353 series extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.8V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) – 1.8V. There is a small transition region, typically (V+) – 2V to (V+) – 1.6V, in which both pairs are on. This 400mV transition region can vary ±400mV with process variation. Thus, the transition region (both input stages on) can range from (V+) – 2.4V to (V+) – 2.0V on the low end, up to (V+) – 1.6V to (V+) – 1.2V on the high end.

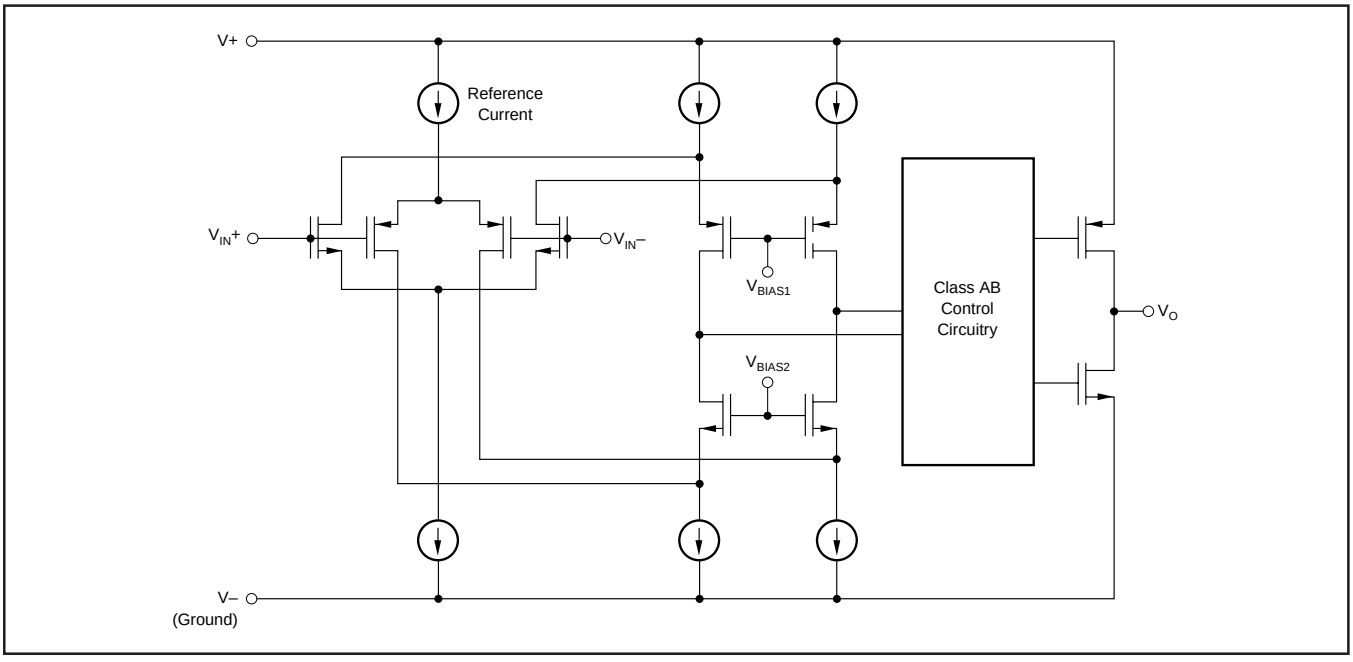



FIGURE 2. Simplified Schematic.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 500fA. However, large inputs (greater than 300mV beyond the supply rails) can turn on the OPA353's input protection diodes, causing excessive current to flow in or out of the input pins. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor as shown in Figure 3. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

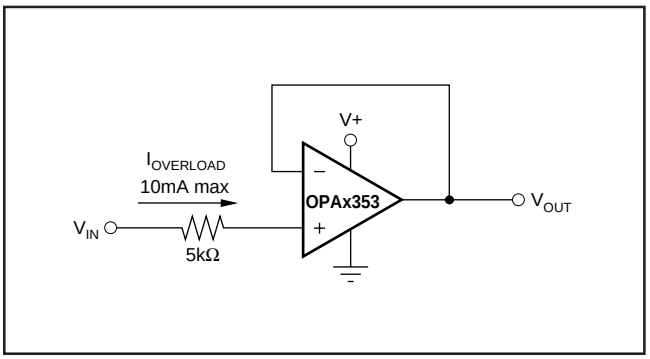



FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage.

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (>10kΩ), the output voltage swing is typically ten millivolts from the supply rails. With heavier resistive loads (600Ω to 10kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See the typical performance curves "Output Voltage Swing vs Output Current" and "Open-Loop Gain vs Output Voltage."

## CAPACITIVE LOAD AND STABILITY

OPA353 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp's output impedance, along with any additional load resistance, to create a pole in the small-signal response which degrades the phase margin.

In unity gain, OPA353 series op amps perform well with large capacitive loads. Increasing gain enhances the amplifier's ability to drive more capacitance. The typical performance curve "Small-Signal Overshoot vs Capacitive Load" shows performance with a 1kΩ resistive load. Increasing load resistance improves capacitive load drive capability.

## FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, $R_F$, as shown in Figure 4. This capacitor compensates for the zero created by the feedback network impedance and the OPA353's input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

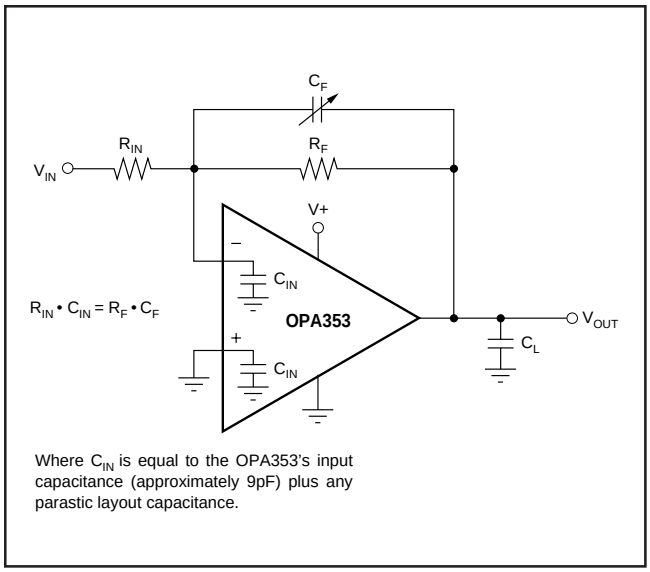



FIGURE 4. Feedback Capacitor Improves Dynamic Performance.

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 4, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA353 (typically 9pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \bullet C_{IN} = R_F \bullet C_F$$

where $C_{IN}$ is equal to the OPA353's input capacitance (sum of differential and common-mode) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

## DRIVING A/D CONVERTERS

OPA353 series op amps are optimized for driving medium speed (up to 500kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA353 series provides an effective means of buffering the A/D's input capacitance and resulting charge injection while providing signal gain. For applications requiring high accuracy, the OPA350 series is recommended.

Figure 5 shows the OPA353 driving an ADS7861. The ADS7861 is a dual, 12-bit, 500kHz sampling converter in the small SSOP-24 package. When used with the miniature package options of the OPA353 series, the combination is ideal for space-limited and low power applications. For further information consult the ADS7861 data sheet.

## OUTPUT IMPEDANCE

The low frequency open-loop output impedance of the OPA353's common-source output stage is approximately 1kΩ. When the op amp is connected with feedback, this value is reduced significantly by the loop gain of the op amp. For example, with 122dB of open-loop gain, the output impedance is reduced in unity-gain to less than 0.001Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount which results in a ten-fold increase in output impedance (see the typical performance curve, "Output Impedance vs Frequency").

At higher frequencies, the output impedance will rise as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive due to parasitic capacitance. This prevents the output impedance from becoming too high, which can cause stability problems when driving capacitive loads. As mentioned previously, the OPA353 has excellent capacitive load drive capability for an op amp with its bandwidth.

## VIDEO LINE DRIVER

Figure 6 shows a circuit for a single supply, G = 2 composite video line driver. The synchronized outputs of a composite video line driver extend below ground. As shown, the input to the op amp should be ac-coupled and shifted positively to provide adequate signal swing to account for these negative signals in a single-supply configuration.

The input is terminated with a 75Ω resistor and ac-coupled with a 47µF capacitor to a voltage divider that provides the dc bias point to the input. In Figure 6, this point is approximately (V–) + 1.7V. Setting the optimal bias point requires some understanding of the nature of composite video signals. For best performance, one should be careful to avoid the distortion caused by the transition region of the OPA353's complementary input stage. Refer to the discussion of rail-to-rail input.

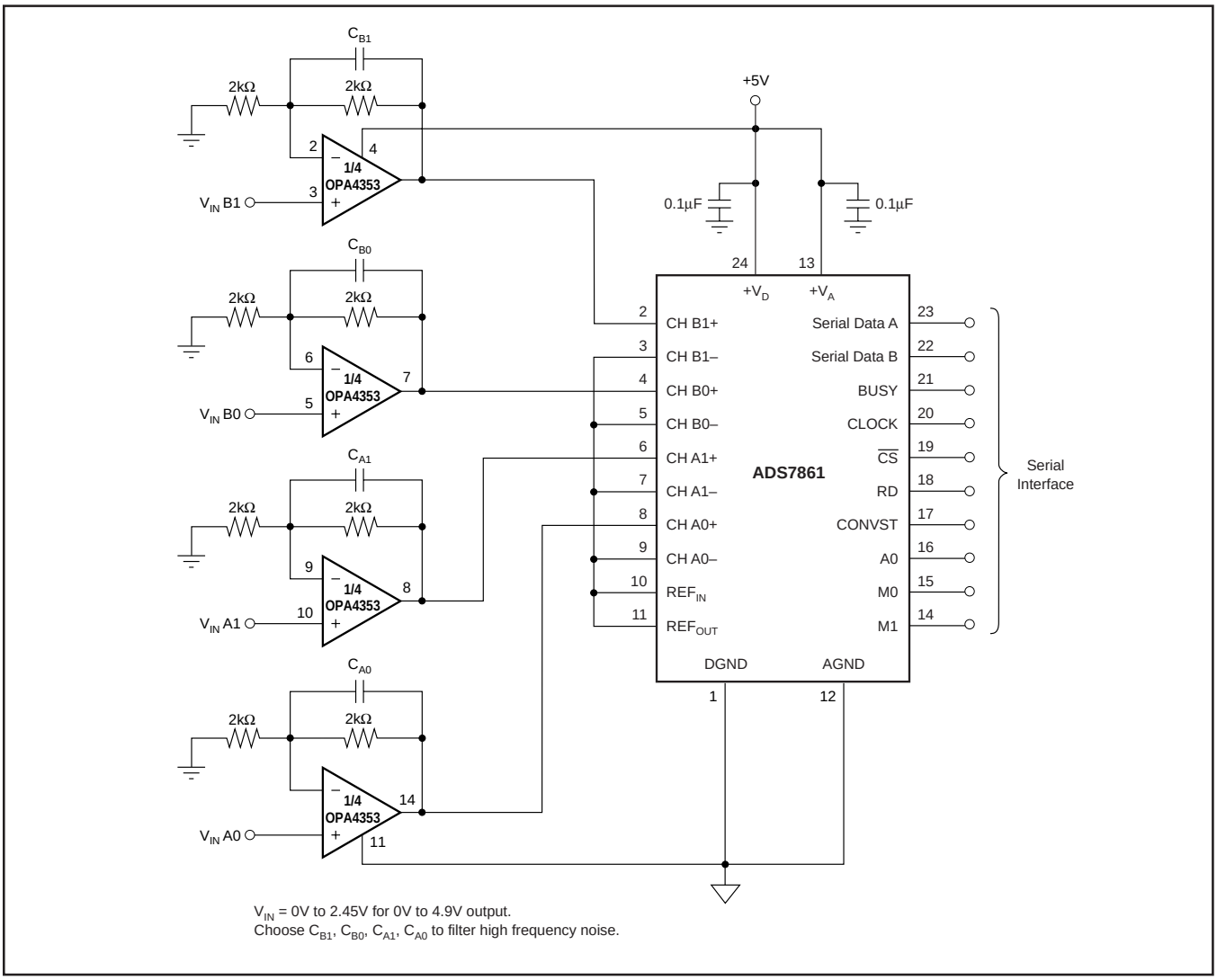



FIGURE 5. OPA4353 Driving Sampling A/D Converter.

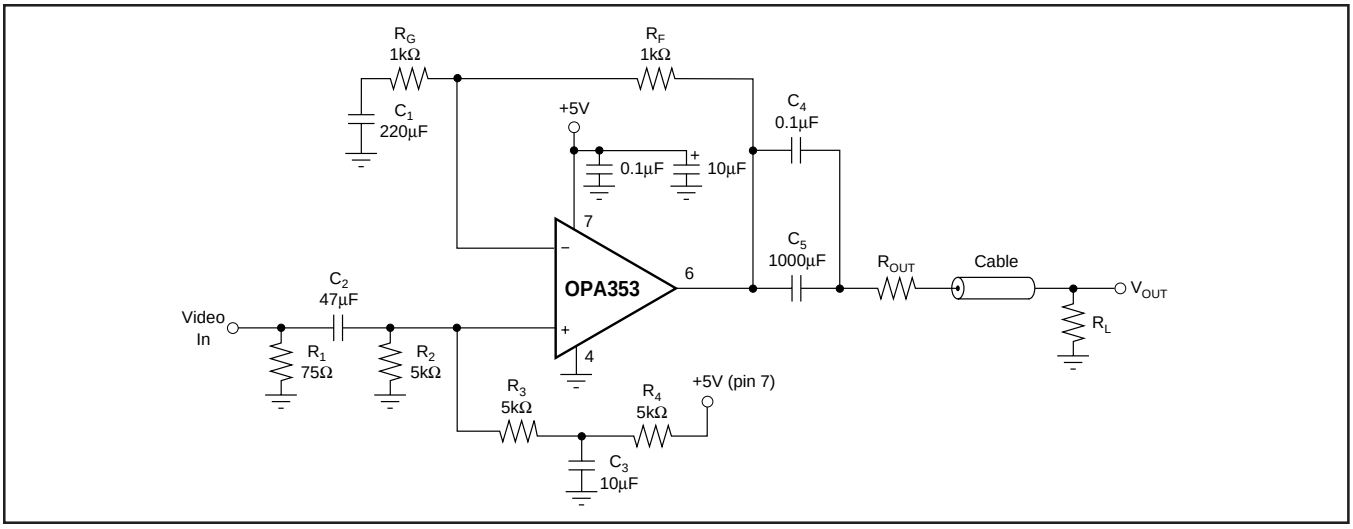



FIGURE 6. Single-Supply Video Line Driver.

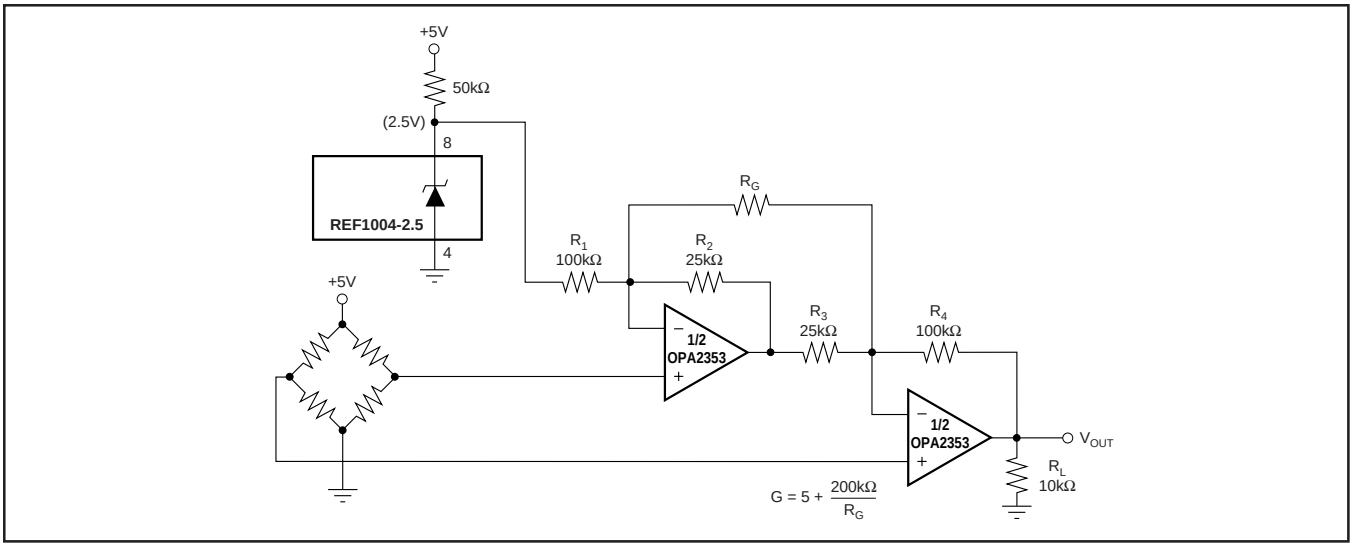



FIGURE 7. Two Op-Amp Instrumentation Amplifier With Improved High Frequency Common-Mode Rejection.

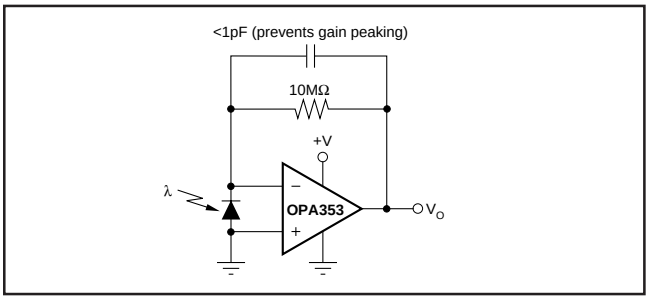



FIGURE 8. Transimpedance Amplifier.

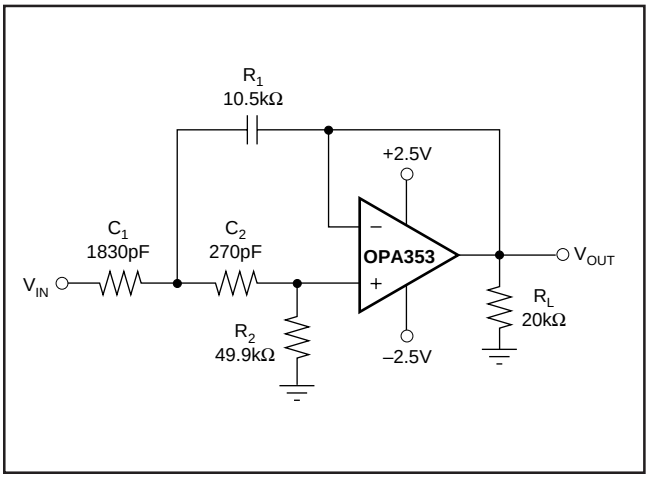



FIGURE 10. 10kHz High-Pass Filter.

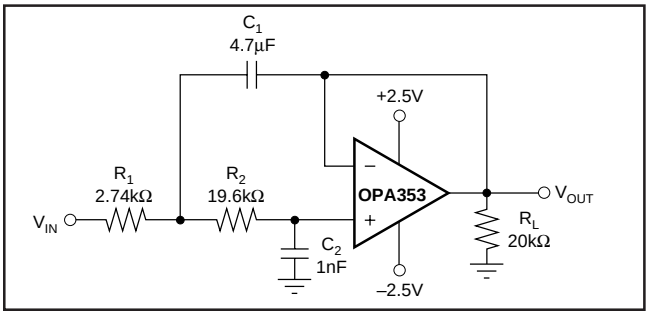



FIGURE 9. 10kHz Low-Pass Filter.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA2353EA/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | Call TI \| Nipdauag \| Nipdau | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353EA/250.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353EA/250G4 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353EA/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI \| Nipdauag \| Nipdau | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353EA/2K5.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353EA/2K5G4 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | E53 |
| OPA2353UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UA.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UA/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UA/2K5.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UA/2K5G4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UA/2K5G4.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA2353UAG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2353UA |
| OPA353NA/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353NA/250.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353NA/250G4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353NA/250G4.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353NA/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353NA/3K.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | D53 |
| OPA353UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 353UA |
| OPA353UA.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 353UA |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA353UA/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 353UA |
| OPA353UA/2K5.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 353UA |
| OPA353UAG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 353UA |
| OPA4353EA/250 | Active | Production | SSOP (DBQ) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 4353EA |
| OPA4353EA/250.B | Active | Production | SSOP (DBQ) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 4353EA |
| OPA4353UA | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | OPA4353UA |
| OPA4353UA.B | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4353UA |
| OPA4353UA/2K5 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4353UA |
| OPA4353UA/2K5.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4353UA |
| OPA4353UA/2K51G4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4353UA |
| OPA4353UA/2K51G4.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4353UA |
| OPA4353UAG4 | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | See OPA4353UA | OPA4353UA |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

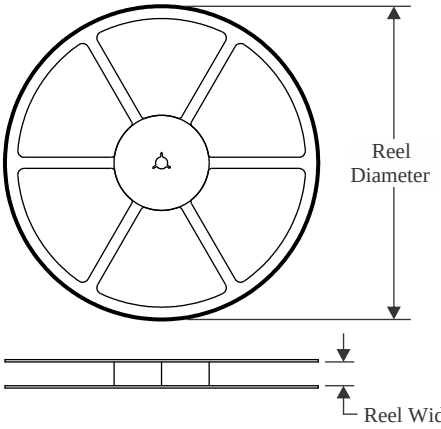
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

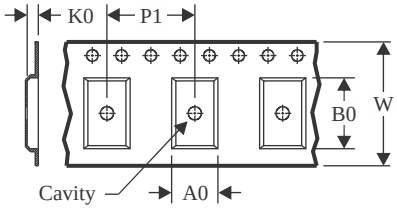
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

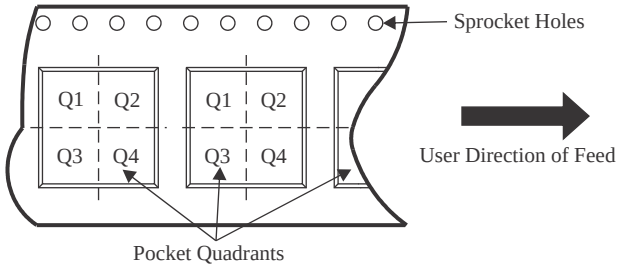



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

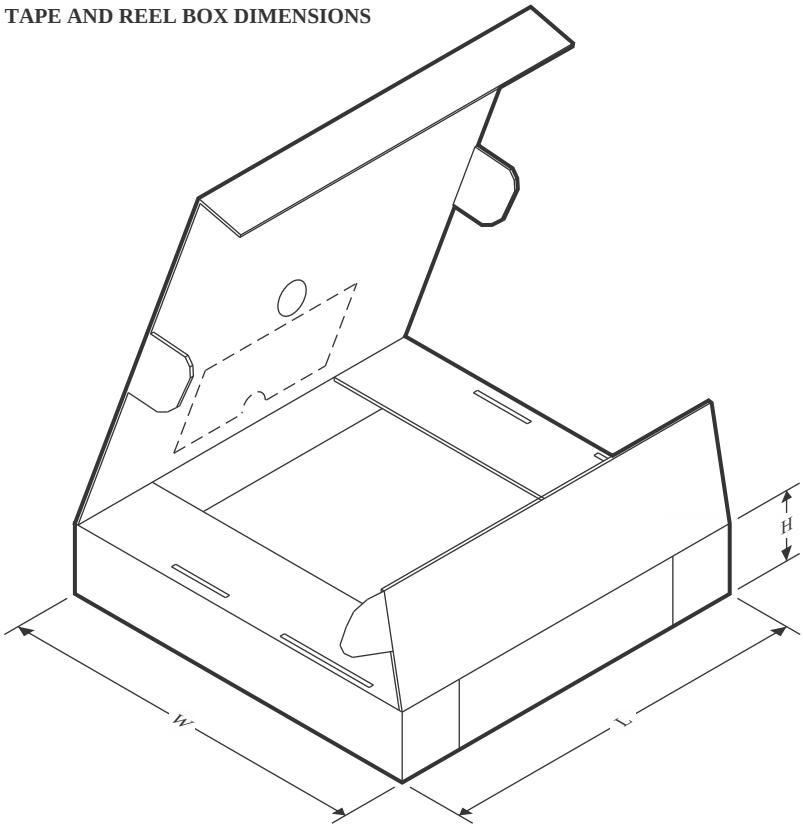
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2353EA/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2353EA/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2353UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2353UA/2K5G4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA353NA/250 | SOT-23 | DBV | 5 | 250 | 178.0 | 8.4 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA353NA/250G4 | SOT-23 | DBV | 5 | 250 | 178.0 | 8.4 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA353NA/3K | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA353UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4353EA/250 | SSOP | DBQ | 16 | 250 | 180.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4353UA/2K5 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4353UA/2K51G4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

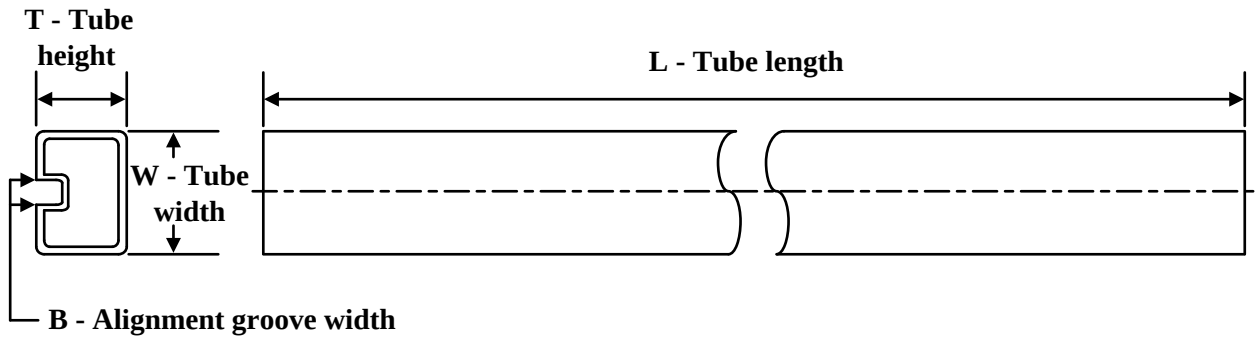
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2353EA/250 | VSSOP | DGK | 8 | 250 | 213.0 | 191.0 | 35.0 |
| OPA2353EA/2K5 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA2353UA/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA2353UA/2K5G4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA353NA/250 | SOT-23 | DBV | 5 | 250 | 445.0 | 220.0 | 345.0 |
| OPA353NA/250G4 | SOT-23 | DBV | 5 | 250 | 445.0 | 220.0 | 345.0 |
| OPA353NA/3K | SOT-23 | DBV | 5 | 3000 | 445.0 | 220.0 | 345.0 |
| OPA353UA/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA4353EA/250 | SSOP | DBQ | 16 | 250 | 213.0 | 191.0 | 35.0 |
| OPA4353UA/2K5 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA4353UA/2K51G4 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

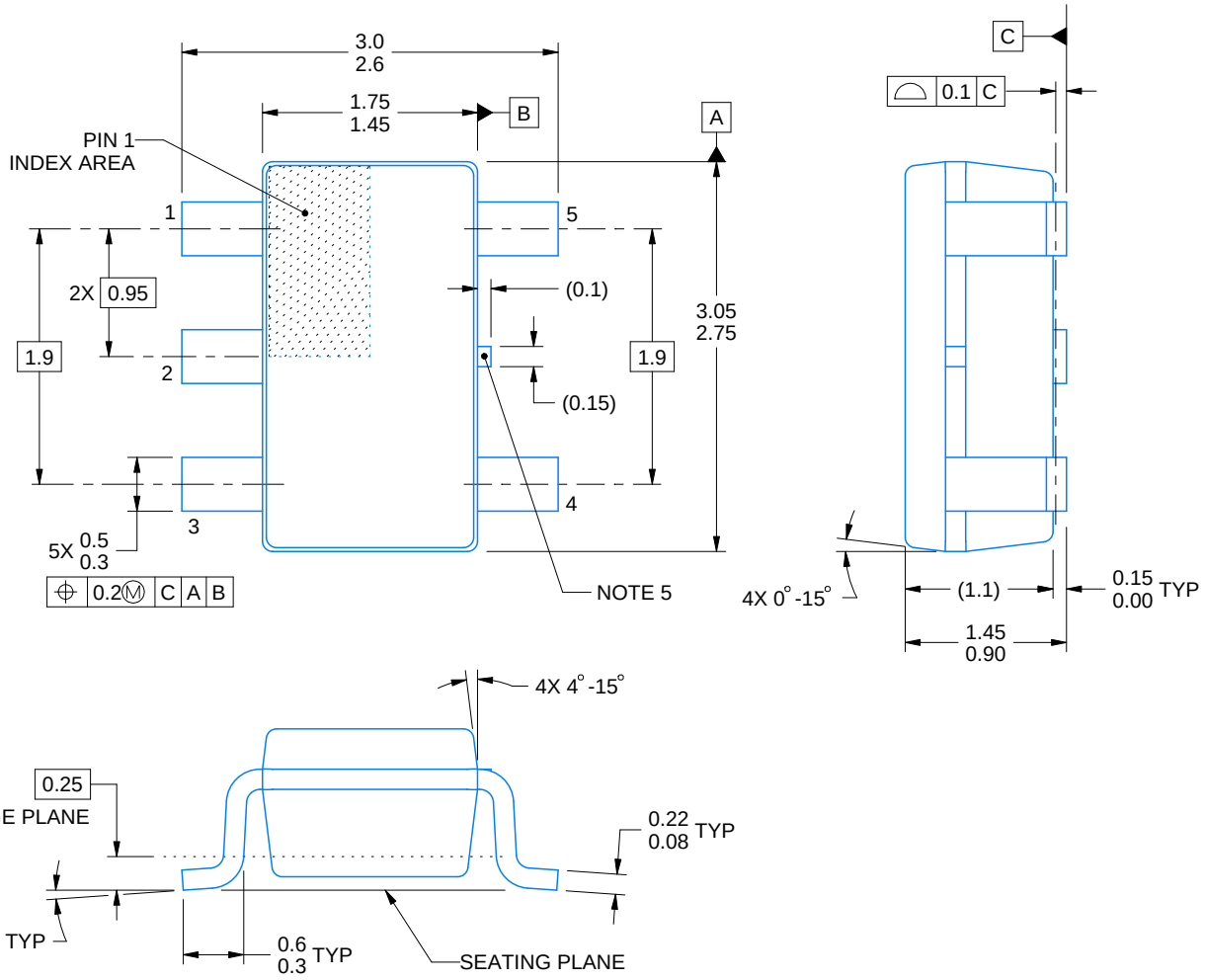
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA2353UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA2353UA.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA2353UAG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA353UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA353UA.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA353UAG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA4353UA | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA4353UA.B | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA4353UAG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

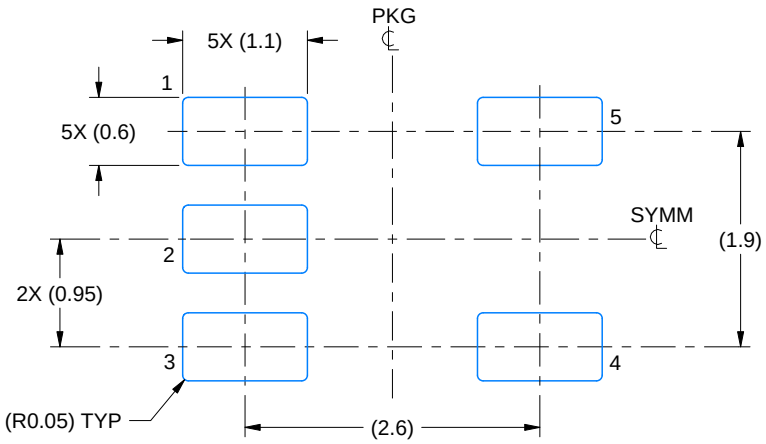
SMALL OUTLINE TRANSISTOR



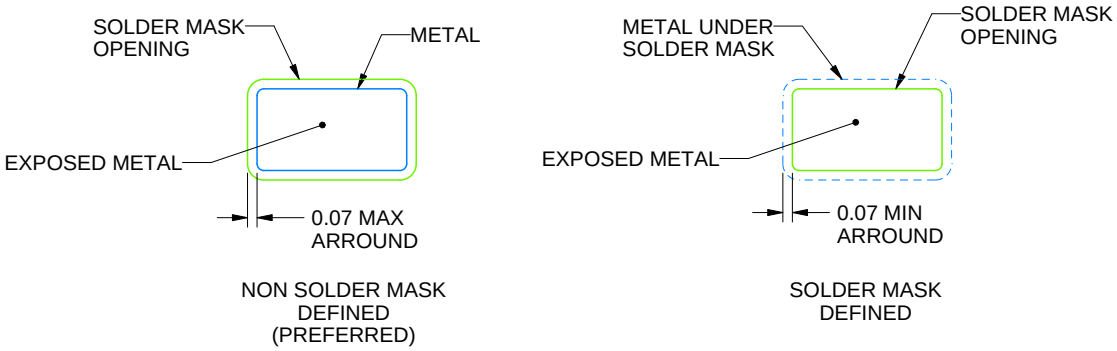

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

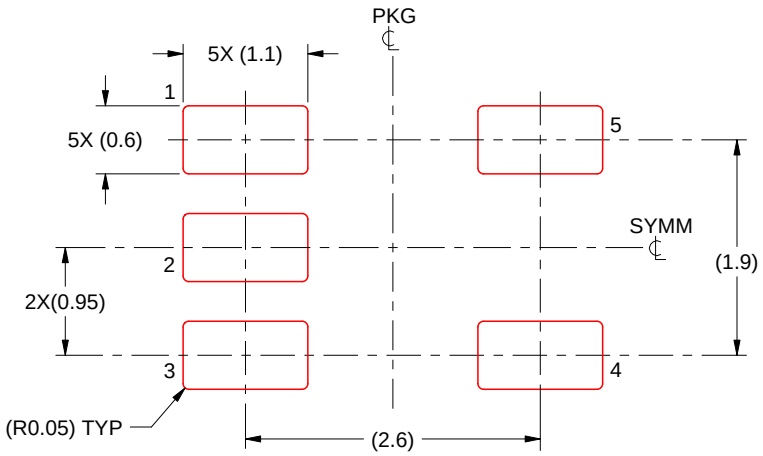



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

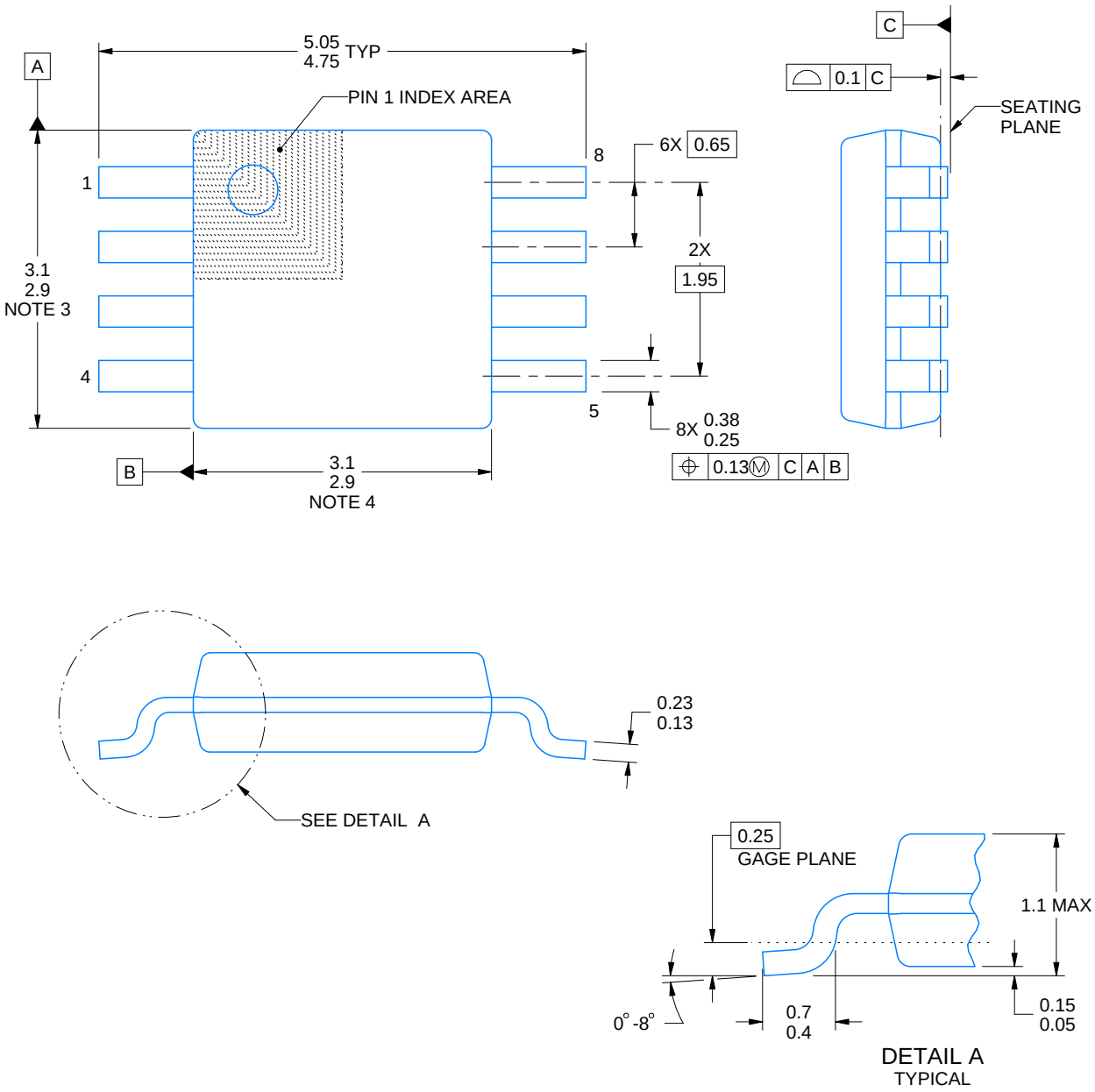
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

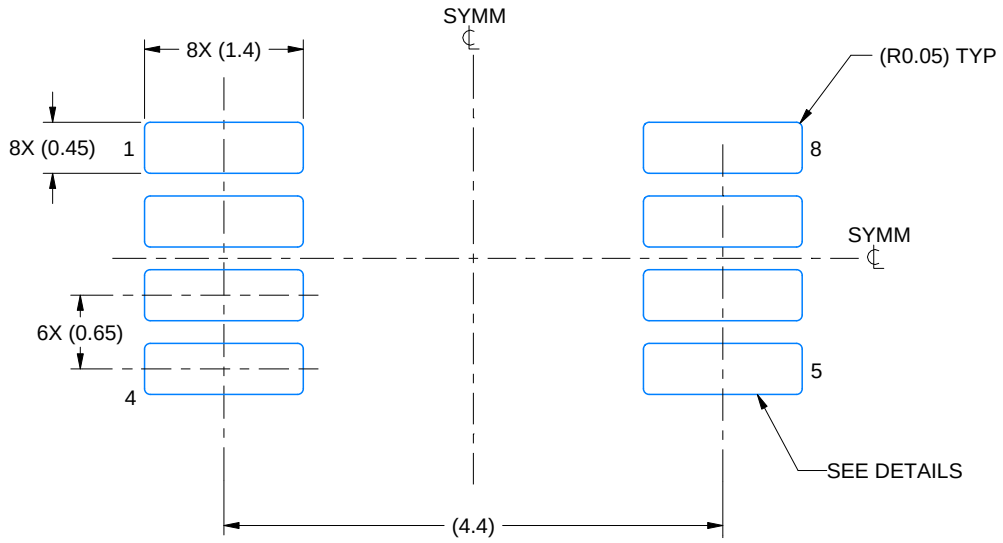
SMALL OUTLINE PACKAGE



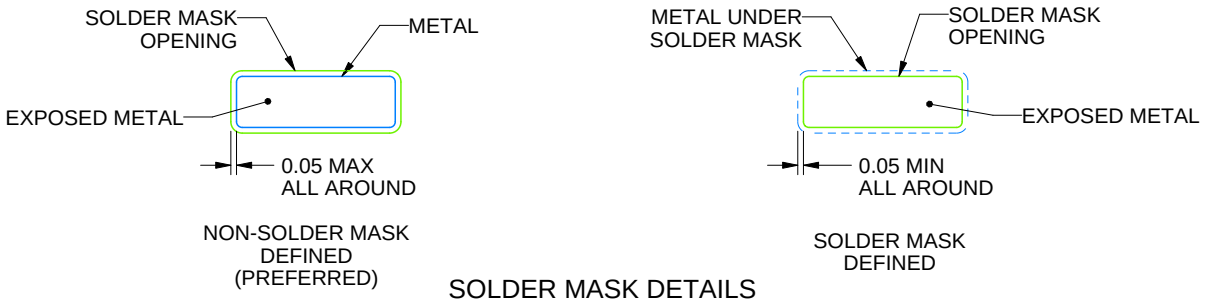

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

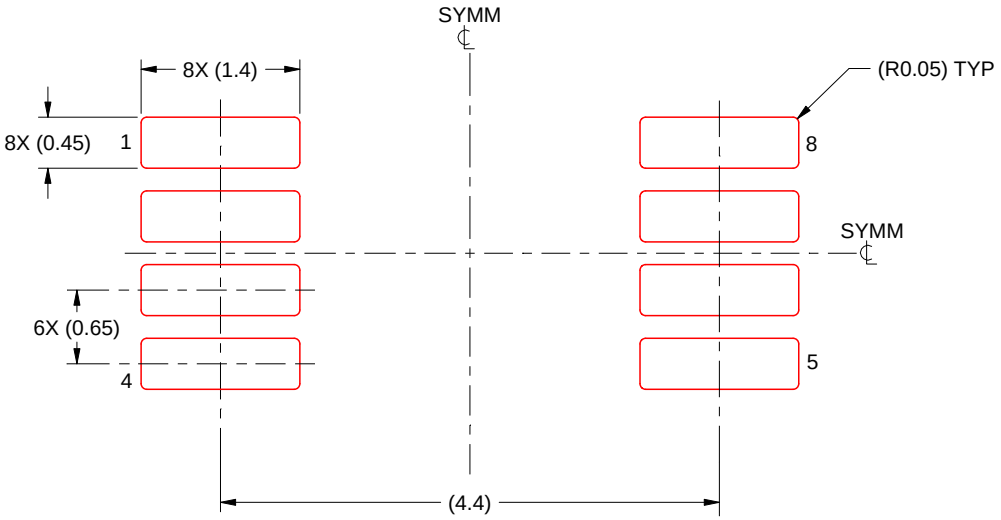



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

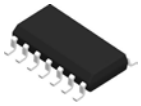



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

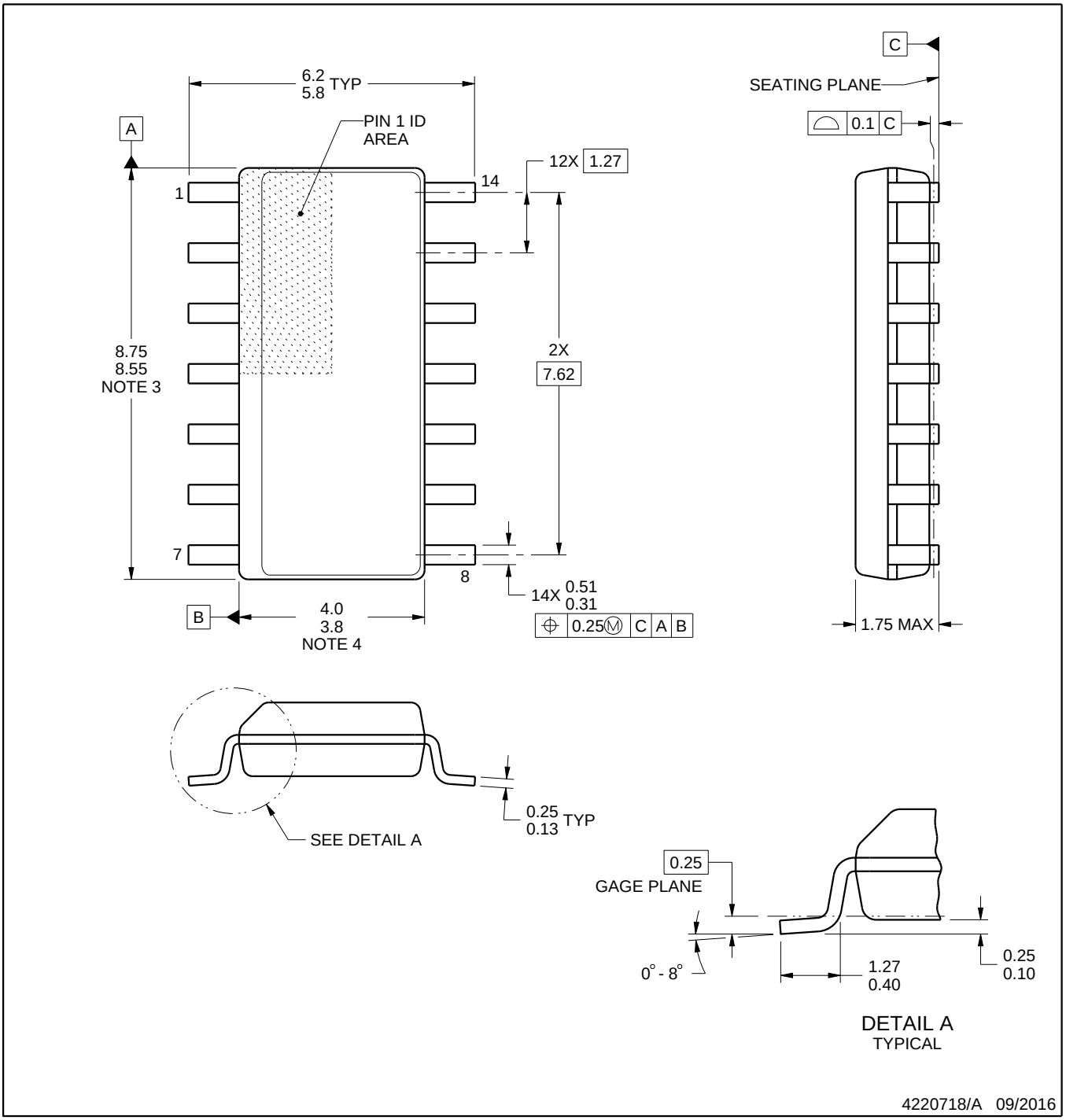


# PACKAGE OUTLINE

## D0014A

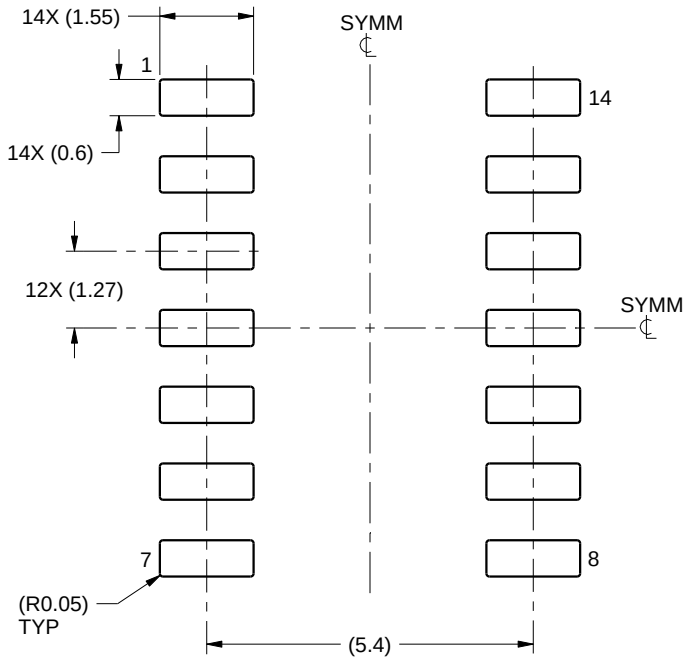
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

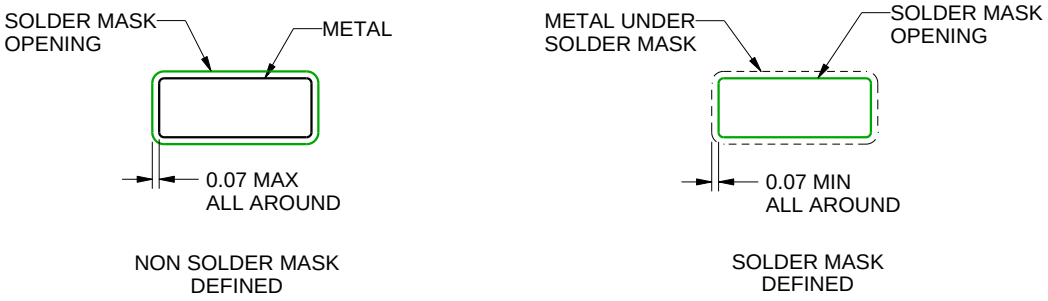



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

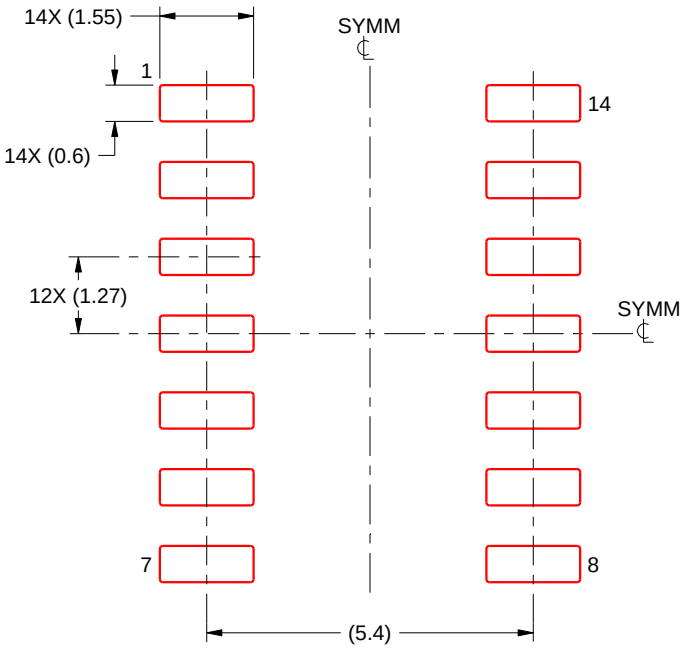
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

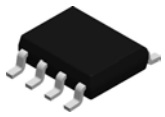



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

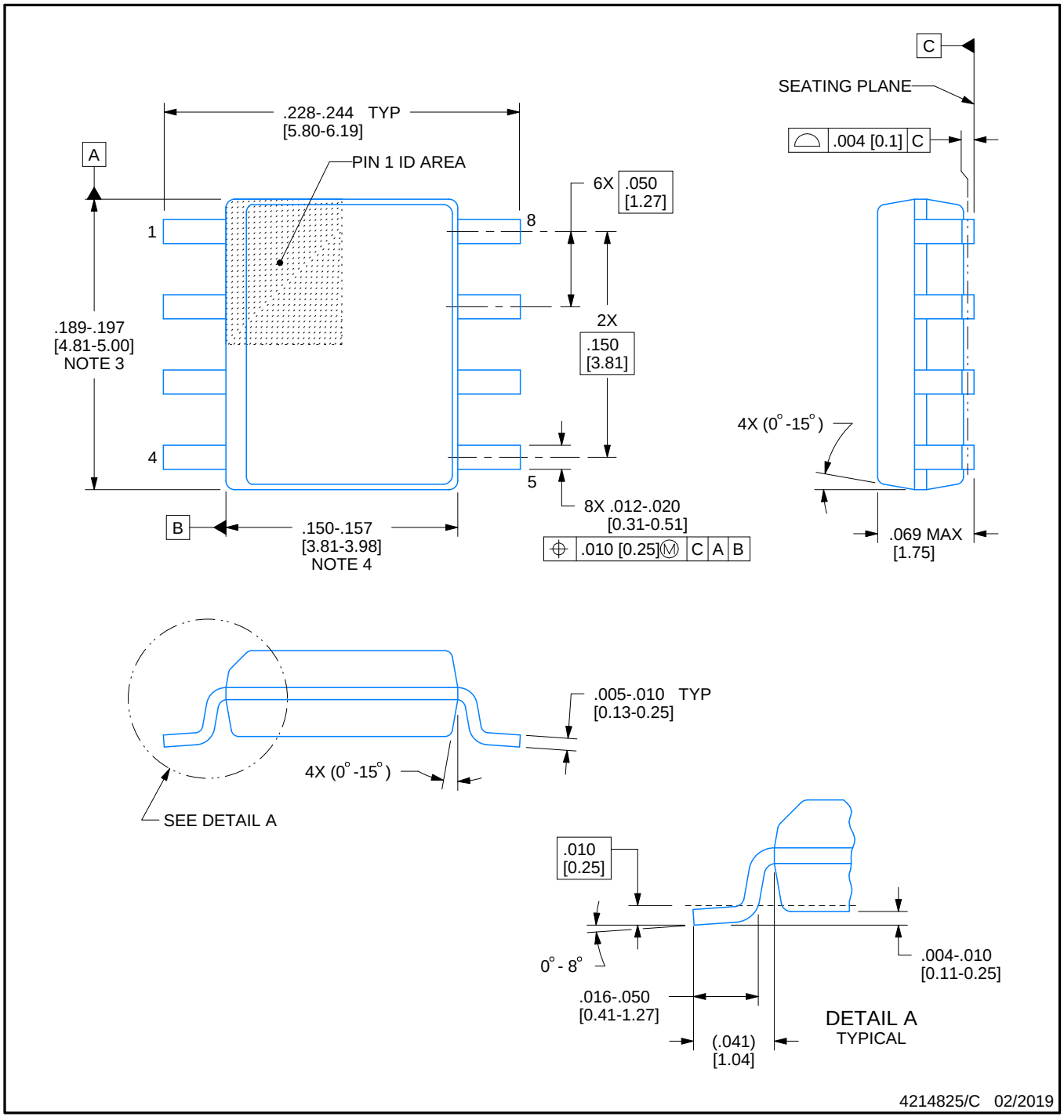


# PACKAGE OUTLINE

## D0008A

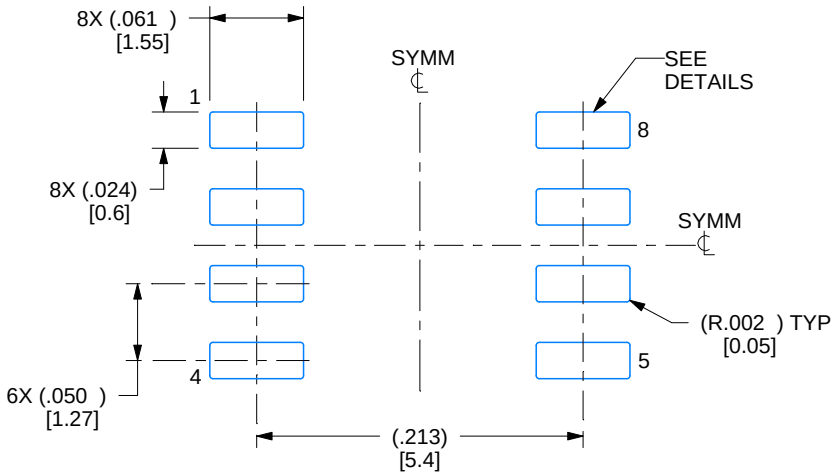
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

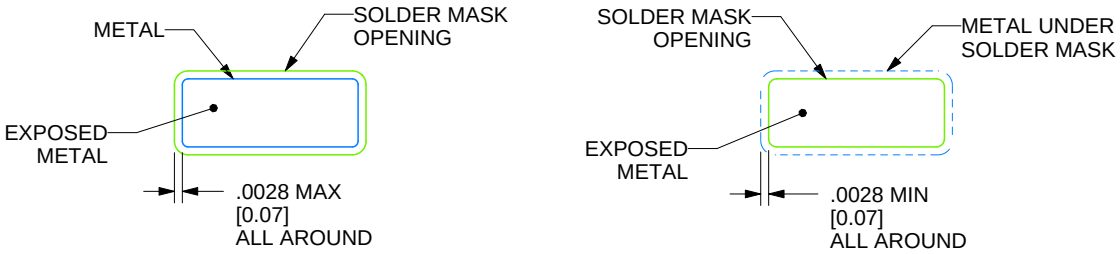



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

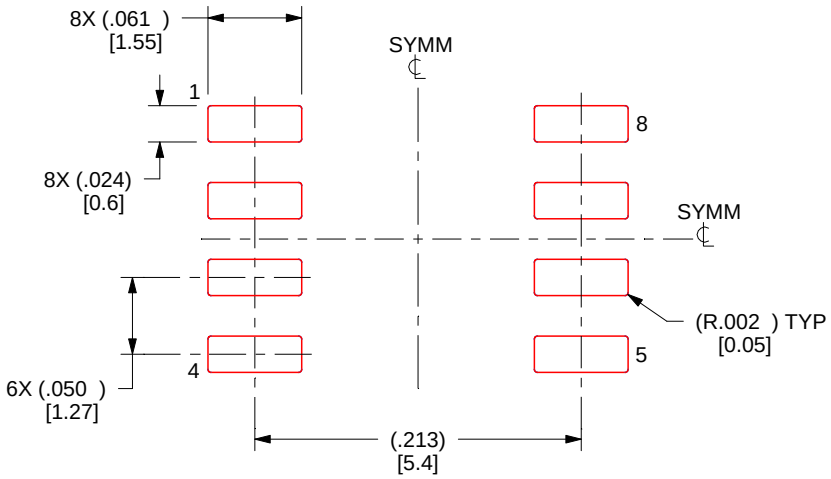
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

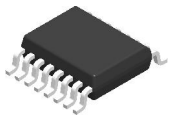



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

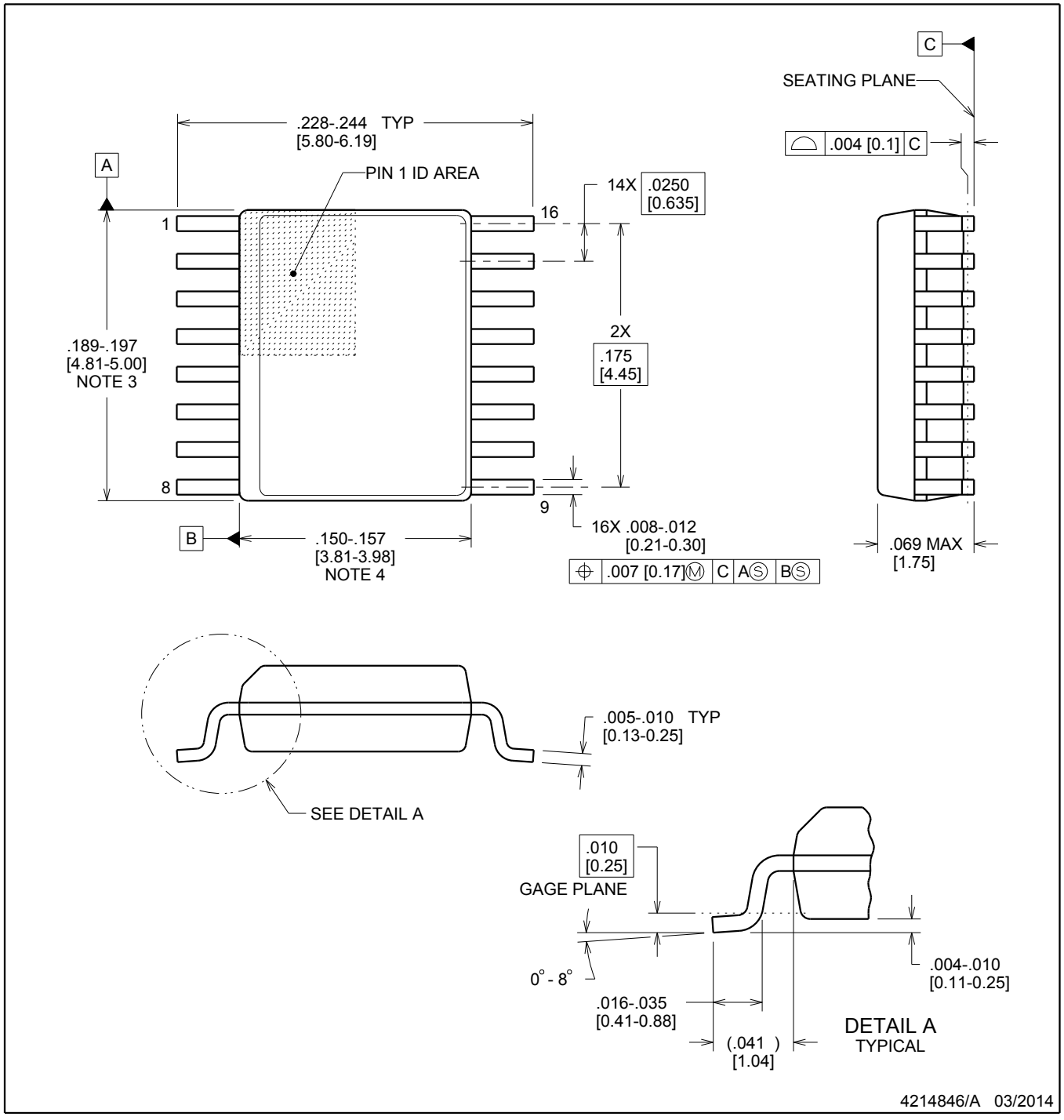


# PACKAGE OUTLINE

## DBQ0016A

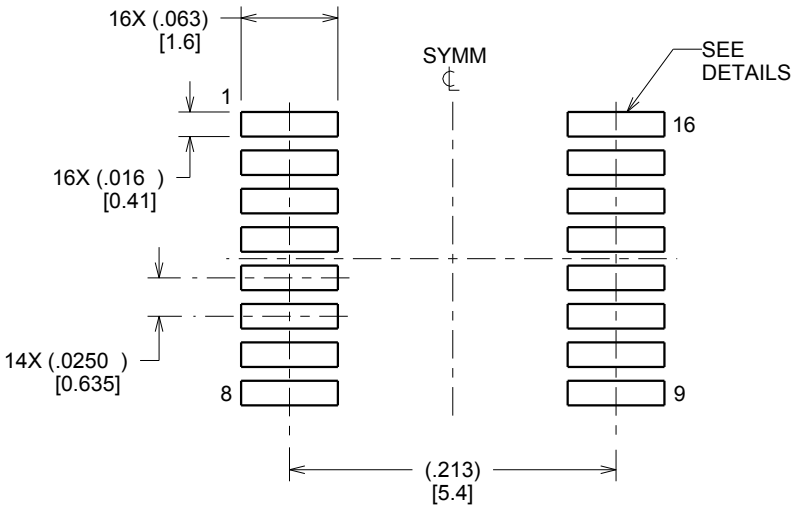
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

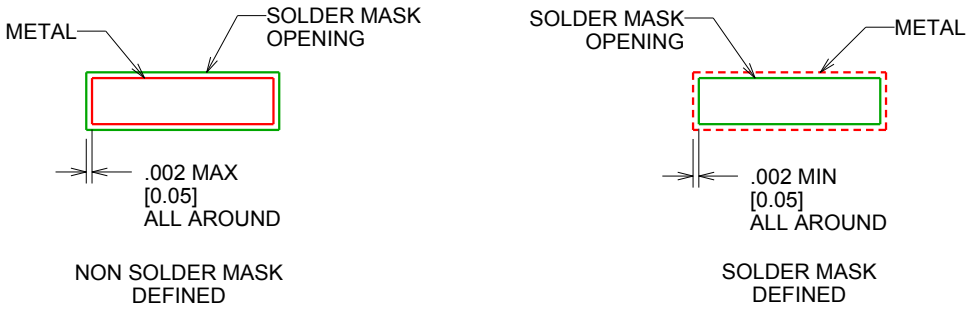



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

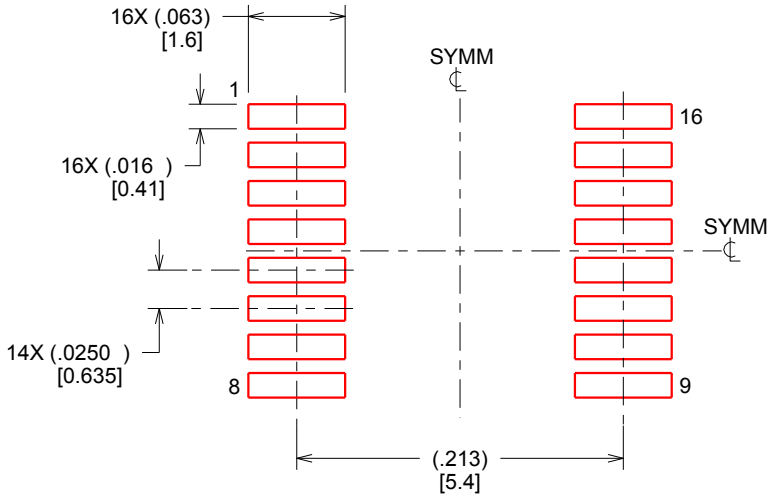
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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