HIGH PRECISION, LOW NOISE OPERATIONAL AMPLIFIER

Check for Samples: OPA2227-EP

FEATURES

- **Low Noise: 3 nV/√Hz**
- **Wide Bandwidth: 8 MHz, 2.3 V/µs**
- **Settling Time: 5 µs**
- **High CMRR: 138 dB (Typical)**
- **High Open-Loop Gain: 160 dB (Typical)**
- **Low Input Bias Current: 10 nA Maximum at 25°C**
- **Low Offset Voltage: 100 µV Maximum at 25°C**
- **Wide Supply Range: ±2.5 V to ±18 V**

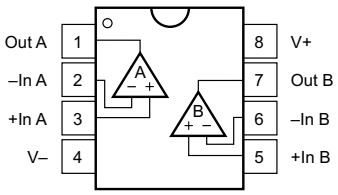
APPLICATIONS

- **Data Acquisition**
- **Telecom Equipment**
- **Geophysical Analysis**
- **Vibration Analysis**
- **Spectral Analysis**
- **Professional Audio Equipment**
- **Active Filters**
- **Power Supply Control**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)



(1) Additional temperature ranges available - contact factory

DESCRIPTION

The OPA2227 operational amplifier combines low noise and wide bandwidth with high precision to make it the ideal choice for applications requiring both ac and precision dc performance.

The OPA2227 is unity-gain stable and features high slew rate (2.3 V/µs) and wide bandwidth (8 MHz).

The OPA2227 operational amplifier is ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPA2227 operational amplifier is a pin-for-pin replacement for the industry standard OP-27 with substantial improvements across the board. The dual and quad versions are available for space savings and perchannel cost reduction.

The OPA2227 is available in an SOIC-8 package. Operation is specified from –55°C to 125°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	TOP-SIDE MARKING	ORDERABLE PART NUMBER	VID NUMBER	TRANSPORT MEDIA
–55°C to 125°C	SOIC-8 – D	2227EP	OPA2227MDREP	V62/12610-01XE	Tape and Reel, large
			OPA2227MDEP	V62/12610-01XE-T	Tube

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage		±18	V
Signal input terminals	Voltage	(V–) – 0.7 to (V+) + 0.7	V
	Current	20	mA
Output short-circuit (to ground)(2)		Continuous	
Operating temperature		-55 to 125	°C
Storage temperature		-65 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) One channel per package.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA2227 D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	91.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	39.9	
θ_{JB}	Junction-to-board thermal resistance(4)	40.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	3.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	39.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

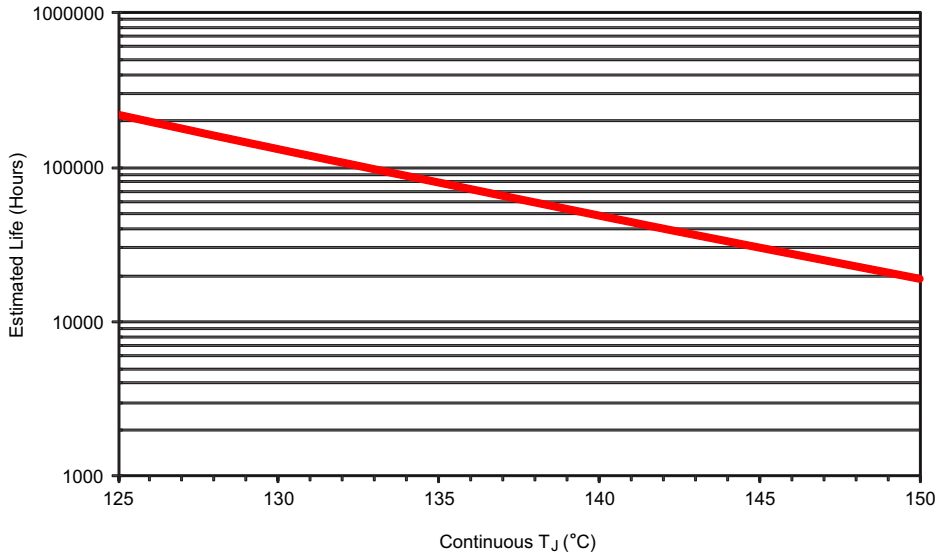
At T_A = 25°C, V_S = ±5 V to ±15 V, R_L = 10 kΩ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage (V_{OS})				±5	±100	µV
vs Temperature, T_A = -55°C to 125°C				±10	±250	µV
vs Temperature (dV_{OS}/dT), T_A = -55°C to 125°C				±0.1		µV/°C
vs Power supply (PSRR) T_A = -55°C to 125°C		V_S = ±2.5 V to ±18 V		±0.5	±2.1	µV/V
vs Time				0.2		µV/mo
Channel separation (dual)		dc		0.2		µV/V
		f = 1 kHz, R_L = 5 kΩ		110		dB
INPUT BIAS CURRENT						
Input bias current (I_B)				±2.5	±10	nA
T_A = -55°C to 125°C			See Typical Characteristics			
Input offset current (I_{OS})				±2.5	±10	nA
T_A = -55°C to 125°C			See Typical Characteristics			
NOISE						
Input voltage noise, f = 0.1 Hz to 10 Hz				90		nVp-p
				15		nVrms
Input voltage noise density (e_n)	f = 10 Hz			3.5		nV/√Hz
	f = 100 Hz			3		nV/√Hz
	f = 1 kHz			3		nV/√Hz
Current noise density (i_n), f = 1 kHz				0.4		pA/√Hz
INPUT VOLTAGE RANGE						
Common-mode voltage range (V_{CM}) T_A = -55°C to 125°C			(V-) + 2		(V+) – 2	V
Common-mode rejection (CMRR)		V_{CM} = (V–) + 2 V to (V+) – 2 V	120	138		dB
T_A = -55°C to 125°C			108	138		dB
INPUT IMPEDANCE						
Differential		Open-loop voltage gain (A_{OL})		10^7 || 12		Ω || pF
Common-mode		V_{CM} = (V–) + 2 V to (V+) – 2 V		10^9 || 3		Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain (A_{OL})		V_O = (V–) + 2 V to (V+) – 2 V, R_L = 10 kΩ	132	160		dB
T_A = -55°C to 125°C			112	160		
		V_O = (V–) + 3.5 V to (V+) – 3.5 V, R_L = 600 Ω	132	160		
T_A = -55°C to 125°C			112	160		
FREQUENCY RESPONSE						
Gain bandwidth product (GBW)				8		MHz
Slew rate (SR)				2.3		V/µs
Settling time:	0.1%	G = 1, 10-V Step, C_L = 100 pF		5		µs
	0.01%	G = 1, 10-V Step, C_L = 100 pF		5.6		µs
Overload recovery time		V_{IN} x G = V_S		1.3		µs
Total harmonic distortion + noise (THD+N)		f = 1 kHz, G = 1, V_O = 3.5 Vrms		0.00005		%
OUTPUT						
Voltage output						
T_A = -55°C to 125°C		R_L = 10 kΩ	(V-) + 2		(V+) – 2	V
T_A = -55°C to 125°C		R_L = 600 Ω	(V-) + 3.5		(V+) – 3.5	
Short-circuit current (I_{SC})				±45		mA
Capacitive load drive (C_{LOAD})			See Typical Characteristics			
POWER SUPPLY						
Specified voltage range (V_S)			±5		±15	V
Operating voltage range			±2.5		±18	V
Quiescent current (per amplifier) (I_Q)		I_O = 0 A		±3.7	±3.95	

ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±5 V to ±15 V, R_L = 10 kΩ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = -55°C to 125°C	I_O = 0 A			±4.30	mA
TEMPERATURE RANGE					
Specified temperature range		–55		125	°C
Operating temperature range		–55		125	°C
Storage temperature range		–65		150	°C



A. See datasheet for absolute maximum and minimum recommended operating conditions.

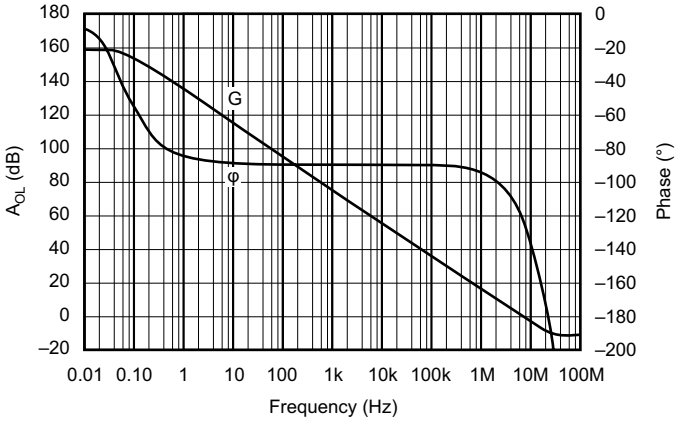
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. OPA2227-EP Wirebond Life Derating Chart

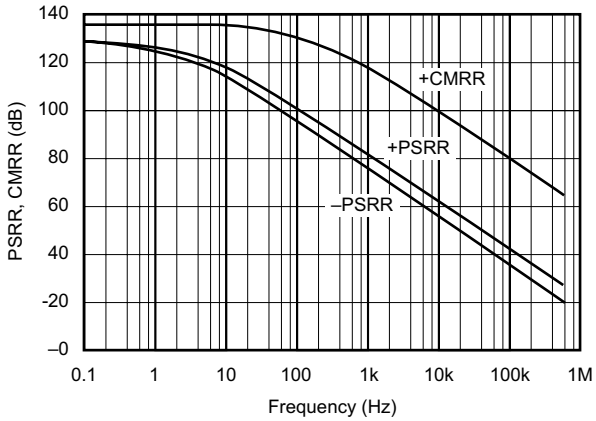
TYPICAL CHARACTERISTICS

At T_A = 25°C, R_L = 10 kΩ, V_S = ±15 V (unless otherwise noted).

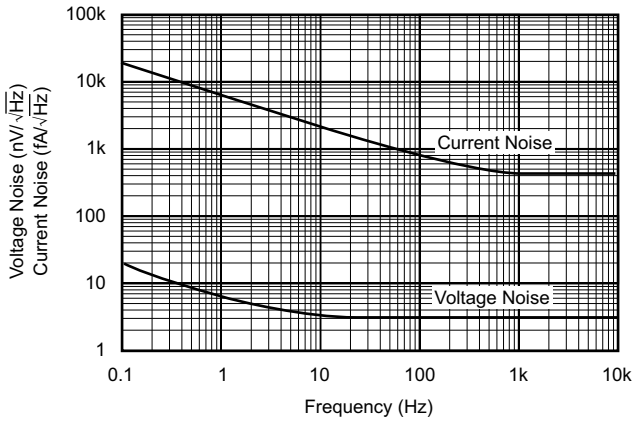
OPEN-LOOP GAIN/PHASE vs FREQUENCY



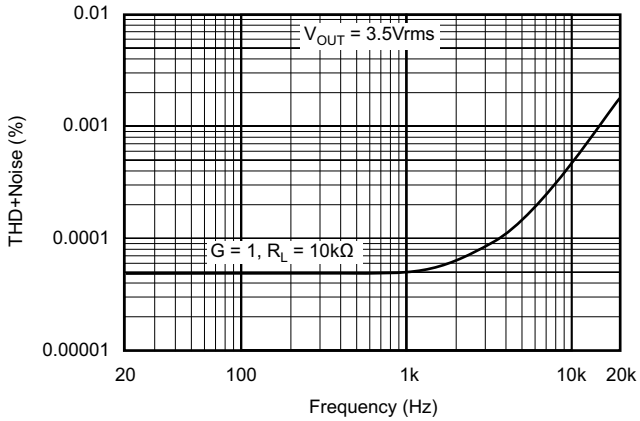
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



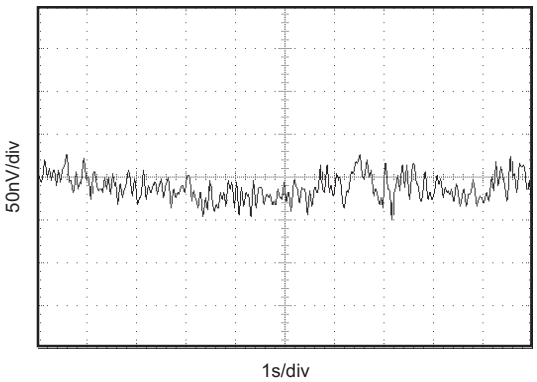
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



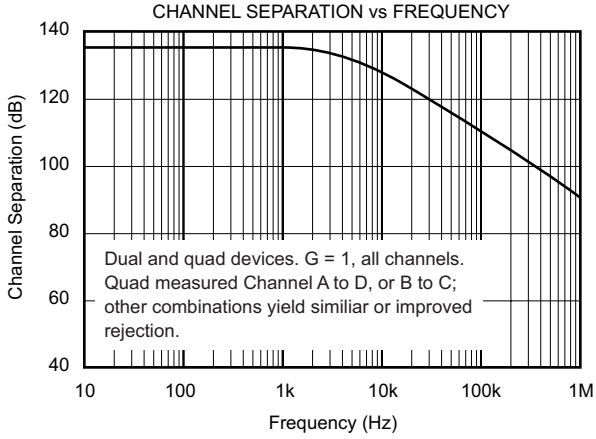
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



INPUT NOISE VOLTAGE vs TIME



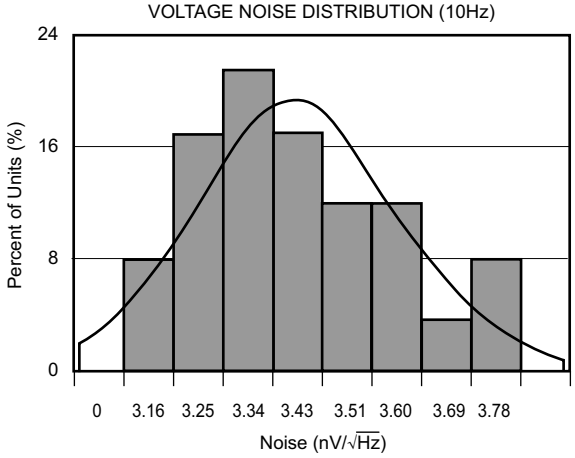
CHANNEL SEPARATION vs FREQUENCY



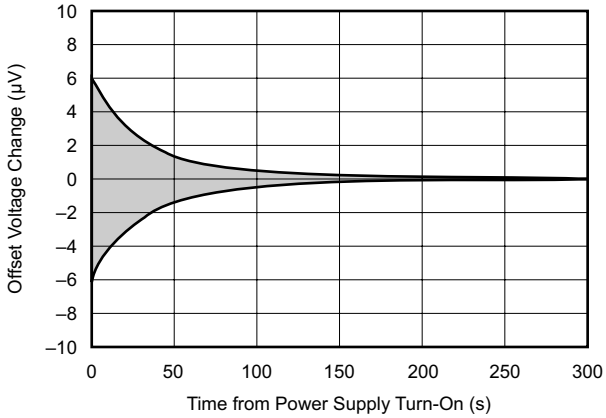
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_L = 10 kΩ, V_S = ±15 V (unless otherwise noted).

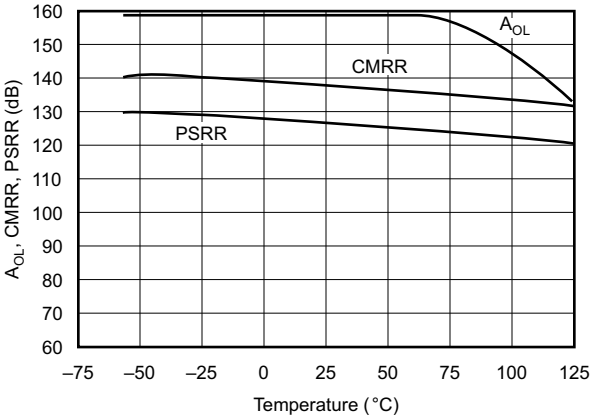
VOLTAGE NOISE DISTRIBUTION (10Hz)



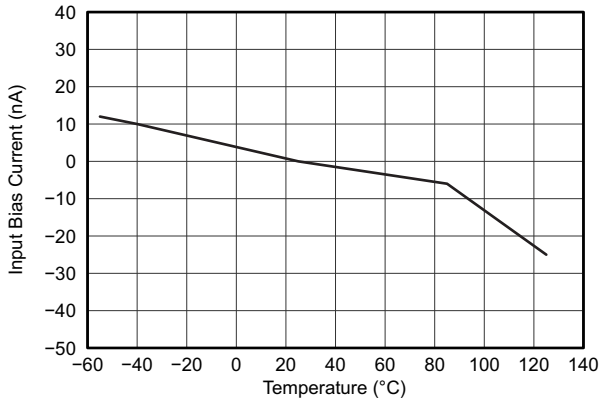
WARM-UP OFFSET VOLTAGE DRIFT



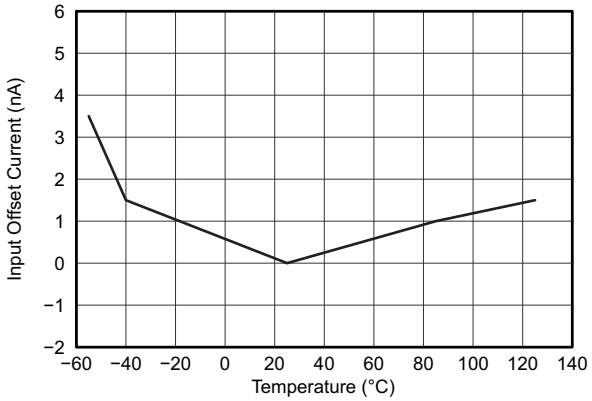
A_{OL}, CMRR, PSRR vs TEMPERATURE



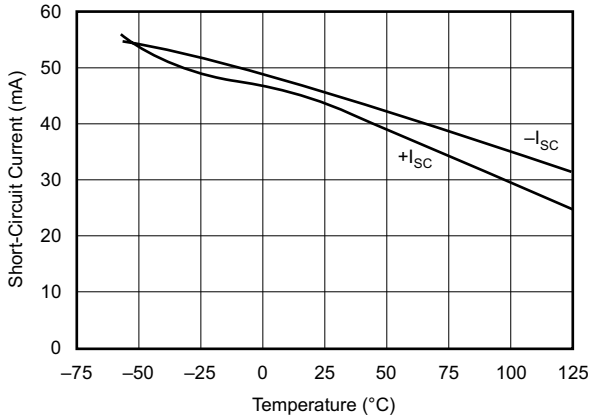
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE



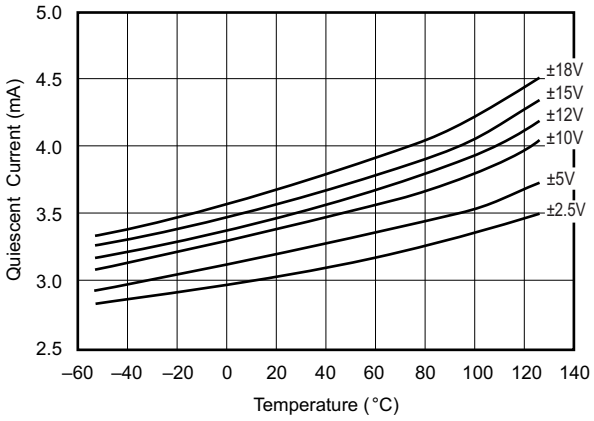
SHORT-CIRCUIT CURRENT vs TEMPERATURE



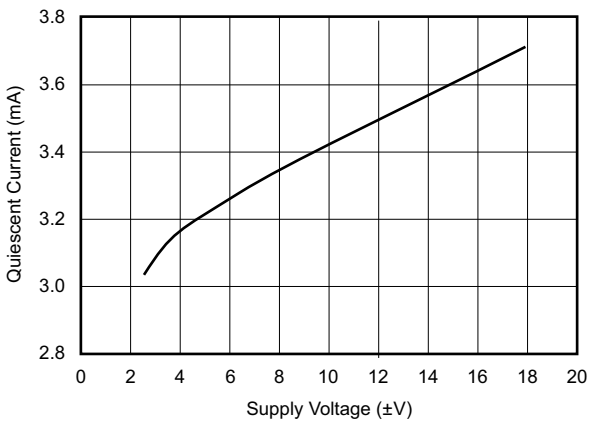
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_L = 10 kΩ, V_S = ±15 V (unless otherwise noted).

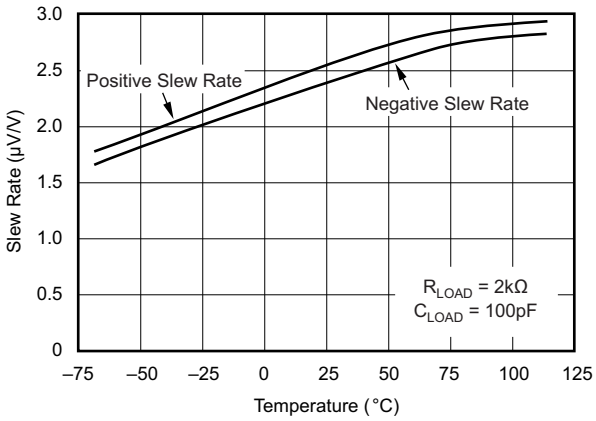
QUIESCENT CURRENT vs TEMPERATURE



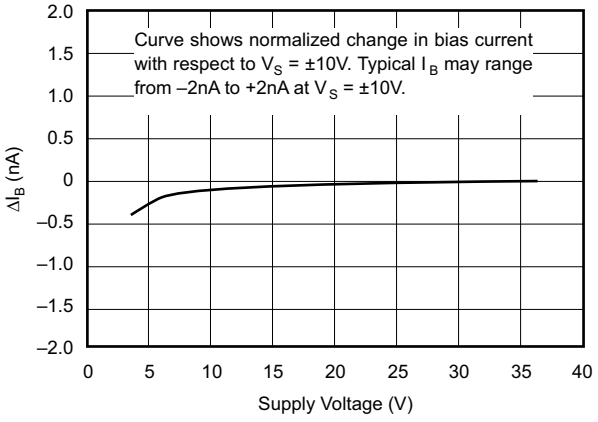
QUIESCENT CURRENT vs SUPPLY VOLTAGE



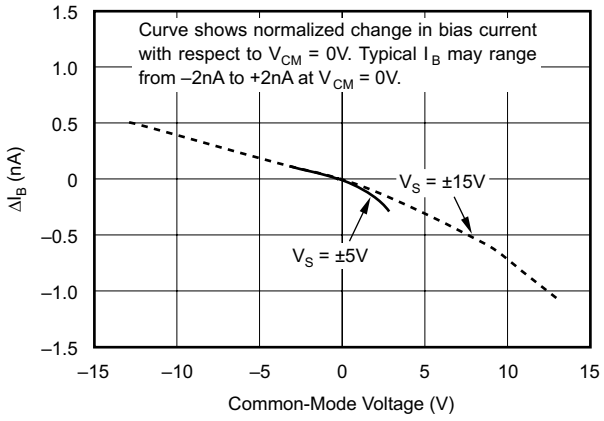
SLEW RATE vs TEMPERATURE



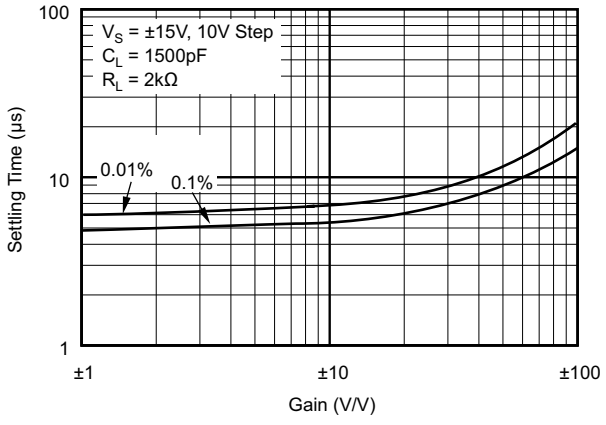
CHANGE IN INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



CHANGE IN INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



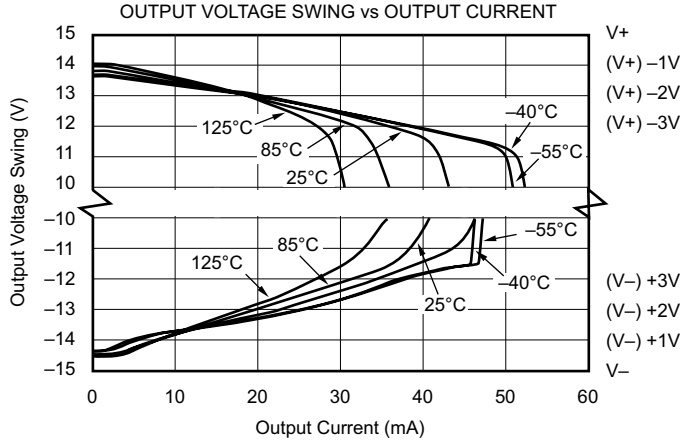
SETTLING TIME vs CLOSED-LOOP GAIN



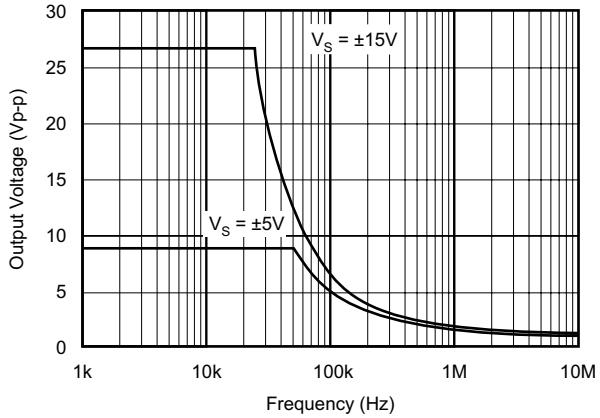
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_L = 10 kΩ, V_S = ±15 V (unless otherwise noted).

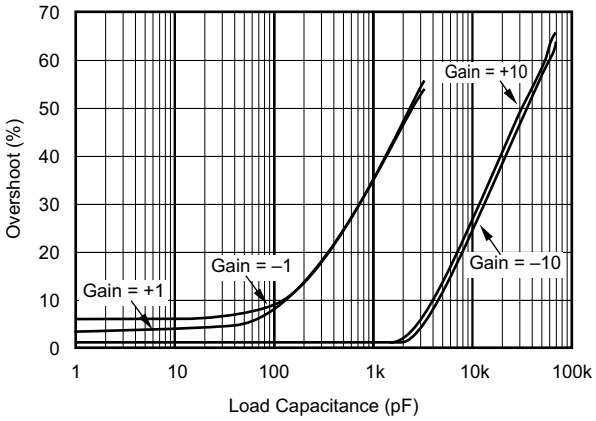
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



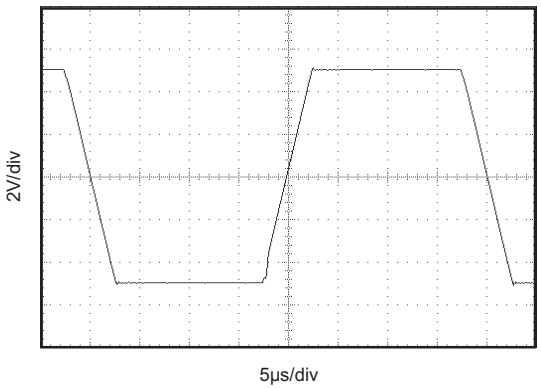
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



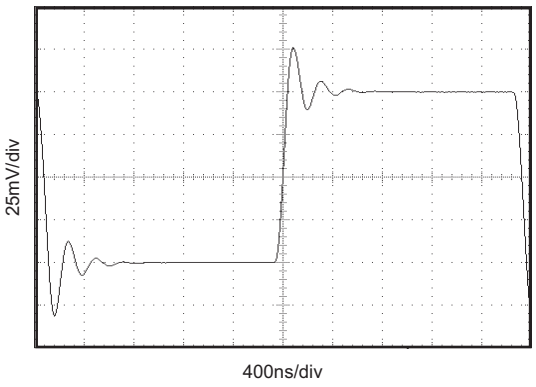
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



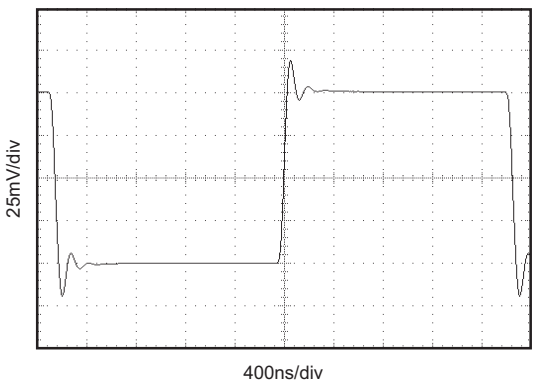
LARGE-SIGNAL STEP RESPONSE
G = –1, C_L = 1500pF



SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 1000pF



SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 5pF



APPLICATION INFORMATION

Basic Connection

The OPA2227 is a precision operational amplifier with very low noise. It is unity-gain stable with a slew rate of 2.3 V/μs and 8-MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

Offset Voltage and Drift

The OPA2227 has very low offset voltage and drift. To achieve highest dc precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the op amp inputs which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as those created by cooling fans.

Operating Voltage

OPA2227 operational amplifier operates from ±2.5-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2227 is specified for real-world applications; a single set of specifications applies over the ±5-V to ±15-V supply range. Specifications are assured for applications between ±5-V and ±15-V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA2227 can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Parameters which vary significantly with operating voltage or temperature are shown in the Typical Performance Curves.

Offset Voltage Adjustment

The OPA2227 is laser-trimmed for very low offset and drift so most applications will not require external adjustment.

Input Protection

Back-to-back diodes (see Figure 2) are used for input protection on the OPA2227. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier's finite slew rate. Without external current-limiting resistors, the input devices can be destroyed. Sources of high input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

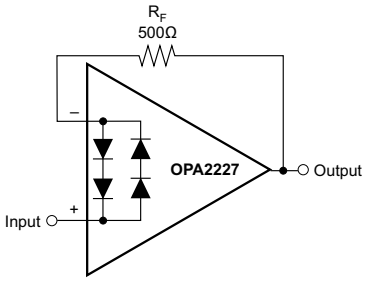


Figure 2. Pulsed Operation

When using the OPA2227 as a unity-gain buffer (follower), the input current should be limited to 20 mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Sufficient resistor size can be calculated:

$$R_X = V_S/20\ mA - R_{SOURCE} \quad (1)$$

where R_X is either in series with the source or inserted in the feedback path. For example, for a 10-V pulse (V_S = 10 V), total loop resistance must be 500 Ω. If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen since they will increase noise. See the Noise Performance section of this data sheet for further information on noise calculation. Figure 2 shows an example implementing a current limiting feedback resistor.

Input Bias Current Cancellation

The input bias current of the OPA2227 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 3) may actually increase offset and noise and is therefore not recommended.

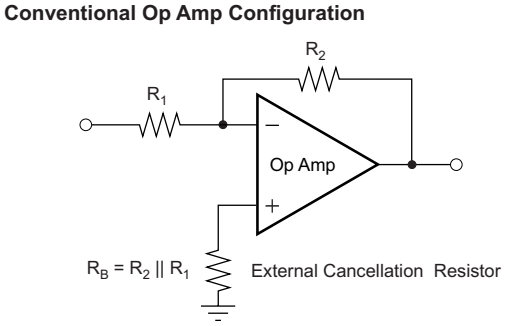


Figure 3. Input Bias Current Cancellation

Noise Performance

Figure 4 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA2227 has very low voltage noise, making it ideal for low source impedances (less than 20 kΩ). A similar precision operational amplifier, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38 x 10^{-23} J/K and T is temperature in K. For more details on calculating noise, see "Basic Noise Calculations."

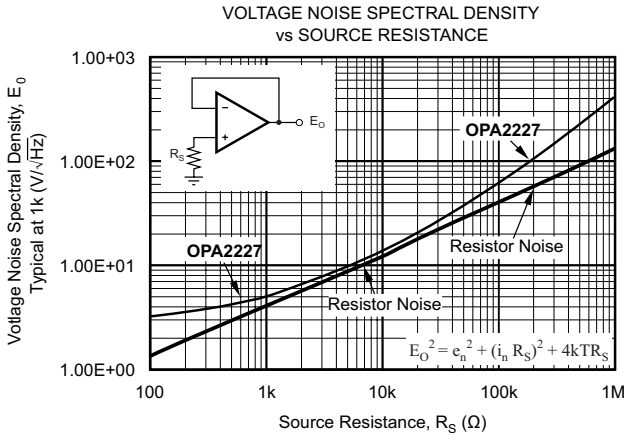


Figure 4. Noise Performance of the OPA2227 in Unity-Gain Buffer Configuration

Basic Noise Calculations

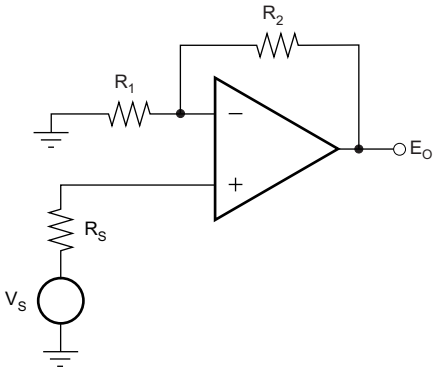
Design of low noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 4. Since the source impedance is usually fixed, select the operational amplifier and the feedback resistors to minimize their contribution to the total noise.

Figure 4 shows total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 5 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Noise in Noninverting Gain Configuration



Noise at the output:

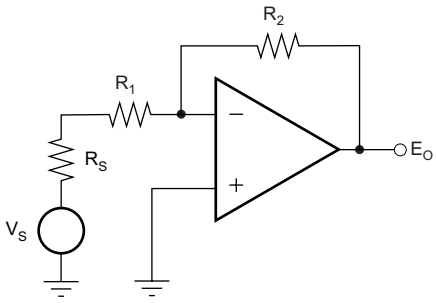
$$E_O^2 = \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1+\frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \cdot \left(1+\frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1+\frac{R_2}{R_1+R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \cdot \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For op amps at 1kHz, e_n = 3nV/$\sqrt{Hz}$ and i_n = 0.4pA/$\sqrt{Hz}$.

Figure 5. Noise Calculation in Gain Configurations

Figure 6 shows the 0.1-Hz to 10-Hz bandpass filter used to test the noise of the OPA2227. The filter circuit was designed using Texas Instruments' FilterPro software (available at www.ti.com). Figure 7 shows the configuration of the OPA2227 for noise testing.

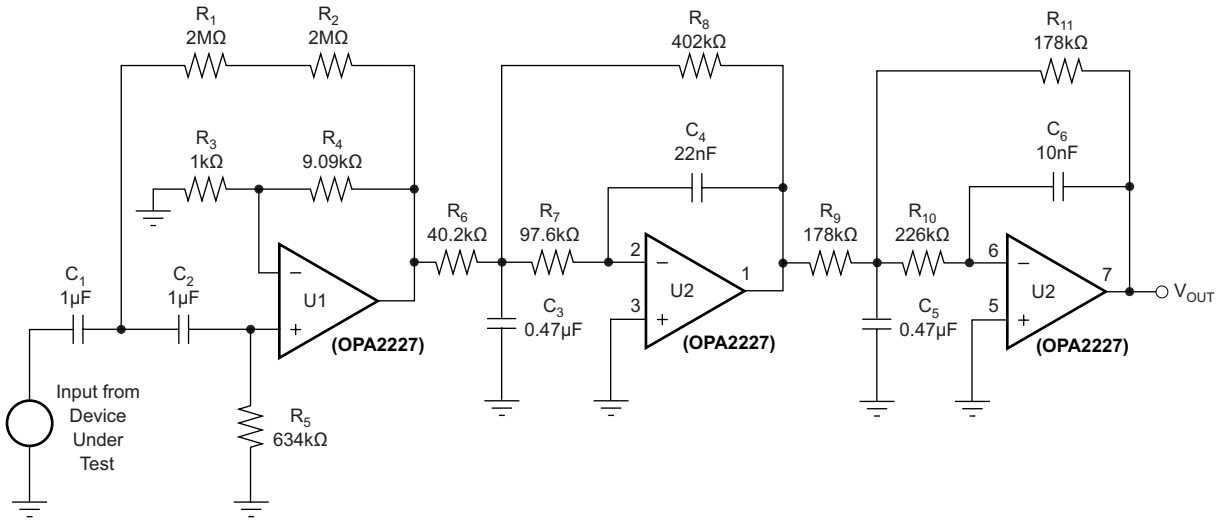


Figure 6. 0.1-Hz to 10-Hz Bandpass Filter Used to Test Wideband Noise of the OPA2227

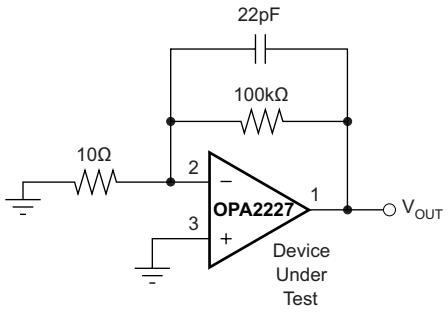


Figure 7. Noise Test Circuit

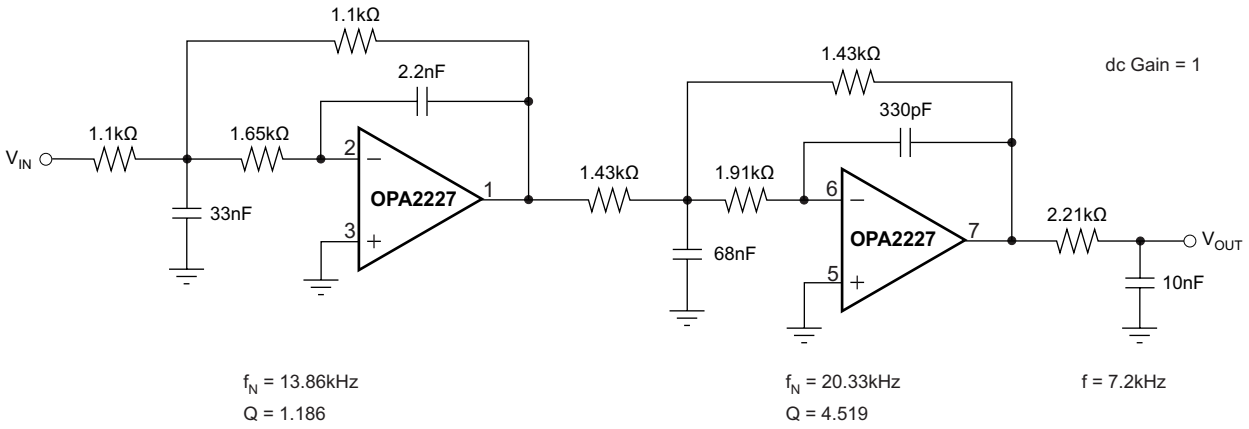


Figure 8. Three-Pole, 20-kHz Low Pass, 0.5-dB Chebyshev Filter

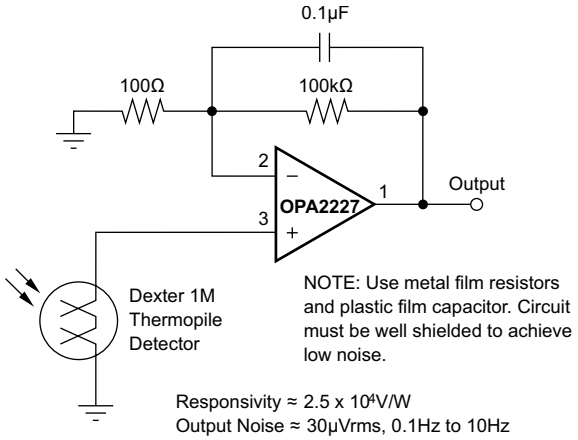


Figure 9. Long-Wavelength Infrared Detector Amplifier

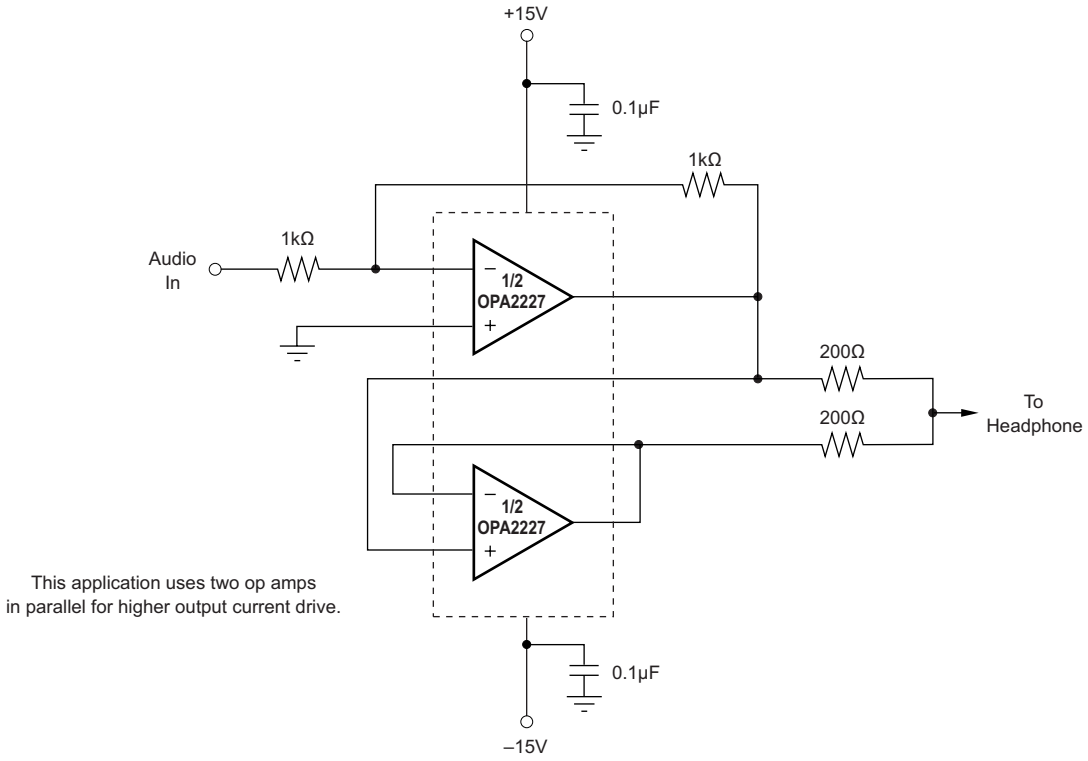


Figure 10. Headphone Amplifier

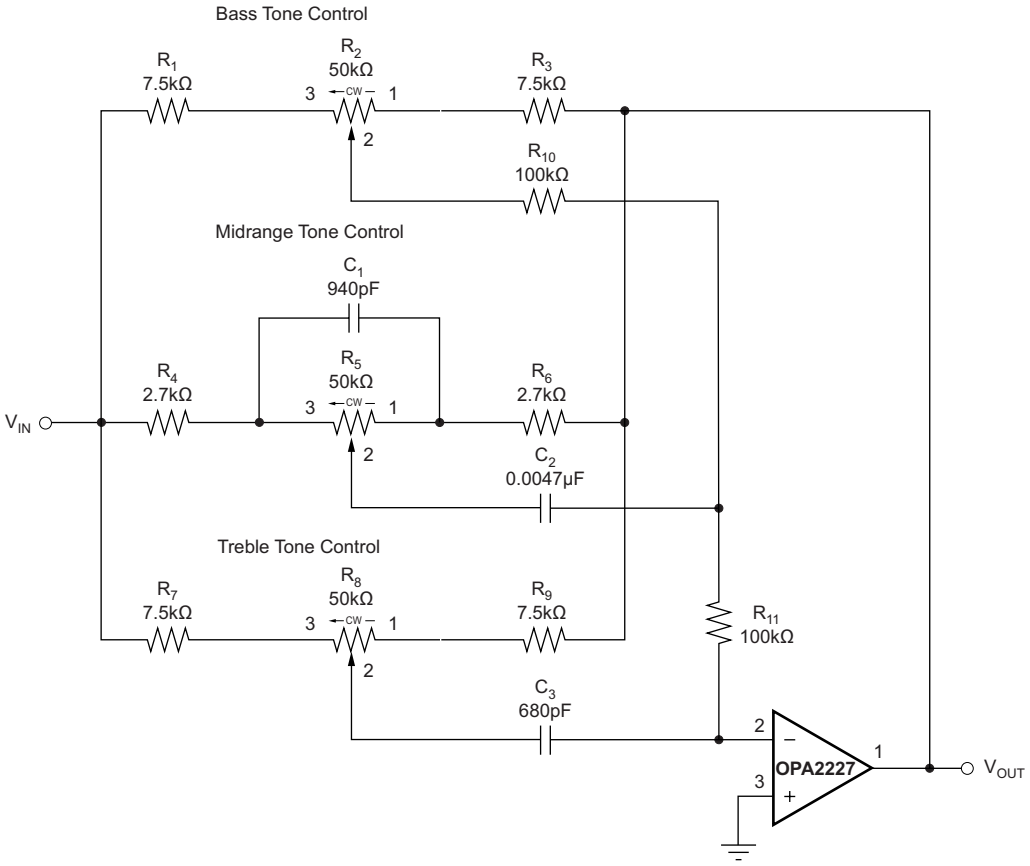


Figure 11. Three-Band ActiveTone Control (Bass, Midrange and Treble)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2227MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	2227EP
OPA2227MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	2227EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

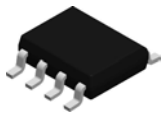
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2227-EP :

- Catalog : OPA2227

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

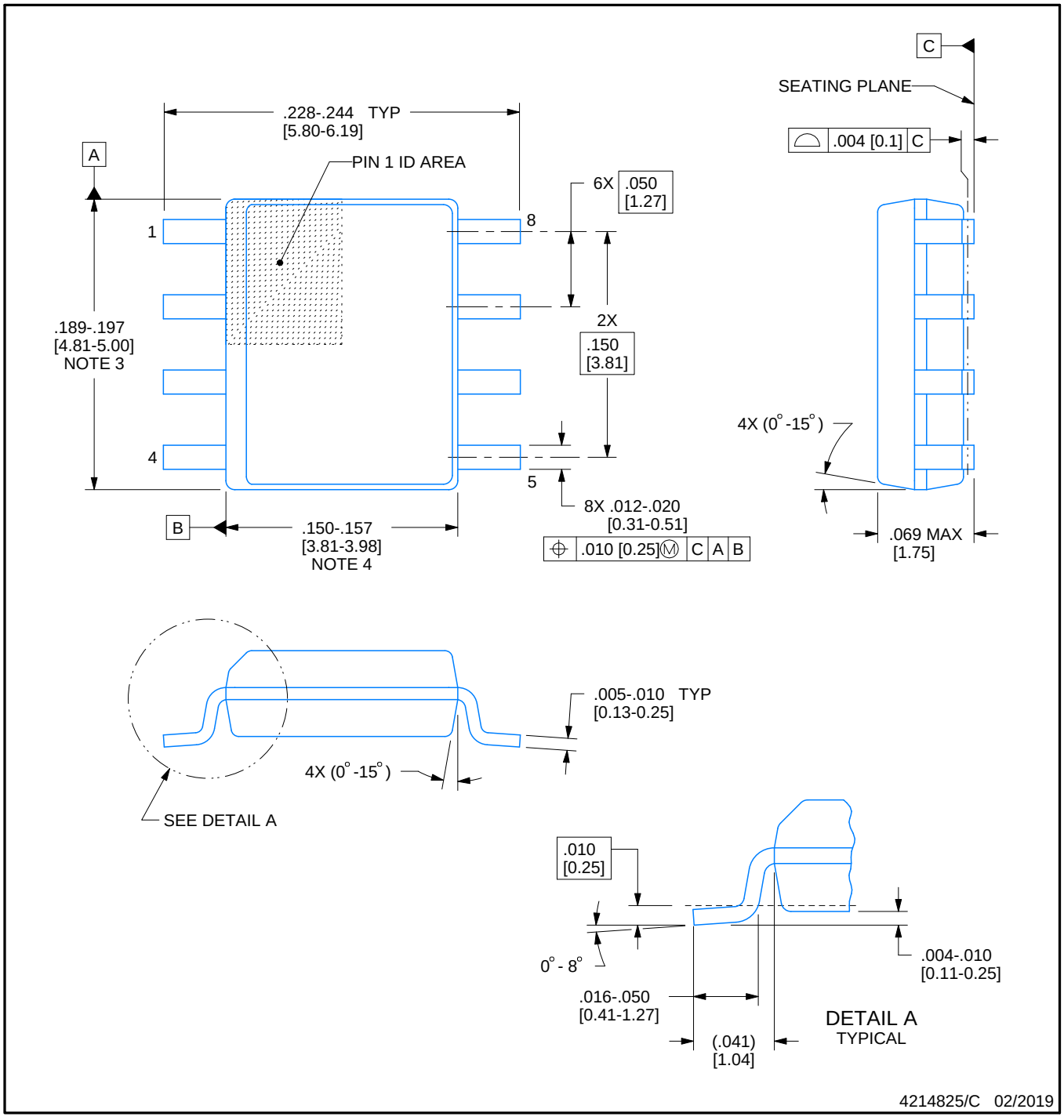


PACKAGE OUTLINE

D0008A

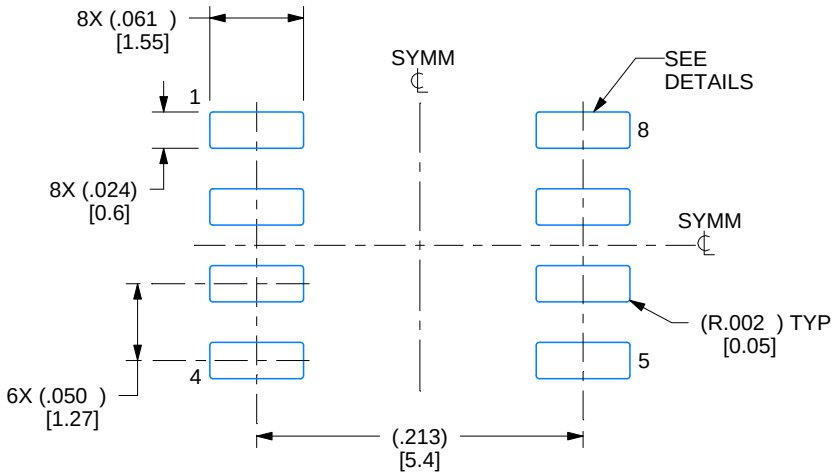
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

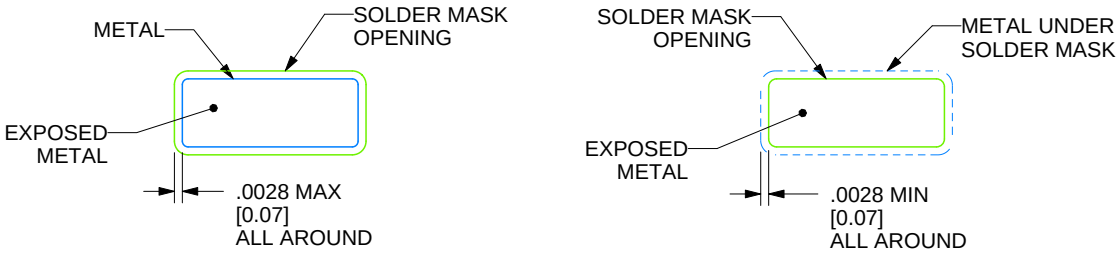


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

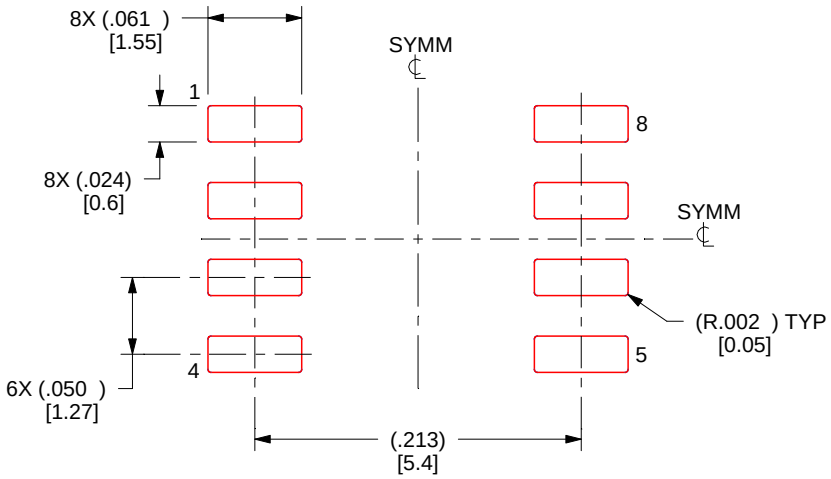
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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