TEXAS INSTRUMENTS
OPA211, OPA2211
JAJS198L – OCTOBER 2006 – REVISED JANUARY 2020

OPAx211 ノイズ 1.1nv/√Hz、低消費電力、高精度オペアンプ

1 特長

- 低い電圧ノイズ： 1kHz で 1.1nV/√Hz
- 入力電圧ノイズ：80nV$_{PP}$ (0.1～10Hz)
- THD + N: –136dB (G = 1、f = 1kHz)
- オフセット電圧：125µV (最大値)
- オフセット電圧ドリフト係数：0.35µV/℃ (標準値)
- 低消費電流：3.6mA/Ch (標準値)
- ユニティ・ゲイン安定
- ゲイン帯域幅積
  - 80MHz (G = 100)
  - 45MHz (G = 1)
- スルーレート：27 V/µs
- 16 ビット・セトリング：700ns
- 広い電源電圧範囲
  - ±2.25～±18V、4.5V～36V
- レール・ツー・レール出力
- 出力電流：30 mA
- SON-8 (3mm×3mm)、VSSOP-8、SOIC-8

2 アプリケーション

- 超音波スキャナ
- 半導体試験装置
- X 線システム
- 実験室およびフィールド用計測機器
- データ・アクイジション (DAQ)
- レーダー
- ワイヤレス通信テスト
- 地震検出データ・アクイジション
- DC 電源、AC 電源、電子負荷
- 電力アナライザ
- ソース・メジャー・ユニット（SMU）

3 概要

OPAx211シリーズの高精度オペアンプは、ノイズ密度が1.1nV/√Hzと非常に低く、消費電流がわずか3.6mAです。また、このシリーズはレール・ツー・レール出力を持ち、ダイナミック・レンジが最大化されます。

OPAx211シリーズのデバイスは電圧ノイズが非常に低く、電流ノイズも低く、高速で出力スイングが広いことから、PLLアプリケーションのループ・フィルタ・アンプに最適な選択肢です。

OPAx211シリーズのオペアンプは、高精度のデータ収集アプリケーション向けに、10Vの出力スイング全体で、16ビット精度に対して700nsのセトリング時間を実現しています。この AC 性能と、わずか 125µV のオフセットおよび 0.35µV/℃の温度ドリフト係数から、OPAx211 シリーズは高精度の 16 ビット・アナログ / デジタル・コンバータ (ADC) の駆動や、高分解能のデジタル / アナログ・コンバータ (DAC) の出力のバッファリングに最適です。

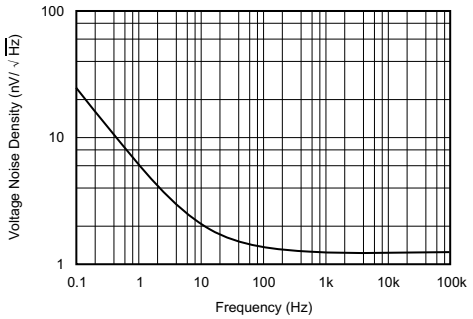
OPAx211シリーズは、デュアル電源で±2.25～±18V、またはシングル電源で4.5～36Vの広い電源電圧範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
OPA211	SOIC (8)	4.90mm×3.90mm
	SON (8)	3.00mm×3.00mm
	VSSOP (8)	3.00mm×3.00mm
OPA2211	SON (8)	3.00mm×3.00mm
	SO PowerPAD (8)	4.90mm × 3.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

入力電圧ノイズ密度と周波数との関係



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision K (September 2018) から **Revision L** に変更 — **Page**

- Deleted NOM value from supply voltage in the *Recommended Operating Conditions* table ... 7
- Changed operating temperature to specified temperature in *Recommended Operating Conditons* table, and changed MIN and MAX from –55°C and +150°C to –40°C and +125°C, respectively ... 7
- Changed electrical characteristics table titles to clarify difference between standard and high-grade devices ... 9

Revision J (February 2018) から **Revision K** に変更 — **Page**

- GPN のフォーマットを「OPA2x11」から「OPAx211」に 変更 ... 1
- Corrected system-generated errors: "Time" units from "ms/div" back to "µs/div" and unit for resistors from "W" back to "Ω" in *Typical Characteristics* ... 13
- Corrected system-generated error in unit for resistors from "W" back to "Ω" in *図 43* ... 22
- Reverted 図 51 back to that of rev. I ... 30

Revision I (June 2016) から **Revision J** に変更 — **Page**

- 製品ステータスを混在ステータスから量産データに 変更 ... 1
- Deleted *Device Comparison* table ... 5
- 変更 formatting of document reference in *EMI Rejection* section ... 25
- 変更 formatting of document references in *SON Layout Guidelines* section ... 30
- 変更「*関連資料*」セクションのドキュメント参照のフォーマット ... 31

Revision H (November 2015) から **Revision I** に変更 — **Page**

- Changed the SON pin number for V+ from 4 to 7 in the *Pin Functions: OPA211* table ... 5
- Changed the SON pin number for V- From: 7 To: 4 in the *Pin Functions: OPA211* table ... 5

Revision G (May 2009) から Revision H に変更 **Page**

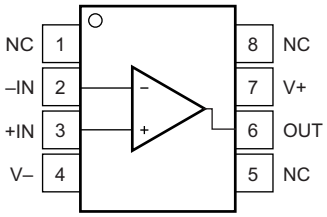
- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを 追加 1

5 概要（続き）

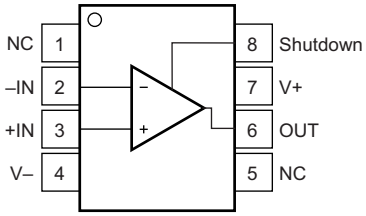
OPA211は小型のSON-8 (3mm×3mm)、VSSOP-8、SOIC-8パッケージで供給されます。デュアル・バージョンのOPA2211 は、SON-8 (3 mm × 3 mm) または SO-8 PowerPAD™パッケージで供給されます。このシリーズのオペアンプは、T_A = -40℃～+125℃で動作が規定されています。

6 Pin Configuration and Functions

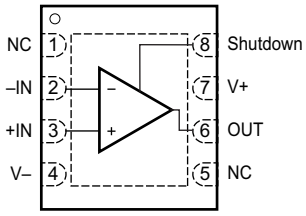
OPA211 D Package
8-Pin SOIC
Top View



OPA211 DGK Package
8-Pin VSSOP
Top View



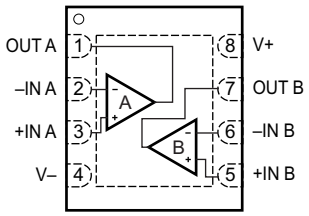
OPA211 DRG Package
8-Pin SON With Exposed Thermal Pad
Top View



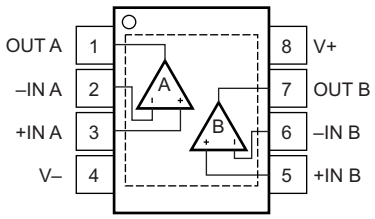
Pin Functions: OPA211

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5	—	No internal connection. This pin can be left floating or connected to any voltage between (V–) and (V+).
OUT	6	O	Output
Shutdown	8	I	Shutdown, active high The shutdown function is as follows: Device enabled: (V–) ≤ $V_{SHUTDOWN}$ ≤ (V+) – 3 V Device disabled: $V_{SHUTDOWN}$ ≥ (V+) – 0.35 V
V+	7	I	Positive power supply
V–	4	I	Negative power supply
Thermal pad	—	—	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad to the printed circuit board is required and improves heat dissipation and provides specified performance.

OPA2211 DRG Package
8-Pin SON With Exposed Thermal Pad
Top View



OPA2211 DDA Package
8-Pin SO PowerPAD With Exposed Thermal Pad
Top View



Pin Functions: OPA2211

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input channel A
–IN A	2	I	Inverting input channel A
+IN B	5	I	Noninverting input channel B
–IN B	6	I	Inverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V+	8	I	Positive power supply
V–	4	I	Negative power supply
Thermal pad	—	—	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		40	V
	Input voltage	(V–) – 0.5	(V+) + 0.5	V
	Input current (any pin except power-supply pins)		±10	mA
	Output short-circuit(2)	Continuous		
T_A	Operating temperature	–55	150	°C
T_J	Junction temperature		200	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
T_A	Specified temperature	–40	25	125	°C

7.4 Thermal Information: OPA211 and OPA211A

THERMAL METRIC(1)		OPA211, OPA211A			UNIT
		D (SOIC)	DRG (SON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, high-K board	122.2	125	184.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.5	N/A	71.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	28.8	104.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	3	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.6	25	103.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	19.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2211 and OPA2211A

THERMAL METRIC(1)		OPA2211, OPA2211A		UNIT
		DDA (SO-PowerPAD)	DRG (SON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, high-K board	50.4	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	28.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics: Standard Grade OPAx211A

at T_A = 25°C, V_S = ±2.25 to ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±15 V	OPA211A		±30	±125	µV
			OPA2211A		±50	±150	
dV_{OS}/dT	Input offset drift	V_S = ±15 V, T_A = –40°C to +125°C			±0.35	±1.5	µV/°C
PSRR	Input offset voltage vs power supply	T_A = 25°C			0.1	1	µV/V
		T_A = –40°C to +125°C				3	
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			±60	±175	nA
		V_{CM} = 0 V, T_A = –40°C to +125°C	OPA211A			±200	
			OPA2211A			±250	
I_{OS}	Input offset current	V_{CM} = 0 V			±25	±100	nA
		V_{CM} = 0 V, T_A = –40°C to +125°C				±150	
NOISE							
e_n	Input voltage noise	f = 0.1 to 10 Hz			80		nV_{PP}
	Input voltage noise density	f = 10 Hz			2		$nV/\sqrt{Hz}$
		f = 100 Hz			1.4		
		f = 1 kHz			1.1		
I_n	Input current noise density	f = 10 Hz			3.2		$pA/\sqrt{Hz}$
		f = 1 kHz			1.7		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	V_S ≥ ±5 V		(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5 V		(V–) + 2		(V+) – 1.4	
CMRR	Common-mode rejection ratio	V_S ≥ ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C		114	120		dB
		V_S < ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C		110	120		
INPUT IMPEDANCE							
	Differential				20 || 8		kΩ || pF
	Common-mode				10 || 2		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ, T_A = –40°C to +125°C		114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 600 Ω		110	114		
		OPA211A: (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C		110			
		OPA211A: (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, 15 mA < I_O ≤ 30 mA, T_A = –40°C to +125°C		103			
		OPA2211A: (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C		100			

Electrical Characteristics: Standard Grade OPAx211A (continued)

at T_A = 25°C, V_S = ±2.25 to ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 100			80		MHz
		G = 1			45		
SR	Slew rate				27		V/µs
t_S	Settling time	V_S = ±15 V, G = –1, 10-V step, C_L = 100 pF	0.01%		400		ns
			0.0015% (16-bit)		700		
	Overload recovery time	G = –10			500		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 600 Ω			0.000015%		
					–136		dB
OUTPUT							
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB, T_A = –40°C to +125°C		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} ≥ 110 dB		(V–) + 0.6		(V+) – 0.6	
		I_O < 15 mA, A_{OL} ≥ 110 dB, T_A = –40°C to +125°C		(V–) + 0.6		(V+) – 0.6	
I_{SC}	Short-circuit current				+30/–45		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1 MHz			5		Ω
SHUTDOWN							
$V_{Shutdown}$	Shutdown pin input voltage(1)	Device disabled (shutdown)		(V+) – 0.35			V
		Device enabled				(V+) – 3	
	Shutdown pin leakage current				1		µA
	Turn-on time(2)				2		µs
	Turn-off time(2)				3		µs
	Shutdown current	Shutdown (disabled)			1	20	µA
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A			3.6	4.5	mA
		I_{OUT} = 0 A, T_A = –40°C to +125°C				6	

(1) When disabled, the output assumes a high-impedance state.
(2) See *Typical Characteristics* curves (図 39 through 図 41).

7.7 Electrical Characteristics: High-Grade OPAx211

at T_A = 25°C, V_S = ±2.25 to ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±15 V		±20	±50	µV
dV_{OS}/dT	Input offset drift	V_S = ±15 V, T_A = –40°C to +125°C		±0.15	±0.85	µV/°C
PSRR	Input offset voltage vs power supply	T_A = 25°C		0.1	0.5	µV/V
		T_A = –40°C to +125°C			3	
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±50	±125	nA
		V_{CM} = 0 V, T_A = –40°C to +125°C			±200	
I_{OS}	Input offset current	V_{CM} = 0 V		±20	±75	nA
		T_A = –40°C to +125°C			±150	
NOISE						
e_n	Input voltage noise	f = 0.1 to 10 Hz		80		nV_{PP}
	Input voltage noise density	f = 10 Hz		2		$nV/\sqrt{Hz}$
		f = 100 Hz		1.4		
		f = 1 kHz		1.1		$pA/\sqrt{Hz}$
I_n	Input current noise density	f = 10 Hz		3.2		
		f = 1 kHz		1.7		
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	V_S ≥ ±5 V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5 V	(V–) + 2		(V+) – 1.4	
CMRR	Common-mode rejection ratio	V_S ≥ ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	114	120		dB
		V_S < ±5 V, (V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V, T_A = –40°C to +125°C	110	120		
INPUT IMPEDANCE						
	Differential			20 || 8		kΩ || pF
	Common-mode			10 || 2		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ, T_A = –40°C to +125°C,	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 600 Ω	110	114		
		OPA211: (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, I_O ≤ 15 mA, T_A = –40°C to +125°C	110			
		OPA211: (V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, 15 mA < I_O ≤ 30 mA, T_A = –40°C to +125°C	103			

Electrical Characteristics: High-Grade OPAx211 (continued)

at T_A = 25°C, V_S = ±2.25 to ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 100			80		MHz
		G = 1			45		
SR	Slew rate				27		V/µs
t_S	Settling time	V_S = ±15 V, G = –1, 10-V step, C_L = 100 pF	0.01%		400		ns
			0.0015% (16-bit)		700		ns
	Overload recovery time	G = –10			500		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 600 Ω			0.000015%		
					–136		dB
OUTPUT							
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB, T_A = –40°C to +125°C		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} ≥ 110 dB		(V–) + 0.6		(V+) – 0.6	
		I_O < 15 mA, A_{OL} ≥ 110 dB, T_A = –40°C to +125°C		(V–) + 0.6		(V+) – 0.6	
I_{SC}	Short-circuit current				+30 /–45		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1 MHz			5		Ω
SHUTDOWN							
$V_{Shutdown}$	Shutdown pin input voltage(1)	Device disabled (shutdown)		(V+) – 0.35			V
		Device enabled				(V+) – 3	
	Shutdown pin leakage current				1		µA
	Turn-on time(2)				2		µs
	Turn-off time(2)				3		µs
	Shutdown current	Shutdown (disabled)			1	20	µA
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A			3.6	4.5	mA
		I_{OUT} = 0 A, T_A = –40°C to +125°C				6	

(1) When disabled, the output assumes a high-impedance state.
(2) See *Typical Characteristics* curves (図 39 through 図 41).

7.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

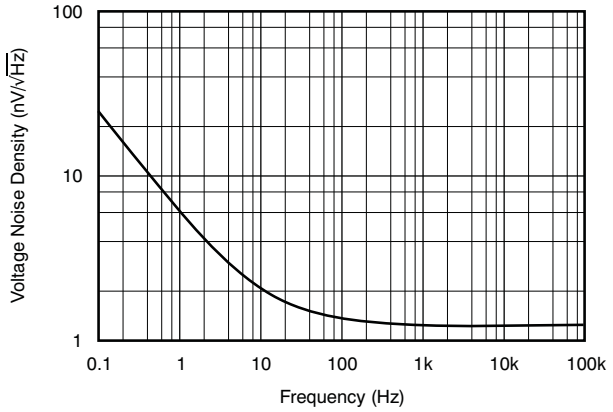


図 1. Input Voltage Noise Density vs Frequency

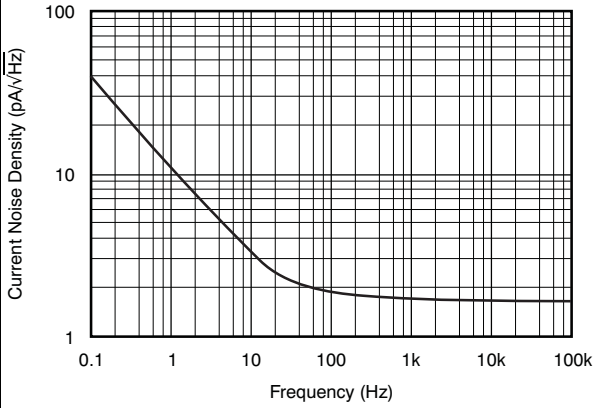


図 2. Input Current Noise Density vs Frequency

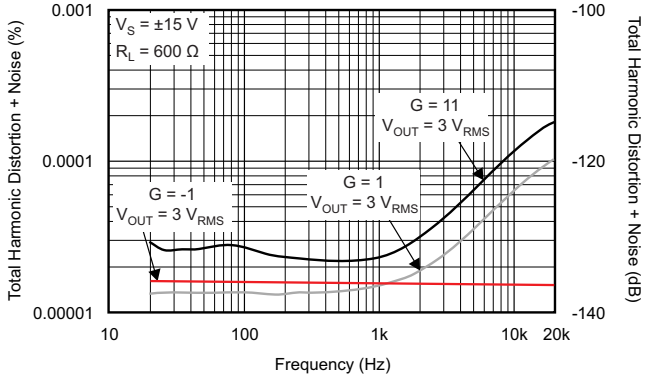


図 3. THD + N Ratio vs Frequency

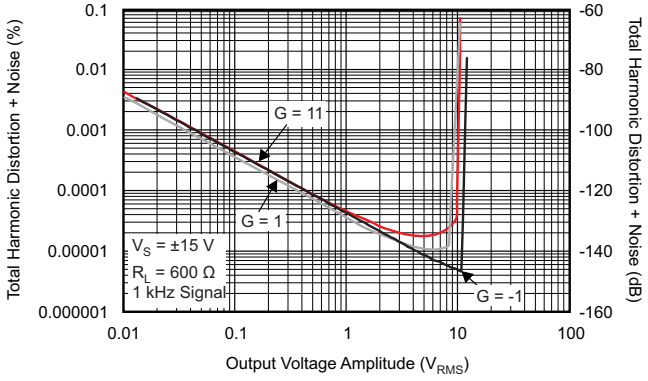


図 4. THD + N Ratio vs Output Voltage Amplitude

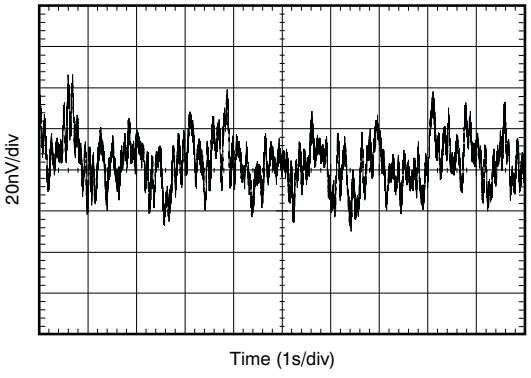


図 5. 0.1- to 10-Hz Noise

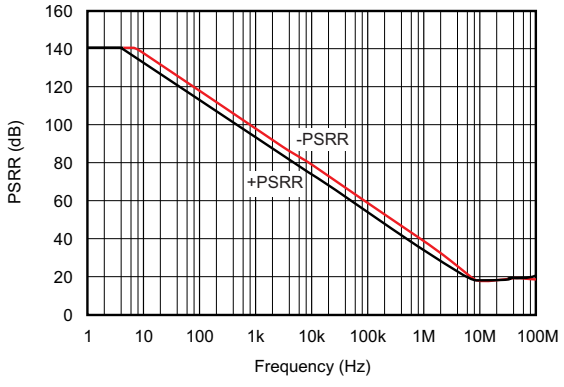


図 6. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

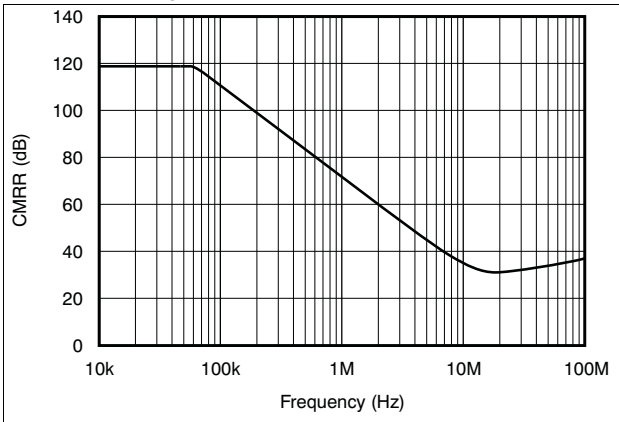


図 7. Common-Mode Rejection Ratio vs Frequency

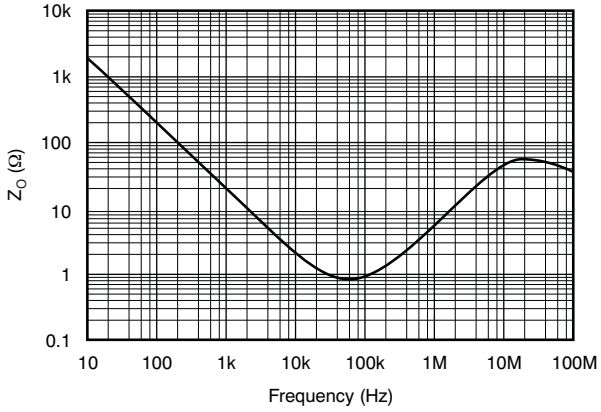


図 8. Open-Loop Output Impedance vs Frequency

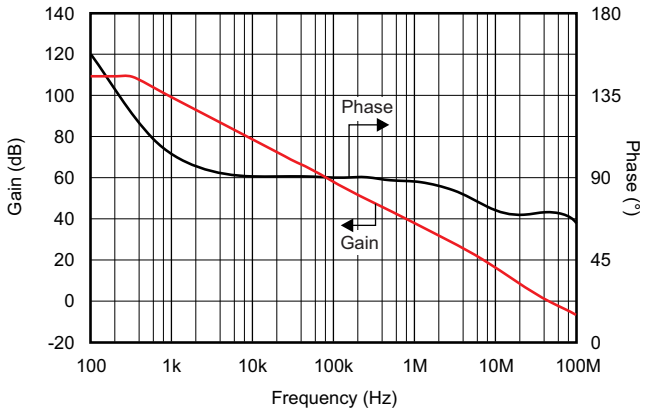


図 9. Gain and Phase vs Frequency

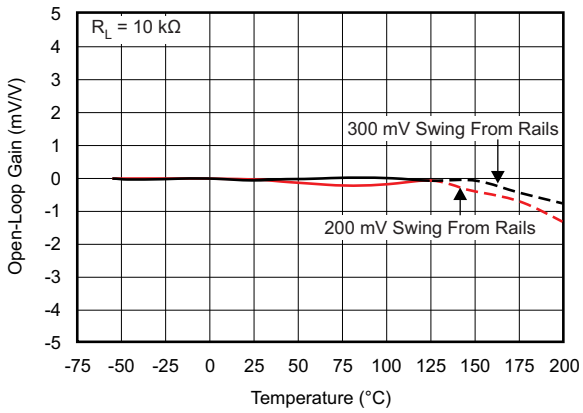


図 10. Open-Loop Gain vs Temperature

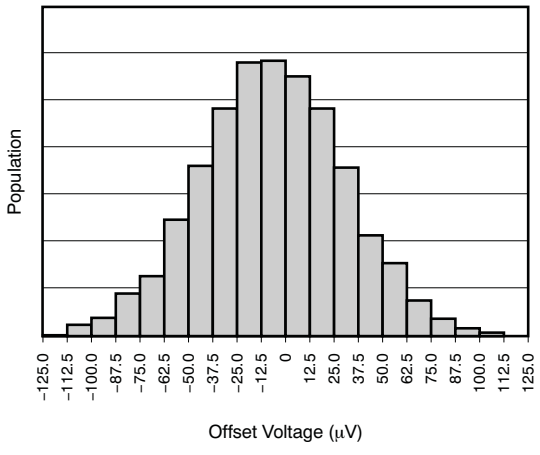


図 11. Offset Voltage Production Distribution

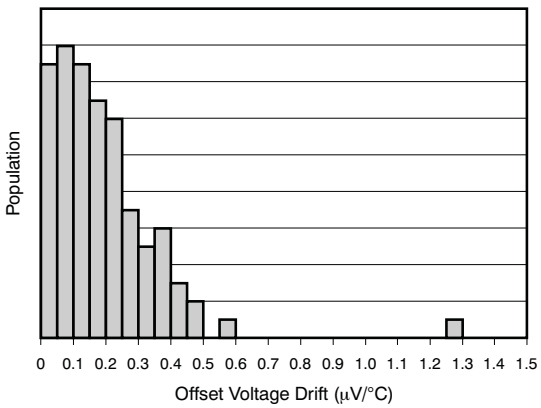


図 12. Offset Voltage Drift Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

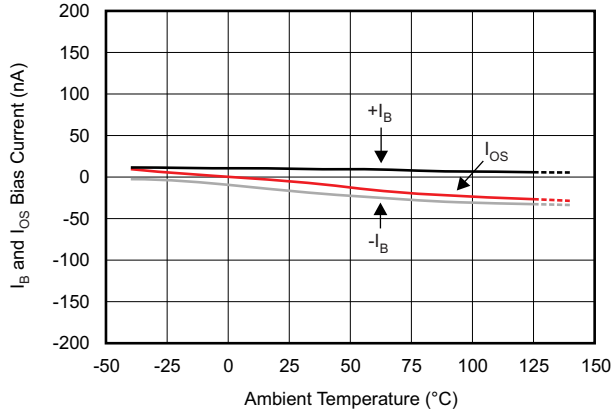


図 13. I_B and I_{OS} Current vs Temperature

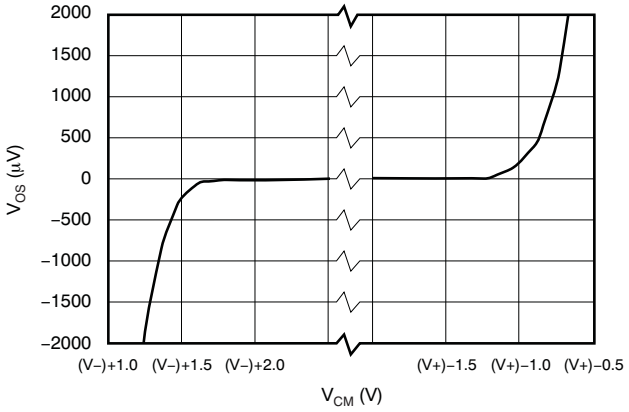


図 14. Offset Voltage vs Common-Mode Voltage

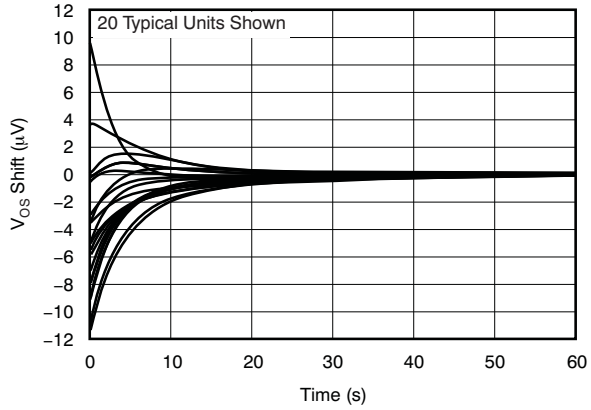


図 15. V_{OS} Warm-Up

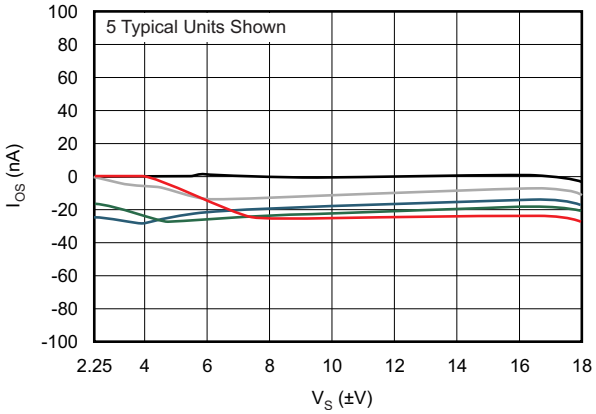


図 16. Input Offset Current vs Supply Voltage

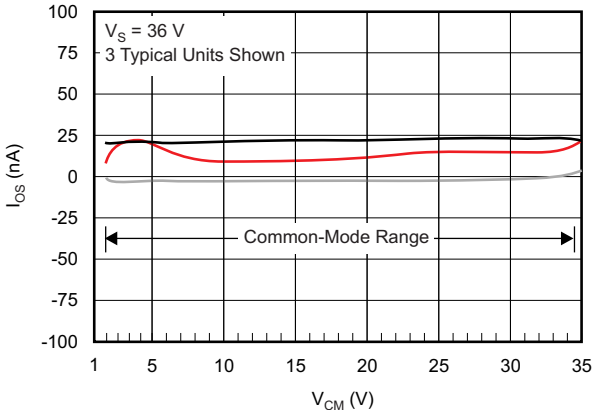


図 17. Input Offset Current vs Common-Mode Voltage

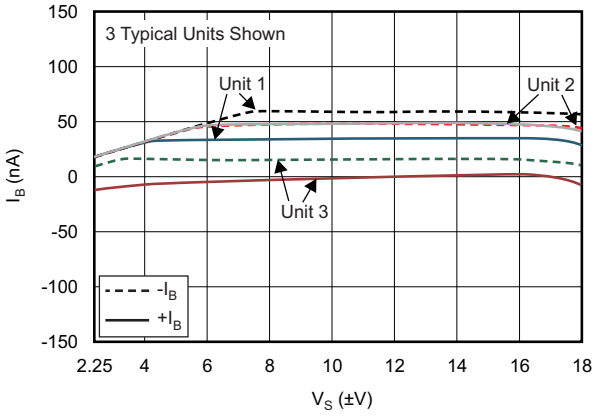


図 18. Input Bias Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

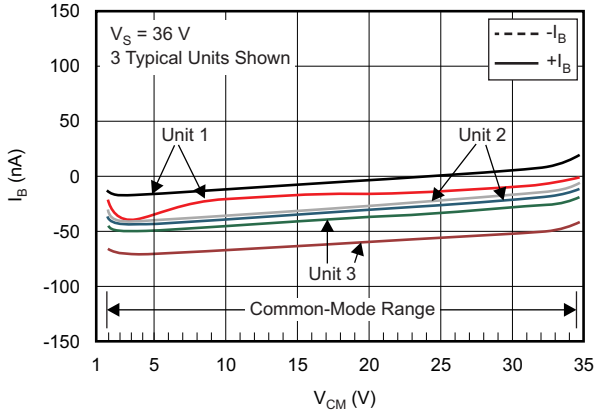


図 19. Input Bias Current vs Common-Mode Voltage

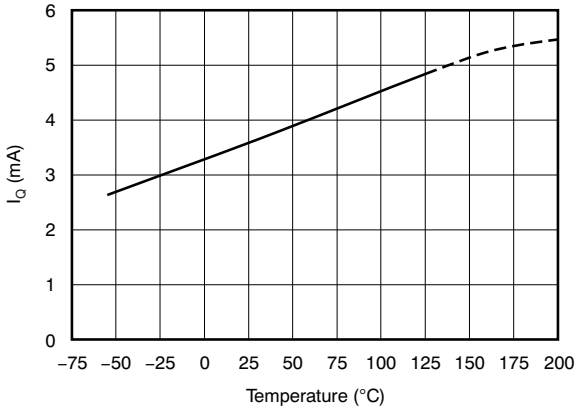


図 20. Quiescent Current vs Temperature

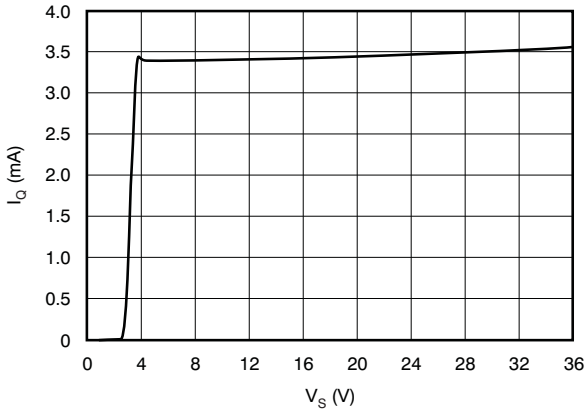


図 21. Quiescent Current vs Supply Voltage

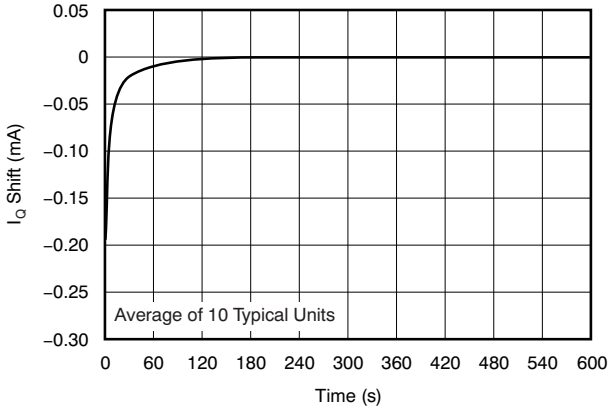


図 22. Normalized Quiescent Current vs Time

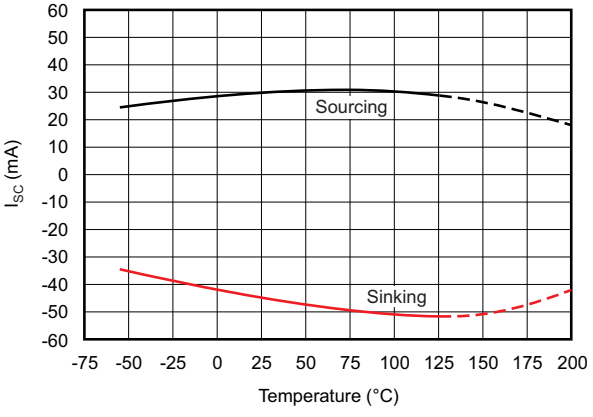


図 23. Short-Circuit Current vs Temperature

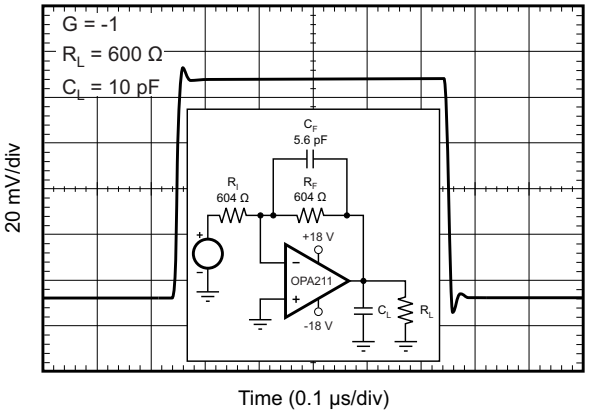


図 24. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

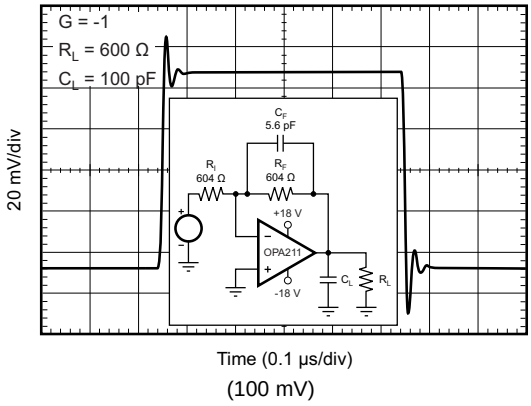


図 25. Small-Signal Step Response

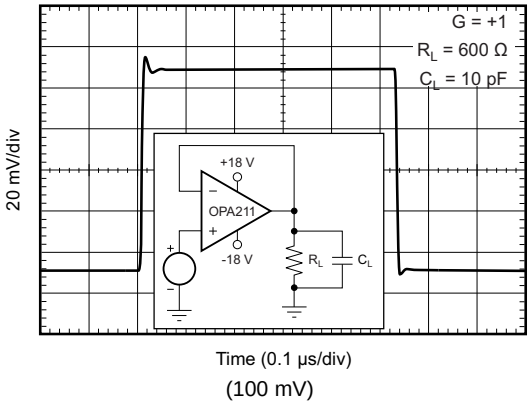


図 26. Small-Signal Step Response

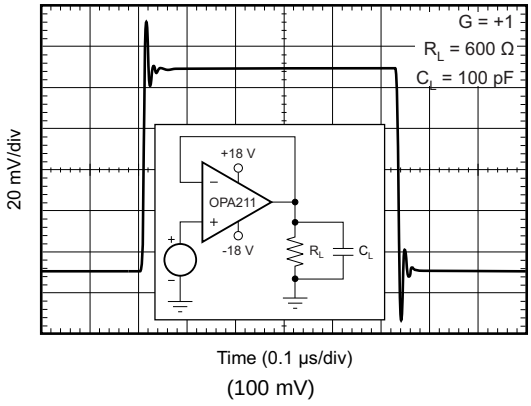


図 27. Small-Signal Step Response

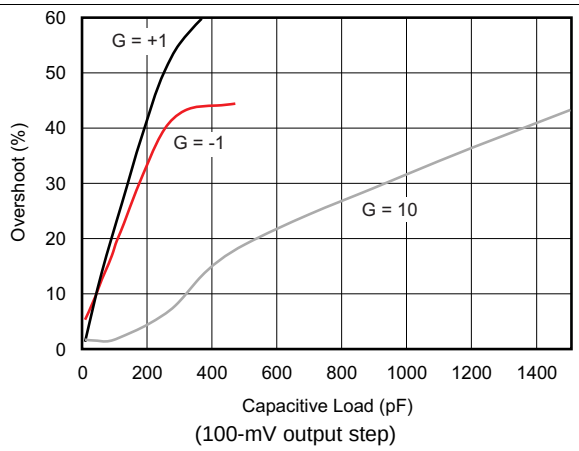


図 28. Small-Signal Overshoot vs Capacitive Load

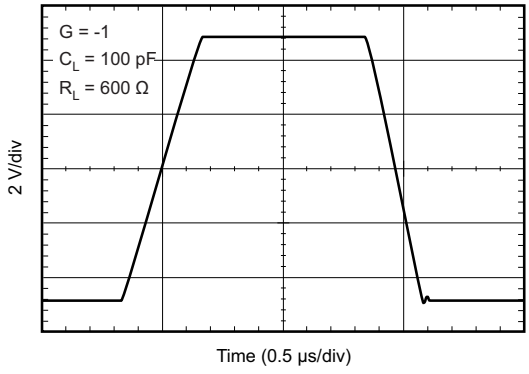


図 29. Large-Signal Step Response

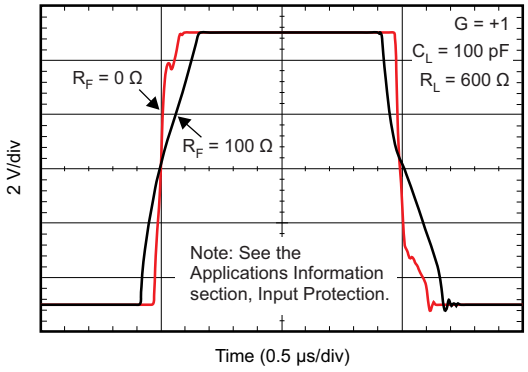


図 30. Large-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

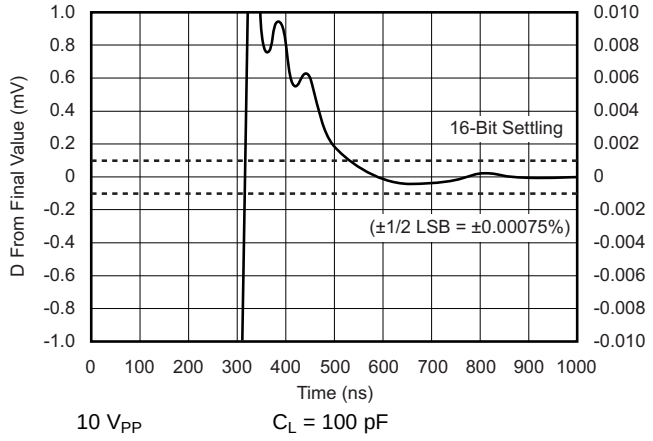


図 31. Large-Signal Positive Settling Time

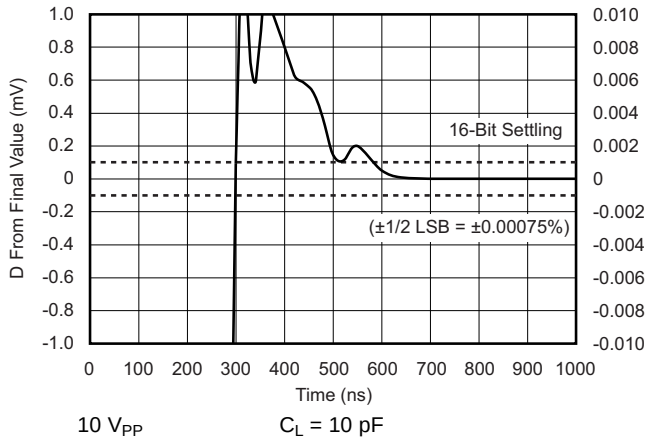


図 32. Large-Signal Positive Settling Time

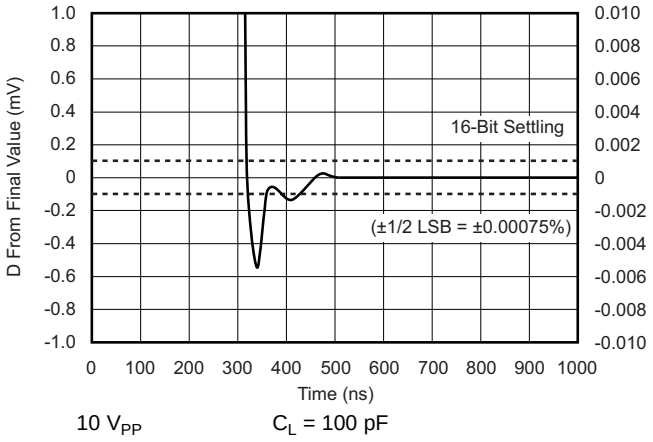


図 33. Large-Signal Negative Settling Time

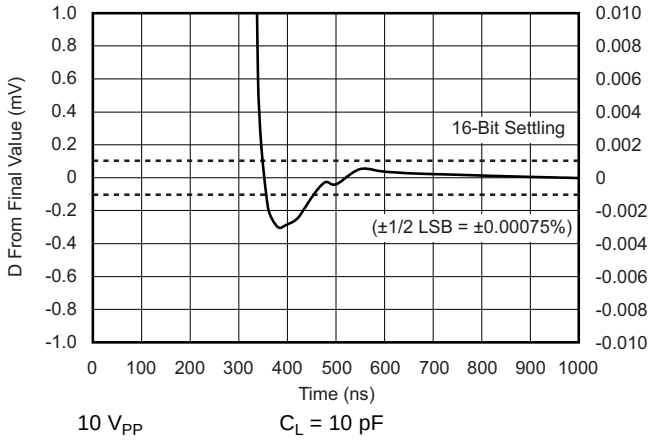


図 34. Large-Signal Negative Settling Time

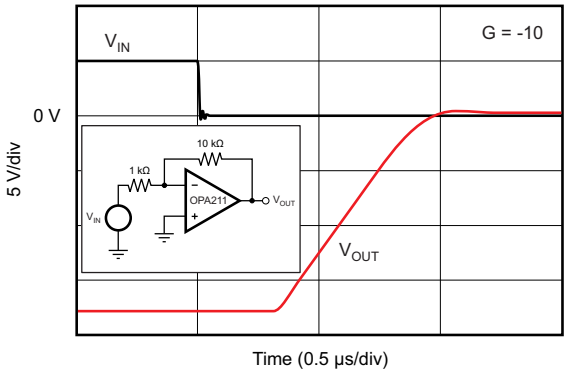


図 35. Negative Overload Recovery

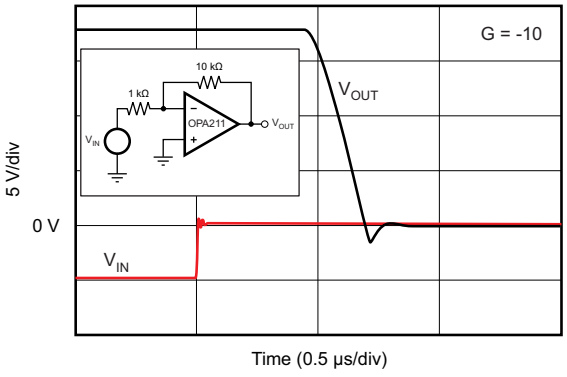


図 36. Positive Overload Recovery

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

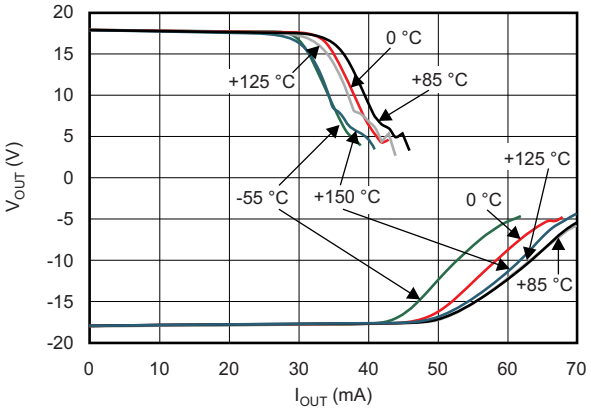


図 37. Output Voltage vs Output Current

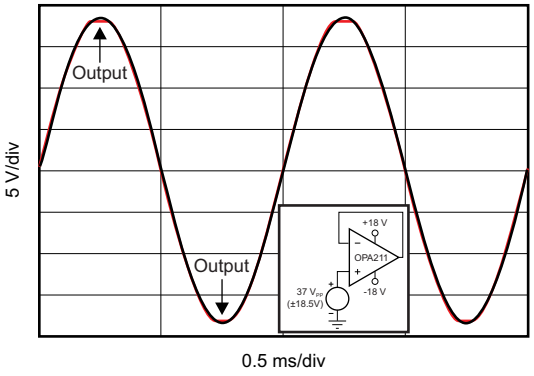


図 38. No Phase Reversal

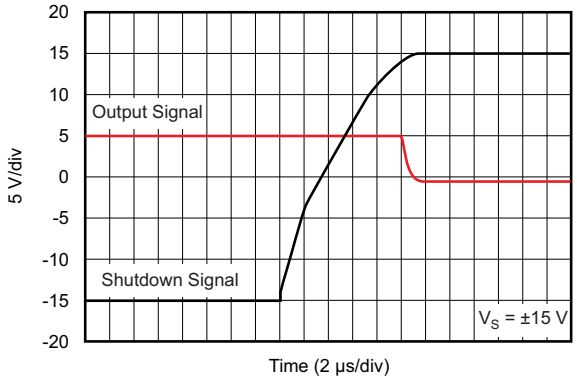


図 39. Turnoff Transient

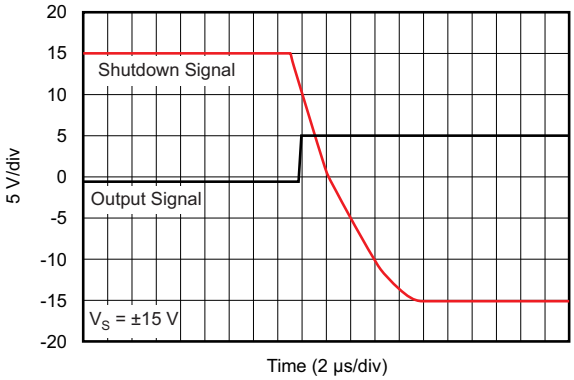


図 40. Turnon Transient

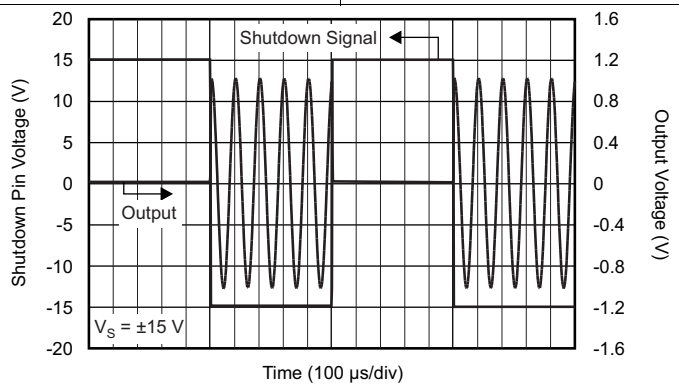


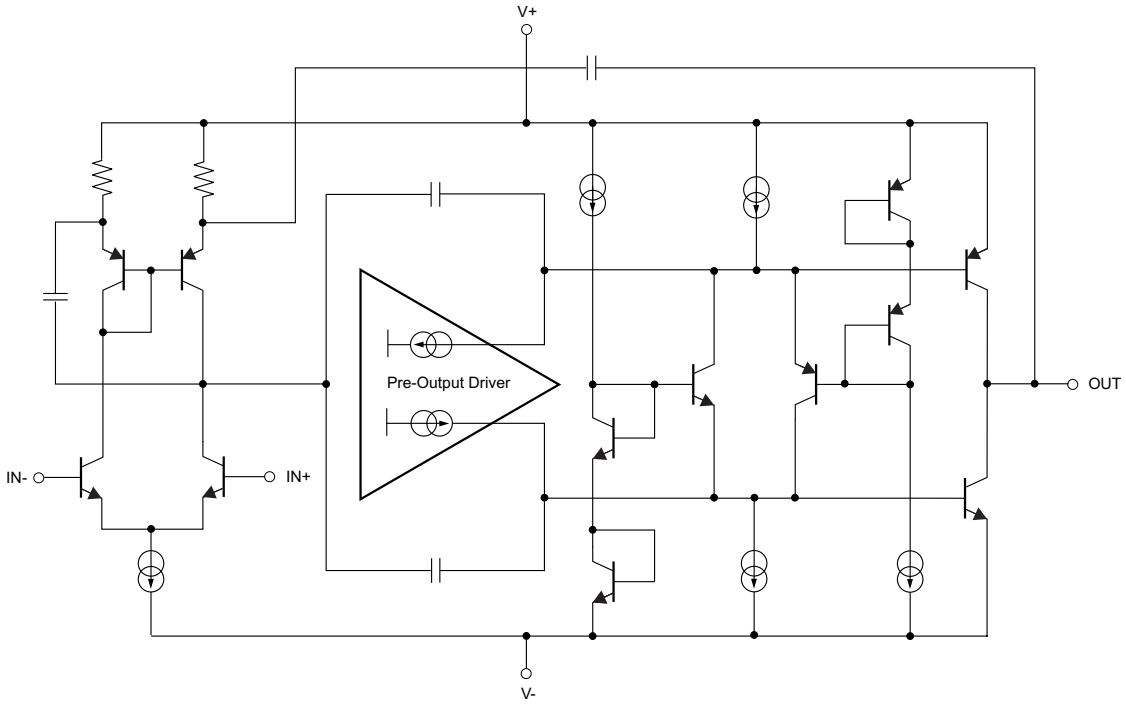
図 41. Turnon and Turnoff Transient

8 Detailed Description

8.1 Overview

The OPAx211 family of operational amplifiers are available in single-channel versions (OPA211) and dual-channel versions (OPA2211). Single-channel versions are available with and without shutdown. The OPAx211 family of operational amplifiers features ultra-low noise of 1.1-nV/√Hz, low total harmonic distortion + noise of 0.000015% and wide, rail-to-rail output swing. These unique features makes the OPAx211 family a great choice for wide dynamic range applications and driving high-speed analog-to-digital converters. The OPAx211 family is protected against excessive differentially applied input voltages and is fully characterized for electromagnetic interference rejection ratio (EMIRR). The OPAx211 operates with as little as 4.5-V (±2.25-V) power supply voltage and with power supply voltages up to 36 V (±18 V). The OPAx211 family is specified to operate from –40°C to +125°C with little change in parametric behavior over the full temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion Measurements

OPA211 series operational amplifiers have excellent distortion characteristics. THD + noise is below 0.0001% (G = 1, V_O = 3 V_{RMS}) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load.

The distortion produced by OPAx211 series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit shown in 図 43 can extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. 図 43 shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101.

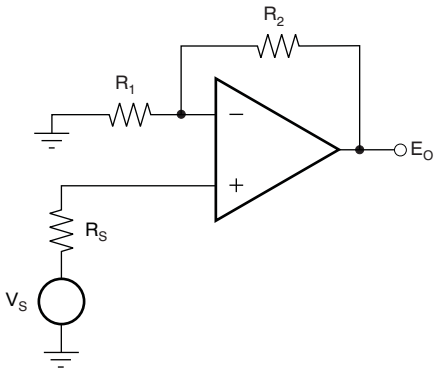
Feature Description (continued)

注

The input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

Noise in Noninverting Gain Configuration



Noise at the output:

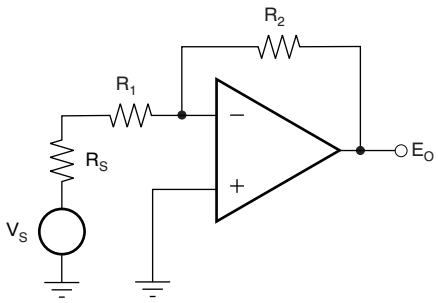
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

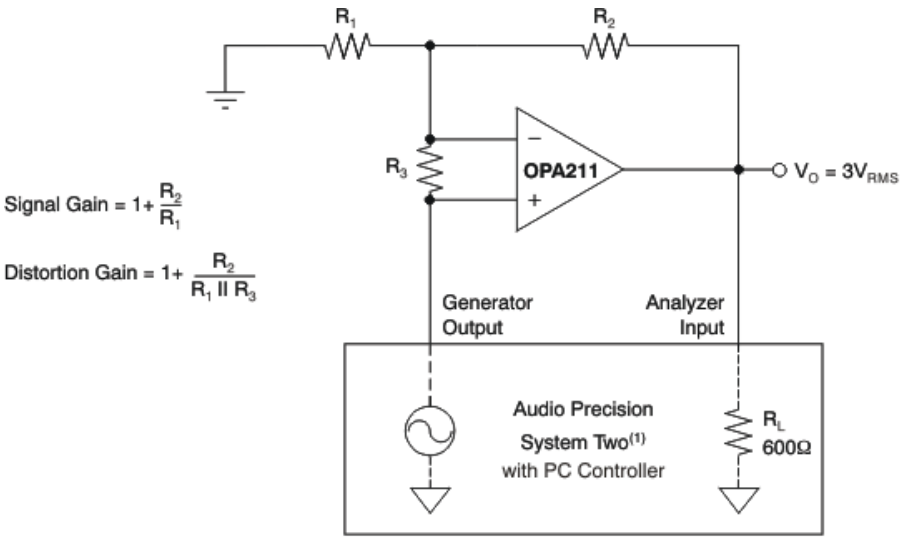
Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1nV/\sqrt{Hz}$ and $i_n = 1.7pA/\sqrt{Hz}$.

図 42. Noise Calculation in Gain Configurations



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

NOTE: (1) Measurement BW = 80kHz.

図 43. Distortion Test Circuit

8.4 Device Functional Modes

The OPAx211 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx211 series is 36 V (±18 V).

8.4.1 Shutdown

The shutdown (enable) function of the OPA211 is referenced to the positive supply voltage of the operational amplifier. A valid high disables the operational amplifier. A valid high is defined as (V+) – 0.35 V of the positive supply applied to the shutdown pin. A valid low is defined as (V+) – 3 V below the positive supply pin. For example, with V_{CC} at ±15 V, the device is enabled at or below 12 V. The device is disabled at or above 14.65 V. If dual or split power supplies are used, make sure the valid high or valid low input signals are properly referred to the positive supply voltage. This pin must be connected to a valid high or low voltage or driven, and not left open-circuit. The enable and disable times are provided in the *Typical Characteristics* section (see 図 39 through 図 41). When disabled, the output assumes a high-impedance state.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA211 and OPA2211 are unity-gain stable, precision operational amplifiers with very-low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

9.1.1 Operating Voltage

OPA211 series operational amplifiers operate from ±2.25- to ±18-V supplies while maintaining excellent performance. The OPA211 series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

9.1.2 Input Protection

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in 図 44. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is shown in 図 30 of the *Typical Characteristics*. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the *Noise Performance* section of this data sheet. 図 44 shows an example implementing a current-limiting feedback resistor.

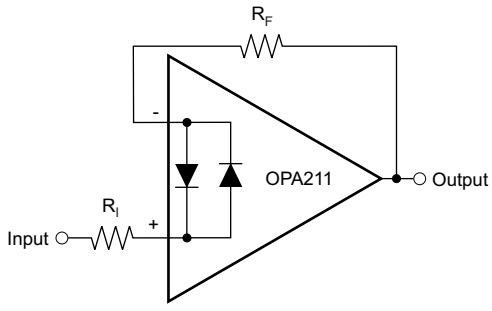


図 44. Pulsed Operation

Application Information (continued)

9.1.3 Noise Performance

図 45 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPAx211 has very low voltage noise, making the family a viable option for low source impedances (less than 2 kΩ). A similar precision operational amplifier, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very low current noise) may provide improved performance. The equation in 図 45 is shown for the calculation of the total circuit noise.

注

e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

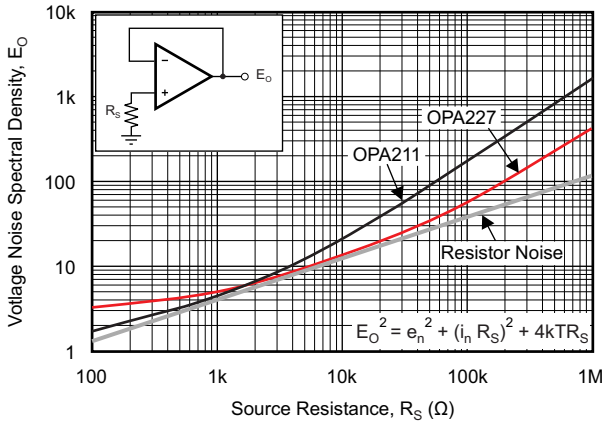


図 45. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

9.1.4 Basic Noise Calculations

Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 図 45. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

図 45 depicts total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

図 42 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Application Information (continued)

9.1.5 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.図 46

The EMIRR IN+ of the OPA211 is plotted versus frequency as shown in 図 46. If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA211 unity-gain bandwidth is 45 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

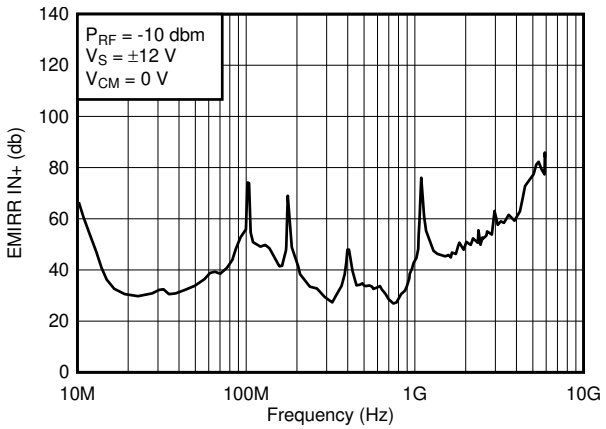


図 46. OPA211 EMIRR

表 1 shows the EMIRR IN+ values for the OPA211 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Application Information (continued)

表 1. OPA211 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	34.6 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	46 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	56.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	61.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	76.7 dB

9.1.6 EMIRR +IN Test Configuration

図 47shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM).

注

A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter.

The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

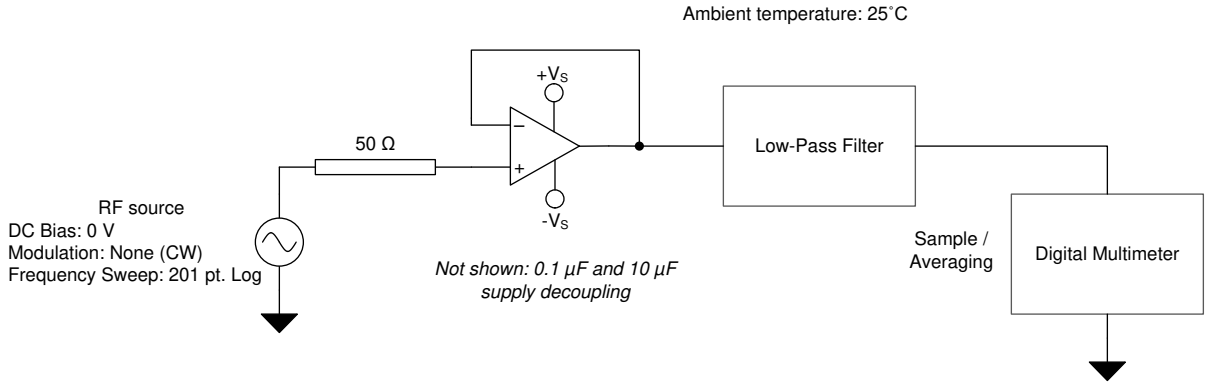


図 47. EMIRR +IN Test Configuration

9.1.7 Electrical Overstress

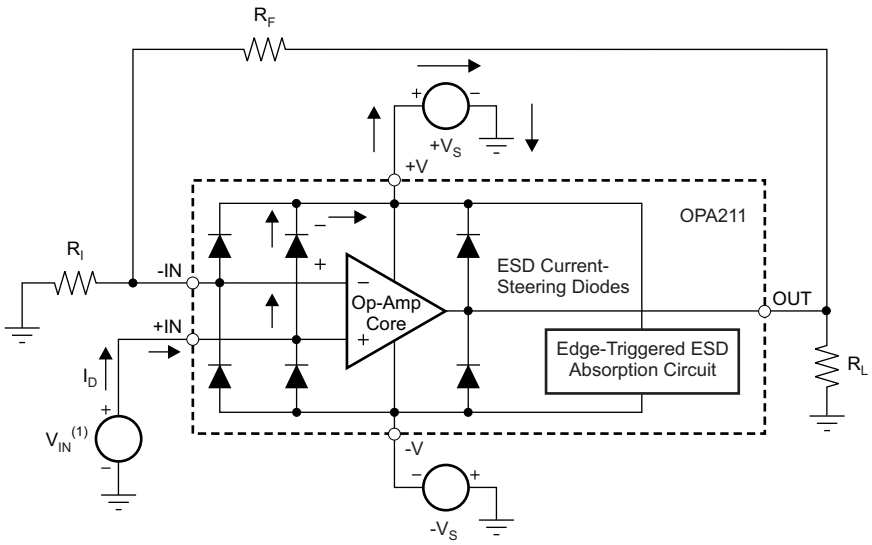
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. 図 48 shows the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that shown in 図 48, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500$ mV.

図 48. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application

図 48 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $-V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

9.2 Typical Application

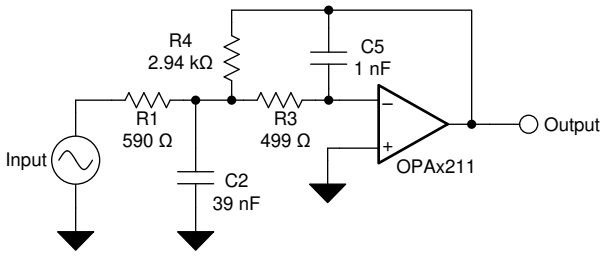


図 49. OPAx211 Simplified Schematic

9.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx211 devices are designed to construct high-speed, high-precision active filters. 図 49 shows a second-order low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 図 50 . Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by 式 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design.WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

Typical Application (continued)

9.2.3 Application Curve

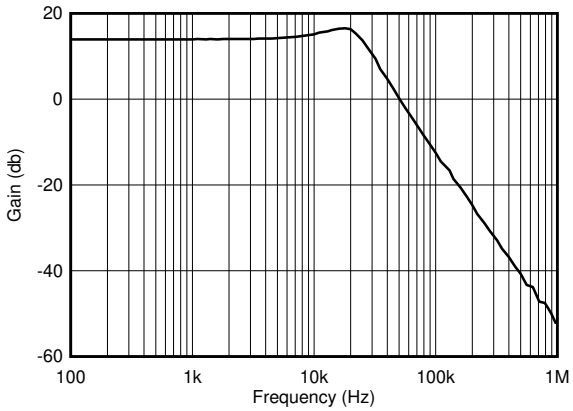


図 50. OPAx211 2nd-Order 25-kHz, Chebyshev, Low-Pass Filter

10 Power Supply Recommendations

The OPAx211 are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pick-up. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 51, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Layout Guidelines (continued)

11.1.1 SON Layout Guidelines

The OPA211 is offered in an SON-8 package (also known as SON). The SON package is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

SON packages are physically small, and have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The SON package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See the *QFN/SON PCB Attachment* application note and the *Quad Flatpack No-Lead Logic Packages* application report, both available for download at www.ti.com.

注

The exposed leadframe die pad on the bottom of the package must be connected to V–. Soldering the thermal pad improves heat dissipation and enables specified device performance.

The exposed leadframe die pad on the SON package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat sink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

11.2 Layout Example

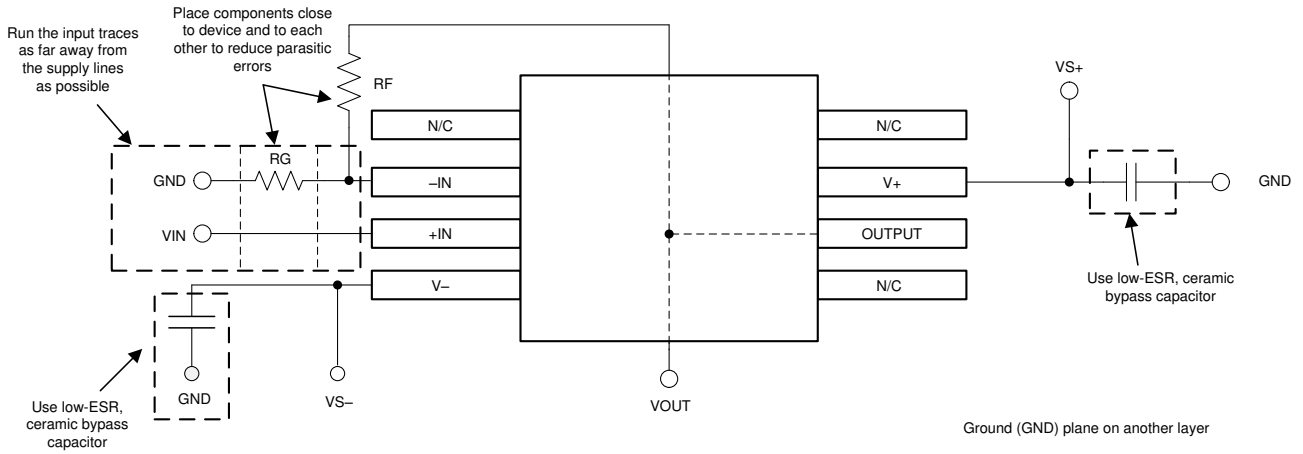


図 51. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIは無料でダウンロードでき（ WEBENCH® Design Centerから）、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

12.1.1.2 TI Precision Designs

OPAx211はいくつかのTI Precision Designsに使用されており、これらは http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

12.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、完全な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『回路基板のレイアウト技法』*
- テキサス・インスツルメンツ、*『誰でも使えるオペアンプ』*
- テキサス・インスツルメンツ、*『OPA211 EMI Immunity Performance』(英語)*
- テキサス・インスツルメンツ、*『Operational amplifier gain stability, Part 3: AC gain-error analysis』* (英語)
- テキサス・インスツルメンツ、*『Operational amplifier gain stability, Part 2: DC gain-error analysis』* (英語)
- テキサス・インスツルメンツ、*『Using infinite-gain, MFB filter topology in fully differential active filters』* (英語)
- テキサス・インスツルメンツ、*『OP AMP PERFORMANCE ANALYSIS』* (英語)
- テキサス・インスツルメンツ、*『SINGLE-SUPPLY OPERATION OF OPERATIONAL AMPLIFIERS』* (英語)
- テキサス・インスツルメンツ、*『TUNING IN AMPLIFIERS』* (英語)
- テキサス・インスツルメンツ、*『Shelf-Life Evaluation of Lead-Free Component Finishes』* (英語)

12.3 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA211	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2211	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comで、お使いのデバイスの製品フォルダを開いてください。右上の「アラートを受け取る」ボタンをクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 商標

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WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA211AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A
OPA211AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A
OPA211AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A
OPA211AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A
OPA211AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211 A
OPA211AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211AIDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211AIDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211
OPA211ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211
OPA211IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ
OPA211IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBCQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA211IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211
OPA211IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 211
OPA211IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA211IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBDQ
OPA2211AIDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDDARG4.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 2211 A
OPA2211AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ
OPA2211AIDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ
OPA2211AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ
OPA2211AIDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBHQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA211 :

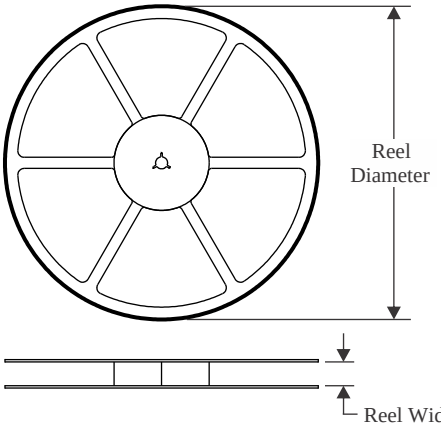
- Enhanced Product : OPA211-EP

NOTE: Qualified Version Definitions:

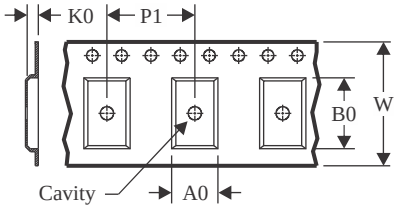
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

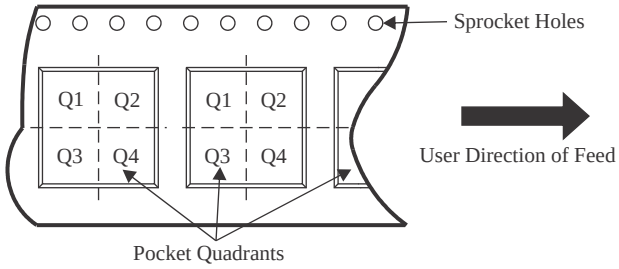


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

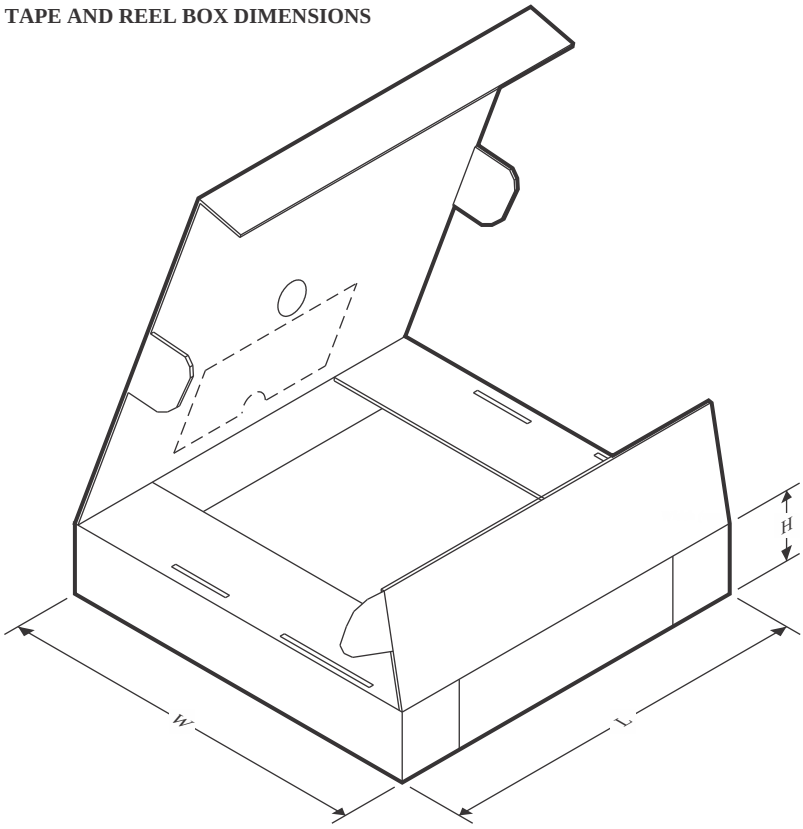
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA211IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA211IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2211AIDDARG4	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2211AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2211AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

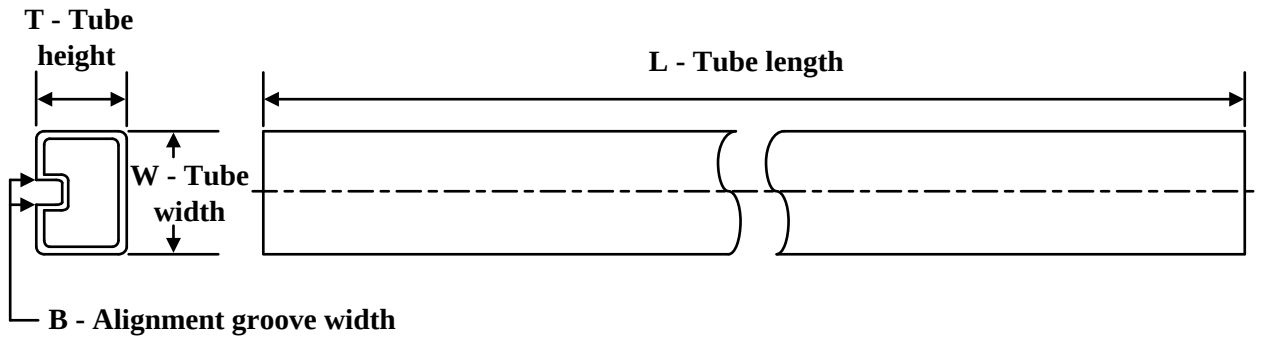
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA211AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA211AIDRGR	SON	DRG	8	3000	353.0	353.0	32.0
OPA211AIDRGT	SON	DRG	8	250	213.0	191.0	35.0
OPA211IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA211IDRGR	SON	DRG	8	3000	353.0	353.0	32.0
OPA211IDRGT	SON	DRG	8	250	213.0	191.0	35.0
OPA2211AIDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA2211AIDDARG4	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA2211AIDRGR	SON	DRG	8	3000	353.0	353.0	32.0
OPA2211AIDRGT	SON	DRG	8	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

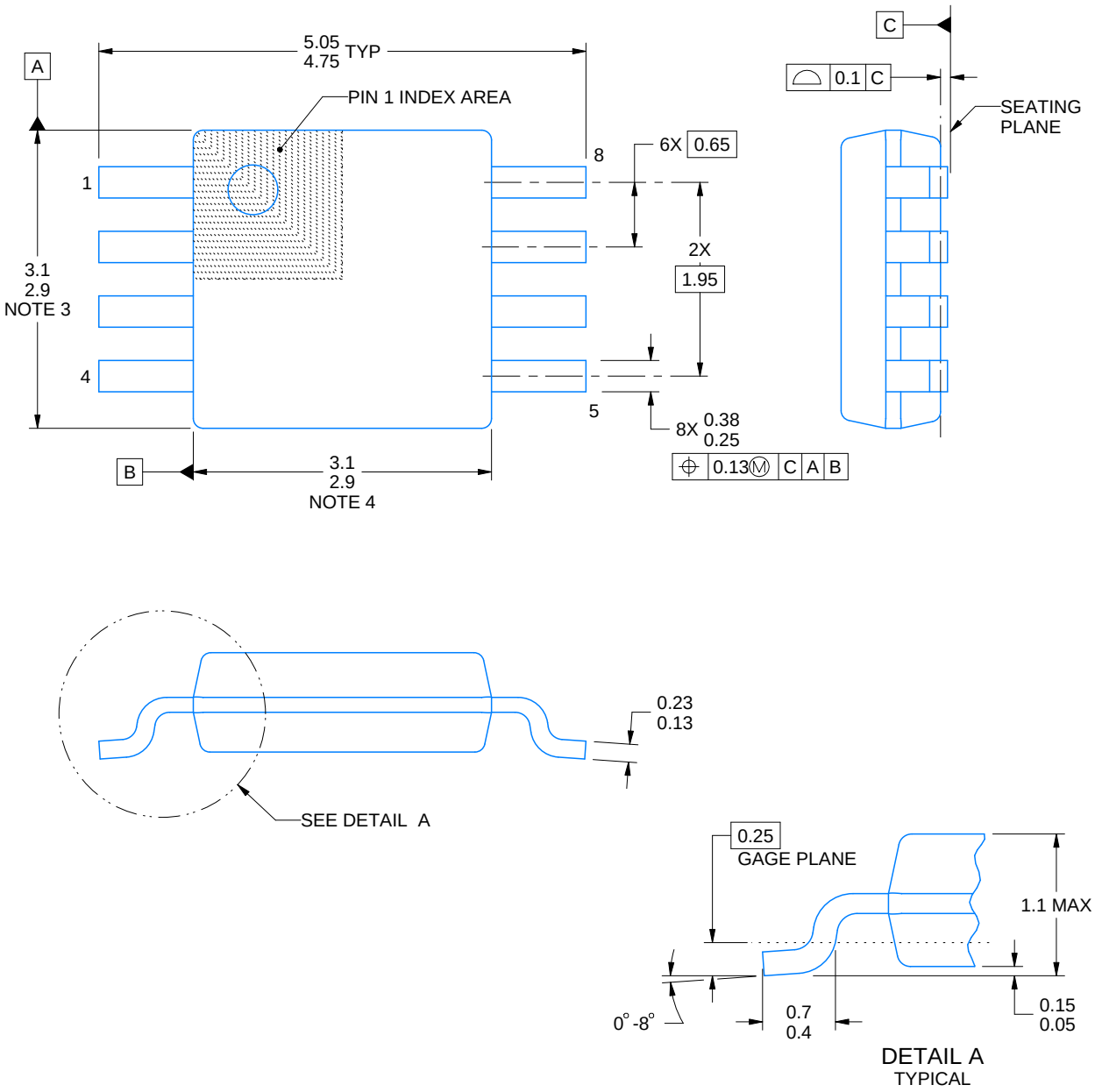
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA211AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA211AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA211AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA211ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA211ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2211AIDDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA2211AIDDA.B	DDA	HSOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

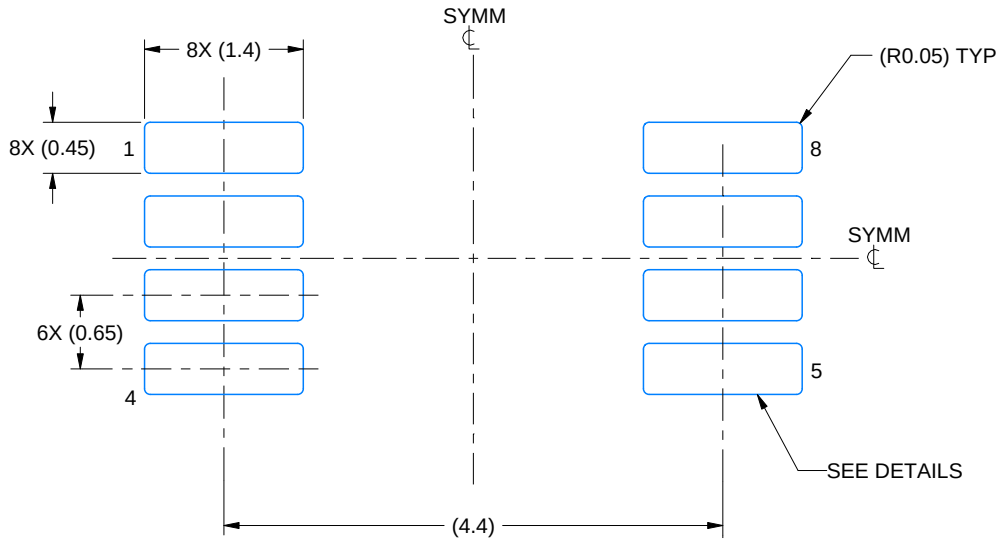
SMALL OUTLINE PACKAGE



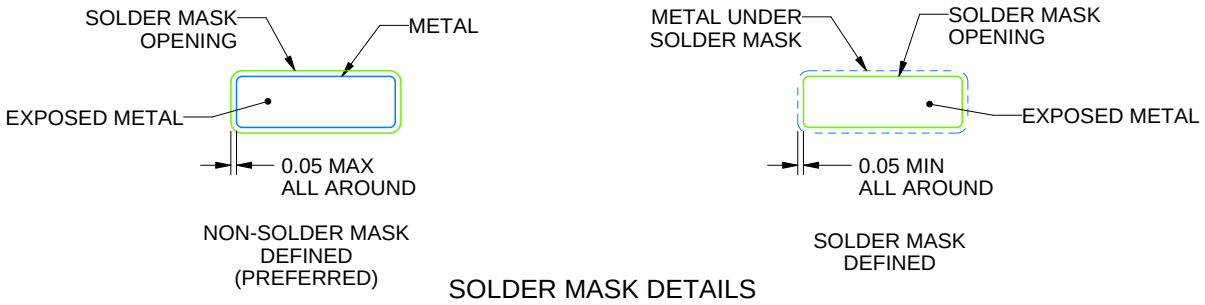
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

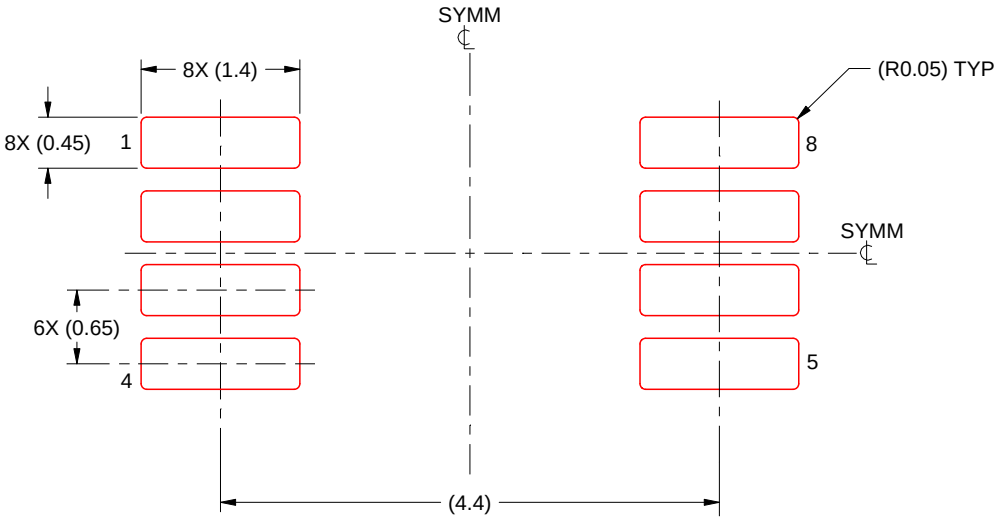


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

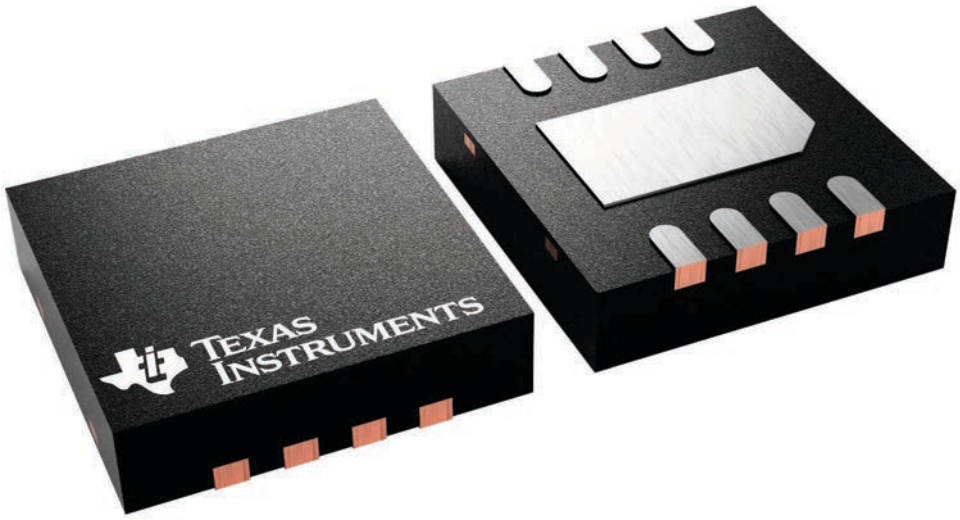
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



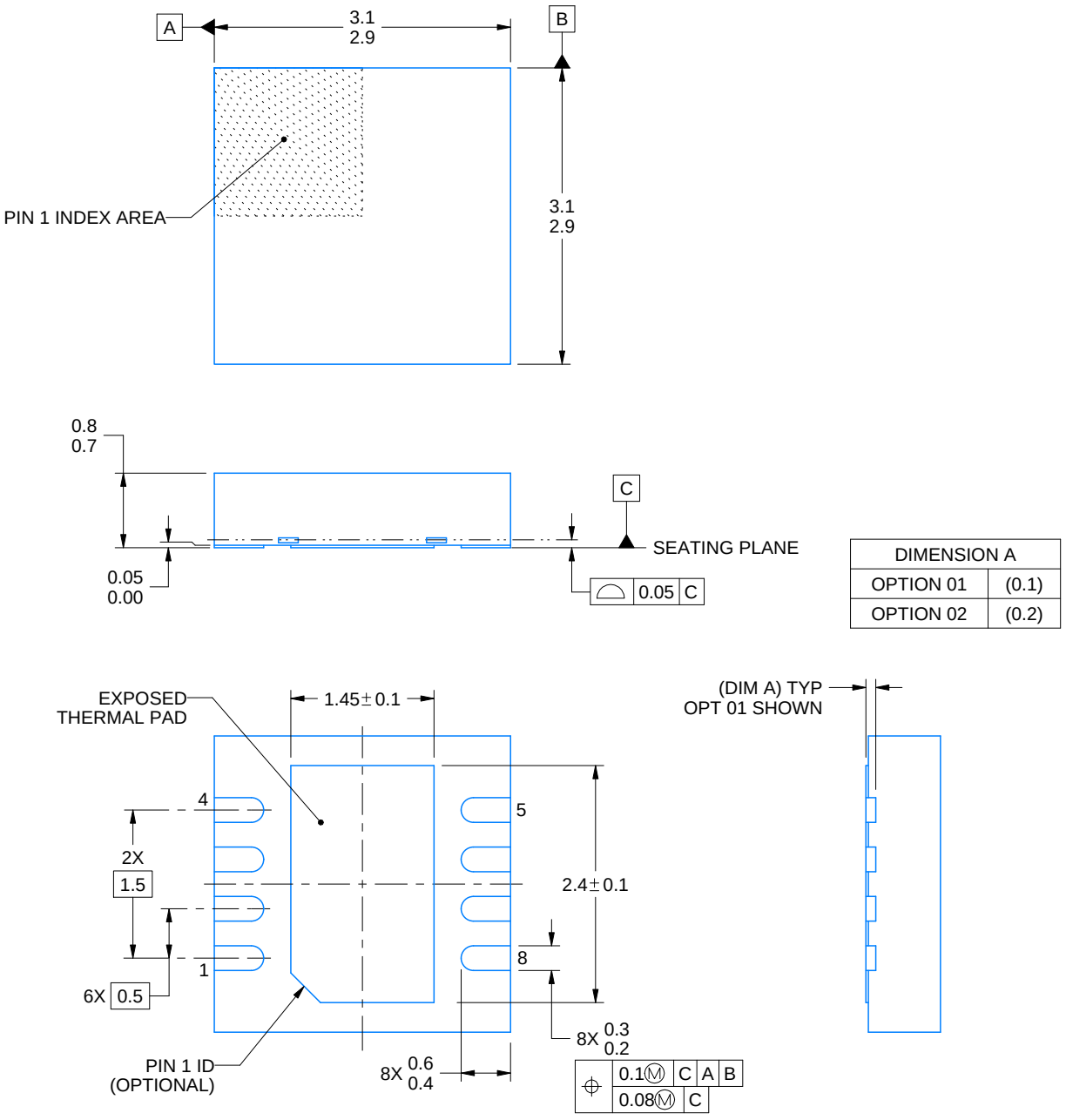
4225794/A

DRG0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

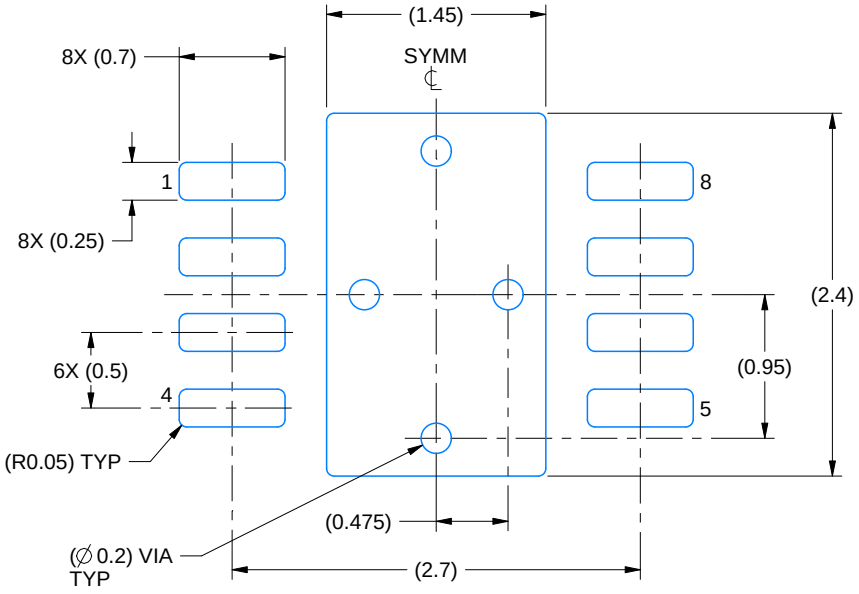


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

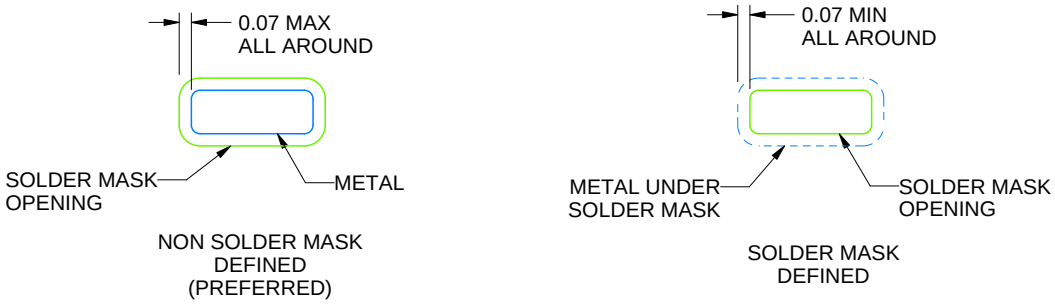
4218886/A 01/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

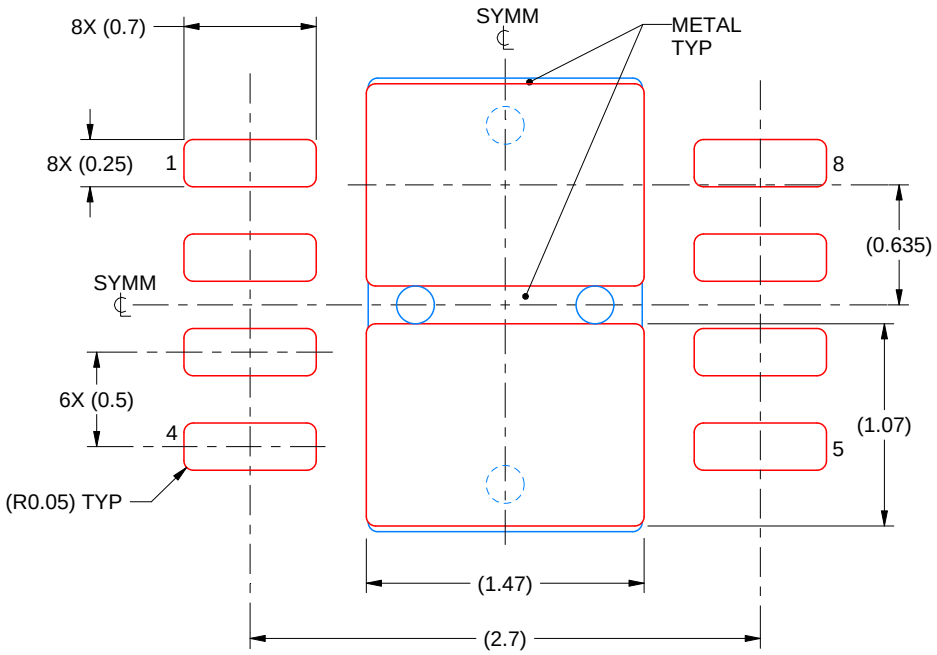


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

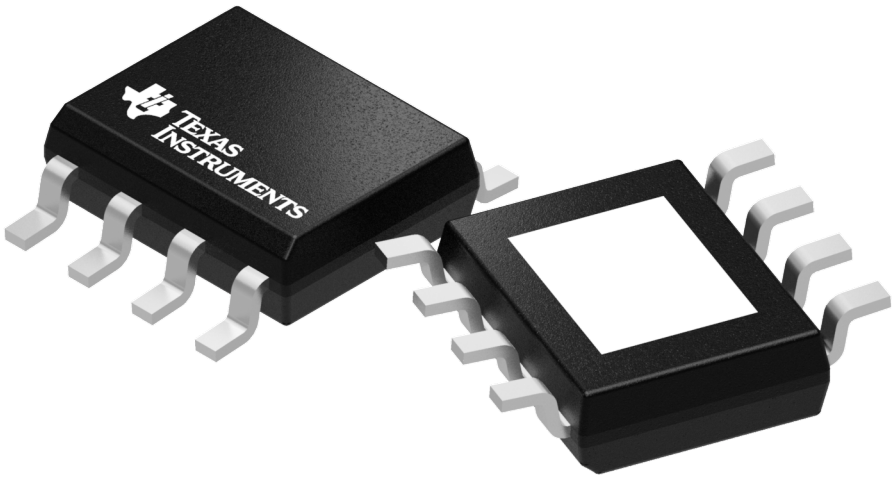
4218886/A 01/2020

NOTES: (continued)

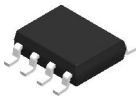
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

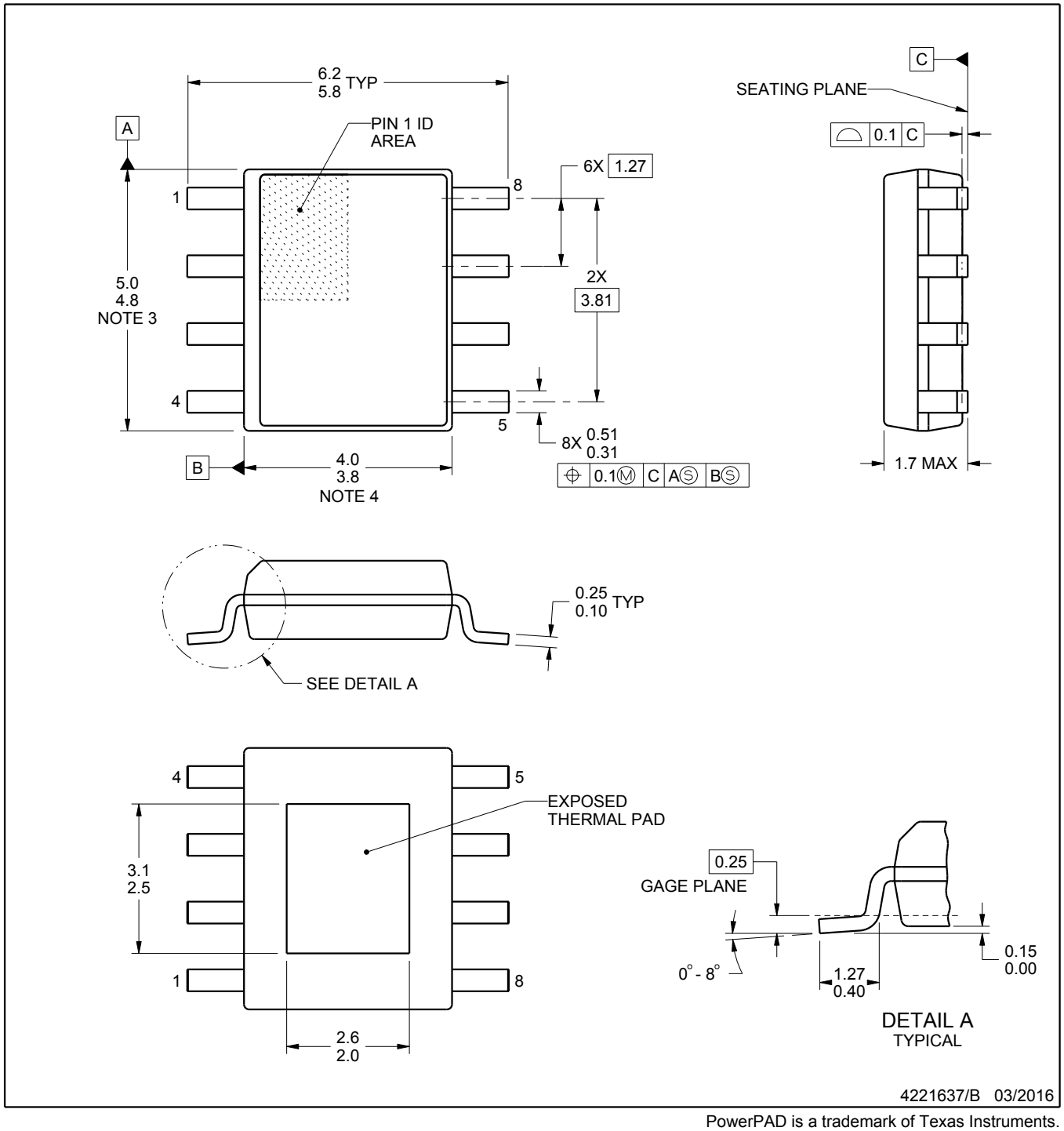


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

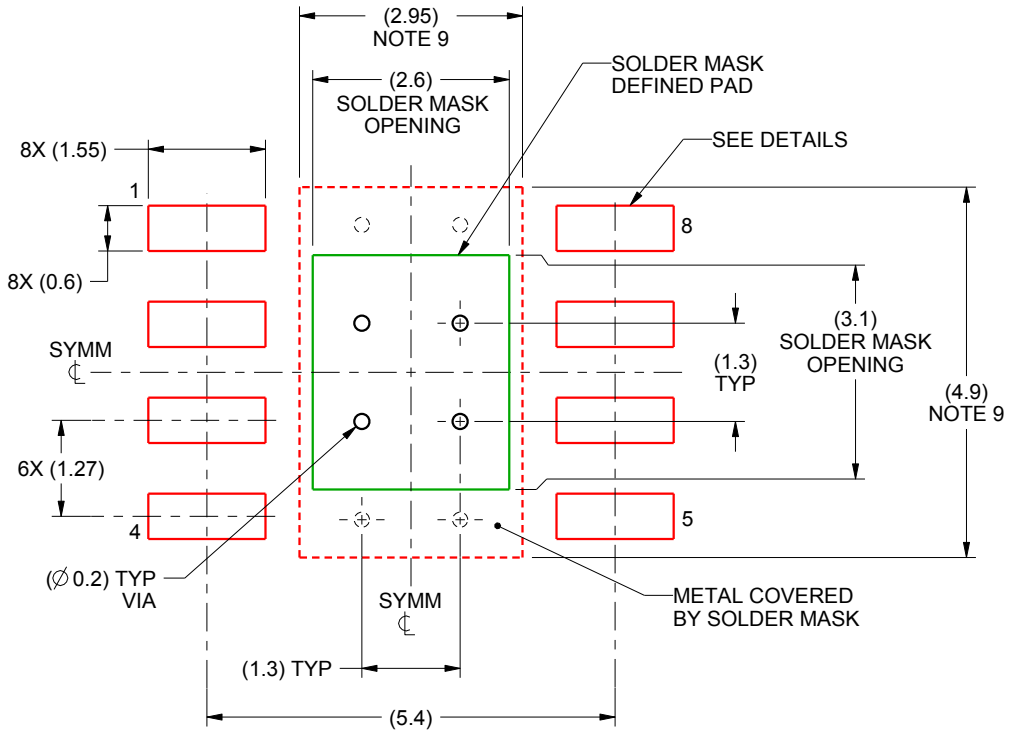
PLASTIC SMALL OUTLINE



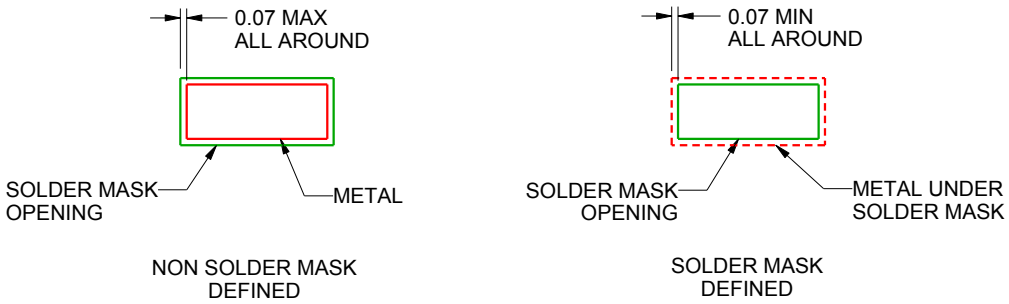
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

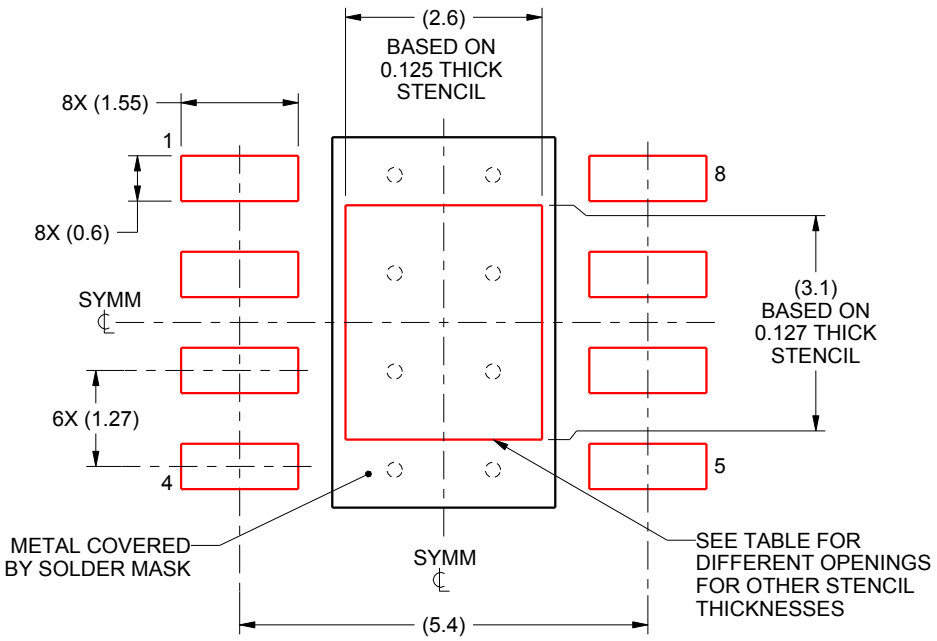


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



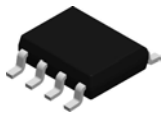
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

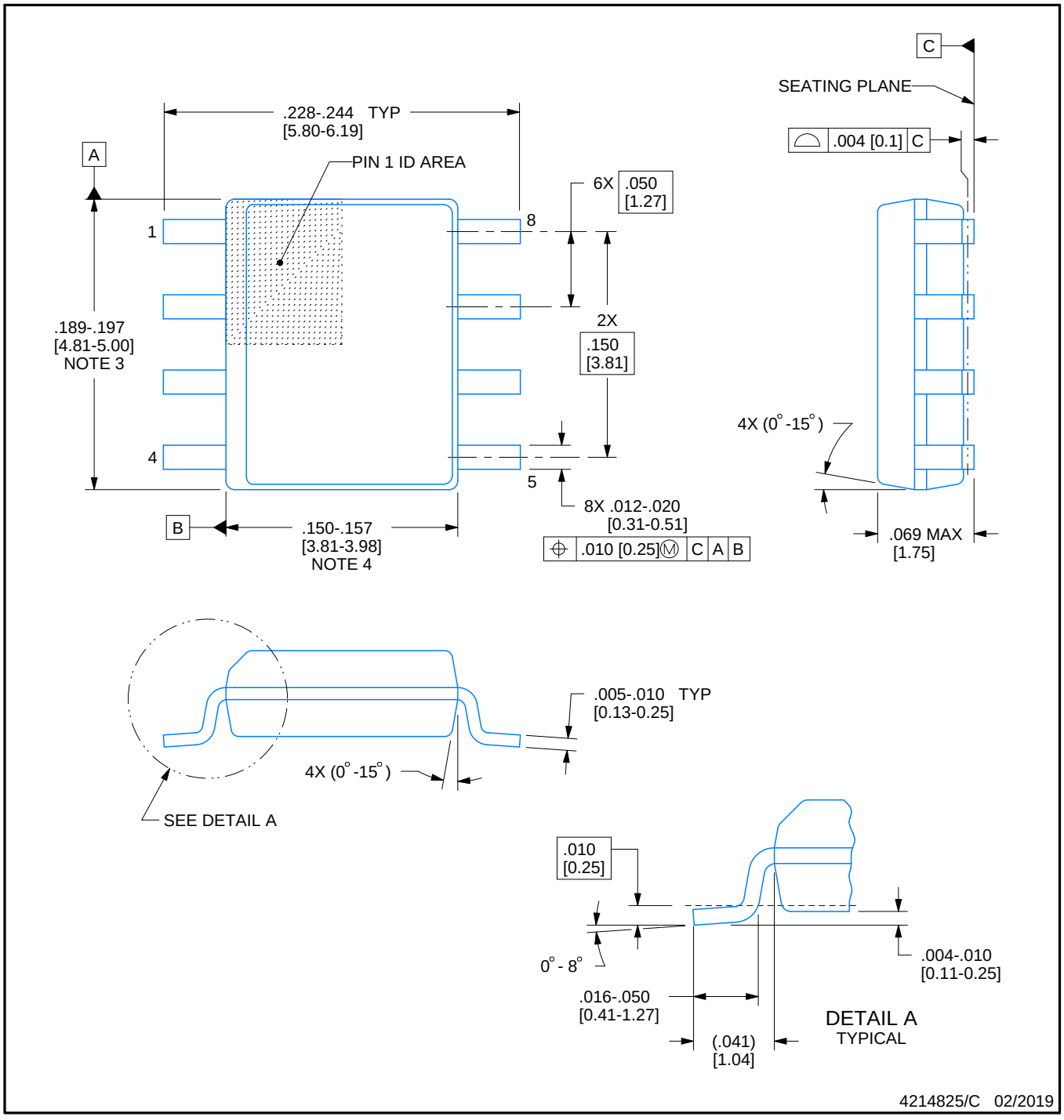


PACKAGE OUTLINE

D0008A

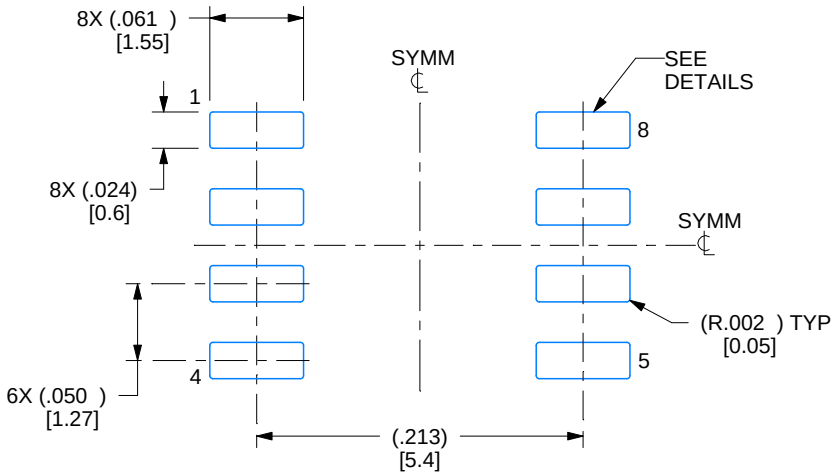
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

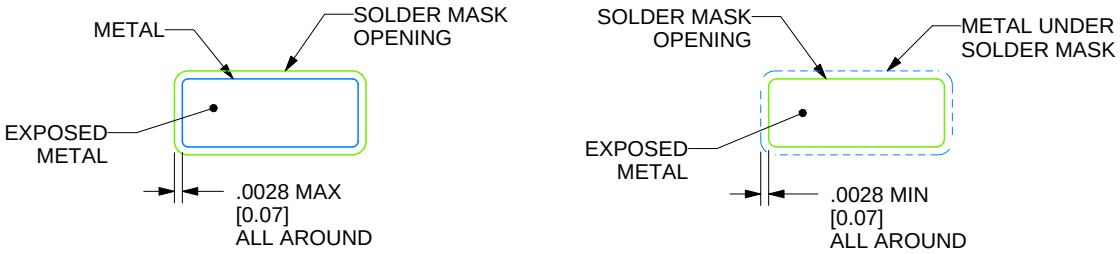


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

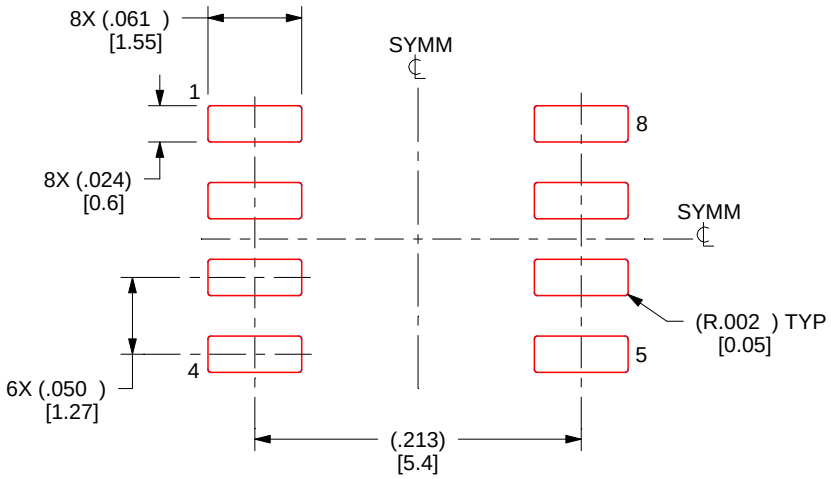
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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