OPA2188 0.03-µV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers

1 Features

- Low Offset Voltage: 25 µV (Maximum)
- Zerø-Drift: 0.03 µV/°C
- Low Noise: 8.8 nV/√Hz
  0.1-Hz to 10-Hz Noise: 0.25 μV_{PP}
- Excellent DC Precision:
  PSRR: 142 dB
  CMRR: 146 dB
  Open-Loop Gain: 136 dB
- Gain Bandwidth: 2 MHz
- Quiescent Current: 475 µA (Maximum)
- Wide Supply Range: ±2 V to ±18 V
- Rail-to-Rail Output:
  Input Includes Negative Rail
- RFI Filtered Inputs
- *Micro*SIZE Packages

2 Applications

- Bridge Amplifiers
- Strain Gauges
- Test Equipment
- Transducer Applications
- Temperature Measurement
- Electronic Scales
- Medical Instrumentation
- Resistance Temperature Detectors
- Precision Active Filters

3 Description

The OPA2188 operational amplifier uses TI proprietary auto-zeroing techniques to provide low offset voltage (25 µV, maximum), and near zero-drift over time and temperature. This miniature, high-precision, low quiescent current amplifier offers high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4 V to 36 V (±2 V to ±18 V).

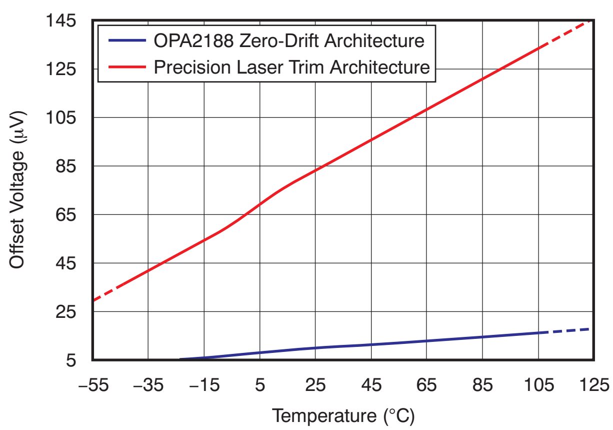
The OPA2188 device is available in MSOP-8 and SO-8 packages. The device is specified for operation from –40°C to +105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2188	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Offset Voltage vs Temperature



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2012) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Input Bias Current, I_B and I_{OS} parameters overtemperature maximum specification in *Electrical Characteristics: High-Voltage Operation* table ... 5
- Changed Noise, *Input voltage noise density* parameter units in *Electrical Characteristics: High-Voltage Operation* table ... 5
- Changed Power Supply, I_Q parameter maximum specifications in *Electrical Characteristics: High-Voltage Operation* table ... 6
- Changed Input Bias Current, I_B and I_{OS} parameters overtemperature maximum specification in *Electrical Characteristics: Low-Voltage Operation* table ... 7
- Changed Noise, *Input voltage noise density* parameter units in *Electrical Characteristics: Low-Voltage Operation* table ... 7
- Changed Power Supply, I_Q parameter maximum specifications in *Electrical Characteristics: Low-Voltage Operation* table ... 8

Changes from Revision A (June 2012) to Revision B — **Page**

- Changed second to last Applications bullet ... 1

Changes from Original (August 2011) to Revision A — **Page**

- Deleted all references to OPA188 and OPA4188 throughout document ... 1
- Updated document to current standards ... 1
- Changed document status to *Production Data* ... 1

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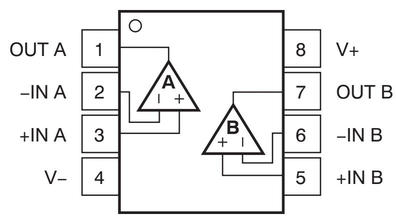
5 Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (µV)	OFFSET VOLTAGE DRIFT (µV/°C)	BANDWIDTH (MHz)
Single	OPA188 (4 V to 36 V)	25	0.085	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4330 (5 V)	50	0.25	0.35

6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and MSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Negative (inverting) input signal, channel A
–IN B	6	I	Negative (inverting) input signal, channel B
+IN A	3	I	Positive (noninverting) input signal, channel A
+IN B	5	I	Positive (noninverting) input signal, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		±20, 40 (single supply)	V
	Signal input terminals, voltage(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input terminals, current(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	4 (±2)		36 (±18)	V
T_A	Specified temperature range	-40		+105	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA2188ID	OPA2188IDGK	UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111	159.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.9	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	48.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	77.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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7.5 Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	μV
		T_A = –40°C to +105°C		0.03	0.085	μV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	μV/V
		V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to +105°C			0.3	μV/V
	Long-term stability			4 (1)		μV
	Channel separation, DC			1		μV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±850	pA
		T_A = –40°C to +105°C			±18	nA
I_{OS}	Input offset current			±320	±1700	pA
		T_A = –40°C to +105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		$μV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density	f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V, T_A = –40°C to +105°C	120	126		dB
INPUT IMPEDANCE						
	Differential			100 || 6		MΩ || pF
	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	130	136		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to +105°C	120	126		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/μs
	Settling time, 0.1%	V_S = ±18 V, G = 1, 10-V step		20		μs
	Settling time, 0.01%	V_S = ±18 V, G = 1, 10-V step		27		μs
	Overload recovery time	V_{IN} × G = V_S		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 μV.

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Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to +105°C		310	350	mV
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage			4 to 36 (±2 to ±18)		V
I_Q	Quiescent current (per amplifier)	V_S = ±4 V to V_S = ±18 V		415	510	µA
		I_O = 0 mA, T_A = –40°C to +105°C			600	µA

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7.6 Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	µV
		T_A = –40°C to +105°C		0.03	0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	µV/V
		V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to +105°C			0.3	µV/V
	Long-term stability			4 (1)		µV
	Channel separation, dc			1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±850	pA
		T_A = –40°C to +105°C			±18	nA
I_{OS}	Input offset current			±320	±1700	pA
		T_A = –40°C to +105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		$µV_{PP}$
	Input voltage noise density	f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density	f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +105°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V, T_A = –40°C to +105°C	110	120		dB
INPUT IMPEDANCE						
	Differential			100 || 6		MΩ || pF
	Common-mode			6 || 95		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 5 kΩ, V_S = 5 V	110	120		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	120	130		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to +105°C	114	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/µs
	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to +105°C		310	350	mV
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range			4 to 36 (±2 to ±18)		V
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		385	485	µA
		I_O = 0 mA, T_A = –40°C to +105°C			590	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		105	°C
T_A	Operating temperature range		–40		125	°C
T_{stg}	Storage temperature		–65		150	°C

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7.7 Typical Characteristics: Table of Graphs

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE NO.
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 10
CMRR vs Temperature	Figure 11, Figure 12
PSRR vs Temperature	Figure 13
0.1-Hz to 10-Hz Noise	Figure 14
Input Voltage Noise Spectral Density vs Frequency	Figure 15
THD+N Ratio vs Frequency	Figure 16
THD+N vs Output Amplitude	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Quiescent Current vs Temperature	Figure 19
Open-Loop Gain and Phase vs Frequency	Figure 20
Closed-Loop Gain vs Frequency	Figure 21
Open-Loop Gain vs Temperature	Figure 22
Open-Loop Output Impedance vs Frequency	Figure 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31, Figure 32
Large-Signal Settling Time (10-V Positive Step)	Figure 33
Large-Signal Settling Time (10-V Negative Step)	Figure 34
Short-Circuit Current vs Temperature	Figure 35
Maximum Output Voltage vs Frequency	Figure 36
Channel Separation vs Frequency	Figure 37
EMIRR IN+ vs Frequency	Figure 38

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7.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

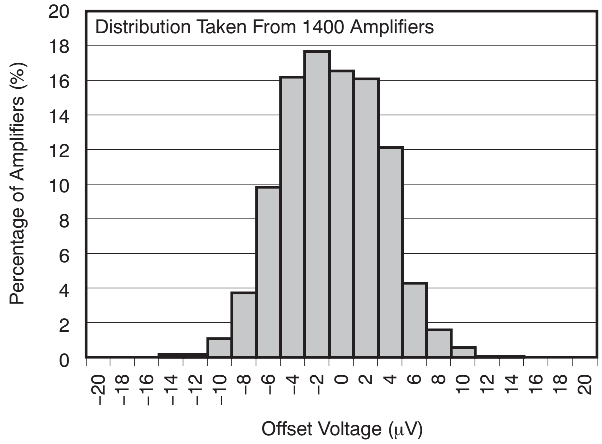

Figure 1. Offset Voltage Production Distribution

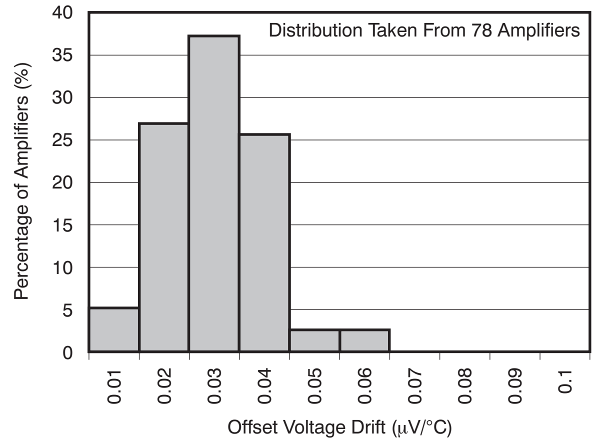

Figure 2. Offset Voltage Drift Distribution

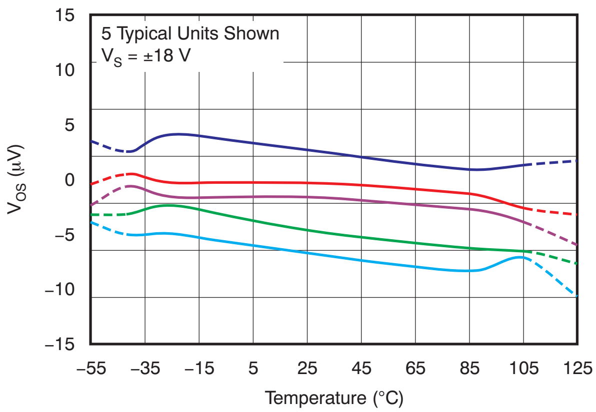

Figure 3. Offset Voltage vs Temperature

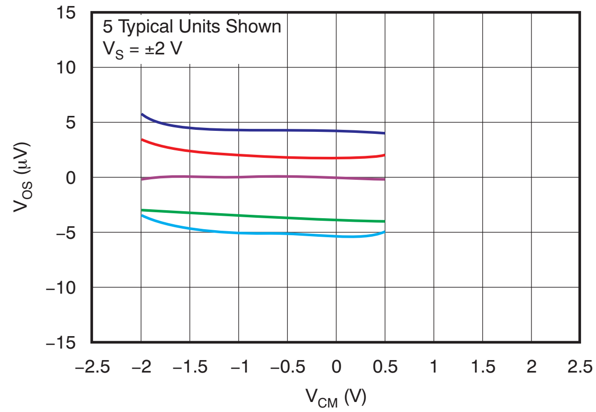

Figure 4. Offset Voltage vs Common-Mode Voltage

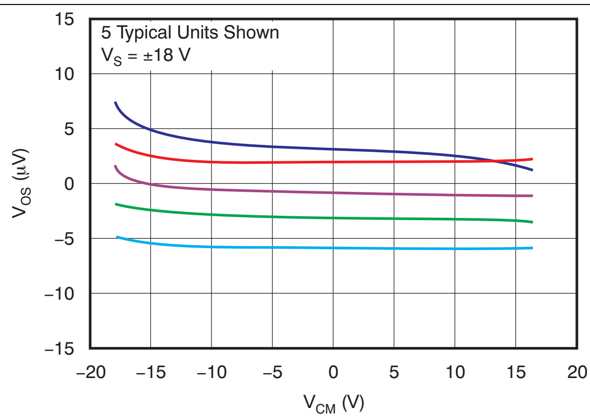

Figure 5. Offset Voltage vs Common-Mode Voltage

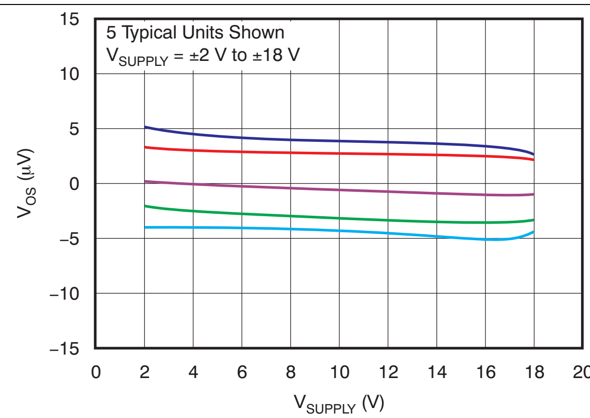

Figure 6. Offset Voltage vs Power Supply

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

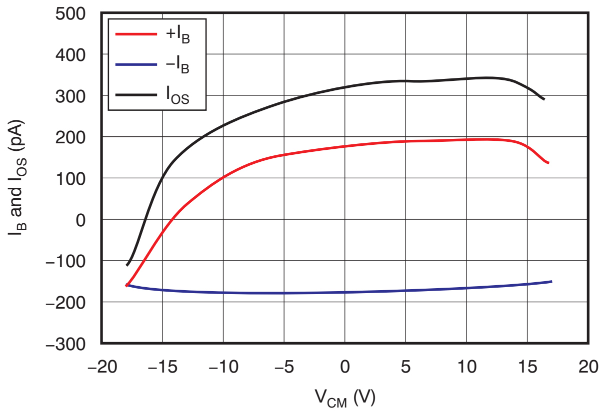

Figure 7. I_B and I_{OS} vs Common-Mode Voltage

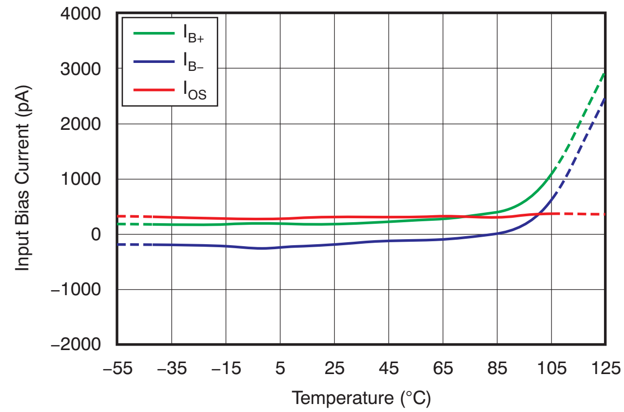

Figure 8. Input Bias Current vs Temperature

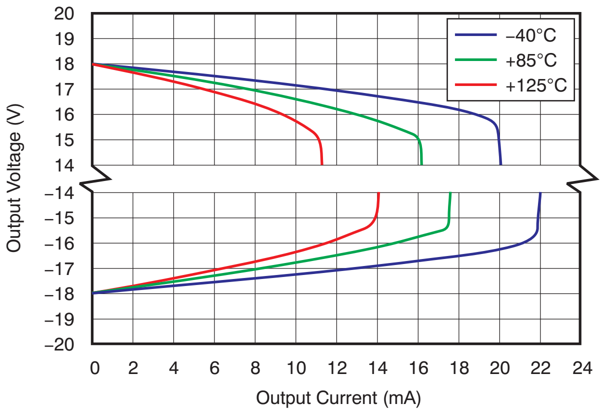

Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

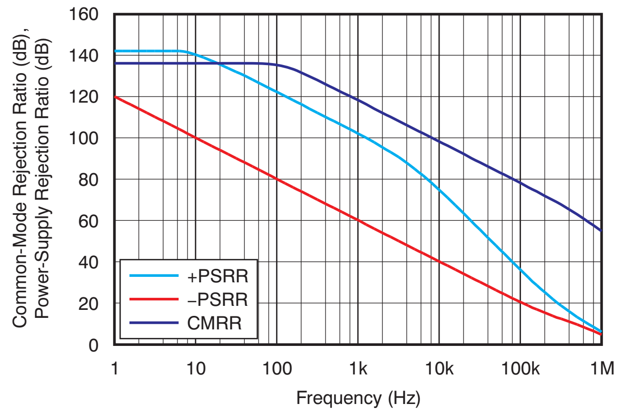

Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)

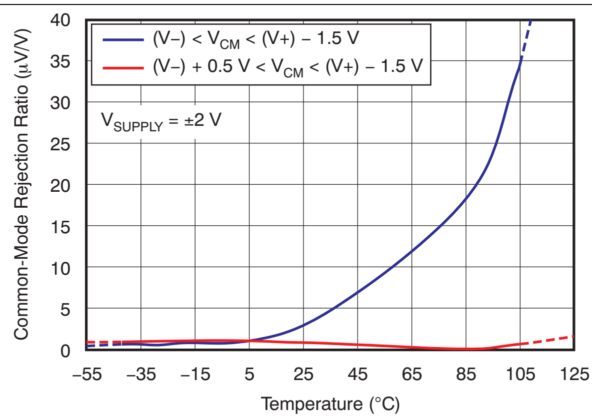

Figure 11. CMRR vs Temperature

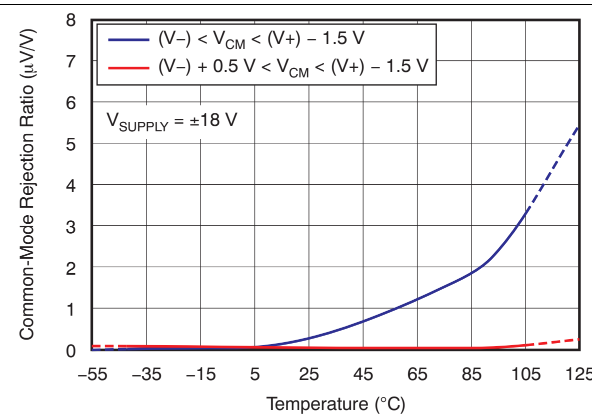

Figure 12. CMRR vs Temperature

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

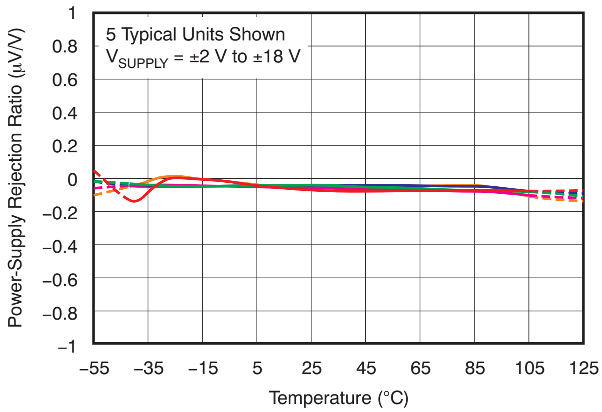

Figure 13. PSRR vs Temperature

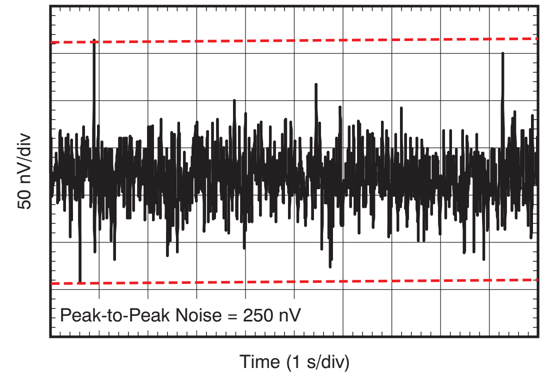

Figure 14. 0.1-Hz to 10-Hz Noise

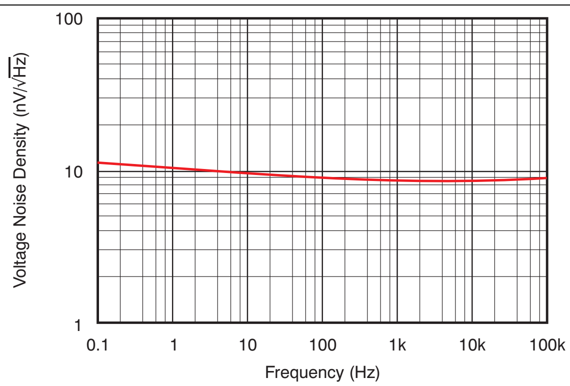

Figure 15. Input Voltage Noise Spectral Density vs Frequency

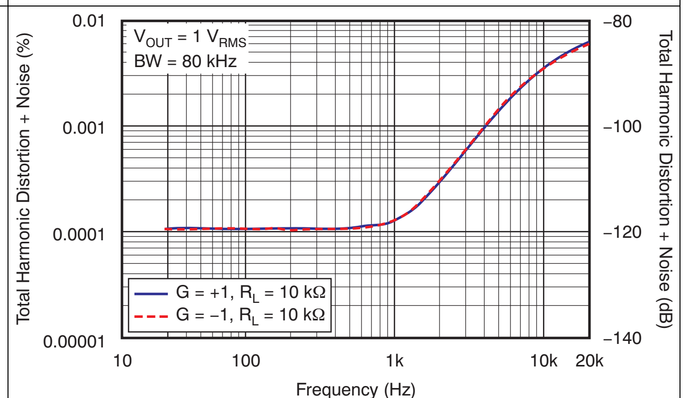

Figure 16. THD+N Ratio vs Frequency

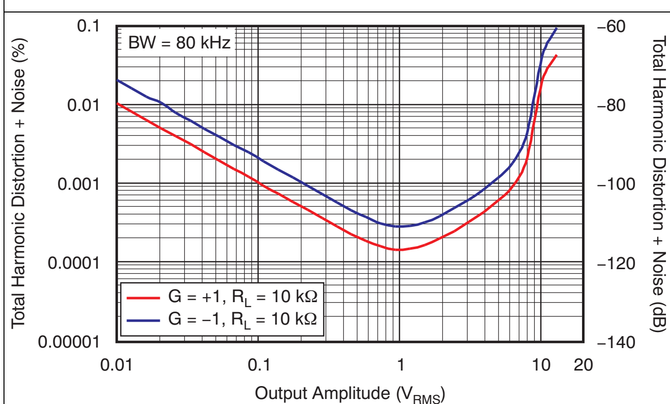

Figure 17. THD+N vs Output Amplitude

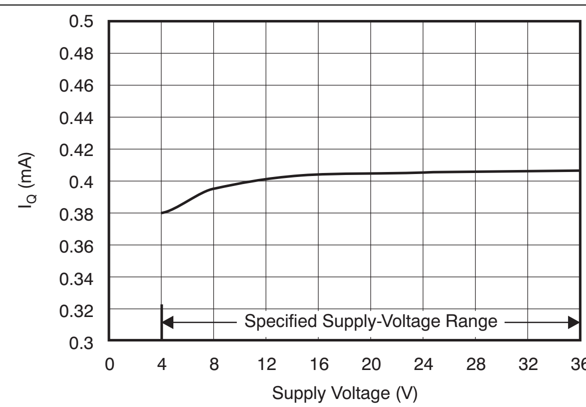

Figure 18. Quiescent Current vs Supply Voltage

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

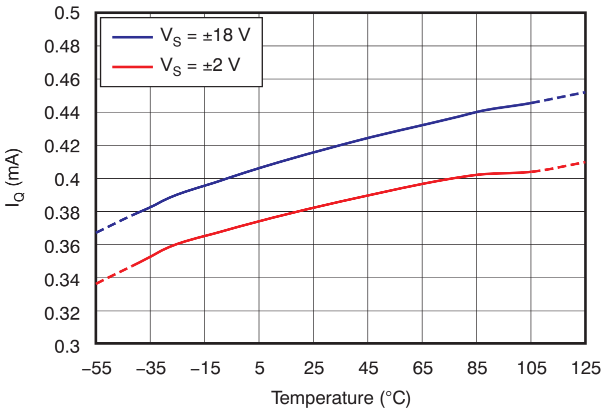

Figure 19. Quiescent Current vs Temperature

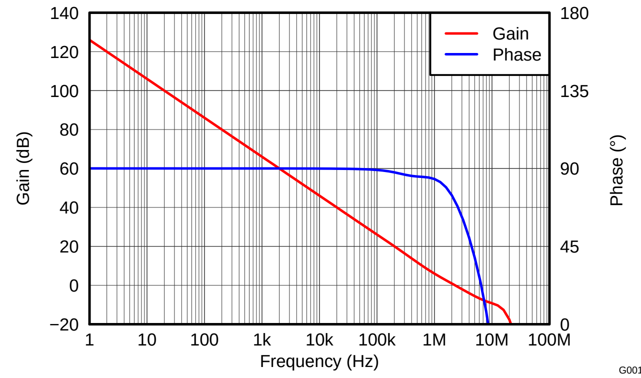

Figure 20. Open-Loop Gain and Phase vs Frequency

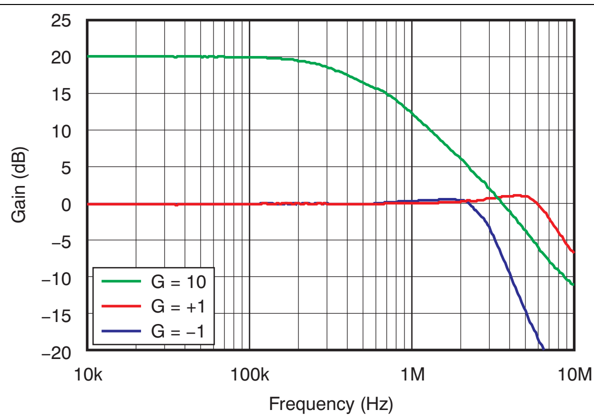

Figure 21. Closed-Loop Gain vs Frequency

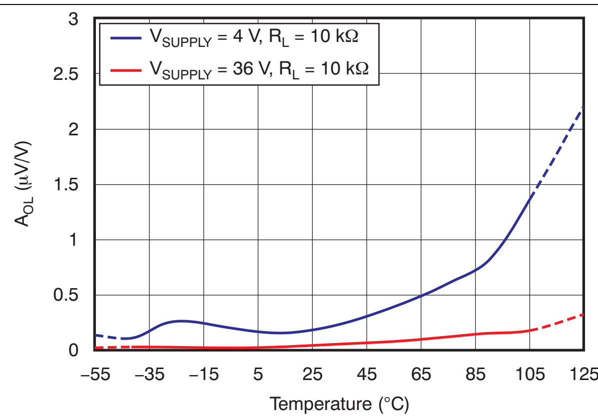

Figure 22. Open-Loop Gain vs Temperature

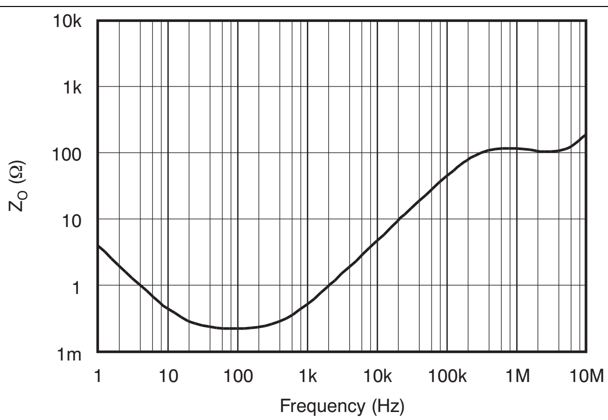

Figure 23. Open-Loop Output Impedance vs Frequency

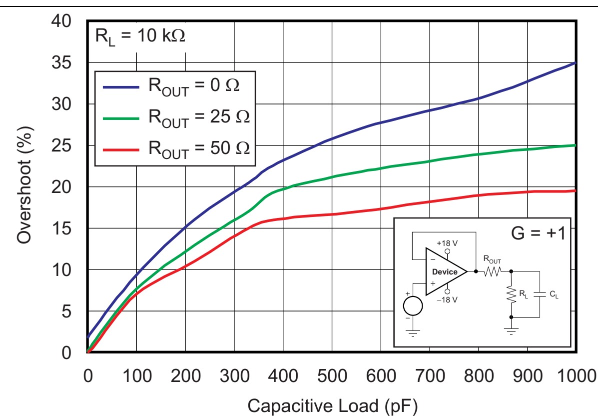

Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

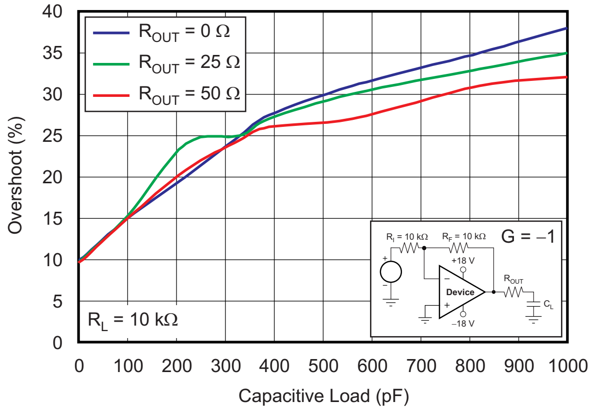

Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

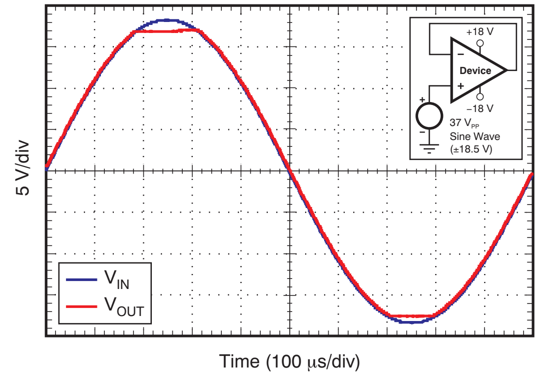

Figure 26. No Phase Reversal

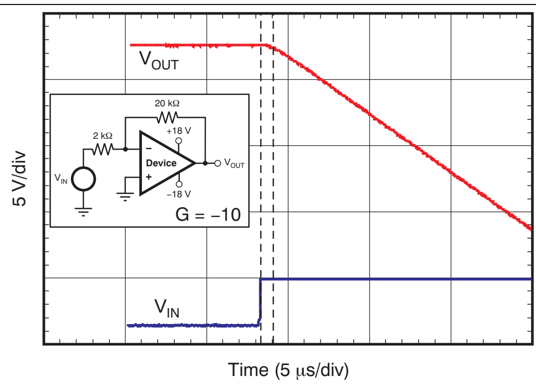

Figure 27. Positive Overload Recovery

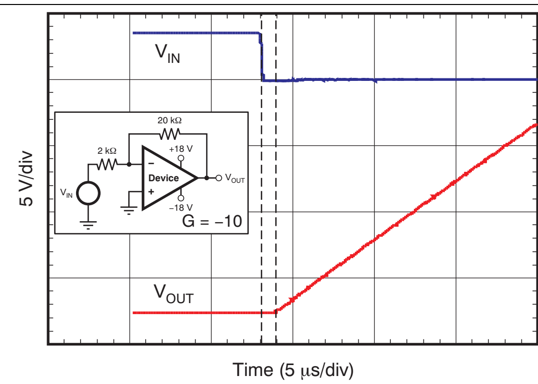

Figure 28. Negative Overload Recovery

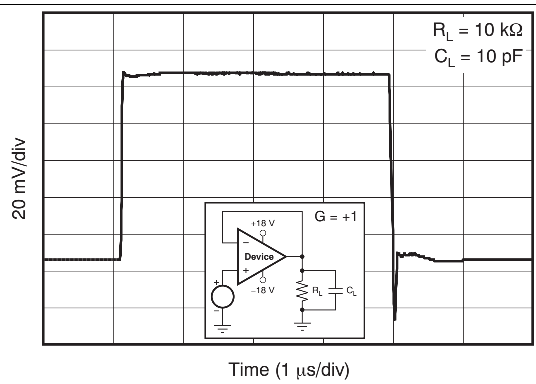

Figure 29. Small-Signal Step Response (100 mV)

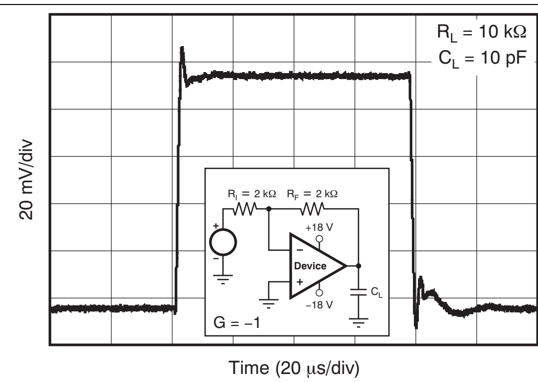

Figure 30. Small-Signal Step Response (100 mV)

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

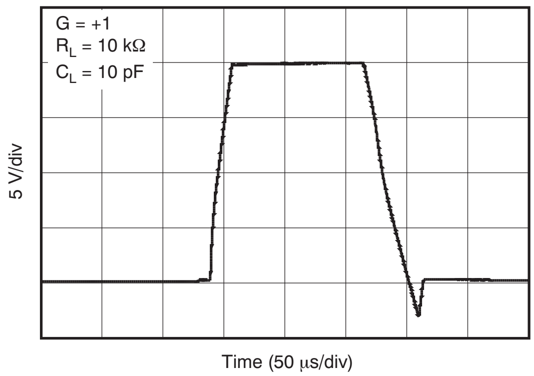

Figure 31. Large-Signal Step Response

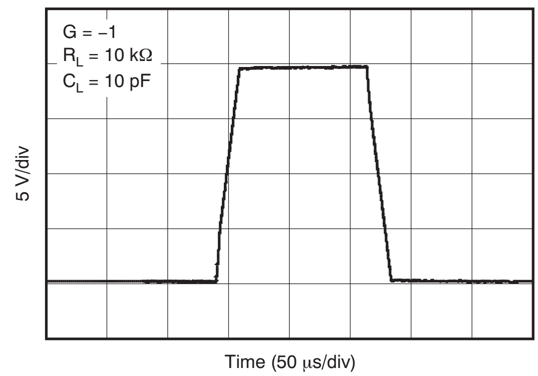

Figure 32. Large-Signal Step Response

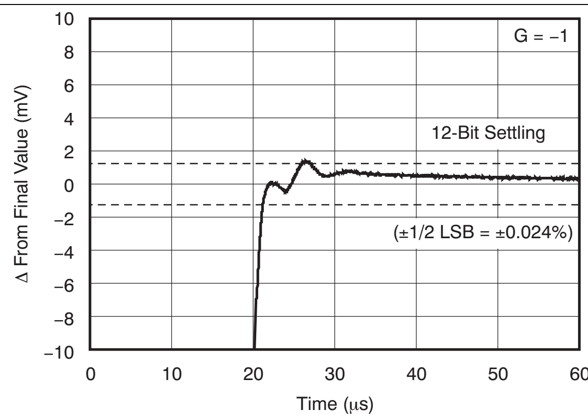

Figure 33. Large-Signal Settling Time (10-V Positive Step)

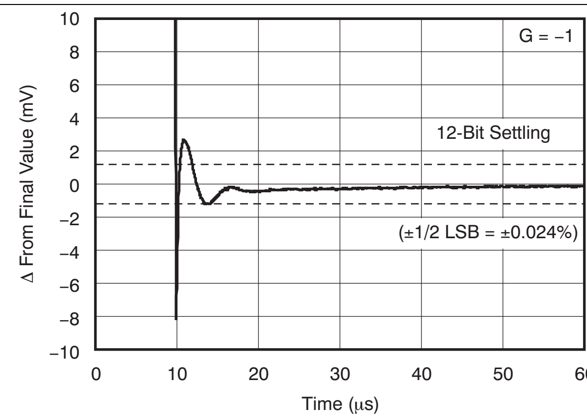

Figure 34. Large-Signal Settling Time (10-V Negative Step)

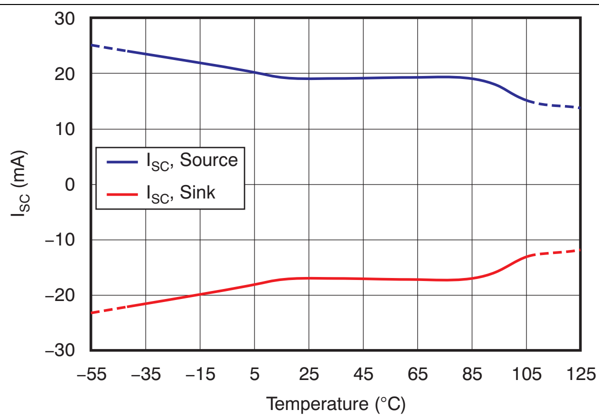

Figure 35. Short-Circuit Current vs Temperature

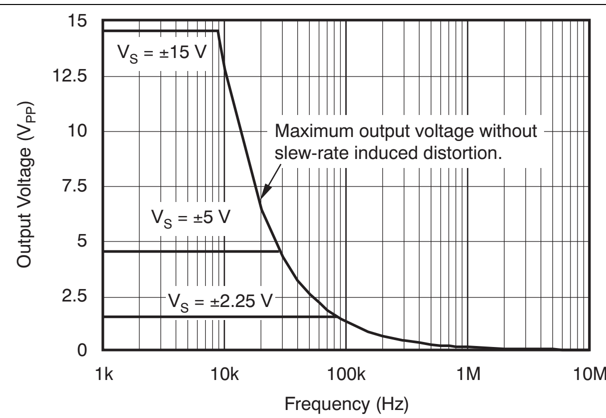

Figure 36. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

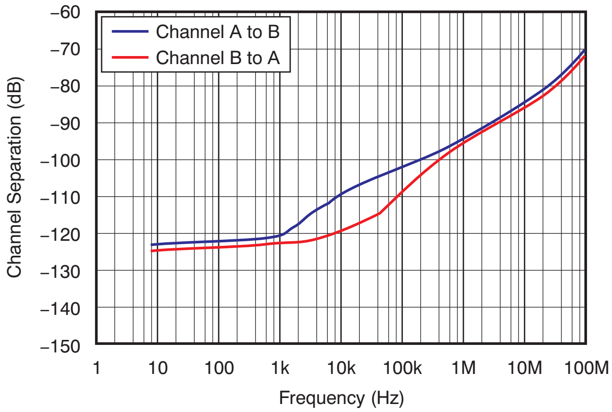

Figure 37. Channel Separation vs Frequency

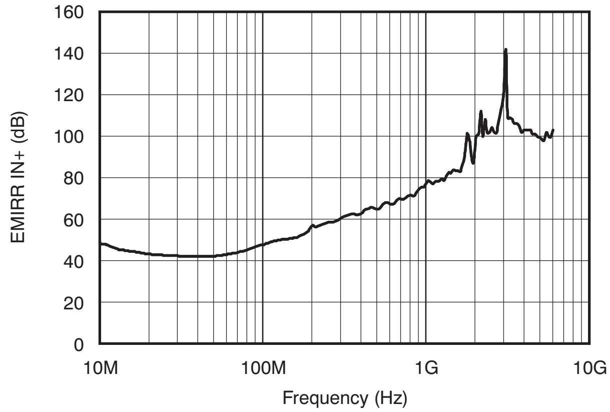

Figure 38. EMIRR IN+ vs Frequency

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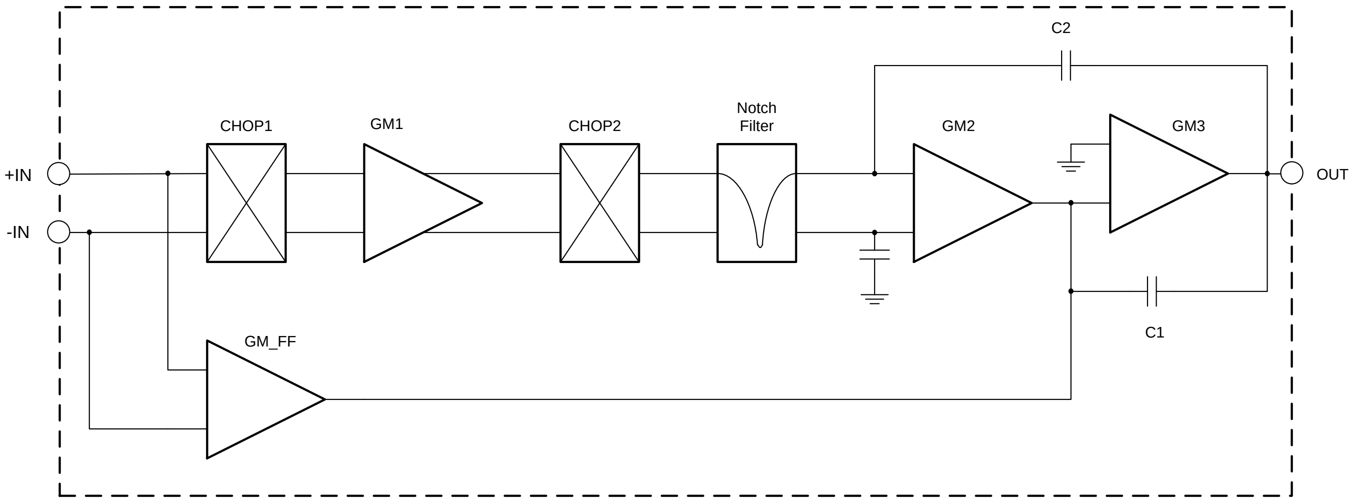
8 Detailed Description

8.1 Overview

The OPA2188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The OPA2188 is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.3.2 EMI Rejection

The OPA2188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 39 shows the results of this testing on the OPA2188. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from the TI website.

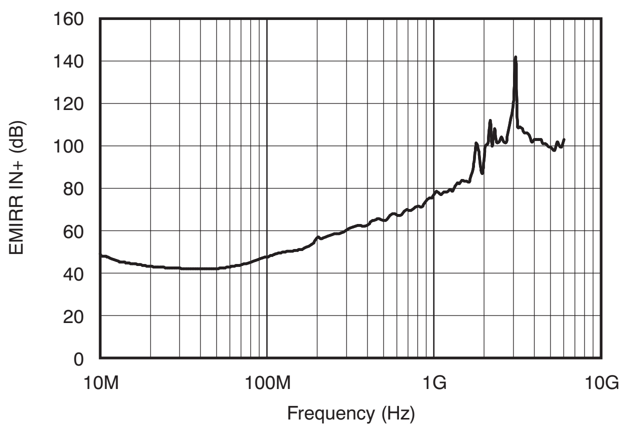


Figure 39. EMIRR Testing

8.3.3 Phase-Reversal Protection

The OPA2188 device has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA2188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 40.

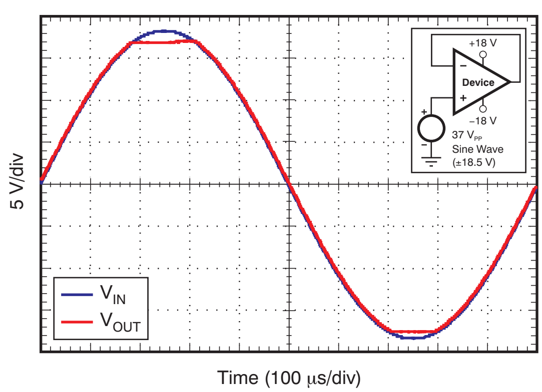


Figure 40. No Phase Reversal

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Feature Description (continued)

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPA2188 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to the applications report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

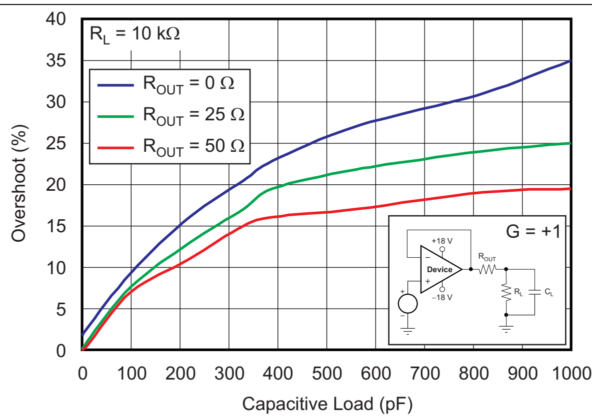

Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

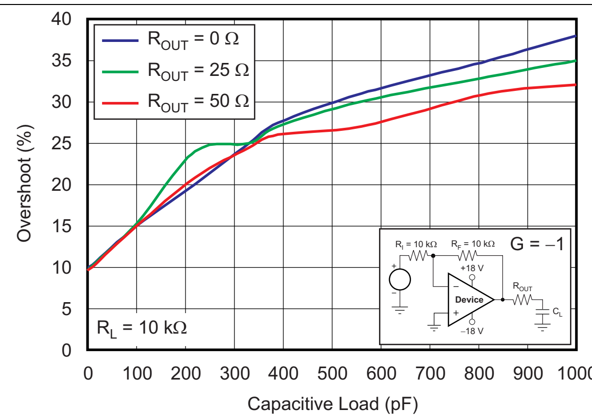

Figure 42. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 43 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

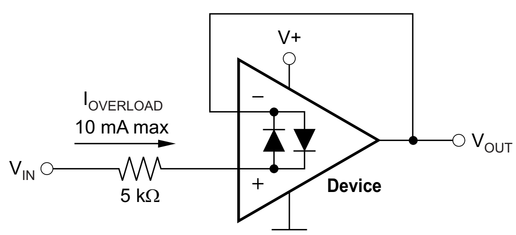

Figure 43. Input Current Protection

Feature Description (continued)

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.4 Device Functional Modes

The OPA2188 device has a single functional mode. The device is powered on as long as the power supply voltage is between 4 V (±2 V) and 36 V (±18 V).

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 44 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 45 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2188 facilitate excellent dc accuracy for the circuit.

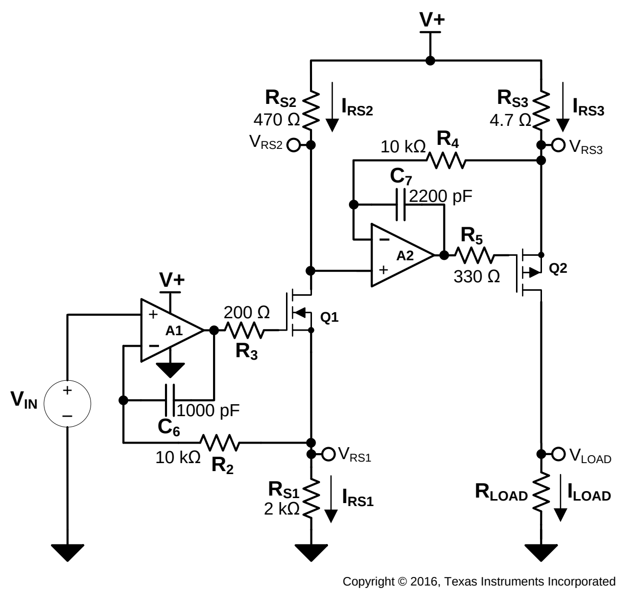

Figure 44. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2188 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 15 mV of the positive rail. The OPA2188 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2188 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in TIPD102.

9.2.1.3 Application Curve

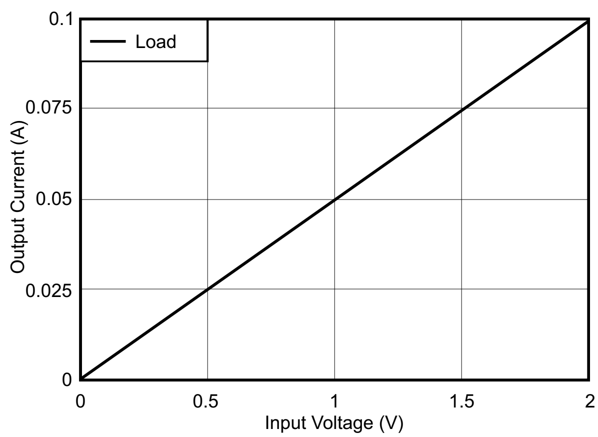

Figure 45. Measured Transfer Function for High-Side V-I Converter

9.3 System Examples

9.3.1 Discrete INA + Attenuation for ADC With 3.3-V Supply

The application examples of Figure 46 and Figure 47 highlight only a few of the circuits where the OPA2188 can be used.

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System Examples (continued)

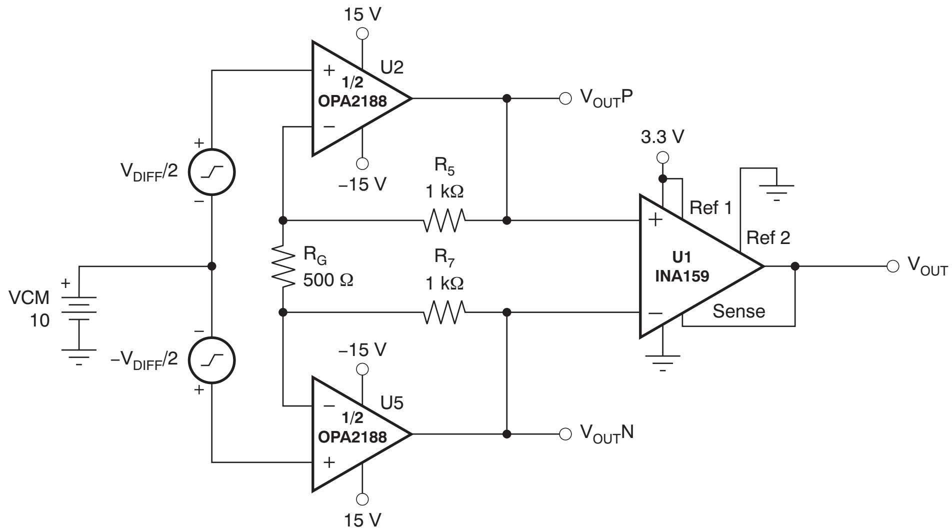
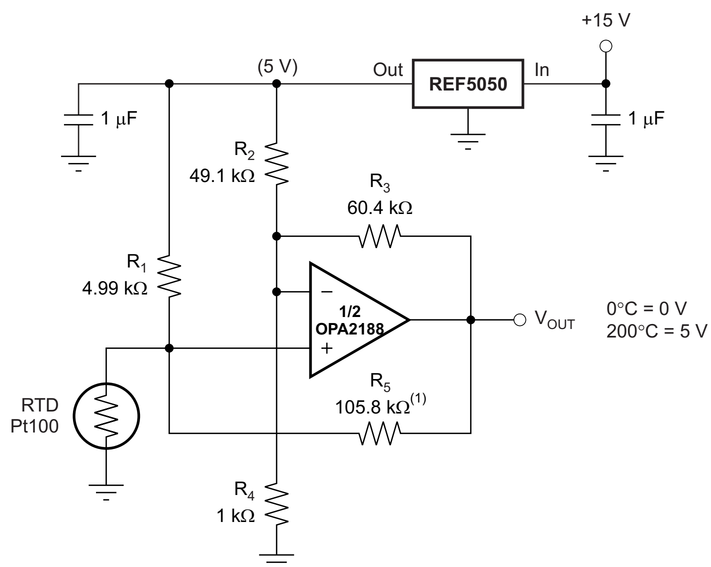


Figure 46. Discrete INA + Attenuation for ADC with 3.3-V Supply

9.3.2 RTD Amplifier with Linearization



(1) R_5 provides positive-varying excitation to linearize output.

Figure 47. RTD Amplifier with Linearization

10 Power Supply Recommendations

The OPA2188 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 105°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

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CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

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11 Layout

11.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA2188 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

11.2 Layout Example

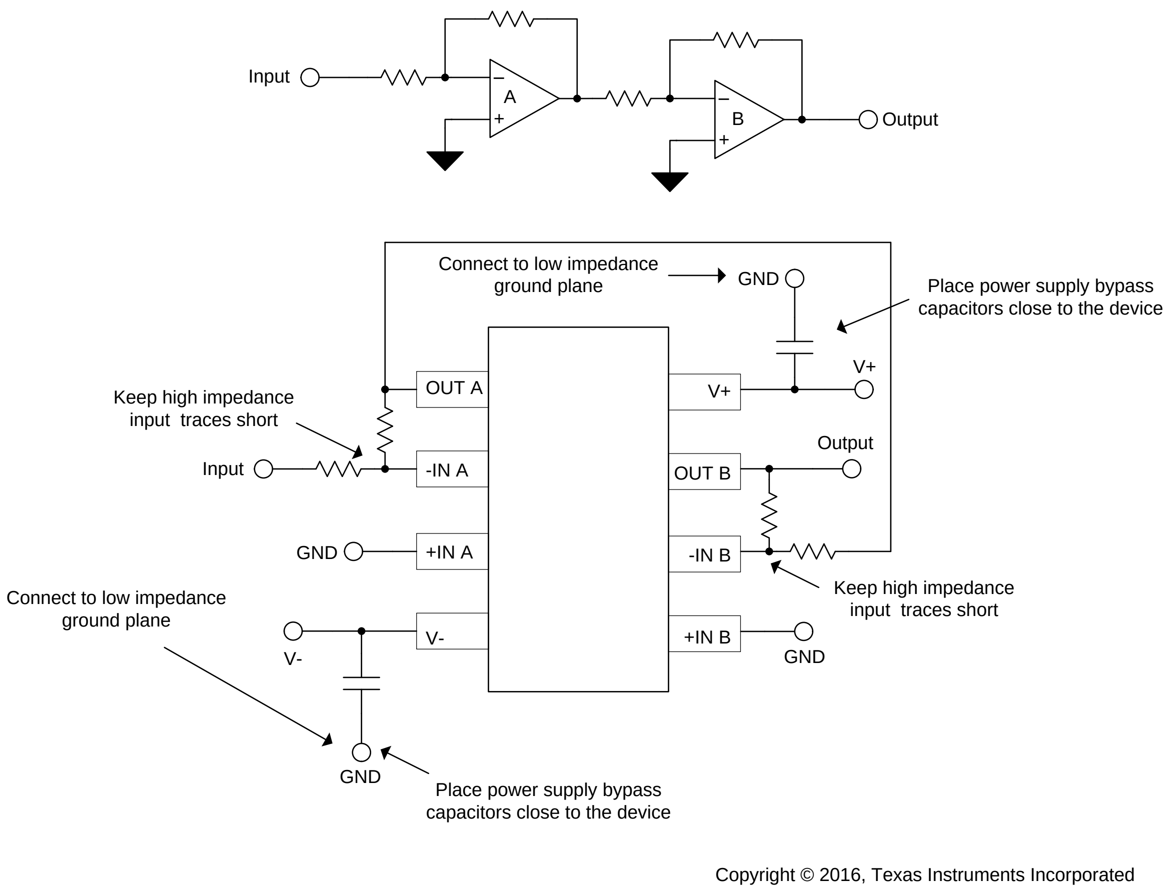

Figure 48. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

12.1.1.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

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12.2 Documentation Support

12.2.1 Related Documentation

The following documents are relevant to using the OPA2188, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *EMI Rejection Ratio of Operational Amplifiers*.
- *Feedback Plots Define Op Amp AC Performance*
- *Op Amp Performance Analysis*.
- *Single-Supply Operation of Operational Amplifiers*
- *Tuning in Amplifiers*.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2188AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)
OPA2188AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)
OPA2188AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)
OPA2188AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDG4.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKTG4.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDGKTG4.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188
OPA2188AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)
OPA2188AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)
OPA2188AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2188 :

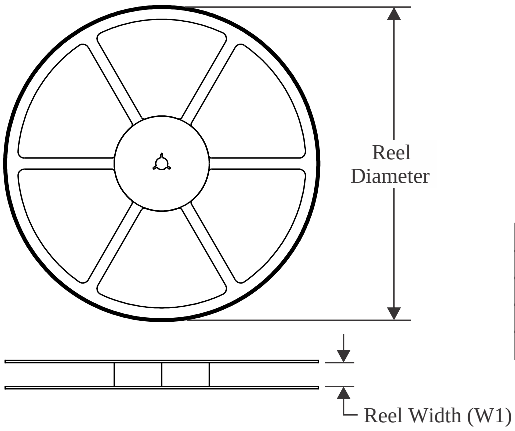
- Automotive : OPA2188-Q1

NOTE: Qualified Version Definitions:

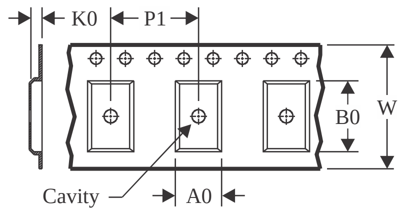
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

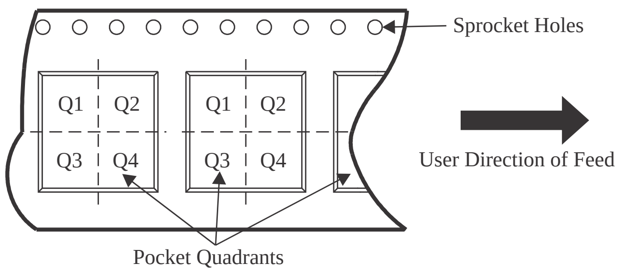


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

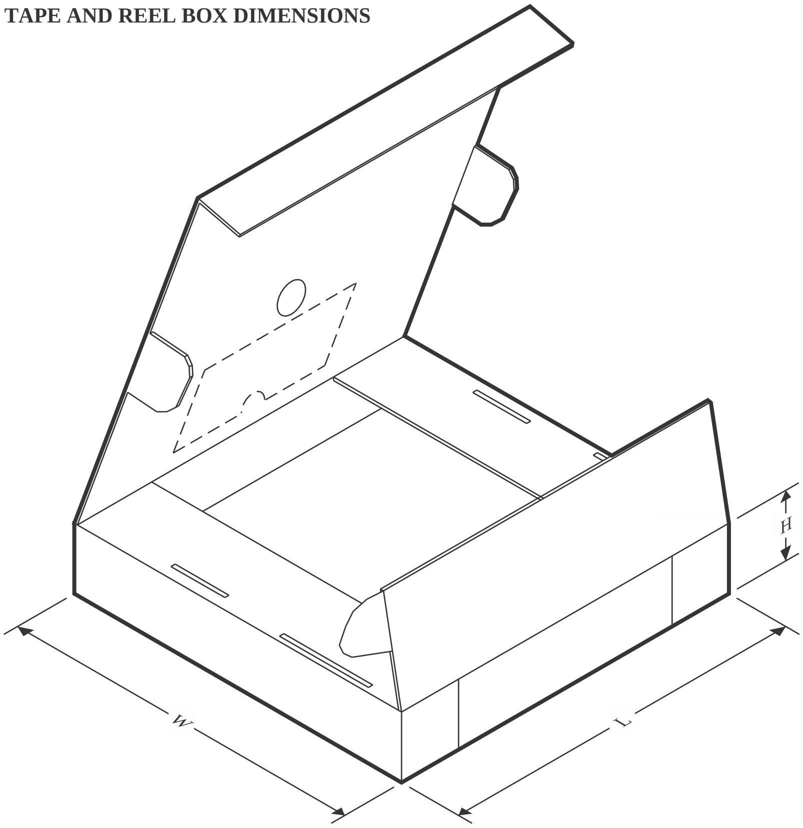
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

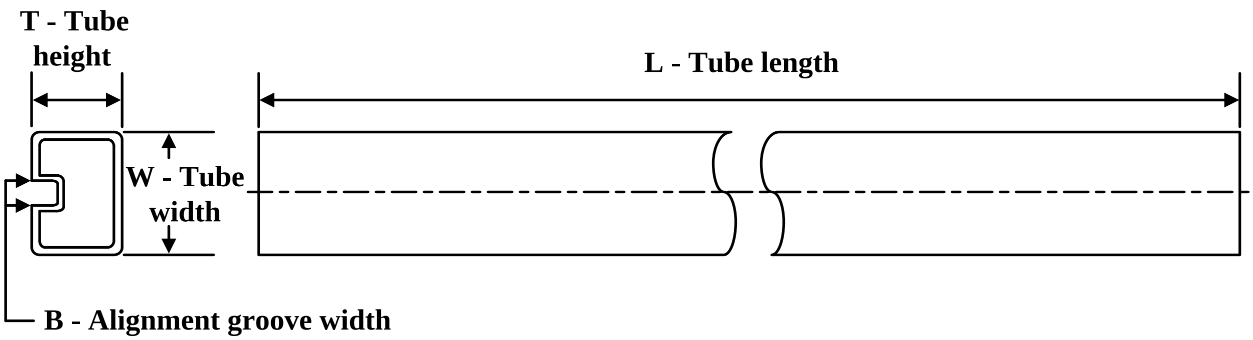
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

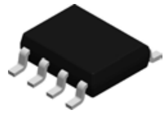
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2188AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2188AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2188AIDGKTG4	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2188AIDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

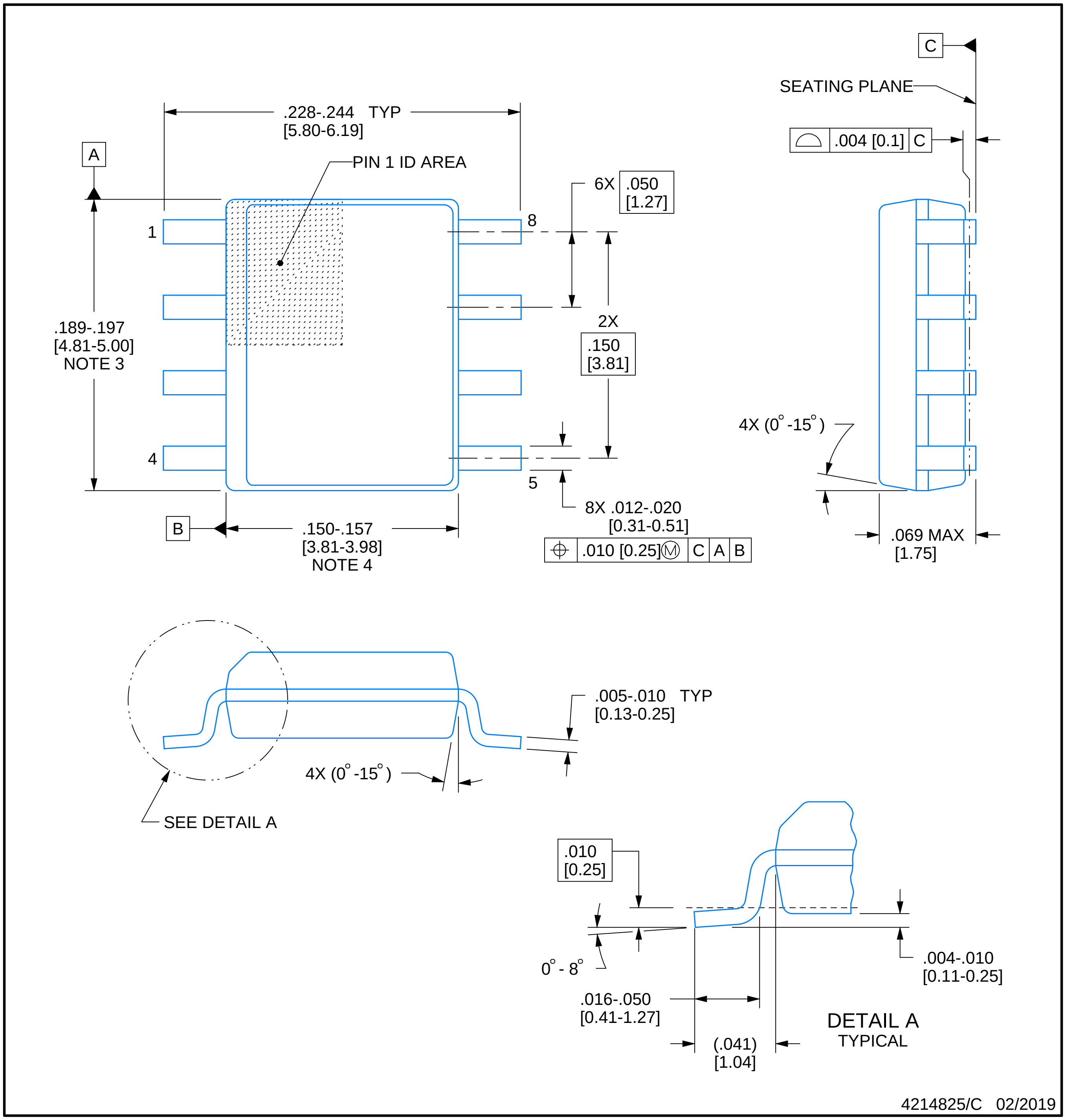
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2188AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2188AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2188AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2188AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2188AIDG4.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2188AIDG4.B	D	SOIC	8	75	506.6	8	3940	4.32



D0008A

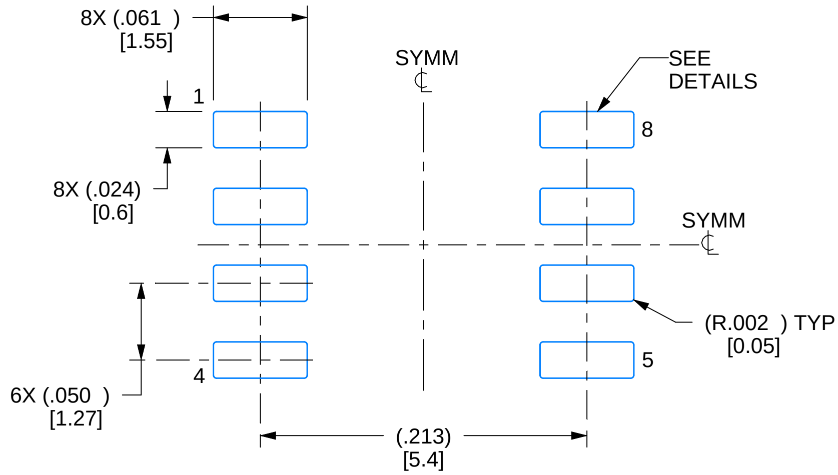
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

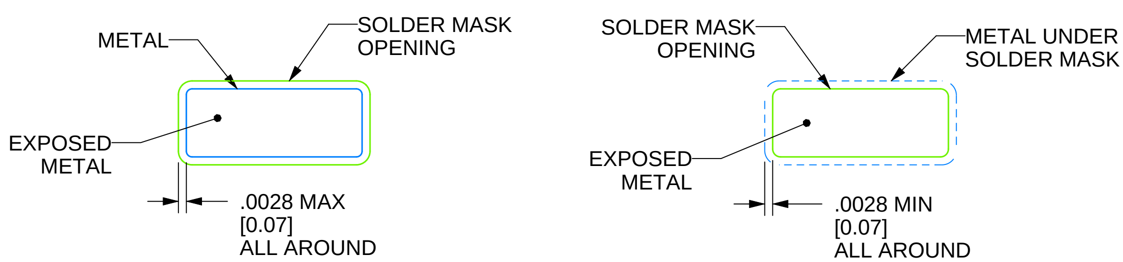


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

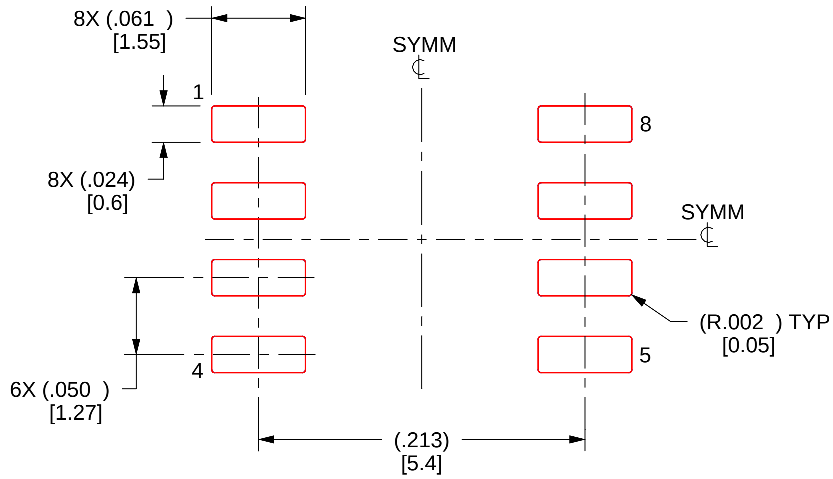
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

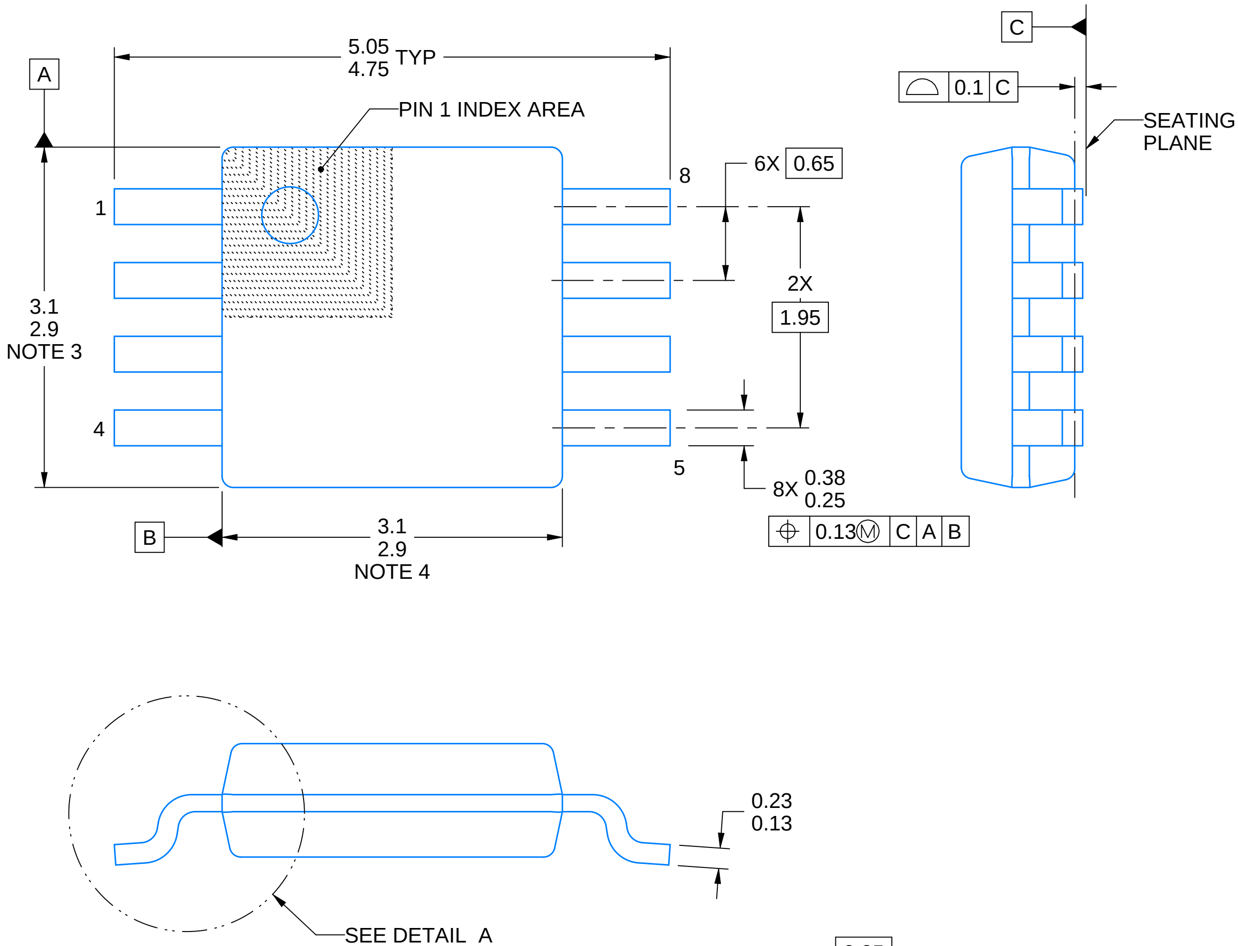
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

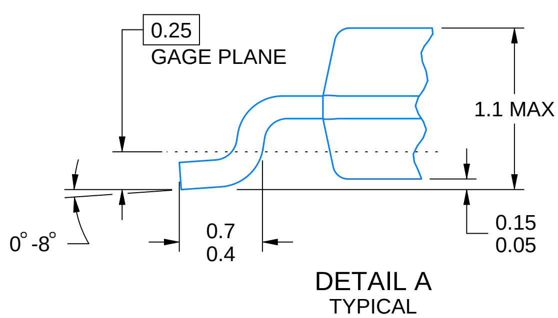
PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



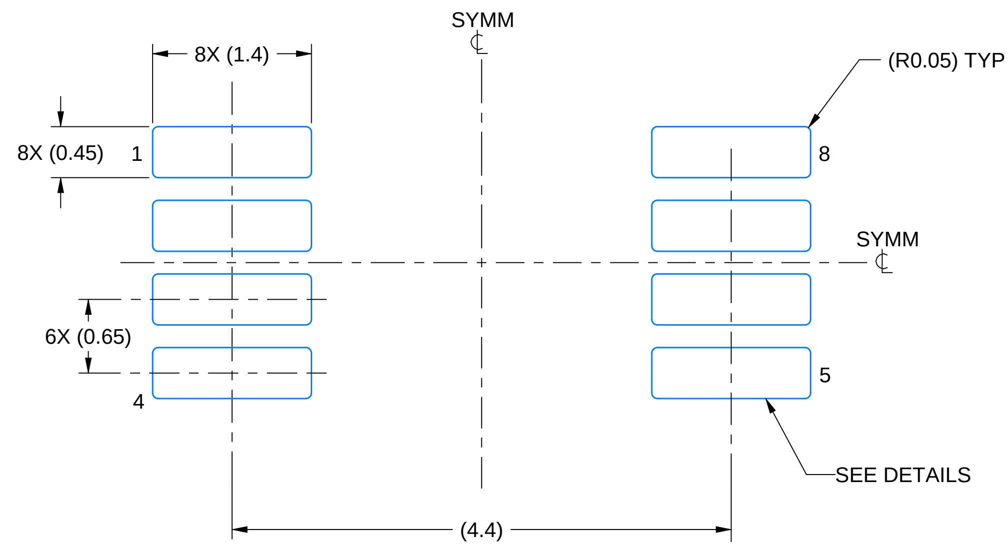


4214862/A 04/2023

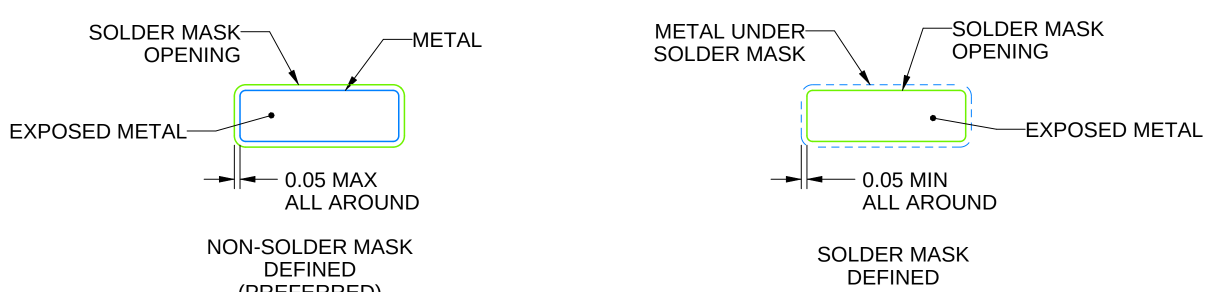
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

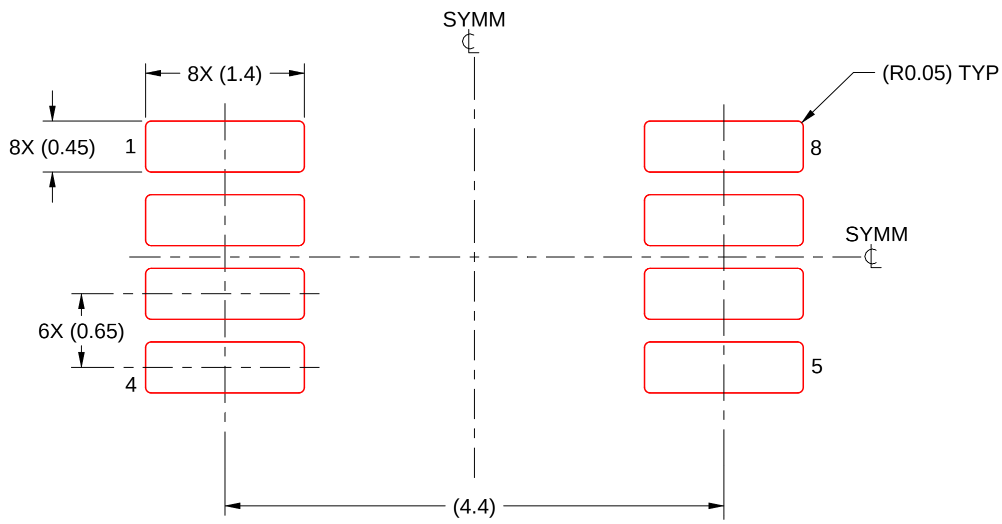


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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