OPA2156 36V、超低ノイズ、広帯域幅、CMOS、高精度、レール・ツー・レール・オペアンプ

1 特長

- 超低ノイズ：10kHz 時に 3nV/√Hz
- 低いオフセット電圧：±25µV
- 低いオフセット電圧ドリフト係数：±0.5µV/℃
- 低いバイアス電流：±5pA
- 同相除去: 120dB
- 低ノイズ: 10kHz時に3nV/√Hz
- 広い帯域幅：25MHz GBW
- 開ループ電圧ゲイン：154dB
- 大きな出力電流：100mA
- レール・ツー・レール入出力
- 高いスルーレート：40V/µs
- 短いセトリング時間：600ns (10V ステップ、0.01%)
- 広い電源電圧範囲：±2.25V～±18V、4.5V～36V
- 業界標準のパッケージ
  - デュアル: SOIC-8、VSSOP-8

2 アプリケーション

- データ・アクイジション (DAQ)
- フォトダイオード・トランスインピーダンス・アンプ
- 振動監視モジュール
- アナログ入力モジュール
- 高分解能の ADC ドライバ・アンプ
- 医療用機器

3 概要

OPA2156は、計画中の新世代36Vレール・ツー・レール・オペアンプの最初の製品です。

このデバイスは、非常に低いオフセット電圧 (±25µV) とドリフト (±0.5µV/℃)、小さなバイアス電流 (±5pA)、および非常に低い広帯域電圧ノイズ (3nV/√Hz) を実現しています。

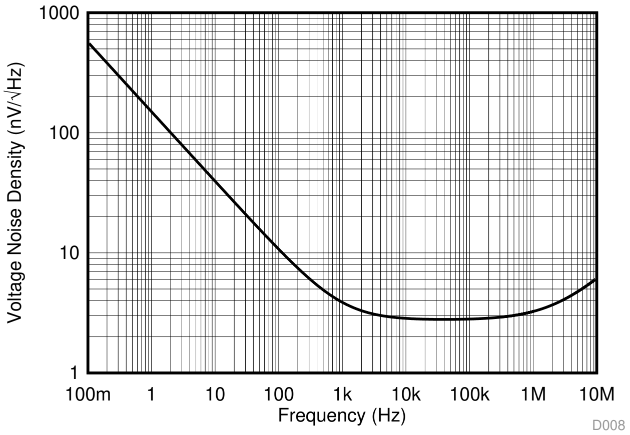
レール・ツー・レールの入力および出力電圧範囲、広い帯域幅 (25MHz)、大きな出力電流 (100mA)、高いスルーレート (40V/µs) など、独自の特長を備えた OPA2156 は高電圧、高精度の産業機器に適した、堅牢かつ高性能なオペアンプです。

製品情報[(1)]

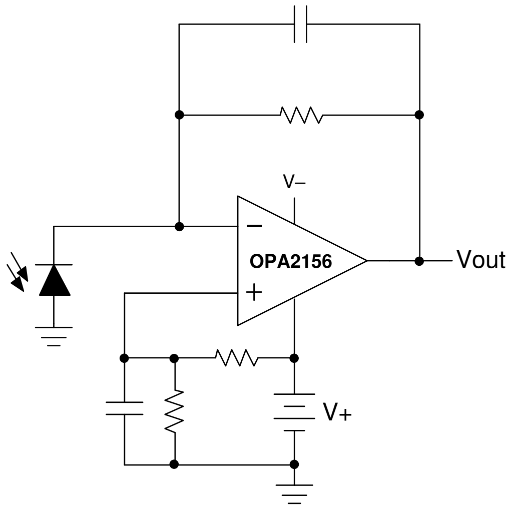
型番	パッケージ	本体サイズ(公称)
OPA2156	SOIC (8)	4.90mm×3.90mm
	VSSOP (8)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

入力電圧のノイズ・スペクトル密度が低い



OPA2156 トランスインピーダンス構成



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2018) から **Revision B** に変更 **Page**

- 新しい DGK (VSSOP) パッケージと関連情報をデータシートに 追加 1
- 変更 Figure 8, *Input Voltage Noise Spectral Density*, to include frequencies up to 10 MHz 9
- 変更 title of input bias and offset current curves (Figures 12 to 14) to specify SOIC package performance 10

2018年**9**月発行のものから更新 **Page**

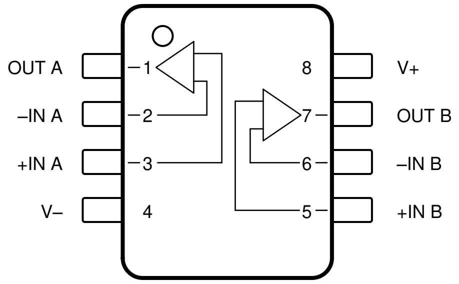
- 量産データ・データシートの初回リリース 1

5 概要（続き）

OPA2156 オペアンプは 8 ピン SOIC および VSSOP パッケージで供給され、–40℃～+125℃の産業用温度範囲で仕様が規定されています。

6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (+40, single supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		0.5	
	Current			±10	mA
Output short circuit[2]			Continuous		
Temperature	Operating junction		–40	150	°C
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extendedperiods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature (SOIC)[1]	–40		125	°C

(1) Please see Thermal Considerations section for information on ambient vs device junction temperature

7.4 Thermal Information: OPA2156

THERMAL METRIC[1]		OPA2156		UNIT
		8 PINS		
		D (SOIC)	DGK (VSSOP)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.2	163.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.1	52.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.7	86.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.7	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.5	84.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25V to ±18V, V_{CM} =V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage, PMOS				±25	±200	µV
		T_A = –40°C to +85°C				±300	µV
		T_A = –40°C to +125°C		See Typical Characteristics			
V_{OS}	Input offset voltage, NMOS	V_{CM} = (V+) – 1.25 V			±0.25	±3	mV
		V_{CM} = (V+) – 1.25 V, T_A = –40°C to +125°C (SOIC)				±5	mV
		V_{CM} = (V+) – 1.25 V, T_A = –40°C to +105°C (MSOP)					
dV_{OS}/dT	Input offset voltage drift	PMOS, SOIC	T_A = –40°C to +125°C		±0.5	±3	µV/°C
		PMOS, MSOP	T_A = –40°C to +105°C				
		NMOS, V_{CM} = (V+) – 1.25 V	T_A = –40°C to +125°C		±1		
PSRR	Power-supply rejection ratio				±0.3	±4.5	µV/V
		T_A = –40°C to +125°C (SOIC)				±5	
		T_A = –40°C to +105°C (MSOP)					
INPUT BIAS CURRENT							
I_B	Input bias current	SOIC			±5	±40	pA
		MSOP			±5	±80	pA
		T_A = –40°C to +85°C (SOIC)				±1.5	nA
		T_A = –40°C to +85°C (MSOP)				±15	nA
		T_A = –40°C to +125°C		See Typical Characteristics			nA
I_{OS}	Input offset current				±2	±40	pA
		T_A = –40°C to +85°C (SOIC)				±1.5	nA
		T_A = –40°C to +85°C (MSOP)				±2.5	nA
		T_A = –40°C to +125°C		See Typical Characteristics			nA
NOISE							
E_n	Input voltage noise	(V–) < V_{CM} < (V+) – 2.25 V	f = 0.1 Hz to 10 Hz		1.9		μV_{PP}
		(V+) – 1.25 V < V_{CM} < (V+)	f = 0.1 Hz to 10 Hz		3.4		
e_n	Input voltage noise density	(V–) < V_{CM} < (V+) – 2.25 V	f = 100 Hz		12.0		nV/√Hz
			f = 1 kHz		4		
			f = 10 kHz		3.0		
e_n	Input voltage noise density	(V+) – 1.25 V < V_{CM} < (V+)	f = 100 Hz		13.0		
			f = 1 kHz		9.7		
			f = 10 kHz		4.0		
i_n	Input current noise density	f = 1 kHz			19		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio, PMOS	(V–) < V_{CM} < (V+) – 2.25 V, V_S = ±18 V		106	120		dB
CMRR	Common-mode rejection ratio, PMOS	T_A = –40°C to +125°C (SOIC)		100			
CMRR	Common-mode rejection ratio, PMOS	T_A = –40°C to +105°C (MSOP)					
CMRR	Common-mode rejection ratio, NMOS	(V+) – 1.25 V < V_{CM} < (V+), V_S = ±18 V		82	120		
CMRR	Common-mode rejection ratio, NMOS	T_A = –40°C to +125°C (SOIC)		74			
CMRR	Common-mode rejection ratio, NMOS	T_A = –40°C to +105°C (MSOP)					

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±2.25V to ±18V, V_{CM} =V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9.1		MΩ || pF
Z_{IC}	Common-mode				6 || 1.9		10^{12}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, V_S = ±18 V (SOIC)		130	154		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, V_S = ±18 V (MSOP)		128	154		
		T_A = –40°C to +85°C		126			
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				20		MHz
	Gain bandwidth product	G = 100			25		MHz
SR	Slew rate	V_S = ±18 V, G = –1, 10-V step			40		V/µs
t_s	Settling time	To 0.01%, C_L = 20 pF	V_S = ±18 V, G = –1, 10-V step		600		ns
t_{OR}	Overload recovery time	G = –10			100		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			–132		dB
					0.000025 %		
		G = 1, f = 20 kHz, V_O = 3.5 V_{RMS}			–126		dB
					0.00005%		
	Crosstalk	dc			150		dB
		f = 100 kHz			120		dB
OUTPUT							
V_O	Voltage output swing from power supply				200	250	mV
I_{SC}	Short-circuit current	V_S = ±18 V			100		mA
C_L	Capacitive load drive				See Typical Characteristics		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			25		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			4.4	5.2	mA
			T_A = –40°C to +125°C (SOIC)			5.2	mA
			T_A = –40°C to +105°C (MSOP)				mA
TEMPERATURE							
	Thermal protection				170		°C
	Thermal hysteresis				15		°C

7.6 Typical Characteristics

表 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage vs Temperature (PMOS)	図 2
Offset Voltage vs Temperature (NMOS)	図 3
Offset Voltage vs Power Supply	図 4
Offset Voltage vs Common-Mode Voltage	図 5
Offset Voltage vs Common-Mode Voltage in Transition Region	図 6
Offset Voltage Drift	図 7
Input Voltage Noise Spectral Density	図 8
0.1-Hz to 10-Hz Noise	図 9
THD+N vs Frequency	図 10
THD+N vs Output Amplitude	図 11
Input Bias and Offset Current vs Common-Mode Voltage	図 12
Input Bias and Offset Current vs Temperature	図 13
Input Bias and Offset Current vs Temperature	図 14
Open-Loop Output Impedance vs Frequency	図 15
Maximum Output Voltage vs Frequency	図 16
Open-Loop Gain and Phase Vs Frequency	図 17
Open-Loop Gain vs Temperature	図 18
Closed-Loop Gain vs Frequency	図 19
CMRR vs Frequency	図 20
PSRR vs Frequency	図 21
CMRR vs Temperature	図 22
PSRR vs Temperature	図 23
Positive Output Voltage vs Output Current	図 24
Negative Output Voltage vs Output Current	図 26
Short-Circuit Current vs Temperature	図 25
No Phase Reversal	図 27
Phase Margin vs Capacitive Load	図 28
Small-Signal Overshoot vs Capacitive Load (G = –1)	図 29
Small-Signal Overshoot vs Capacitive Load (G= +1)	図 30
Settling Time	図 31
Negative Overload Recovery	図 32
Positive Overload Recovery	図 33
Small-Signal Step Response (Noninverting)	図 34
Small-Signal Step Response (Inverting)	図 35
Large-Signal Step Response (Noninverting)	図 36
Large-Signal Step Response (Inverting)	図 37
Quiescent Current vs Supply Voltage	図 38
Quiescent Current vs Temperature	図 39
Channel Separation vs Frequency	図 40
EMIRR vs Frequency	図 41

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

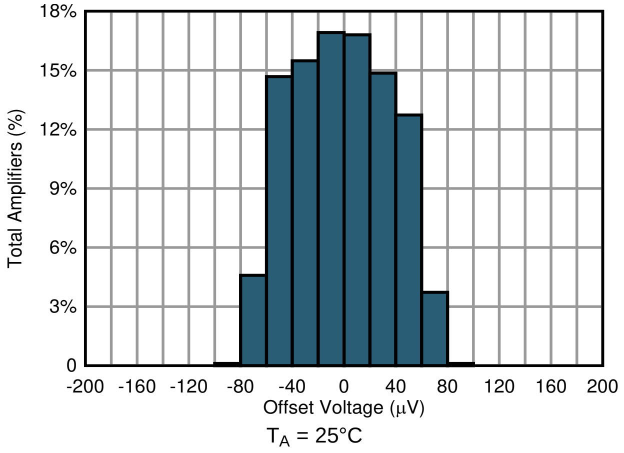


図 1. Offset Voltage Production Distribution

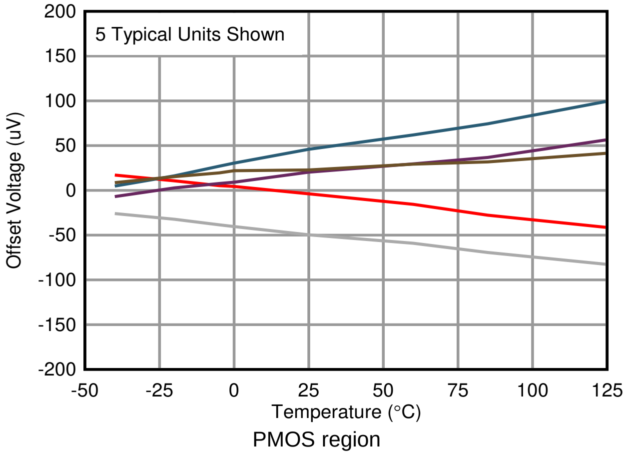


図 2. Offset Voltage vs Temperature (PMOS)

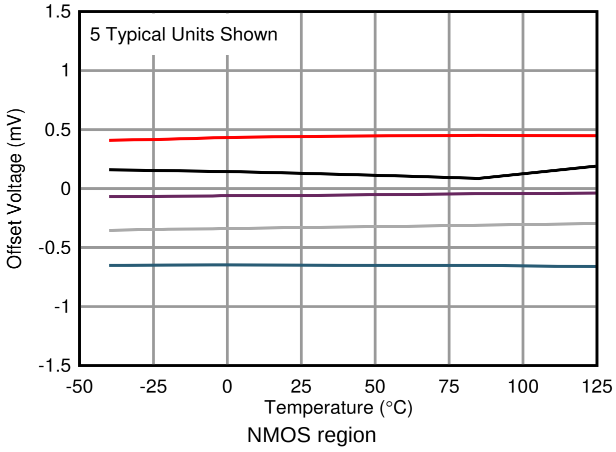


図 3. Offset Voltage vs Temperature (NMOS)

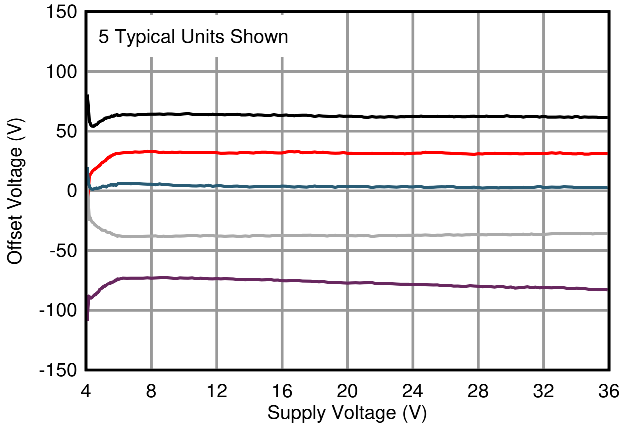


図 4. Offset Voltage vs Power Supply

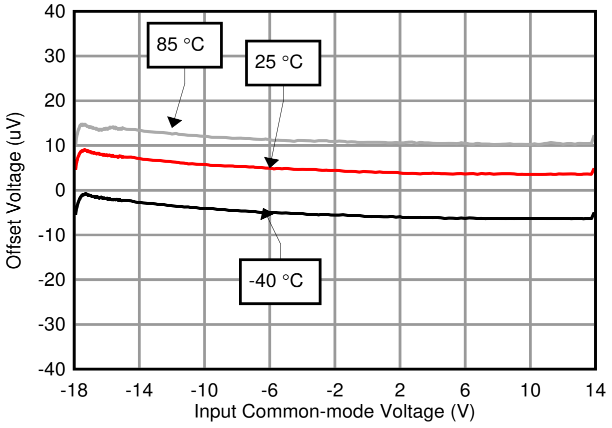


図 5. Offset Voltage vs Common-Mode Voltage

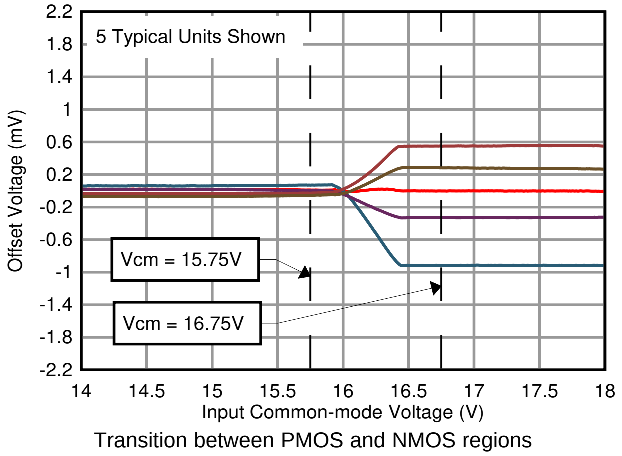
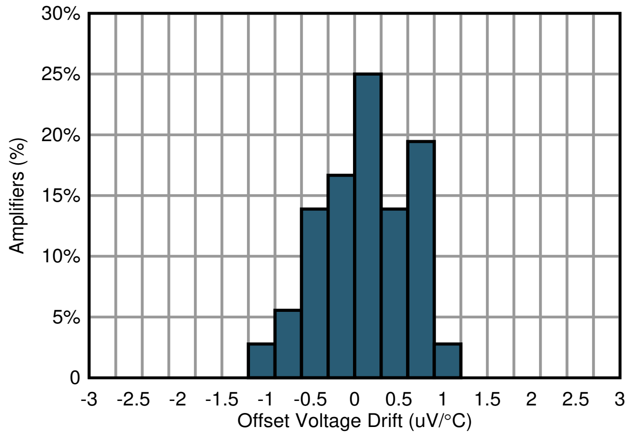


図 6. Offset Voltage vs Common-Mode Voltage in Transition Region

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



T_A = –40°C to +125°C

図 7. Offset Voltage Drift

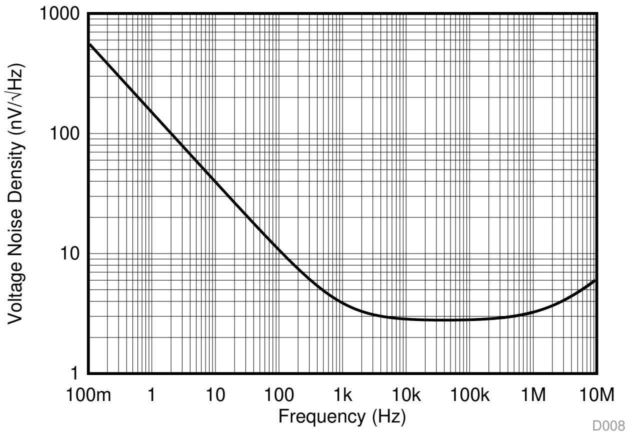


図 8. Input Voltage Noise Spectral Density

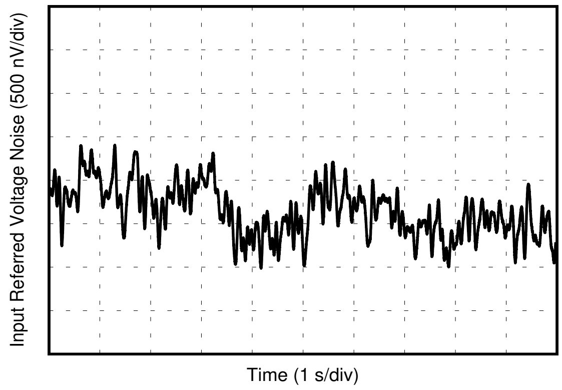
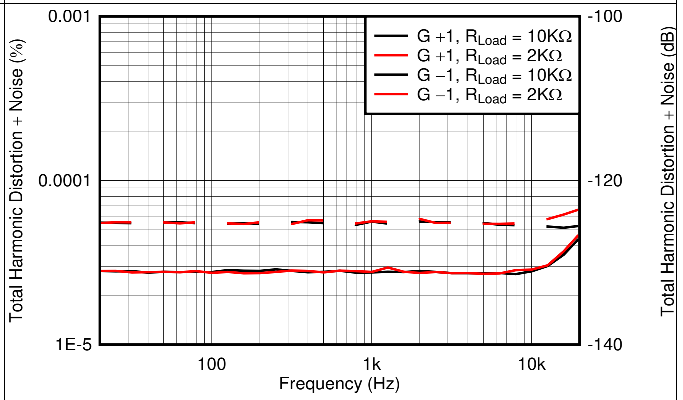
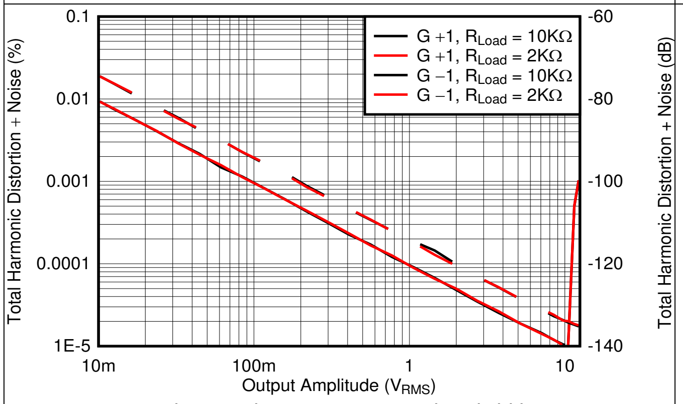


図 9. 0.1-Hz to 10-Hz Noise



3.5 V_{RMS}, 80-kHz measurement bandwidth

図 10. THD+N vs Frequency



1 kHz, 80-kHz measurement bandwidth

図 11. THD+N vs Output Amplitude

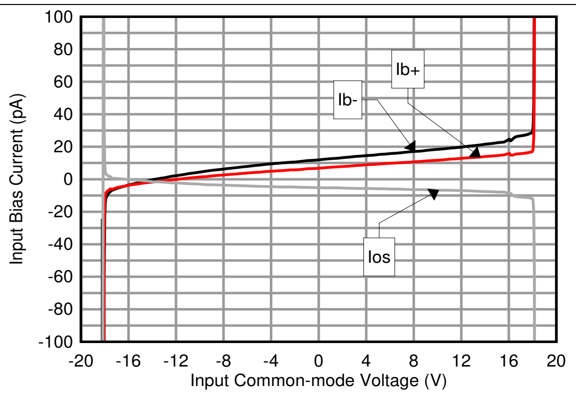
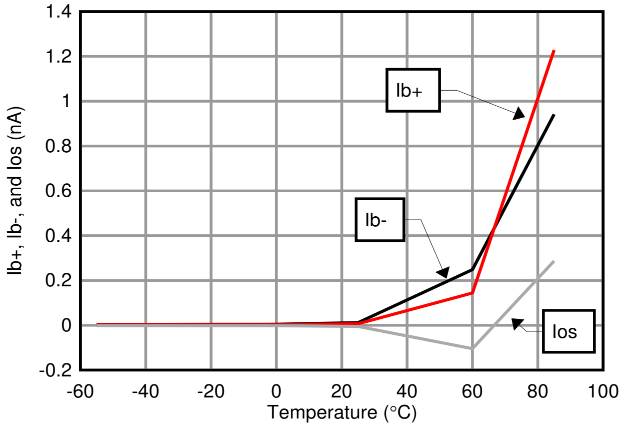


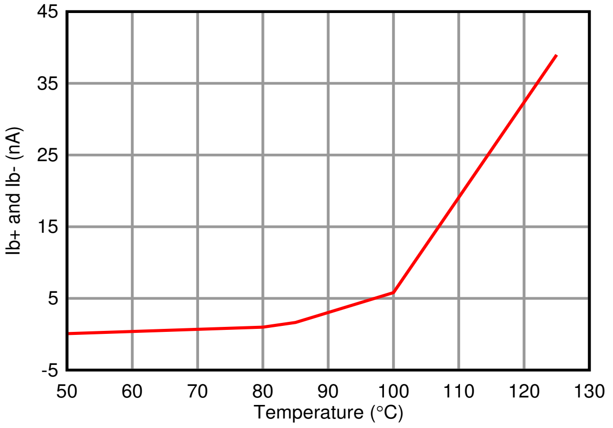
図 12. Input Bias and Offset Current vs Common-Mode Voltage (SOIC)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



T_A = –55°C to +85°C

図 13. Input Bias and Offset Current vs Temperature (SOIC)



T_A = –55°C to +125°C

図 14. Input Bias and Offset Current vs Temperature (SOIC)

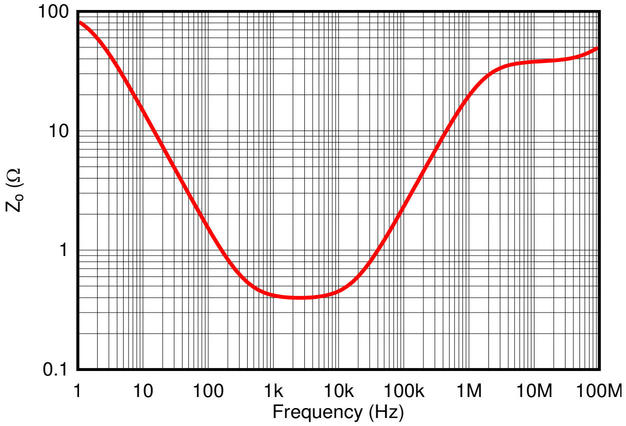


図 15. Open-Loop Output Impedance vs Frequency

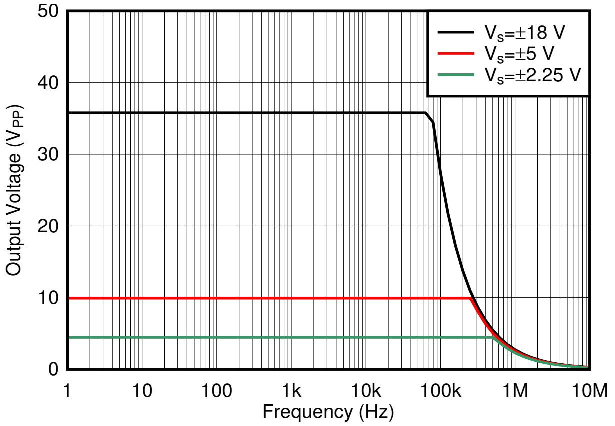


図 16. Maximum Output Voltage vs Frequency

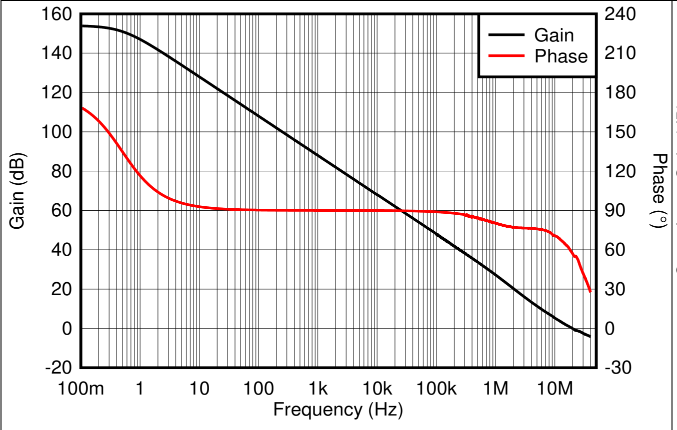


図 17. Open-Loop Gain and Phase vs Frequency

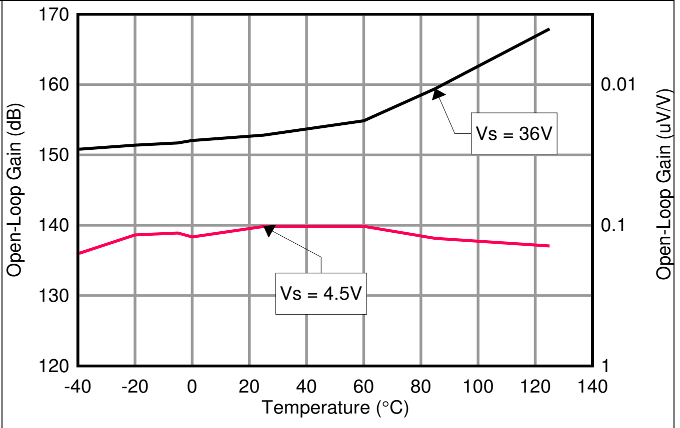


図 18. Open-Loop Gain vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

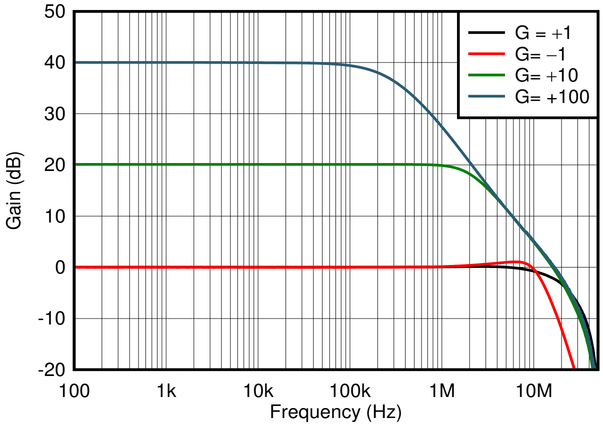


図 19. Closed-Loop Gain vs Frequency

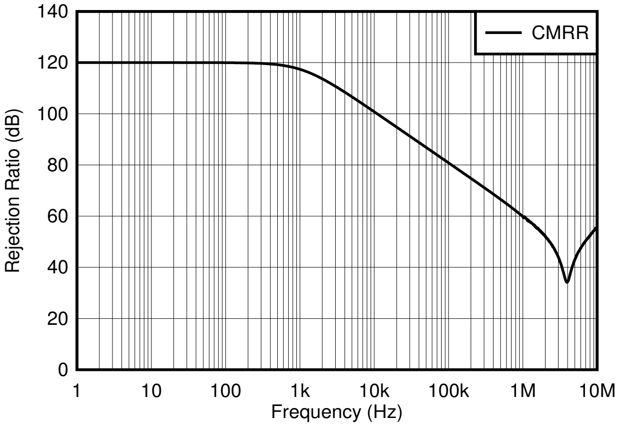


図 20. CMRR vs Frequency

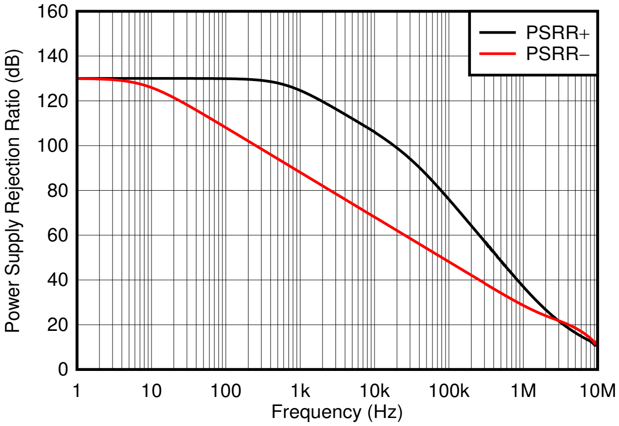


図 21. PSRR vs Frequency

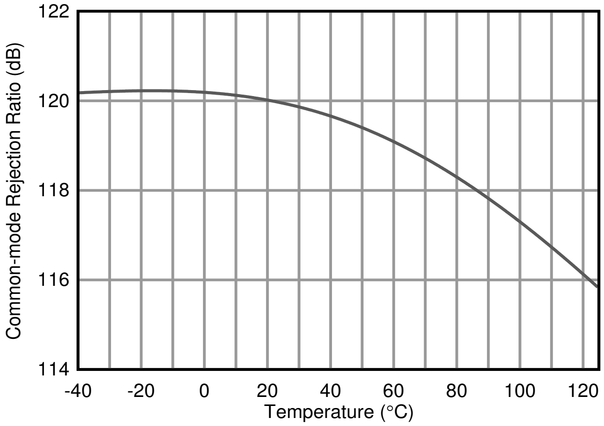


図 22. CMRR vs Temperature

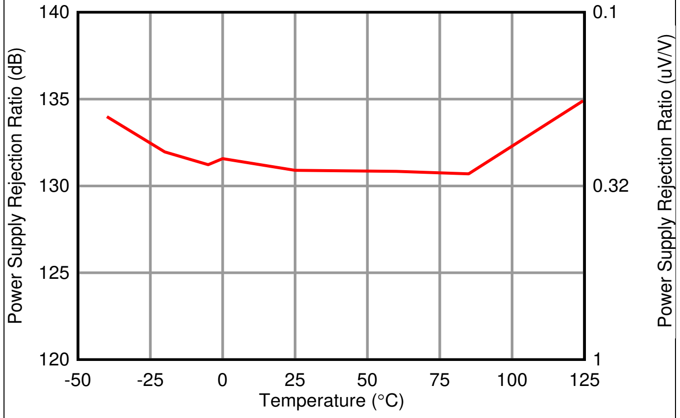


図 23. PSRR vs Temperature

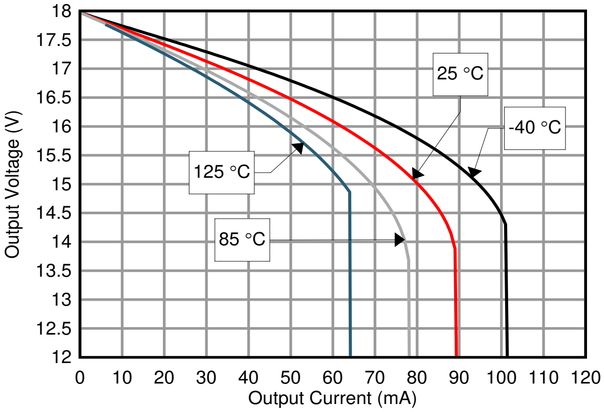


図 24. Positive Output Voltage vs Output Current

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

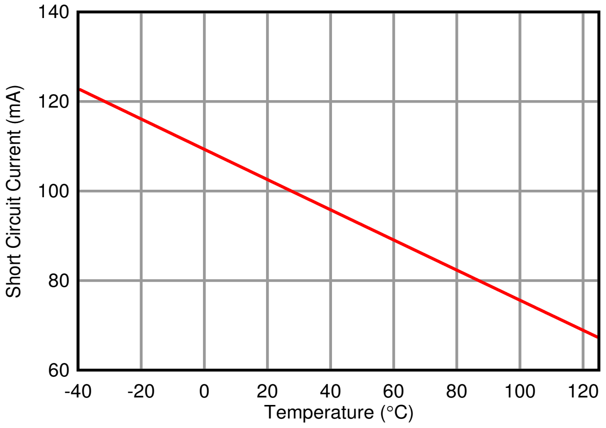


図 25. Short-Circuit Current vs Temperature

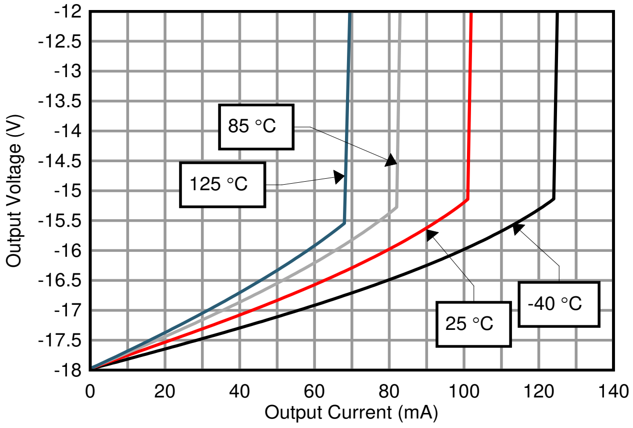


図 26. Negative Output Voltage vs Output Current

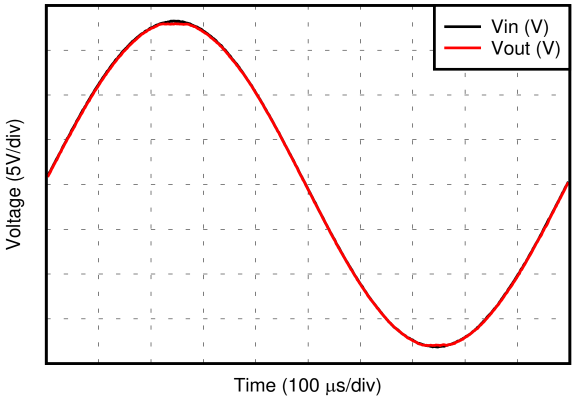


図 27. No Phase Reversal

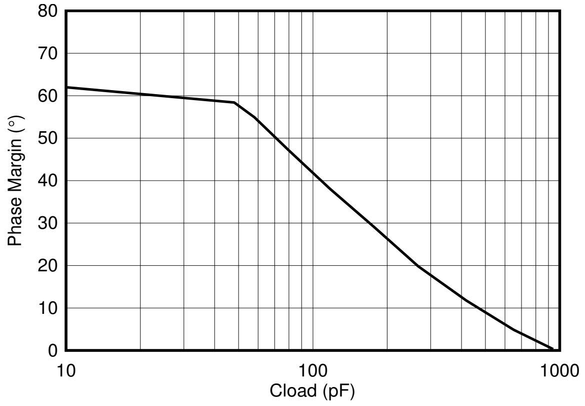
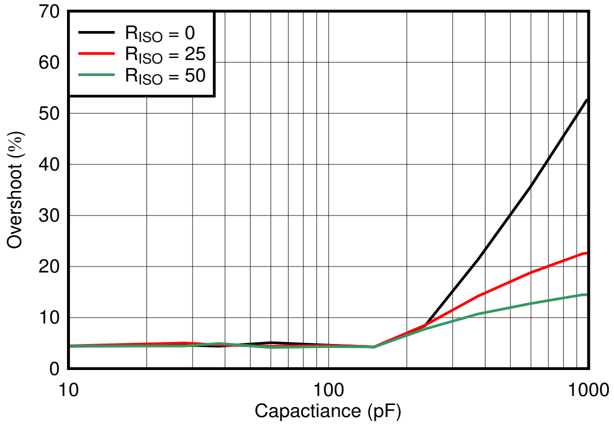
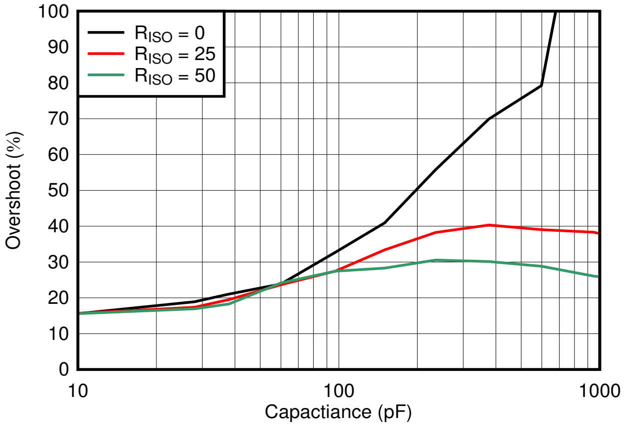


図 28. Phase Margin vs Capacitive Load



10-mV output step, gain = –1

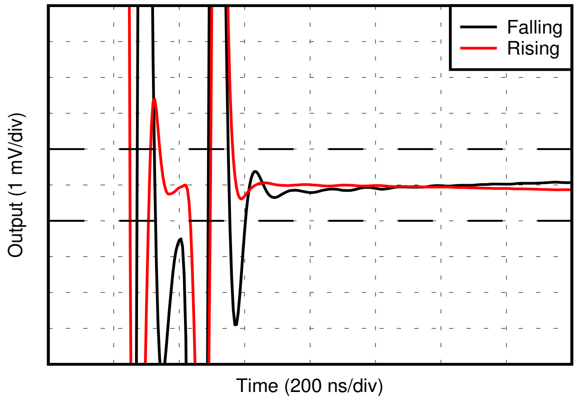
図 29. Small Signal Overshoot vs Capacitive Load



10-mV output step, gain = +1

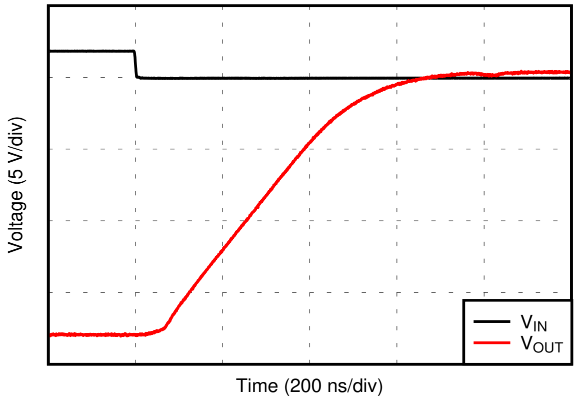
図 30. Small Signal Overshoot vs Capacitive Load

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



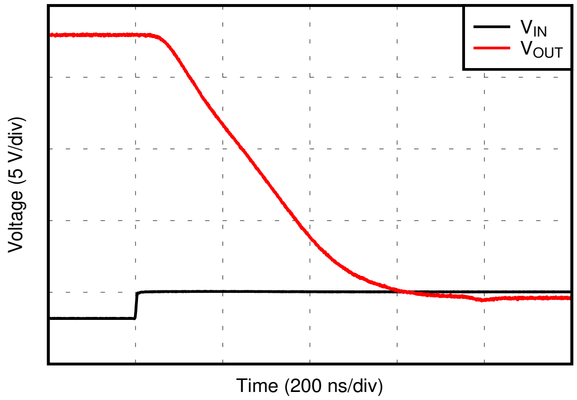
Vin = 5-Vpp

図 31. Normalized Settling Time



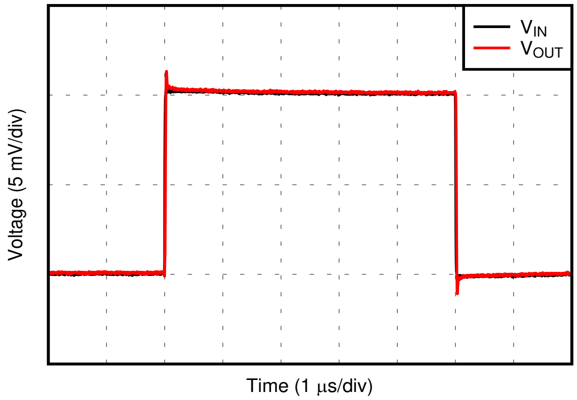
Gain = –10

図 32. Negative Overload Recovery



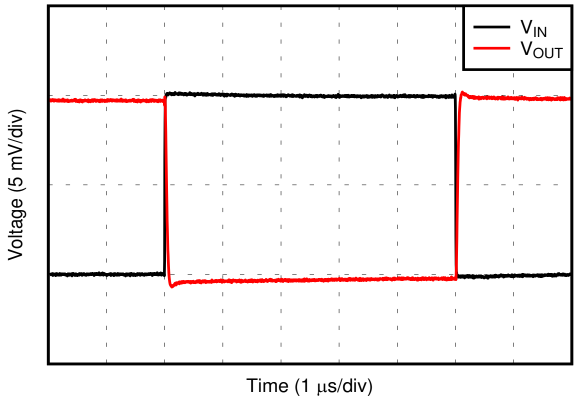
Gain = –10

図 33. Positive Overload Recovery



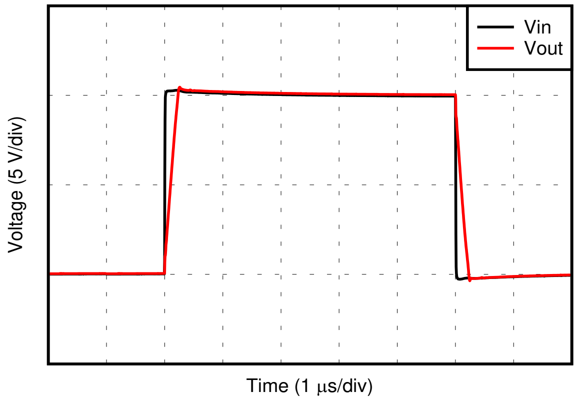
Vin = 10 mVpp, gain = 1

図 34. Small-Signal Step Response (Noninverting)



Vin = 10 mVpp, gain = –1

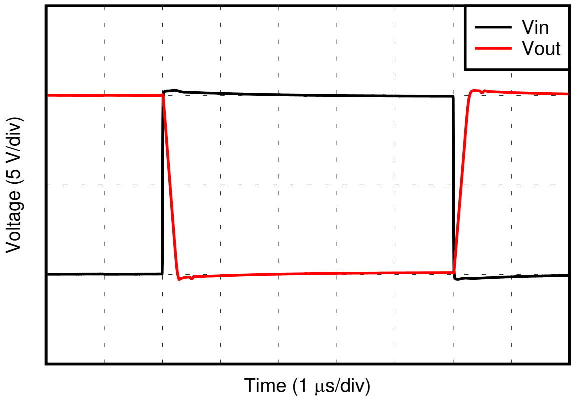
図 35. Small-Signal Step Response (Inverting)



Vin = 5 Vpp, gain = 1

図 36. Large-Signal Step Response (Noninverting)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



Vin = 5 Vpp, gain = –1

図 37. Large Signal Step Response (Inverting)

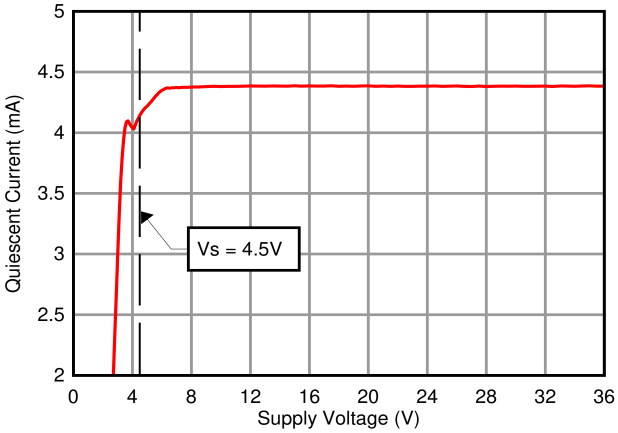


図 38. Quiescent Current vs Supply Voltage

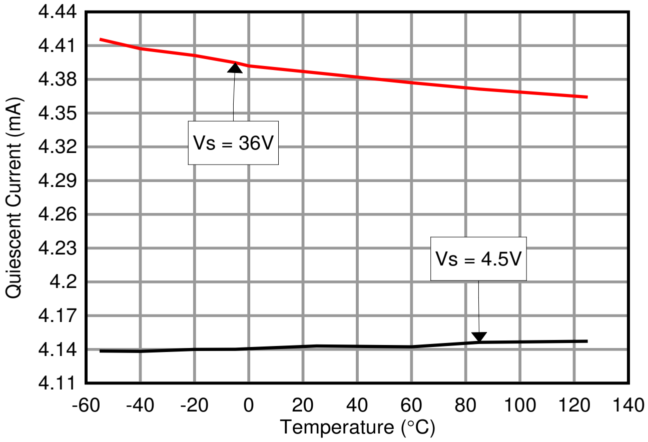


図 39. Quiescent Current vs Temperature

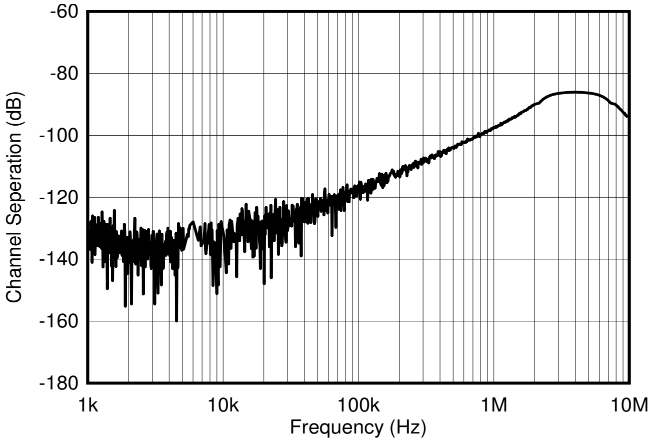
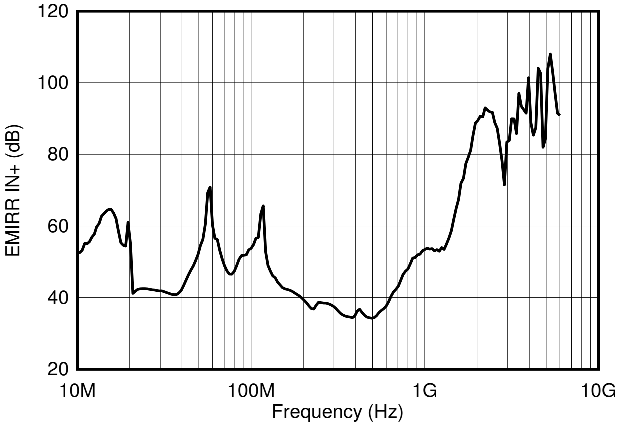


図 40. Channel Separation vs Frequency



Prf =-10 dBm

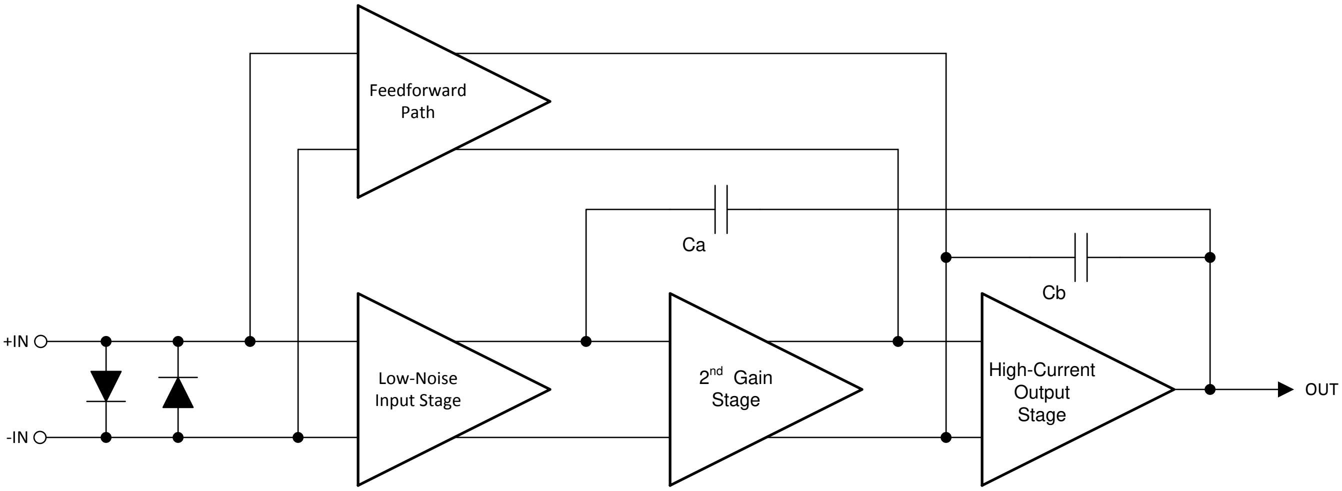
図 41. EMIRR vs Frequency

8 Detailed Description

8.1 Overview

The OPA2156 is laser trimmed to improve offset and uses a three-gain-stage architecture to achieve very low noise and distortion. The *Functional Block Diagram* shows a simplified schematic of the OPA2156 (one channel shown). The device consists of a low noise input stage and feed-forward pathway coupled to a high-current output stage. This topology exhibits superior distortion performance under a wide range of loading conditions compared to other operational amplifiers.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Phase Reversal Protection

The OPA2156 has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA2156 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 図 42.

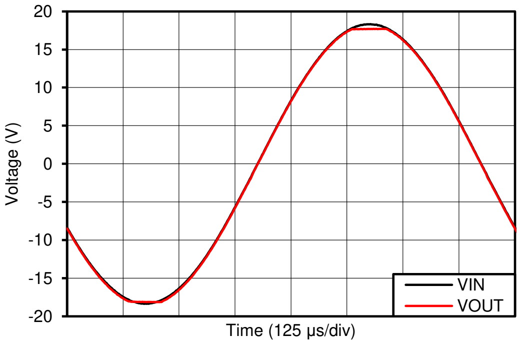


図 42. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

Feature Description (continued)

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 43 illustrates the ESD circuits contained in the OPA2156 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

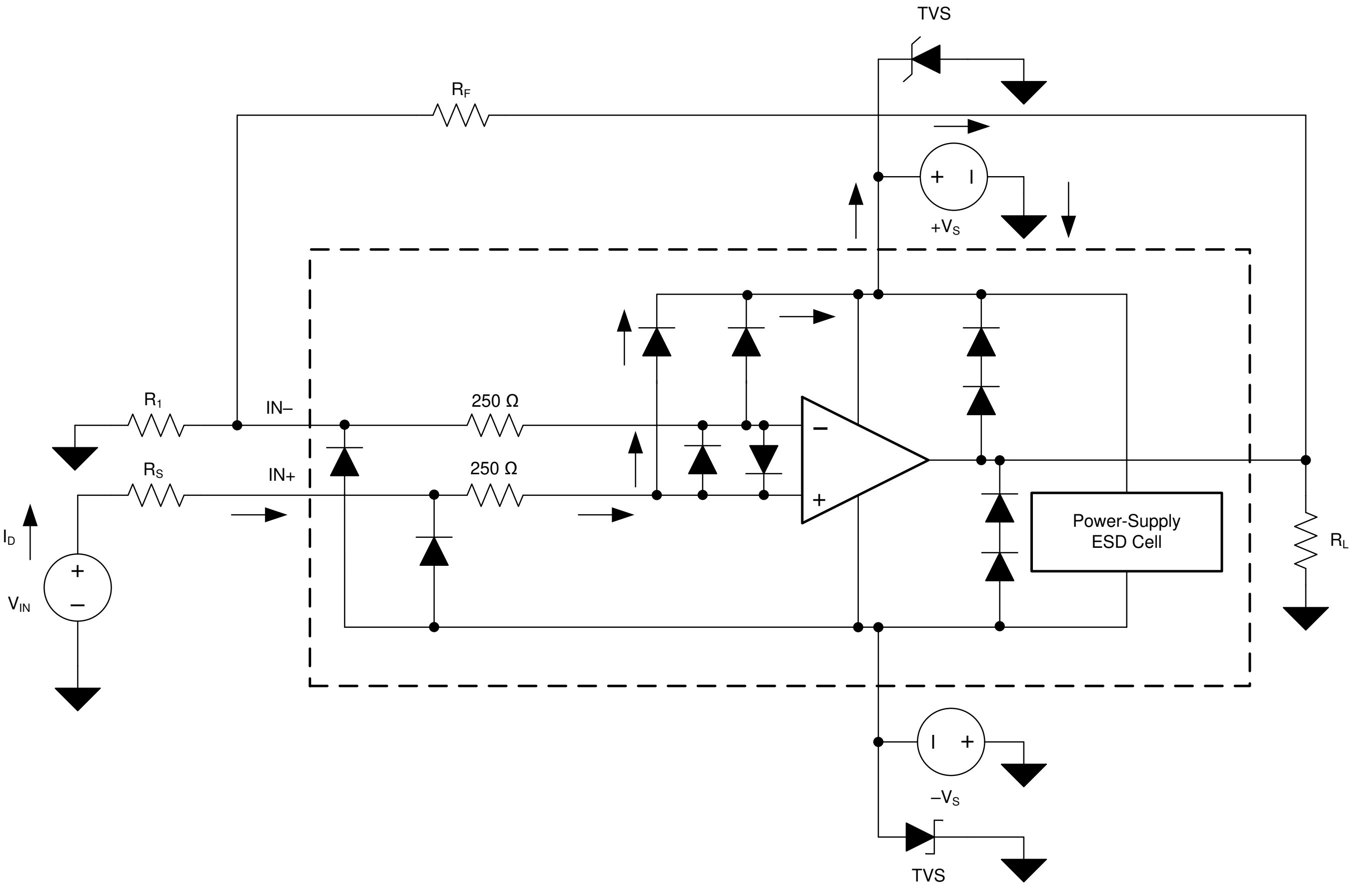


図 43. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2156 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Feature Description (continued)

When the operational amplifier connects into a circuit (see 図 43), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 43 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 43. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

Feature Description (continued)

8.3.3 Thermal Considerations

Through normal operation the OPA2156 will experience self-heating, a natural increase in the die junction temperature which occurs in every amplifier. This is a result of several factors including the quiescent power consumption, the package's thermal dissipation, PCB layout and the device operating conditions.

To fully ensure the amplifier will operate without entering thermal shutdown it is important to calculate the approximate junction (die) temperature which can be done using 式 1.

$$T_J = P_D * \Theta J_A + T_A \quad (1)$$

式 2 shows the approximate junction temperature for the OPA2156 while unloaded with an ambient temperature of 25°C.

$$T_J = (36V * 4.4mA) * 120°C / W + 25°C$$
$$T_J = 44°C \quad (2)$$

For high voltage, high precision amplifiers such as the OPA2156 the junction temperature can easily be 10s of degrees higher than the ambient temperature in a quiescent (unloaded) condition. If the device then begins to drive a heavy load the junction temperature may rise and trip the thermal shutdown circuit. The 図 44 shows the maximum output voltage of the OPA2156 without entering thermal shutdown vs ambient temperature in both a loaded and unloaded condition.

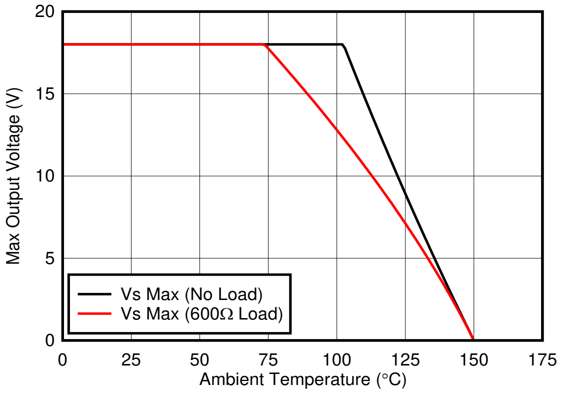


図 44. **OPA2156 Thermal Safe Operating Area**

Feature Description (continued)

8.3.4 Thermal Shutdown

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The OPA2156 has a thermal protection feature that prevents damage from self heating.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 170°C. Thermal protection forces the output to a high-impedance state. The OPA2156 is also designed with approximately 15°C of thermal hysteresis. Thermal hysteresis prevents the output stage from cycling in and out of the high-impedance state. The OPA2156 returns to normal operation when the output stage temperature falls below approximately 155°C.

The absolute maximum junction temperature of the OPA2156 is 150°C. Exceeding the limits shown in the *Absolute Maximum Ratings* table may cause damage to the device. Thermal protection triggers at 170°C because of unit-to-unit variance, but does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

8.3.5 Common-Mode Voltage Range

The OPA2156 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 2.25 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.25 V. There is a small transition region, typically (V+) – 2.25V to (V+) – 1.25 V in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPA2156 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range.

8.3.6 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

8.4 Device Functional Modes

The OPA2156 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPA2156 is 36 V (±18 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA2156 offers excellent dc precision and ac performance. The device operates with up to 36-V supply rails offering true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 25-MHz bandwidth and low input bias. These features make the OPA2156 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.1.1 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPA2156 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. 図 45 shows the OPA2156 in a slew-rate limit design.

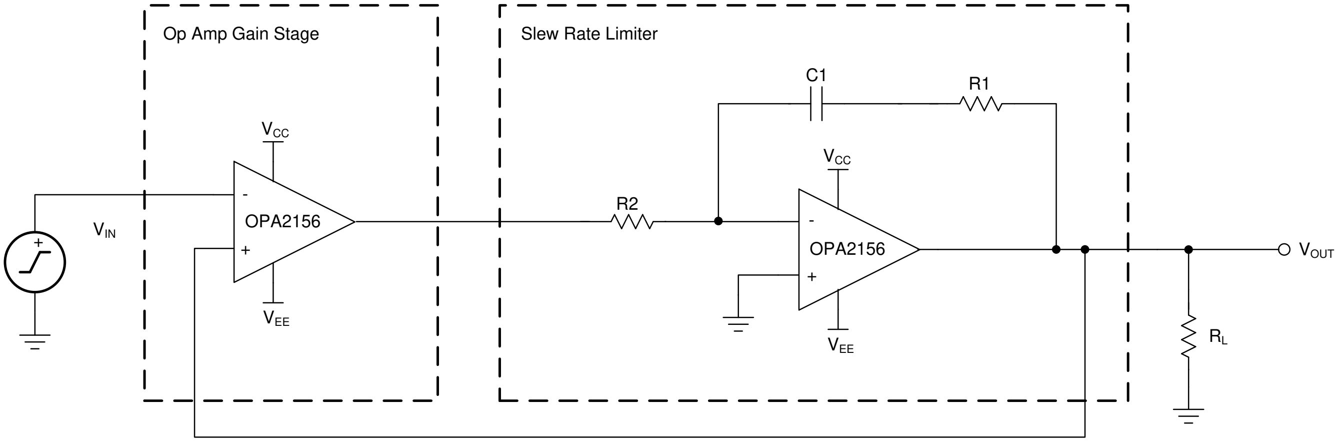


図 45. Slew Rate Limiter Uses One Op Amp

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

9.2 Typical Application

The combination of low input bias, high slew rate and a rail-to-rail input and output enable the OPA2156 to serve as an accurate differential photodiode transimpedance amplifier. This application example shows the design of such a system.

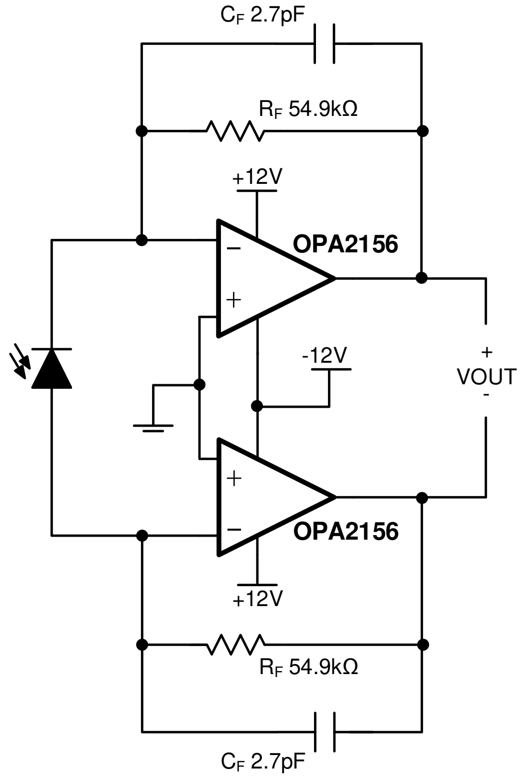


図 46. OPA2156 Configured as a Differential Photodiode Transimpedance Amplifier

9.2.1 Design Requirements

The design requirements for this design are:

- Photodiode current: 0 µA to 90 µA
- Output voltage: –5 V to 5 V
- Supply voltage: ±12 V
- Filter cutoff frequency: 1 MHz

9.2.2 Detailed Design Procedure

In this example the OPA2156 serves as a transimpedance amplifier for a differential photodiode. The differential configuration allows for a wider output range (0 to 10-V differential) compared to a single-ended configuration (0 V to 5 V). This output can be connected to a differential successive approximation register (SAR) analog-to-digital converter (ADC). The basic equation for a differential transimpedance amplifier output voltage is shown in 式 3.

$$V_{OUT} = I_{PD} \times 2 \times R_F \tag{3}$$

式 3 can be rearranged to calculate the value of the feedback resistors as shown in 式 4.

Typical Application (continued)

$$\frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{2 \times I_{IN(MAX)}} \leq R_F$$

$$\frac{5V - (-5V)}{2 \times 90 \mu A} \leq 55.6 k\Omega \tag{4}$$

Adding a capacitor to the feedback loop creates a filter which will remove undesired noise beyond its cutoff frequency. For this application a 1-MHz cutoff frequency was selected. The equation for an RC filter is provided in 式 5.

$$f_C = \frac{1}{2 \times \pi \times R_F \times C_F} \tag{5}$$

Rearranging this equation to solve for the capacitor value is show in 式 6.

$$C_F \leq \frac{1}{2 \times \pi \times 54k\Omega \times 1MHz} \leq 2.7 pF \tag{6}$$

For more information on photodiode transimpedance amplifier system design and for a single-ended example, see *TIDU535: 1 MHz, Single-Supply, Photodiode Amplifier Reference Design*.

9.2.3 Application Curves

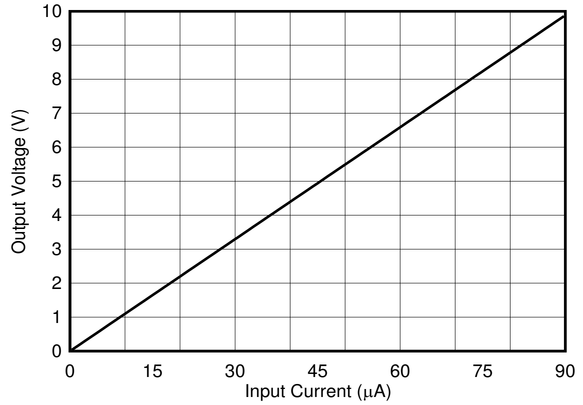


図 47. Differential Photodiode DC Transfer

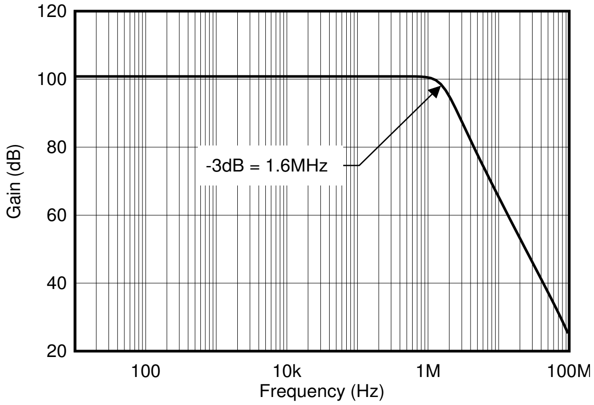


図 48. Differential Photodiode AC Transfer

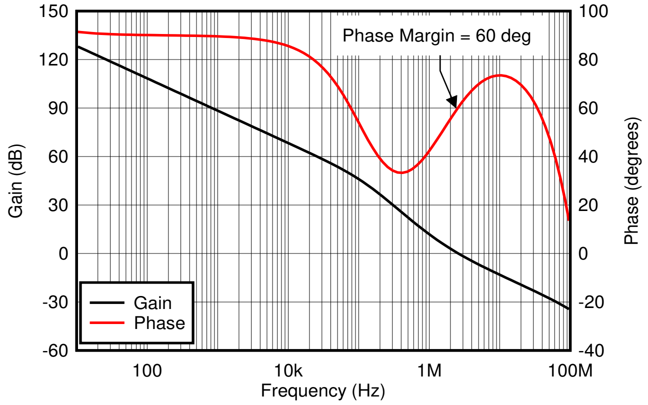


図 49. Differential Photodiode Stability

10 Power Supply Recommendations

The OPA2156 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

> **注意**
>
> Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 50, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

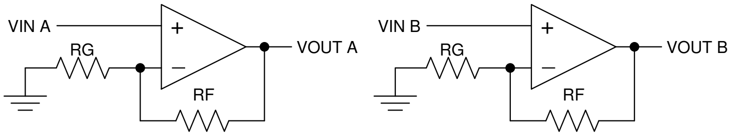
11.1.1 Power Dissipation

The OPA2156 op amp is capable of driving a variety of loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages and/or high output currents. Copper leadframe construction used in the OPA2156 improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

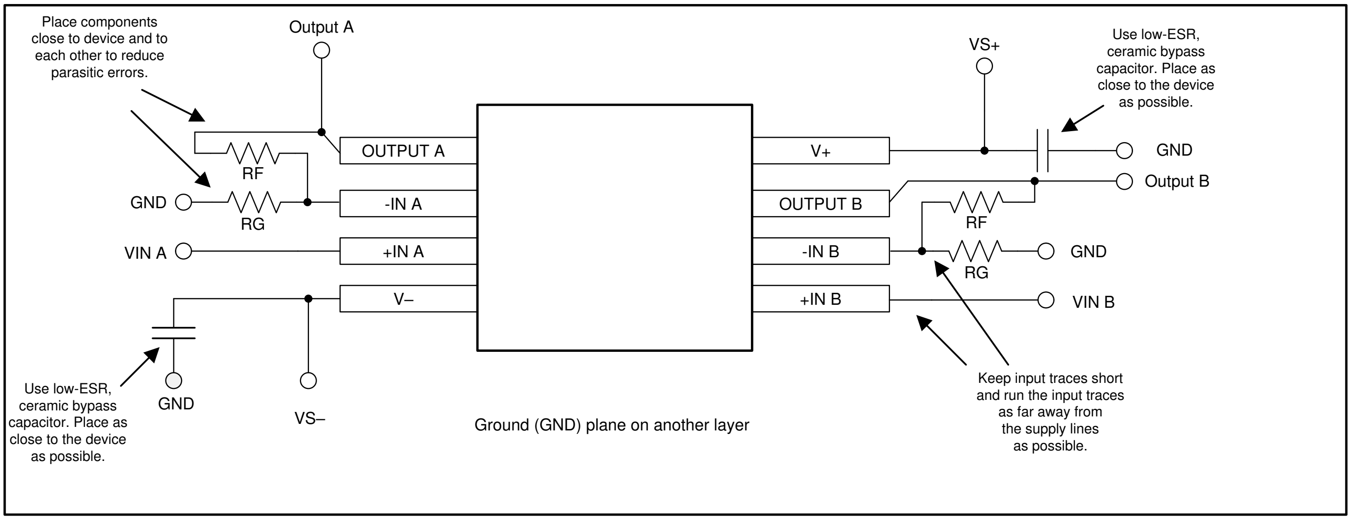
Layout Guidelines (continued)

The OPA2156 has an internal thermal protection feature which prevents it from being damaged due to self heating, or the internal heating generated during normal operation. The protection circuitry works by monitoring the temperature of the output stage and turns of the output drive if the junction temperature of the device rises to approximately 170°C. The device has a thermal hysteresis of approximately 15°C, which allows the device to safely cool down before returning to normal operation at approximately 155°C. TI recommends that the system design takes into account the thermal dissipation of the OPA2156 to ensure that the recommended operating junction temperature of 125°C is not exceeded to avoid decreasing the lifespan of the device or permanently damaging the amplifier.

11.2 Layout Example



(Schematic Representation)



Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Ground (GND) plane on another layer

Keep input traces short and run the input traces as far away from the supply lines as possible.

図 50. Operational Amplifier Board Layout for Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。無料のTINA-TIソフトウェアは、TINA-TIフォルダ(http://www.tij.co.jp/tool/jp/tina-ti)からダウンロードできます。

12.1.1.2 TI Precision Designs

TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

12.2 ドキュメントのサポート

12.2.1 関連資料

- テキサス・インスツルメンツ、*『オペアンプのEMI除去率』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『0-1A, Single-Supply, Low-Side, Current Sensing Solution』*リファレンス・デザイン (英語)
- テキサス・インスツルメンツ、*『Op Amps for Everyone』*デザイン・リファレンス (英語)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商標

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2156ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

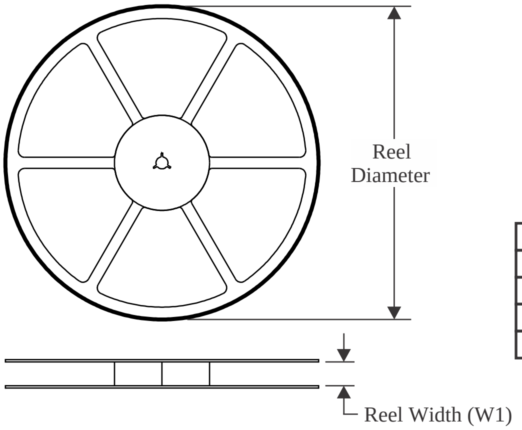
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

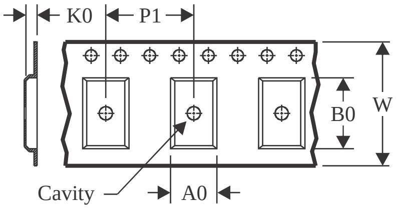
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

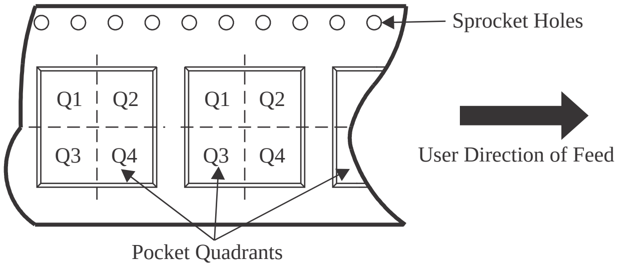


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

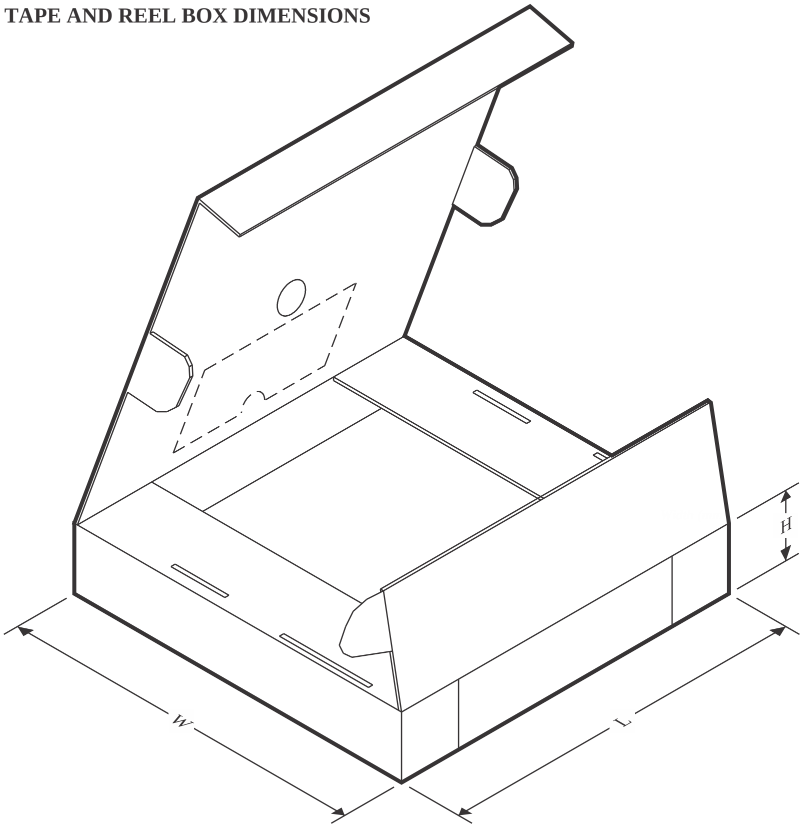
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2156IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2156IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2156IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2156IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2156IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

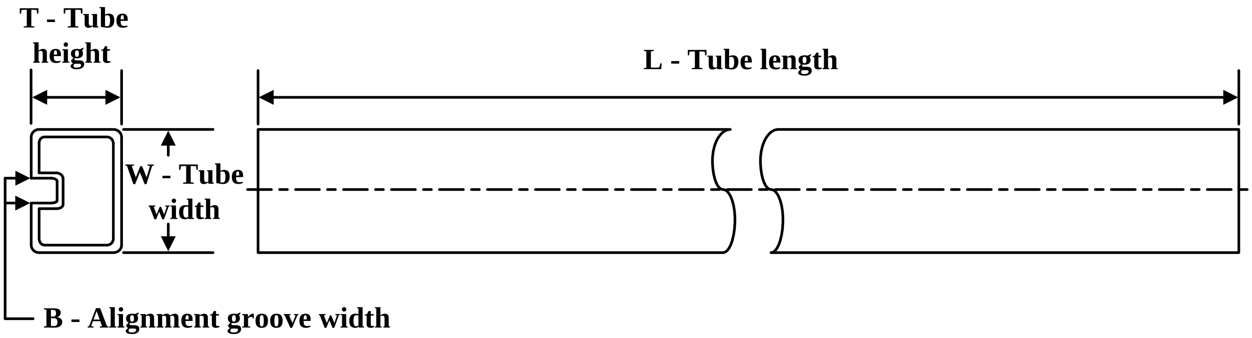
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

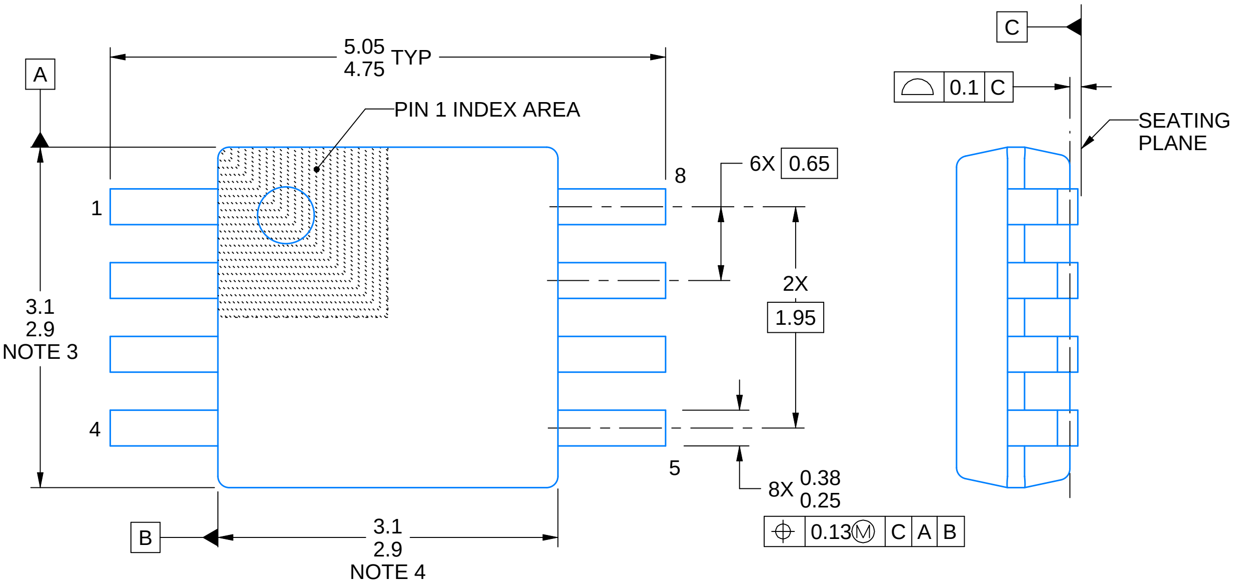
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2156IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2156IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2156IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2156IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2156IDR	SOIC	D	8	2500	353.0	353.0	32.0

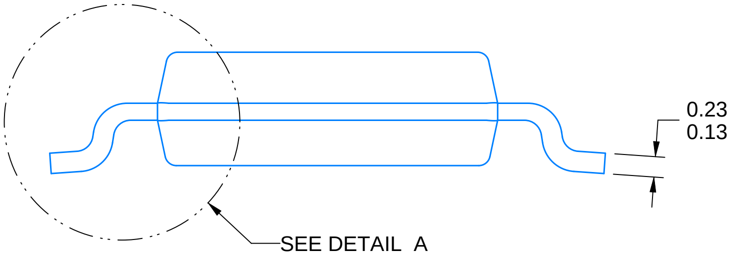
TUBE

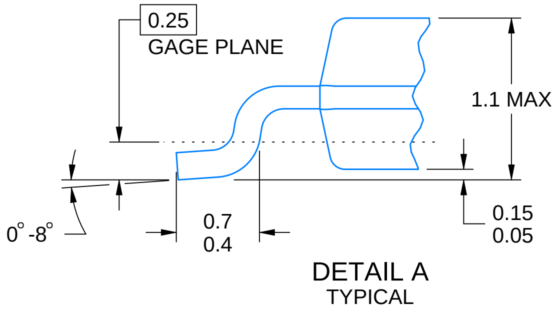


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2156ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156ID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156IDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156IDG4.A	D	SOIC	8	75	506.6	8	3940	4.32





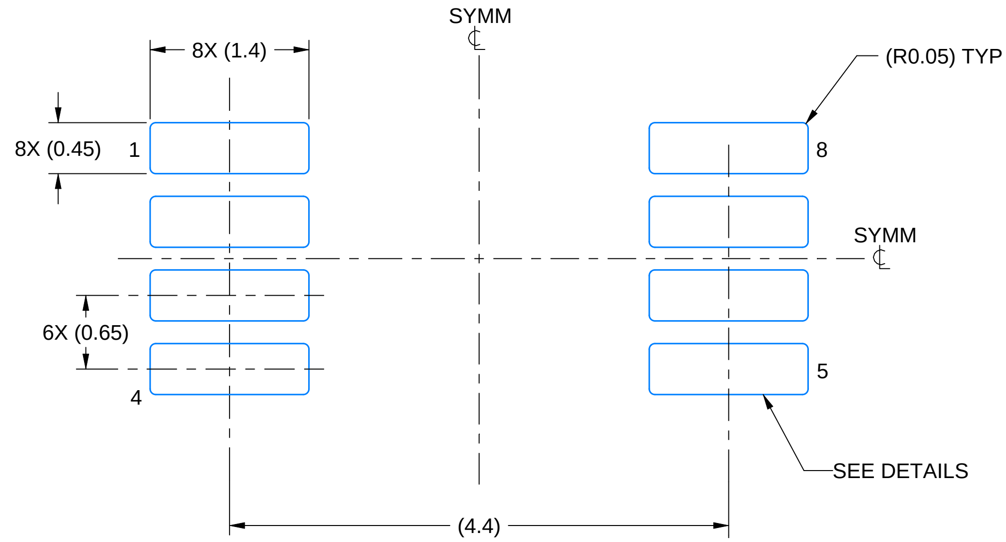


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

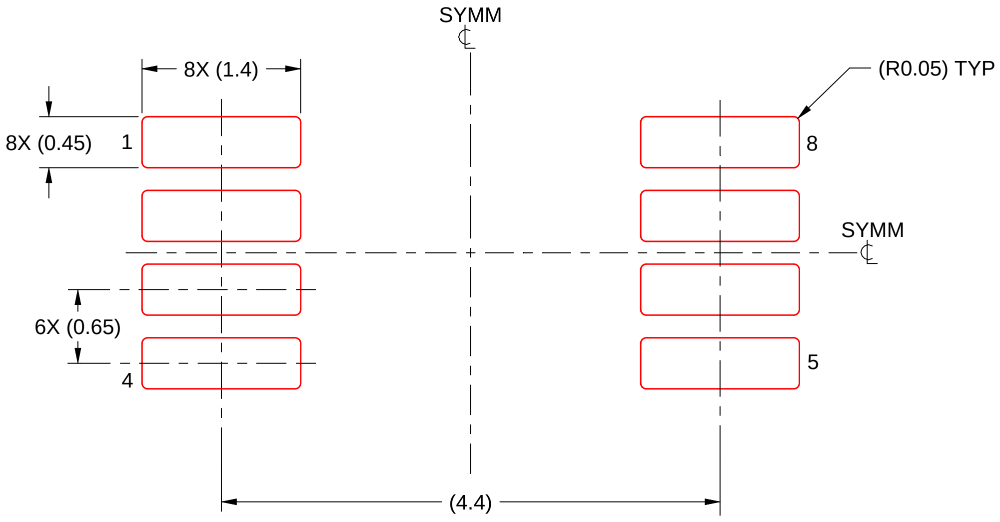
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

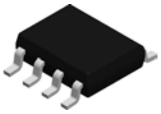
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

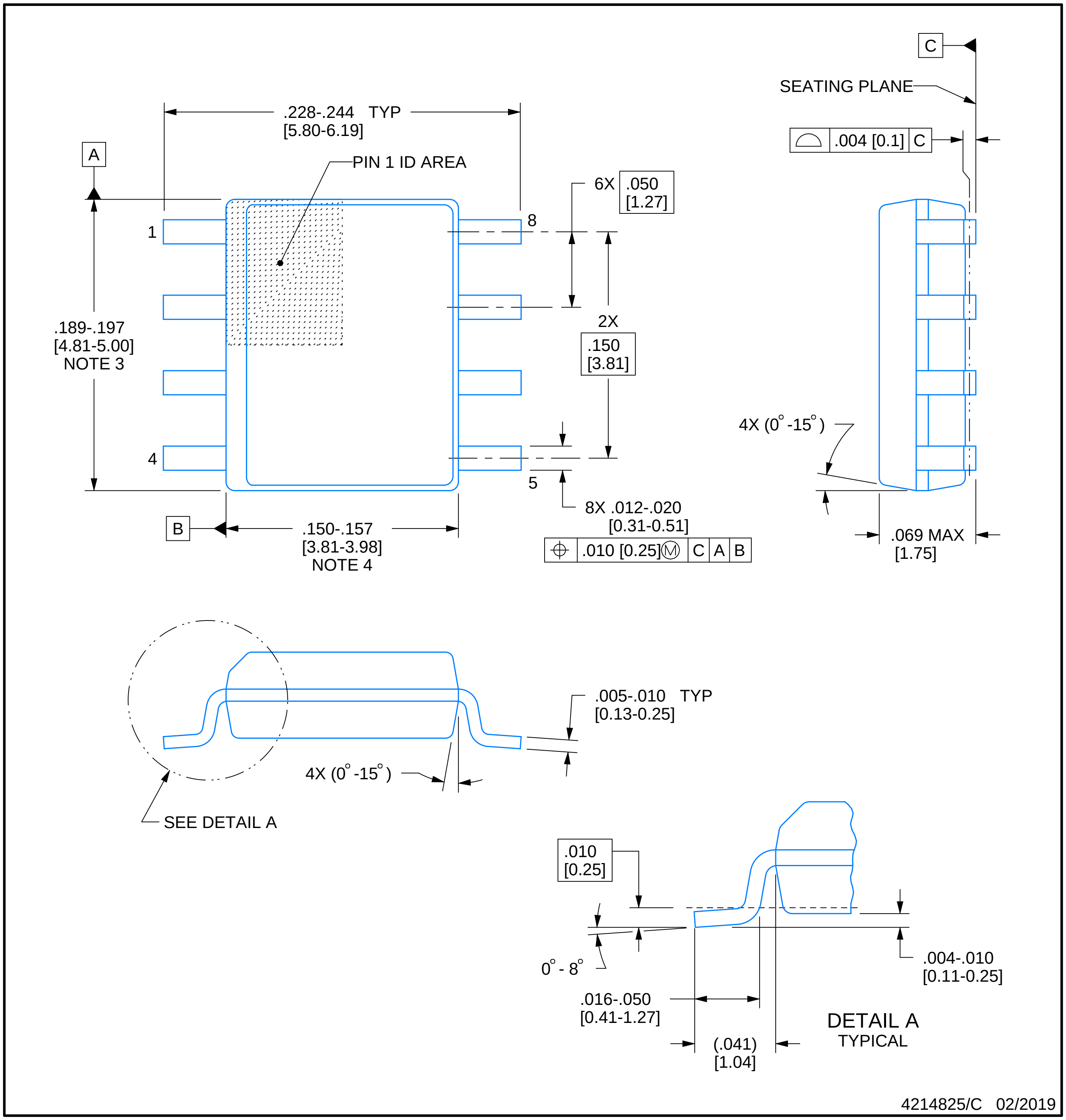


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

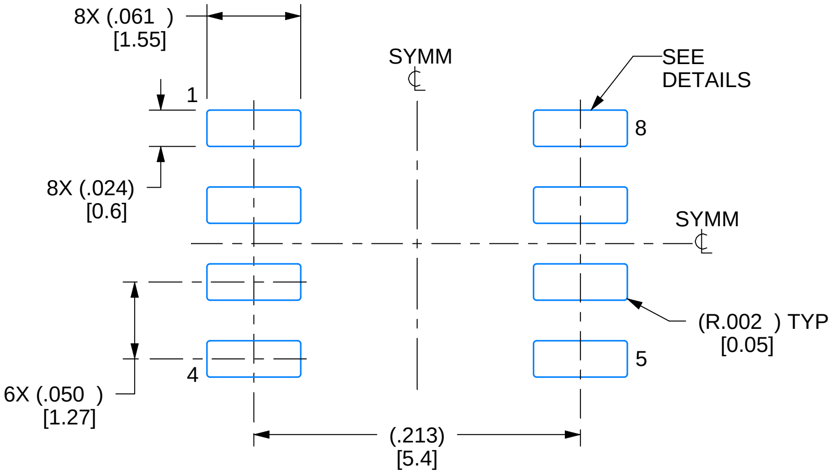
SMALL OUTLINE INTEGRATED CIRCUIT



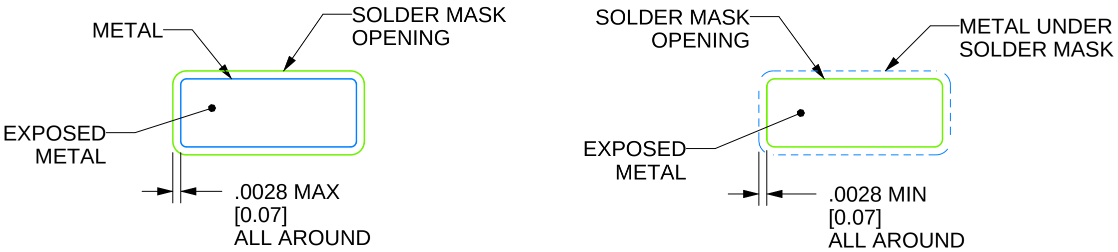
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



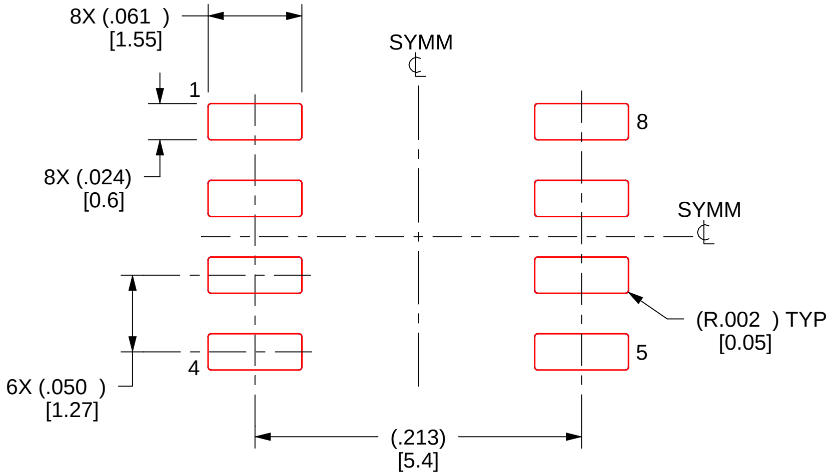
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265