TEXAS INSTRUMENTS
OPA189, OPA2189, OPA4189
JAJSE34I – SEPTEMBER 2017 – REVISED OCTOBER 2021

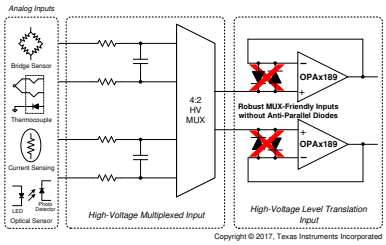
OPAx189 高精度、最低ノイズ、36V、ゼロドリフト、14MHz、MUX フレンドリ、レール・ツー・レール出力オペアンプ

1 特長

- 非常に高い精度
  - ゼロドリフト:0.005μV/℃ (OPA189)
  - 非常に小さいオフセット電圧:3μV 以下 (OPA189)
- 非常に優れた DC 精度
  - CMRR:168dB
  - 開ループ・ゲイン:170dB
- 低ノイズ
  - 1kHz での e_n:5.2nV/$\sqrt{Hz}$
  - 0.1Hz～10Hz のノイズ:0.1μV_{PP}
- 非常に優れた動的性能
  - ゲイン帯域幅:14MHz
  - スルーレート:20V/μs
  - 高速セトリング:10V ステップ、0.01% まで 1.1μs
- 堅牢性の高い設計
  - MUX フレンドリな入力
  - 入力の RFI/EMI フィルタ処理
- 広い電源電圧範囲:4.5V～36V
- 静止電流:1.7mA 以下
- レール・ツー・レール出力
- 入力に負のレールも含む

2 アプリケーション

- バッテリ試験装置
- アナログ入力モジュール
- 重量計
- DC 電源、AC 電源、電子負荷
- マルチファンクション・リレー



OPAx189 は、スイッチまたは多重化されたアプリケーションで、R-C セトリング性能を保持する

3 概要

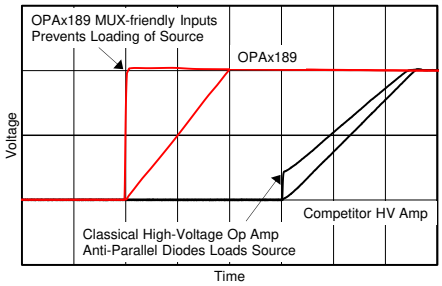
OPA189、OPA2189、OPA4189 (OPAx189) 高精度オペアンプは、非常にノイズが低くセトリングが高速なゼロドリフトのデバイスで、レール・ツー・レール出力動作を行い、独自の MUX フレンドリなアーキテクチャと、制御されたスタートアップ・システムが採用されています。これらの機能と、非常に優れた AC 性能、およびオフセット電圧がわずか 0.4μV、シングル・チャネル・バージョンでは温度範囲にわたってドリフト係数が 0.005μV/℃であることから、OPAx189 は高精度の計測機器、信号測定、およびアクティブ・フィルタ処理アプリケーションに最適です。さらに、MUX フレンドリな入力アーキテクチャにより、大きな入力差動電圧を印加するときに突入電流が防止され、マルチ・チャネル・システムでセトリング性能が改善され、同時に輸送時、取り扱い時、組み立て時における堅牢な ESD 保護が行われます。

どのバージョンも、–40℃～+125℃で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
OPA189	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (5)	2.90mm × 1.60mm
	VSSOP (8)	3.00mm × 3.00mm
OPA2189	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm
OPA4189	TSSOP (14)	5.00mm × 4.40mm
	SOIC (14)	8.65mm × 3.91mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



OPAx189 の MUX フレンドリ入力はスイッチ時に迅速にセトリングし、高い入力インピーダンスを維持する

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- OPA4189 を事前情報 (プレビュー) から量産データ (アクティブ) に変更.....1

Changes from Revision G (April 2021) to Revision H (August 2021) — **Page**

- OPA4189 (SOIC-14 (D) パッケージ) を事前情報 (プレビュー) として追加.....1
- Changed OPA4189IPW thermal information to final values.....8

Changes from Revision F (July 2020) to Revision G (April 2021) — **Page**

- OPA4189 (TSSOP-14 (PW) パッケージ) を事前情報 (プレビュー) として追加.....1

Changes from Revision E (May 2019) to Revision F (July 2020) — **Page**

- OPA2189 の VSSOP-8 (DGK) パッケージをプレビューから量産データ (アクティブ) に変更.....1
- Added Added input offset for OPA2189IDGK.....9
- Added Added input offset drift for OPA2189IDGK.....9

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- Changed Figure 3, *Input Bias Current Production Distribution*, to show updated data.....12
- Changed Figure 4, *Input Offset Current Production Distribution*, to show updated data.....12
- Changed Figure 8, *Open-Loop Gain and Phase vs Frequency*, for clarity.....12
- Changed Figure 9, *Closed-Loop Gain vs Frequency*, for clarity.....12
- Added new Figure 39, *OPA2189 Long-Term Drift*.....12

Changes from Revision C (October 2018) to Revision D (November 2018) — **Page**

- OPA2189 の SOIC (D) パッケージをプレビューから量産データに変更.....1
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- Added crosstalk for OPA2189ID....9
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- OPA189IDGK の量産データシートの初版リリース....1

Changes from Revision A (November 2017) to Revision B (October 2018) **Page**

- Added input offset for OPA2189ID....9
- Added input offset drift for OPA2189ID....9

Changes from Revision * (September 2017) to Revision A (October 2017) **Page**

- OPA189ID デバイスの量産データシートの初版リリース....1

5 Device Comparison Table

PRODUCT	FEATURES
OPA188	25-μV, 0.085-μV/°C, 8.8-nV/√Hz, Rail-to-Rail Output, 36-V, Zero-Drift CMOS
OPA388	5-μV, 0.05-μV/°C, 7-nV/√Hz, 10-MHz, *True* Rail-to-Rail Input/Output, 5.5-V, Zero-Drift CMOS
OPA333	10-μV, 0.05-μV/°C, 25-μA, Rail-to-Rail Input/Output, 5.5-V, Zero-Drift CMOS
OPA192	25-μV, 0.8-μV/°C, 1-mA, 10-MHz, Rail-to-Rail Input/Output, 36-V, e-Trim CMOS
OPA140	120-μV, 10-MHz, 5.1-nV/√Hz, 36-V JFET Input Industrial Op Amp
OPA209	2.2-nV/√Hz, 150-μV, 18-MHz, 36-V Bipolar Op Amp in SOT-23 package

6 Pin Configuration and Functions

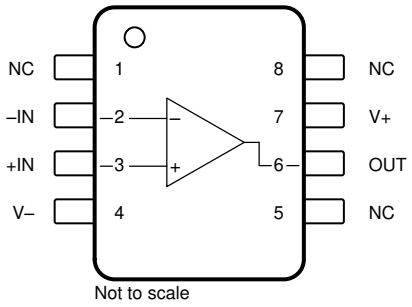

図 6-1. OPA189 D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

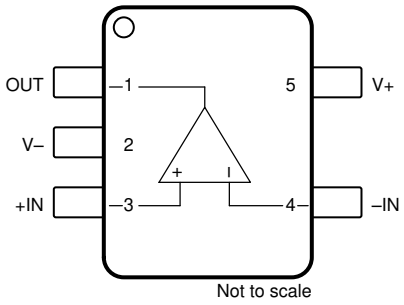

図 6-2. OPA189 DBV (5-Pin SOT-23) Package, Top View

表 6-1. Pin Functions: OPA189

PIN			I/O	DESCRIPTION
NAME	D (SOIC) DGK (VSSOP)	DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

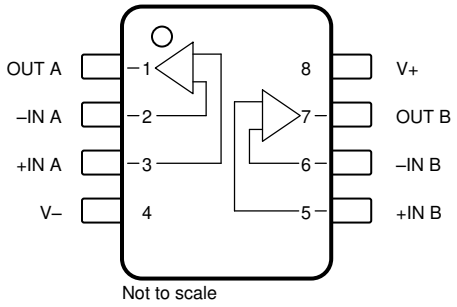

図 6-3. OPA2189 D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

表 6-2. Pin Functions: OPA2189

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

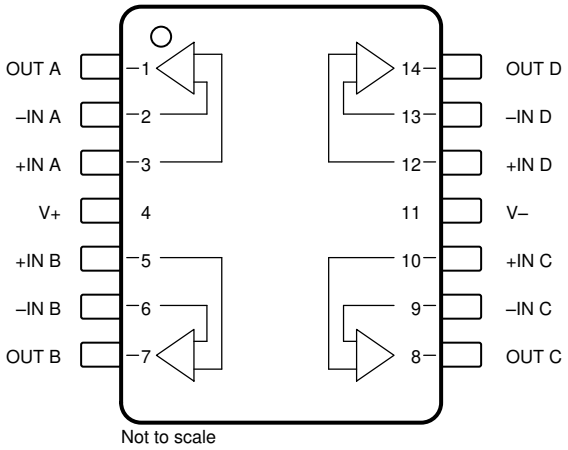

図 6-4. OPA4189 D (14-Pin SOIC) and PW (14-Pin TSSOP) Packages, Top View

表 6-3. Pin Functions: OPA4189

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
–IN C	9	I	Inverting input channel C
+IN C	10	I	Noninverting input channel C
–IN D	13	I	Inverting input channel D
+IN D	12	I	Noninverting input channel D
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
OUT C	8	O	Output channel C
OUT D	14	O	Output channel D
V–	11	—	Negative supply
V+	4	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)	Single-supply		40	V
		Dual-supply		±20	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous	Continuous	
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	4.5		36	V
	Dual-supply	±2.25		±18	
Specified temperature		–40		125	°C

7.4 Thermal Information: OPA189

THERMAL METRIC[1]		OPA189			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT)	
		8 PINS	8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.0	166.4	134.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.6	54.2	90.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.3	87.9	41.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.7	5.5	22.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.2	86.4	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Thermal Information: OPA2189

THERMAL METRIC[1]		OPA2189		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.7	150.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	71.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.7	70	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Thermal Information: OPA4189

THERMAL METRIC[1]		OPA4189		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.4	106.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.0	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	52.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.5	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.8	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.7 Electrical Characteristics

at T_A = 25°C, V_S = ±18V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage, OPA189				±0.4	±3	µV
		T_A = –40°C to 125°C				±4	µV
	Input offset voltage, OPA2189IDGK & OPA4189IPW	V_S = ±2.25V			±0.5	±3	µV
		V_S = ±18V			±0.8	±5	µV
		T_A = –40°C to 125°C, V_S = ±18V				±8	µV
	Input offset voltage, OPA2189ID				±1.5	±5	µV
		T_A = –40°C to 125°C				±8	µV
dV_{OS}/dT	Input offset voltage drift, OPA189	T_A = –40°C to 125°C			±0.005	±0.02	µV/°C
	Input offset voltage drift, OPA2189IDGK & OPA4189IPW	T_A = 0°C to 85°C			±0.006	±0.015	µV/°C
		T_A = -40°C to 125°C			±0.01	±0.03	µV/°C
	Input offset voltage drift, OPA2189ID	T_A = 0°C to 85°C			±0.007	±0.03	µV/°C
		T_A = –40°C to 125°C			±0.01	±0.05	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C			±0.005	±0.05	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current, OPA189	Z_{IN} = 100 kΩ || 500 pF			±70	±300	pA
			T_A = 0°C to 85°C			±1	nA
			T_A = –40°C to 125°C			±10	nA
	Input bias current, OPA2189				±70	±300	pA
			T_A = 0°C to 85°C			±1.5	nA
			T_A = –40°C to 125°C			±10	nA
	Input bias current, OPA4189				±70	±500	pA
			T_A = 0°C to 85°C			±2	nA
			T_A = –40°C to 125°C			±15	nA
I_{OS}	Input offset current, OPA189	Z_{IN} = 100 kΩ || 500 pF			±140	±600	pA
			T_A = 0°C to 85°C			±1.6	nA
			T_A = –40°C to 125°C			±3	nA
	Input offset current, OPA2189				±140	±600	pA
			T_A = 0°C to 85°C			±2.5	nA
			T_A = –40°C to 125°C			±5	nA
	Input offset current, OPA4189				±140	±1	pA
			T_A = 0°C to 85°C			±2.5	nA
			T_A = –40°C to 125°C			±5	nA
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			17		nV_{RMS}
					0.1		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			5.2		nV/√Hz
		f = 100 Hz			5.2		nV/√Hz
		f = 1 kHz			5.2		nV/√Hz
		f = 10 kHz			5.2		nV/√Hz
i_n	Input current noise density	f = 1 kHz			165		fA/√Hz

7.7 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 2.5	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V	V_S = ±2.25 V	120	140		dB
			V_S = ±18 V	146	168		
		(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V, T_A = –40°C to 125°C	V_S = ±18 V	120			
			V_S = ±2.25 V	110			
INPUT IMPEDANCE							
z_{id}	Differential input impedance				0.1 || 5.5		GΩ || pF
z_{ic}	Common-mode input impedance				60 || 1.7		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±18 V	(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ	150	170		dB
			(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ, T_A = –40°C to 125°C	140			
			(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ	150	170		
			(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ, T_A = –40°C to 125°C	140			
FREQUENCY RESPONSE							
UGB	Unity-gain Bandwith	A_V = 1			8		MHz
GBW	Gain-bandwith Product	A_V = 1000			14		
SR	Slew rate	G = 1, 10-V step			20		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00006%		
	Crosstalk	OPA2189ID, at dc			150		dB
		OPA2189ID, f = 100 kHz			120		
t_S	Settling time	To 0.1%	V_S = ±18 V, G = 1, 10-V step		0.8		µs
		To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.1		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			320		ns

7.7 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		20	110	
			R_{LOAD} = 2 kΩ		80	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		20	110	
			R_{LOAD} = 2 kΩ		80	500	
		T_A = –40°C to 125°C, both rails, R_{LOAD} = 10 kΩ	OPA189 & OPA2189		20	120	
			OPA4189		20	140	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive	See Small-Signal Overshoot vs Capacitive Load					
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Open-Loop Output Impedance vs Frequency			380		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±2.25 V to ±18 V (V_S = 4.5 V to 36 V)	T_A = 25°C		1.3	1.7	mA
			T_A = –40°C to 125°C			1.8	

7.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

表 7-1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 7-1
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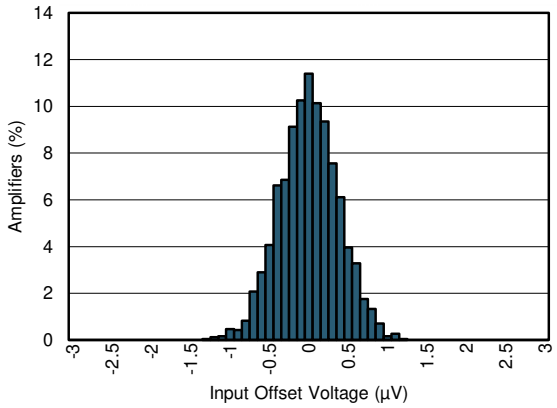
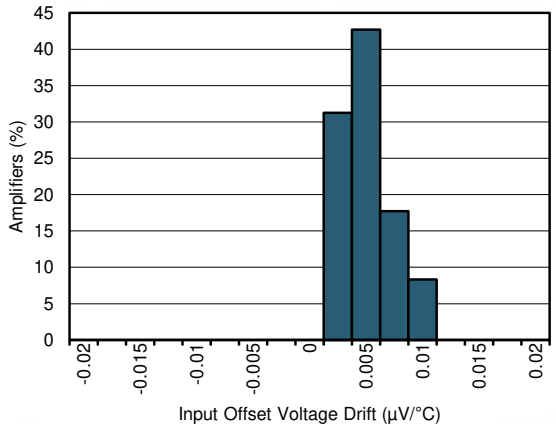
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



µ = 46.67 nV σ = 374.5 nV N = 2554
V_{OS} (maximum) = ±3 µV

図 7-1. Offset Voltage Production Distribution



µ = 2.83 nV/°C σ = 2.78 nV/°C N = 96
dV_{OS} / dT (maximum) = ±0.02 µV/°C

図 7-2. Offset Voltage Drift Distribution

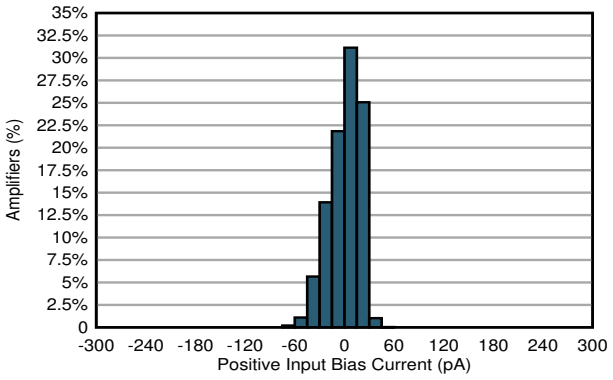


図 7-3. Input Bias Current Production Distribution

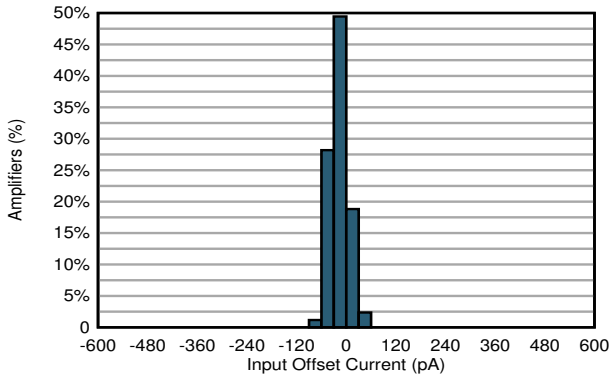
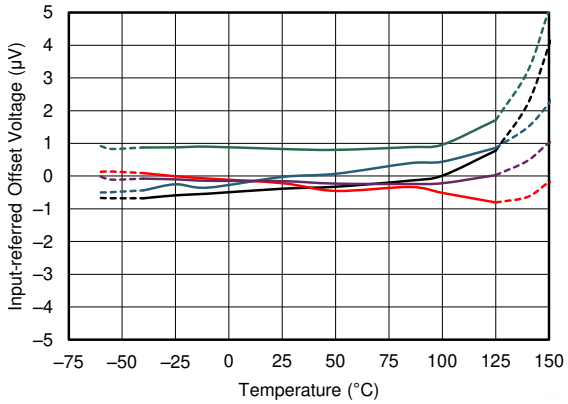
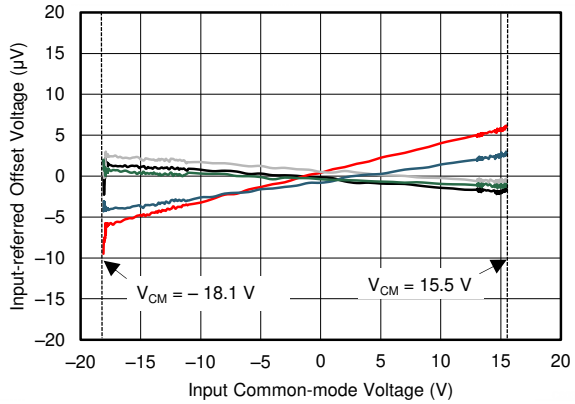


図 7-4. Input Offset Current Production Distribution



5 Typical Units

図 7-5. Offset Voltage vs Temperature

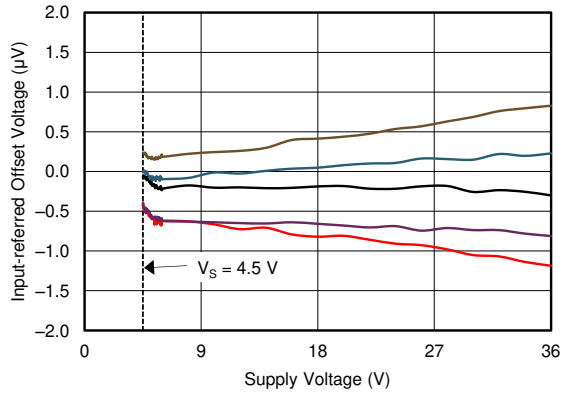


5 Typical Units

図 7-6. Offset Voltage vs Common-Mode Voltage

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



5 Typical Units

図 7-7. Offset Voltage vs Supply Voltage

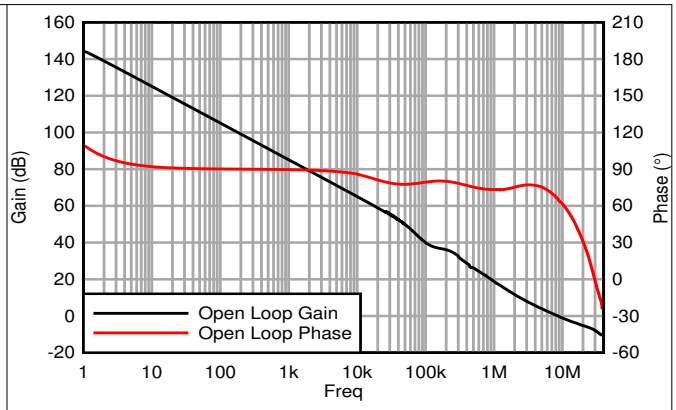


図 7-8. Open-Loop Gain and Phase vs Frequency

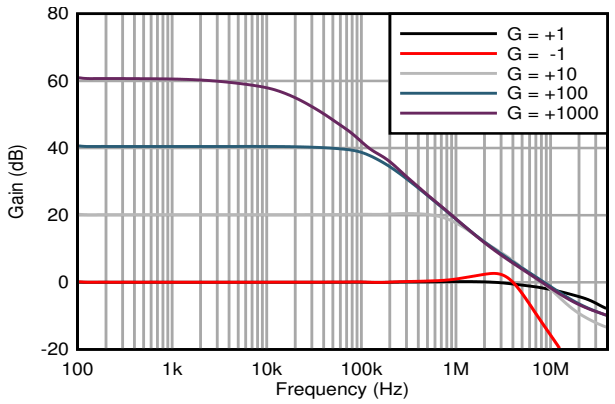


図 7-9. Closed-Loop Gain vs Frequency

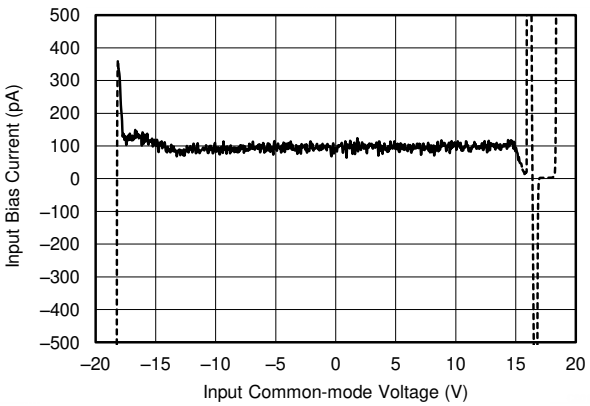


図 7-10. Input Bias Current vs Common-Mode Voltage

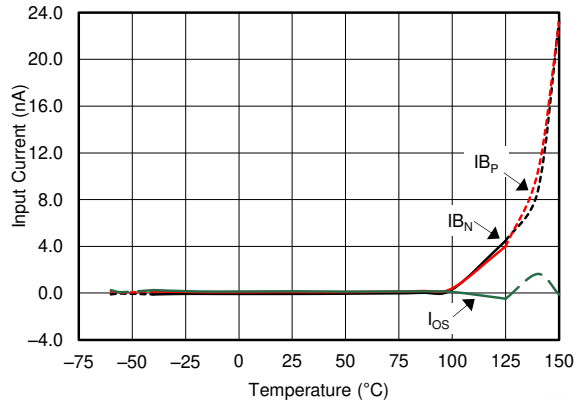
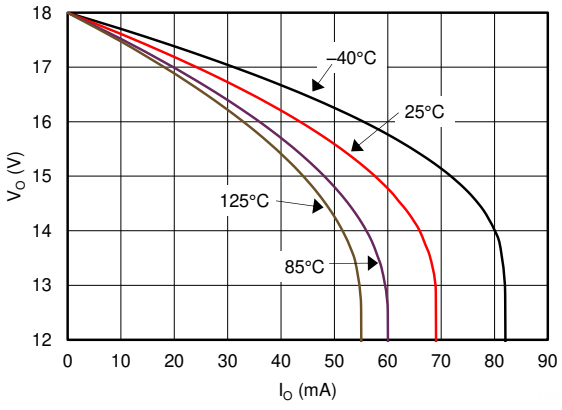


図 7-11. Input Bias Current and Offset vs Temperature

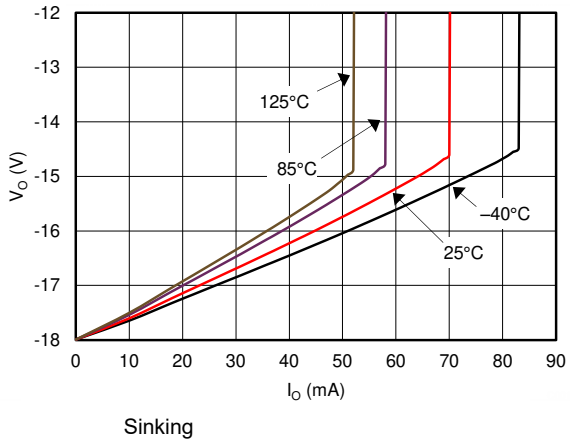


Sourcing

図 7-12. Output Voltage Swing vs Output Current

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



Sinking

図 7-13. Output Voltage Swing vs Output Current

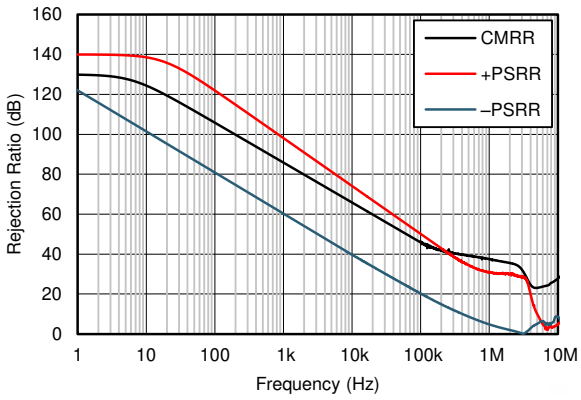


図 7-14. CMRR and PSRR vs Frequency

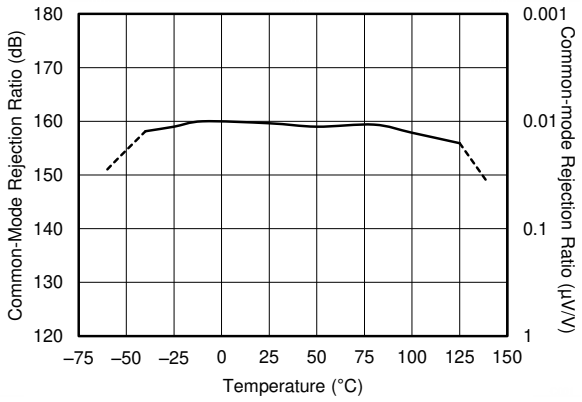


図 7-15. CMRR vs Temperature

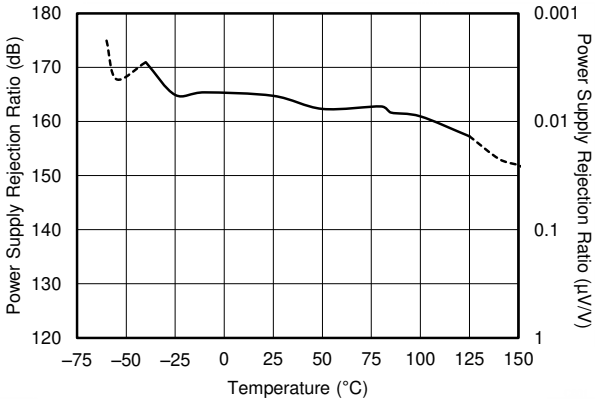


図 7-16. PSRR vs Temperature

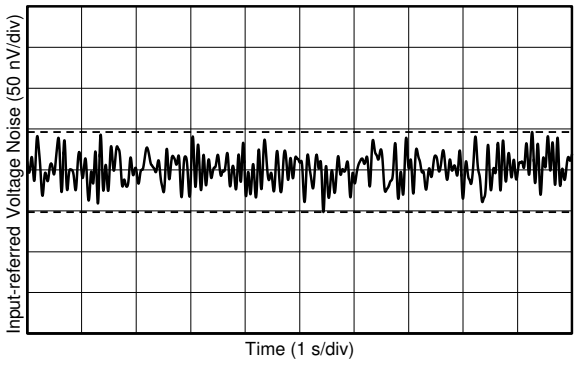


図 7-17. 0.1-Hz to 10-Hz Voltage Noise

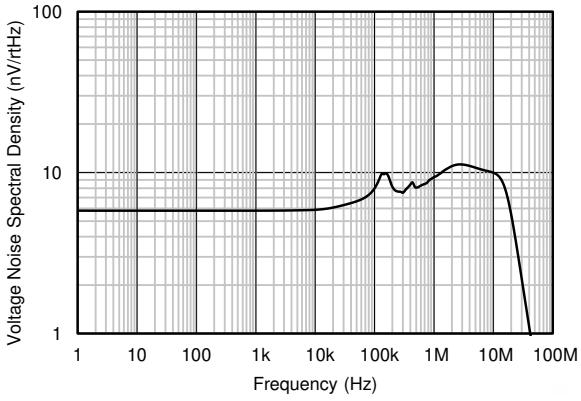
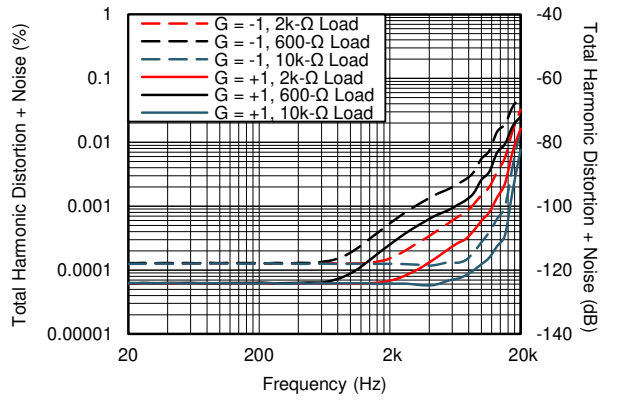


図 7-18. Input Voltage Noise Spectral Density vs Frequency

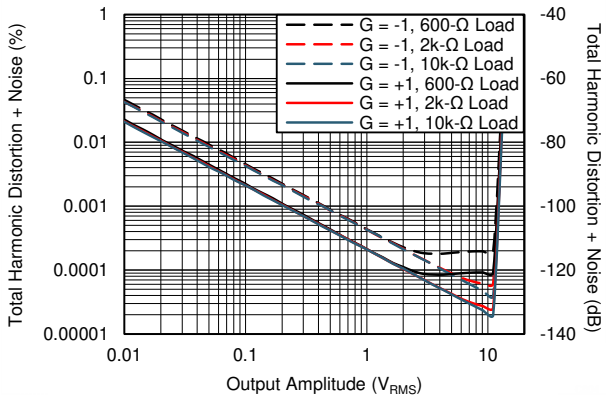
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



V_{OUT} = 3.5 V V_{RMS}, BW = 90 kHz

図 7-19. THD+N Ratio vs Frequency



f = 1 kHz, BW = 90 kHz

図 7-20. THD+N vs Output Amplitude

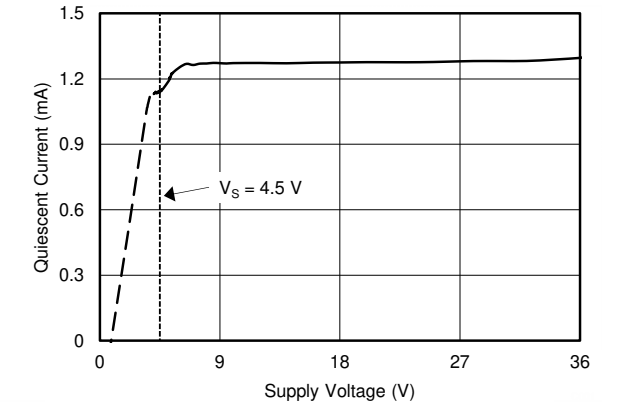


図 7-21. Quiescent Current vs Supply Voltage

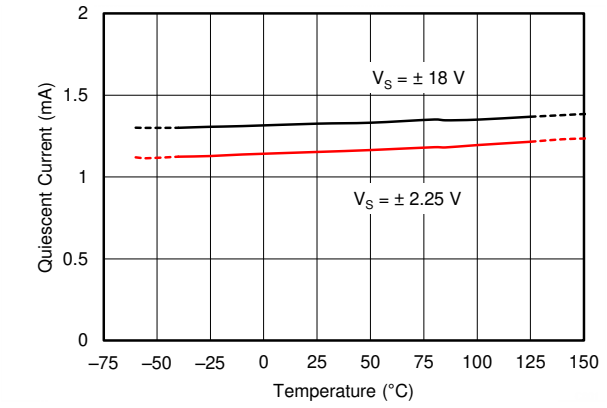
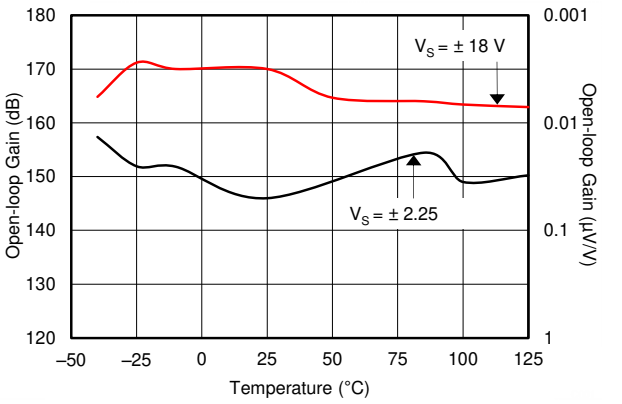
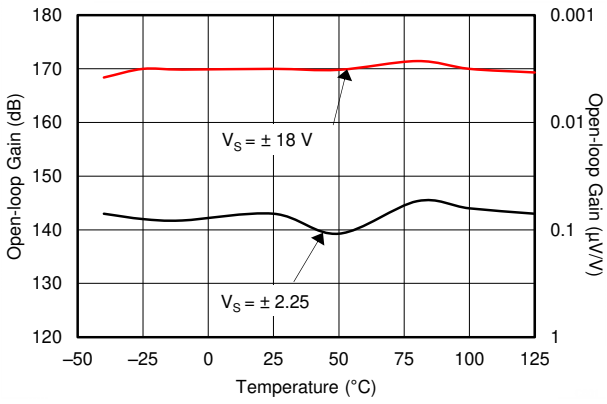


図 7-22. Quiescent Current vs Temperature



10-kΩ Load

図 7-23. Open-Loop Gain vs Temperature



2-kΩ Load

図 7-24. Open-Loop Gain vs Temperature

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

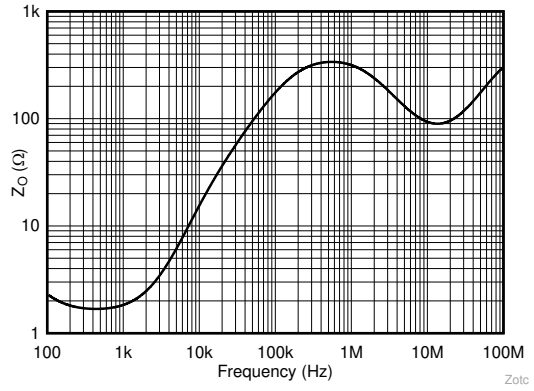
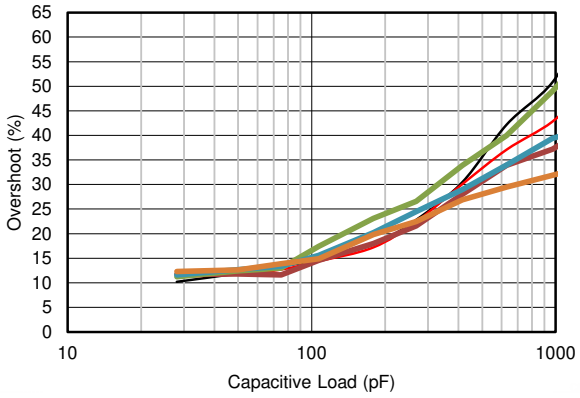


図 7-25. Open-Loop Output Impedance vs Frequency



10-mV Step

図 7-26. Small-Signal Overshoot vs Capacitive Load

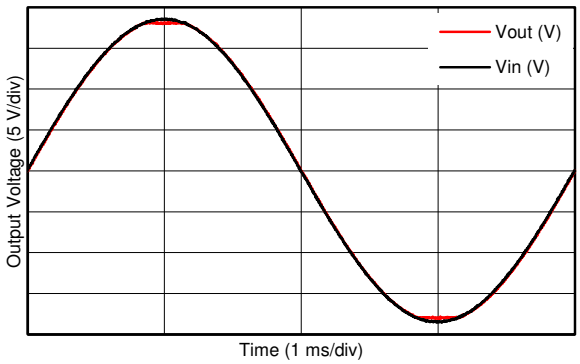


図 7-27. No Phase Reversal

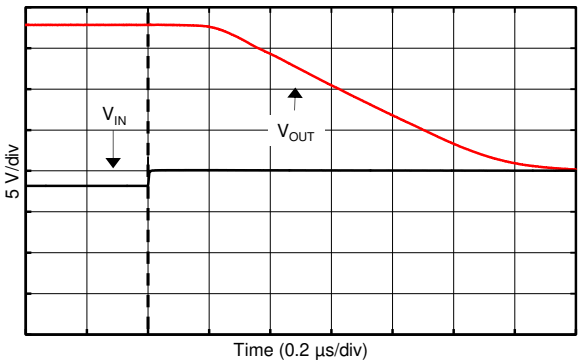


図 7-28. Positive Overload Recovery

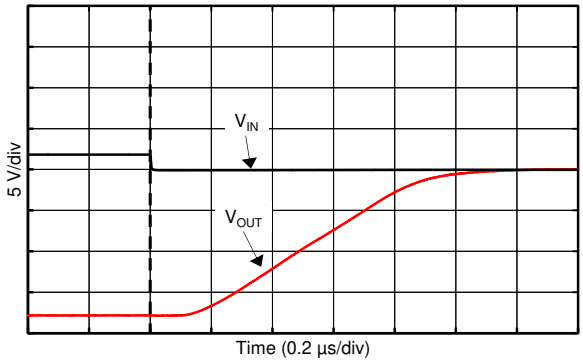
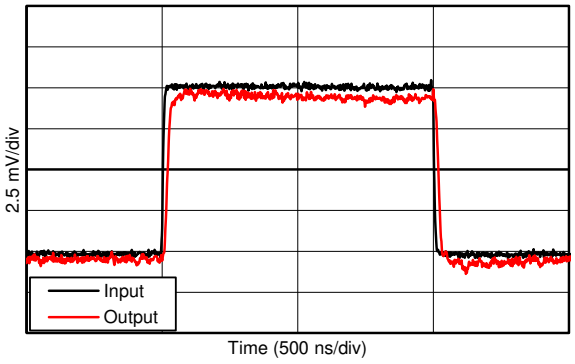


図 7-29. Negative Overload Recovery

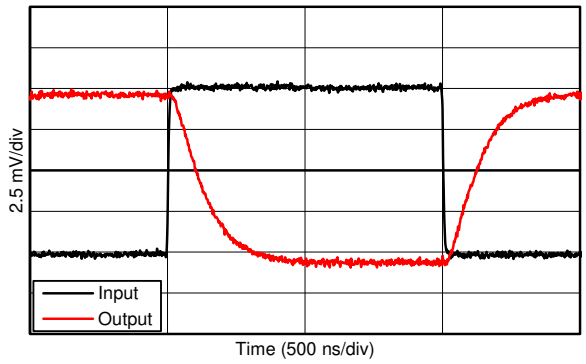


10-mV Step G = +1

図 7-30. Small-Signal Step Response

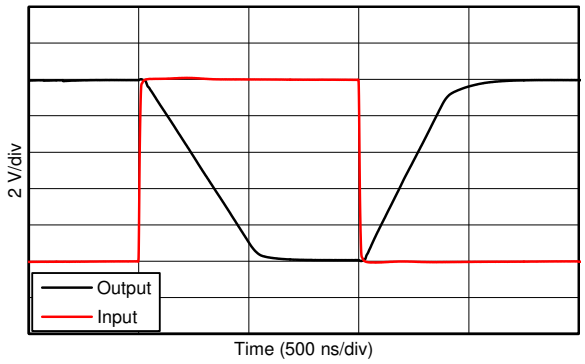
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



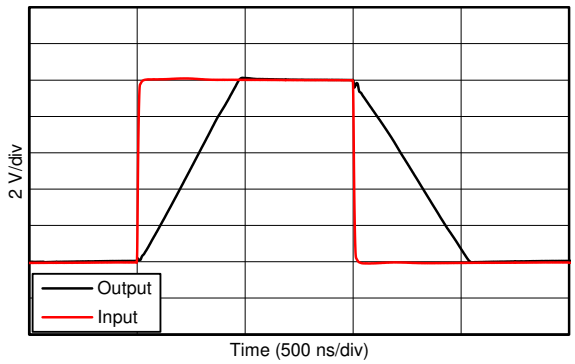
10-mV Step G = –1

図 7-31. Small-Signal Step Response



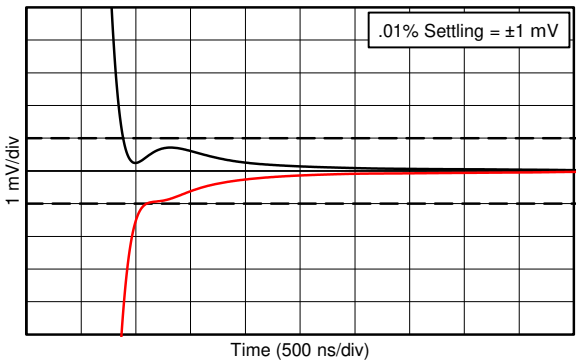
10-V Step G = –1

図 7-32. Large-Signal Step Response



10-V Step G = +1

図 7-33. Large-Signal Step Response



10-V Step

図 7-34. Settling Time

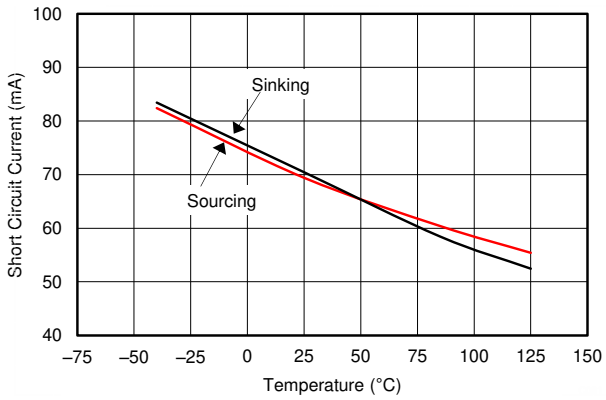


図 7-35. Short-Circuit Current vs Temperature

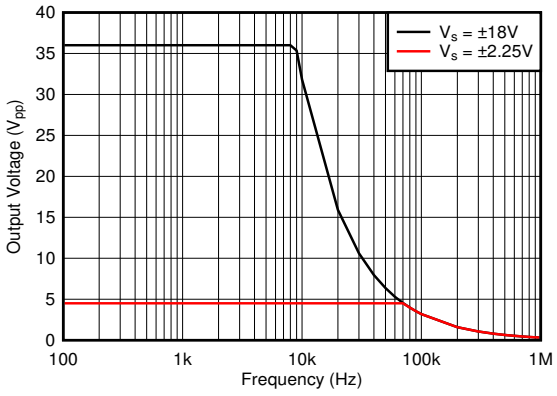
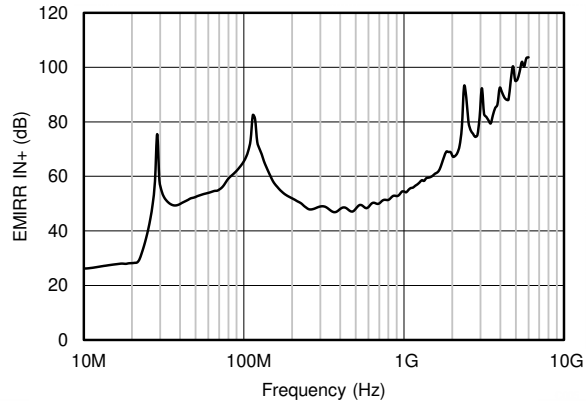


図 7-36. Maximum Output Voltage Amplitude vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



P_{RF} = –10 dBm

図 7-37. EMIRR vs Frequency

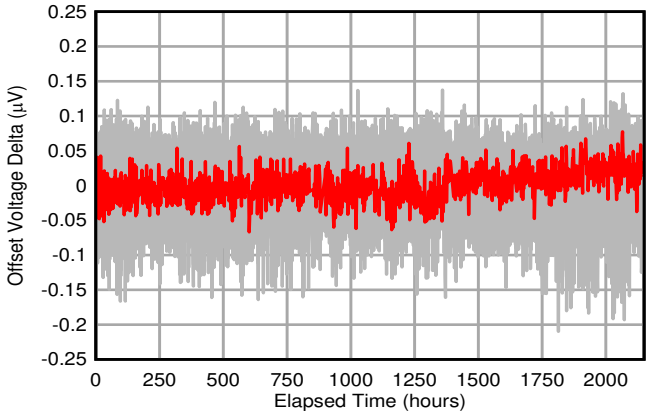


図 7-38. OPA189 Long-Term Drift

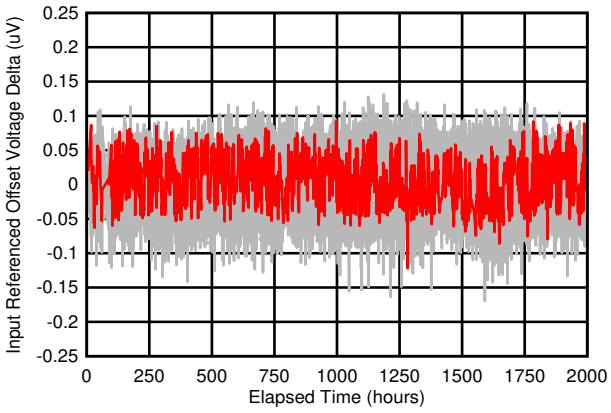


図 7-39. OPA2189 Long-Term Drift

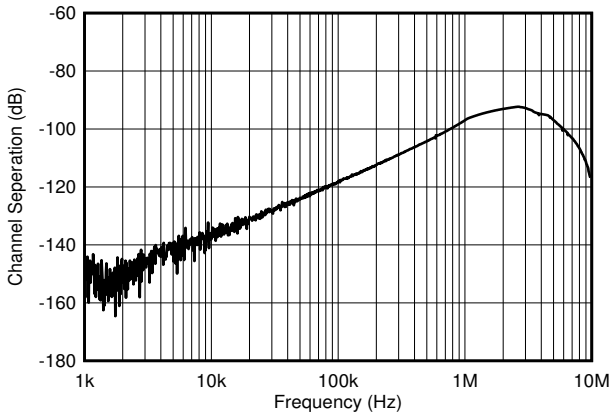


図 7-40. OPA2189 Channel Separation

8 Detailed Description

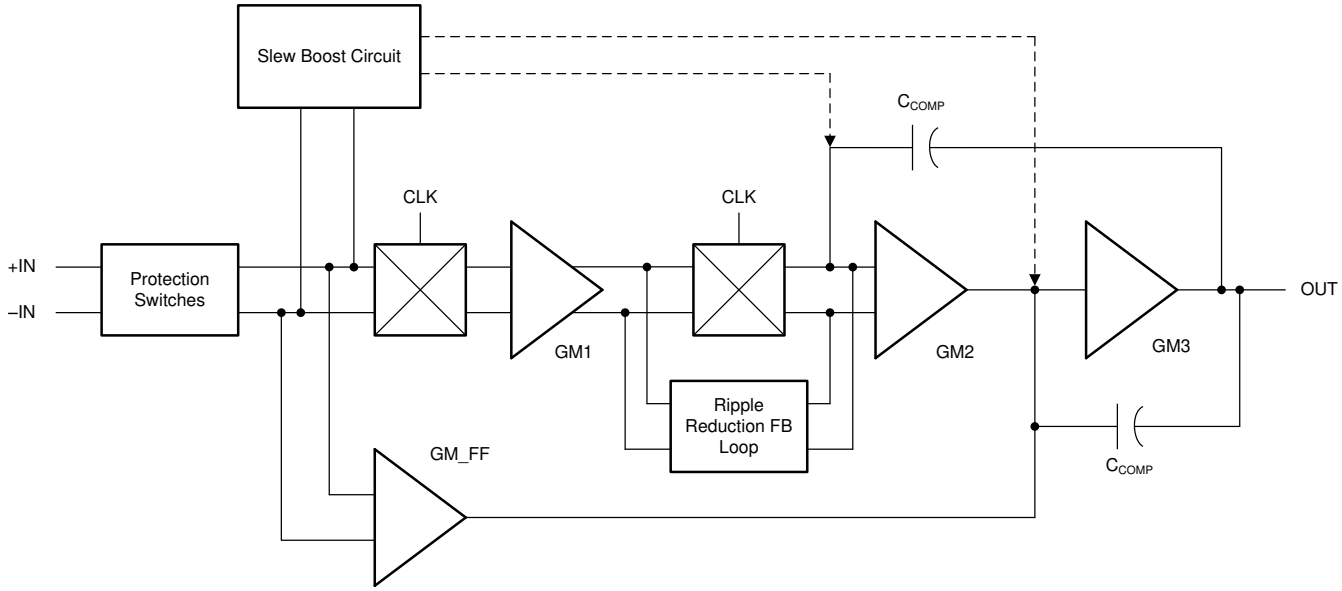
8.1 Overview

The OPAx189 operational amplifiers combine precision offset and drift with excellent overall performance, making these devices an excellent choice for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, these devices offer excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. See the *Layout Guidelines* section for details and layout example.

The OPAx189 are part of a family of zero-drift, MUX-friendly, rail-to-rail output operational amplifiers. These devices operate from 4.5 V to 36 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating below the chopper frequency.

8.2 Functional Block Diagram

The *Functional Block Diagram* shows a representation of the proprietary OPAx189 architecture.



8.3 Feature Description

The OPAx189 series of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; they only require a minimum supply voltage of 4.5 V (±2.25 V). For V_S less than ±2.5 V, the
common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table for details. Key parameters are given over the specified temperature range, T_A = –40°C to +125°C, in the *Electrical Characteristics* table. Key parameters that vary over the supply voltage, temperature range, or frequency are shown in the *Typical Characteristics* section.

The OPAx189 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic autocalibration technique to provide low input offset voltage and very low input offset voltage drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by ensuring they are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 µV/°C or higher, depending on the materials used. See the *Layout Guidelines* section for details and a layout example.

8.3.1 Operating Characteristics

The OPAx189 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.3.2 Phase-Reversal Protection

The OPAx189 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx189 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 図 8-1.

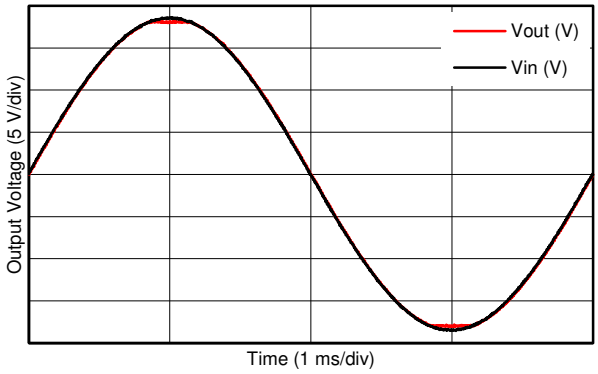


図 8-1. No Phase Reversal

8.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the OPAx189 use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying, however the pulses may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.4 EMI Rejection

The OPAx189 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx189 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 8-2 shows the results of this testing on the OPAx189. 表 8-1 lists the EMIRR +IN values for the OPAx189 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 8-1 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

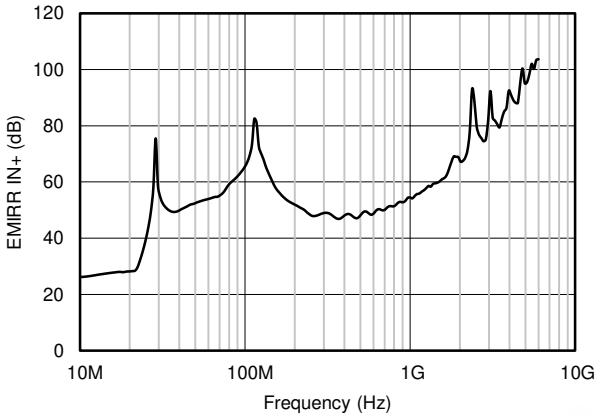


図 8-2. EMIRR Testing

表 8-1. OPAx189 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	69.1 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	88.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	95.5 dB

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this

section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier may result in adverse effects, as the amplifier would not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected DC offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

The EMIRR +IN of the OPAx189 is plotted versus frequency as shown in 図 8-2. If available, any dual and quad op amp device versions have nearly similar EMIRR +IN performance. The OPAx189 unity-gain bandwidth is 14 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

8.3.5 EMIRR +IN Test Configuration

図 8-3 shows the circuit configuration for testing the EMIRR +IN. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The multimeter samples and measures the resulting DC offset voltage. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

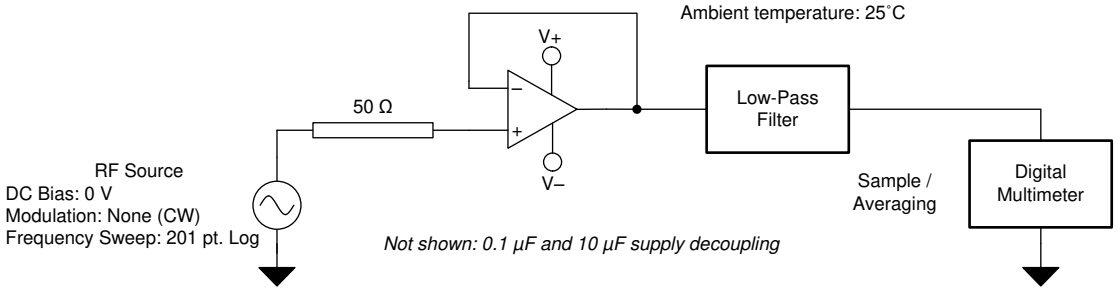
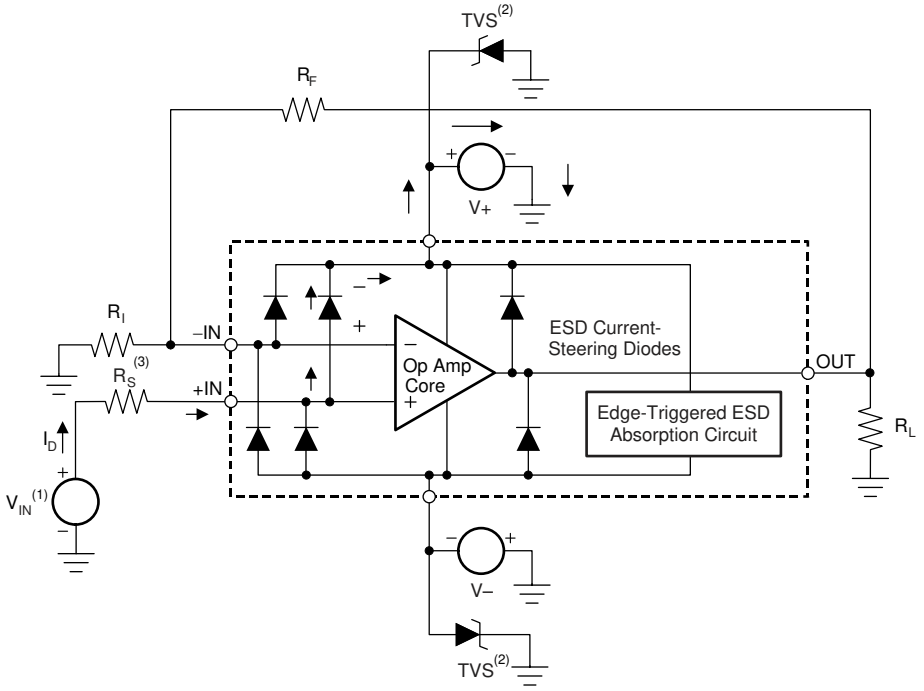


図 8-3. EMIRR +IN Test Configuration

8.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. See 図 8-4 for an illustration of the ESD circuits contained in the OPAx189 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) V_{IN} = V+ + 500 mV.

(2) TVS: 40 V > $V_{TVSBR\ (min)}$ > V+ ; where $V_{TVSBR\ (min)}$ is the minimum specified value for the transient voltage suppressor breakdown voltage.

(3) Suggested value is approximately 5 kΩ in overvoltage conditions.

図 8-4. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger or threshold voltage that is above the normal operating voltage of the OPAx189 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in 図 8-4), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should

this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 8-4 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes must be added to the supply pins, as shown in 図 8-4. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.3.7 MUX-Friendly Inputs

The OPAx189 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature anti-parallel diodes that protect input transistors from large V_{GS} voltages that may exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

OPAx189 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This solves many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. OPAx189 offers outstanding settling performance due to these design innovations and built-in slew rate boost and wide bandwidth. The OPAx189 can also be used as a comparator. Differential and common-mode *Absolute Maximum Ratings* still apply relative to the power supplies.

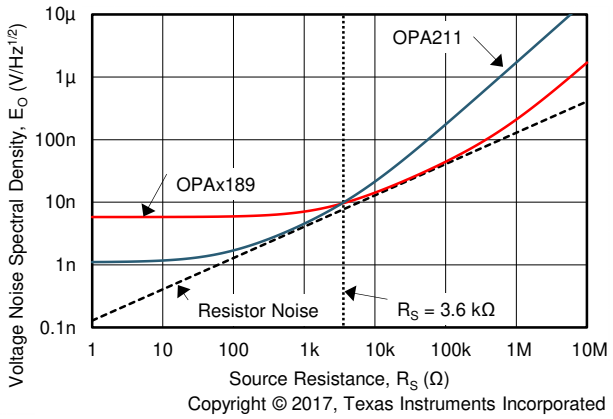
8.3.8 Noise Performance

図 8-5 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPAx189 and OPA211 are shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPAx189 family has both low voltage noise and low current noise because of the CMOS input of the op amp. As a result, the current noise contribution of the OPAx189 series is negligible for any practical source impedance, which makes this device the better choice for applications with high source impedance.

The equation in 図 8-5 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- i_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in kelvins (K)

For more details on calculating noise, see the *Basic Noise Calculations* section.



NOTE: R_S = 3.6 kΩ is indicated in 図 8-5. This is the source impedance above which OPAx189 is a lower noise option than the OPA211.

図 8-5. Noise Performance of the OPAx189 and OPA211 in Unity-Gain Buffer Configuration

8.3.9 Basic Noise Calculations

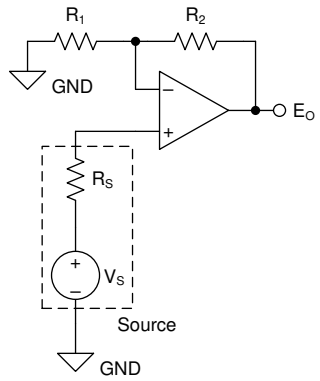
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 図 8-5. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

図 8-6 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx189 means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations. For additional resources on noise calculations visit *TI's Precision Labs Series*

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where:

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

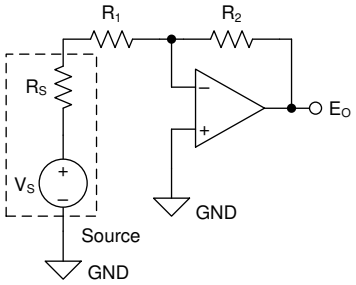
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \text{ || } R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 273.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where:

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \text{ || } R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 273.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

where:

- e_n is the voltage noise spectral density of the amplifier. For the OPAx189 series of operational amplifiers, e_n = 5.2 nV/ $\sqrt{\text{Hz}}$ at 1 kHz.
- i_n is the current noise spectral density of the amplifier. For the OPAx189 series of operational amplifiers, i_n = 165 fA/ $\sqrt{\text{Hz}}$ at 1 kHz.

図 8-6. Noise Calculation in Gain Configurations

8.4 Device Functional Modes

The OPAx189 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx189 is 36 V (±18 V).

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The OPAx189 operational amplifier combines precision offset and drift with excellent overall performance, making the series an excellent for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx189 can be used.

9.2 Typical Applications

9.2.1 25-kHz Low-Pass Filter

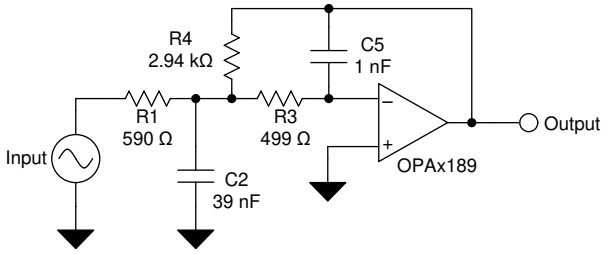


図 9-1. 25-kHz Low-Pass Filter

9.2.1.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx189 devices are designed to construct high-speed, high-precision active filters. 図 9-1 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 図 9-1. Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets the user create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows board-level designers to create, optimize, and simulate complete multistage active filter solutions within minutes.

9.2.1.3 Application Curve

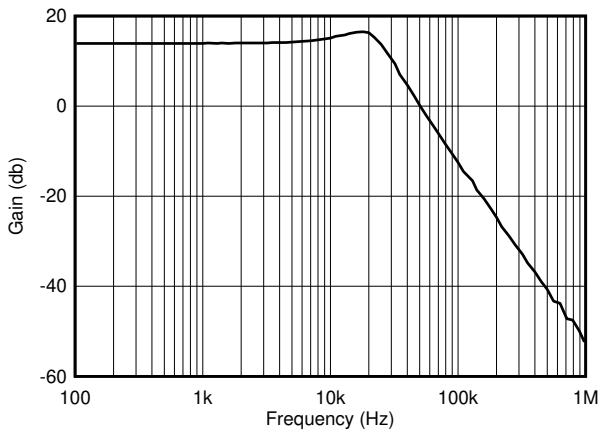


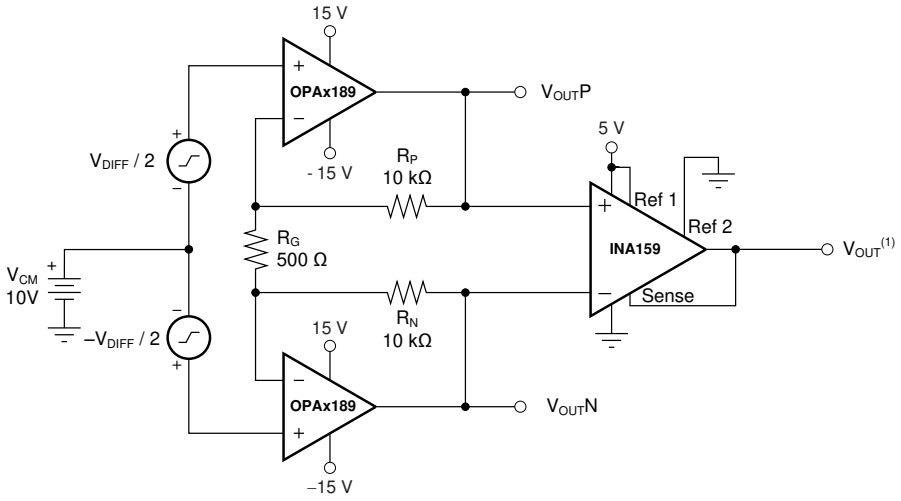
図 9-2. OPAx189 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

Note

The TINA-TI™ software files shown in the following sections require that either the TINA™ software (from DesignSoft™) or TINA-TI simulation software be installed. See セクション 12.1.1.1 for more information.

図 9-3 shows an example of how the OPAx189 is used as a high-voltage, high-impedance front end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to simply interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link download the TINA-TI software file: Discrete INA.



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref 1) / 2$.

図 9-3. Discrete INA + Attenuation for ADC With 3.3-V Supply

9.2.3 Bridge Amplifier

図 9-4 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI software file: Bridge Amplifier Circuit.

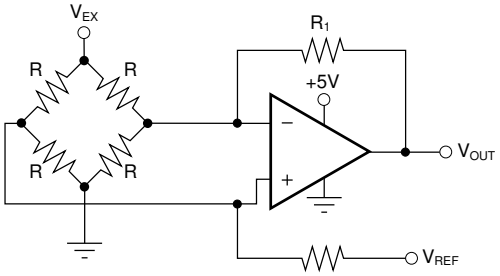


図 9-4. Bridge Amplifier

9.2.4 Low-Side Current Monitor

図 9-5 shows the OPAx189 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPAx189, with a gain of 201. In this example the load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI software file: Current-Sensing Circuit.

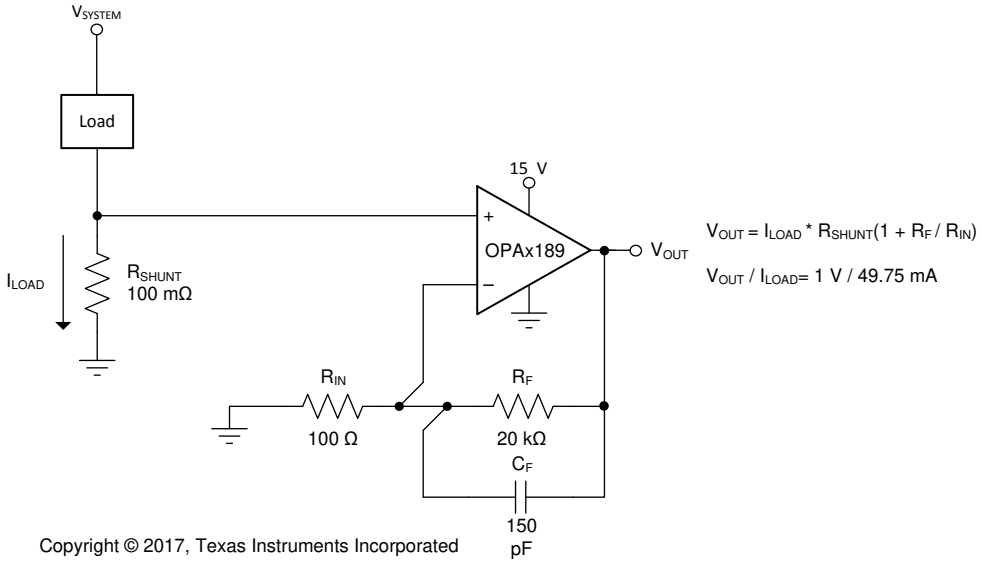


図 9-5. Low-Side Current Monitor

9.2.5 Programmable Power Supply

図 9-6 shows the OPAx189 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPAx189 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI software file: Programmable Power-Supply Circuit.

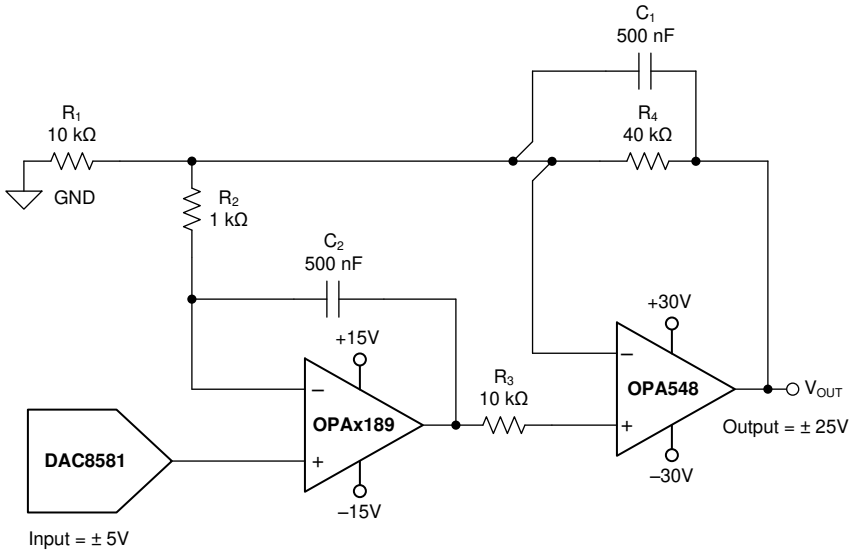
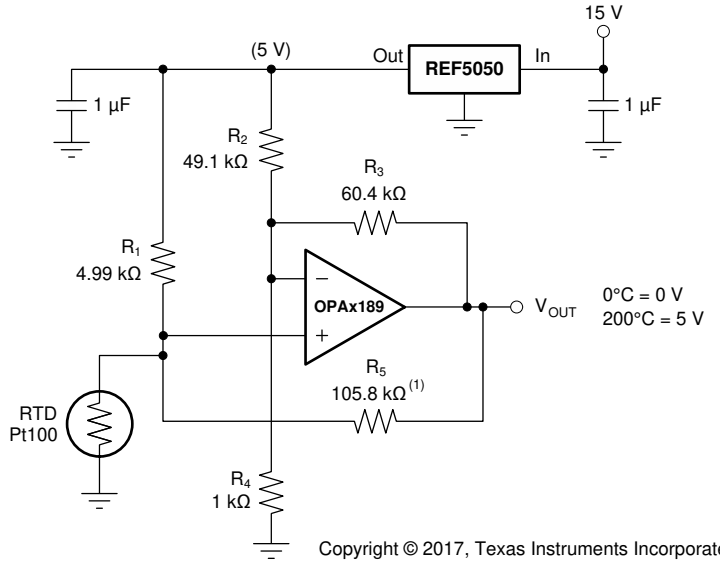


図 9-6. Programmable Power Supply

9.2.6 RTD Amplifier With Linearization

See *Analog Linearization of Resistance Temperature Detectors* for an in-depth analysis of 図 9-7. Click the following link to download the TINA-TI software file: RTD Amplifier with Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

図 9-7. RTD Amplifier With Linearization

9.3 System Examples

9.3.1 24-Bit, Delta-Sigma, Differential Load Cell or Strain Gauge Sensor Signal Conditioning

OPAx189 is used in a 24-bit, differential load cell or strain gauge sensor signal conditioning system alongside the ADS1225. A pair of OPAx189 amplifiers are configured in a two-amp instrumentation amplifier (IA) configuration and are band-limited to reduce noise and allow heavy capacitive drive. The load cell is powered by an excitation voltage (denoted V_{EX}) of 5-V and provides a differential voltage proportional to force applied. The differential voltage can be quite small and both outputs are biased to V_{EX} / 2.

In this example the OPAx189 is employed here due to the excellent input offset voltage (0.4 µV) and input offset voltage drift (0.005 µV/°C), the low broadband noise (5.2 nV/√ Hz) and zero-flicker noise, and excellent linearity and high input impedance. The two-amp IA configuration removes the dc bias and amplifies the differential signal of interest and drives the 24-bit, delta-sigma ADS1225 analog-to-digital converter (ADC) for acquisition and conversion. The ADS1225 features a 100-SPS data rate, single-cycle settling, and simple conversion control with the dedicated START pin.

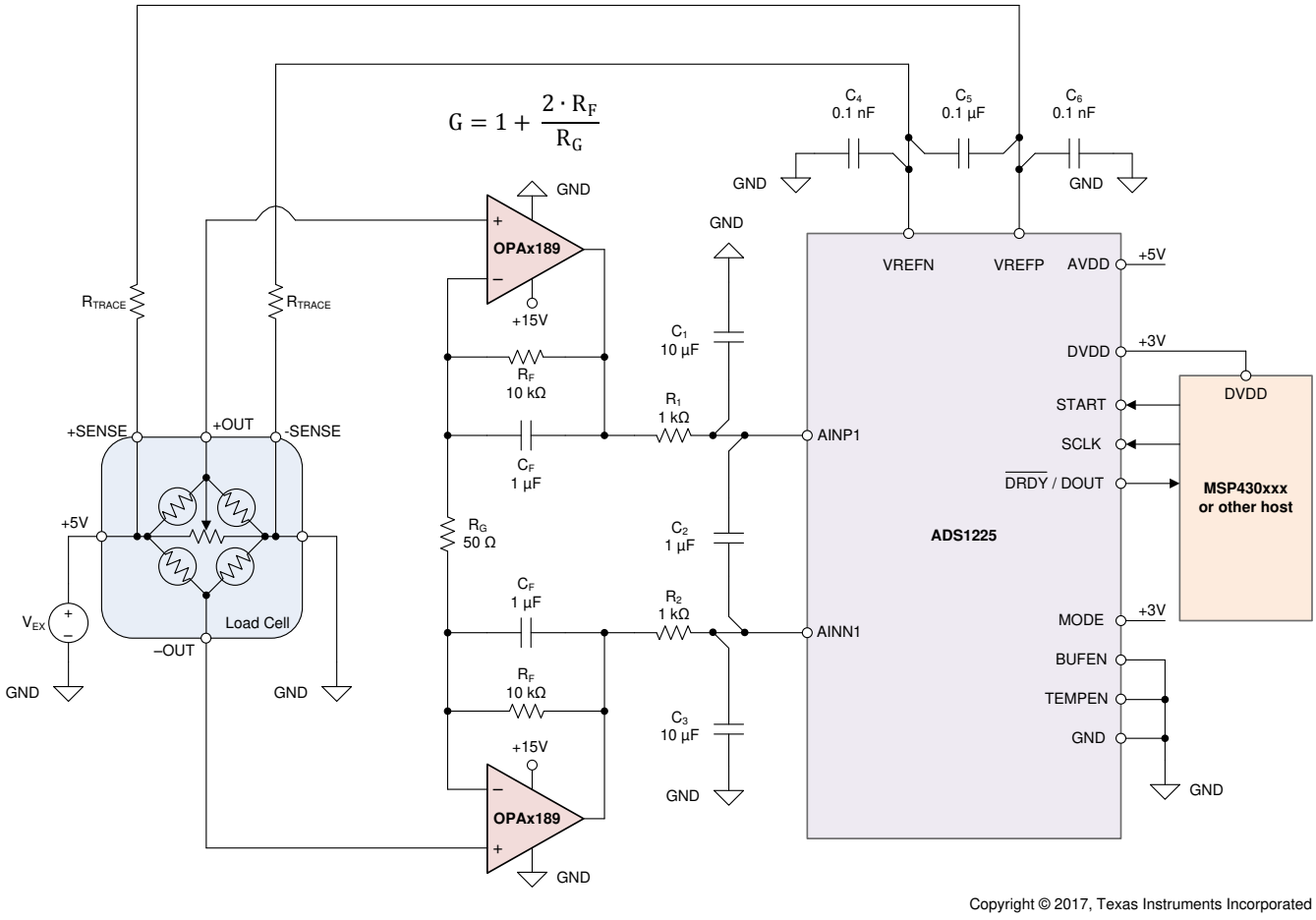


図 9-8. 24-Bit, Differential Load Cell or Strain Gauge Sensor Signal Conditioning Schematic

10 Power Supply Recommendations

The OPAx189 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *The PCB is a component of op amp design* techincal brief.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in 図 11-1, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

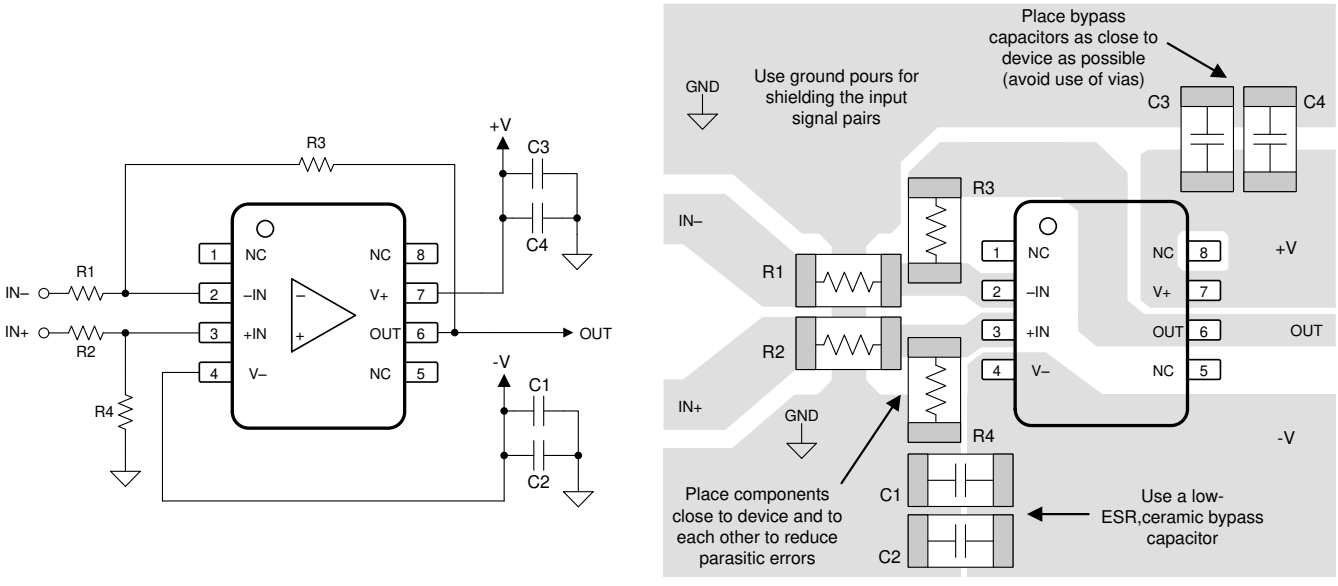


図 11-1. Operational Amplifier Board Layout for Difference Amplifier Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI folder.

12.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* technical brief
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis* technical brief
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis* technical brief
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* technical brief
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *Tuning in Amplifiers* application bulletin
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application report
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application bulletin
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)* application report
- Texas Instruments, *Analog linearization of resistance temperature detectors* technical brief
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter* reference guide

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.5 Trademarks

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TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA189ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA189ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA189IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CTV
OPA189IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CS6
OPA189IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CS6
OPA189IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CS6
OPA189IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CS6
OPA189IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA189IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA189IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA189IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA189
OPA2189ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2189
OPA2189ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2189
OPA2189IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1VQQ
OPA2189IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1VQQ
OPA2189IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1VQQ
OPA2189IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1VQQ
OPA2189IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2189
OPA2189IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OP2189
OPA4189IDR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IDR.B	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IDT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IDT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IPWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4189IPWR.B	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189
OPA4189IPWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4189

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

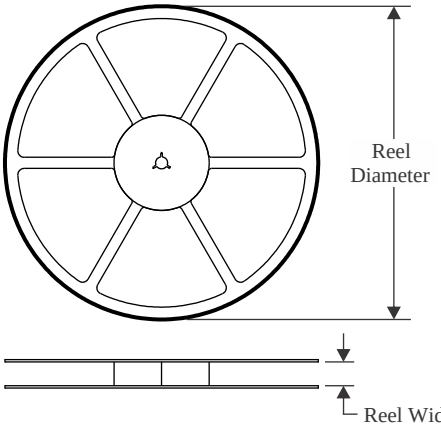
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

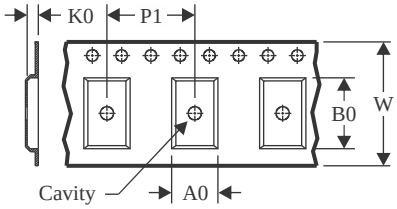
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

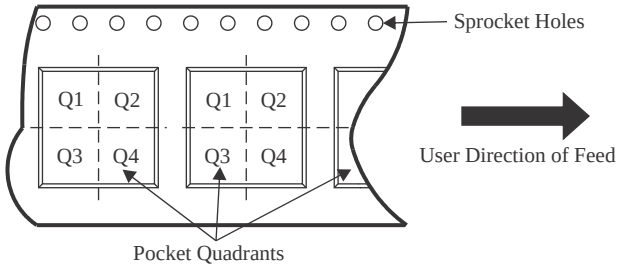


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

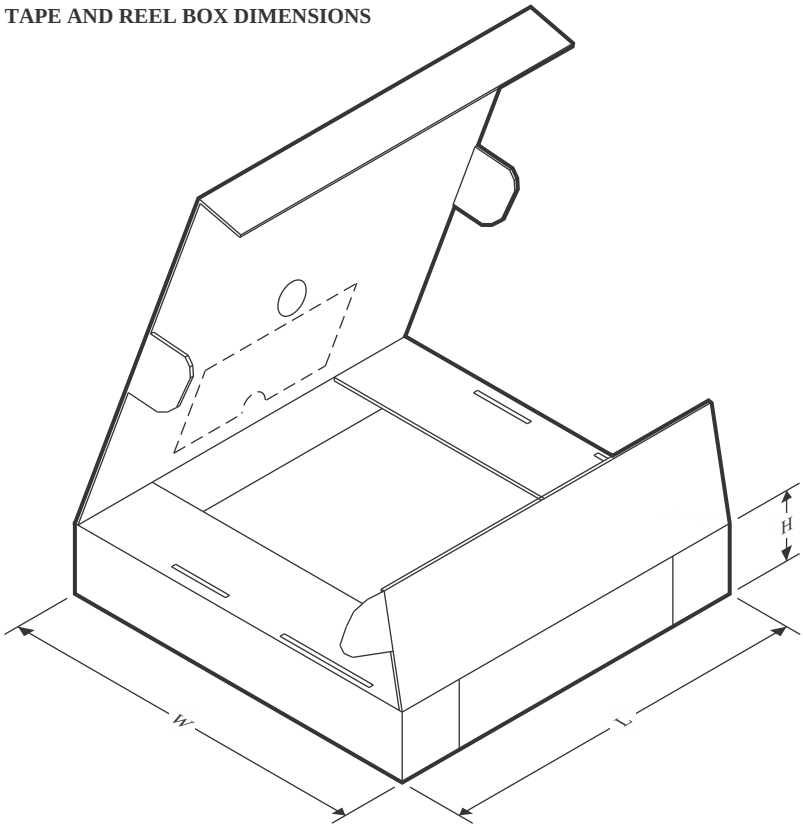
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA189IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA189IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA189IDBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA189IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA189IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA189IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA189IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2189IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2189IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2189IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
OPA4189IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.5	2.1	8.0	16.0	Q1
OPA4189IDT	SOIC	D	14	250	330.0	16.4	6.5	9.5	2.1	8.0	16.0	Q1
OPA4189IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4189IPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

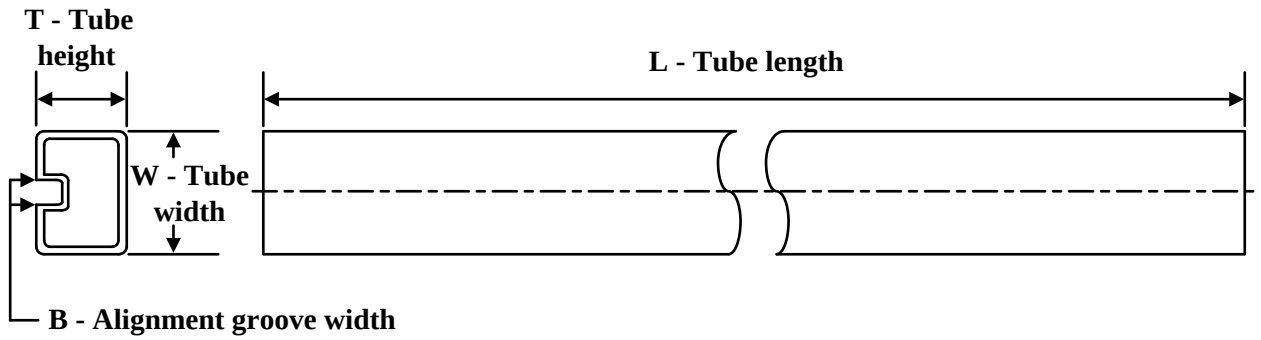
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

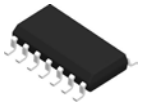
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA189IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA189IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA189IDBVTG4	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA189IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA189IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA189IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA189IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA2189IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2189IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2189IDR	SOIC	D	8	2500	366.0	364.0	50.0
OPA4189IDR	SOIC	D	14	3000	366.0	364.0	50.0
OPA4189IDT	SOIC	D	14	250	366.0	364.0	50.0
OPA4189IPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
OPA4189IPWT	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA189ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA189ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2189ID	D	SOIC	8	75	517	7.87	635	4.25
OPA2189ID.B	D	SOIC	8	75	517	7.87	635	4.25

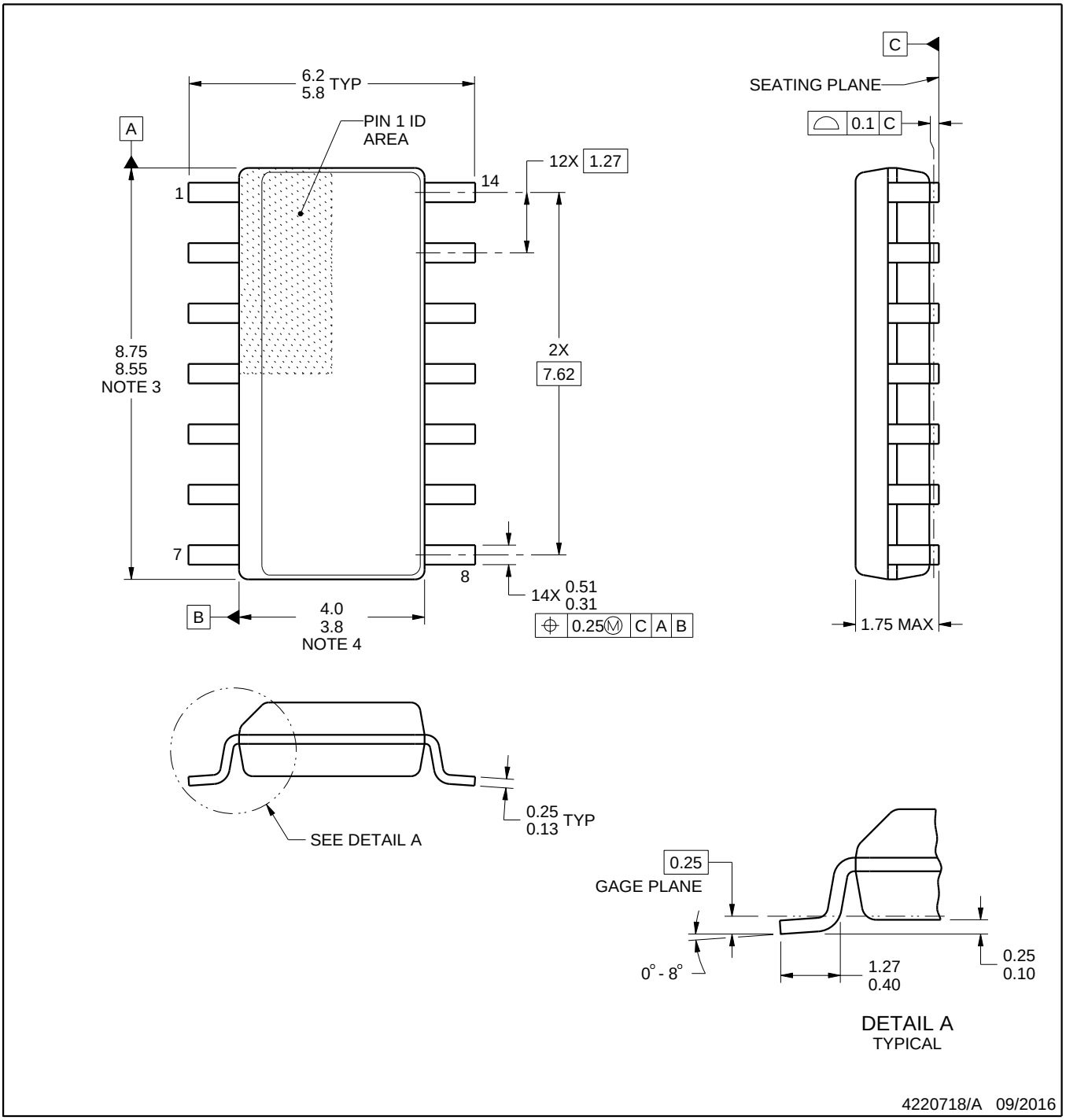


PACKAGE OUTLINE

D0014A

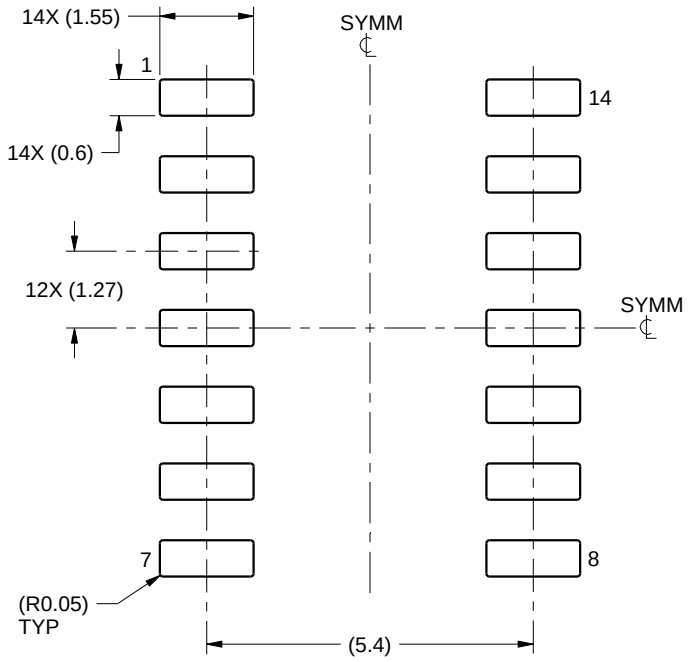
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

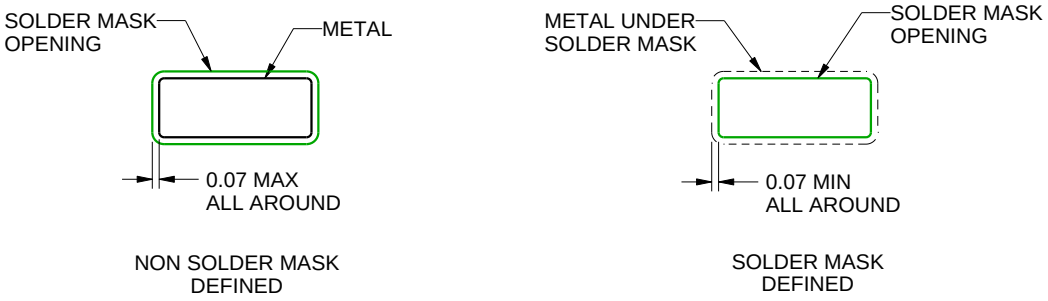


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

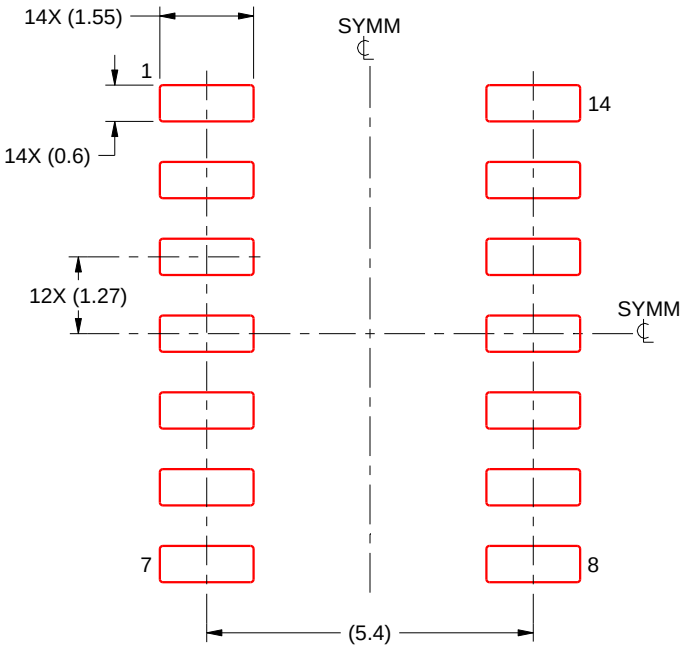
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

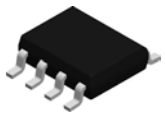


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

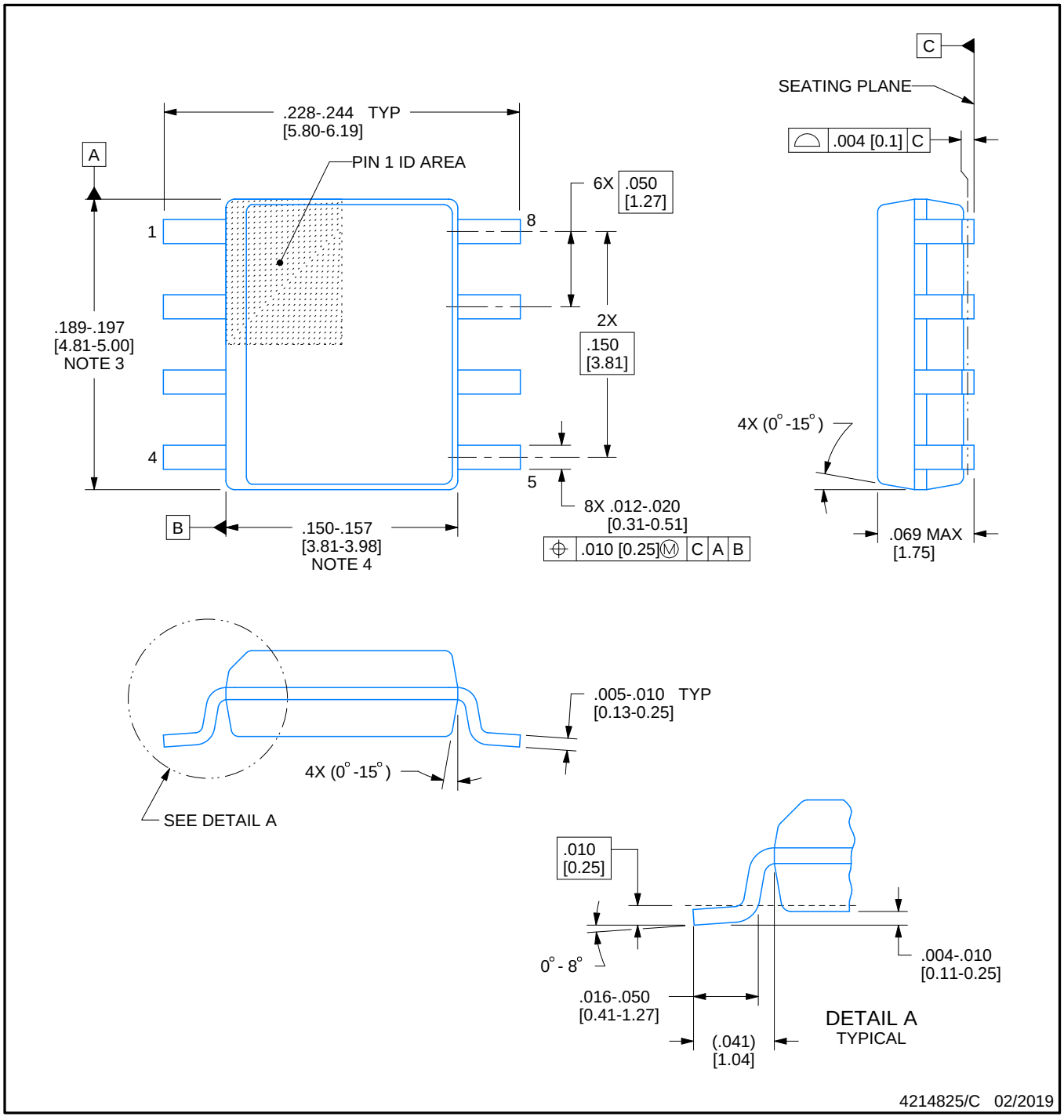


PACKAGE OUTLINE

D0008A

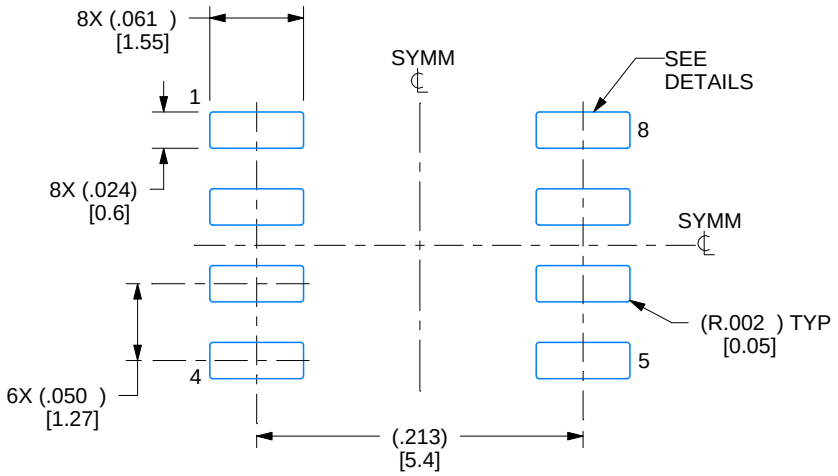
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

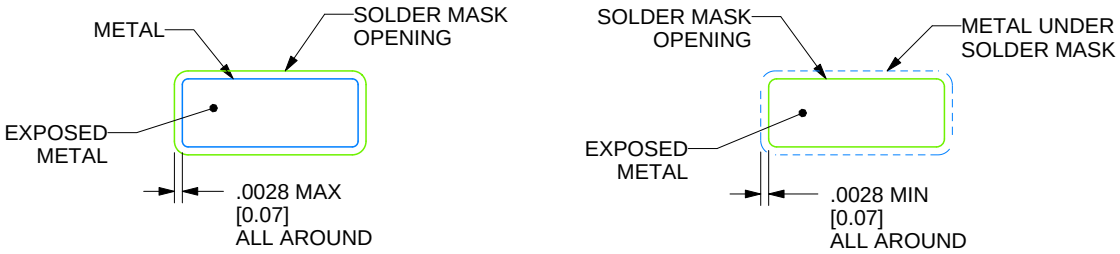


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

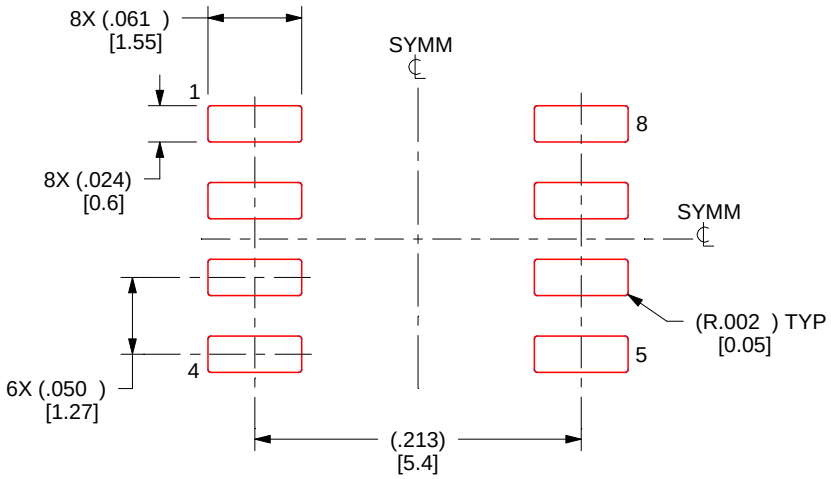
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

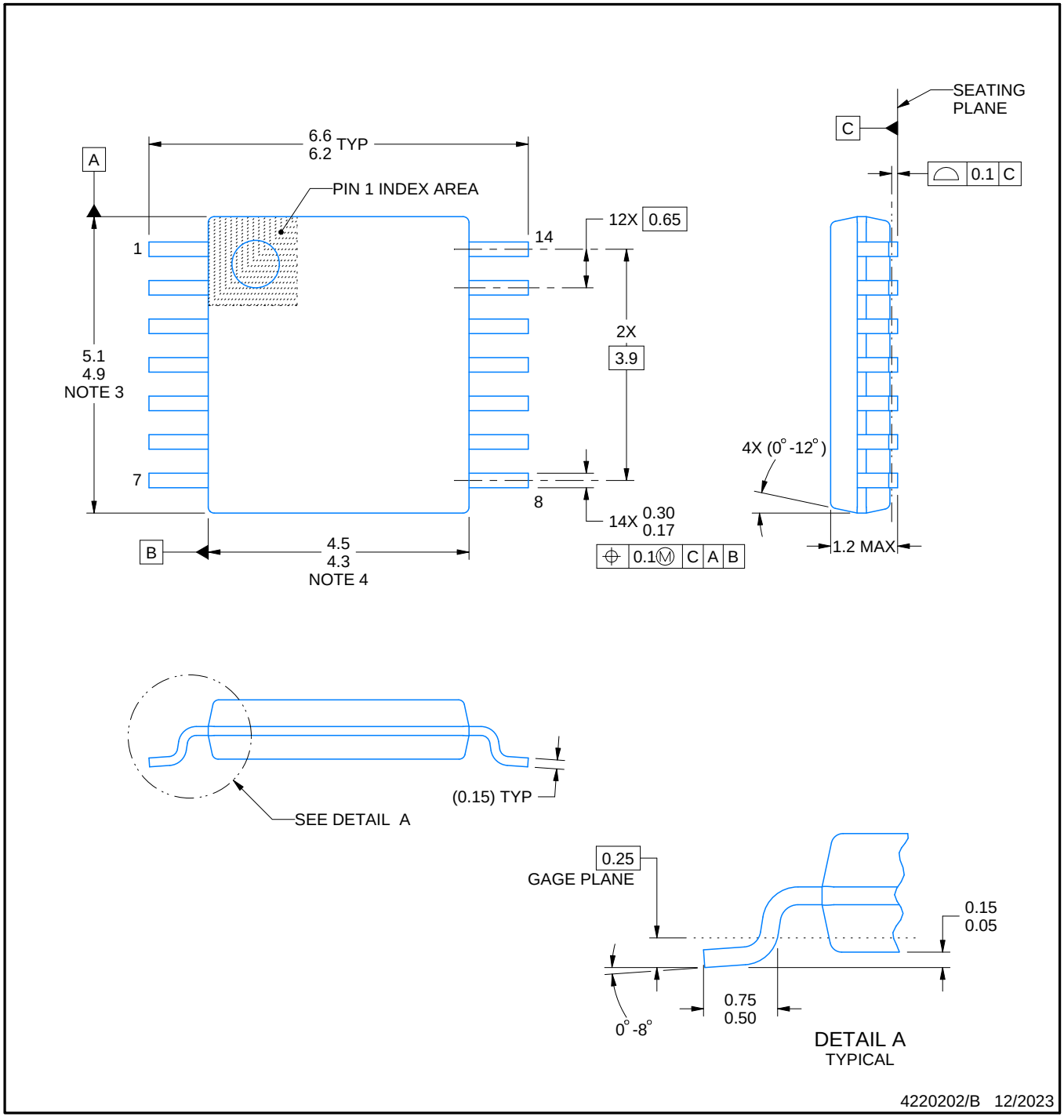
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

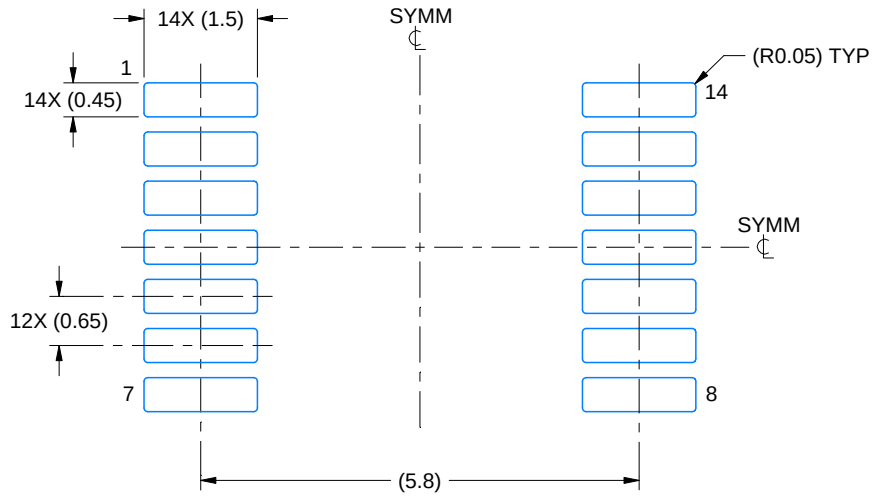
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

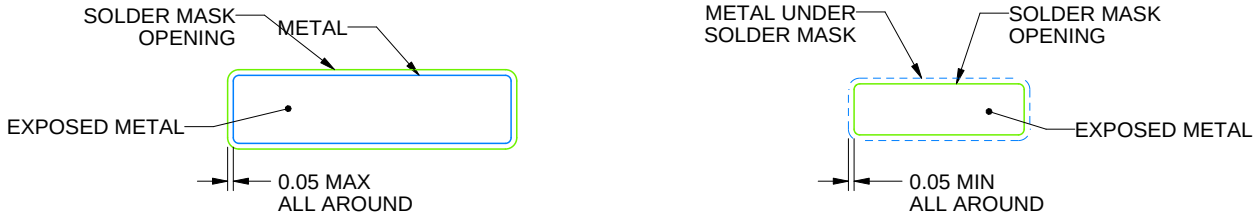


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

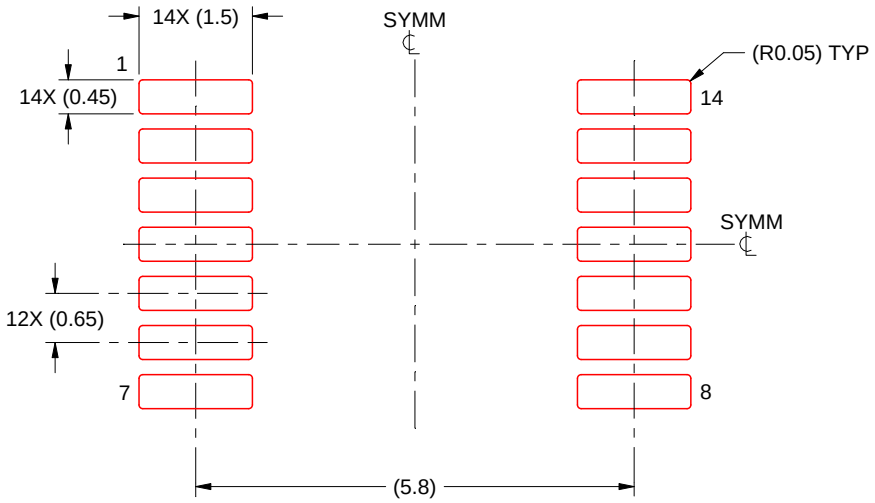


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

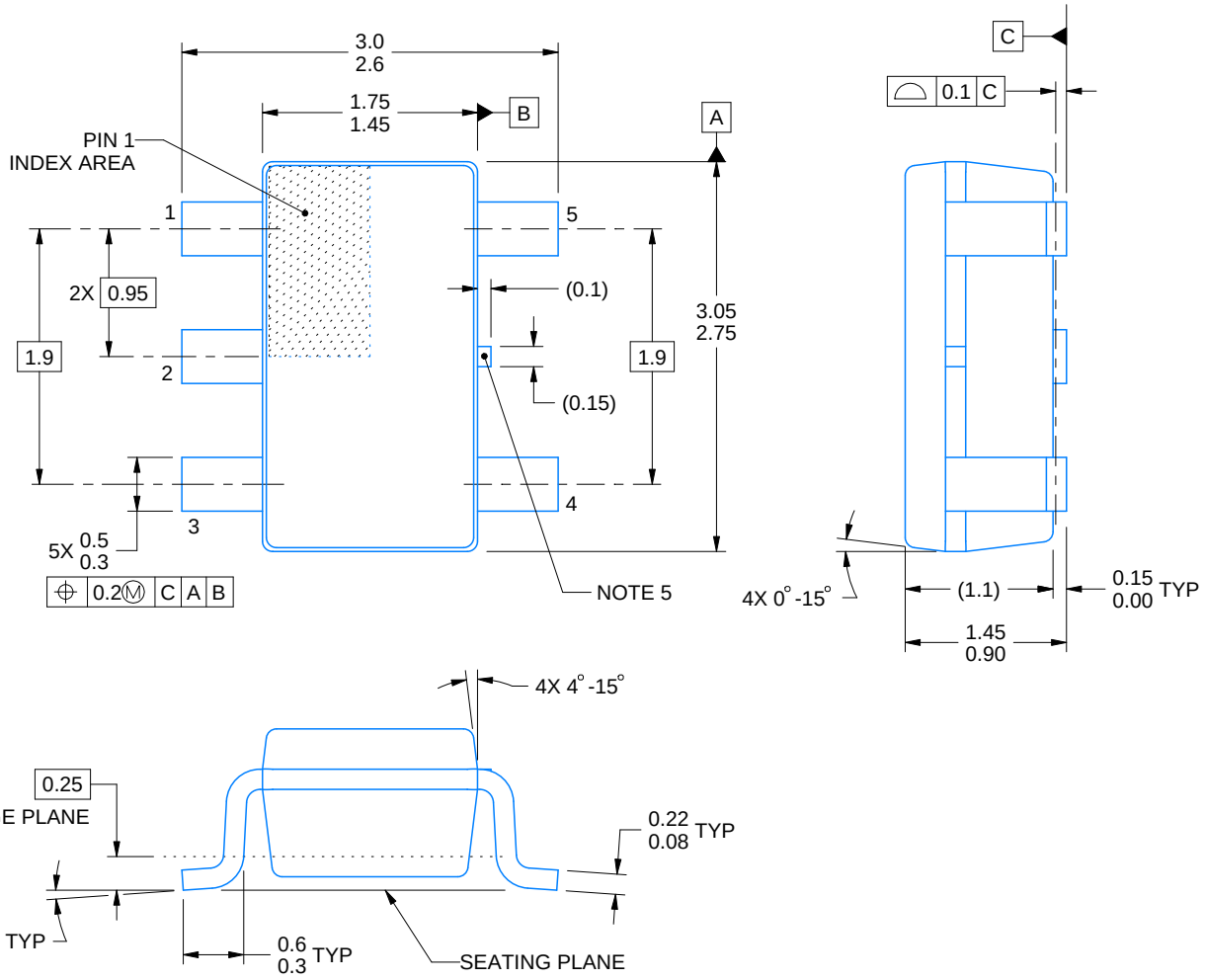
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

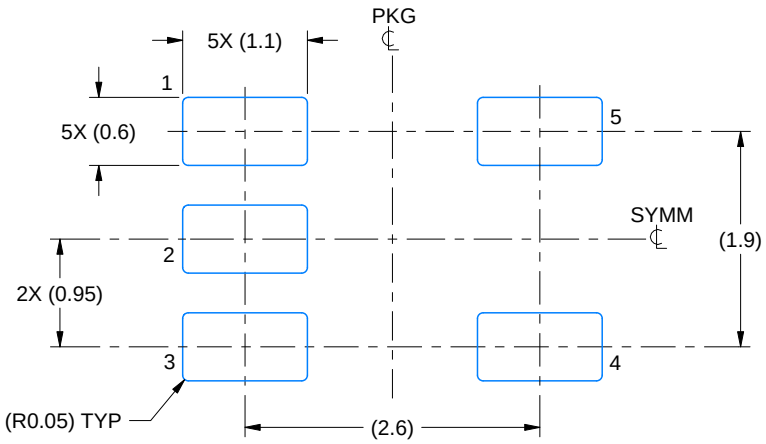
SMALL OUTLINE TRANSISTOR



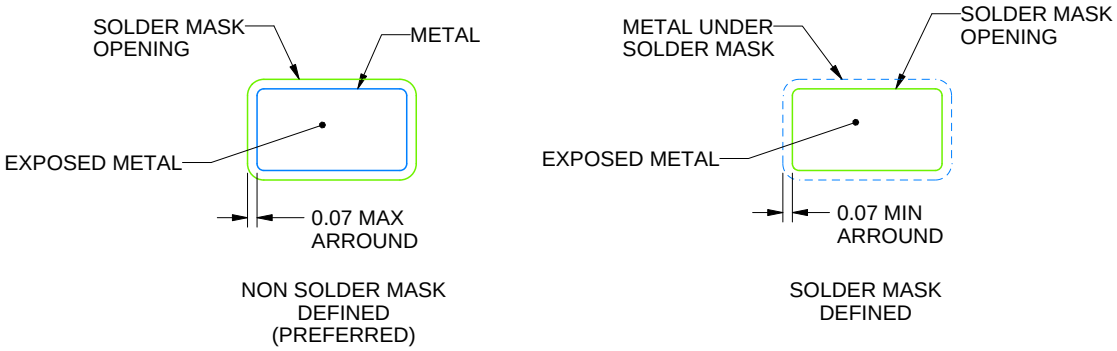
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

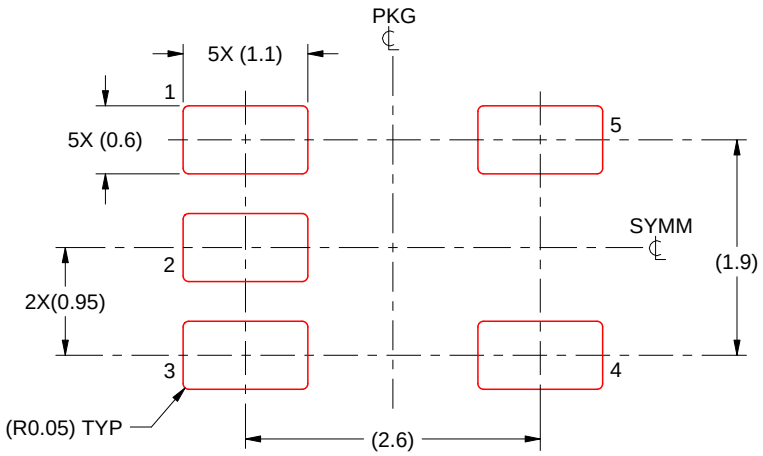


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

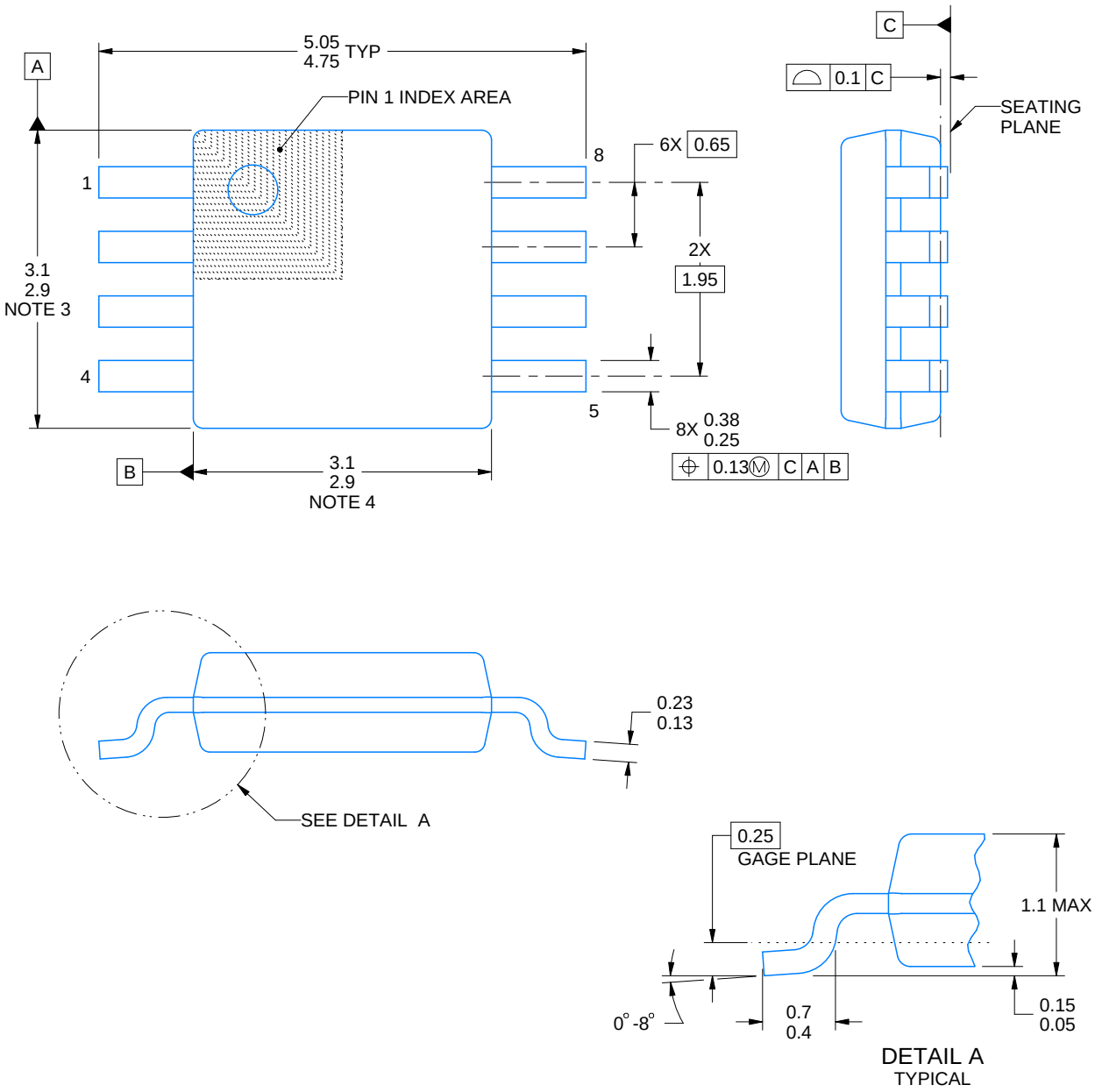
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

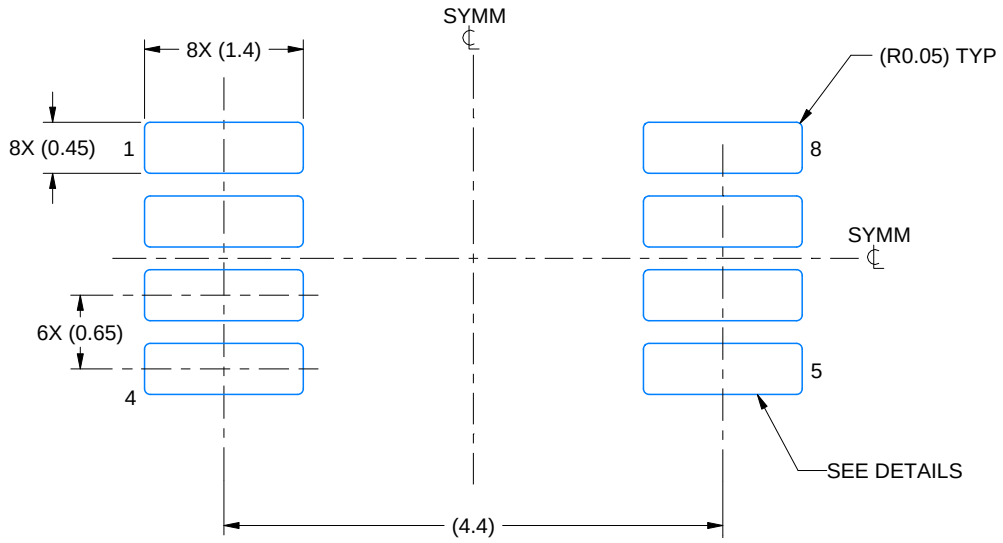
SMALL OUTLINE PACKAGE



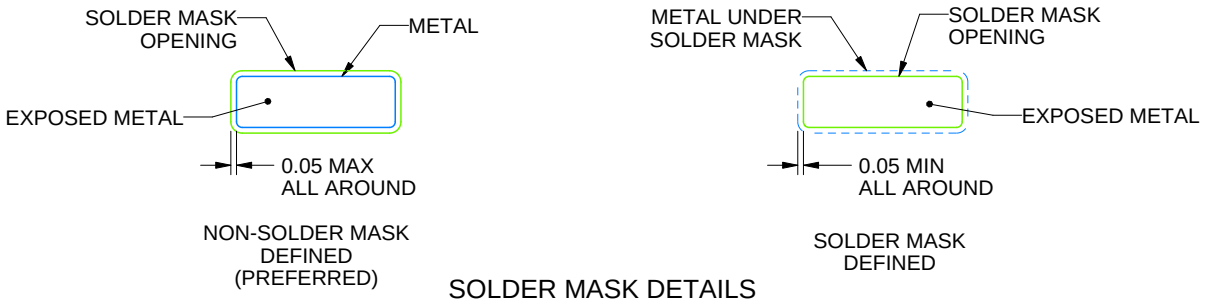
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

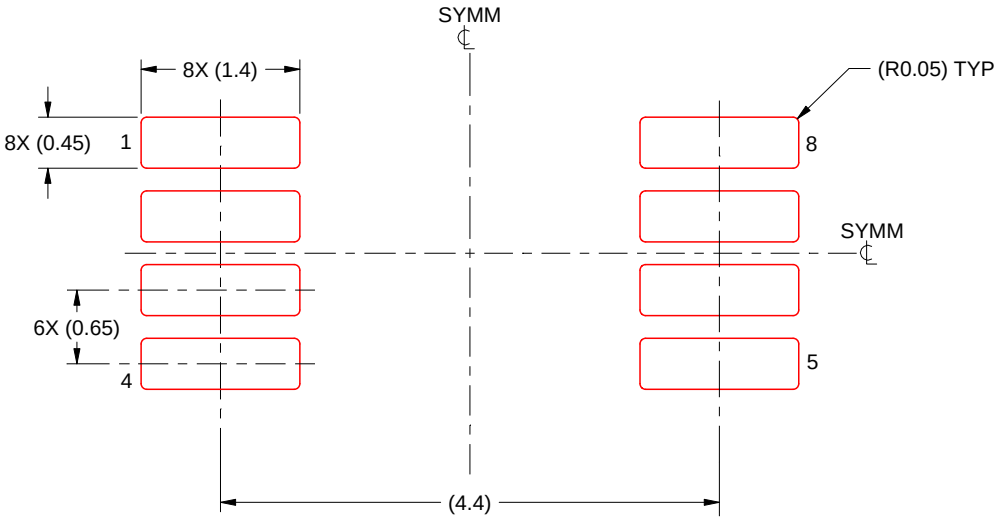


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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