OPAx180 ドリフト係数0.1µV/℃、低ノイズ、レール・ツー・レール出力、36V、ゼロ・ドリフト・オペアンプ

1 特長

- 低いオフセット電圧: 75µV (最大値)
- ゼロ・ドリフト: 0.1µV/℃
- 低ノイズ: 10nV/√Hz
- 非常に低い1/fノイズ
- 非常に優れたDC精度
  - PSRR: 126dB
  - CMRR: 114dB
  - オープン・ループ・ゲイン(A_{OL}): 120dB
- 静止電流: 525µA (最大値)
- 広い電源電圧範囲: ±2V～±18V
- レール・ツー・レール出力:
  入力に負のレールも含む
- 低いバイアス電流: 250pA (標準値)
- RFIフィルタ付きの入力
- *Micro*Sizeパッケージ

2 アプリケーション

- ブリッジ・アンプ
- 歪みゲージ
- 試験用機器
- トランスデューサ・アプリケーション
- 温度測定
- 電子計測器
- 医療用計測機器
- 抵抗熱検出器
- 高精度アクティブ・フィルタ

3 概要

OPA180、OPA2180、OPA4180オペアンプは、TI独自のゼロ・ドリフト技法を使用して、低いオフセット電圧(75µV)と、時間や温度に対してほぼゼロのドリフト係数を同時に実現しています。これらの小型、高精度、低静止電流オペアンプは、高い入力インピーダンスと、レールから18mV以内のレール・ツー・レール出力を提供します。入力同相範囲には、負のレールも含まれます。4V～36V (±2V～±18V)の範囲の単一またはデュアル電源を使用できます。

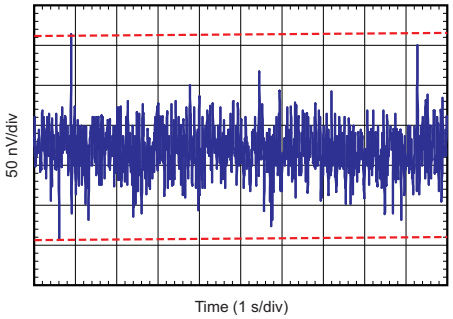
デュアル・チャネル・バージョンは、は、VSSOP-8パッケージとSOIC-8パッケージで供給されます。クワッド・チャネル・バージョンは、SOIC-14およびTSSOP-14パッケージで供給されます。シングルおよびクワッド・パッケージ製品(OPA180とOPA4180)は-40℃～+125℃で、デュアル・パッケージ製品(OPA2180)は-40℃～+105℃で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA180	SOT-23 (5)	1.60mm×2.90mm
	VSSOP、MSOP (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
OPA2180	VSSOP、MSOP (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
OPA4180	TSSOP (14)	5.00mm×4.40mm
	SOIC (14)	8.65mm×3.91mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

低ノイズ
(ピーク・ツー・ピークのノイズ = 250nV)



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (May 2014) から **Revision E** に変更 **Page**

- 「概要」セクションで、OPA180とOPA4180の動作温度を「-40℃～+105℃」から「-40℃～+125℃」に 変更 ... 1
- Added storage temperature parameter as the last row in the *Absolute Maximum Ratings* table ... 8
- Changed maximum operating temperature value from 105°C to 125°C in *Absolute Maximum Ratings* table ... 8
- Changed maximum operating temperature value from 105°C to 125°C in *Recommended Operating Conditions* table ... 8
- Changed input offset voltage drift temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Changed power supply rejection ratio temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Changed OPA180 input bias current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Added minimum OPA2180 input bias current value of 18 nA in *Electrical Characteristics* table ... 10
- Added minimum OPA180 input bias current value of 18 nA in *Electrical Characteristics* table ... 10
- Changed OPA180 input offset current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Added minimum OPA2180 input offset current value of 6 nA in *Electrical Characteristics* table ... 10
- Added minimum OPA180 input offset current value of 6 nA in *Electrical Characteristics* table ... 10
- Changed common-mode rejection ratio temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Changed open-loop voltage gain temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 10
- Changed voltage output swing from rail temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 11
- Changed quiescent current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 11
- 変更 operating temperature from "–40°C to +105°C" to " –40°C to +125°C" in *Feature Description* section ... 18
- Updated 図 34 ... 24
- 変更 operating temperature from "–40°C to +105°C" to " –40°C to +125°C" in *Power Supply Recommendations* section 25

改訂履歴 (continued)

Revision C (December 2012) から Revision D に変更 **Page**

- 最新のデータシート標準に合わせてフォーマットを変更、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクションを追加、既存のセクションを移動 ... 1
- OPA180をドキュメントに追加 ... 1
- 製品情報の表を追加 ... 1
- Deleted Package Information table ... 5
- OPA180 pinout drawings ... 5
- Added Pin Functions table ... 5
- Added Pin Functions table ... 6
- Added Pin Functions table ... 7
- Added Recommended Operating Conditions table ... 8
- Added Thermal Information: OPA180 table ... 9
- Changed Offset Voltage, *Long-term stability* parameter typical specification in Electrical Characteristics table ... 10
- Changed last sentence of *EMI Rejection* section ... 18

Revision B (December 2011) から Revision C に変更 **Page**

- 製品ステータスを混在ステータスから量産データへ 変更 ... 1
- OPA4180のステータスを量産データへ 変更 ... 1
- Added package marking to OPA2180 VSSOP-8 row in Package Information table ... 5
- Deleted ordering number and transport media columns from Package Information table ... 5
- Changed Input Bias Current section in Electrical Characteristics (V_S = +4 V to +36 V) table ... 10

Revision A (November 2011) から Revision B に変更 **Page**

- Changed footnote 1 of Electrical Characteristics table ... 10
- Updated 図 7 ... 13

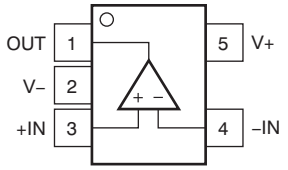
5 Device Comparison Table

Table 1. Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT (μV/°C)	BANDWIDTH (MHz)
Single	OPA188(4 V to 36 V)	25	0.085	2
	OPA180 (4 V to 36 V)	75	0.35	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2180 (4 V to 36 V)	75	0.35	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4180 (4 V to 36 V)	75	0.35	2
	OPA4330 (5 V)	50	0.25	0.35

6 Pin Configuration and Functions

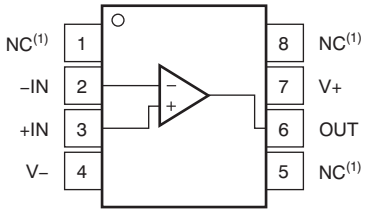
OPA180 DBV Package
5-Pin SOT-23
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative supply or ground (for single-supply operation)
V+	5	—	Positive supply or ground (for single-supply operation)

OPA180 D, DGK Packages
8-Pin SO, MSOP
Top View

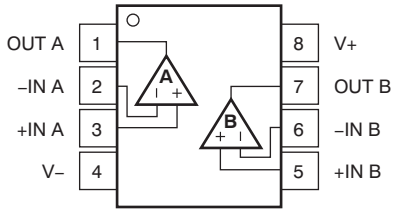


(1) NC- no internal connection

Pin Functions: OPA180

PIN		DESCRIPTION
NAME	NO.	
–IN	2	Inverting input
+IN	3	Noninverting input
NC	1, 5, 8	No connection
OUT	6	Output
V–	4	Negative power supply
V+	7	Positive power supply

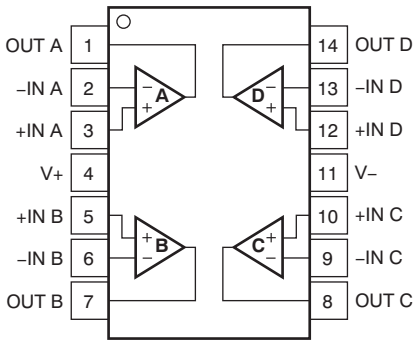
OPA2180 D, DGK Packages
8-Pin SOIC, VSSOP
Top View



Pin Functions: OPA2180

PIN		DESCRIPTION
NAME	NO.	
–IN A	2	Inverting input, channel A
+IN A	3	Noninverting input, channel A
–IN B	6	Inverting input, channel B
+IN B	5	Noninverting input, channel B
OUT A	1	Output, channel A
OUT B	7	Output, channel B
V–	4	Negative power supply
V+	8	Positive power supply

OPA4180 D, PW Packages
14-Pin SOIC, TSSOP
(Top View)



Pin Functions: OPA4180

PIN		DESCRIPTION
NAME	NO.	
–IN A	2	Inverting input, channel A
+IN A	3	Noninverting input, channel A
–IN B	6	Inverting input, channel B
+IN B	5	Noninverting input, channel B
–IN C	9	Inverting input, channel C
+IN C	10	Noninverting input, channel C
–IN D	13	Inverting input, channel D
+IN D	12	Noninverting input, channel D
OUT A	1	Output, channel A
OUT B	7	Output, channel B
OUT C	8	Output, channel C
OUT D	14	Output, channel D
V–	11	Negative supply or ground (for single-supply operation)
V+	4	Positive supply or ground (for single-supply operation)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage			±20, ±40 (single-supply)	V
	Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
		Current		±10	mA
	Output short-circuit(2)		Continuous		
	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1.5	1.5	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted), R_L = 10 kΩ connected to V_S / 2, and $V_{COM} = V_{OUT} = V_S$ / 2, (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage [(V+) – (V–)]	Single-supply	4.5		36	V
	Bipolar-supply	±2.25		±18	V
Operating temperature		–40		125	°C

7.4 Thermal Information: OPA180

THERMAL METRIC(1)		OPA180			UNIT
		D (SOIC)	DBV (SOT-23)	DGK (MSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	158.8	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	60.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	44.8	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	1.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	4.2	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2180

THERMAL METRIC(1)		OPA2180		UNIT
		D (SOIC)	DGK (MSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111	159.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.9	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	48.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	77.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4180

THERMAL METRIC(1)		OPA4180		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S = ±2 V to ±18 V (V_S = 4 V to 36 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage				15	75	µV
dV_{IO}/dT	Input offset voltage drift		T_A = –40°C to +125°C		0.1	0.35	µV/°C
PSRR	Power supply rejection ratio		V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.1	0.5	µV/V
			T_A = –40°C to +125°C, V_S = 4 V to 36 V, V_{CM} = V_S / 2			0.5	µV/V
	Long-term stability				4 (1)		µV
	Channel separation, DC				1		µV/V
INPUT BIAS CURRENT							
I_{IB}	Input bias current		OPA2180		±0.25	±1	nA
			OPA2180: T_A = –40°C to +105°C	18		±5	nA
			OPA180, OPA4180		±0.25	±1.7	nA
			OPA180, OPA4180: T_A = –40°C to +125°C	18		±6	nA
I_{IO}	Input offset current		OPA2180		±0.5	±2	nA
			OPA2180: T_A = –40°C to +105°C	6		±2.5	nA
			OPA180, OPA4180			±3.4	nA
			OPA180, OPA4180: T_A = –40°C to +125°C	6		±3	nA
NOISE							
	Input voltage noise		f = 0.1 Hz to 10 Hz		0.25		μV_{PP}
e_n	Input voltage noise density		f = 1 kHz		10		nV/√Hz
i_n	Input current noise density		f = 1 kHz		10		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio		(V–) < V_{CM} < (V+) – 1.5 V	104	114		dB
			T_A = –40°C to +125°C, (V–) + 0.5 V < V_{CM} < (V+) – 1.5 V	100	104		dB
INPUT IMPEDANCE							
z_{id}	Differential				100 || 6		MΩ || pF
z_{ic}	Common-mode				6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	110	120		dB
			T_A = –40°C to +125°C, (V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	104	114		dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				2		MHz
SR	Slew rate		G = 1		0.8		V/µs
t_s	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		22		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		30		µs
t_{or}	Overload recovery time		V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise		f = 1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		

(1) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits, or approximately 4 µV.

Electrical Characteristics: V_S = ±2 V to ±18 V (V_S = 4 V to 36 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		8	18	mV
		R_L = 10 kΩ		250	300	mV
		T_A = –40°C to +125°C R_L = 10 kΩ		325	360	mV
I_{OS}	Short-circuit current			±18		mA
r_o	Output resistance (open loop)	f = 2 MHz, I_O = 0 mA		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		±2 (or 4)		±18 (or 36)	V
I_Q	Quiescent current (per amplifier)			450	525	µA
		T_A = –40°C to +125°C I_O = 0 mA			600	µA
TEMPERATURE						
	Specified range		–40		105	°C
	Operating range		–40		105	°C

7.8 Typical Characteristics: Table of Graphs

表 2. Characteristic Performance Measurements

DESCRIPTION	FIGURE
I_B and I_{OS} vs Common-Mode Voltage	図 1
Input Bias Current vs Temperature	図 2
Output Voltage Swing vs Output Current (Maximum Supply)	図 3
CMRR vs Temperature	図 4
0.1-Hz to 10-Hz Noise	図 5
Input Voltage Noise Spectral Density vs Frequency	図 6
Open-Loop Gain and Phase vs Frequency	図 7
Open-Loop Gain vs Temperature	図 8
Open-Loop Output Impedance vs Frequency	図 9
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	図 10, 図 11
No Phase Reversal	図 12
Positive Overload Recovery	図 13
Negative Overload Recovery	図 14
Small-Signal Step Response (100 mV)	図 15, 図 16
Large-Signal Step Response	図 17, 図 18
Large-Signal Settling Time (10-V Positive Step)	図 19
Large-Signal Settling Time (10-V Negative Step)	図 20
Short-Circuit Current vs Temperature	図 21
Maximum Output Voltage vs Frequency	図 22
Channel Separation vs Frequency	図 23
EMIRR IN+ vs Frequency	図 24

7.9 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

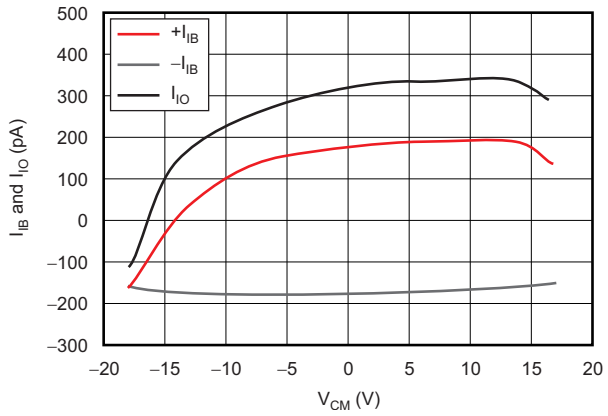


図 1. I_{IB} and I_{IO} vs Common-Mode Voltage

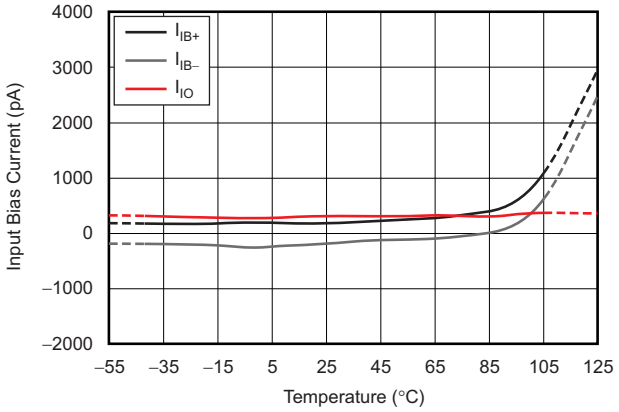


図 2. Input Bias Current vs Temperature

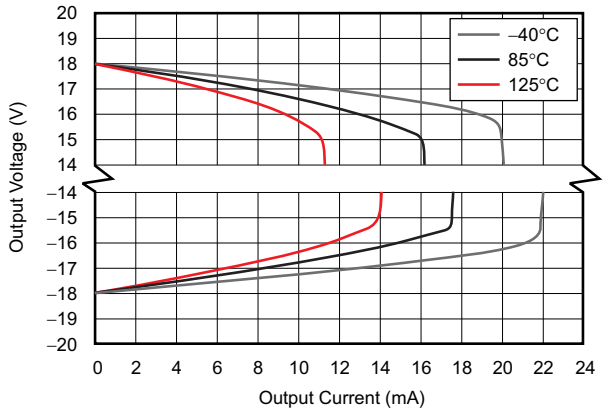
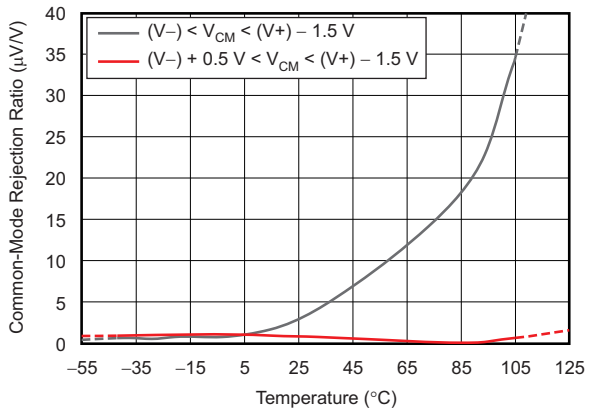
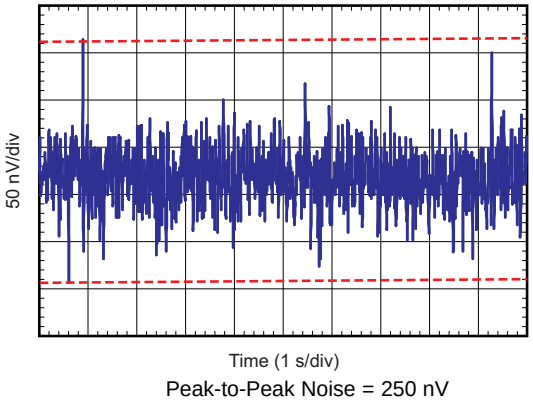


図 3. Output Voltage Swing vs Output Current (Maximum Supply)



V_{SUPPLY} = ±2 V

図 4. CMRR vs Temperature



Peak-to-Peak Noise = 250 nV

図 5. 0.1-Hz to 10-Hz Noise

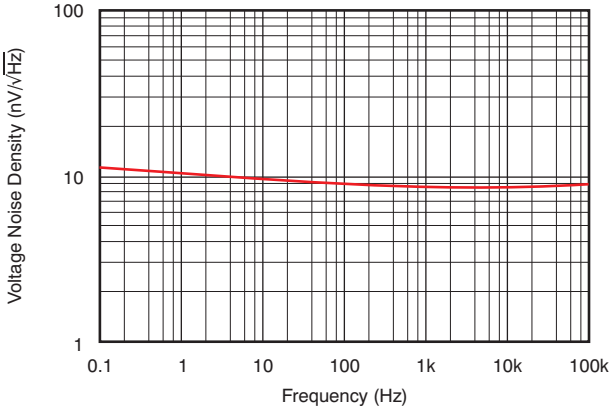


図 6. Input Voltage Noise Spectral Density vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

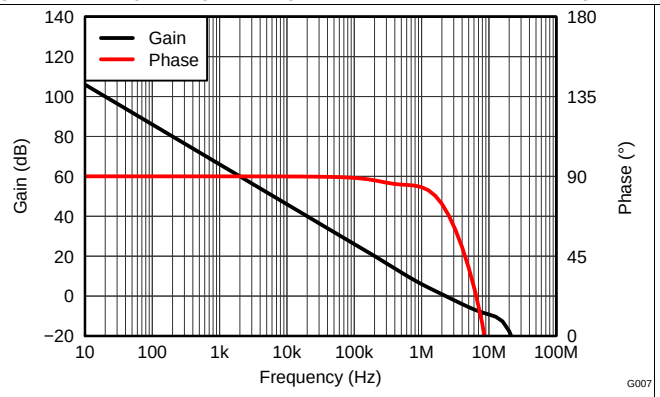


図 7. Open-Loop Gain and Phase vs Frequency

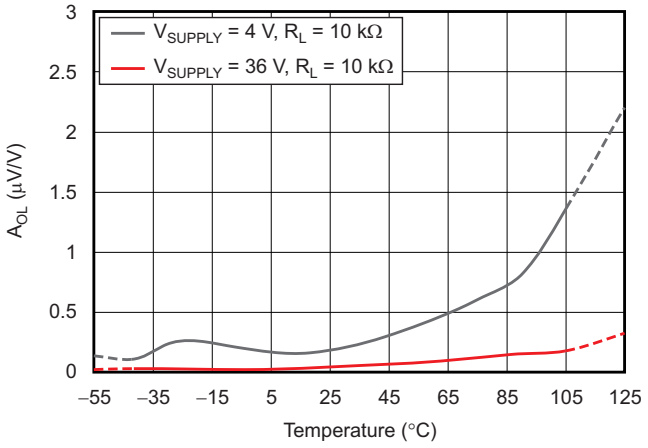


図 8. Open-Loop Gain vs Temperature

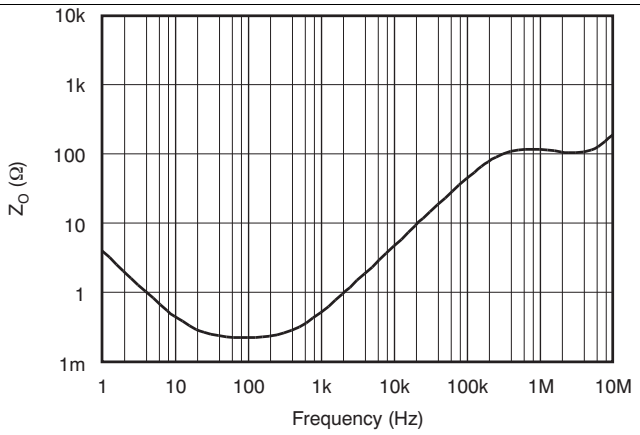


図 9. Open-Loop Output Impedance vs Frequency

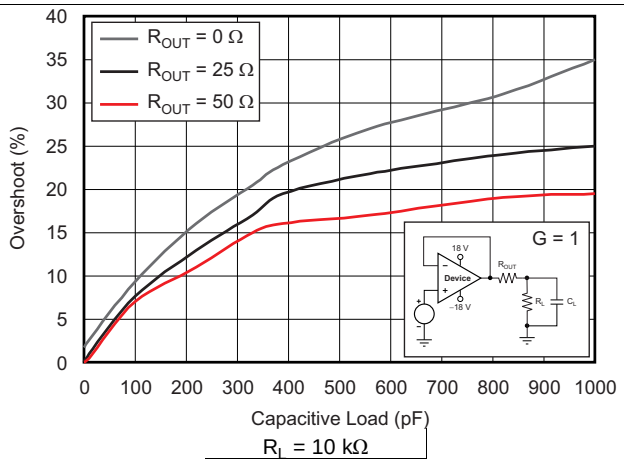


図 10. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

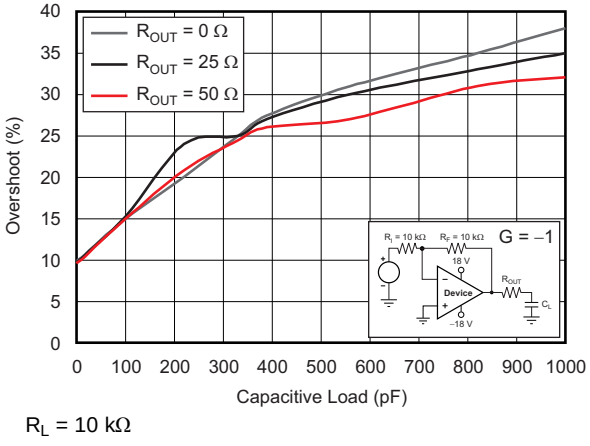


図 11. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

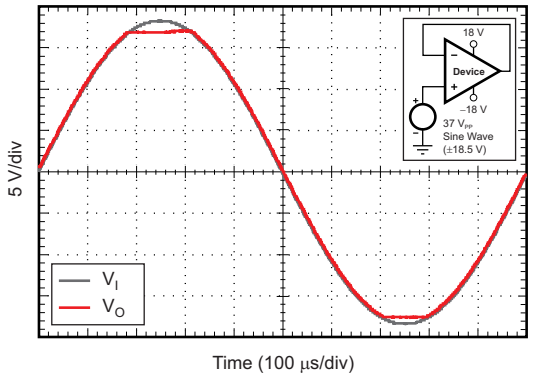


図 12. No Phase Reversal

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

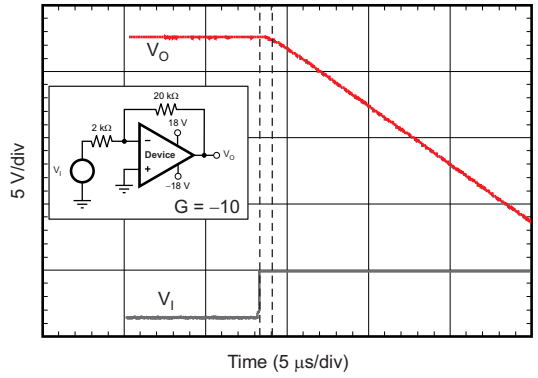


図 13. Positive Overload Recovery

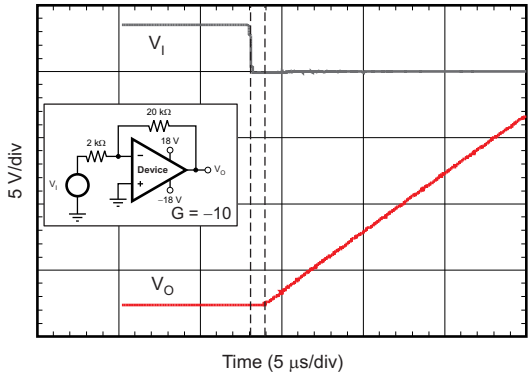
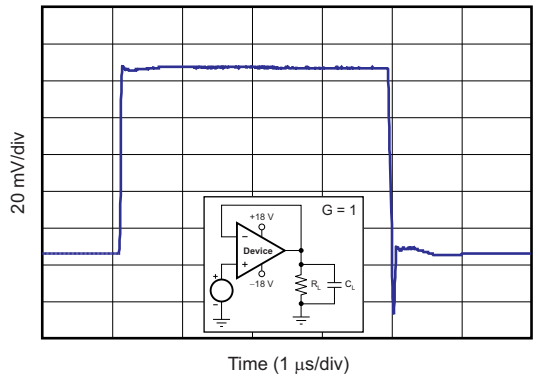
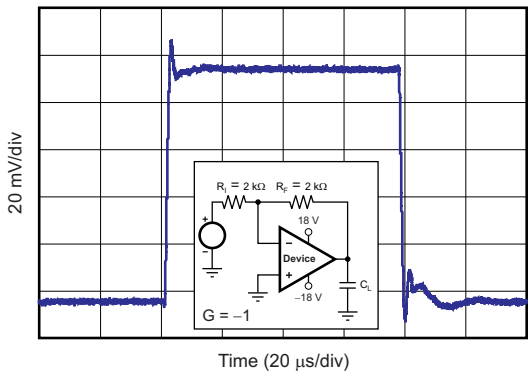


図 14. Negative Overload Recovery



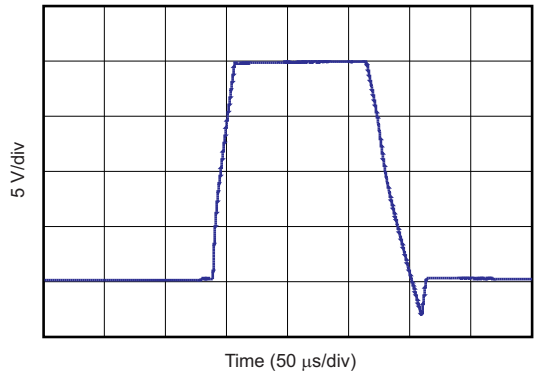
R_L = 10 kΩ C_L = 10 pF

図 15. Small-Signal Step Response (100 mV)



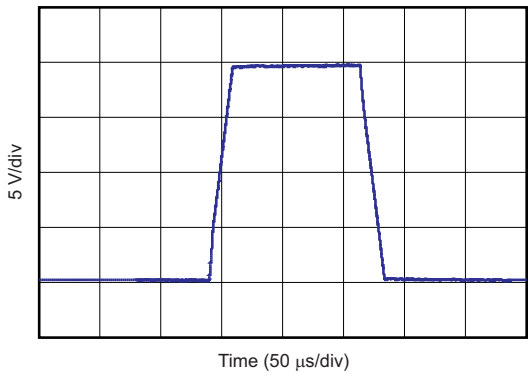
R_L = 10 kΩ C_L = 10 pF

図 16. Small-Signal Step Response (100 mV)



G = 1 R_L = 10 kΩ C_L = 10 pF

図 17. Large-Signal Step Response

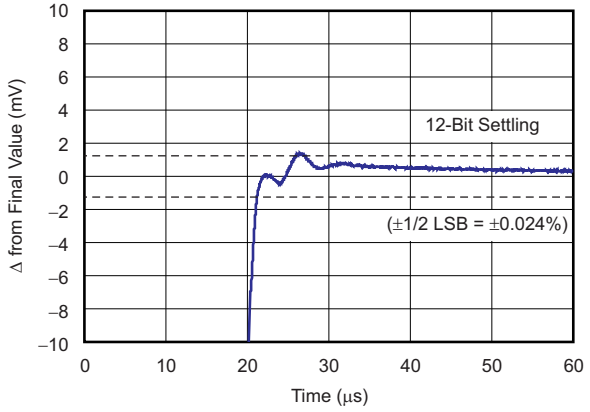


G = –1 R_L = 10 kΩ C_L = 10 pF

図 18. Large-Signal Step Response

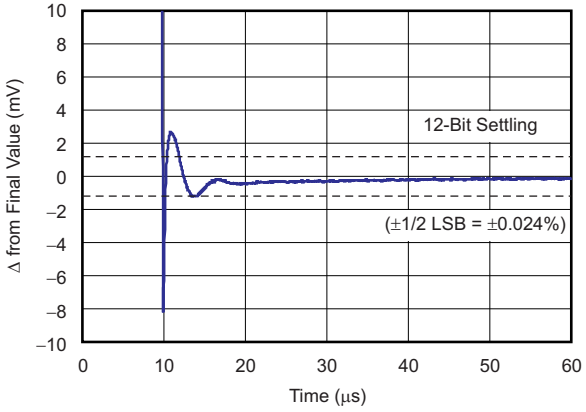
Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



G = –1

図 19. Large-Signal Settling Time (10-V Positive Step)



G = –1

図 20. Large-Signal Settling Time (10-V Negative Step)

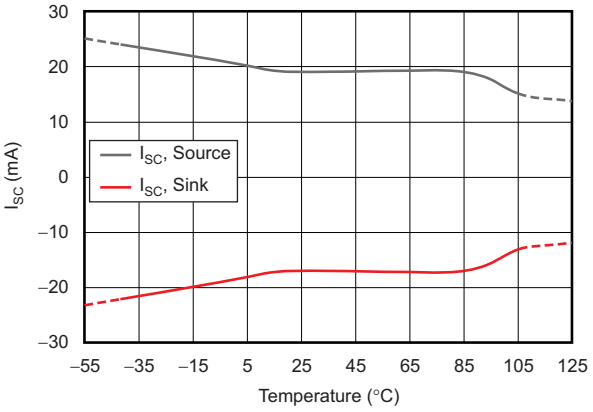


図 21. Short-Circuit Current vs Temperature

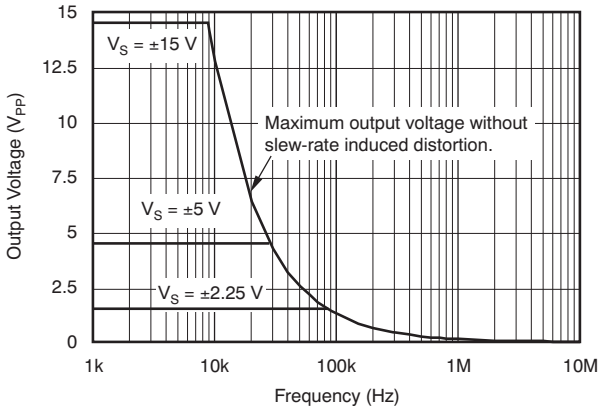


図 22. Maximum Output Voltage vs Frequency

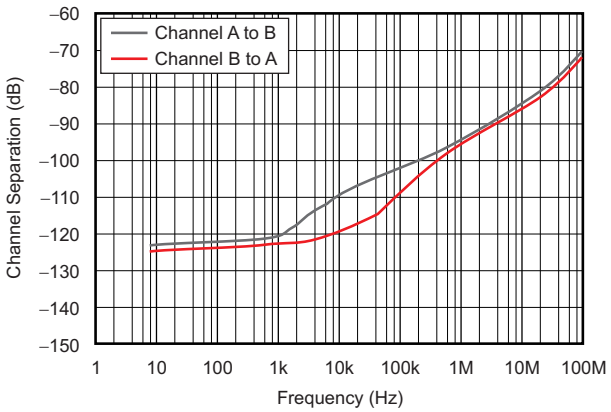


図 23. Channel Separation vs Frequency

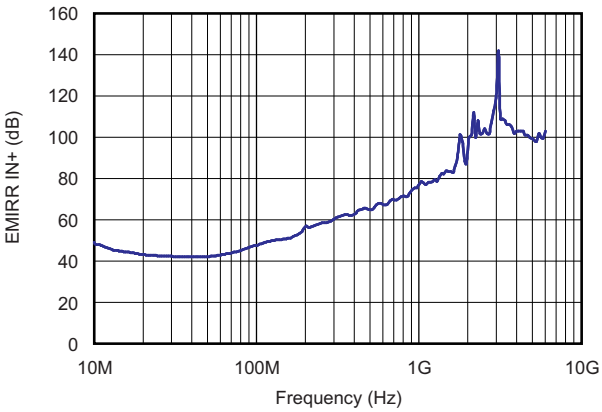


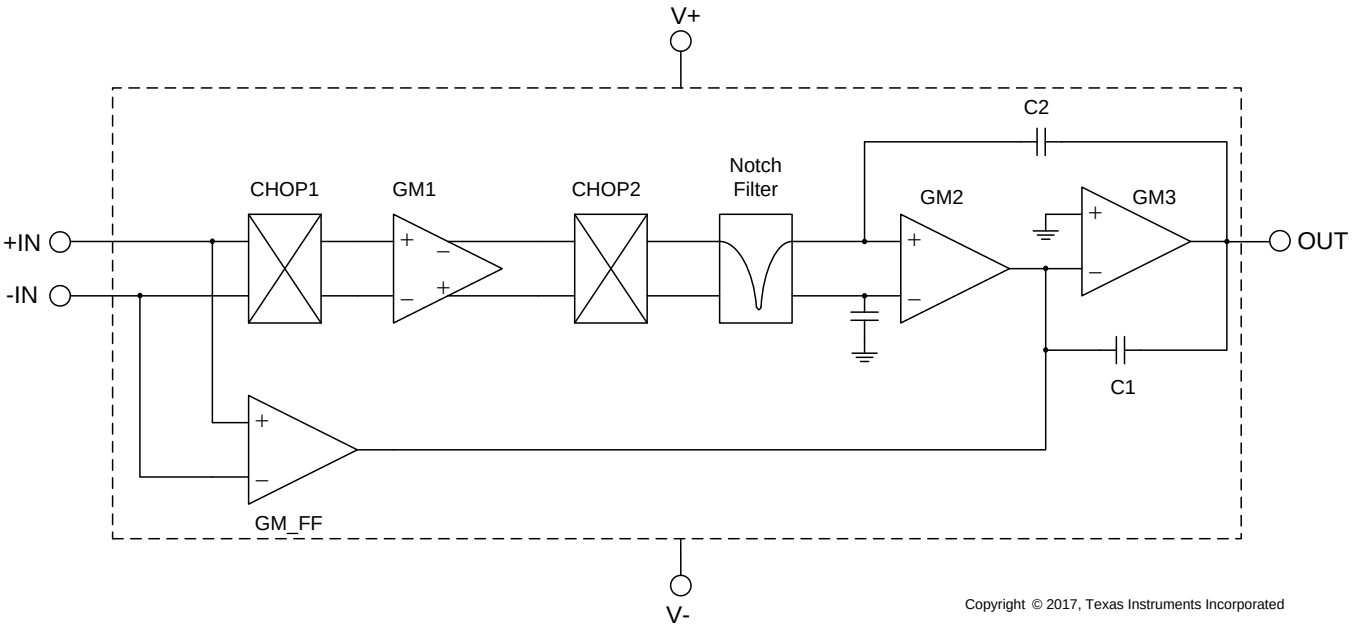
図 24. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPAx180 family of operational amplifiers combine precision offset and drift with excellent overall performance, making them designed for many precision applications. The precision offset drift of only 0.1 µV/°C provides stability over the entire temperature range. In addition, the devices offer excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The OPAx180 family of amplifiers is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.3.2 EMI Rejection

The OPAx180 family uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can improve with circuit design techniques; the OPAx180 family benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 25 shows the results of this testing on the OPAx180 family . For more detailed information, see the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

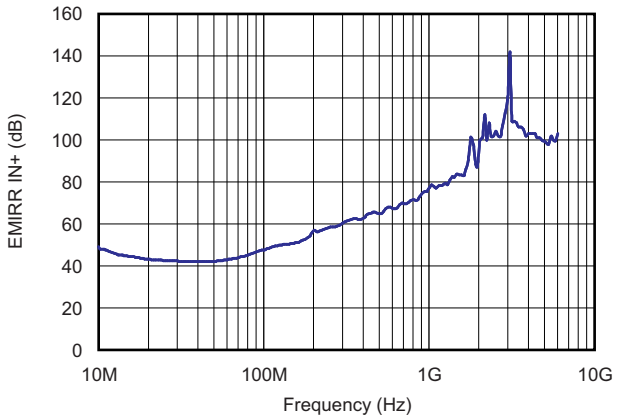


図 25. OPAx180 EMIRR Testing

8.3.3 Phase-Reversal Protection

The OPAx180 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx180 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 図 26.

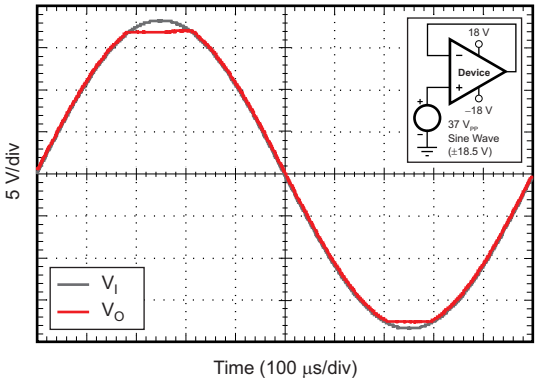


図 26. No Phase Reversal

Feature Description (continued)

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx180 are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 27 and 図 28 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See the *Feedback Plots Define Op Amp AC Performance*, application report, available for download from the TI website, for details of analysis techniques and application circuits.

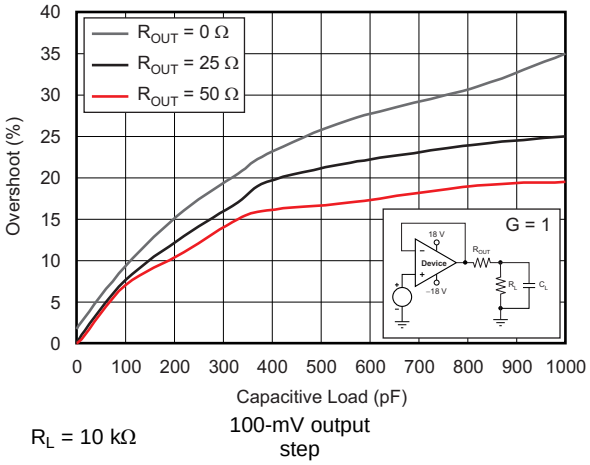


図 27. Small-Signal Overshoot Versus Capacitive Load

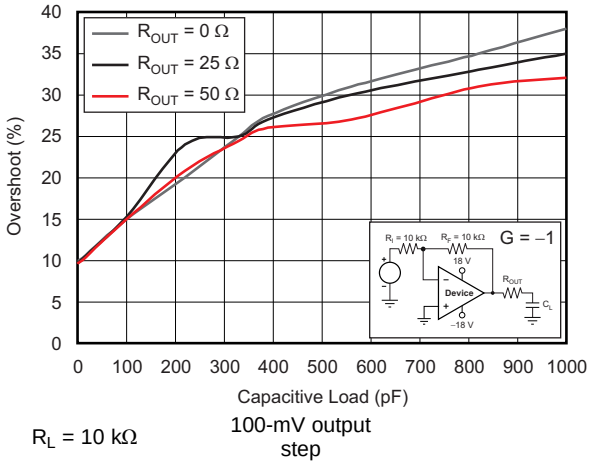


図 28. Small-Signal Overshoot Versus Capacitive Load

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. 図 29 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

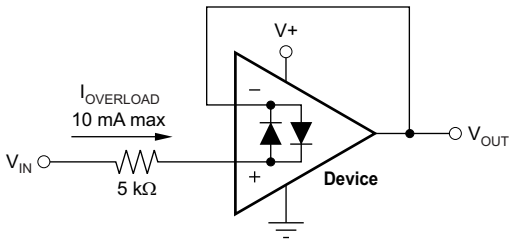


図 29. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as the pulse discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to protect the core from damage. The energy absorbed by the protection circuitry is then dissipated as heat.

Feature Description (continued)

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise when an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected so the diode does not turn on during normal operation.

However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.4 Device Functional Modes

The OPAx180, OPA2180 , and OPA4180 devices are powered on when the supply is connected. These devices can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. In single-supply operation with V– at ground (0 V), V+ can be any value between 4 V and 36 V. In dual-supply operation, the supply voltage difference between V– and V+ is from 4 V to 36 V. Typical examples of dual-supply configuration are ±5 V, ±10 V, ±15 V, and ±18 V. However, the supplies must not be symmetrical. Less common examples are V– at –3 V and V+ at 9 V, or V– at –16 V and V+ at 5 V. Any combination where the difference between V– and V+ is at least 4 V and no greater than 36 V is within the normal operating capabilities of these devices.

9 Application and Implementation

9.1 Application Information

The OPAx180 family offers excellent DC precision and AC performance. These devices operate up to 36-V supply rails and offer rail-to-rail output, ultra-low offset voltage, offset voltage drift and 2-MHz bandwidth. These features make the OPAx180 a robust, high-performance amplifier for high-voltage industrial applications.

9.2 Typical Applications

These application examples highlight a few of the circuits where the OPAx180 family can be used.

9.2.1 Bipolar ±10-V Analog Output from a Unipolar Voltage Output DAC

This design is used for conditioning a unipolar digital-to-analog converter (DAC) into an accurate bipolar signal source using the OPAx180 family and three resistors. The circuit is designed with reactive load stability in mind, and is compensated to drive nearly any conventional capacitive load associated with long cable lengths.

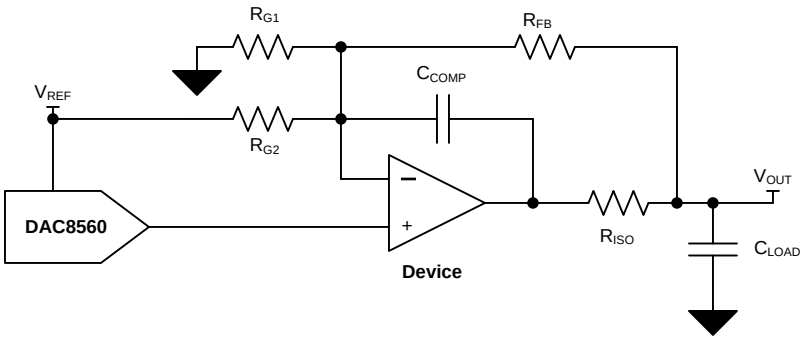


図 30. Circuit Schematic

9.2.1.1 Design Requirements

The design requirements are as follows:

- DAC supply voltage: +5-V dc
- Amplifier supply voltage: ±15-V dc
- Input: 3-wire, 24-bit SPI
- Output: ±10-V dc

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Component Selection

DAC: For convenience, devices with an external reference option or devices with accessible internal references are desirable in this application because the reference creates an offset. The DAC selection in this design must primarily be based on DC error contributions typically described by offset error, gain error, and integral nonlinearity error. Occasionally, additional specifications are provided that summarize end-point errors of the DAC typically called zero-code and full-scale errors. For AC applications, slew rate and settling time may require additional consideration.

Amplifier: Amplifier input offset voltage (V_{IO}) is a key consideration for this design. V_{IO} of an operational amplifier is a typical data sheet specification, but in-circuit performance is also affected by drift over temperature, the common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR); thus consideration should be given to these parameters as well. For ac operation, additional considerations should be made concerning slew rate and settling time. Input bias current (I_{IB}) can also be a factor, but typically the resistor network is implemented with sufficiently small resistor values that the effects of input bias current are negligible.

Passive: Resistor matching for the op-amp resistor network is critical for the success of this design; components with tight tolerances must be selected. For this design, 0.1% resistor values are implemented, but this constraint may be adjusted based on application-specific design goals. Resistor matching contributes to offset error and gain error in this design; see *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC* for further details. The tolerance of the $R_{ISO}$and C_{COMP} stability components is not critical, and 1% components are acceptable.

9.2.1.3 Application Curves

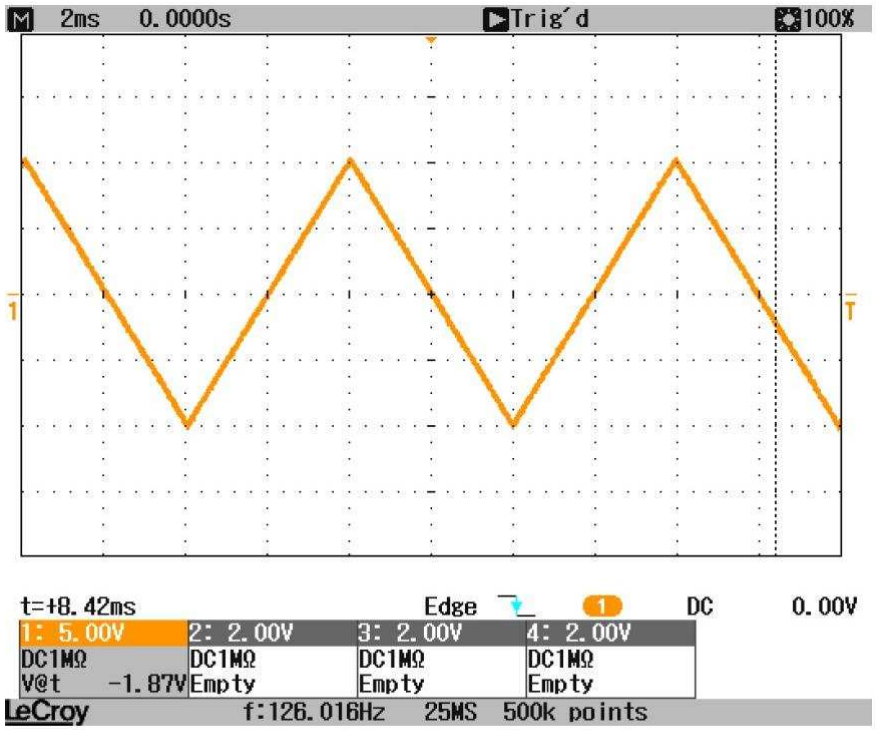


図 31. Full-Scale Output Waveform

Typical Applications (continued)

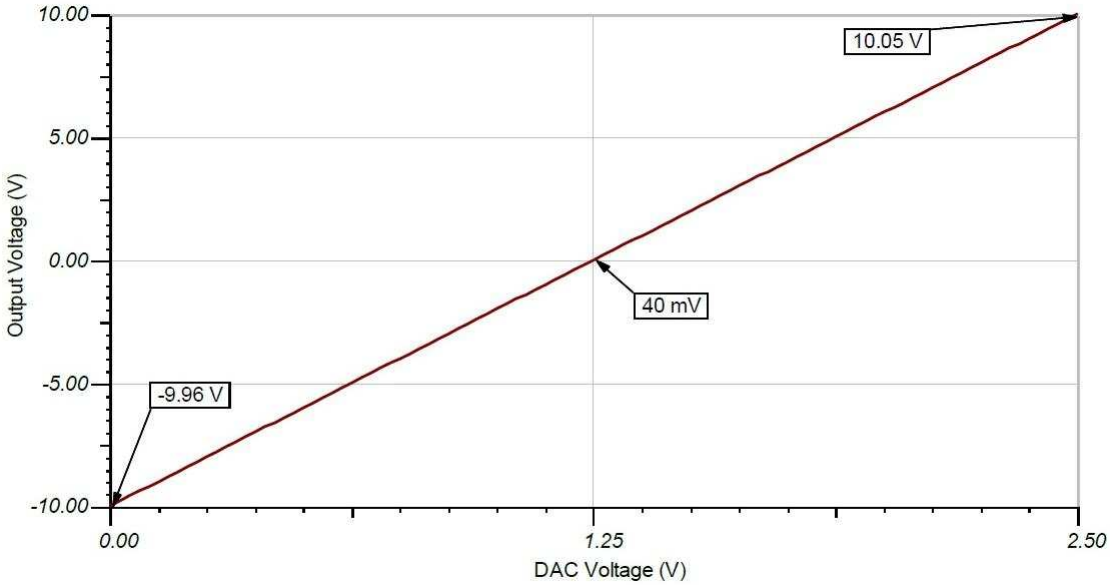


図 32. DC Transfer Characteristic

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD125, *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC*

9.2.2 Discrete INA + Attenuation

The OPAx180 family can be used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 in 図 33 provides the attenuation that allows this circuit to simply interface with 3.3-V or 5-V analog-to-digital converters (ADCs).

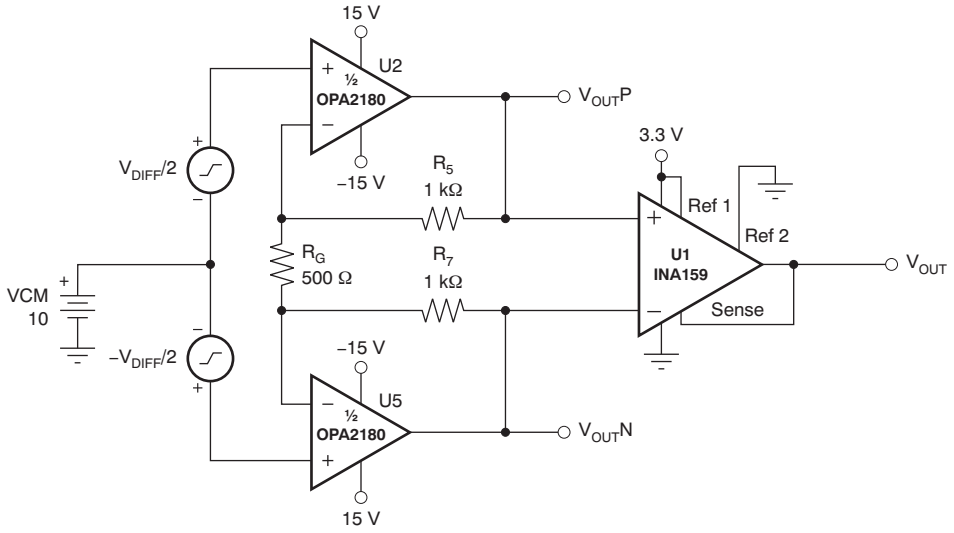
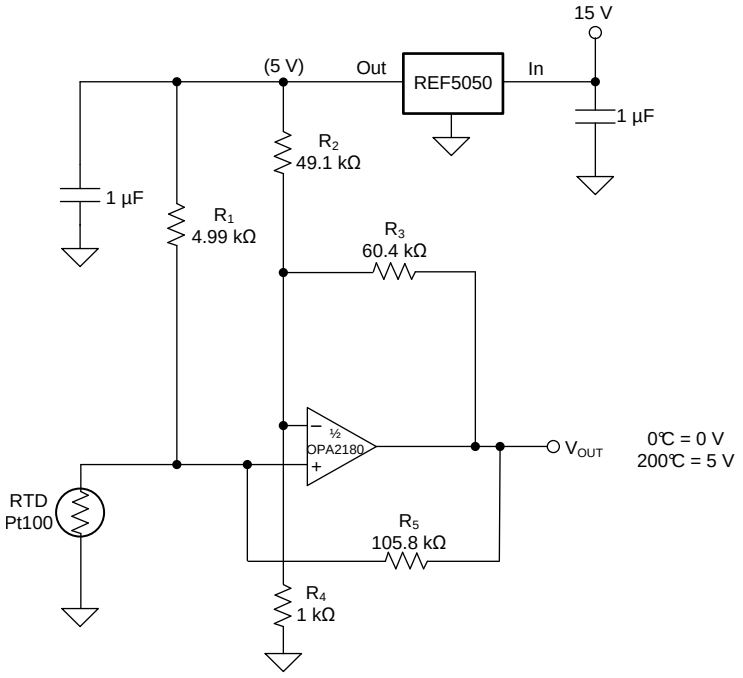


図 33. Discrete INA + Attenuation for ADC With a 3.3-V Supply

9.2.3 RTD Amplifier

The OPAx180 is excellent for use in analog linearization of resistance temperature detectors (RTDs). The circuit below (図 34) combines the precision of the OPAx180 amplifier and the precision reference of the REF5050 to linearize a Pt100 RTD.



(1) R_5 provides positive-varying excitation to linearize output.

図 34. RTD Amplifier with Linearization

10 Power Supply Recommendations

The OPAx180 family is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Layout*

注意

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout* .

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep the input traces separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 35, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

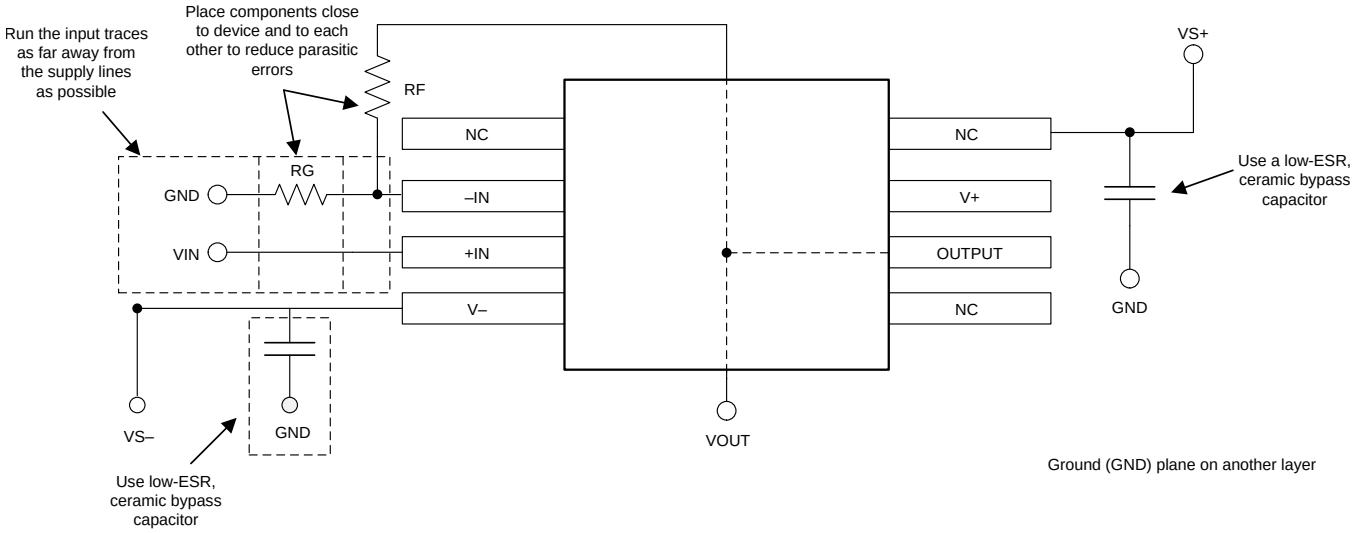


図 35. Operational Amplifier Board Layout for Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 関連リンク

表 3 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA180	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2180	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4180	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.2 商標

All trademarks are the property of their respective owners.

12.3 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA180ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA2180ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2180IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA4180ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180ID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA180, OPA2180 :

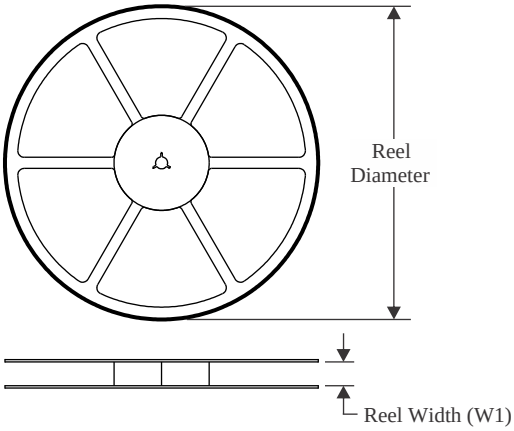
- Automotive : OPA180-Q1, OPA2180-Q1

NOTE: Qualified Version Definitions:

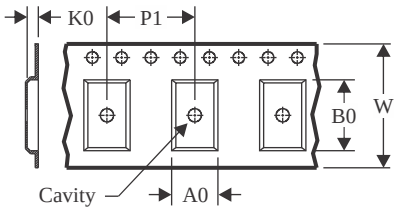
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

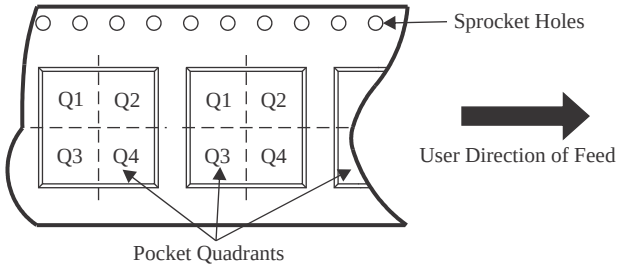


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

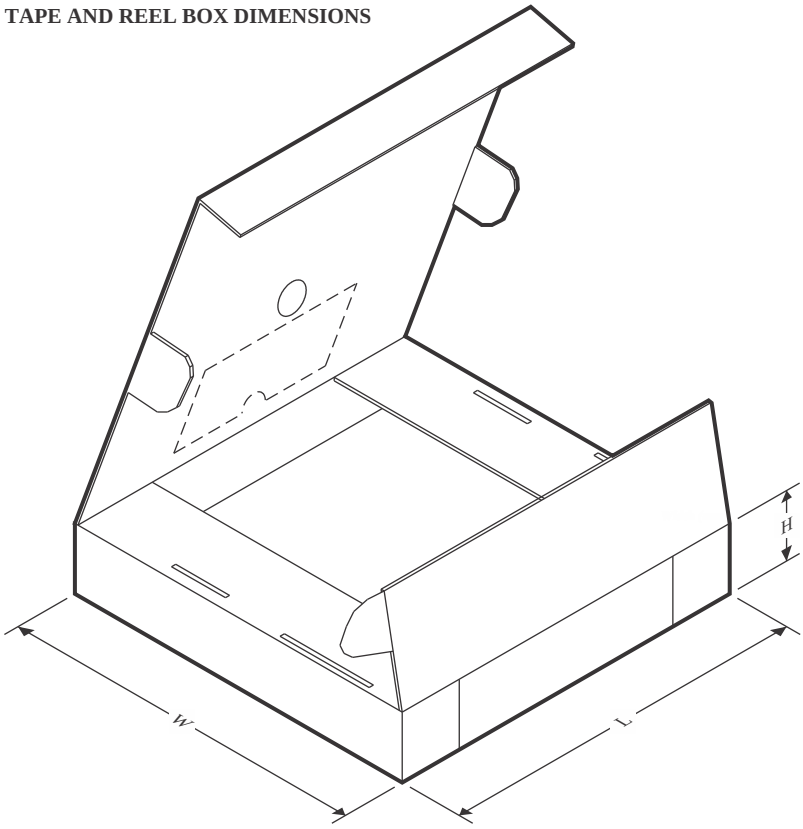
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA180IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA180IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA180IDBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA180IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA180IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA180IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2180IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2180IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2180IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4180IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4180IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4180IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

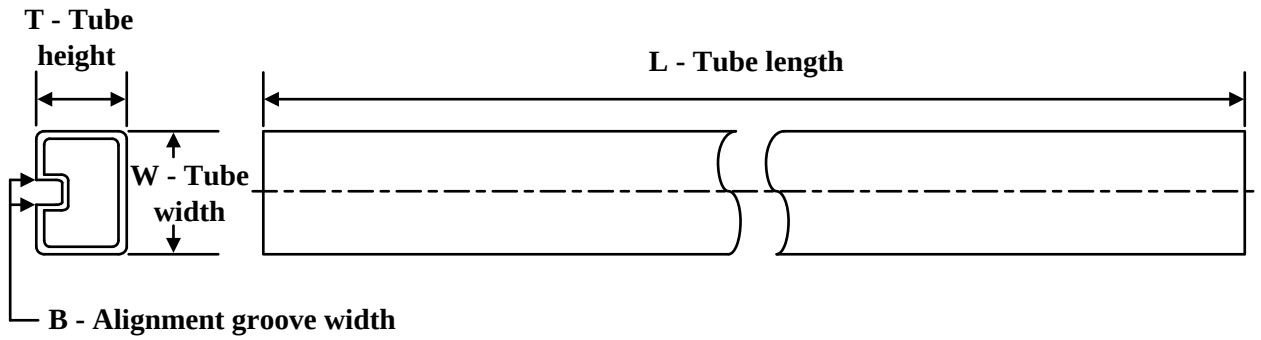
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA180IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA180IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA180IDBVTG4	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA180IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA180IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA180IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA180IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA2180IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2180IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2180IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2180IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA4180IDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4180IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA4180IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

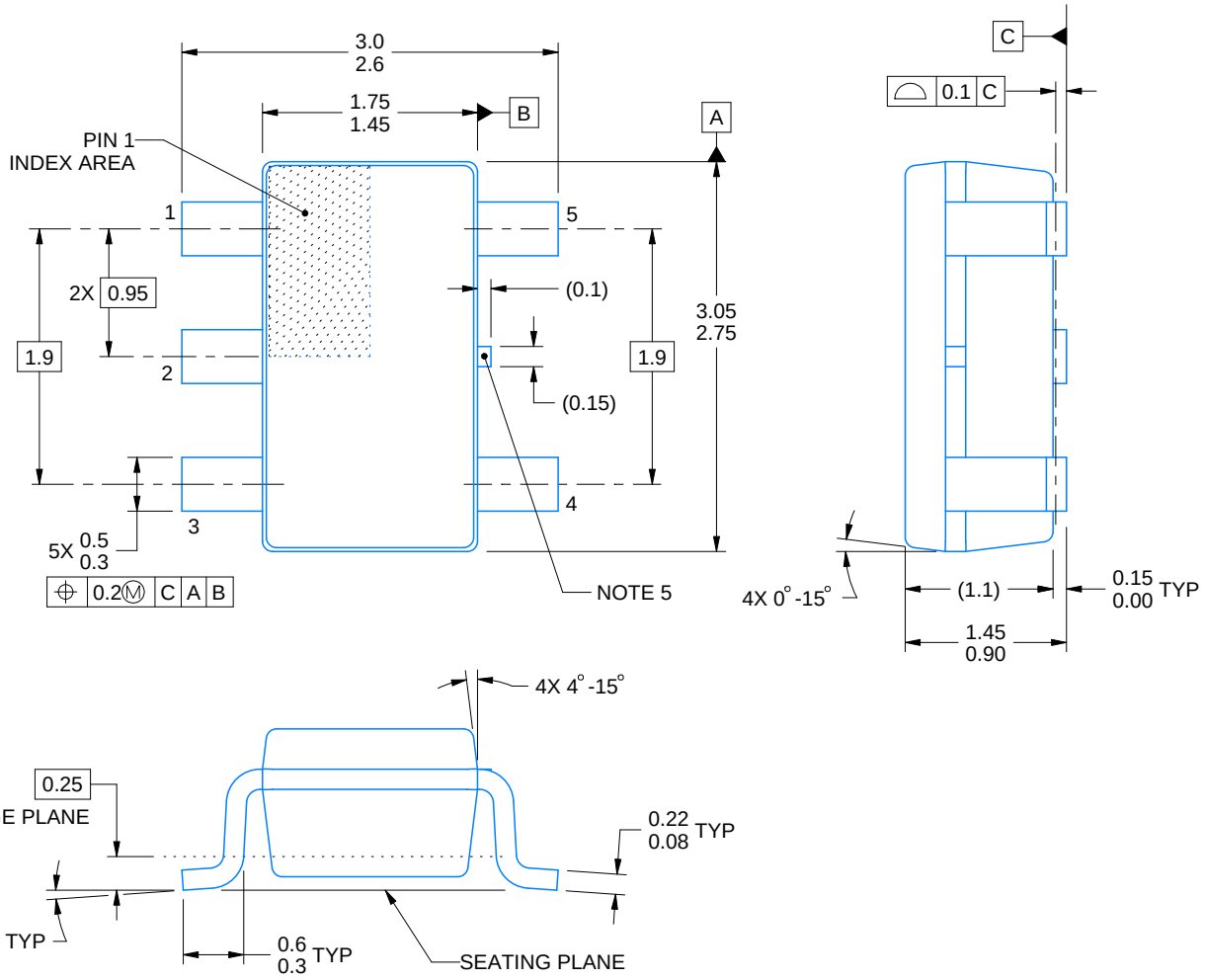
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA180ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA180ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2180IDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2180IDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4180ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4180ID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4180IPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4180IPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

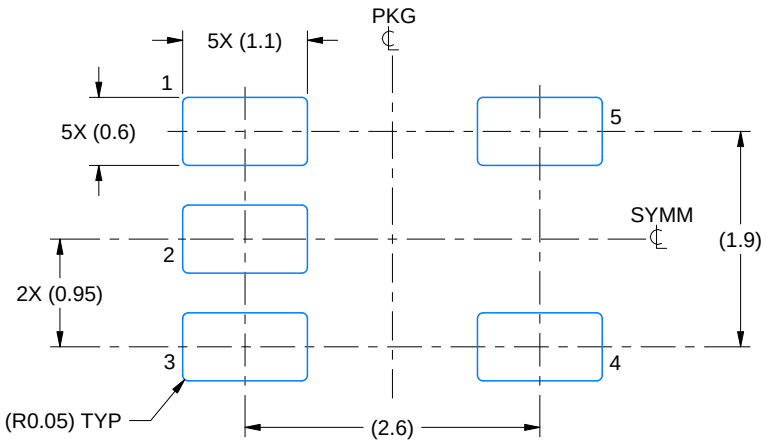
SMALL OUTLINE TRANSISTOR



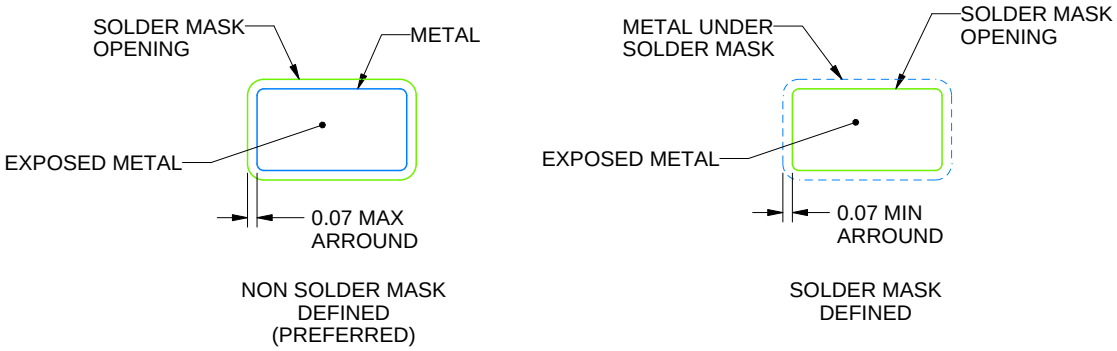
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

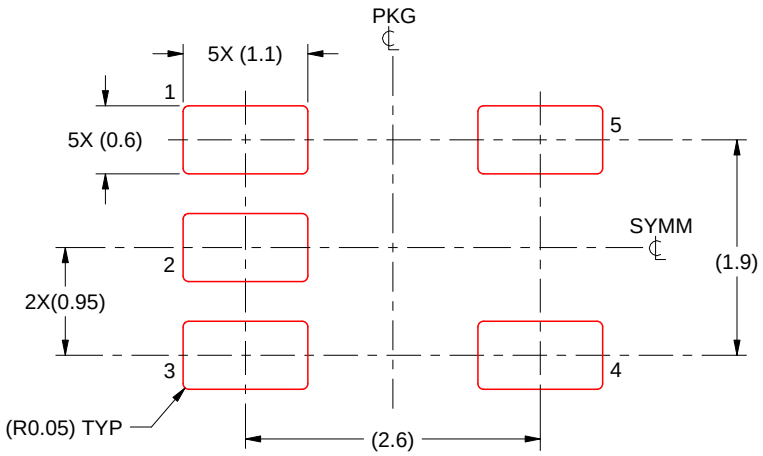


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

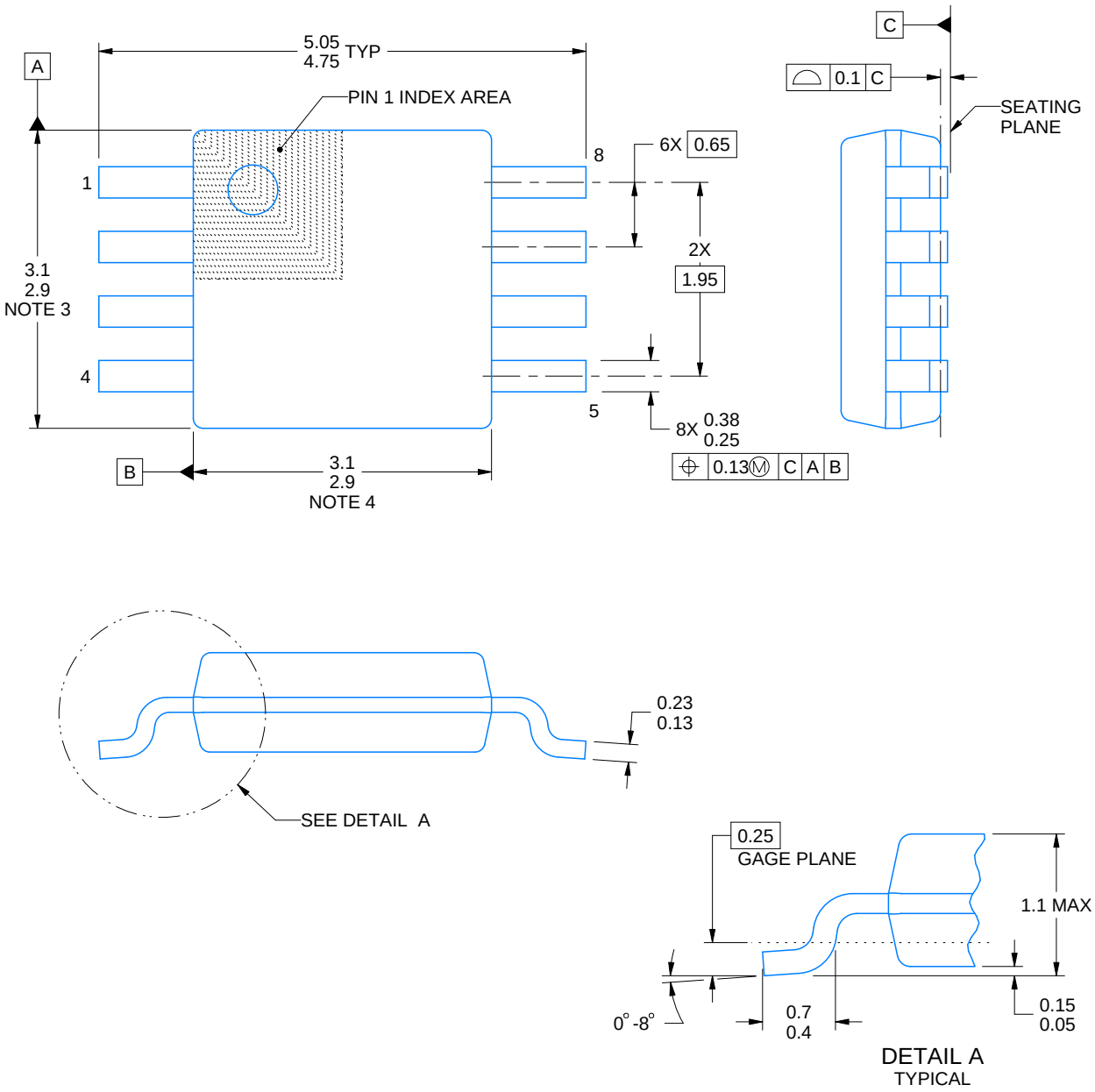
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

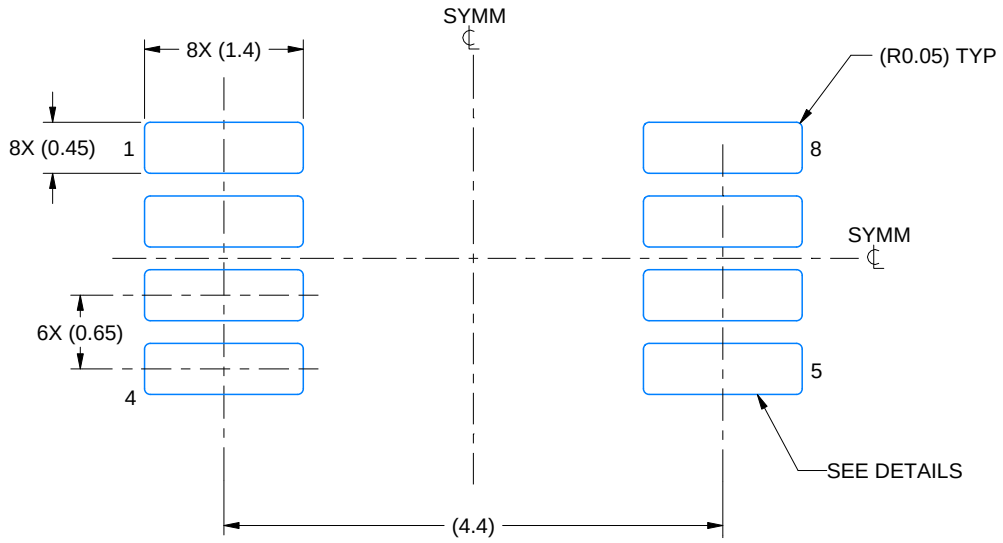
SMALL OUTLINE PACKAGE



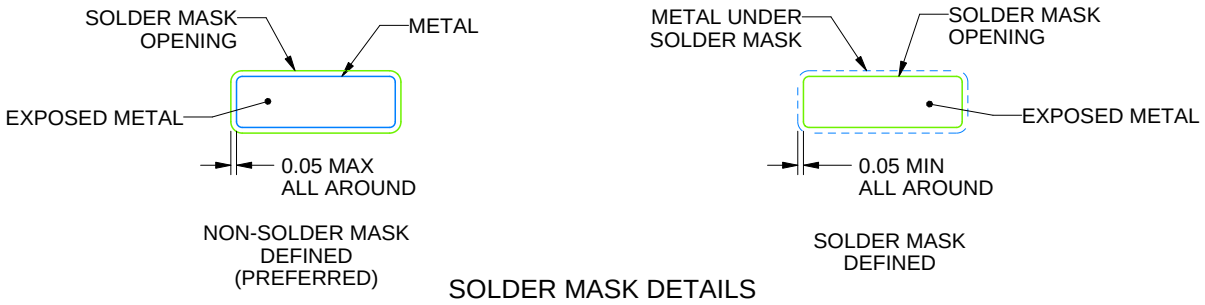
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

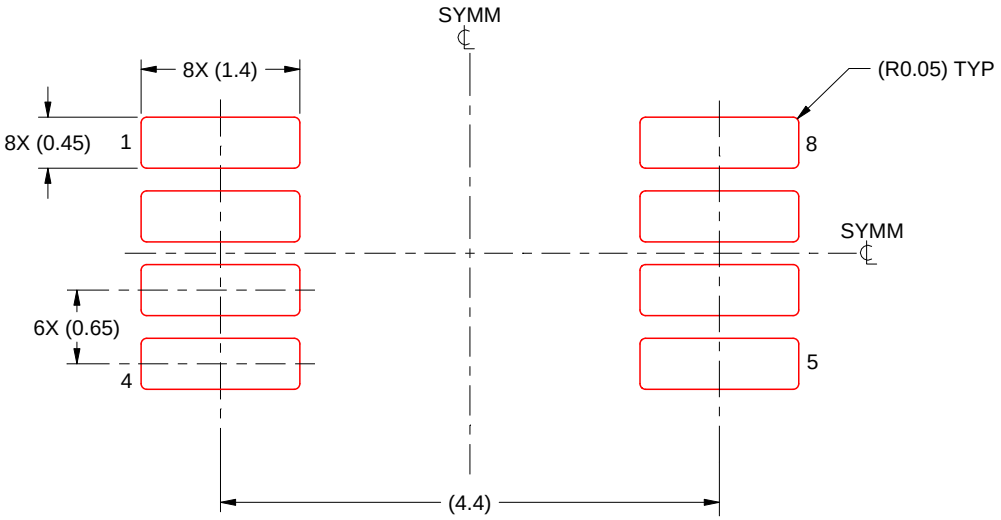


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

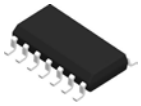


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

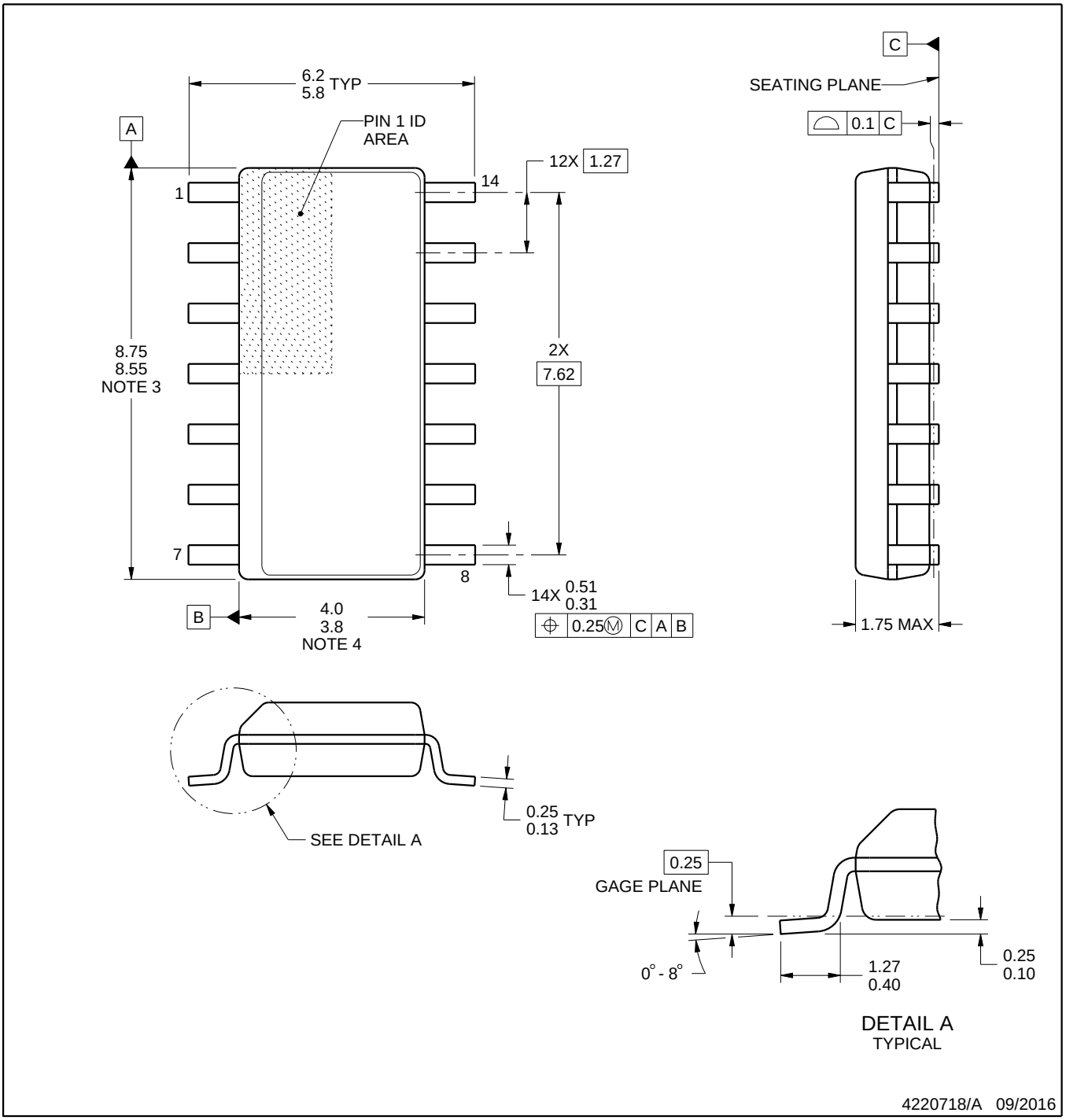


PACKAGE OUTLINE

D0014A

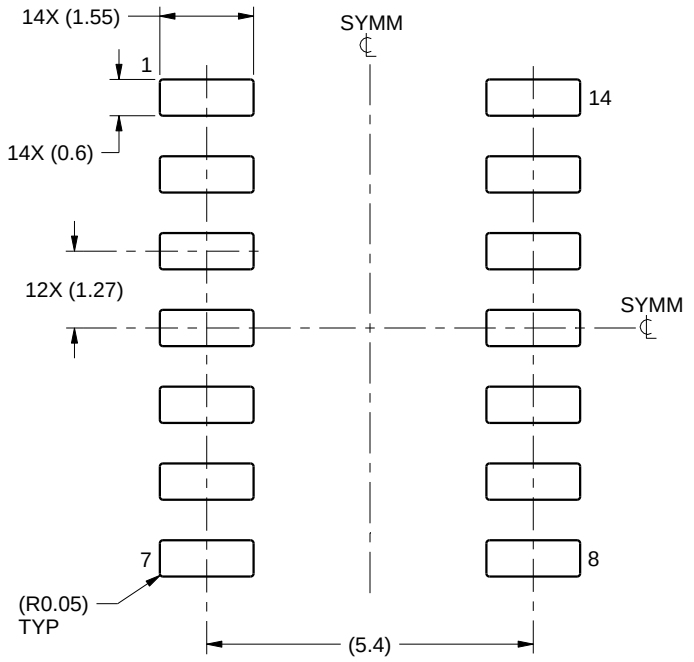
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

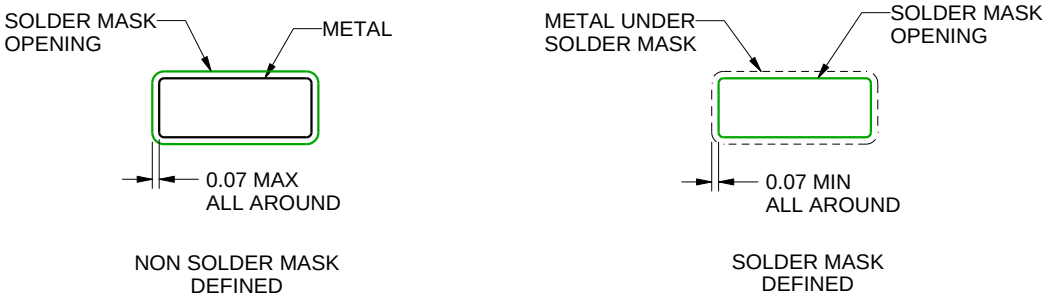


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

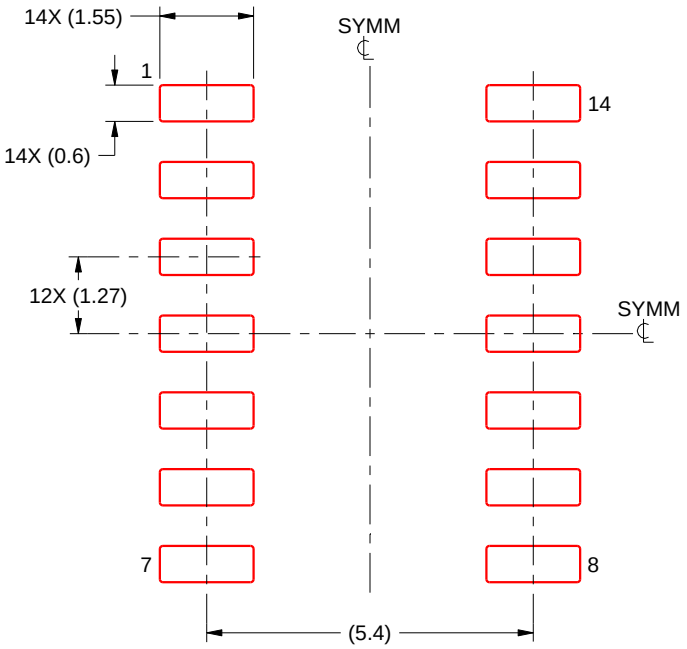
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

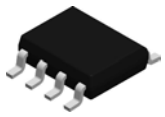


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

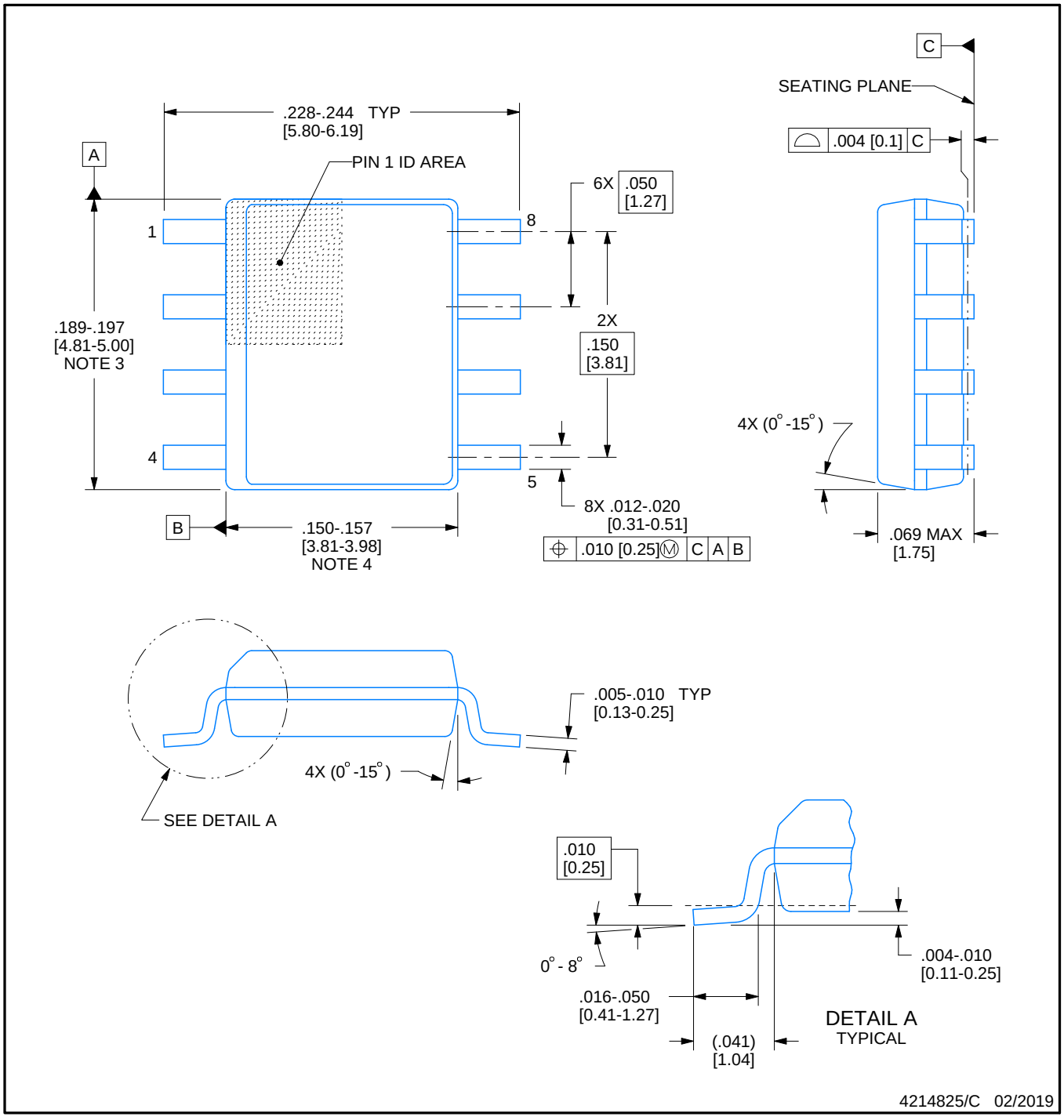


PACKAGE OUTLINE

D0008A

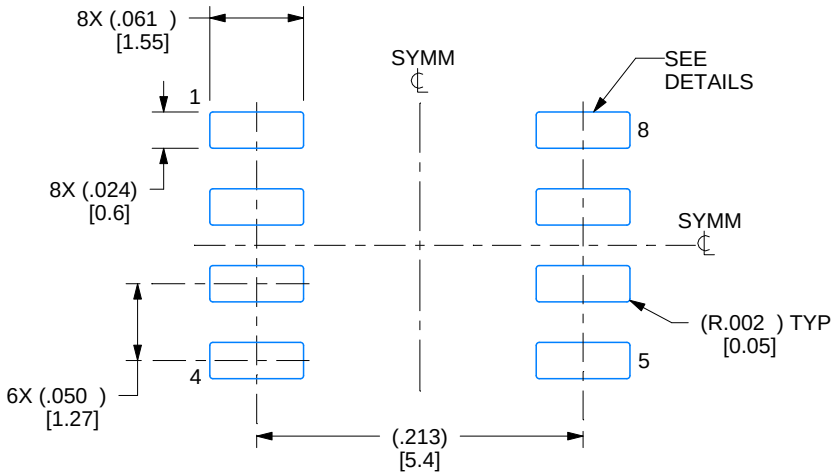
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

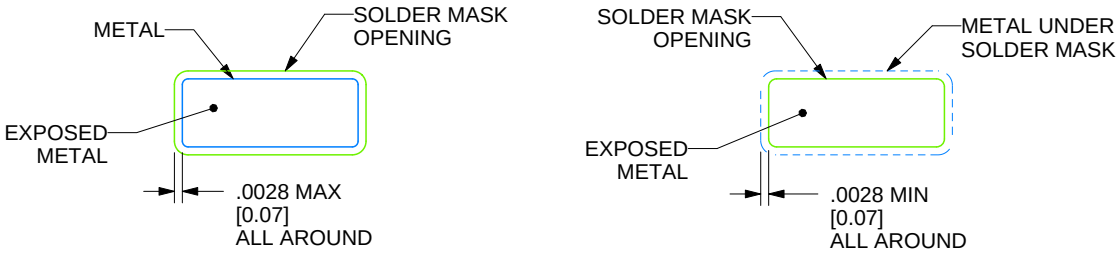


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

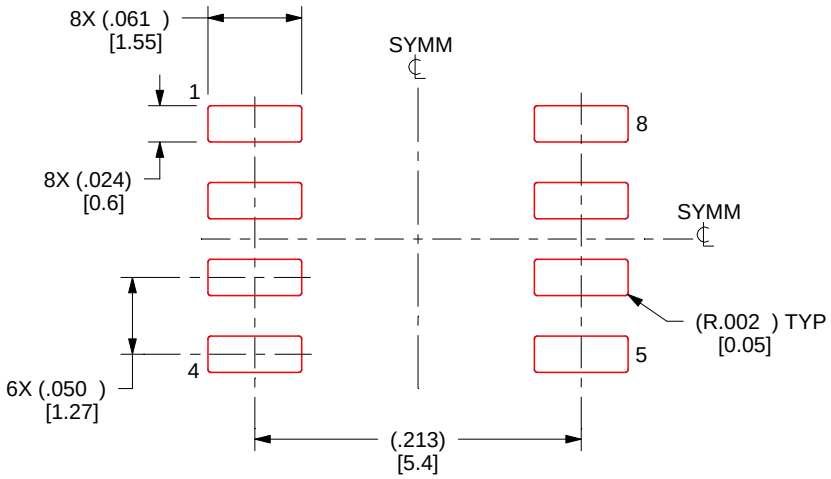
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

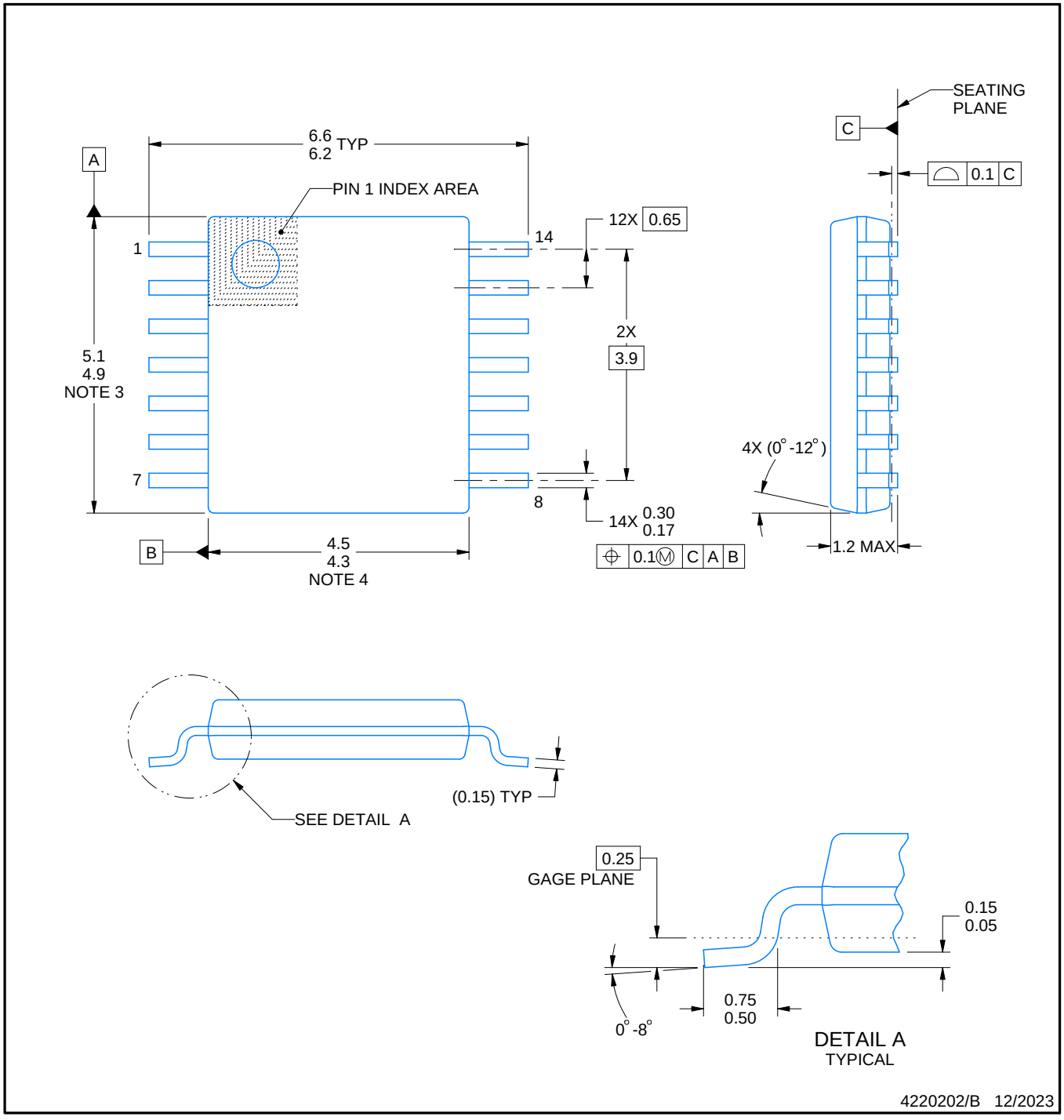
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

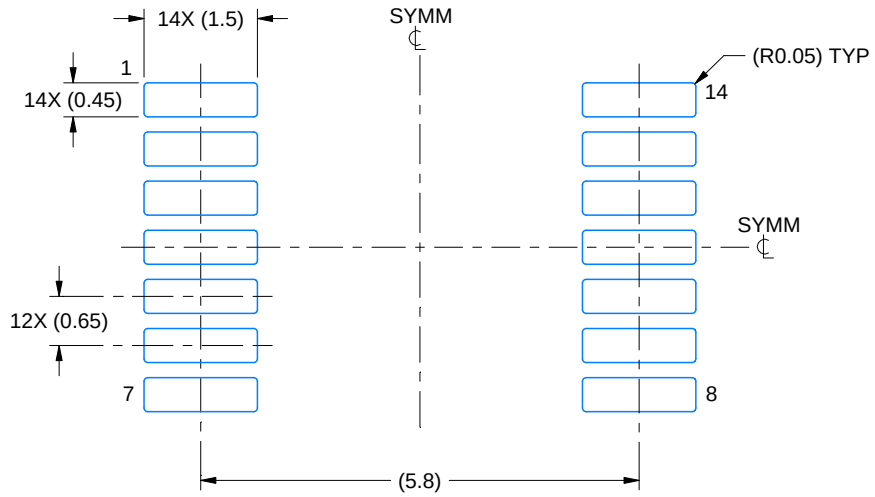
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

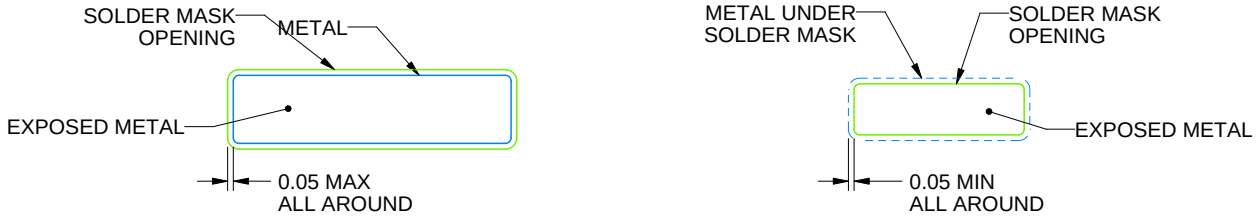


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

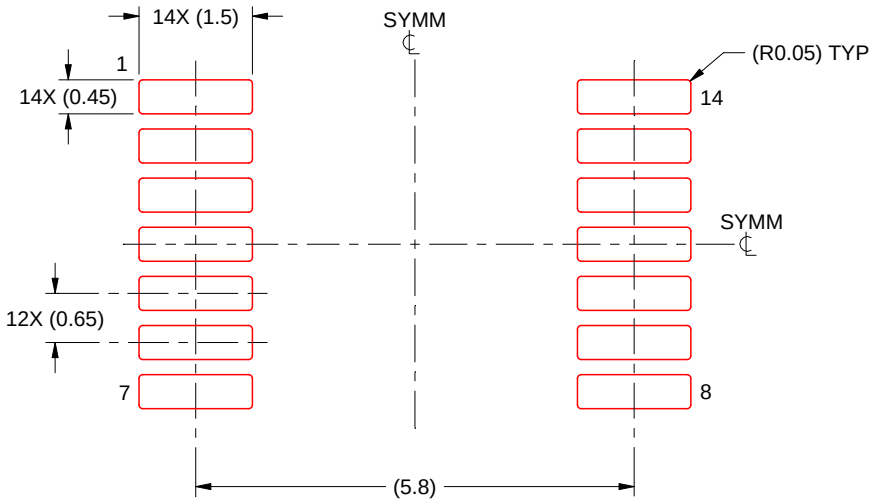


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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