

OPAx172 36V、単一電源、10MHz、レール・ツー・レール出力オペアンプ

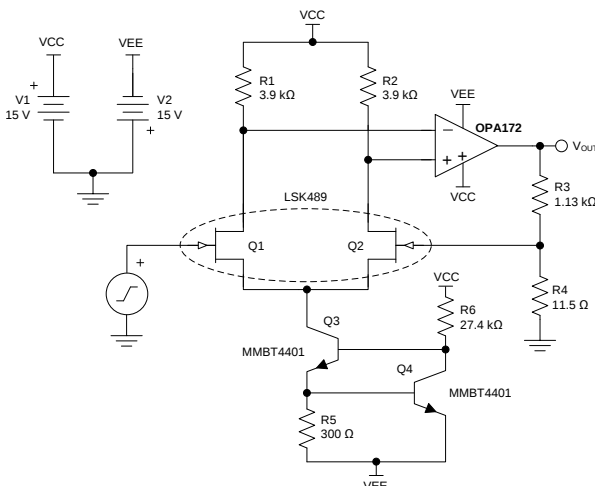
1 特長

- 広い電源電圧範囲:
+4.5V~+36V、 $\pm 2.25V \sim \pm 18V$
- 低いオフセット電圧: $\pm 0.2mV$
- 低いオフセット・ドリフト: $\pm 0.3\mu V/^\circ C$
- ゲイン帯域幅: 10MHz
- 低い入力バイアス電流: $\pm 8pA$
- 低い静止電流: アンプごとに1.6mA
- 低ノイズ: $7nV/\sqrt{Hz}$
- EMIおよびRFIフィルタ入力
- 入力範囲は負の電源電圧にも対応
- 入力範囲は正の電源電圧まで動作
- レール・ツー・レール出力
- 高い同相除去: 120dB
- 業界標準のパッケージ
 - SOIC-8、VSSOP-8、SOIC-14、TSSOP-14
- *micro*パッケージ: シングルはSC70およびSOT-23、デュアルはWSO-8

2 アプリケーション

- 電源モジュールのトラッキング・アンプ
- 商業施設の電源
- トランスデューサ・アンプ
- ブリッジ・アンプ
- 温度計測
- ひずみゲージ・アンプ
- 高精度積分器
- 試験用機器

JFET入力の低ノイズ・アンプ



3 概要

OPA172、OPA2172、OPA4172 (OPAx172)は36V、単一電源、低ノイズのオペアンプのファミリで、+4.5V ($\pm 2.25V$)~+36V ($\pm 18V$)の範囲の電源で動作できます。高電圧CMOSオペアンプの新しい追加製品として、OPAx171およびOPAx170シリーズとともに、広範なアプリケーションの要求を満たす帯域幅、ノイズ、電力オプションのファミリを提供します。OPAx172はマイクロパッケージで供給され、低いオフセット、ドリフト係数、静止電流を実現します。広い帯域幅、高速なスルー・レート、高い出力電流駆動能力も、これらのデバイスの特長です。シングル、デュアル、クワッドの各製品で同一の仕様を備え、設計の柔軟性を高めています。

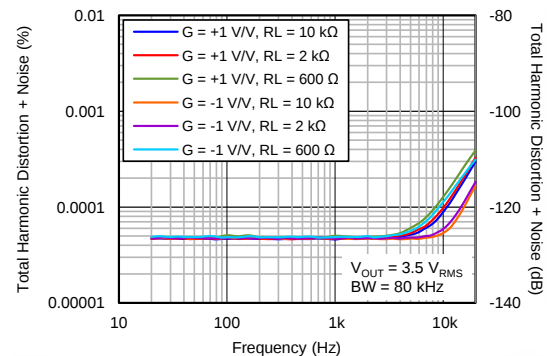
製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
OPA172	SC70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm
	SOIC (8)	4.90mm×3.91mm
OPA2172	SOIC (8)	4.90mm×3.91mm
	VSSOP (8) ⁽²⁾	3.00mm×3.00mm
	WSO (8)	3.00mm×3.00mm
OPA4172	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	4.40mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

(2) VSSOPパッケージはMSOPパッケージと同じです。

優れたTHD性能



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4 改訂履歴

Revision H (September 2015) から Revision I に変更 Page

•	Changed supply voltage values within <i>Absolute Maximum Ratings</i> table	8
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Revision G (June 2015) から Revision H に変更 Page

•	OPA2172デバイスにDRGパッケージを追加	1
•	「特長」の最後の箇条書き項目にWSONを追加	1
•	「製品情報」表にOPA2172 WSONの行を追加	1
•	Added WSON-8 to OPA2172 row of <i>Device Comparison</i> table	5
•	Added DRG pinout drawing	7
•	Added DRG column to OPA2172 and OPA4172 <i>Pin Functions</i> table	7
•	Added DRG column to OPA2172 <i>Thermal Information</i> table	9

Revision F (June 2015) から Revision G に変更 Page

•	Added input bias current (I_B) values for DGK and PW packages	10
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Revision E (December 2014) から Revision F に変更 Page

•	デバイスのステータスを「量産データ」から「混在ステータス」に変更	1
•	OPA2172 DGKおよびOPA4172 PWパッケージを量産データに変更	1
•	「製品情報」表にOPA2172 VSSOPおよびOPA4172 TSSOPの行を追加	1
•	Deleted footnote from <i>Device Comparison</i> table	5
•	Deleted footnote from OPA2172 DGK and OPA4172 PW pin out drawings	7
•	Added OPA2172 DGK thermal information	9

Revision D (September 2014) から Revision E に変更 **Page**

• OPA2172 Dパッケージを製品プレビューから量産データに変更	1
• 「製品情報」表を変更	1
• Changed <i>Device Comparison</i> table note (1) to show preview packages.....	5
• Changed <i>Handling Ratings</i> table to <i>ESD Ratings</i> table	8

Revision C (July 2014) から Revision D に変更 **Page**

• 特長の低ノイズの簡条書き項目を $6\text{nV}/\sqrt{\text{Hz}}$ から7に変更	1
• 特長の簡条書き項目でMSOPをVSSOPに変更	1
• 「製品情報」表にパッケージと新しい注2を追加	1
• Changed OPAx172 voltage noise density from $6\text{nV}/\sqrt{\text{Hz}}$ to 7 in <i>Device Family Comparison</i> table	5
• Changed OPA4172 package from DGK to PW in <i>Pin Functions</i> table	7
• Added OPA2172 <i>Thermal Information</i> table.....	9
• Changed input voltage noise value in <i>Electrical Characteristics</i> from $1.2\text{ }\mu\text{V}_{\text{PP}}$ to $2.5\text{ }\mu\text{V}_{\text{PP}}$	10
• Changed input voltage noise density value at 100 Hz in <i>Electrical Characteristics</i> from $8.6\text{ nV}/\sqrt{\text{Hz}}$ to 12	10
• Changed input voltage noise density value at 1 kHz in <i>Electrical Characteristics</i> from $6\text{ nV}/\sqrt{\text{Hz}}$ to 7.....	10
• Changed voltage output swing values in the <i>Electrical Characteristics</i>	11
• Changed 図 13	14
• Changed 図 14	14
• Added new note to Applications and Implementation section	26

Revision B (May 2014) から Revision C に変更 **Page**

• OPA4172 Dパッケージ(SOIC-14)を製品プレビューから量産データに変更	1
• Added OPA4172-D Thermal information	9
• Added Channel separation parameter to the <i>Electrical Characteristics</i>	10
• Added Channel Separation vs Frequency plot	18

Revision A (April 2014) から Revision B に変更 **Page**

• DCK (SC70)パッケージを製品プレビューから量産データに変更	1
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2013年12月発行のものから更新 **Page**

• 最新のデータシート標準に合わせてドキュメントのフォーマットを変更、「取り扱い定格」セクション、「推奨動作条件」セクション、「デバイスおよびドキュメントのサポート」セクションを追加、既存のセクションを移動	1
• Changed DCK package pin names from IN+ and IN– to +IN and –IN, respectively	6
• Changed DBV package from product preview to production data	6
• Changed 図 9	13
• Added Functional Block Diagram section.....	20
• Added Capacitive Load Drive Solution Using an Isolation Resistor section	26
• Added Power-Supply Recommendations section	29
• Changed Layout Guidelines section.....	30

5 概要（続き）

ほとんどのオペアンプでは1つの電源電圧でしか動作が規定されていないのに対して、OPAx172ファミリは+4.5V～+36Vでの動作が規定されています。電源レールの範囲外の入力信号が位相反転を起こすことはありません。通常の動作時に、入力は負のレールより100mV下、および上限レールの2V以内で動作できます。これらのデバイスは完全なレール・ツー・レール入力で、上限レールを100mV超えて動作しますが、上限レールから2V以内では性能が低下することに注意してください。

OPAx172シリーズのオペアンプは、-40°C～+125°Cでの動作が規定されています。

6 Device Comparison

6.1 Device Comparison

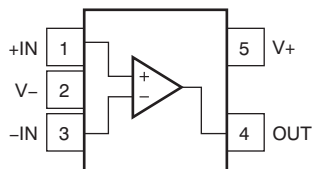
DEVICE	PACKAGE
OPA172 (single)	SC70-5, SOT-23-5, SOIC-8
OPA2172 (dual)	SOIC-8, VSSOP-8, WSON-8
OPA4172 (quad)	SOIC-14, TSSOP-14

6.2 Device Family Comparison

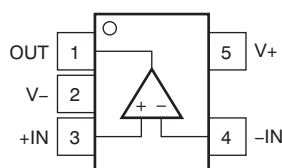
DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPAx172	1600 μ A	10 MHz	7 nV/ $\sqrt{\text{Hz}}$
OPAx171	475 μ A	3.0 MHz	14 nV/ $\sqrt{\text{Hz}}$
OPAx170	110 μ A	1.2 MHz	19 nV/ $\sqrt{\text{Hz}}$

7 Pin Configuration and Functions

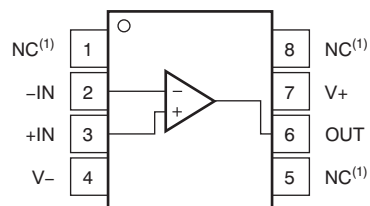
DCK Package: OPA172
SC70-5
Top View



DBV Package: OPA172
SOT-23-5
Top View



D Package: OPA172
SOIC-8
Top View

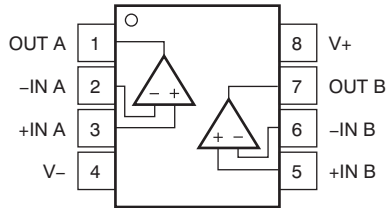


(1) No internal connection.

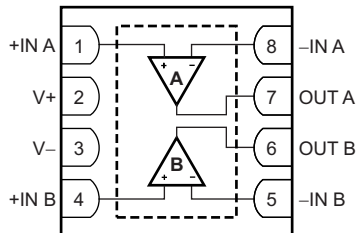
Pin Functions: OPA172

NAME	OPA172			I/O	DESCRIPTION
	D (SOIC)	DBV (SOT)	DCK (SC70)		
+IN	3	3	1	I	Noninverting input
-IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V-	4	2	2	—	Negative (lowest) power supply

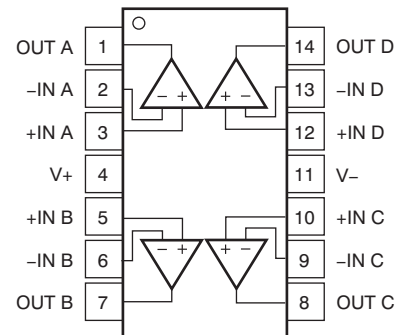
**D and DGK Packages: OPA2172
SOIC-8 and VSSOP-8
Top View**



**DRG Package: OPA2172
WSO-8
Top View**



**D and PW Packages: OPA4172
SO-14 and TSSOP-14
Top View**



Pin Functions: OPA2172 and OPA4172

NAME	PIN			I/O	DESCRIPTION
	OPA2172		OPA4172		
	D (SOIC), DGK (VSSOP)	DRG (WSO)	D (SOIC), PW (TSSOP)		
+IN A	3	1	3	I	Noninverting input, channel A
+IN B	5	4	5	I	Noninverting input, channel B
+IN C	—	—	10	I	Noninverting input, channel C
+IN D	—	—	12	I	Noninverting input, channel D
-IN A	2	8	2	I	Inverting input, channel A
-IN B	6	5	6	I	Inverting input, channel B
-IN C	—	—	9	I	Inverting input, channel C
-IN D	—	—	13	I	Inverting input, channel D
OUT A	1	7	1	O	Output, channel A
OUT B	7	6	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	8	2	4	—	Positive (highest) power supply
V-	4	3	11	—	Negative (lowest) power supply

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, [(V+) – (V-)]			40		V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential ⁽³⁾	±0.5		
Signal input pins	Current		±10		mA
Output short circuit ⁽⁴⁾			Continuous		
Operating temperature			–55	+150	°C
Junction temperature, T _J				+150	°C
Storage temperature, T _{stg}			–65	+150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
- (3) Refer to the [Electrical Overstress](#) section for more information.
- (4) Short-circuit to ground, one amplifier per package.

8.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V-)	4.5 (±2.25)	36 (±18)	V
Specified temperature	–40	125	°C

8.4 Thermal Information: OPA172

THERMAL METRIC ⁽¹⁾		OPA172			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	80.6	115.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	65.9	78.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.6	65.3	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package Thermal Metrics](#) application report.

8.5 Thermal Information: OPA2172

THERMAL METRIC ⁽¹⁾		OPA2172			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	158	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	48.6	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	78.7	36.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.5	3.9	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.1	77.3	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	6.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package Thermal Metrics](#) application report.

8.6 Thermal Information: OPA4172

THERMAL METRIC ⁽¹⁾		OPA4172		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	54.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package Thermal Metrics](#) application report.

OPA172, OPA2172, OPA4172

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8.7 Electrical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage				±0.2	±1	mV
		T _A = −40°C to +125°C				±1.15	
dV _{OS} /dT	Drift	T _A = −40°C to +125°C	OPA172, OPA4172		±0.3	±1.5	μV/°C
			OPA2172			±1.8	
PSRR	vs power supply	T _A = −40°C to +125°C			±1	±3	μV/V
	Channel separation, dc	At dc			5		μV/V
INPUT BIAS CURRENT							
I _B	Input bias current				±8	±15	pA
		T _A = −40°C to +125°C				±14	nA
		T _A = −40°C to +125°C	OPA2172IDGK			±18	
			OPA41721PW				
I _{OS}	Input offset current				±2	±15	pA
		T _A = −40°C to +125°C	OPA172, OPA4172			±1	nA
			OPA2172				
NOISE							
E _n	Input voltage noise	f = 0.1 Hz to 10 Hz			2.5		μV _{pp}
e _n	Input voltage noise density	f = 100 Hz			12		nV/√Hz
		f = 1 kHz			7		
i _n	Input current noise density	f = 1 kHz			1.6		fA/√Hz

Electrical Characteristics (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
V _{CM}	Common-mode voltage range ⁽¹⁾			(V _−) − 0.1 V	(V ₊) − 2 V		V
CMRR	Common-mode rejection ratio	V _S = ±2.25 V, (V _−) − 0.1 V < V _{CM} < (V ₊) − 2 V, T _A = −40°C to +125°C		90	104		dB
		V _S = ±18 V, (V _−) − 0.1 V < V _{CM} < (V ₊) − 2 V, T _A = −40°C to +125°C		110	120		
INPUT IMPEDANCE							
	Differential			100 4			MΩ pF
	Common-mode			6 4			10 ¹³ Ω pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	(V _−) + 0.35 V < V _O < (V ₊) − 0.35 V, R _L = 10 kΩ, T _A = −40°C to +125°C	OPA172, OPA4172	110	130		dB
			OPA2172	107	115		
		(V _−) + 0.5 V < V _O < (V ₊) − 0.5 V, R _L = 2 kΩ, T _A = −40°C to +125°C	OPA172, OPA4172		116		
			OPA2172		107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product			10			MHz
SR	Slew rate	G = +1		10			V/μs
t _S	Settling time	To 0.1%, V _S = ±18 V, G = +1, 10-V step		2			μs
		To 0.01% (12 bit), V _S = ±18 V, G = +1, 10-V step		3.2			
	Overload recovery time	V _{IN} × Gain > V _S		200			ns
THD+N	Total harmonic distortion + noise	V _S = +36 V, G = +1, f = 1 kHz, V _O = 3.5 V _{RMS}		0.00005%			
OUTPUT							
V _O	Voltage output swing from rail	V _S = +36 V	R _L = 10 kΩ	70	90		mV
			R _L = 2 kΩ	330	400		
		V _S = +36 V, T _A = −40°C to +125°C	R _L = 10 kΩ	95	120		
			R _L = 2 kΩ	470	530		
		V _S = +4.5V	R _L = 10 kΩ	10	20		
			R _L = 2 kΩ	40	50		
		V _S = +4.5 V, T _A = −40°C to +125°C	R _L = 10 kΩ	10	25		
			R _L = 2 kΩ	55	70		
I _{SC}	Short-circuit current			±75			mA
C _{LOAD}	Capacitive load drive			See Typical Characteristics			pF
Z _O	Open-loop output impedance	f = 1 MHz, I _O = 0 A		60			Ω
POWER SUPPLY							
V _S	Specified voltage range			+4.5	+36		V
I _Q	Quiescent current per amplifier	I _O = 0 A		1.6	1.8		mA
		I _O = 0 A, T _A = −40°C to +125°C			2		
TEMPERATURE							
	Specified range			−40	+125		°C

(1) The input range can be extended beyond $(V_+) - 2\text{ V}$ up to $(V_+) + 0.1\text{ V}$. For additional information, see the [Typical Characteristics](#) and [Application Information](#) sections.

8.8 Typical Characteristics: Table of Graphs

表 1. List of Typical Characteristics

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Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature ($V_S = \pm 18\text{ V}$)	Figure 3
Offset Voltage vs Common-Mode Voltage ($V_S = \pm 18\text{ V}$)	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
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Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
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PSRR vs Temperature	Figure 12
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Small-Signal Step Response (10 mV)	Figure 29 , Figure 30
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8.9 Typical Characteristics

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

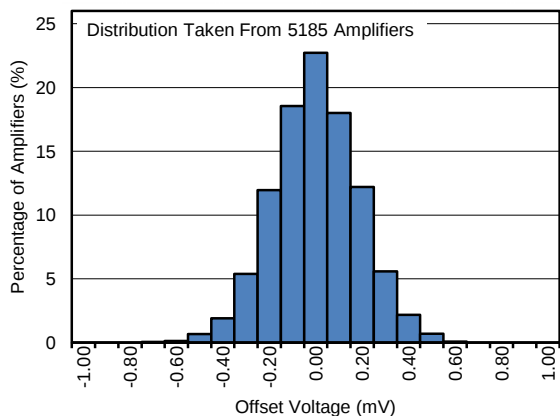


FIG 1. Offset Voltage Production Distribution

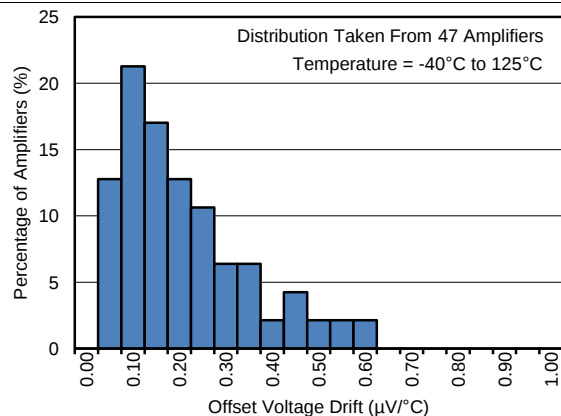


FIG 2. Offset Voltage Drift Production Distribution

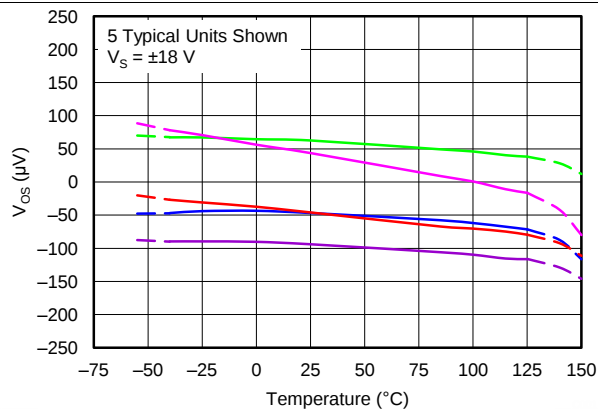


FIG 3. Offset Voltage vs Temperature
($V_S = \pm 18\text{ V}$)

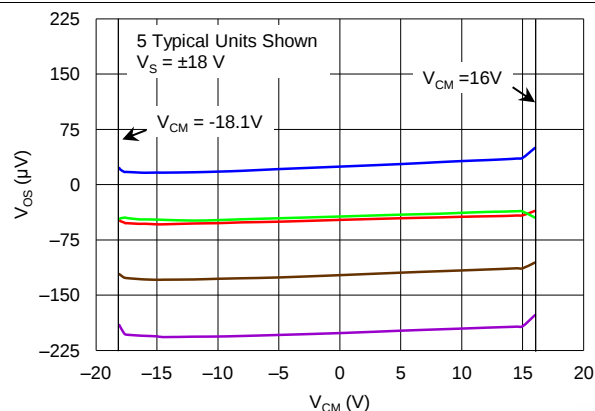


FIG 4. Offset Voltage vs Common-Mode Voltage
($V_S = \pm 18\text{ V}$)

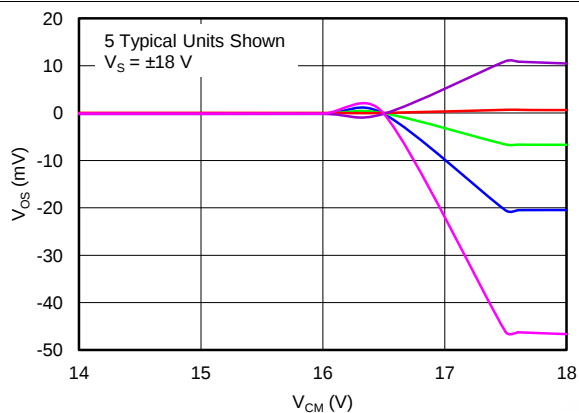


FIG 5. Offset Voltage vs Common-Mode Voltage
(Upper Stage)

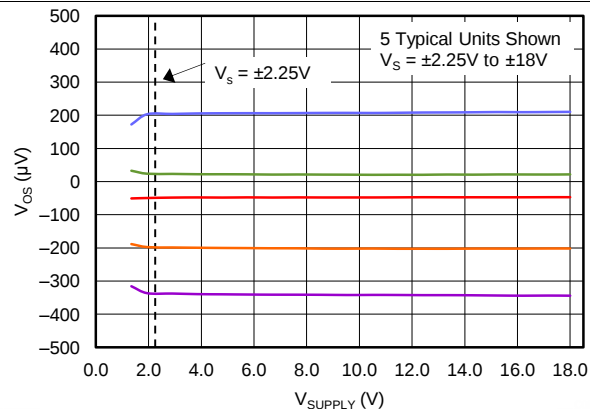


FIG 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

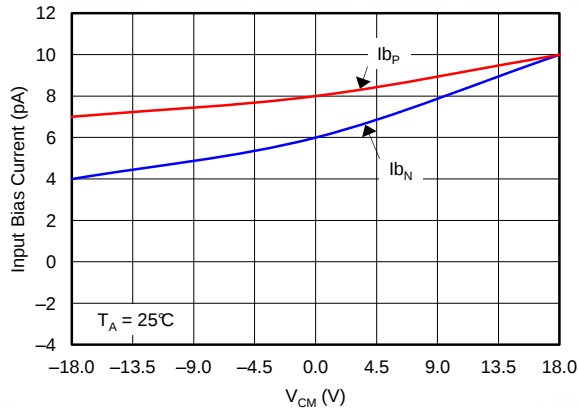


Figure 7. Input Bias Current vs Common-Mode Voltage

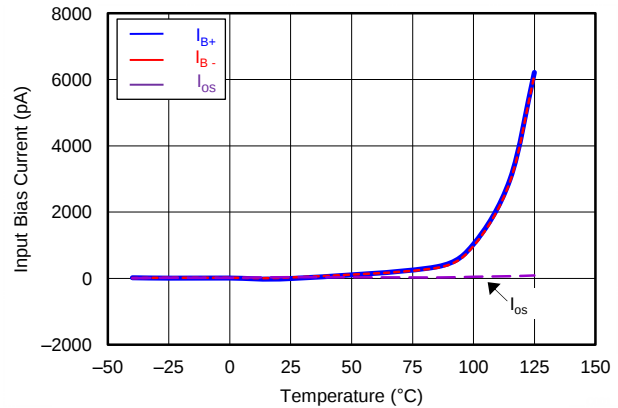


Figure 8. Input Bias Current vs Temperature

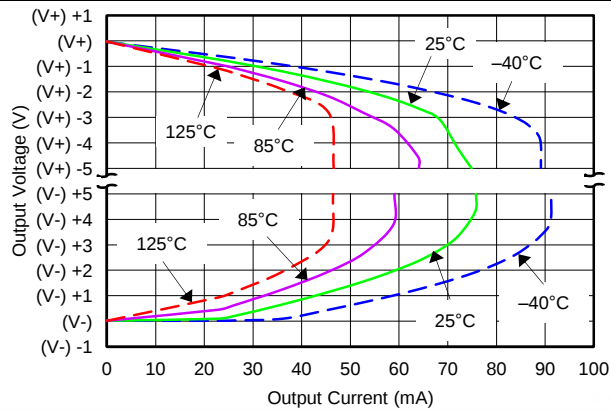


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

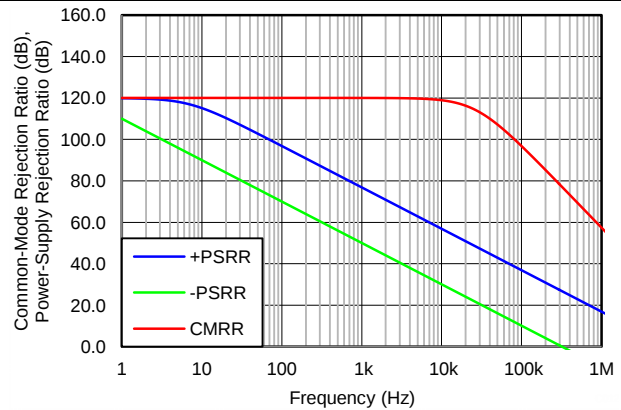


Figure 10. CMRR and PSRR vs Frequency (Referred-To-Input)

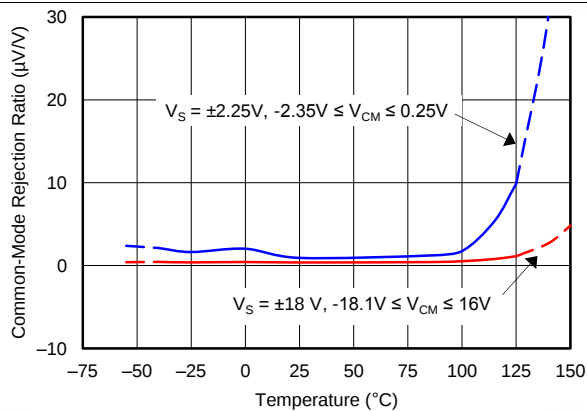


Figure 11. CMRR vs Temperature

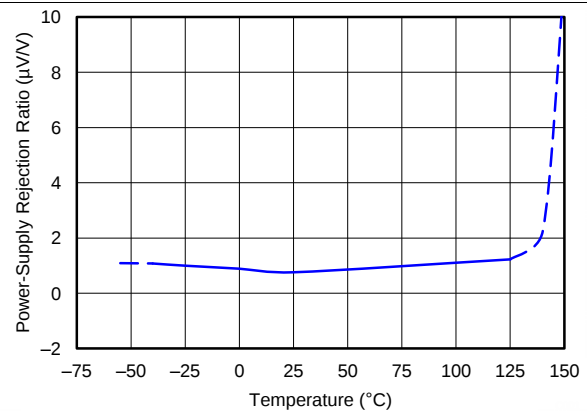


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

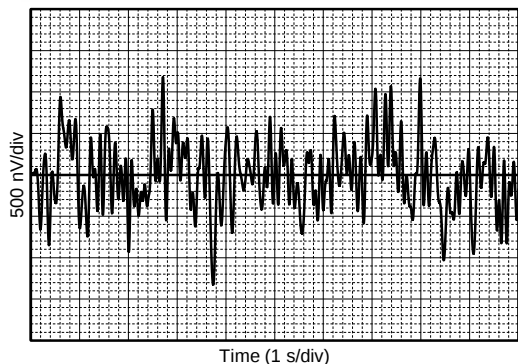


FIG 13. 0.1-Hz to 10-Hz Noise

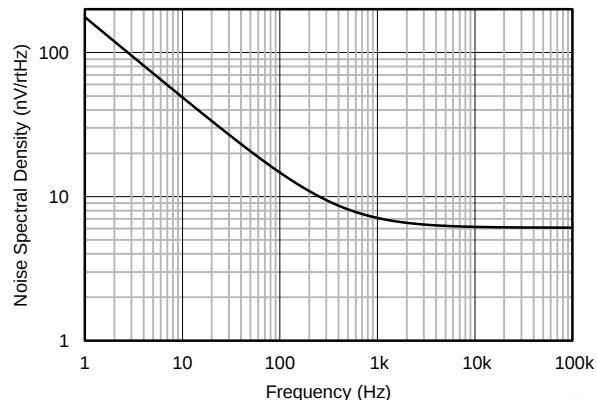


FIG 14. Input Voltage Noise Spectral Density vs Frequency

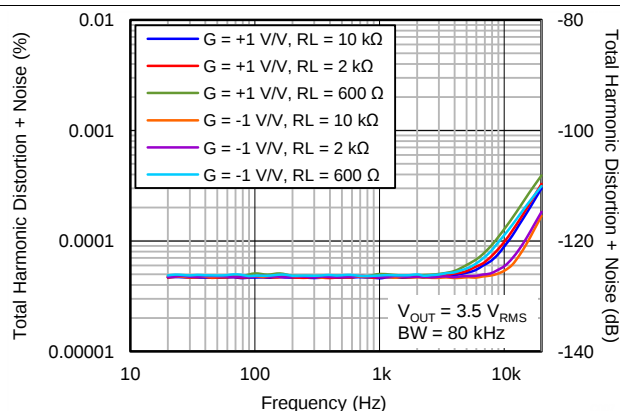


FIG 15. THD+N Ratio vs Frequency

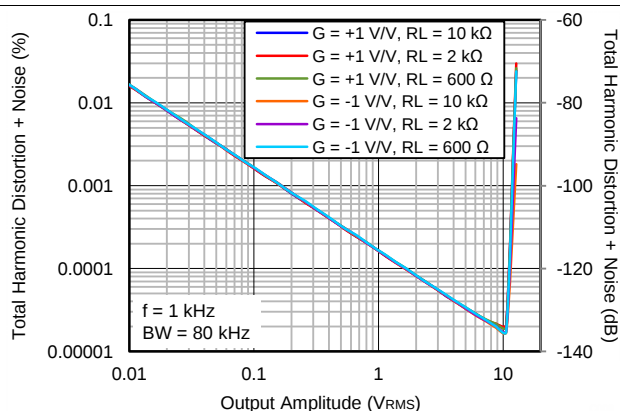


FIG 16. THD+N vs Output Amplitude

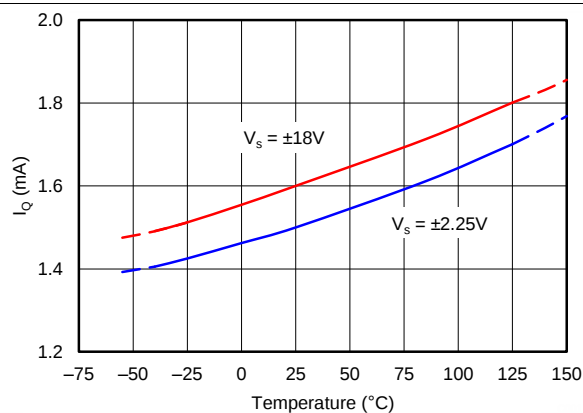


FIG 17. Quiescent Current vs Temperature

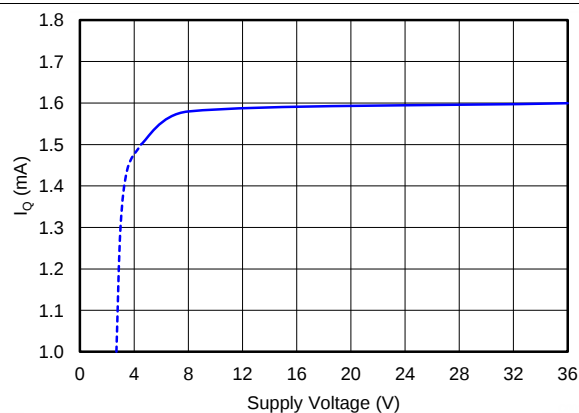


FIG 18. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

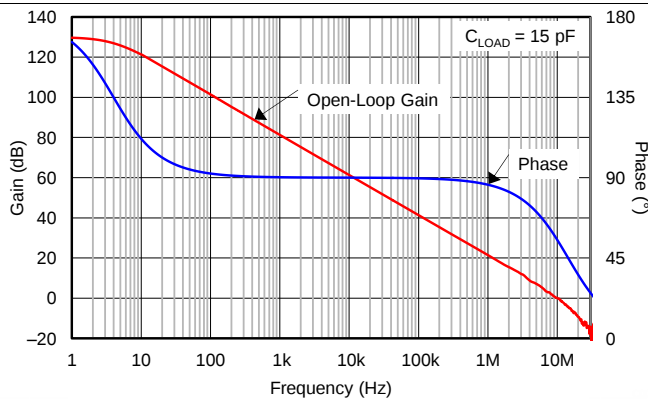


Figure 19. Open-Loop Gain and Phase vs Frequency

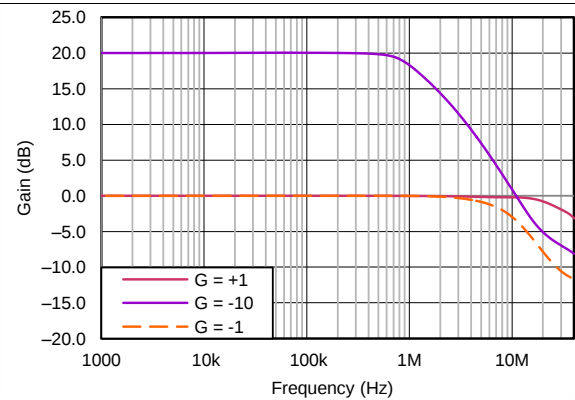


Figure 20. Closed-Loop Gain vs Frequency

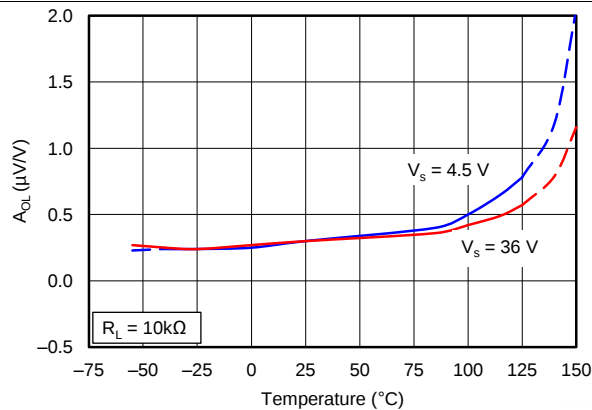


Figure 21. Open-Loop Gain vs Temperature

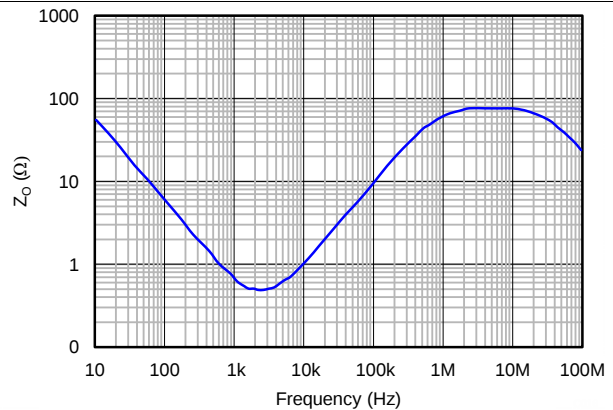


Figure 22. Open-Loop Output Impedance vs Frequency

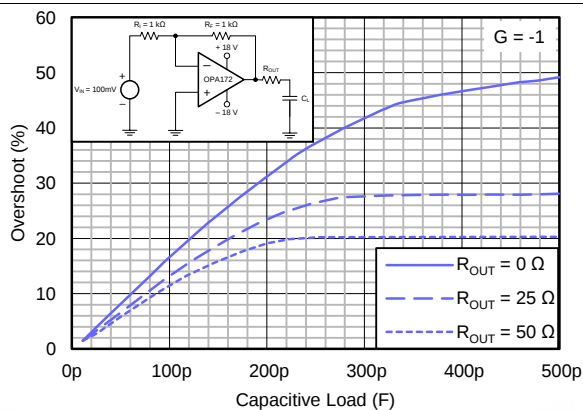


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

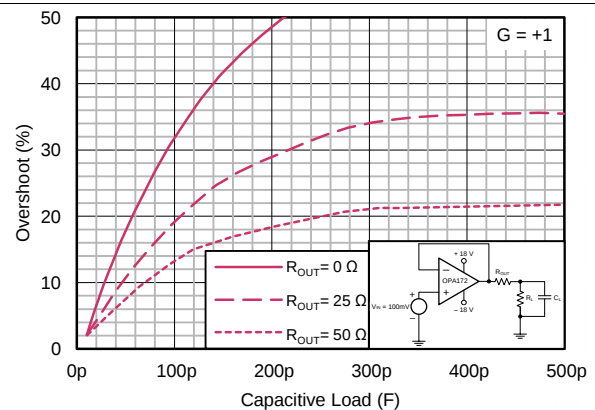


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

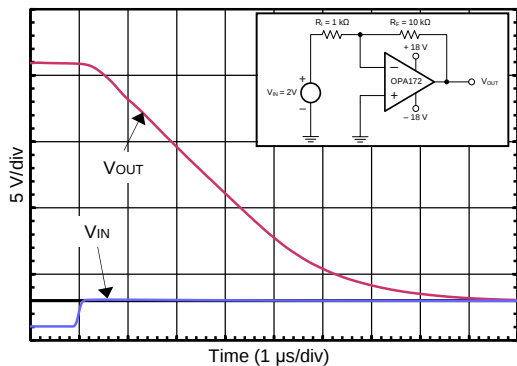


FIG 25. Positive Overload Recovery

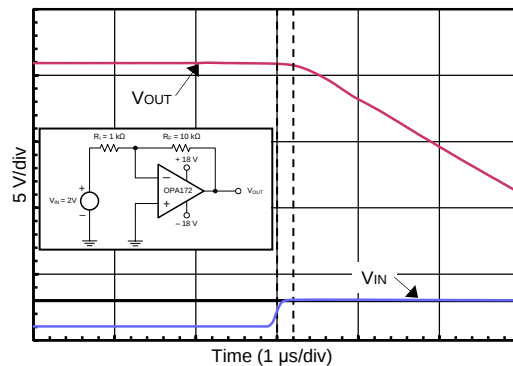


FIG 26. Positive Overload Recovery (Zoomed In)

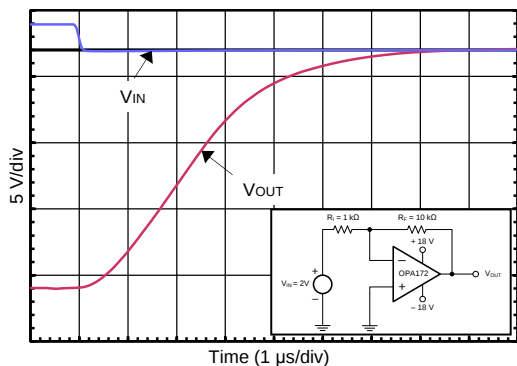


FIG 27. Negative Overload Recovery

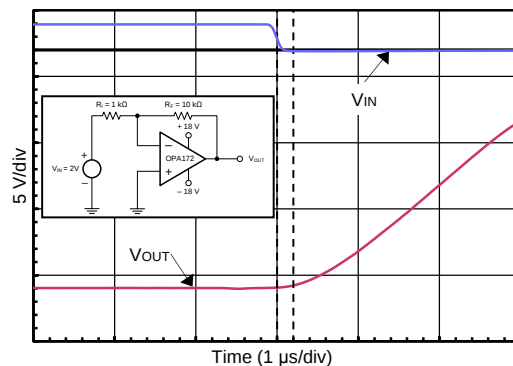


FIG 28. Negative Overload Recovery (Zoomed In)

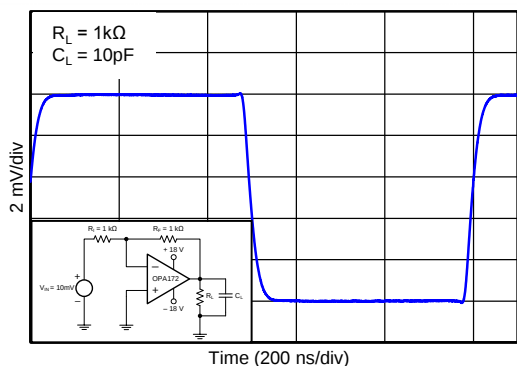


FIG 29. Small-Signal Step Response (10 mV, $G = -1$)

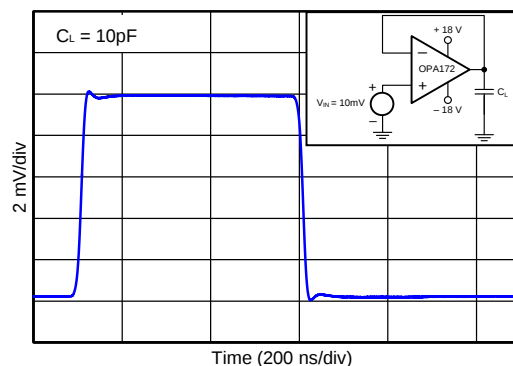


FIG 30. Small-Signal Step Response (10 mV, $G = +1$)

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

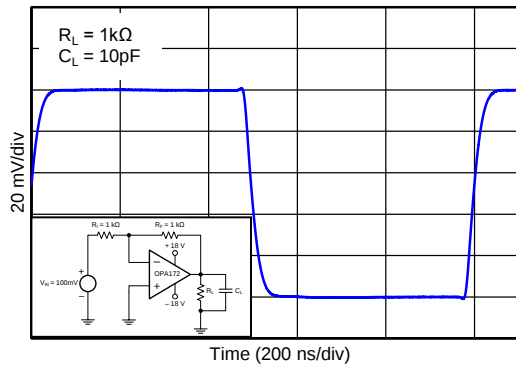


Figure 31. Small-Signal Step Response (100 mV, $G = -1$)

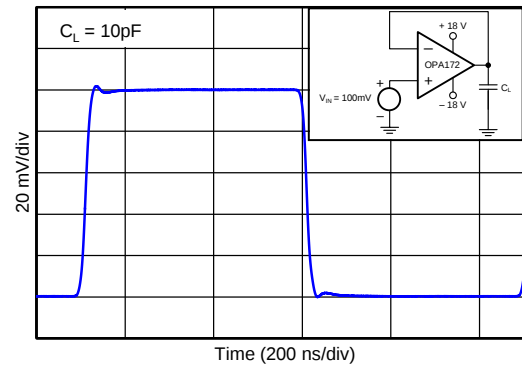


Figure 32. Small-Signal Step Response (100 mV, $G = +1$)

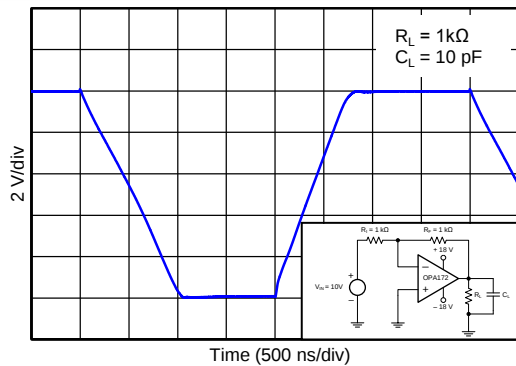


Figure 33. Large-Signal Step Response (10 V, $G = -1$)

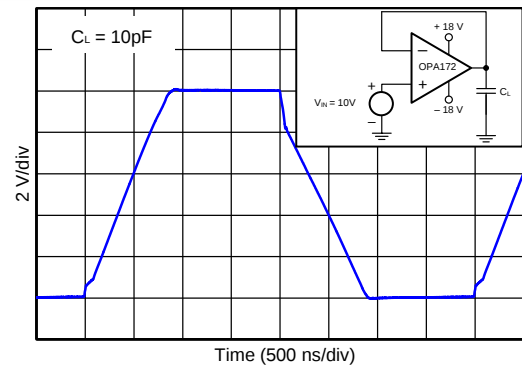


Figure 34. Large-Signal Step Response (10 V, $G = +1$)

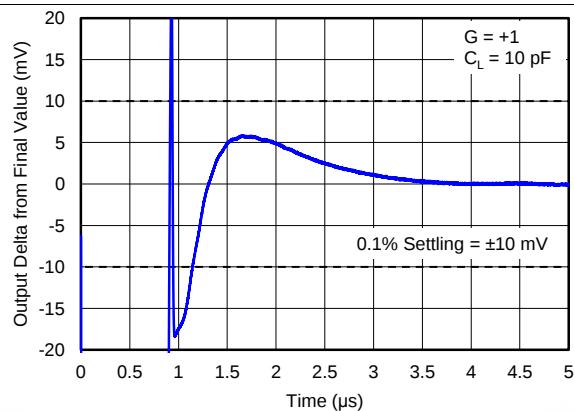


Figure 35. Large-Signal Settling Time (10-V Positive Step)

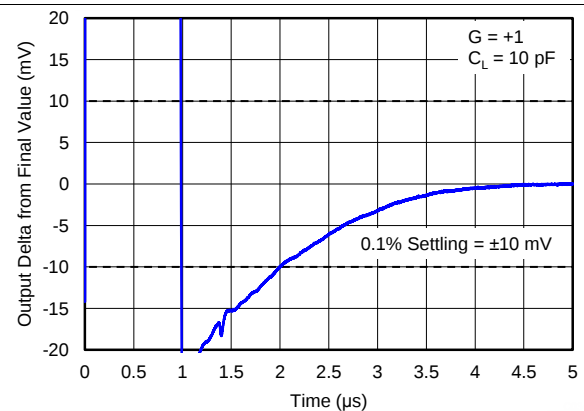


Figure 36. Large-Signal Settling Time (10-V Negative Step)

Typical Characteristics (continued)

At $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

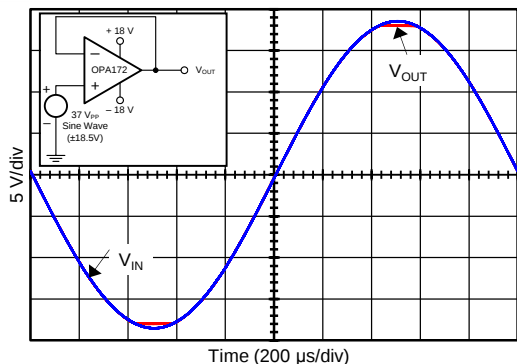


Figure 37. No Phase Reversal

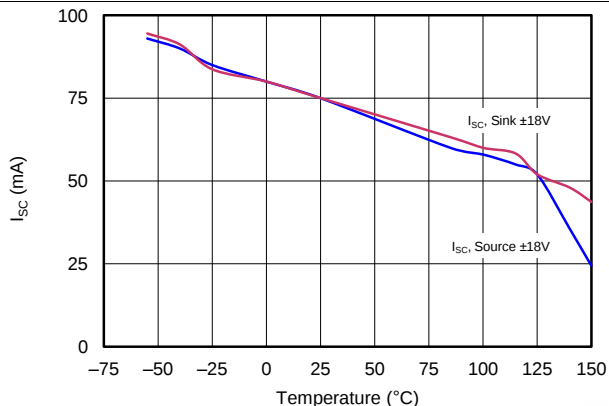


Figure 38. Short-Circuit Current vs Temperature

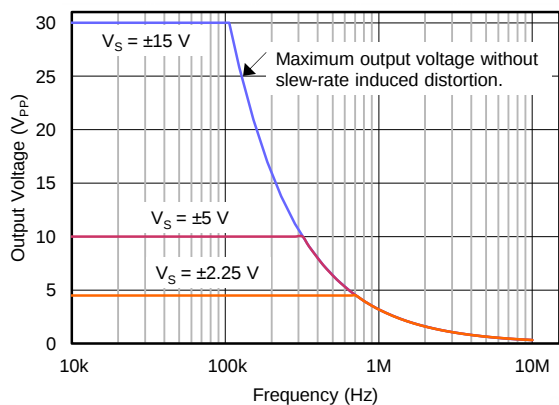


Figure 39. Maximum Output Voltage vs Frequency

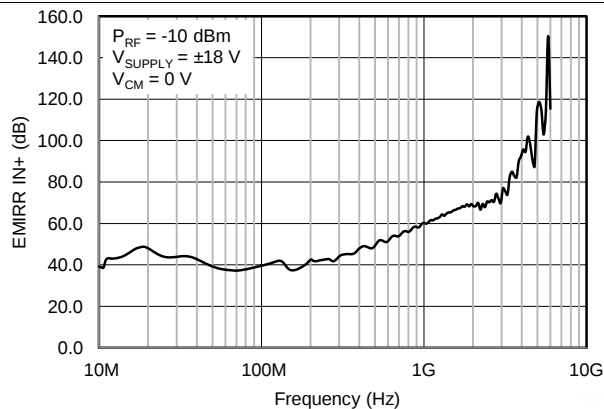


Figure 40. EMIRR vs Frequency

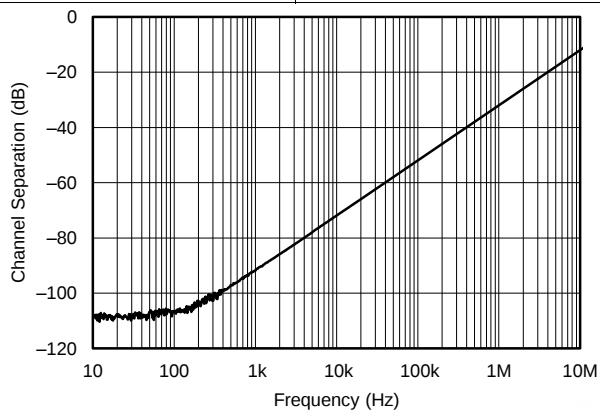


Figure 41. Channel Separation vs Frequency

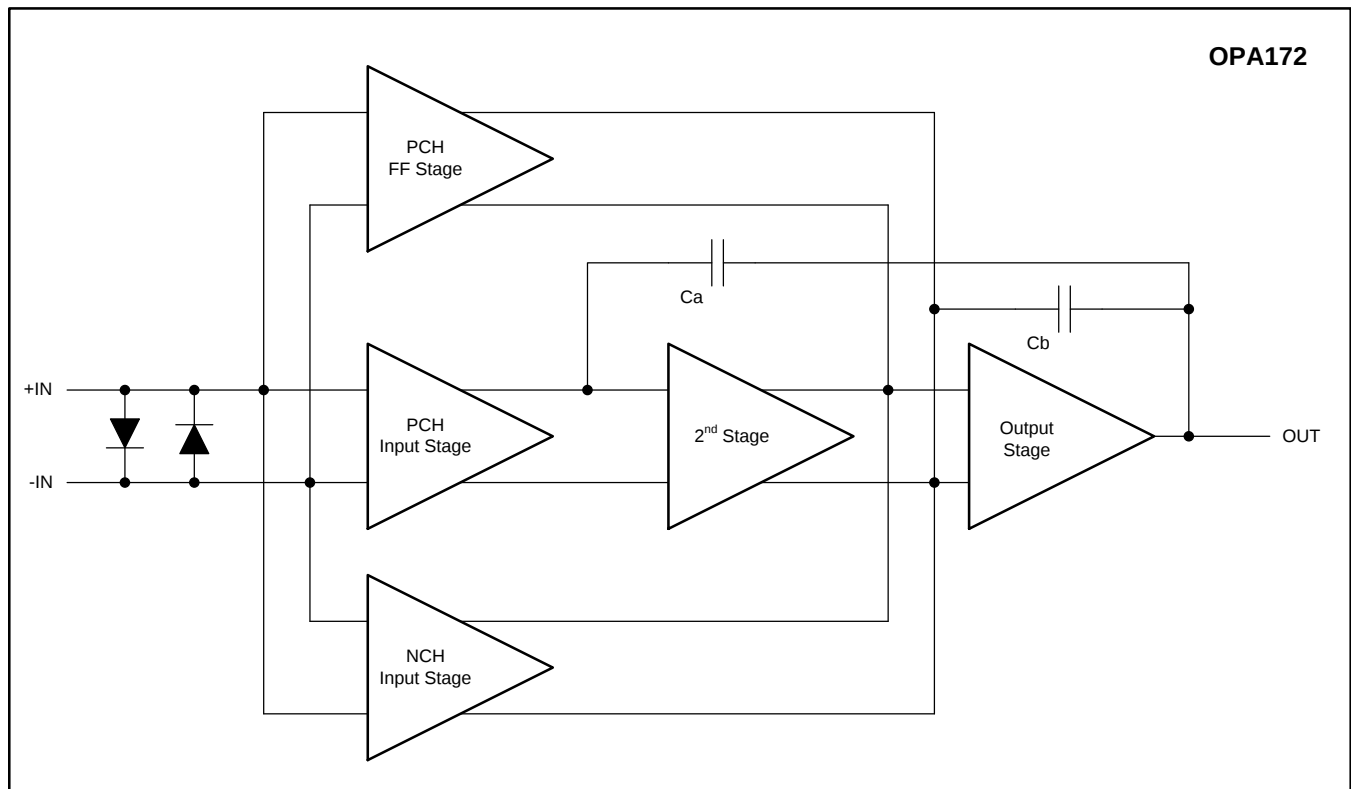
9 Detailed Description

9.1 Overview

The OPAx172 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only $1.5 \mu\text{V}/^\circ\text{C}$ (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL} , and superior THD.

The [Functional Block Diagram](#) section shows the simplified diagram of the OPA172 design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 EMI Rejection

The OPAx172 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx172 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 42 shows the results of this testing on the OPAx172. 表 2 shows the EMIRR IN+ values for the OPAx172 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in Application Report [SBOA128](#), *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

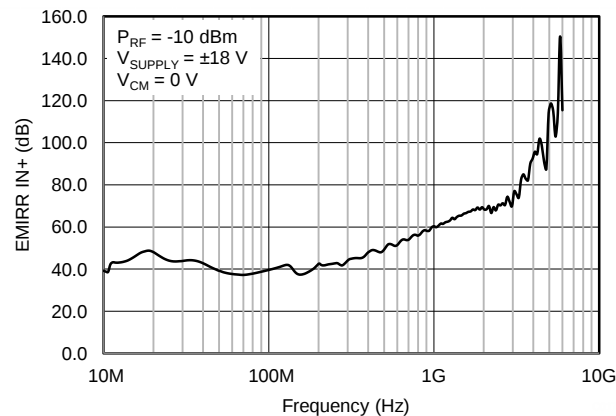


図 42. EMIRR Testing

表 2. OPAx172 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	114 dB

9.3.2 Phase-Reversal Protection

The OPAx172 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx172 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in [Figure 43](#).

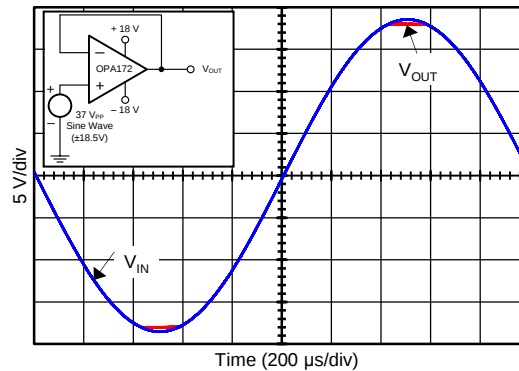


Figure 43. No Phase Reversal

9.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx172 are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT} = 50 \Omega$) in series with the output. [Figure 44](#) and [Figure 45](#) show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Refer to Application Bulletin [SBOA015 \(AB-028\)](#), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

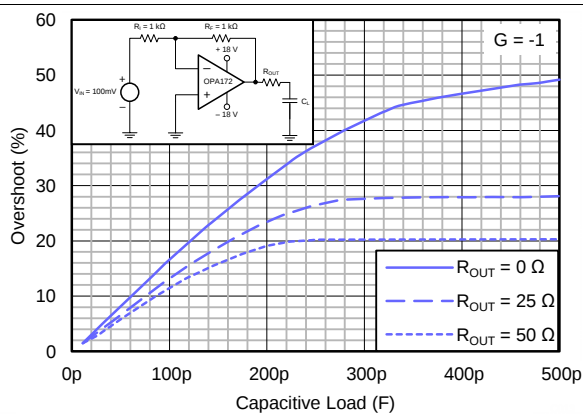


Figure 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

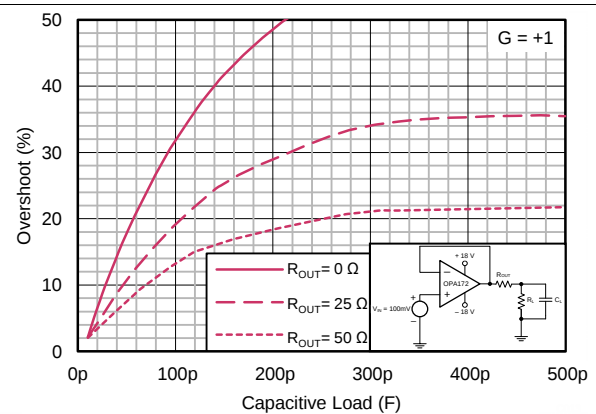


Figure 45. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

9.4 Device Functional Modes

9.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx172 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 3.

表 3. Typical Performance Range ($V_S = \pm 18\text{ V}$)

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	$(V+) - 2$		$(V+) + 0.1$	V
Offset voltage		5		mV
Offset voltage vs temperature ($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$)		10		$\mu\text{V}/^\circ\text{C}$
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/ μs
Noise at $f = 1\text{ kHz}$		22		nV/ $\sqrt{\text{Hz}}$

9.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage terminals or even the output terminal. Each of these different terminal functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the terminal. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful.  46 illustrates the ESD circuits contained in the OPAx172 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output terminals and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

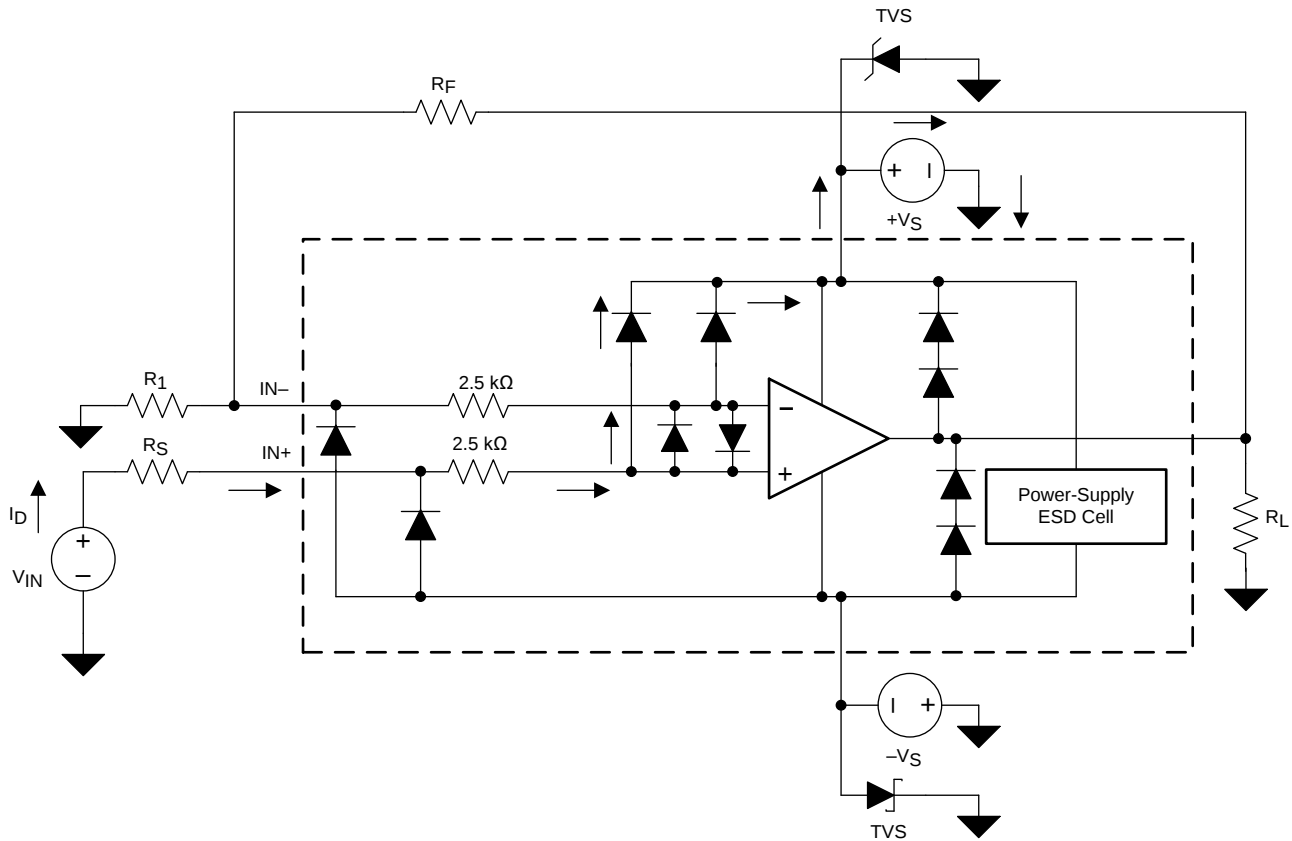


FIG 46. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in FIG 46), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

FIG 46 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $-V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply terminals; see [Figure 46](#). Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAX172 input terminals are protected from excessive differential voltage with back-to-back diodes; see [Figure 46](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAX172. [Figure 46](#) illustrates an example configuration that implements a current-limiting feedback resistor.

9.4.3 Overload Recovery

Overload recovery is defined as the time it takes for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAX172 is approximately 200 ns.

10 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

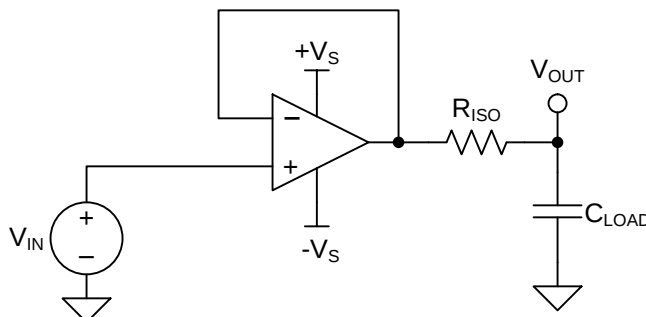
The OPAx172 family of amplifiers is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V). Many of the specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

10.2 Typical Applications

The following application examples highlight only a few of the circuits where the OPAx172 can be used.

10.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPA172 can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.



✎ 47. Unity-Gain Buffer with R_{ISO} Stability Compensation

10.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (± 15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μF , 0.1 μF , and 1 μF
- Phase margin: 45° and 60°

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

Figure 47 depicts a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 47. Not depicted in Figure 47 is the open-loop output resistance of the op amp, R_o .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by $(R_o + R_{ISO})$ and C_{LOAD} . Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB per decade. Figure 48 shows the concept. Note that the $1/\beta$ curve for a unity-gain buffer is 0 dB.

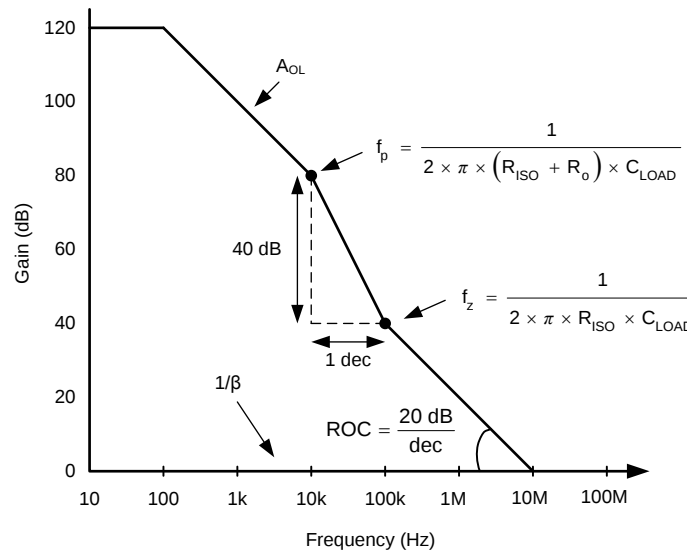


Figure 48. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 4 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA172, refer to the precision design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

Table 4. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

10.2.1.3 Application Curve

The OPA172 meets the supply voltage requirements of 30 V. The OPA172 is tested for various capacitive loads and R_{ISO} is adjusted to get an overshoot corresponding to 表 4. The results of these tests are summarized in 图 49.

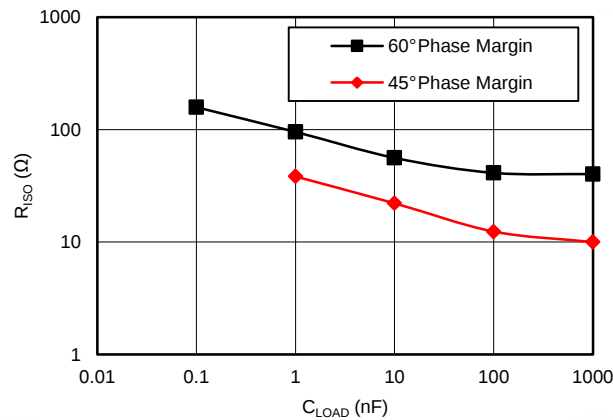


图 49. R_{ISO} VS C_{LOAD}

10.2.2 Bidirectional Current Source

The improved Howland current-pump topology shown in 图 50 provides excellent performance because of the extremely tight tolerances of the on-chip resistors of the INA132. By buffering the output using an OPA172, the output current the circuit is able to deliver is greatly extended.

The circuit dc transfer function is shown in 式 2:

$$I_{OUT} = V_{IN} / R1 \quad (2)$$

The OPA172 can also be used as the feedback amplifier because the low bias current minimizes error voltages produced across $R1$. However, for improved performance, select a FET-input device with extremely low offset, such as the OPA192, OPA140, or OPA188 as the feedback amplifier.

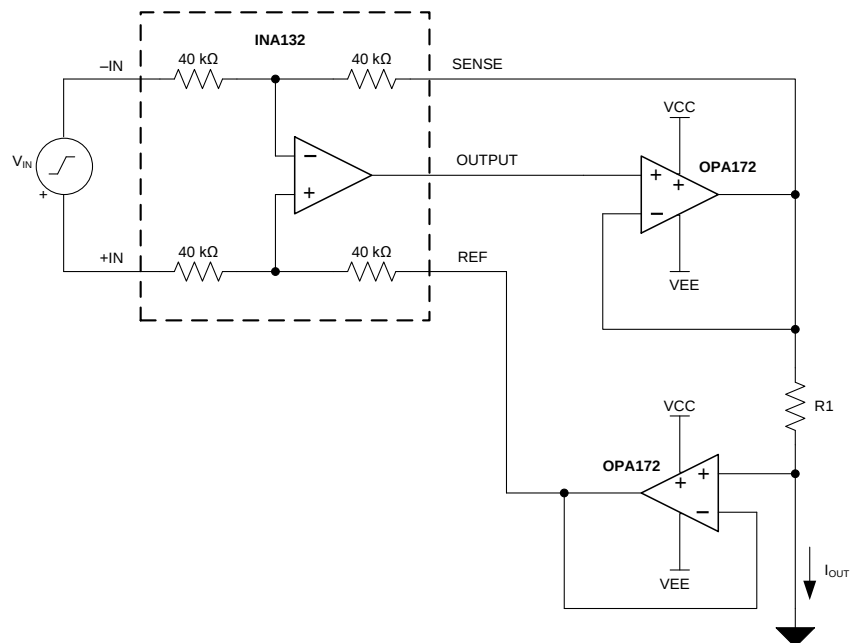


图 50. Bidirectional Current Source

10.2.3 JFET-Input Low-Noise Amplifier

Figure 51 shows a low-noise composite amplifier built by adding a low noise JFET pair (Q1 and Q2) as an input preamplifier for the OPA172. Transistors Q3 and Q4 form a 2-mA current sink that biases each JFET with 1 mA of drain current. Using 3.9-kΩ drain resistors produces a gain of approximately 10 in the input amplifier, making the extremely-low, broadband-noise spectral density of the JFET pair, Q1 and Q2, the dominant noise source of the amplifier. The output impedance of the input differential amplifier is large enough that a FET-input amplifier such as the OPA172 provides superior noise performance over bipolar-input amplifiers.

The gain of the composite amplifier is given by 式 3:

$$A_v = (1 + R_3 / R_4) \quad (3)$$

The resistances shown are standard 1% resistor values that produce a gain of approximately 100 (99.26) with 68° of phase margin. Gains less than 10 may require additional compensation methods to provide stability. Select low resistor values to minimize the resistor thermal noise contribution to the total output noise.

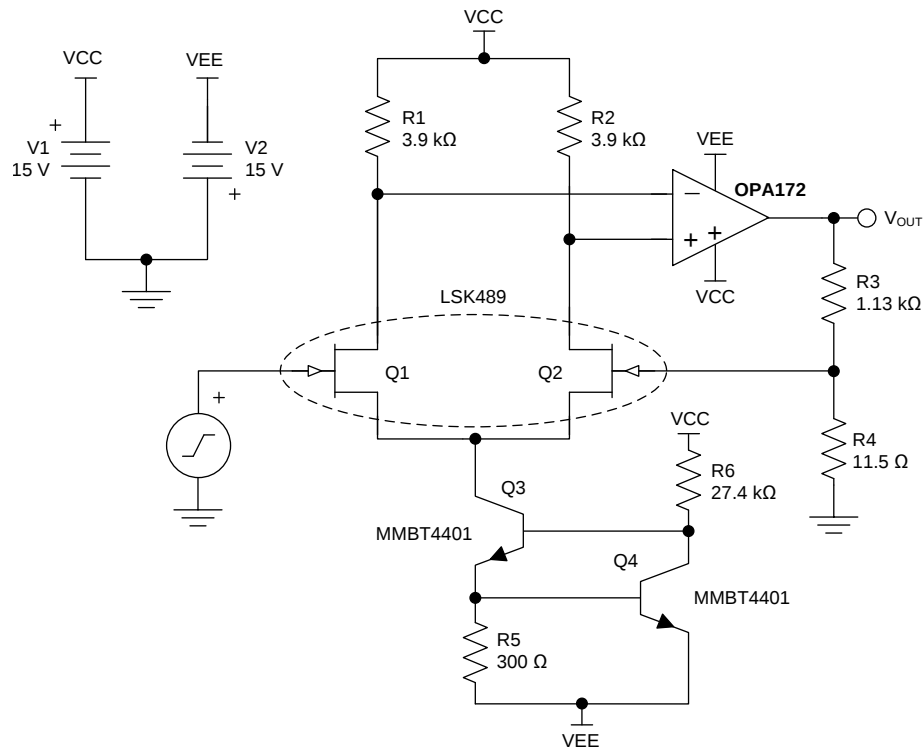


Figure 51. JFET-Input Low-Noise Amplifier

11 Power-Supply Recommendations

The OPA172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

注意

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1-μF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to [SLOA089](#), *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is preferable.
- Place the external components as close to the device as possible. As shown in [Figure 52](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Example

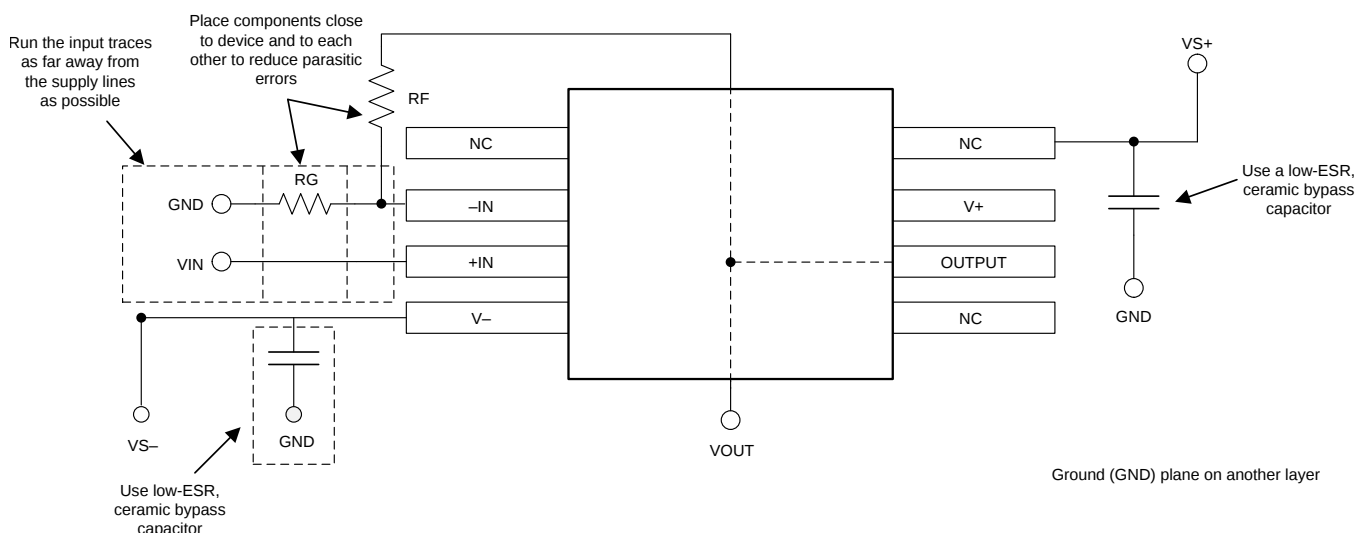


Figure 52. Operational Amplifier Board Layout for Noninverting Configuration

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 開発サポート

13.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから[無料でダウンロード](#)でき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。[TINA-TIフォルダ](#)から、無料のTINA-TIソフトウェアをダウンロードしてください。

13.2 ドキュメントのサポート

13.2.1 関連資料

[SBOA015 \(AB-028\)](#) - 『フィードバック・プロットによるオペアンプAC性能の定義』

[SLOA089](#) - 『基板のレイアウト技法』

[SLOD006](#) - 『誰でも使えるオペアンプ』

[SBOA128](#) - 『オペアンプのEMI除去率』

[TIPD128](#) - 『絶縁抵抗の使用による容量性負荷駆動のソリューション』

13.3 関連リンク

[表 5](#) に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.5 商標

E2E is a trademark of Texas Instruments.

TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA172ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172
OPA172ID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172
OPA172IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ
OPA172IDBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ
OPA172IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ
OPA172IDBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ
OPA172IDBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ
OPA172IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
OPA172IDCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
OPA172IDCKRG4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
OPA172IDCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
OPA172IDCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
OPA172IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172
OPA172IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172
OPA172IDRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172
OPA2172ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A
OPA2172ID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A
OPA2172IDGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVJQ
OPA2172IDGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVJQ
OPA2172IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	OVJQ
OPA2172IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OVJQ
OPA2172IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A
OPA2172IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A
OPA2172IDRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A
OPA2172IDRGR	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172
OPA2172IDRGR.B	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172
OPA2172IDRGT	Active	Production	SON (DRG) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172
OPA2172IDRGT.B	Active	Production	SON (DRG) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172
OPA4172ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4172ID.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172
OPA4172IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172
OPA4172IDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172
OPA4172IPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172
OPA4172IPW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172
OPA4172IPWG4.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172
OPA4172IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172
OPA4172IPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2172, OPA4172 :

- Automotive : [OPA2172-Q1](#), [OPA4172-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA172IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2172IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA4172IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4172IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

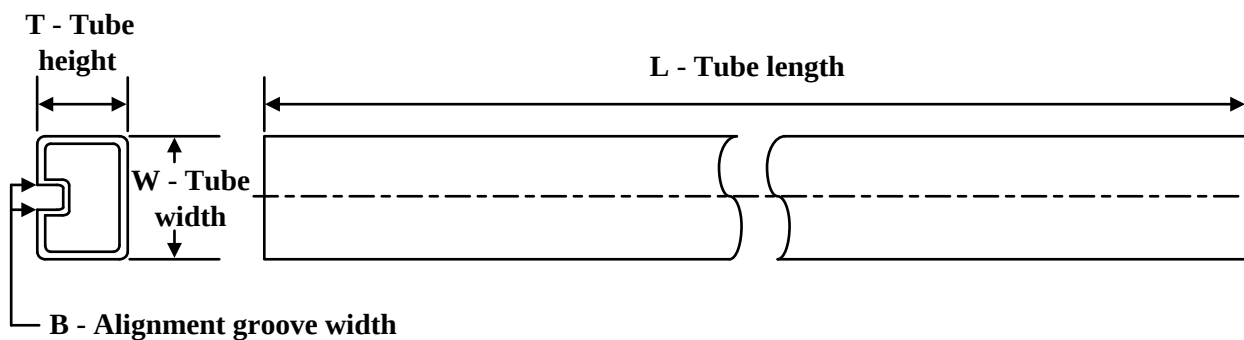
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA172IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA172IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA172IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA172IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA172IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2172IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2172IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2172IDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA2172IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA4172IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4172IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA172ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA172ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2172ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2172ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2172IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2172IDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4172ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4172ID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4172IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4172IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4172IPWG4.B	PW	TSSOP	14	90	530	10.2	3600	3.5



SOT-23 - 1.45 mm max height

Technical drawing of a connector housing showing three views: front, side, and end view.

Front View Dimensions:

- Overall width: 3.0
- Overall height: 2.6
- Pin 1 Index Area (shaded)
- Pin locations: 1, 2, 3, 4, 5
- Dimensions: 1.75, 1.45, 1.9, 3.05, 2.75, 0.1, 0.15
- Table:

0.2	C	A	B
-----	---	---	---

Side View Dimensions:

- Height: 3.05
- Width: 1.45
- Table:

0.1	C
-----	---

End View Dimensions:

- Width: 1.1
- Height: 0.15
- Table:

0.1	C
-----	---

Other Dimensions:

- 4X 0° -15°
- 4X 4° -15°
- 0.25
- 0.22 TYP
- 0.08
- 0.6 TYP
- 0.3
- SEATING PLANE
- E PLANE
- TYP

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

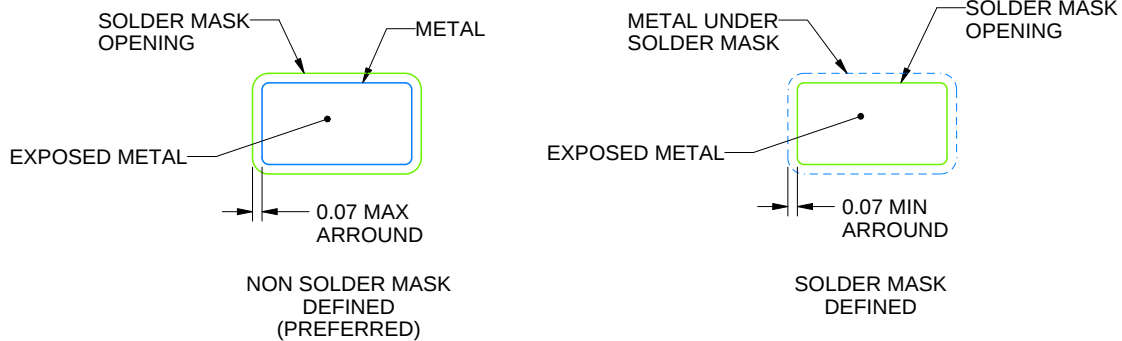
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



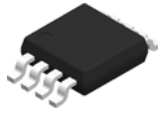
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

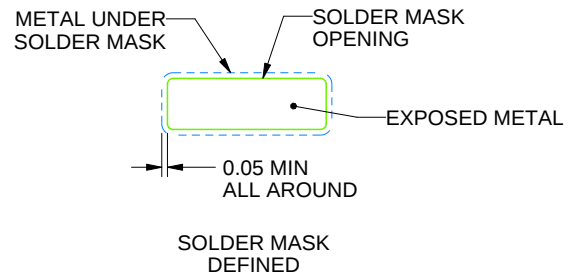
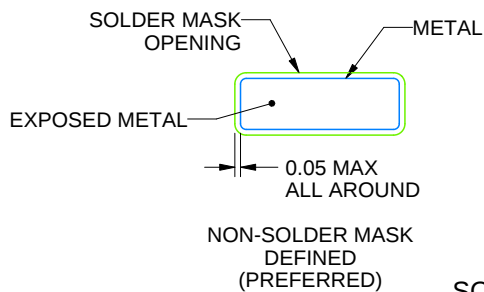
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

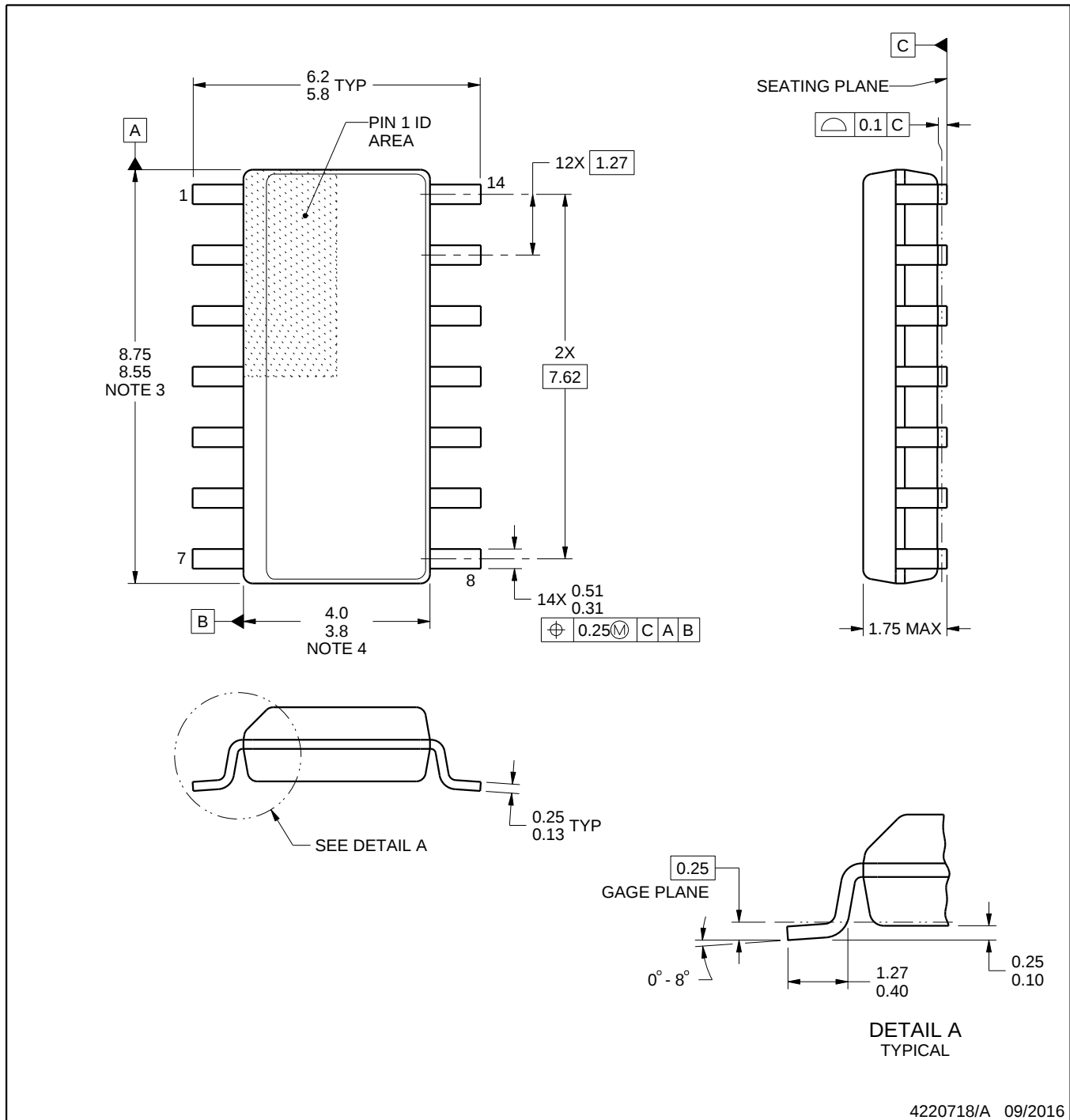
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

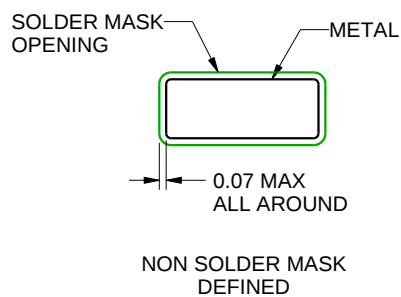
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

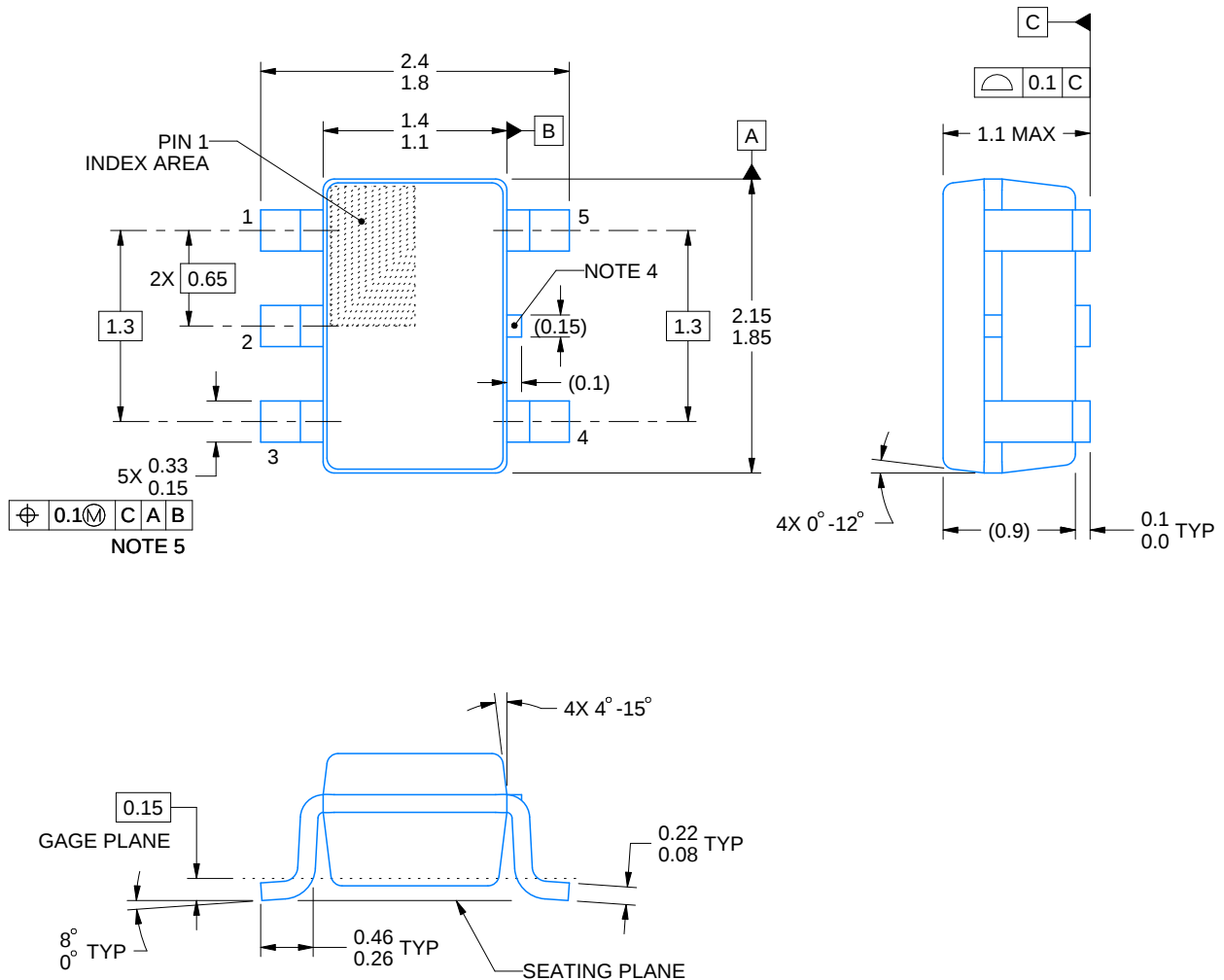


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

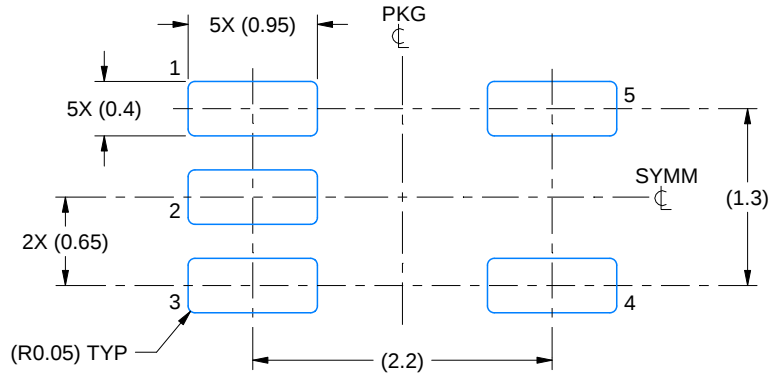
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



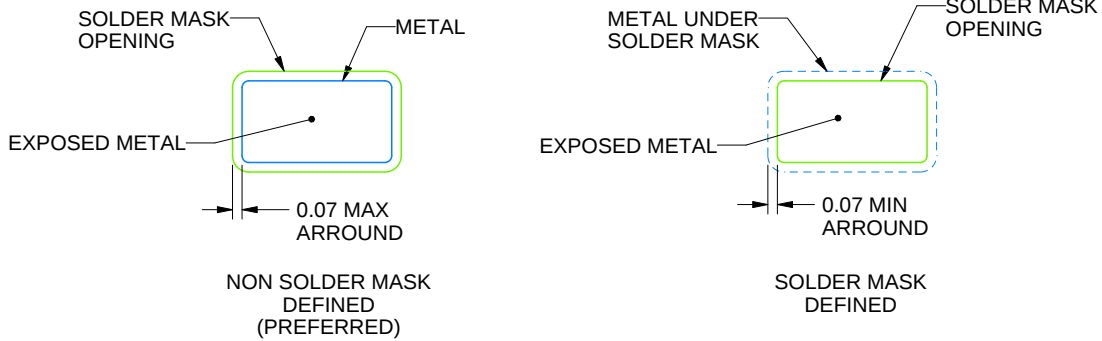
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

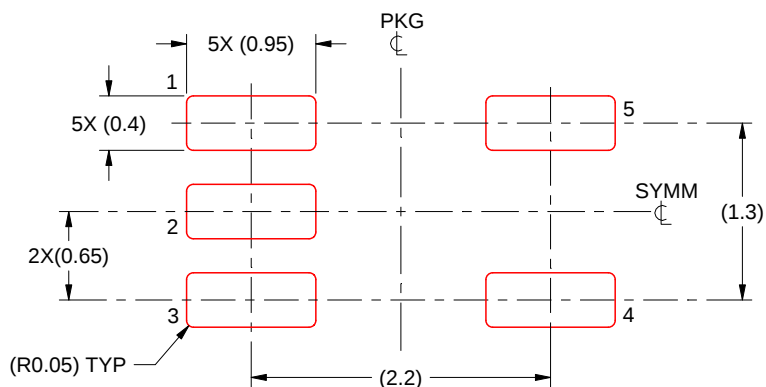


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

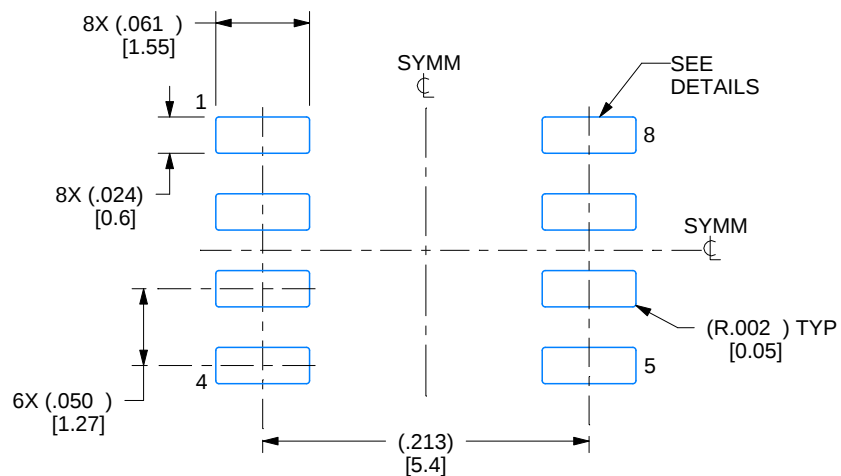


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

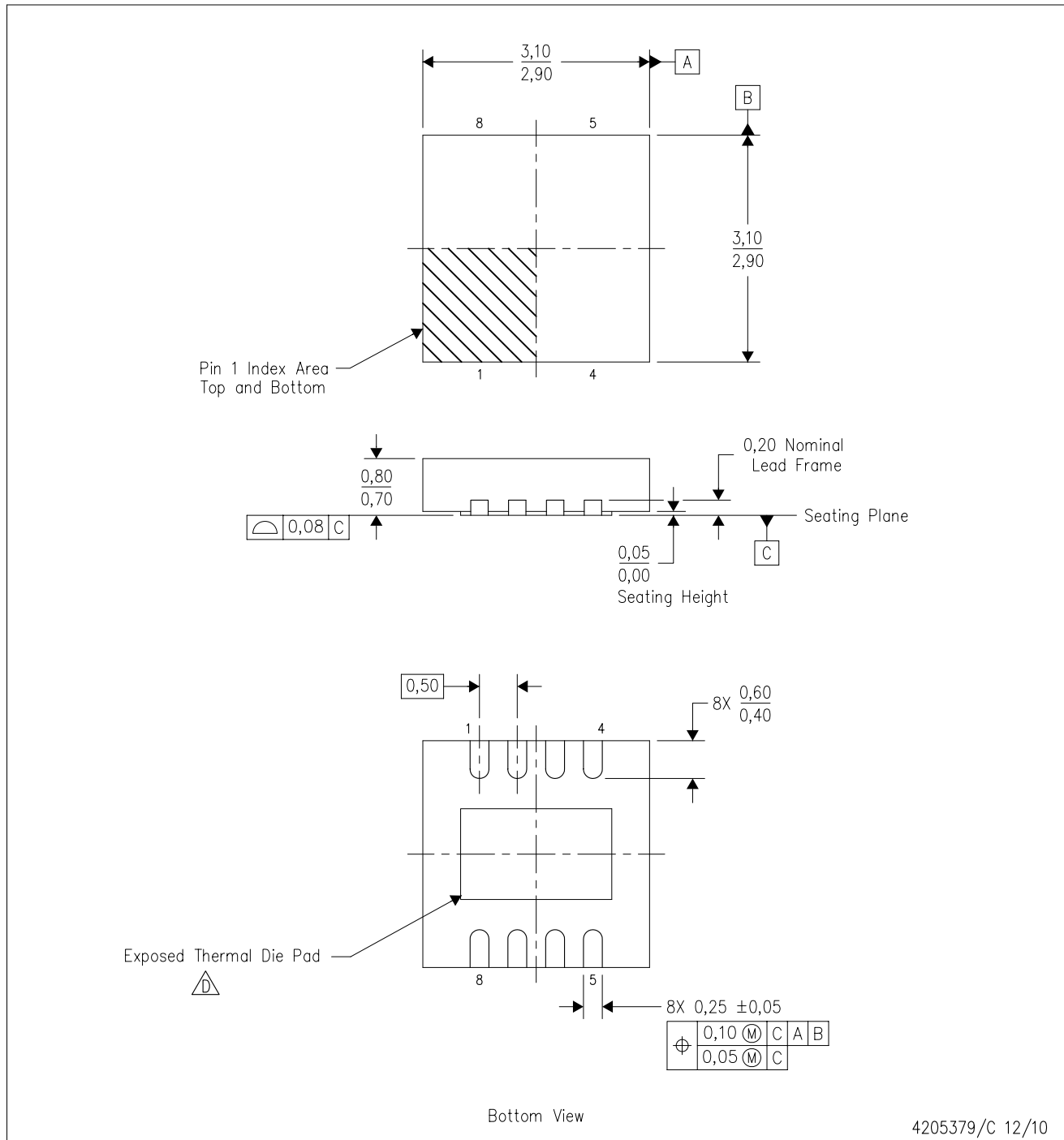
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



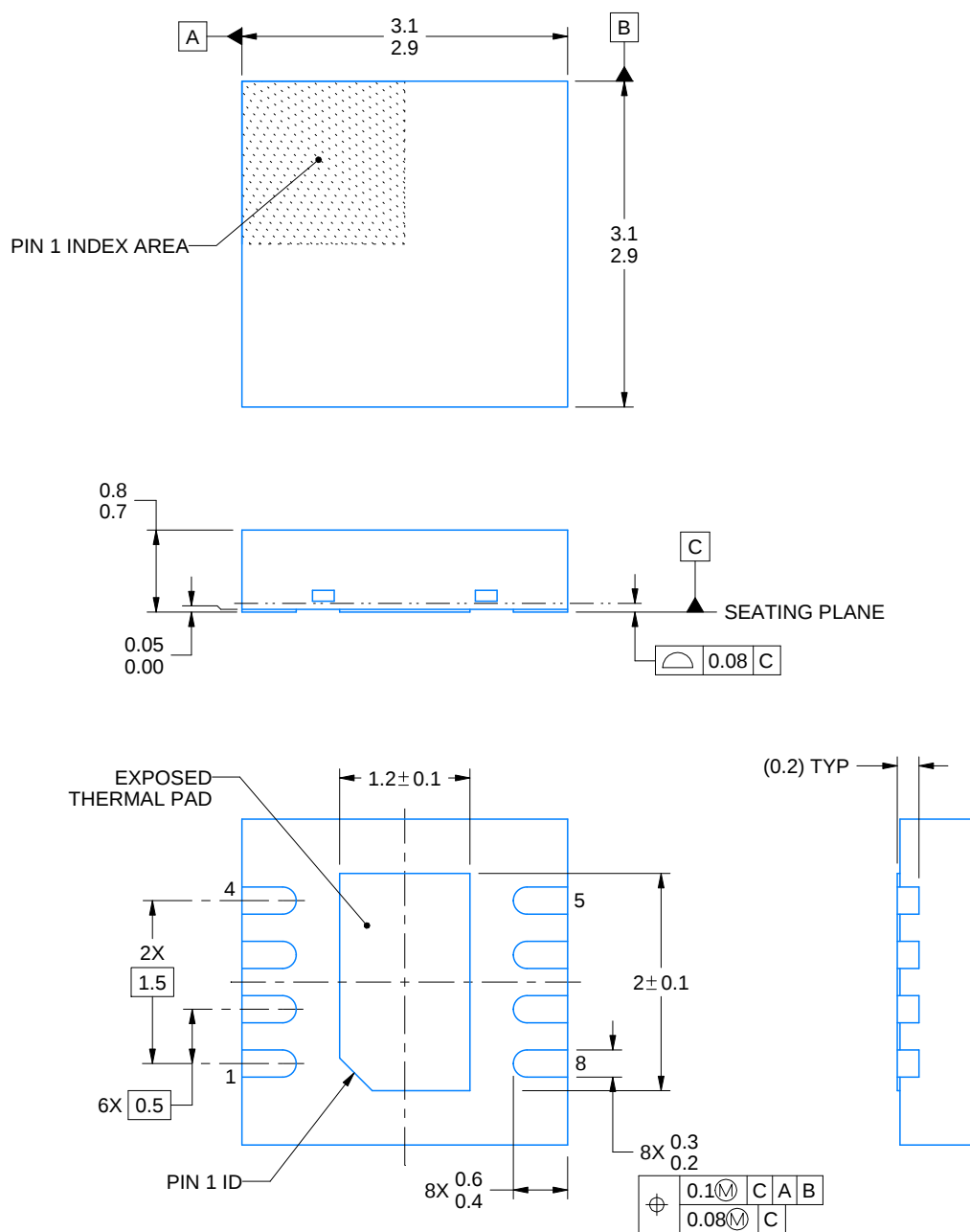
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. JEDEC MO-229 package registration pending.



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218885/A 03/2020

NOTES:

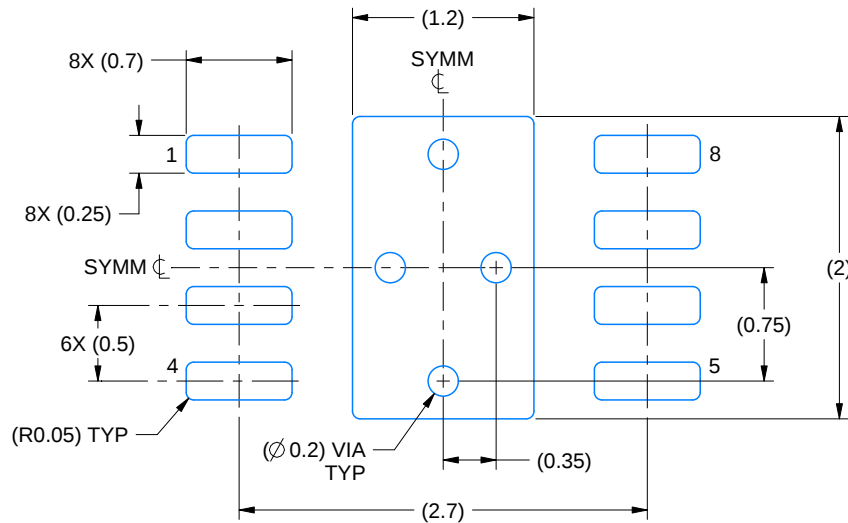
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

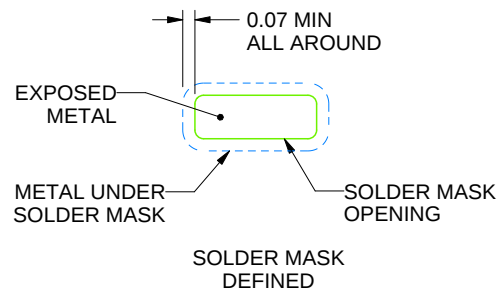
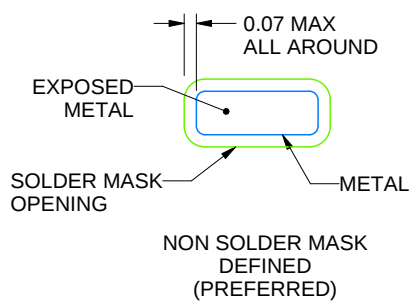
DRG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

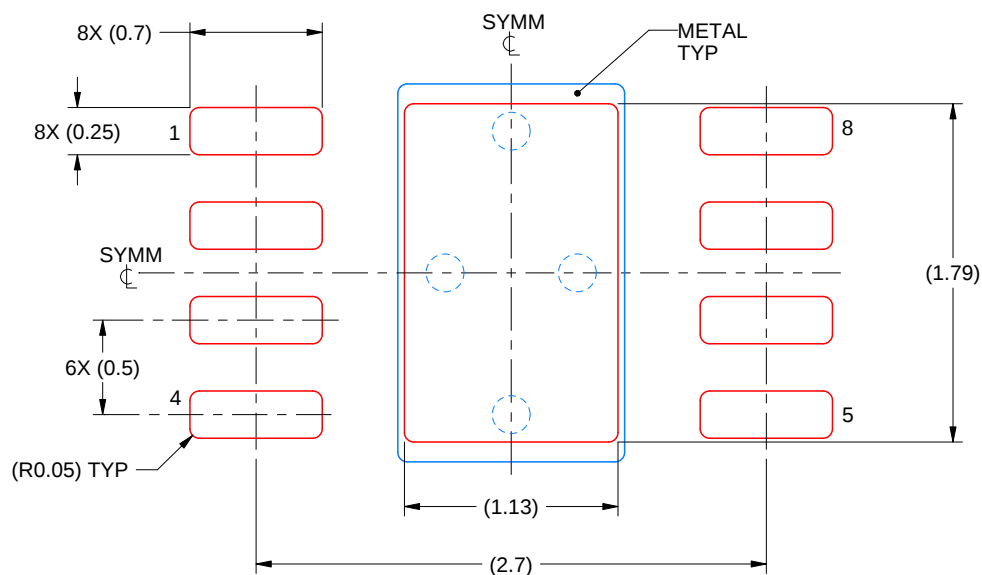
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRG0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

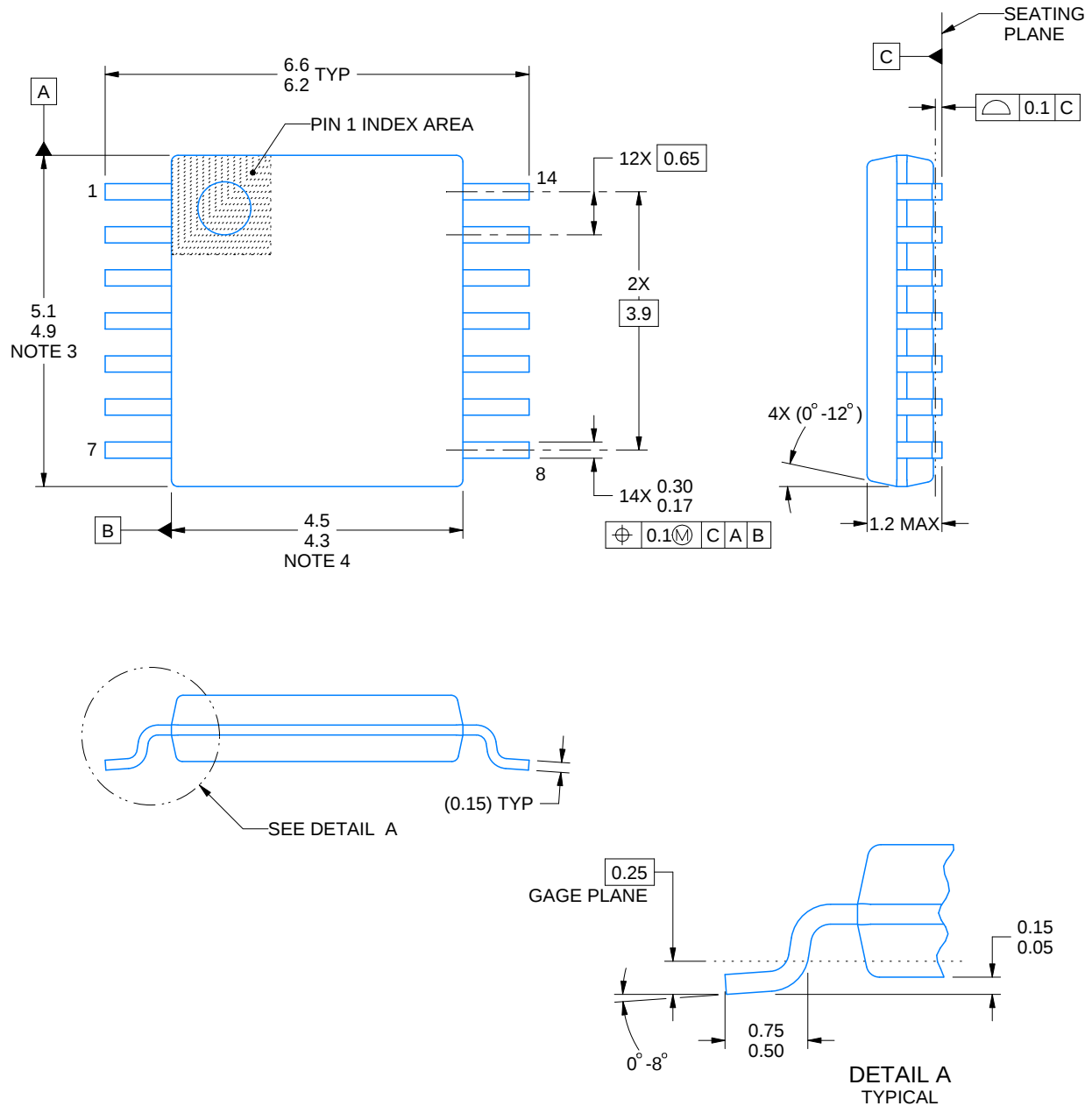
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

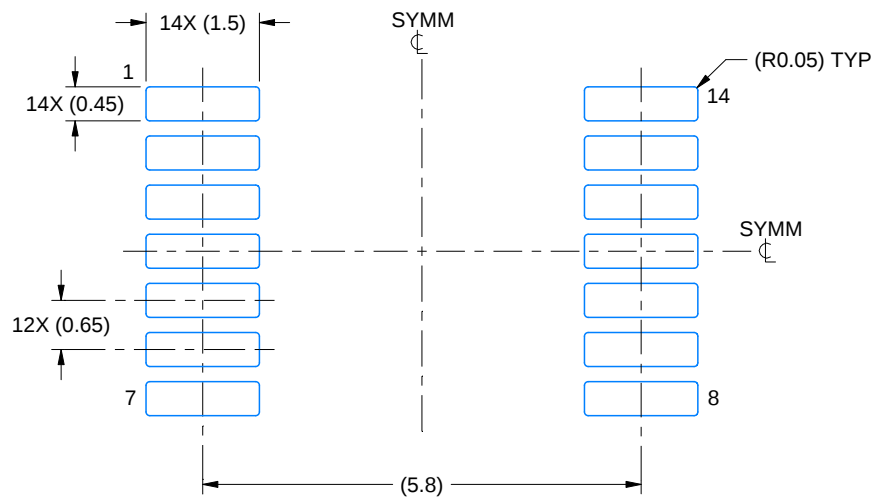
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

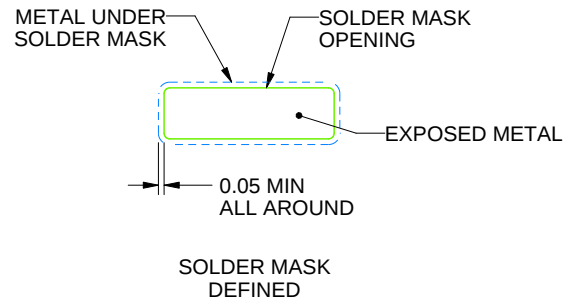
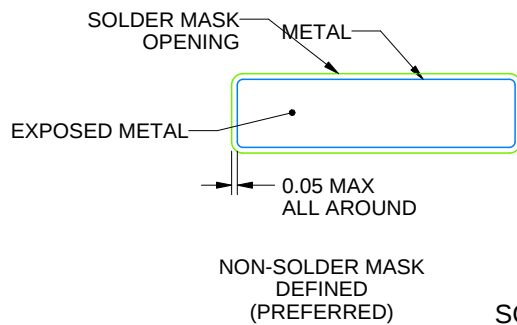
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

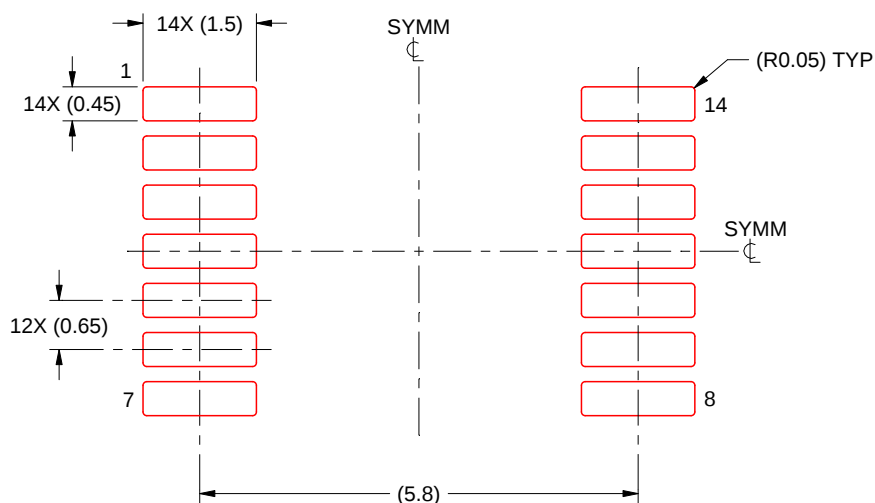
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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