OPA167x 低歪オーディオ・オペアンプ

1 特長

- 低いノイズ:1 kHz 時に 4.5nV/√Hz
- 低歪:1kHz 時に 0.0001%
- 高いオープン・ループ・ゲイン:114dB
- 大きい同相除去比:110dB
- 低い静止電流:
  - チャネルごとに 2mA
- 低い入力バイアス電流:10pA (標準値)
- スルーレート:9V/µs
- 広いゲイン帯域幅:16 MHz (G = 1)
- ユニティ・ゲイン安定
- レール・ツー・レール出力
- 広い電源電圧範囲:
  - ±2.25V～±18V、または 4.5V～36V
- シングル、デュアル、およびクワッド・チャネル・バージョン
- 利用可能なパッケージ:
  - シングル:SOIC-8、SOT-23
  - デュアル:SOIC-8、小型 SON-8、VSSOP-8
  - クワッド:小型 QFN-16、SO-14、TSSOP-14
- 温度範囲:-40℃～+85℃

2 アプリケーション

- 業務用マイクとワイヤレス・システム
- 業務用オーディオ・ミキサ / 制御卓
- ギターアンプ / その他楽器用アンプ
- AV レシーバ
- 車載用外部アンプ

3 概要

シングル・チャネル OPA1677、デュアル・チャネル OPA1678 およびクワッド・チャネル OPA1679 (OPA167x) オペアンプは、オーディオ回路での一般的な使用において、従来型のオペアンプよりも高いシステム・レベルの性能を実現します。

OPA167x アンプは、ノイズ密度が 4.5nV/√Hz と低く、歪みも 1kHz で 0.0001% と低いため、オーディオ信号の忠実度が向上します。また、2kΩ 負荷で電源の 800mV 内側までのレール・ツー・レール出力が可能なため、ヘッドルームが増大し、ダイナミック・レンジが最大化されます。

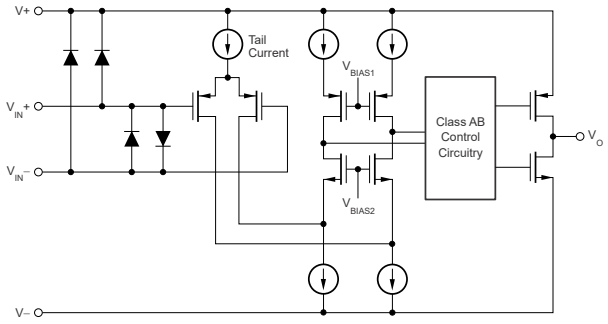
OPA167x は、多くの種類のオーディオ製品の電源に対応するために、わずか 2mA の電源電流で、±2.25V～±18V (または 4.5V～36V) の非常に広い電源電圧範囲で動作します。これらのオペアンプは安定したユニティ・ゲインを持ち、広い範囲の負荷条件についてダイナミック特性が非常に優れているため、多くのオーディオ回路で使用できます。

OPA167x アンプは、オーバードライブまたは過負荷時でも、チャネル間のクロストークが最小限になるように、完全に独立した内部回路を使用しています。

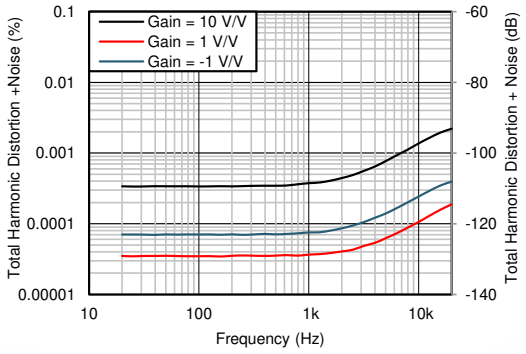
デバイス情報

部品番号	チャネル	パッケージ (1)
OPA1677	シングル	SOIC (8)
		SOT-23 (5)
OPA1678	デュアル	SOIC (8)
		VSSOP (8)
		SON (8)
OPA1679	クワッド	SOIC (14)
		TSSOP (14)
		QFN (16)

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



概略内部回路図



THD+N と周波数との関係 (2kΩ 負荷)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (December 2021) to Revision E (December 2022) — **Page**

- OPA1677 D (SOIC、8) パッケージをプレビューから量産データ (アクティブ) に変更 ... 1

Changes from Revision C (April 2019) to Revision D (December 2021) — **Page**

- 文書全体の表、図、相互参照の採番方法を更新 ... 1
- OPA1677 の量産データ (アクティブ) デバイスと関連する内容を追加 ... 1

Changes from Revision B (June 2018) to Revision C (April 2019) — **Page**

- OPA1679 QFN パッケージのステータスを「量産データ」に変更 ... 1
- Changed GPN BUF634A in Figure 8-6, *Composite Headphone Amplifier (Single-Channel Shown)* ... 25

Changes from Revision A (May 2018) to Revision B (June 2018) — **Page**

- プレビュー版 QFN (RUM) パッケージについての内容を追加 ... 1

Changes from Revision * (February 2017) to Revision A (May 2018) — **Page**

- DRG (SON) 8 ピン・パッケージを「製品情報」の表に追加 ... 1
- 「特長」の表に SON-8 パッケージを追加。 ... 1
- Added DRG (SON) 8-pin pinout drawing to *Pin Configuration and Functions* section ... 3
- Added thermal pad information to *Pin Functions: OPA1678* table ... 3

5 Pin Configuration and Functions

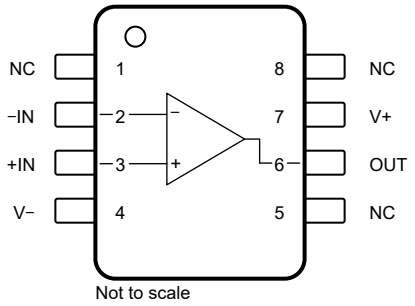


図 5-1. OPA1677: D Package, 8-Pin SOIC (Top View)

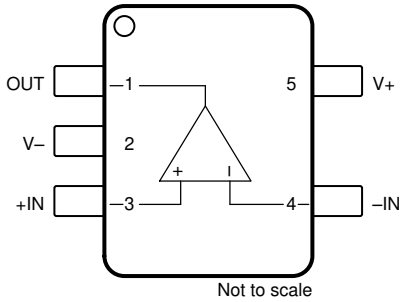


図 5-2. OPA1677: DBV Package, 5-Pin SOT-23 (Top View)

Pin Functions: OPA1677

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
OUT	6	1	Output	Output
V–	4	2	Power	Negative (lowest) power supply
V+	7	5	Power	Positive (highest) power supply

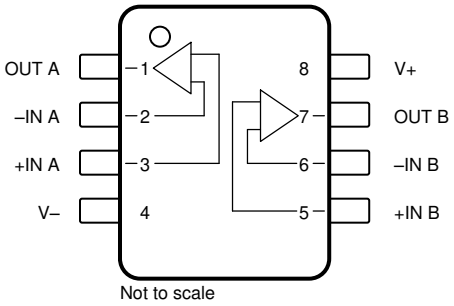


図 5-3. OPA1678: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

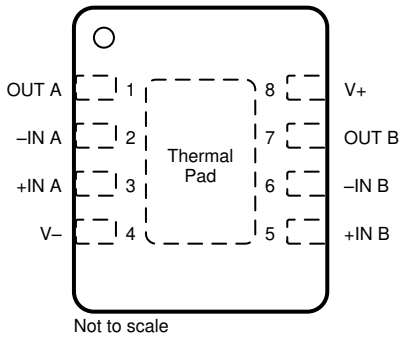


図 5-4. OPA1678: DRG Package, 8-Pin SON With Exposed Thermal Pad (Top View)

Pin Functions: OPA1678

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
+IN A	3	Input	Noninverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply
Thermal Pad	Thermal pad	—	For DRG (SON-8) package. Exposed thermal die pad on underside. Connect thermal die pad to V–. Solder the thermal pad to improve heat dissipation and provide specified performance.

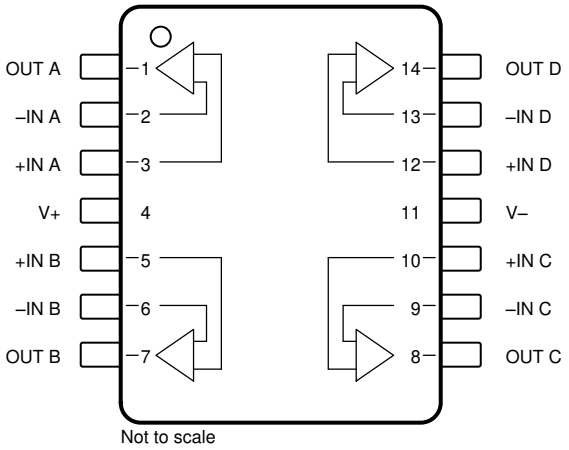


図 5-5. OPA1679: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

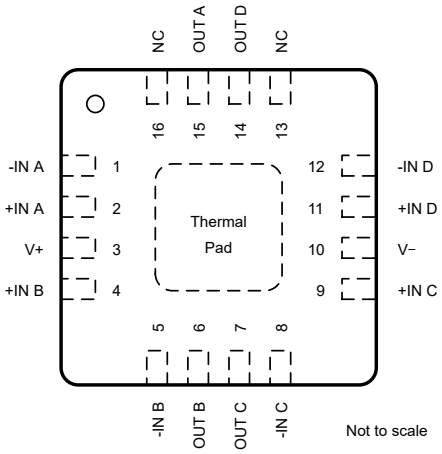


図 5-6. OPA1679: RUM Package, 16-Pin QFN With Exposed Thermal Pad (Top View)

Pin Functions: OPA1679

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC) PW (TSSOP)	RUM (QFN)		
–IN A	2	1	Input	Inverting input, channel A
+IN A	3	2	Input	Noninverting input, channel A
–IN B	6	5	Input	Inverting input, channel B
+IN B	5	4	Input	Noninverting input, channel B
–IN C	9	8	Input	Inverting input, channel C
+IN C	10	9	Input	Noninverting input, channel C
–IN D	13	12	Input	Inverting input, channel D
+IN D	12	11	Input	Noninverting input, channel D
NC	—	13	—	No connect
NC	—	16	—	No connect
OUT A	1	15	Output	Output, channel A
OUT B	7	6	Output	Output, channel B
OUT C	8	7	Output	Output, channel C
OUT D	14	14	Output	Output, channel D
V+	4	3	Power	Positive (highest) power supply
V–	11	10	Power	Negative (lowest) power supply
Thermal Pad	—	Thermal pad	—	Exposed thermal die pad on underside. Connect thermal die pad to V–. Solder the thermal pad to improve heat dissipation and provide specified performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
		Input voltage	(V–) – 0.5	(V+) + 0.5	V
	Current	Input current (all pins except power-supply pins)	–10	10	mA
		Output short-circuit current(2)	Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Machine Model was not tested on OPA1679IRUM.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T_A	Operating temperature		–40		125	°C

6.4 Thermal Information: OPA1677

THERMAL METRIC[1]		OPA1677		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.9	180.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.0	78.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.3	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.9	20.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.6	47.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA1678

THERMAL METRIC[1]		OPA1678			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	144	219	66.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77	79	54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	104	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28	15	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61	102	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA1679

THERMAL METRIC[1]		OPA1679			UNIT
		D (SOIC)	PW (TSSOP)	RUM (QFN)	
		14 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90	127	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	47	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	59	17.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20	55	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44	58	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at V_S = ±15 V, T_A = 25°C, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, R_L = 600 Ω, f = 1 kHz, V_O = 3 V_{RMS}			0.0001%		
					–120		dB
IMD	Intermodulation distortion	G = 1 V_O = 3 V_{RMS}	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)		0.0001%		
					–120		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.0001%		
					–120		dB
			CCIF twin-tone (19 kHz and 20 kHz)		0.0001%		
					–120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			16		MHz
SR	Slew rate	G = –1			9		V/µs
	Full power bandwidth(1)	V_O = 1 V_P			1.4		MHz
	Overload recovery time	G = –10			1		µs
	Channel separation (dual and quad)	f = 1 kHz			–130		dB
NOISE							
en	Input voltage noise	f = 20 Hz to 20 kHz			5.4		μV_{PP}
		f = 0.1 Hz to 10 Hz			1.74		
	Input voltage noise density	f = 1 kHz			4.5		nV/√Hz
i_n	Input current noise density	f = 1 kHz			3		fA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V to ±18 V			±0.5	±2	mV
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C(2)			2		µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V			3	8	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			±10		pA
I_{OS}	Input offset current	V_{CM} = 0 V			±10		pA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)+0.5		(V+) – 2	V
CMRR	Common-mode rejection ratio			100	110		dB
INPUT IMPEDANCE							
	Differential				100 || 6		MΩ || pF
	Common-mode				6000 || 2		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.8 V ≤ V_O ≤ (V+) – 0.8 V		106	114		dB
OUTPUT							
V_O	Output voltage			(V–) + 0.8		(V+) – 0.8	V
I_{OUT}	Output Current			See セクション 6.8			mA
Z_O	Open-loop output impedance	f = 1 MHz		See セクション 6.8			Ω
I_{SC}	Short-circuit current(3)				±50		mA
C_L	Capacitive load drive				100		pF
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_O = 0 A			2	2.5	mA
		I_O = 0 A, T_A = –40°C to 125°C(2)				2.8	

(1) Full-power bandwidth = SR / (2π ×V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

6.8 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, (unless otherwise noted)

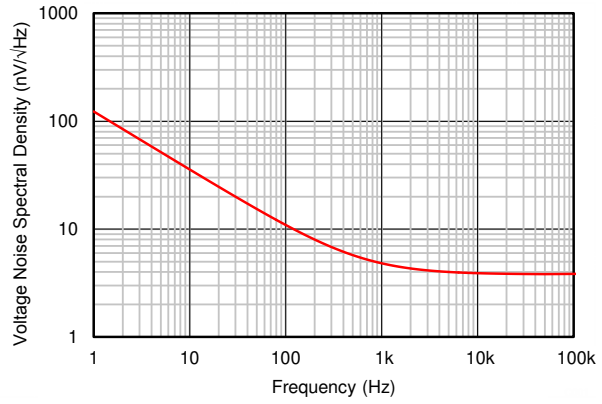


図 6-1. Input Voltage Noise Density vs Frequency

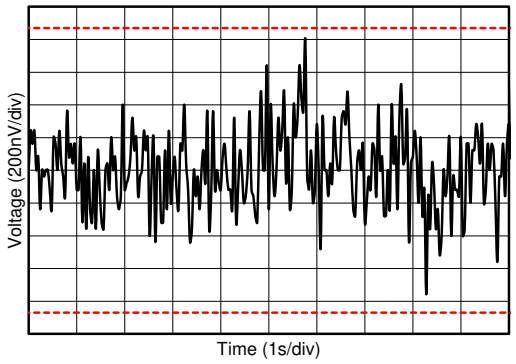


図 6-2. 0.1-Hz to 10-Hz Noise

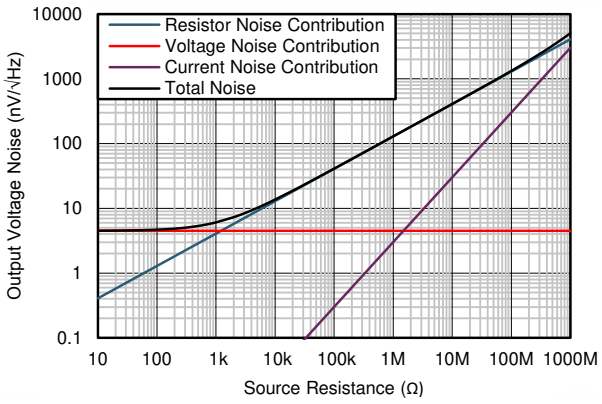


図 6-3. Voltage Noise vs Source Resistance

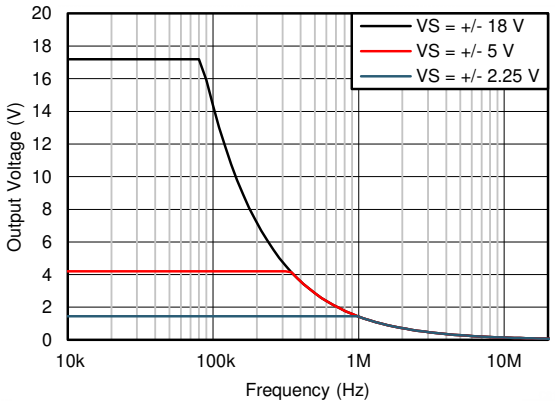
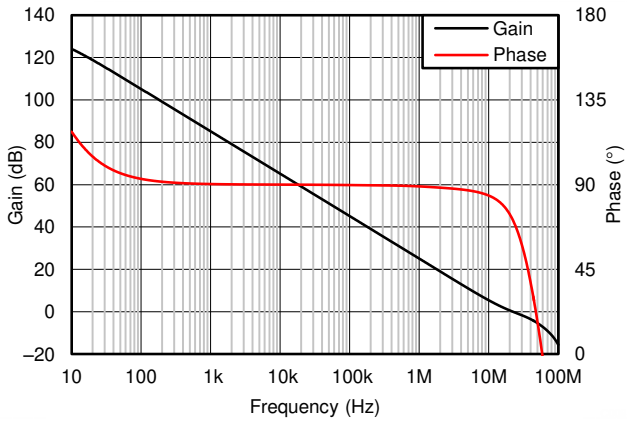
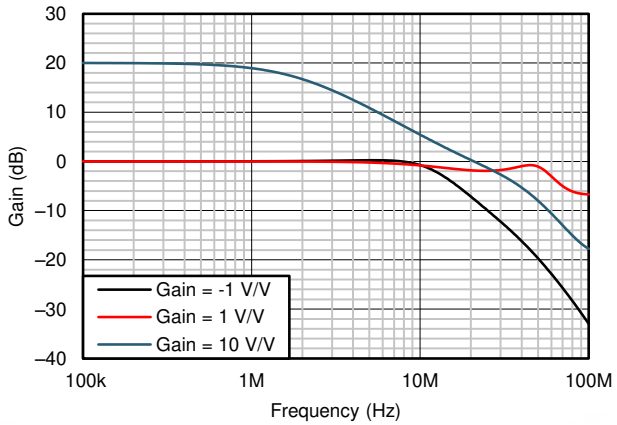


図 6-4. Maximum Output Voltage vs Frequency



C_L = 10 pF

図 6-5. Open-Loop Gain and Phase vs Frequency

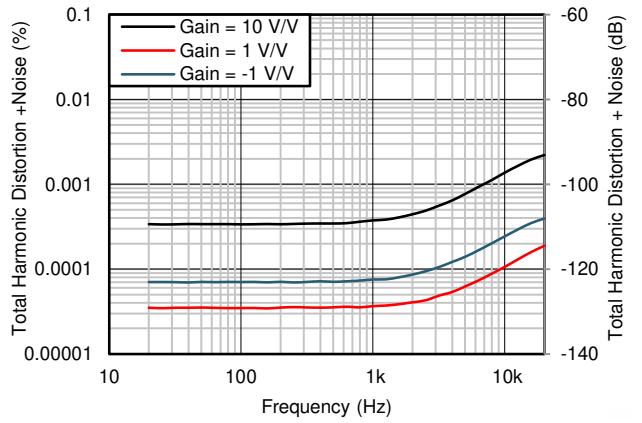


C_L = 10 pF

図 6-6. Closed-Loop Gain vs Frequency

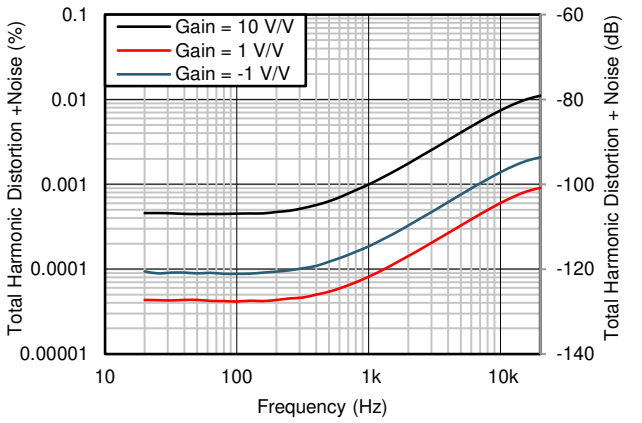
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, (unless otherwise noted)



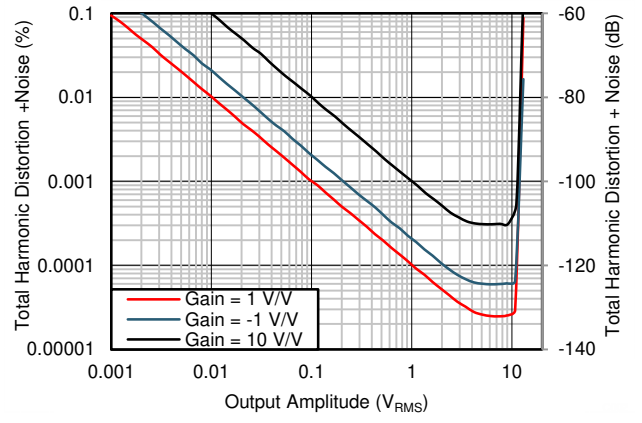
V_{OUT} = 3 V_{RMS} R_L = 2 kΩ Bandwidth = 80 kHz

図 6-7. THD+N Ratio vs Frequency



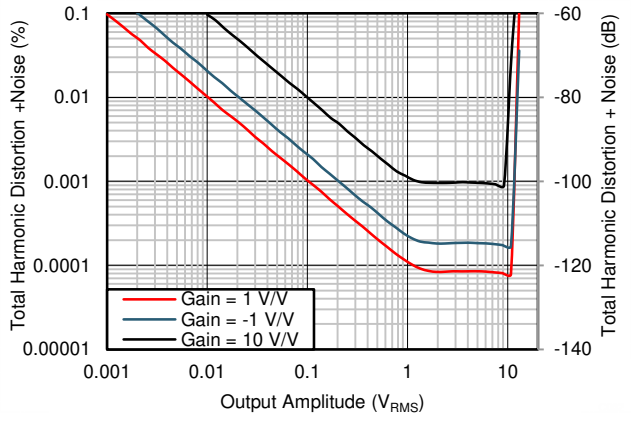
V_{OUT} = 3 V_{RMS} R_L = 600 Ω Bandwidth = 80 kHz

図 6-8. THD+N Ratio vs Frequency



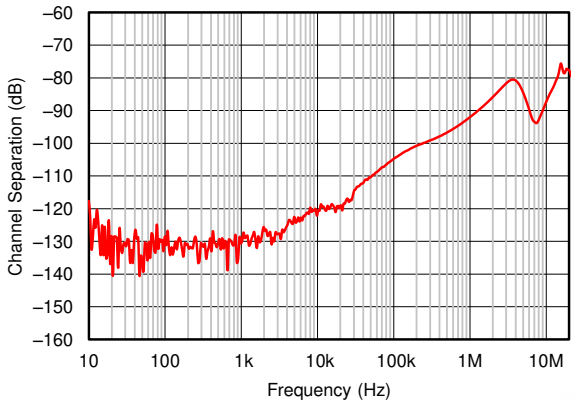
f = 1 kHz R_L = 2 kΩ Bandwidth = 80 kHz

図 6-9. THD+N Ratio vs Output Amplitude



f = 1 kHz R_L = 600 Ω Bandwidth = 80 kHz

図 6-10. THD+N Ratio vs Output Amplitude



V_{OUT} = 3 V_{RMS} Gain = 1 V/V

図 6-11. Channel Separation vs Frequency

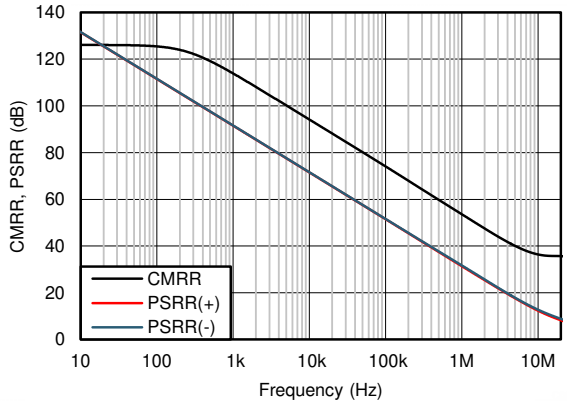
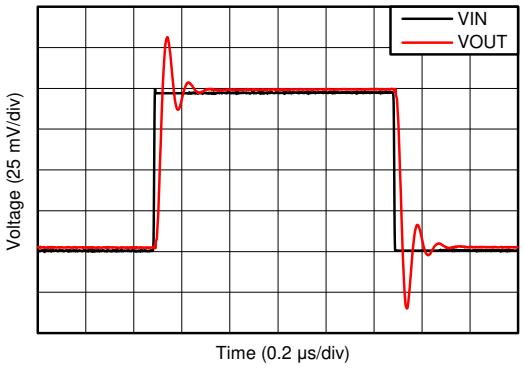


図 6-12. CMRR and PSRR vs Frequency (Referred to Input)

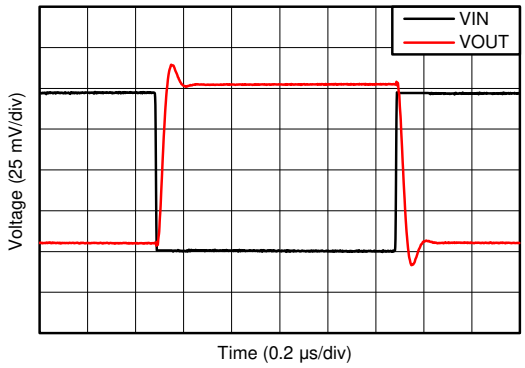
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, (unless otherwise noted)



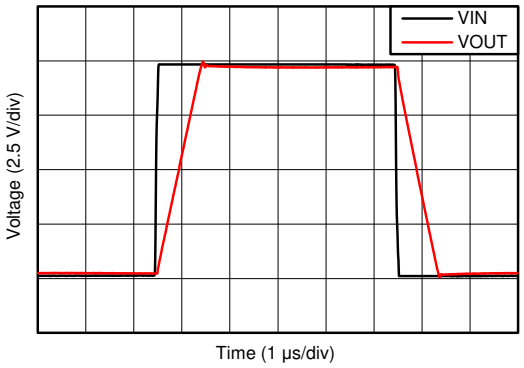
Gain = 1 V/V C_L = 100 pF

図 6-13. Small-Signal Step Response (100 mV)



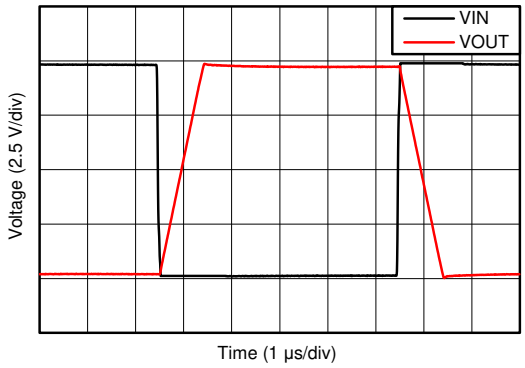
Gain = –1 V/V C_L = 100 pF

図 6-14. Small-Signal Step Response (100 mV)



Gain = +1 V/V R_F = 2 kΩ C_L = 100 pF

図 6-15. Large-Signal Step Response



Gain = –1 V/V C_L = 100 pF

図 6-16. Large-Signal Step Response

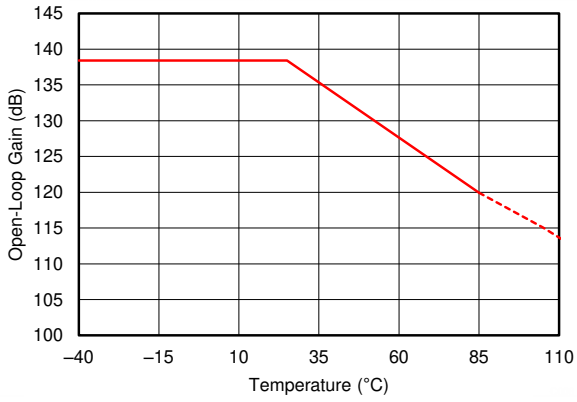


図 6-17. Open-Loop Gain vs Temperature

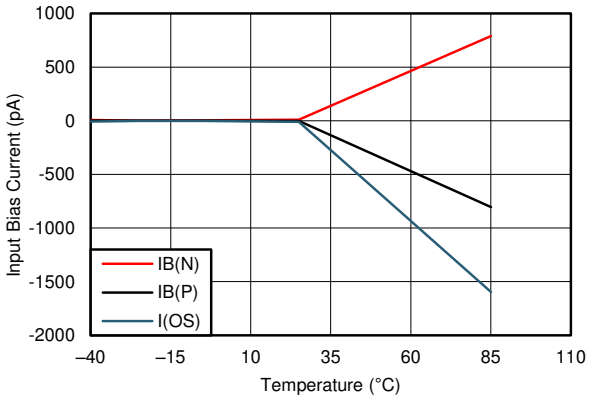


図 6-18. I_B and I_{OS} vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, (unless otherwise noted)

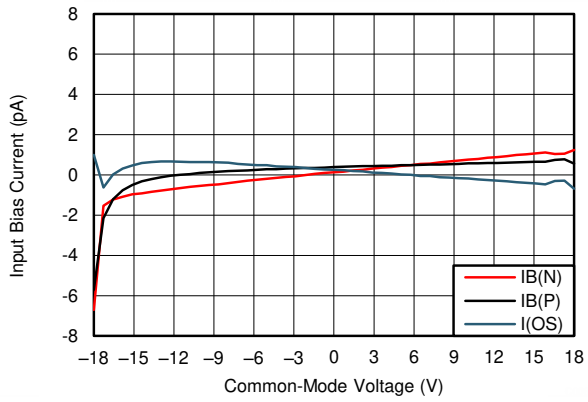


図 6-19. I_B and I_{OS} vs Common-Mode Voltage

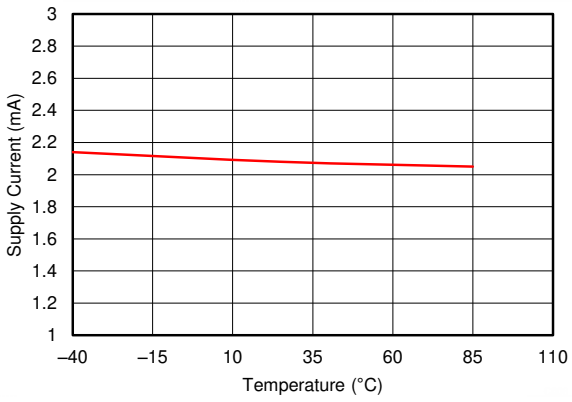


図 6-20. Supply Current vs Temperature

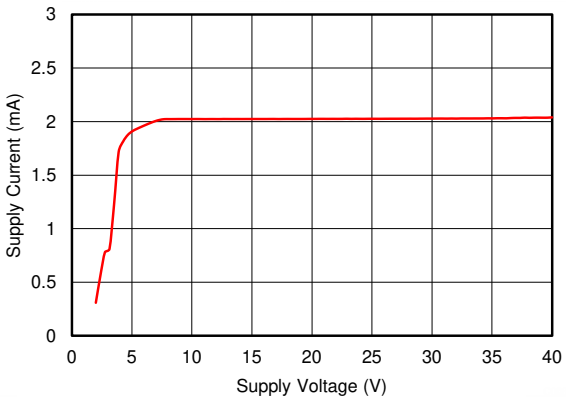


図 6-21. Supply Current vs Supply Voltage

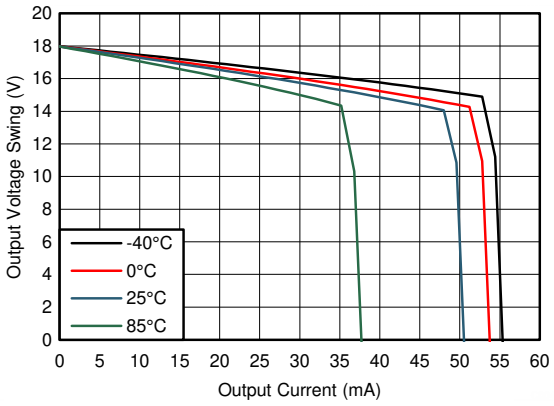


図 6-22. Output Voltage vs Output Current (Sourcing)

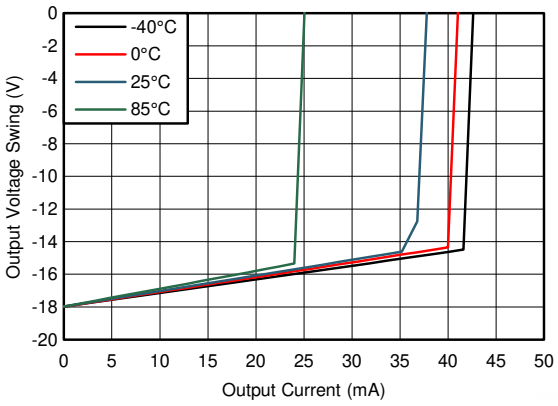


図 6-23. Output Voltage vs Output Current (Sinking)

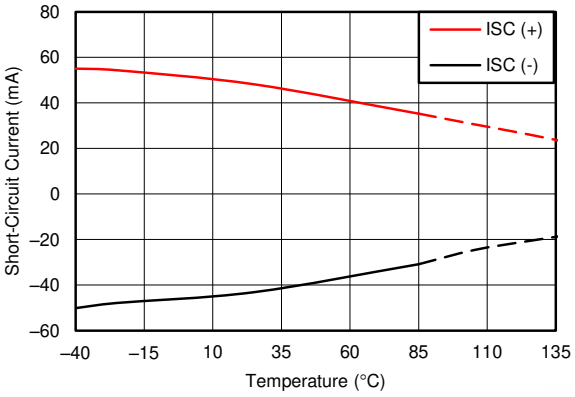
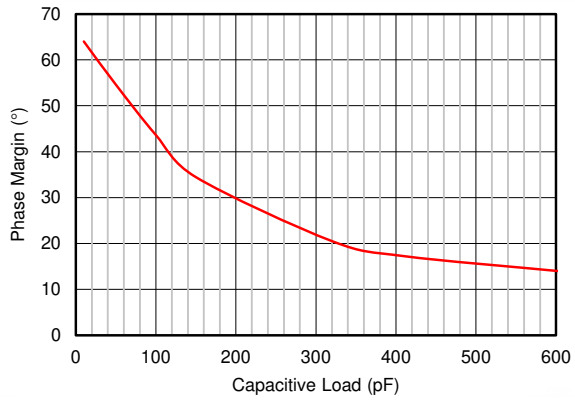


図 6-24. Short-Circuit Current vs Temperature

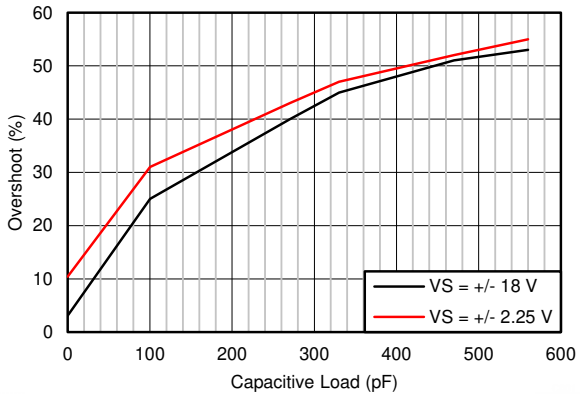
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, (unless otherwise noted)



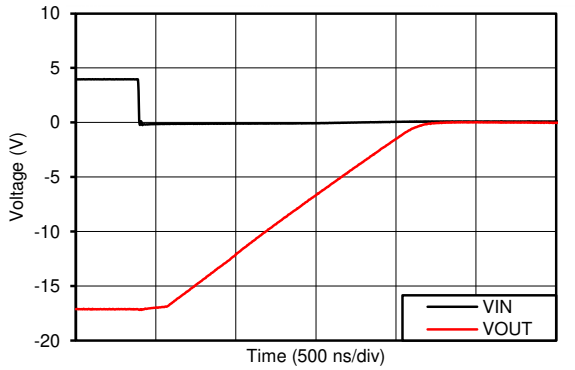
G = 1

図 6-25. Phase Margin vs Capacitive Load



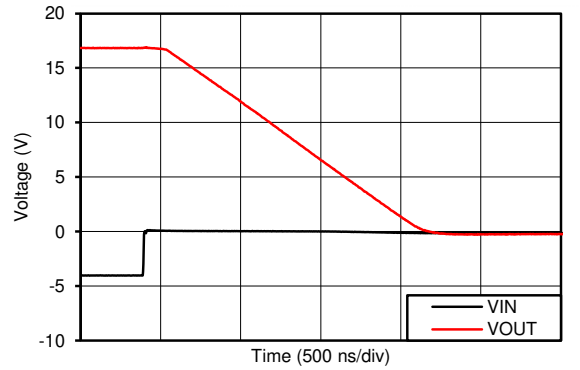
G = 1

図 6-26. Percent Overshoot vs Capacitive Load



Gain = –10 V/V

図 6-27. Negative Overload Recovery



Gain = –10 V/V

図 6-28. Positive Overload Recovery

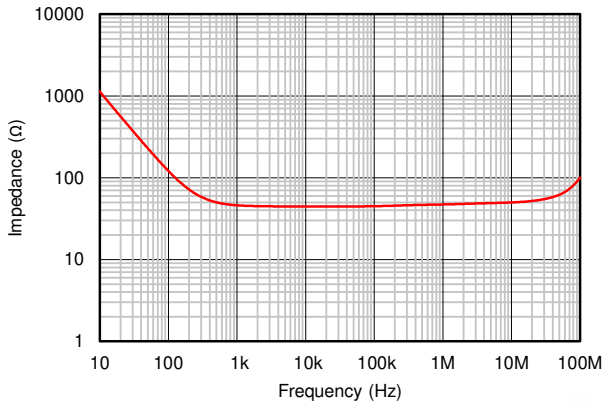
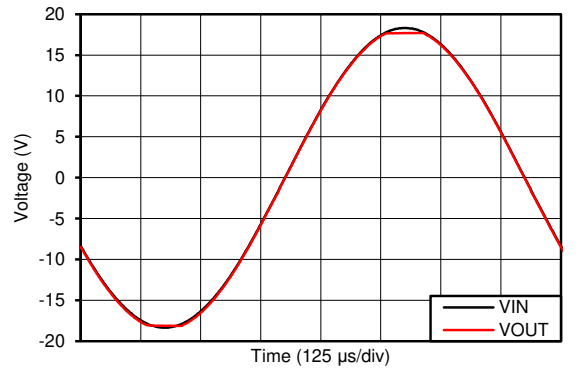


図 6-29. Open-Loop Output Impedance vs Frequency



Gain = 1 V/V

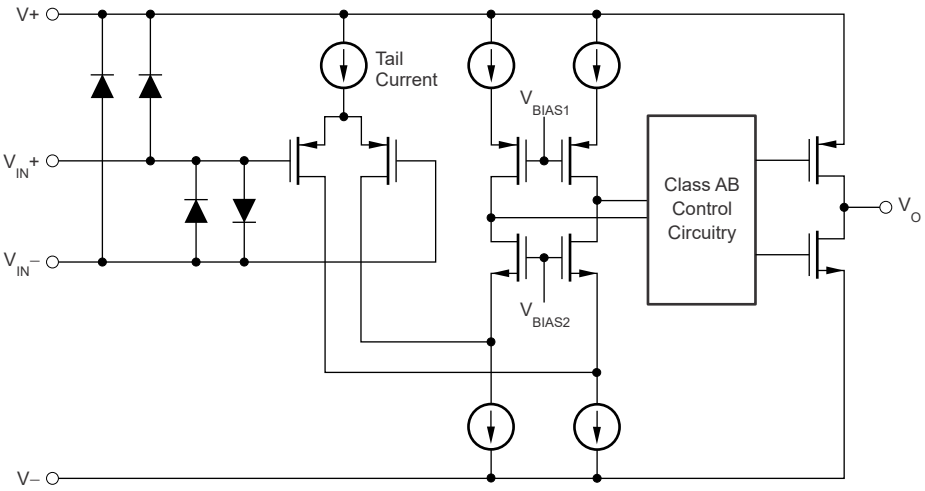
図 6-30. No Phase Reversal

7 Detailed Description

7.1 Overview

The OPA167x devices are unity-gain stable, dual-channel and quad-channel op amps with low noise and distortion. セクション 7.2 shows a simplified schematic of the OPA167x (one channel shown). These devices consist of a low-noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits excellent noise and distortion performance across a wide range of supply voltages that are not delivered by legacy, commodity, audio operational amplifiers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA167x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA167x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 図 7-1.

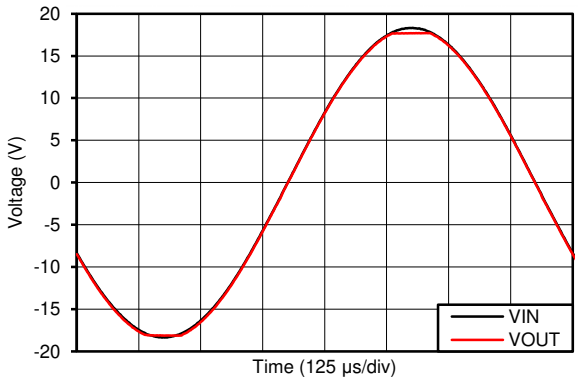


図 7-1. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown

characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 7-2 illustrates the ESD circuits contained in the OPA167x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

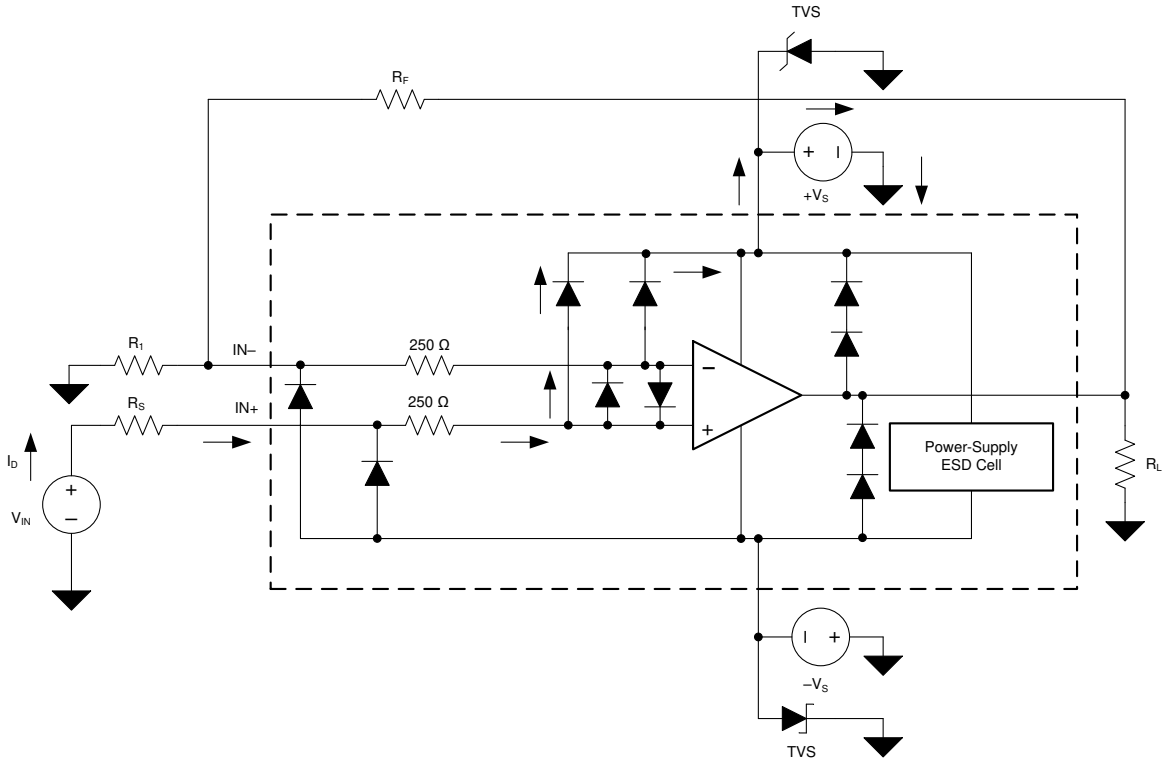


図 7-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPA167x but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see 図 7-2), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 7-2 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current

levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 7-2. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is shown in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download at www.ti.com.

The EMIRR IN+ of the OPA167x is plotted versus frequency in 図 7-3. The dual and quad operational amplifier device versions have approximately identical EMIRR IN+ performance. The OPA167x unity-gain bandwidth is 16 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

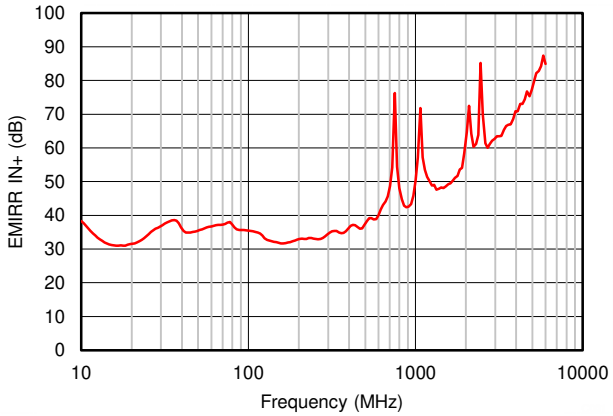


図 7-3. OPA167x EMIRR vs Frequency

表 7-1 lists the EMIRR IN+ values for the OPA167x at particular frequencies commonly encountered in real-world applications. Applications listed in 表 7-1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

表 7-1. OPA167x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	36 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	42 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	52 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	64 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	67 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	77 dB

7.3.3.1 EMIRR IN+ Test Configuration

図 7-4 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See the *EMI Rejection Ratio of Operational Amplifiers* application report for more details.

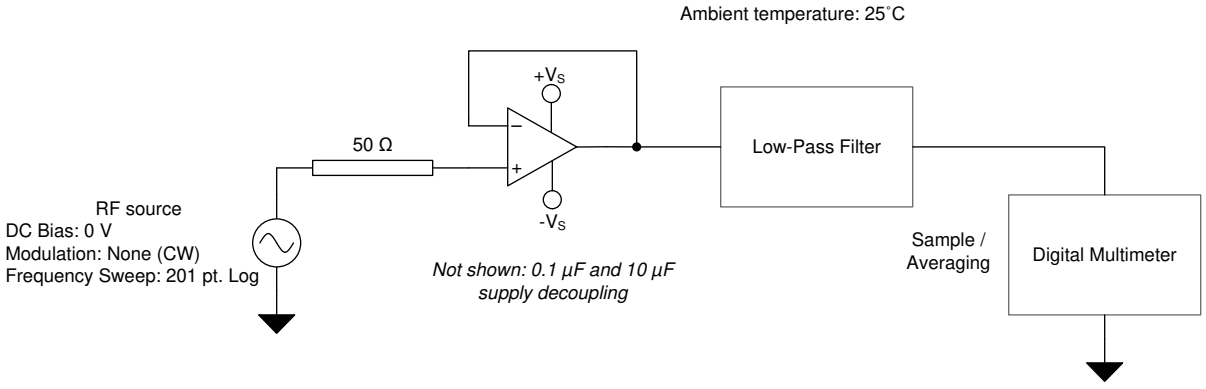


図 7-4. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA167x series op amps operate from ±2.25 V to ±18 V supplies while maintaining excellent performance. The OPA167x series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA167x series, power-supply voltages are not required to be equal. For example, the positive supply can be set to 25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are specified over the temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in セクション *6.8*.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Capacitive Loads

The dynamic characteristics of the OPA167x series are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier, and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device short-circuits. For more details about analysis techniques and application circuits, see the *Feedback Plots Define Op Amp AC Performance* application report, available for download from the TI website (www.ti.com).

8.2 Typical Applications

8.2.1 Phantom-Powered Preamplifier for Piezo Contact Microphones

Contact microphones are useful for amplifying the sound of musical instruments that do not contain electric pickups, such as acoustic guitars and violins. Most contact microphones use a piezo element to convert vibrations in the body of the musical instrument to a voltage which can be amplified or recorded. The low noise and low input bias current of the OPA1678 make the device an excellent choice for high impedance preamplifiers for piezo elements. This preamplifier circuit provides high input impedance for the piezo element but has low output impedance for driving long cable runs. The circuit is also designed to be powered from 48-V phantom power which is commonly available in professional microphone preamplifiers and recording consoles.

A TINA-TI™ simulation schematic of the circuit below is available in the *Tools and Software* section of the OPA1678 or OPA1679 product folder.

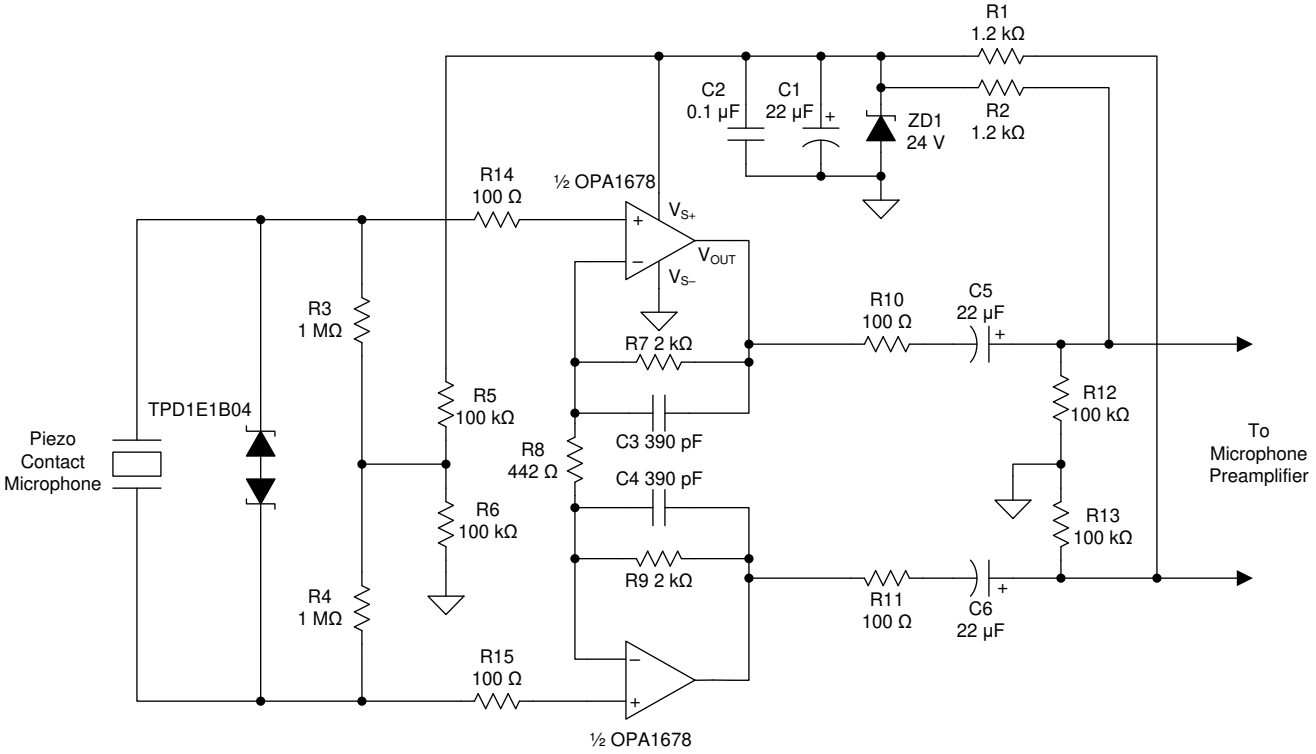


図 8-1. Phantom-Powered Preamplifier for Piezo Contact Microphones

8.2.1.1 Design Requirements

- –3-dB bandwidth: 20 Hz to 20 kHz
- Gain: 20 dB (10 V/V)
- Piezo element capacitance: 8 nF (9-kHz resonance)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Power Supply

In professional audio systems, phantom power is applied to the two signal lines that carry a differential audio signal from the microphone. 図 8-2 is a diagram of the system showing 48-V phantom power applied to the differential signal lines between the piezo preamplifier output and the input of a professional microphone preamplifier.

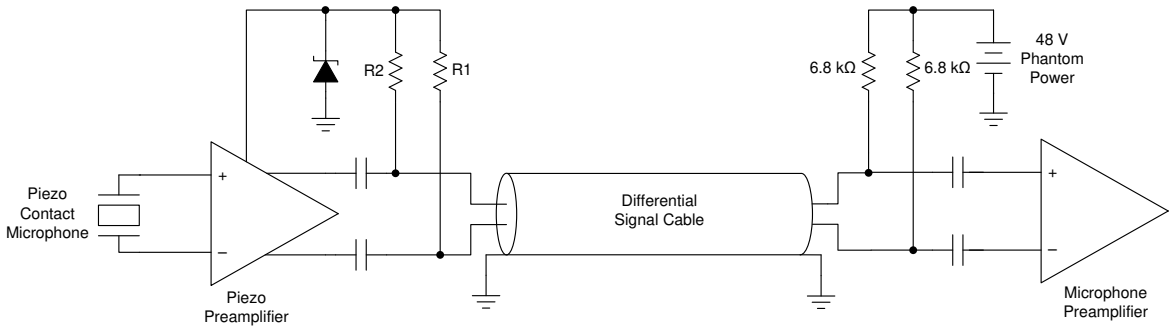


図 8-2. System Diagram Showing the Application of Phantom Power to the Audio Signal Lines

A voltage divider is used to extract the common-mode phantom power from the differential audio signal in this type of system. The voltage at center point of the voltage divider formed by R1 and R2 does not change when audio signals are present on the signal lines (assuming R1 and R2 are matched). A Zener diode forces the voltage at the center point of R1 and R2 to a regulated voltage. The values of R1 and R2 are determined by the allowable voltage drop across these resistors from the current delivered to both op amp channels and the Zener diode. There are two power supply current pathways in parallel, each sharing half the total current of the op amp and Zener diode. Resistors R1 and R2 can be calculated using 式 1:

$$R_1 = R_2 = R_{PS}$$
$$\frac{V_{ZD}}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8\ k\Omega = R_{PS} \quad (1)$$

A 24-V Zener diode is selected for this design, and 1 mA of current flows through the diode at idle conditions to maintain the reverse-biased condition of the Zener diode. The maximum idle power supply current of both op amp channels is 5 mA. Inserting these values into 式 1 gives the values for R1 and R2 shown in 式 2.

$$\frac{24V}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8\ k\Omega = \frac{24V}{\left(\frac{5.0\ mA}{2} + \frac{1.0\ mA}{2}\right)} - 6.8\ k\Omega = 1.2\ k\Omega = R_{PS} \quad (2)$$

Using a value of 1.2 kΩ for resistors R1 and R2 establishes a 1-mA current through the Zener diode and properly regulate the node to 24 V. Capacitor C1 forms a low-pass filter with resistors R1 and R2 to filter the Zener diode noise and any residual differential audio signals. Mismatch in the values of R1 and R2 causes a portion of the audio signal to appear at the voltage divider center point. The corner frequency of the low-pass filter must be set below the audio band, as shown in 式 3.

$$C_1 \geq \frac{1}{2 \cdot \pi \cdot R_1 \,||\, R_2 \cdot f_{-3dB}} \geq \frac{1}{2 \cdot \pi \cdot 600\ \Omega \cdot 20\ Hz} \geq 13\ \mu F \rightarrow 22\ \mu F \quad (3)$$

A 22-µF capacitor is selected because the capacitor meets the requirements for power supply filtering and is a widely available denomination. A 0.1-µF capacitor (C2) is added in parallel with C1 as a high-frequency bypass capacitor.

8.2.1.2.2 Input Network

Resistors R3 and R4 provide a pathway for the input bias current of the OPA1678 while maintaining the high input impedance of the circuit. The contact microphone capacitance and the required
low-frequency response determine the values of R3 and R4. The –3-dB frequency formed by the microphone capacitance and amplifier input impedance is shown in Equation 4:

$$F_{-3dB} = \frac{1}{2 \cdot \pi \cdot (R_3 + R_4) \cdot C_{MIC}} \leq 20 \text{ Hz} \tag{4}$$

A piezo element with 8 nF of capacitance was selected for this design because the 9-kHz resonance is towards the upper end of the audible bandwidth, and is less likely to affect the frequency response of many musical instruments. The minimum value for resistors R3 and R4 is then calculated with Equation 5:

$$R_3 = R_4 = R_{IN}$$
$$R_{IN} \geq \frac{1}{4 \cdot \pi \cdot F_{-3dB} \cdot C_{MIC}} \geq \frac{1}{4 \cdot \pi \cdot 20 \text{ Hz} \cdot 8 \text{ nF}} \geq 497.4 \text{ k}\Omega \tag{5}$$

1-MΩ resistors are selected for R3 and R4 to make sure the circuit meets the design requirements for –3-dB bandwidth. The center point of resistors R3 and R4 is biased to half the supply voltage through the voltage divider formed by R5 and R6. This sets the input common-mode voltage of the circuit to a value within the input voltage range of the OPA1678. Piezo elements can produce very large voltages if the elements are struck with sufficient force. To prevent damage, the input of the OPA1678 is protected by a transient voltage suppressor (TVS) diode placed across the preamplifier inputs. The TPD1E1B04 TVS was selected due to low capacitance and the 6.4-V clamping voltage does not clamp the desired low amplitude vibration signals. Resistors R14 and R15 limit current flow into the amplifier inputs in the event that the internal protection diodes of the amplifier are forward-biased.

8.2.1.2.3 Gain

R7, R8, and R9 determines the gain of the preamplifier circuit. The gain of the circuit is shown in Equation 6:

$$A_V = 1 + \frac{R_7 + R_9}{R_8} = 10 \text{ V/V} \tag{6}$$

Resistors R7 and R9 are selected with a value of 2 kΩ to avoid loading the output of the OPA1678 and producing distortion. The value of R8 is then calculated in Equation 7:

$$R_8 = \frac{R_7 + R_9}{A_V - 1} = \frac{2 \text{ k}\Omega + 2 \text{ k}\Omega}{10 - 1} = 444.4 \ \Omega \rightarrow 442 \ \Omega \tag{7}$$

Capacitors C3 and C4 limit the bandwidth of the circuit so that signals outside the audio bandwidth are not amplified. The corner frequency produced by capacitors C3 and C4 is shown in Equation 8. This corner frequency must be above the desired –3-dB bandwidth point to avoid attenuating high-frequency audio signals.

$$C_3 = C_4 = C_{FB}$$
$$C_{FB} \leq \frac{1}{2 \cdot \pi \cdot F_{-3dB} \cdot R_{7/9}} \leq \frac{1}{2 \cdot \pi \cdot 20 \text{ kHz} \cdot 2 \text{ k}\Omega} \leq 3.98 \text{ nF} \tag{8}$$

C3 and C4 are 390-pF capacitors, which places the corner frequency approximately 1 decade above the desired –3-dB bandwidth point. Capacitors C3 and C4 must be NP0 or C0G type ceramic capacitors or film capacitors. Other ceramic dielectrics, such as X7R, are not suitable for these capacitors and produce distortion.

8.2.1.2.4 Output Network

The audio signal is ac-coupled onto the microphone signal lines through capacitors C5 and C6. The value of capacitors C5 and C6 are determined by the low-frequency design requirements and the input impedance of the microphone preamplifier that connect to the output of the circuit. 式 9 shows an approximation of the capacitor value requirements, and neglects the effects of R10, R11, R12, and R13 on the frequency response. The microphone preamplifier input impedance (R_{IN_MIC}) uses a typical value of 4.4 kΩ for the calculation.

$$C_5 = C_6 = C_{OUT}$$

$$C_{OUT} \geq \frac{2}{2 \cdot \pi \cdot R_{IN\_MIC} \cdot 20\ Hz} \geq \frac{2}{2 \cdot \pi \cdot 4.4\ k\Omega \cdot 20\ Hz} \geq 3.6\ \mu F \quad (9)$$

For simplicity, the same 22-µF capacitors selected for the power supply filtering are selected for C5 and C6 to satisfy 式 9. At least 50-V rated capacitors must be used for C5 and C6. If polarized capacitors are used, the positive terminal must be oriented towards the microphone preamplifier. Resistors R10 and R11 isolate the op amp outputs from the capacitance of long cables that can cause instability. R12 and R13 discharge ac-coupling capacitors C4 and C5 when phantom power is removed.

8.2.1.3 Application Curves

The frequency response of the preamplifier circuit is shown in 図 8-3. The –3-dB frequencies are 15.87 Hz and 181.1 kHz, which meet the design requirements. The gain within the passband of the circuit is 18.9 dB, slightly less than the design goal of 20 dB. The reduction in gain is a result of the voltage division between the output resistors of the piezo preamplifier circuit and the input impedance of the microphone preamplifier. The A-weighted noise of the circuit (referred to the input) is 842.2 nV_{RMS} or –119.27 dBu.

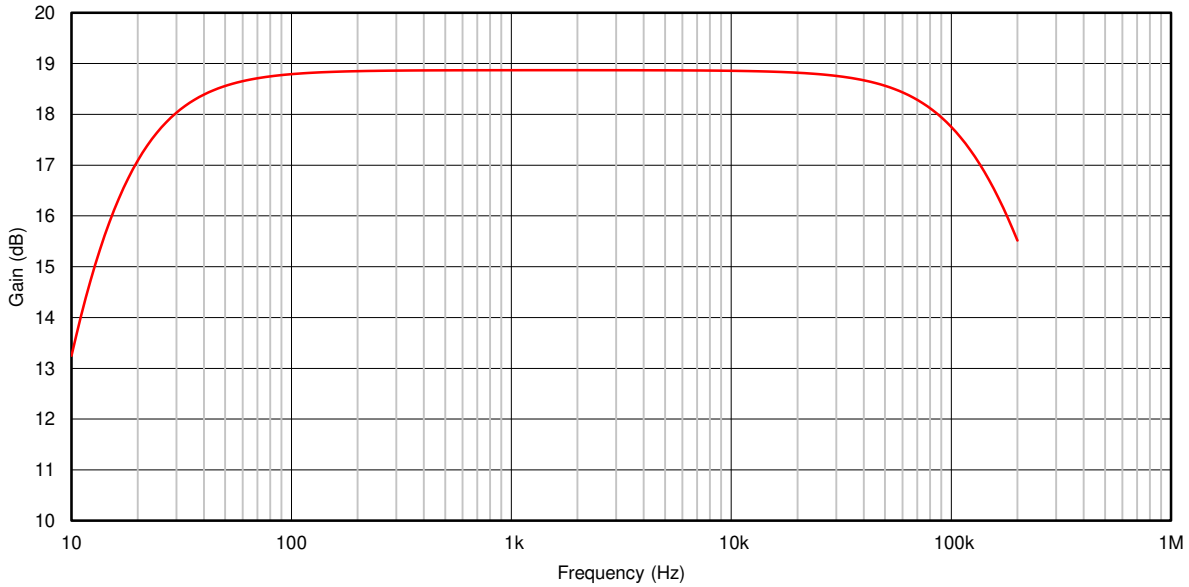


図 8-3. Frequency Response of the Preamplifier Circuit for a 8-nF Piezo Element

8.2.2 Phono Preamplifier for Moving Magnet Cartridges

The noise and distortion performance of the OPA167x family of amplifiers is exceptional in applications with high source impedances, which makes these devices a viable choice in preamplifier circuits for moving magnet (MM) phono cartridges. 図 8-4 shows a preamplifier circuit for MM cartridges with 40 dB of gain at 1 kHz.

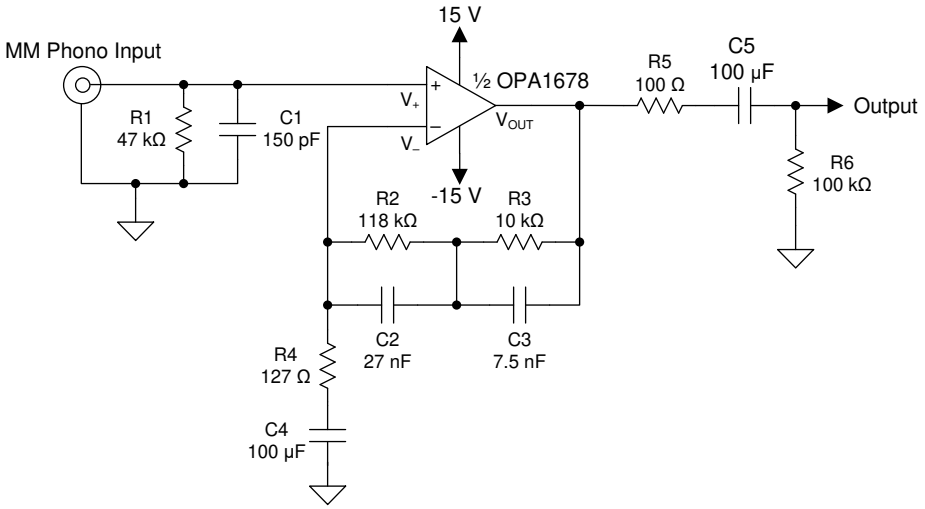


図 8-4. Phono Preamplifier for Moving Magnet Cartridges (Single-Channel Shown)

8.2.3 Single-Supply Electret Microphone Preamplifier

The preamplifier circuit shown in 図 8-5 operates the OPA1678 as a transimpedance amplifier that converts the output current from the electret microphone internal JFET into a voltage. Resistor R4 determines the gain of the circuit. Resistors R2 and R3 bias the input voltage to half the power supply voltage for proper functionality on a single-supply.

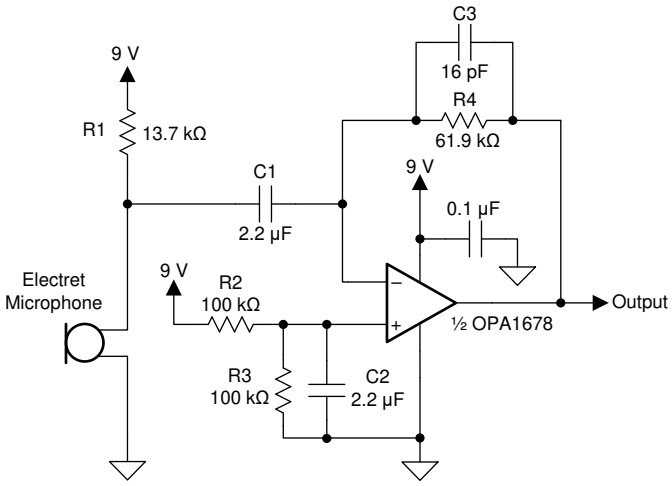


図 8-5. Single-Supply Electret Microphone Preamplifier

8.2.4 Composite Headphone Amplifier

図 8-6 shows the BUF634A buffer inside the feedback loop of the OPA1678 to increase the available output current for low-impedance headphones. If the BUF634A is used in wide-bandwidth mode, no additional components besides the feedback resistors are required to maintain loop stability.

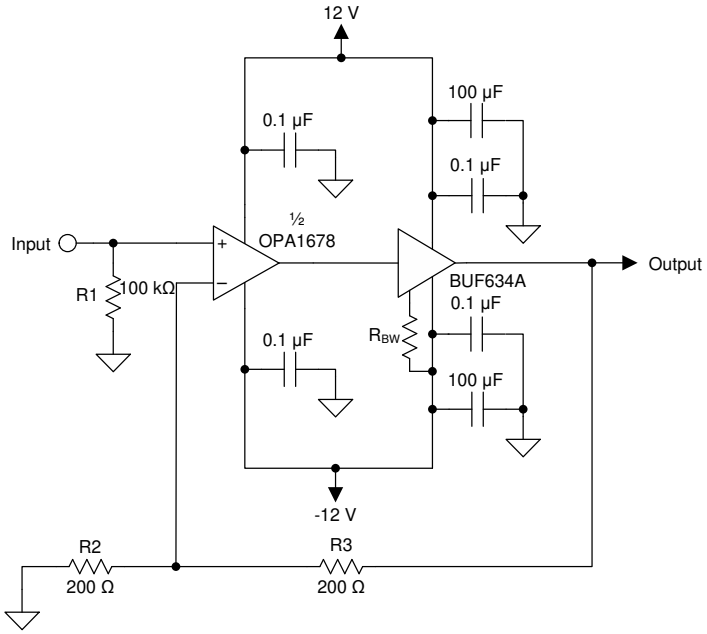


図 8-6. Composite Headphone Amplifier (Single-Channel Shown)

8.2.5 Differential Line Receiver With AC-Coupled Outputs

図 8-7 shows the OPA1678 used as an integrator that drives the reference pin of the INA1650, which forces the output dc voltage to 0 V. This configuration is an alternative to large ac-coupling capacitors that can distort at high output levels. The low input bias current and low input offset voltage of the OPA1678 make the device an excellent choice for integrator applications.

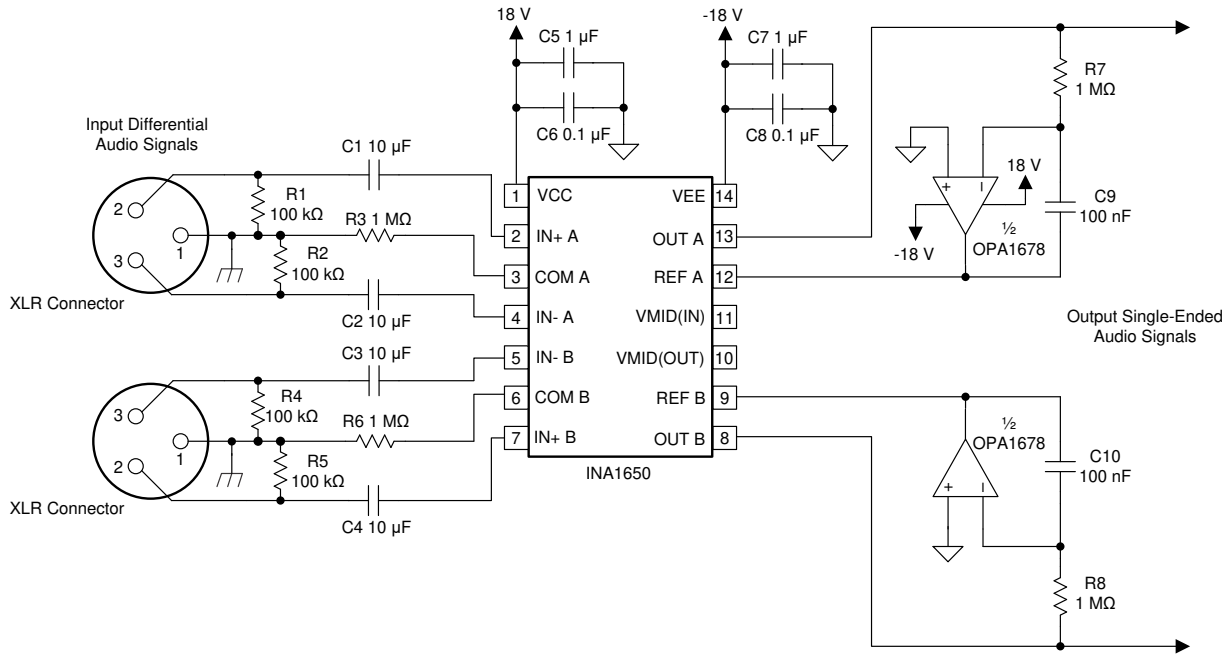


図 8-7. Differential Line Receiver With AC-Coupled Outputs

8.3 Power Supply Recommendations

The OPA167x devices are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in *セクション 6.8*. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

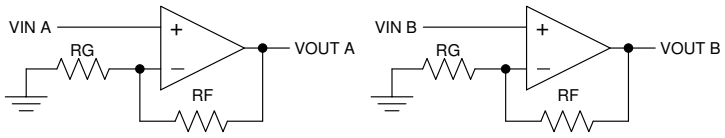
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 8-8, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.

- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.1.1 Power Dissipation

The OPA167x series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA167x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

8.4.2 Layout Example



(Schematic Representation)

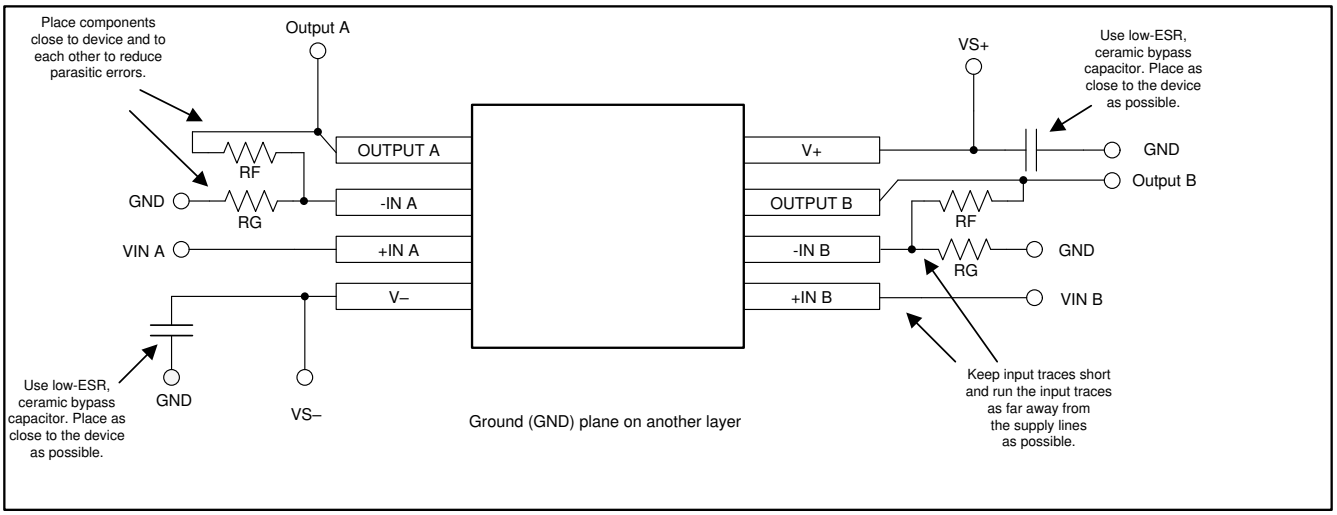


図 8-8. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

9.1.1.2 TINA-TI™ シミュレーション・ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア・フォルダから、無償の TINA-TI シミュレーション・ソフトウェアをダウンロードしてください。

9.1.1.3 DIP アダプタ評価基板

DIP アダプタ評価基板は、オペアンプの迅速なプロトタイプ製作とテストを可能にする評価基板です。小型の表面実装デバイスとのインターフェイスを迅速、容易、低コストで実現します。付属の Samtec 端子ストリップか、直接配線により既存の回路へサポートされているオペアンプを接続します。DIP アダプタ評価基板キットは、以下の業界標準パッケージをサポートしています。D または U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV (SOT-23-6、SOT-23-5、および SOT-23-3)、DCK (SC70-6 および SC70-5)、および DRL (SOT563-6)。

9.1.1.4 DIYAMP-EVM

DIYAMP-EVM は、実際のアンプ回路を提供する独自の評価基板 (EVM) であり、設計コンセプトの迅速な評価とシミュレーションの検証を実現します。この評価基板は、3 つの業界標準パッケージ (SC70、SOT23、SOIC) で供給されており、シングル / デュアル電源向けに、アンプ、フィルタ、安定性補償、コンパレータの各構成など、12 の一般的なアンプ構成が可能です。

9.1.1.5 TI のリファレンス・デザイン

TI のリファレンス・デザインは、TI の高精度アナログ・アプリケーション専門家により作成されたアナログ・ソリューションです。TI のリファレンス・デザインは、動作原理、部品の選択、シミュレーション、完全な PCB 回路図およびレイアウト、部品表、測定済みの性能を提供します。TI のリファレンス・デザインは、http://www.ti.com/ww/en/analog/precision-designs/ からオンラインで入手できます。

9.1.1.6 フィルタ設計ツール

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フィルタ設計ツールは、設計ツールとシミュレーション Web ページから Web 対応ツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

9.2 Documentation Support

9.2.1 Related Documentation

The following documents are relevant to using the OPA167x, and are recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- Texas Instruments, *Source resistance and noise considerations in amplifiers* technical brief
- Burr Brown, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Burr Brown, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively* application report
- Burr Brown, *Tuning in Amplifiers* application bulletin
- Burr Brown, *Feedback Plots Define Op Amp AC Performance* application bulletin
- Texas Instruments, *Active Volume Control for Professional Audio* precision design

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 Trademarks

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9.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1677DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	O1677
OPA1677DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O1677
OPA1677DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	O1677
OPA1677DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O1677
OPA1677DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP1677
OPA1677DR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP1677
OPA1678IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1AW7
OPA1678IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678
OPA1678IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGR.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGRG4	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGRG4.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGRG4.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGT.A	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1678IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OP1678
OPA1679IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1679IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679
OPA1679IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	OPA1679
OPA1679IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679
OPA1679IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679
OPA1679IPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679
OPA1679IRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679
OPA1679IRUMR.A	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679
OPA1679IRUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679
OPA1679IRUMT	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679
OPA1679IRUMT.A	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679
OPA1679IRUMT.B	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1679

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA1679 :

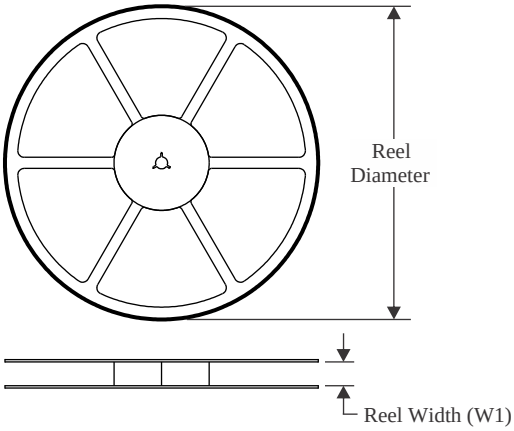
- Automotive : OPA1679-Q1

NOTE: Qualified Version Definitions:

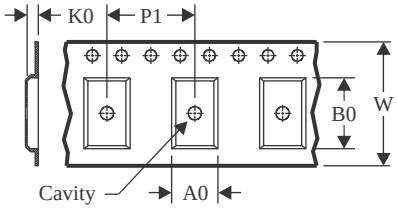
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

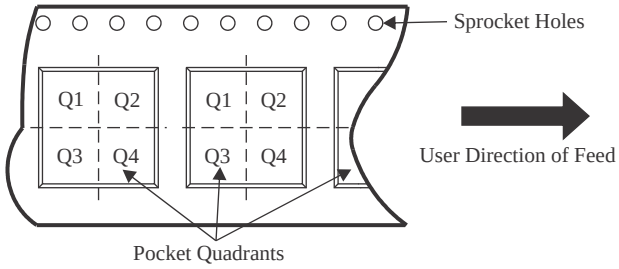


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

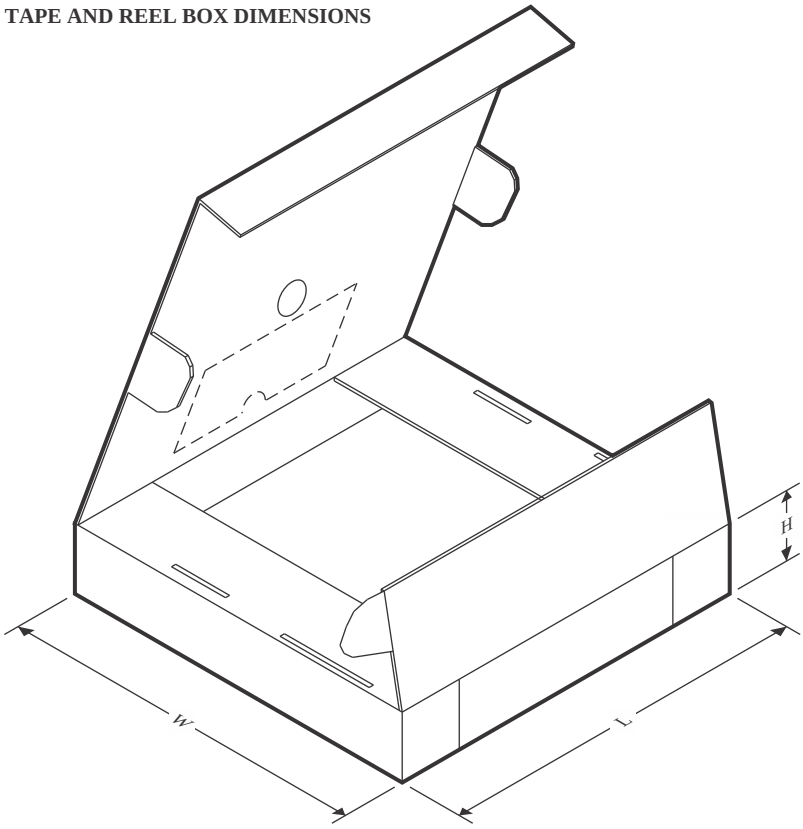
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1677DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1677DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1677DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1678IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1678IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1678IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1678IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1678IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1678IDRGRG4	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1678IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1679IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1679IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA1679IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA1679IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA1679IRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

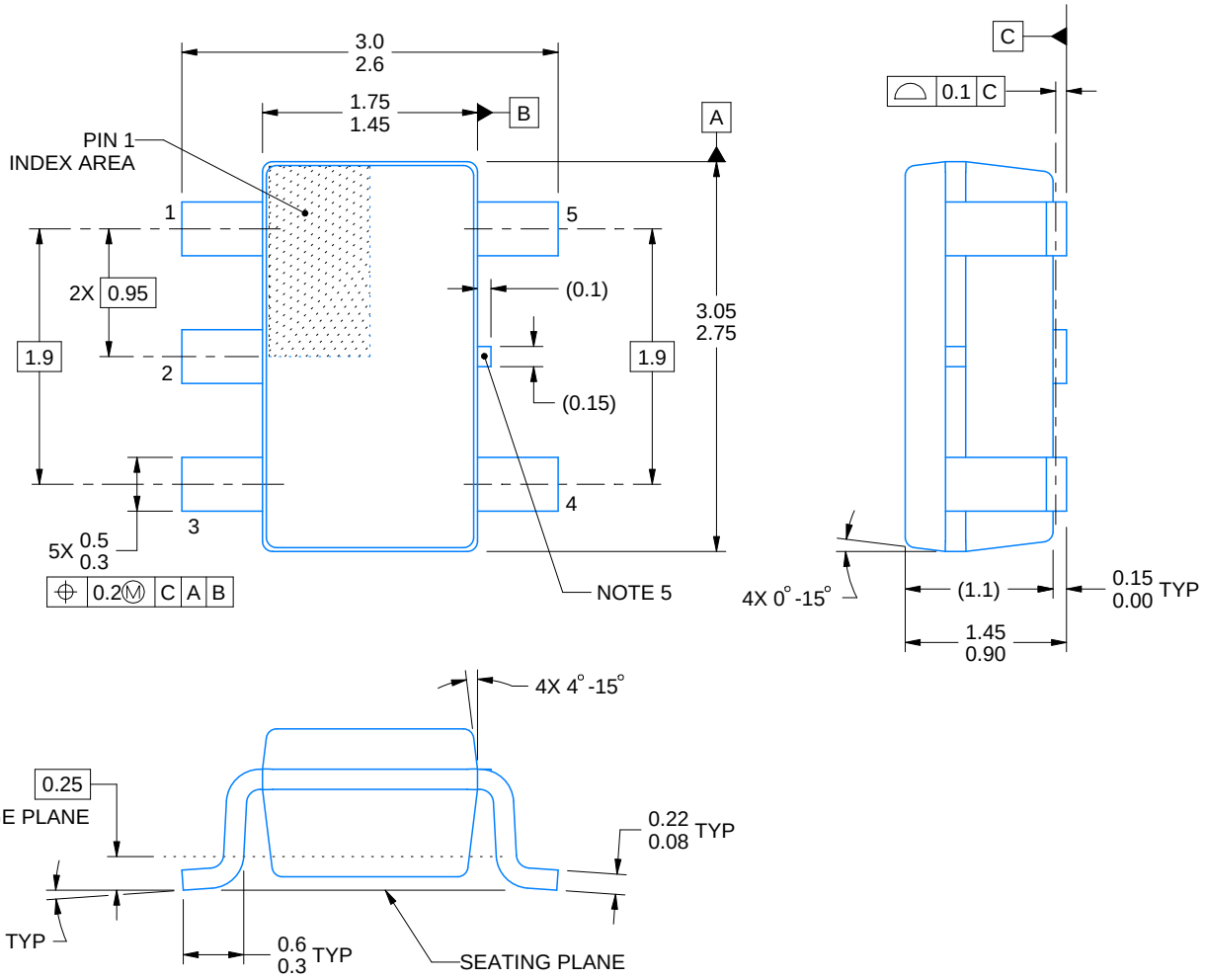
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1677DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA1677DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA1677DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA1678IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1678IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA1678IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA1678IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA1678IDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA1678IDRGRG4	SON	DRG	8	3000	346.0	346.0	33.0
OPA1678IDRGT	SON	DRG	8	250	182.0	182.0	20.0
OPA1679IDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA1679IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA1679IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA1679IRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
OPA1679IRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

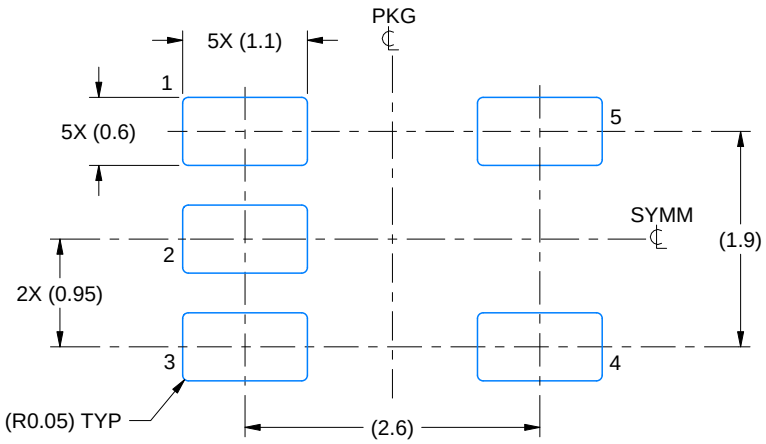
SMALL OUTLINE TRANSISTOR



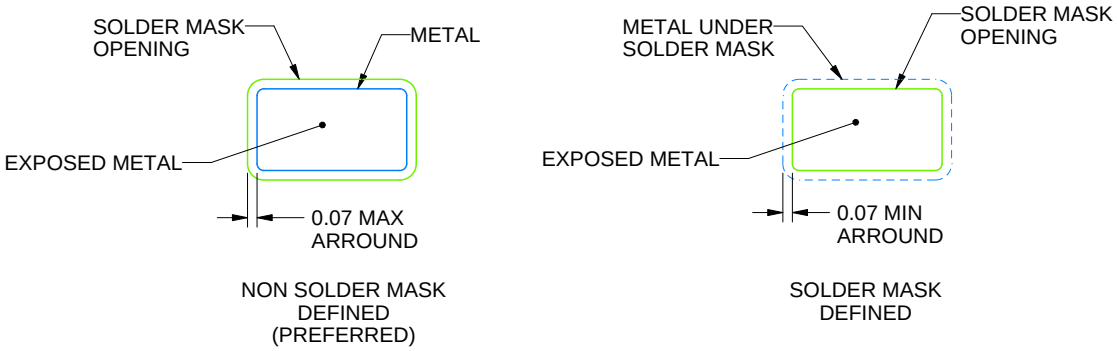
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

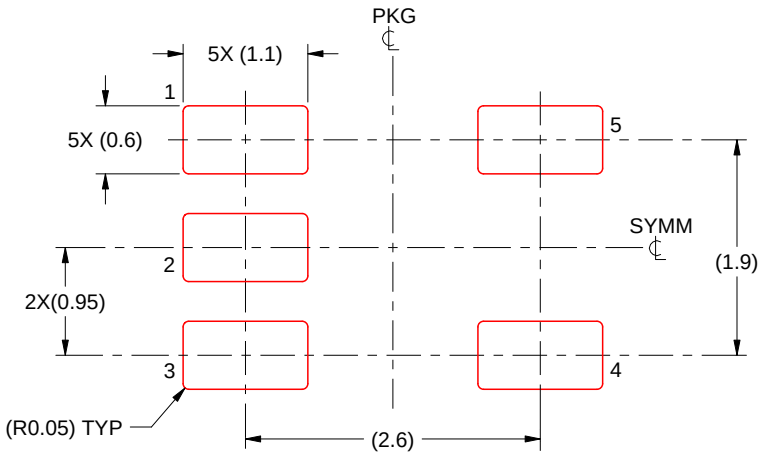


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

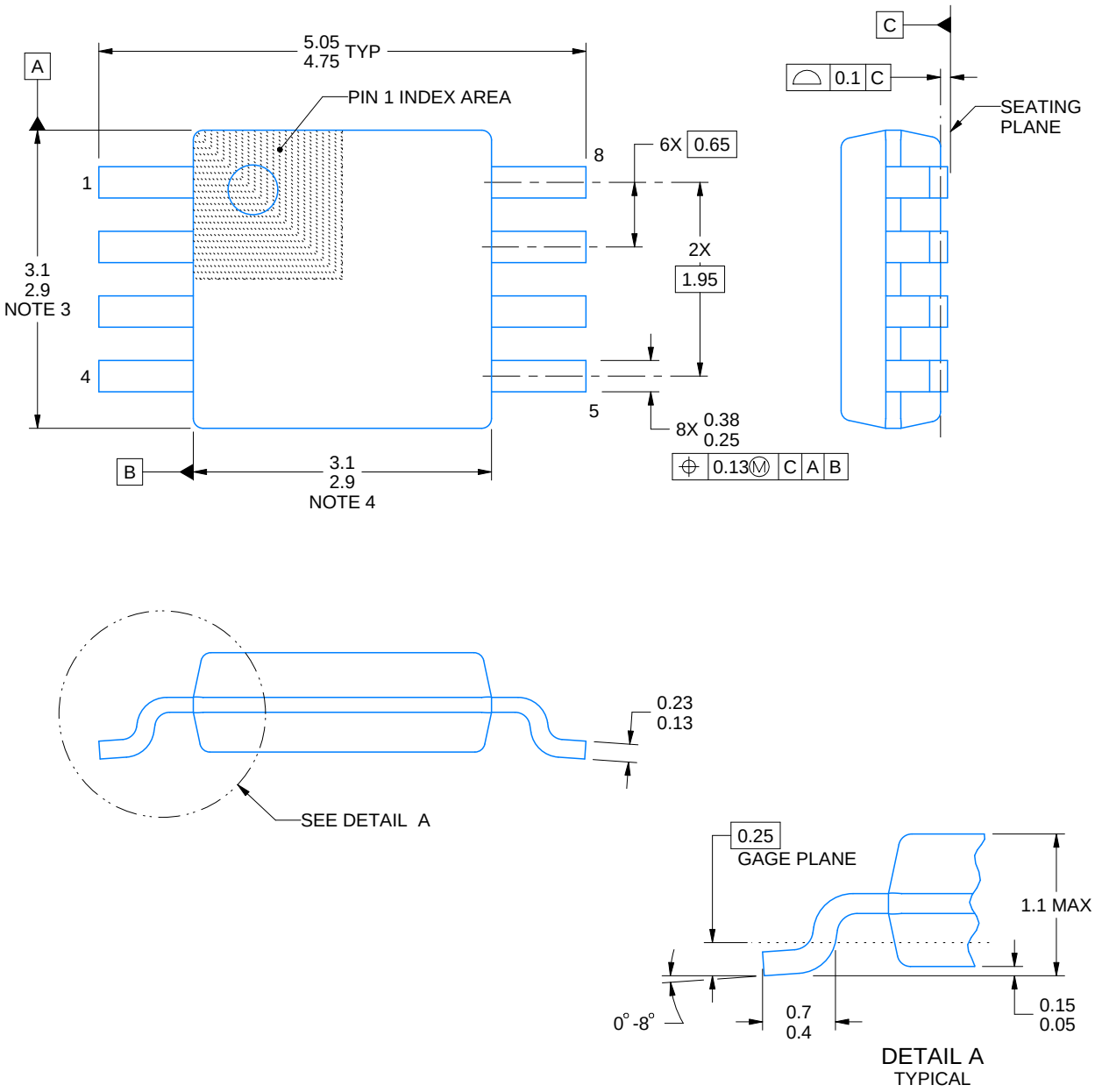
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

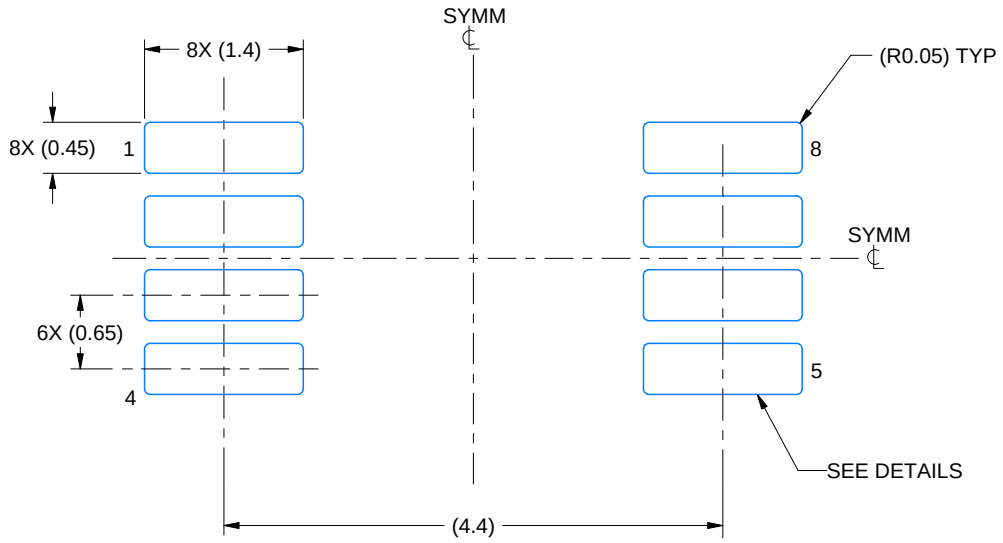
SMALL OUTLINE PACKAGE



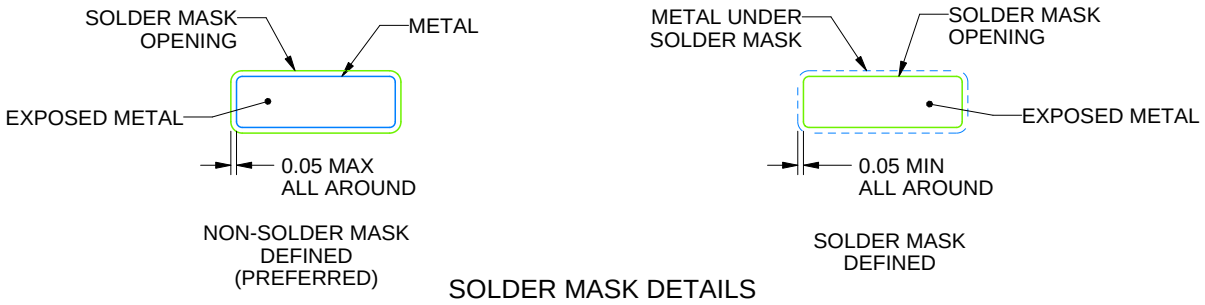
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

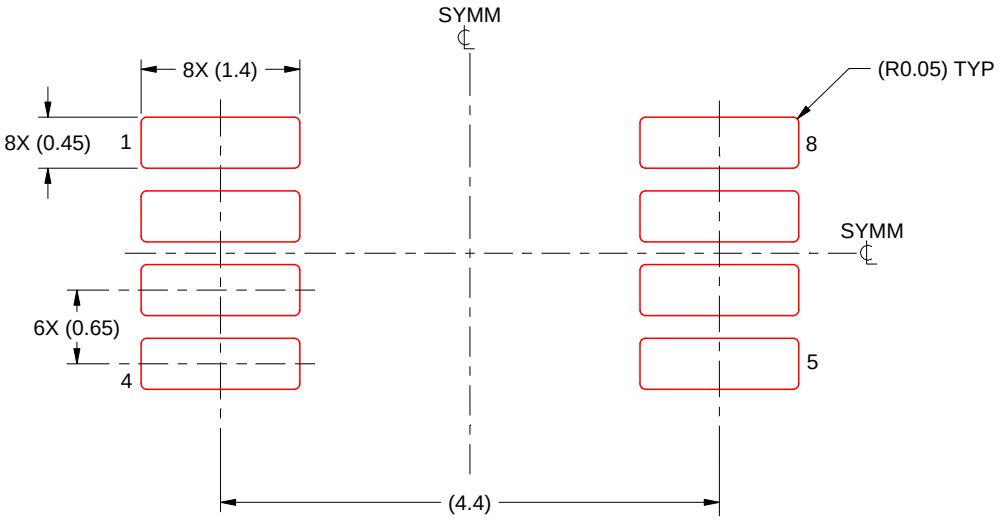


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

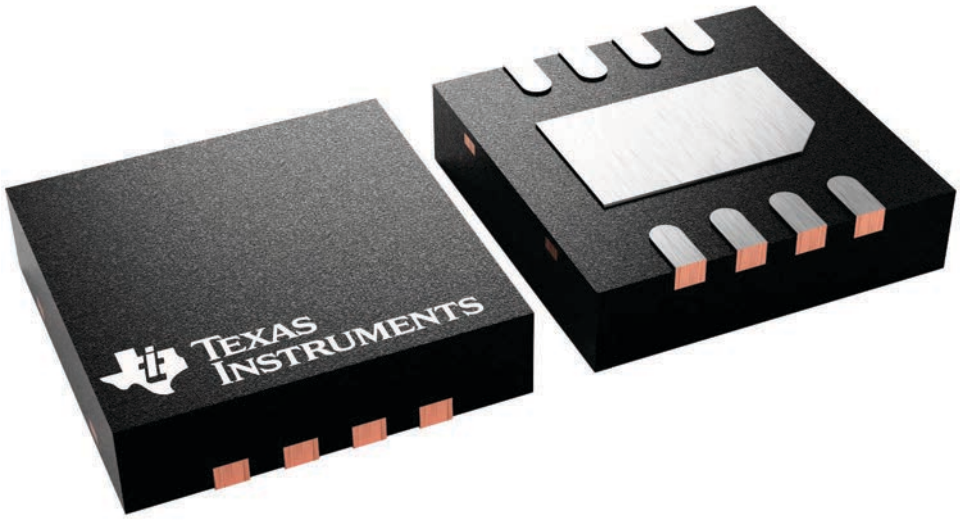
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



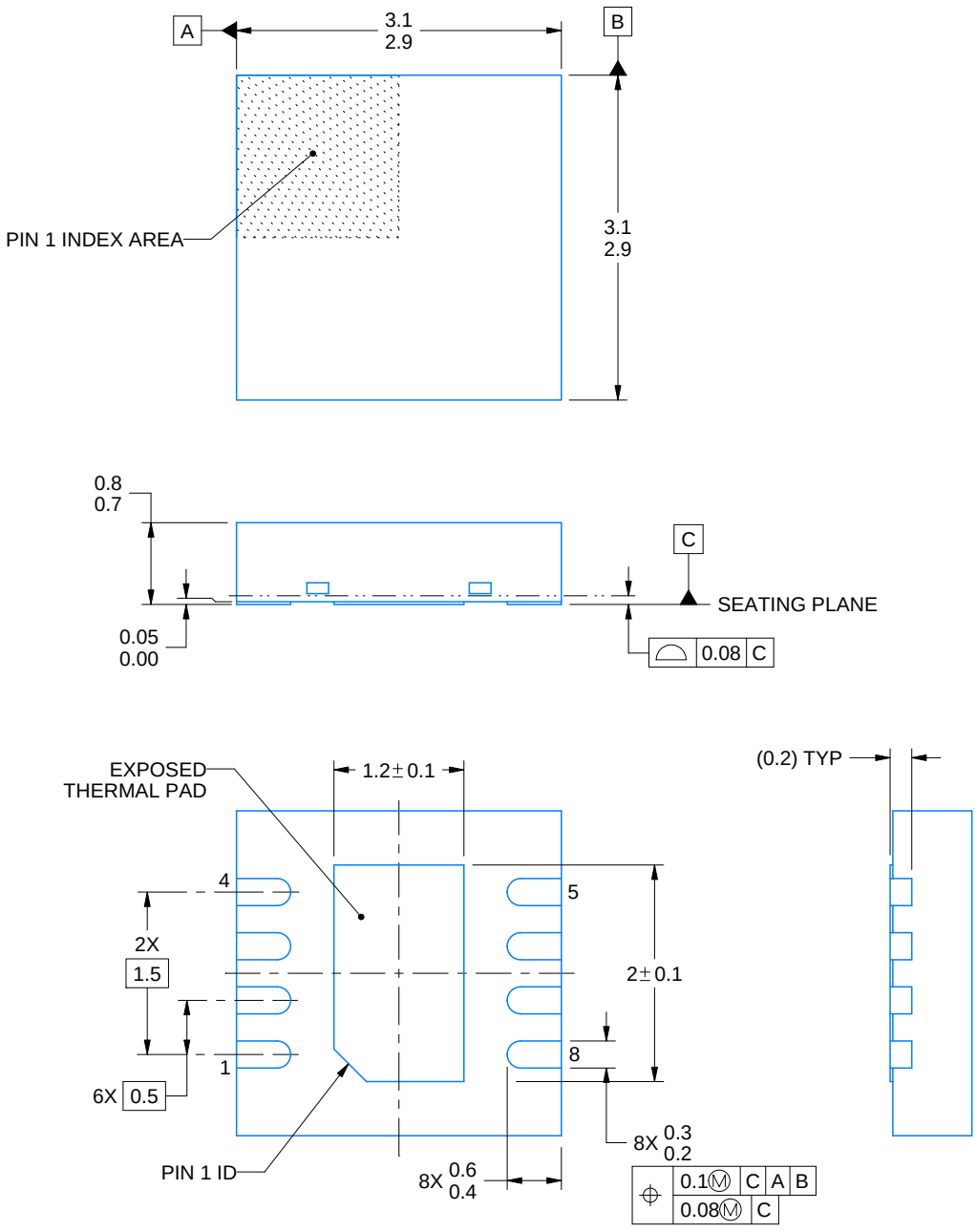
4225794/A

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

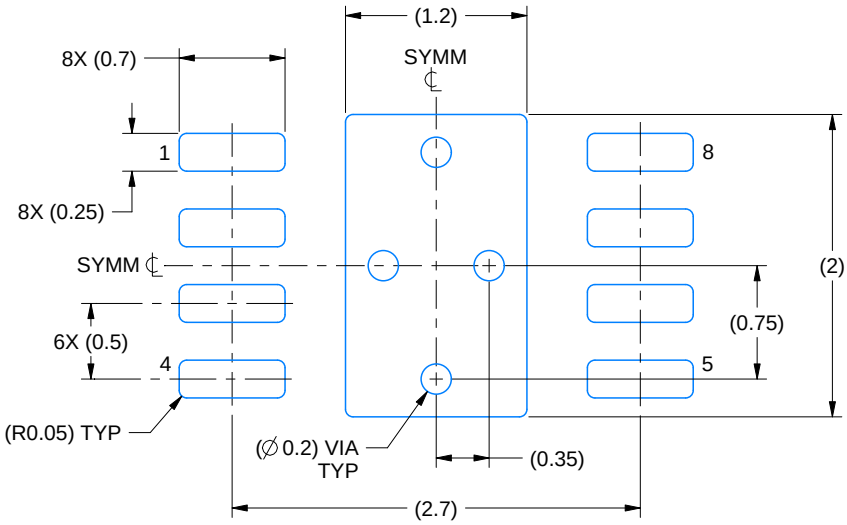
PLASTIC SMALL OUTLINE - NO LEAD



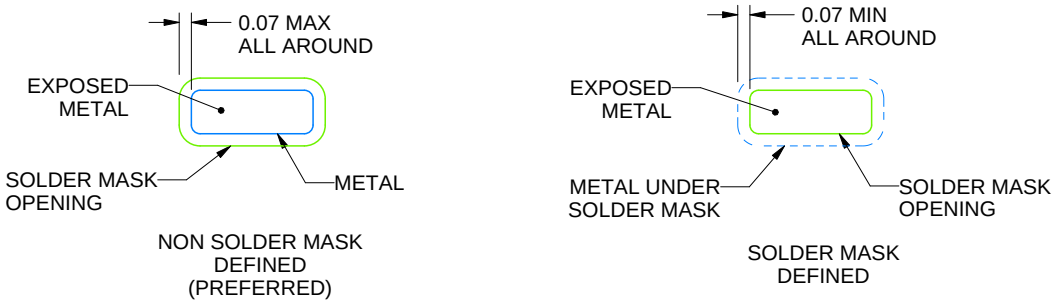
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

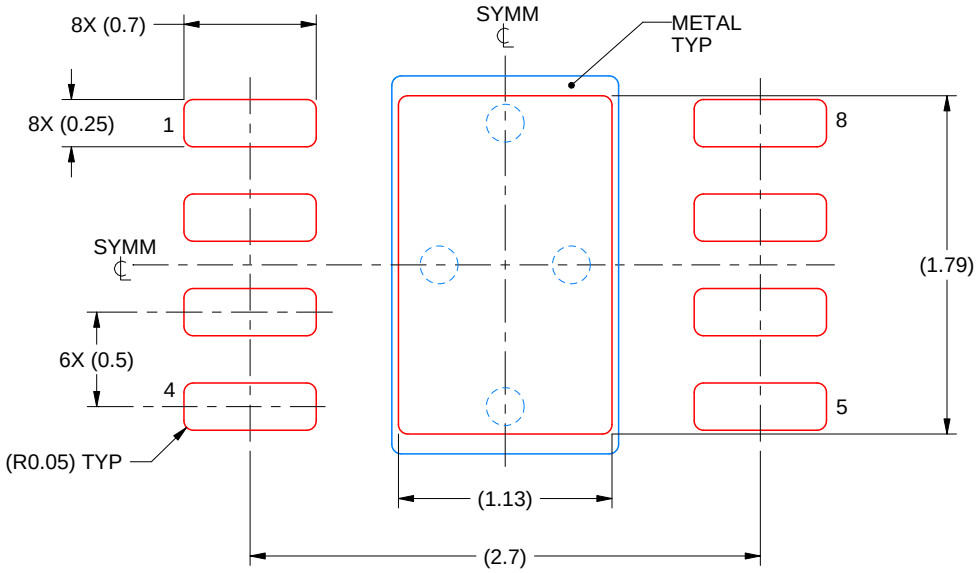


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



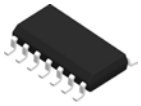
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

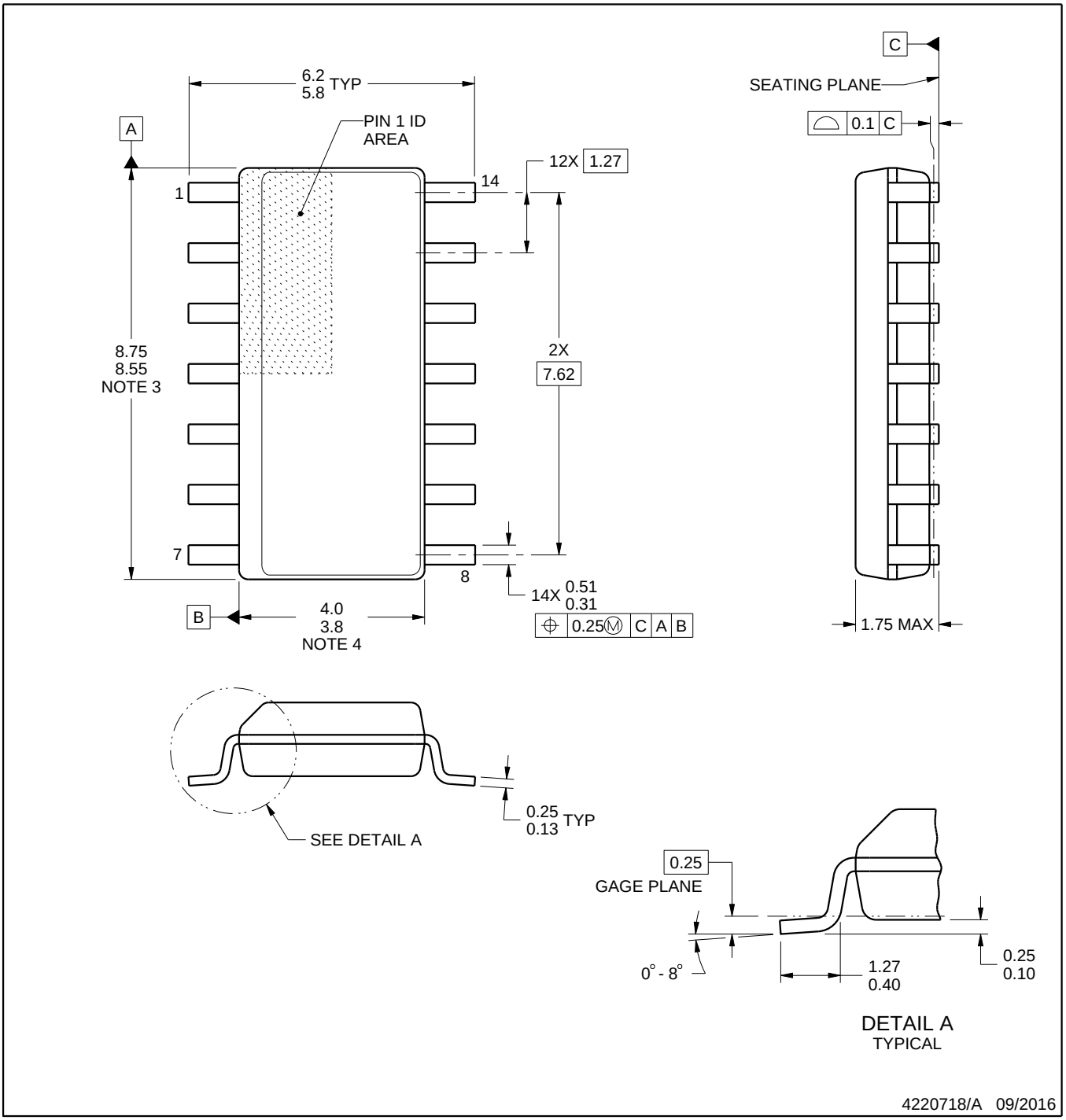


PACKAGE OUTLINE

D0014A

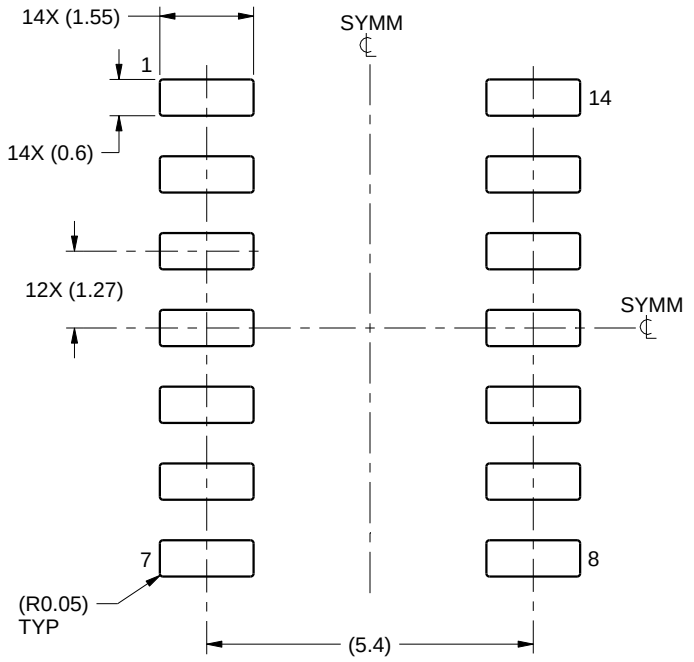
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

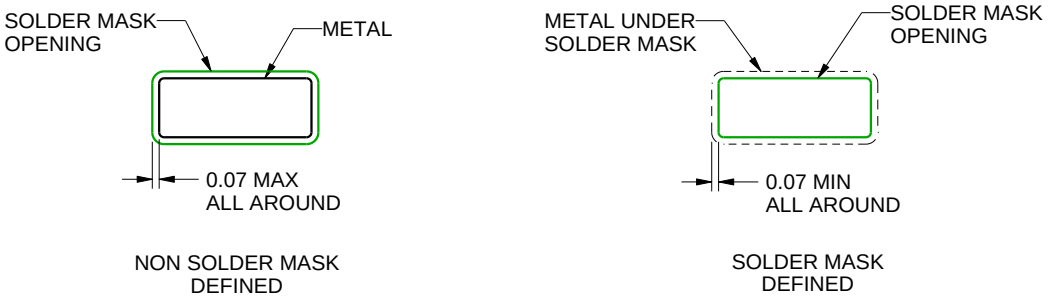


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

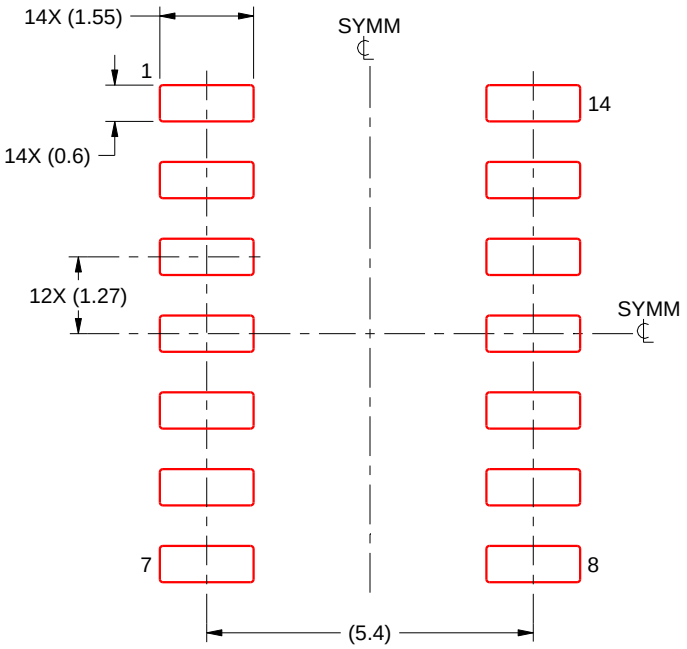
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

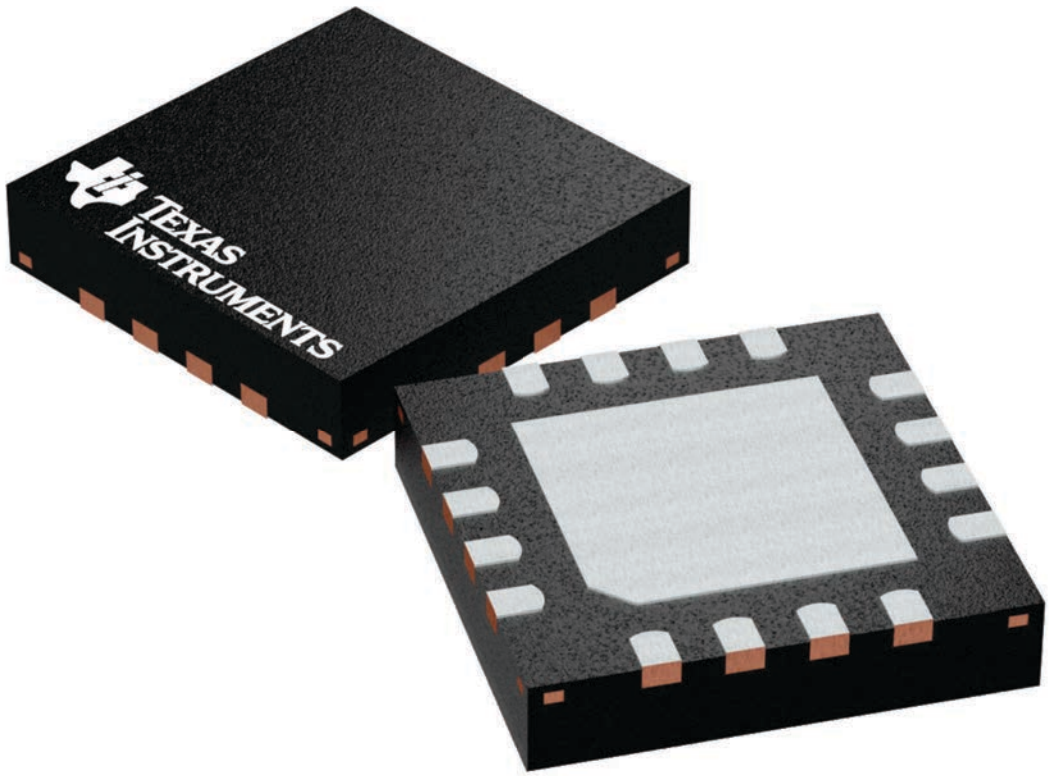
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

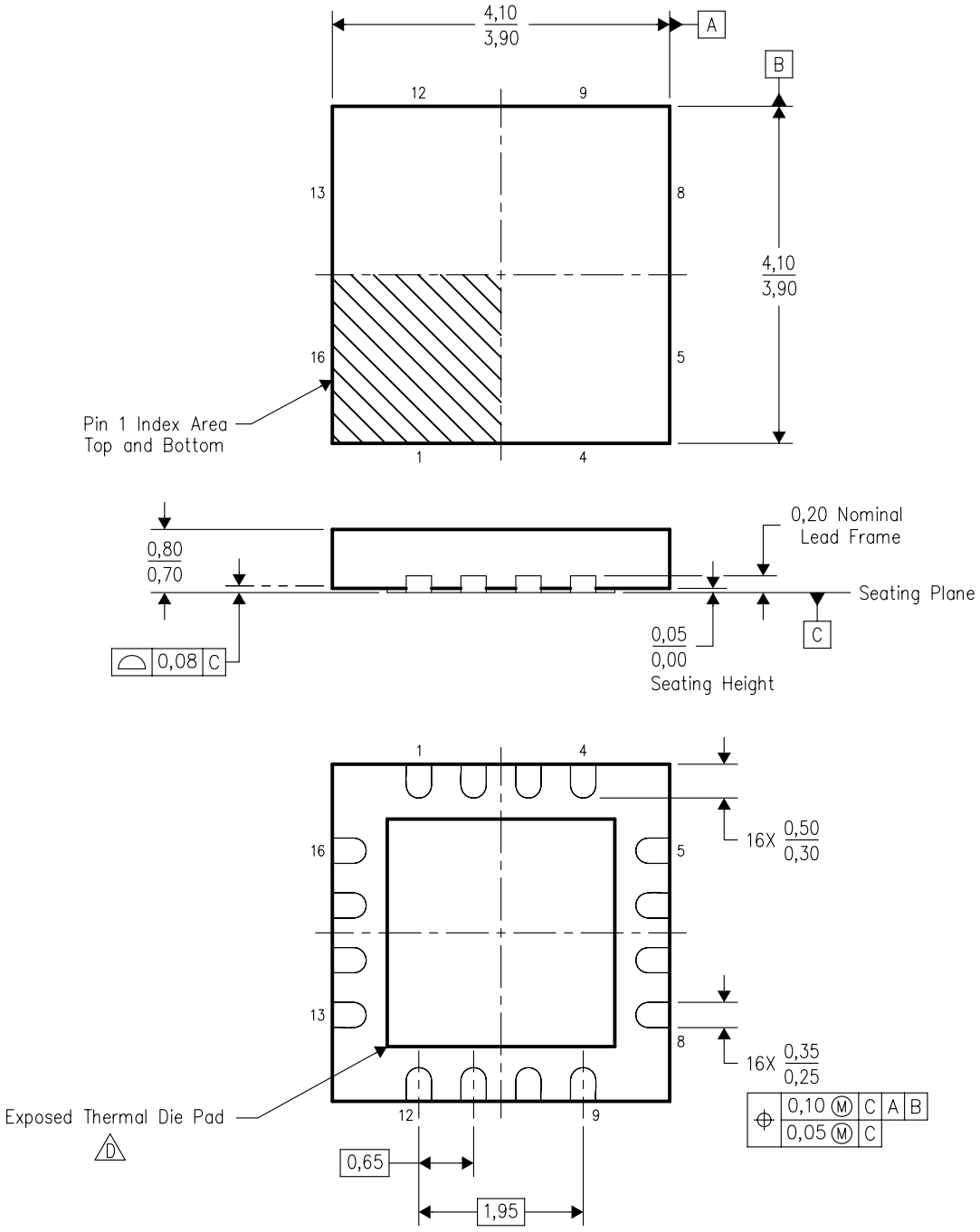
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

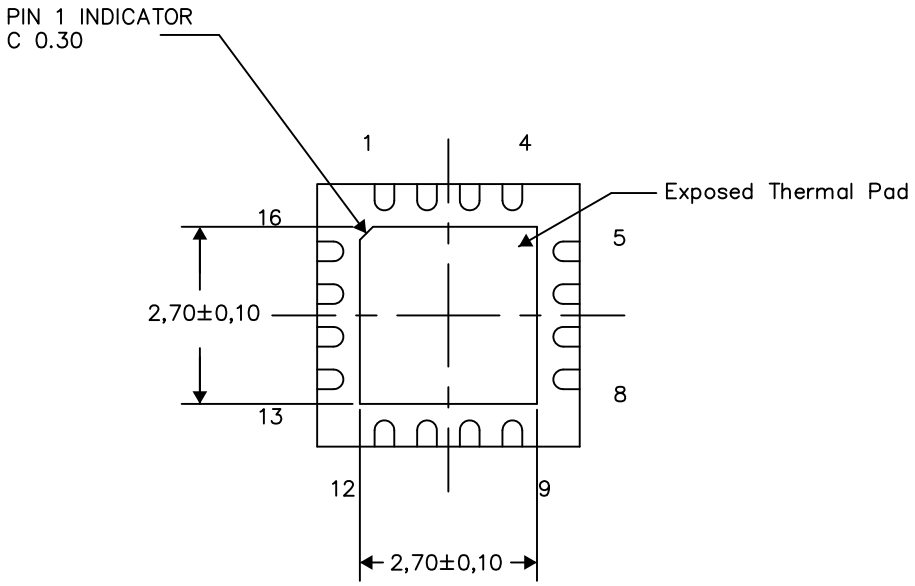
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

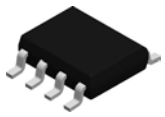


Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

NOTES: All linear dimensions are in millimeters

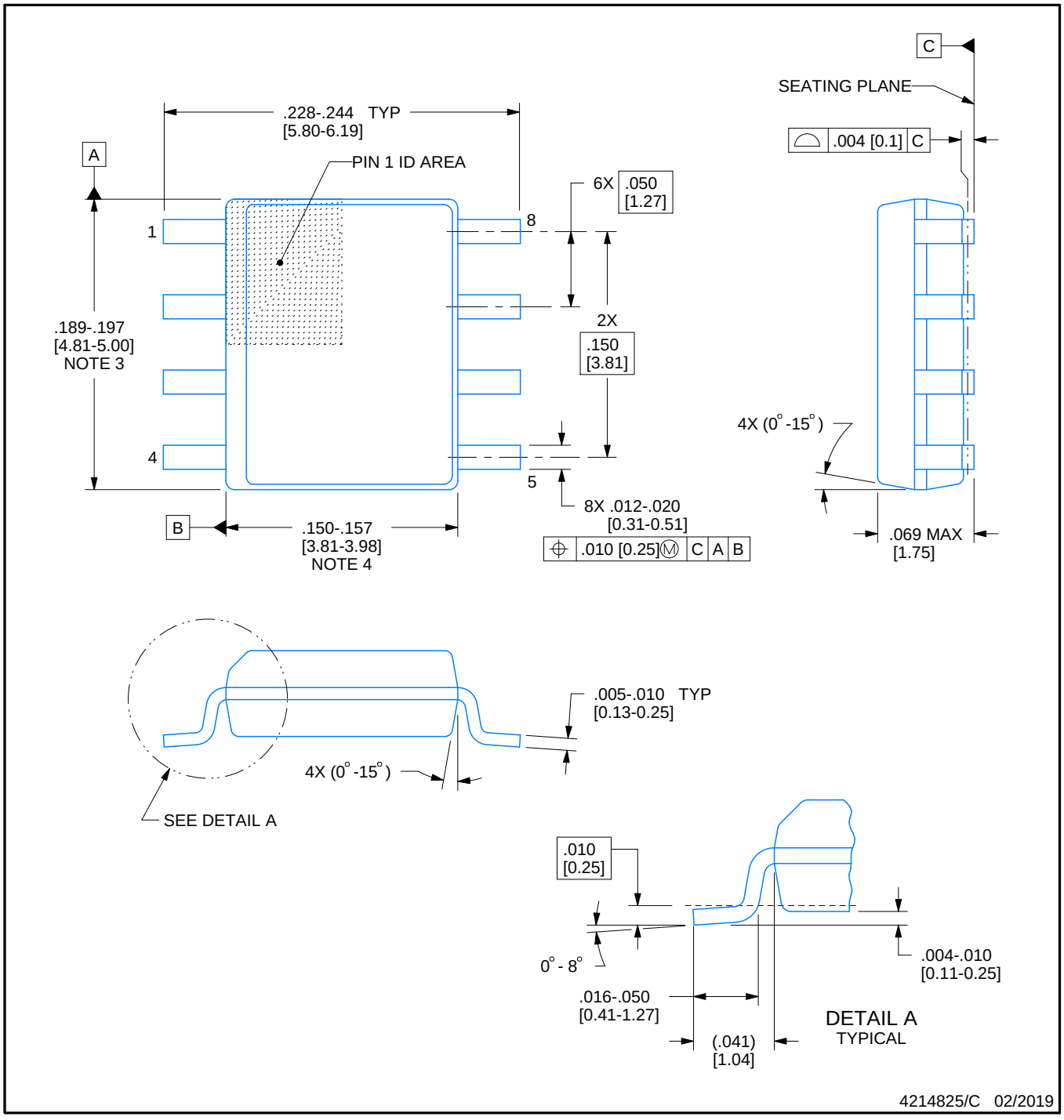


PACKAGE OUTLINE

D0008A

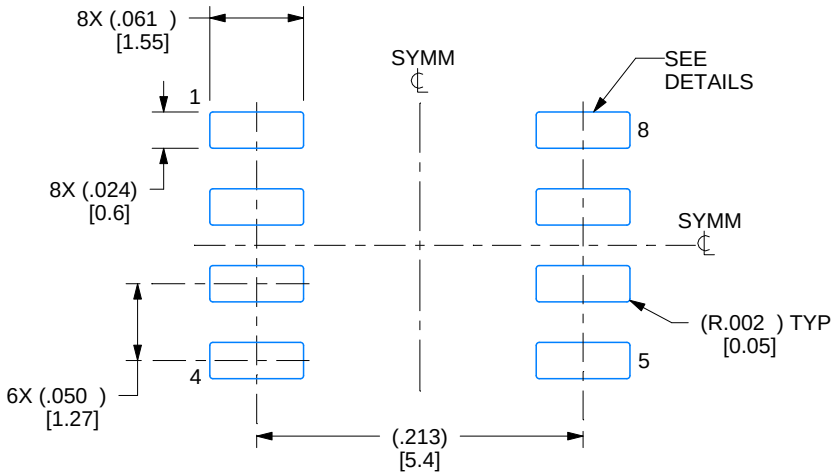
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

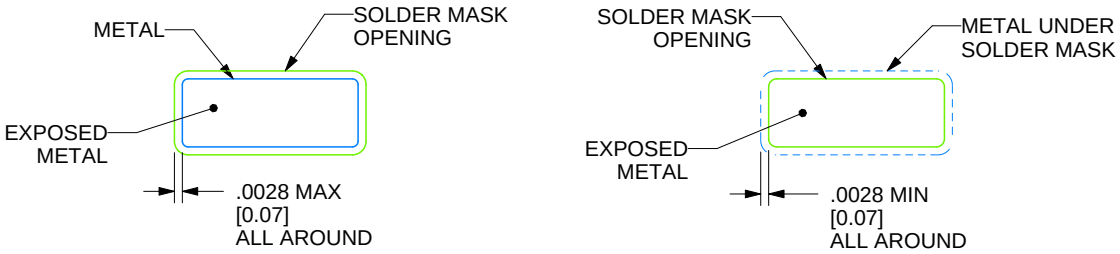


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

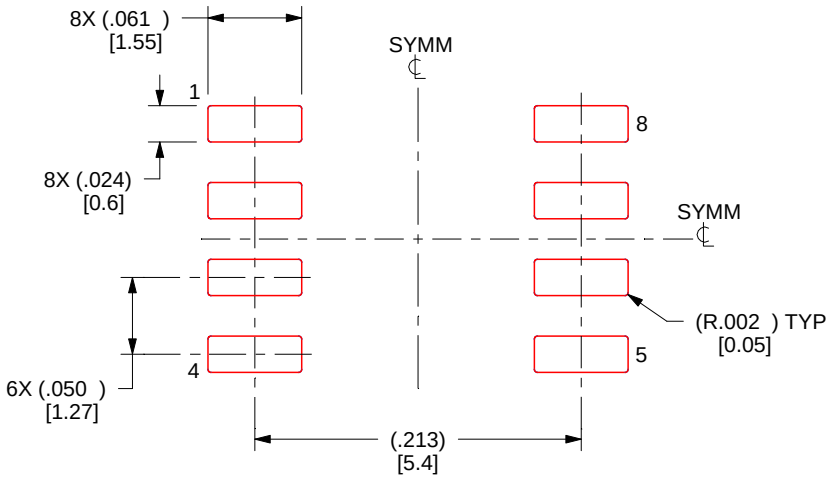
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

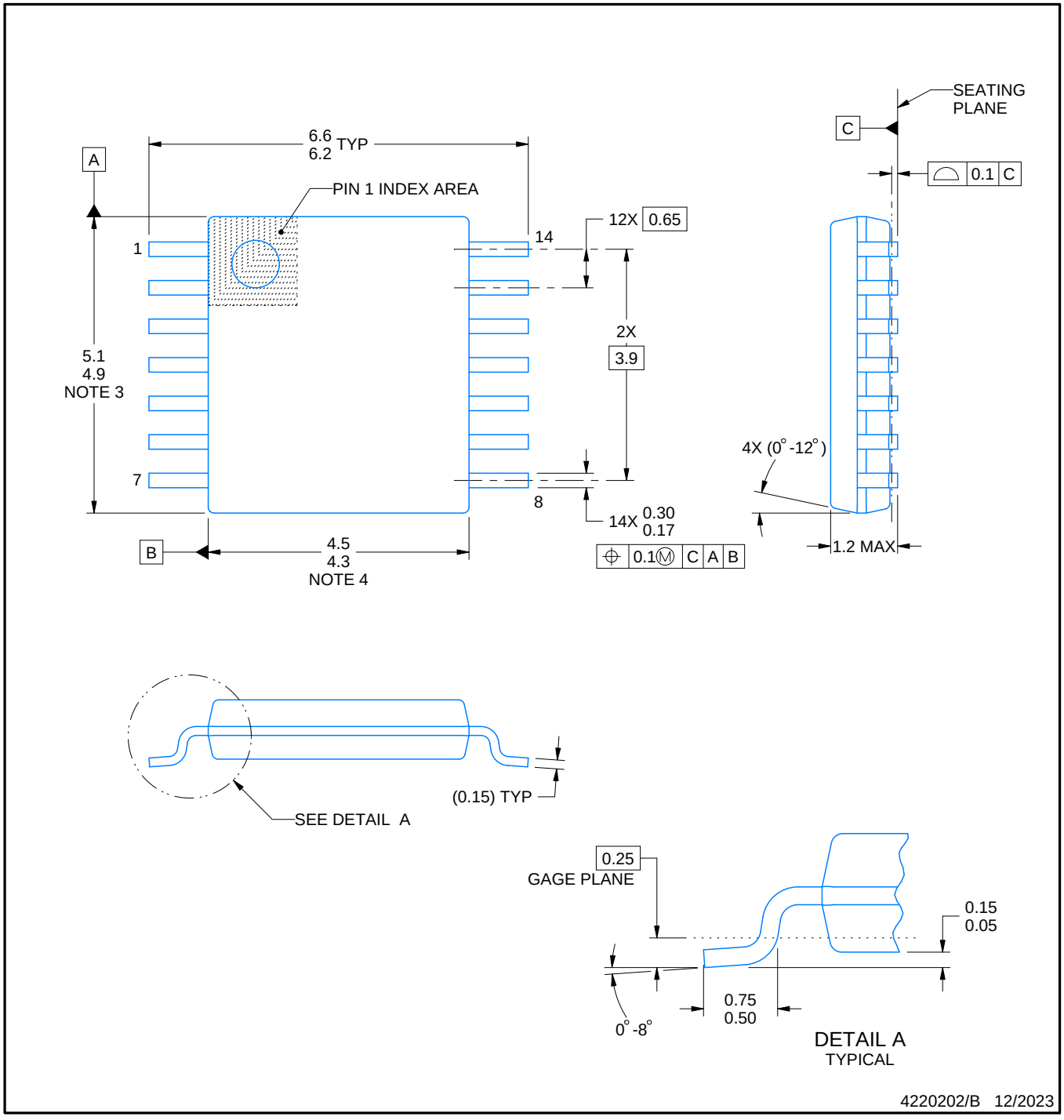
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

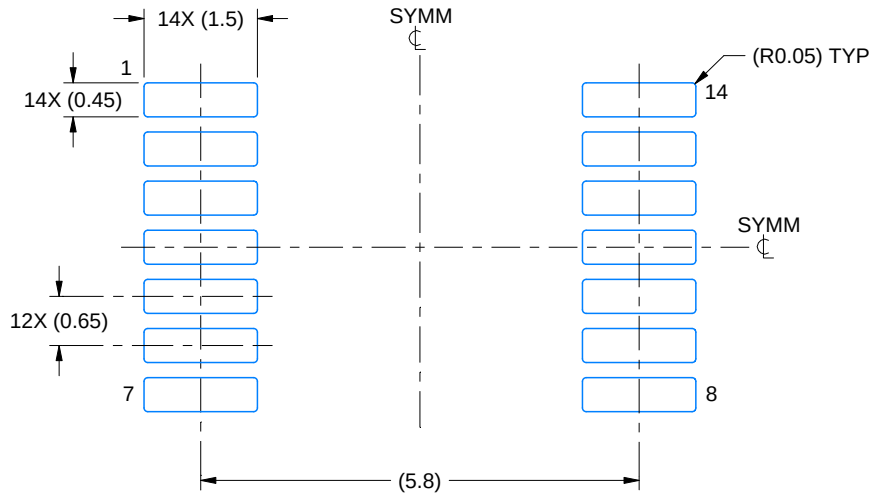
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

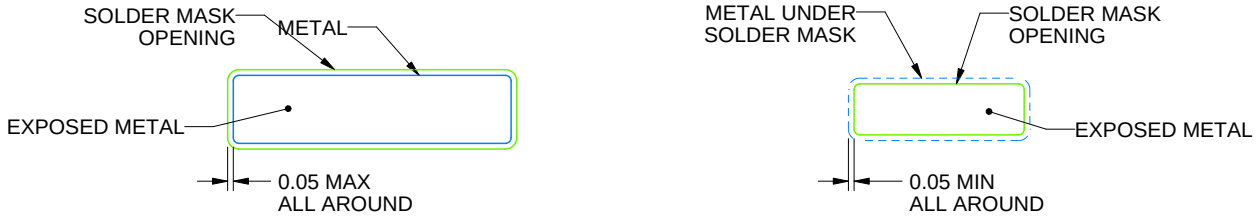


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

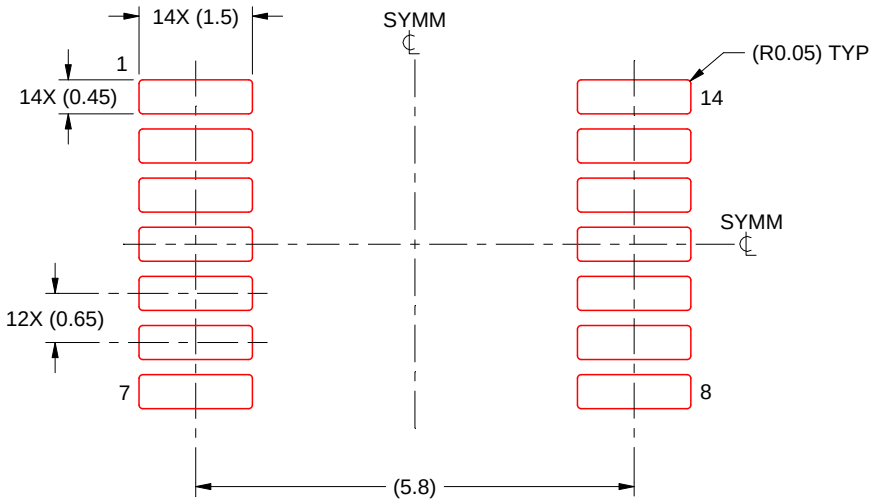


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月