参考資料

Texas Instruments

MUX50x 低容量、低リーク電流、36V高精度アナログ・マルチプレクサ

1 特長

- 低オン容量
  - MUX506: 13.5pF
  - MUX507: 8.7pF
- 低入力リーク電流: 1pA
- 低電荷注入: 0.31pC
- レール・ツー・レール動作
- 幅広い電源電圧範囲: ±5V～±18V、10V～36V
- 低オン抵抗: 125Ω
- 遷移時間: 97ns
- ブレイク・ビフォー・メイクの切り替え動作
- V_{DD}に接続可能なENピン
- ロジック・レベル: 2V～V_{DD}
- 低い消費電流: 45µA
- ESD保護(HBM): 2000V
- 業界標準のTSSOP/SOICパッケージ

2 アプリケーション

- ファクトリ・オートメーションと産業用プロセス制御
- プログラマブル・ロジック・コントローラ（PLC）
- アナログ入力モジュール
- ATE試験装置
- デジタル・マルチメータ
- バッテリ・モニタリング・システム

3 概要

MUX506およびMUX507 (MUX50x)は、最新のCMOS (相補型金属酸化膜半導体)高精度アナログ・マルチプレクサ(MUX)です。MUX506は16:1シングルエンド・チャネル、MUX507は差動8:1またはデュアル8:1シングルエンド・チャネルを提供します。MUX506およびMUX507は、デュアル電源(±5V～±18V)でも単電源(10V～36V)でも正常に動作します。また、対称電源(V_{DD} = 12V、V_{SS} = –12Vなど)でも、非対称電源(V_{DD} = 12V、V_{SS} = –5Vなど)でも正常に動作します。すべてのデジタル入力は、TTL (トランジスタ・トランジスタ・ロジック)互換しきい値を備えており、有効電源電圧範囲内で動作するときにTTLおよびCMOS両方のロジック互換性を提供します。

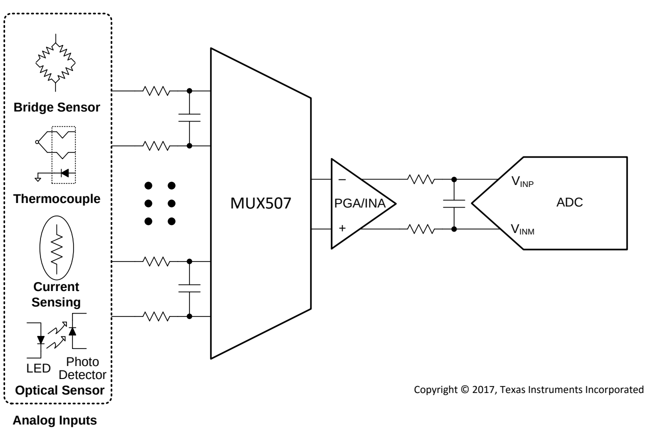
MUX506およびMUX507のオン/オフ・リーク電流は非常に低いため、入力インピーダンスの高い信号源からの信号を最小限の誤差でスイッチング可能です。45µAの低い消費電流により、低消費電力が重要なアプリケーションで使用できます。

製品情報(1)

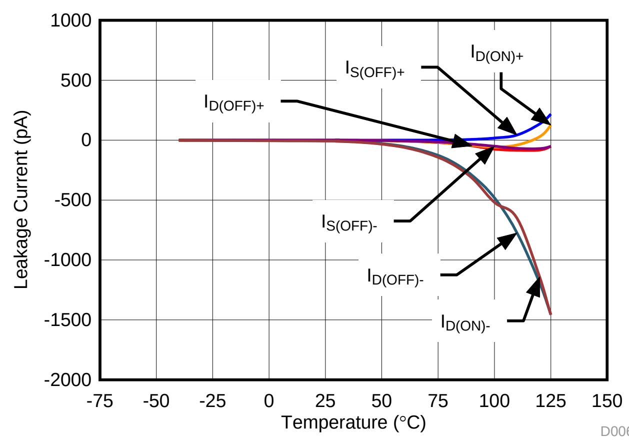
型番	パッケージ	本体サイズ(公称)
MUX506	TSSOP (28)	9.70mm×6.40mm
MUX507	SOIC (28)	17.9mm×7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

概略回路図



リーク電流と温度



English Data Sheet: SBAS803

目次

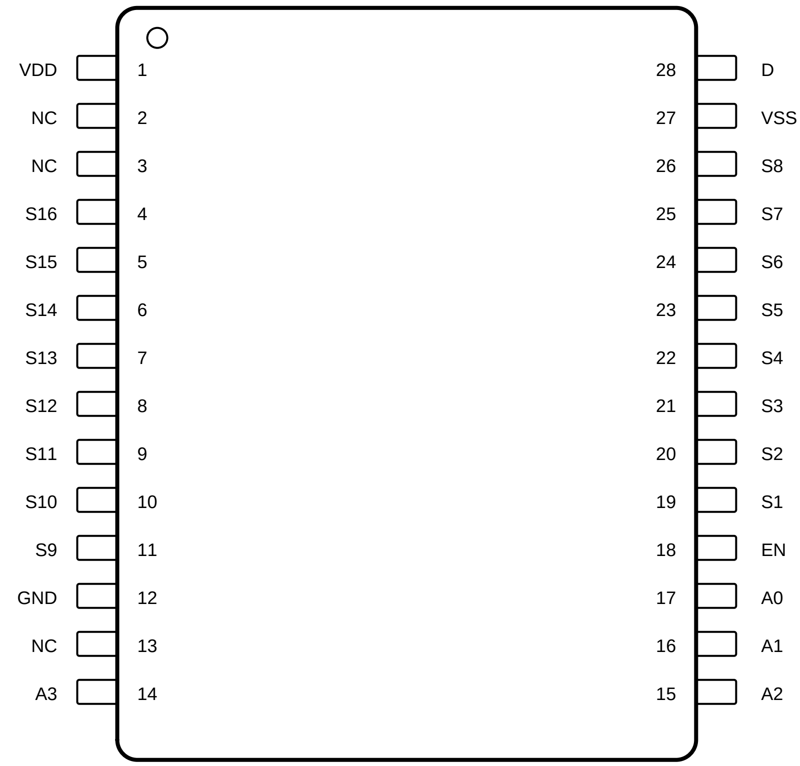
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年11月発行のものから更新	**Page**
• 「*特長*」一覧で遷移時間を85nsから97ns (標準値)に 変更	1
• 「*特長*」および「*製品情報*」にSOICパッケージを 追加	1
• Added the DW (SOIC) package to the *Pin Configuration and Functions* section	3
• Added SOIC package to the *Thermal Information* table	7
• Changed Transition time Typ value From 85: ns To: 97ns for ±15 V supplies in the *Electrical Characteristics: Dual Supply* table	8
• Added additional specifications for the SOIC packages (Q_J, Off-isolation, and channel-to-channel crosstalk) for ±15 V supplies in *Electrical Characteristics: Dual Supply*	8
• Changed Transition time Typ value From: 91 To: 102 ns for 12 V supply in the *Electrical Characteristics: Single Supply* table	10
• Added additional specifications for the SOIC packages (Q_J, Off-isolation, and channel-to-channel crosstalk) for 12 V supply in *Electrical Characteristics: Single Supply*	10
• Added NOTE to the *Application and Implementation* section	28

5 Pin Configuration and Functions

MUX506: PW and DW Packages
28-Pin TSSOP and SOIC
Top View



Not to scale

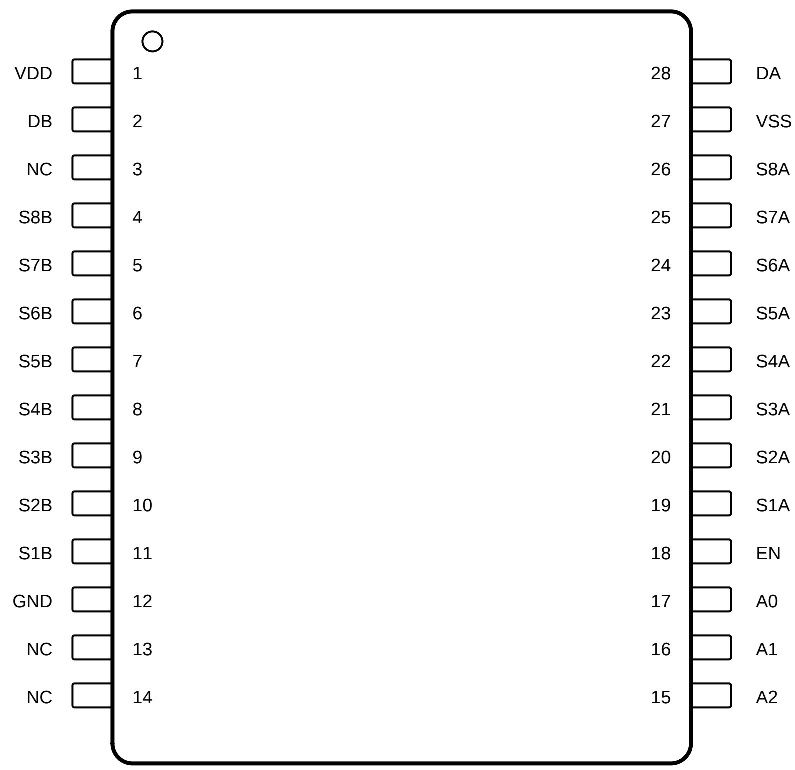
Pin Functions: MUX506

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
A0	17	Digital input	Address line 0
A1	16	Digital input	Address line 1
A2	15	Digital input	Address line 2
A3	14	Digital input	Address line 3
D	28	Analog input or output	Drain pin. Can be an input or output.
EN	18	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[3:0] logic inputs determine which switch is turned on.
GND	12	Power supply	Ground (0 V) reference
NC	2, 3, 13	No connect	Do not connect
S1	19	Analog input or output	Source pin 1. Can be an input or output.
S2	20	Analog input or output	Source pin 2. Can be an input or output.
S3	21	Analog input or output	Source pin 3. Can be an input or output.
S4	22	Analog input or output	Source pin 4. Can be an input or output.
S5	23	Analog input or output	Source pin 5. Can be an input or output.
S6	24	Analog input or output	Source pin 6. Can be an input or output.
S7	25	Analog input or output	Source pin 7. Can be an input or output.
S8	26	Analog input or output	Source pin 8. Can be an input or output.
S9	11	Analog input or output	Source pin 9. Can be an input or output.

Pin Functions: MUX506 (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
S10	10	Analog input or output	Source pin 10. Can be an input or output.
S11	9	Analog input or output	Source pin 11. Can be an input or output.
S12	8	Analog input or output	Source pin 12. Can be an input or output.
S13	7	Analog input or output	Source pin 13. Can be an input or output.
S14	6	Analog input or output	Source pin 14. Can be an input or output.
S15	5	Analog input or output	Source pin 15. Can be an input or output.
S16	4	Analog input or output	Source pin 16. Can be an input or output.
VDD	1	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	27	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND.

MUX507: PW and DW Package
28-Pin TSSOP and SOIC
Top View



Not to scale

Pin Functions: MUX507

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
A0	17	Digital input	Address line 0
A1	16	Digital input	Address line 1
A2	15	Digital input	Address line 2
DA	28	Analog input or output	Drain pin A. Can be an input or output.

Pin Functions: MUX507 (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
DB	2	Analog input or output	Drain pin B. Can be an input or output.
EN	18	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which pair of switches is turned on.
GND	12	Power supply	Ground (0 V) reference
NC	3, 13, 14	No connect	Do not connect
S1A	19	Analog input or output	Source pin 1A. Can be an input or output.
S2A	20	Analog input or output	Source pin 2A. Can be an input or output.
S3A	21	Analog input or output	Source pin 3A. Can be an input or output.
S4A	22	Analog input or output	Source pin 4A. Can be an input or output.
S5A	23	Analog input or output	Source pin 5A. Can be an input or output.
S6A	24	Analog input or output	Source pin 6A. Can be an input or output.
S7A	25	Analog input or output	Source pin 7A. Can be an input or output.
S8A	26	Analog input or output	Source pin 8A. Can be an input or output.
S1B	11	Analog input or output	Source pin 1B. Can be an input or output.
S2B	10	Analog input or output	Source pin 2B. Can be an input or output.
S3B	9	Analog input or output	Source pin 3B. Can be an input or output.
S4B	8	Analog input or output	Source pin 4B. Can be an input or output.
S5B	7	Analog input or output	Source pin 5B. Can be an input or output.
S6B	6	Analog input or output	Source pin 6B. Can be an input or output.
S7B	5	Analog input or output	Source pin 7B. Can be an input or output.
S8B	4	Analog input or output	Source pin 8B. Can be an input or output.
VDD	1	Power supply	Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	27	Power supply	Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply	V_{DD}	–0.3	40	V
		V_{SS}	–40	0.3	
		$V_{DD} – V_{SS}$		40	
	Digital pins(2): EN, A0, A1, A2, A3		V_{SS} – 0.3	V_{DD} + 0.3	
	Analog pins(2): Sx, SxA, SxB, D, DA, DB		V_{SS} – 2	V_{DD} + 2	
Current(3)			–30	30	mA
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage limits are valid if current is limited to ±30 mA.
(3) Only one pin at a time.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}(1)	Positive power-supply voltage	Dual supply	5		18	V
		Single supply	10		36	
V_{SS}(2)	Negative power-supply voltage (dual supply)		–5		–18	V
$V_{DD} – V_{SS}$	Supply voltage		10		36	V
V_S	Source pins voltage(3)		V_{SS}		V_{DD}	V
V_D	Drain pins voltage		V_{SS}		V_{DD}	V
V_{EN}	Enable pin voltage		V_{SS}		V_{DD}	V
V_A	Address pins voltage		V_{SS}		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)		–25		25	mA
T_A	Operating temperature		–40		125	°C

(1) When V_{SS} = 0 V, V_{DD} can range from 10 V to 36 V.
(2) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 36 V.
(3) V_S is the voltage on all the S pins.

6.4 Thermal Information

THERMAL METRIC(1)		MUX50x PW (TSSOP) 28 PINS	MUX50x DW (SOIC) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.8	53.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.0	30.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.6	28.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	9.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = –1 mA			125	170	Ω
		V_S = ±10 V, I_S = –1 mA			145	200	
			T_A = –40°C to +85°C			230	
			T_A = –40°C to +125°C			250	
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = –1 mA			6	9	Ω
			T_A = –40°C to +85°C			14	
			T_A = –40°C to +125°C			16	
R_{FLAT}	On-resistance flatness	V_S = 10 V, 0 V, –10 V			20	45	Ω
			T_A = –40°C to +85°C			53	
			T_A = –40°C to +125°C			58	
	On-resistance drift	V_S = 0 V			0.62		Ω/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V(1)		–1	–0.001	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–25		25	
$I_{D(OFF)}$	Output off-leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V(1)		–1	–0.01	1	nA
			T_A = -40°C to +85°C	–10		10	
			T_A = -40°C to +125°C	–25		25	
$I_{D(ON)}$	Output on-leakage current	Switch state is on, V_D = ±10 V, V_S = floating		–1	–0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–50		50	
LOGIC INPUT							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
I_D	Input current					0.1	µA

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics: Dual Supply (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SWITCH DYNAMICS(2)								
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF				82	136	ns
			T_A = –40°C to +85°C				145	
			T_A = –40°C to +125°C				151	
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF				63	78	ns
			T_A = –40°C to +85°C				89	
			T_A = –40°C to +125°C				97	
t_t	Transition time	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF,				97	143	ns
			T_A = –40°C to +85°C				151	
			T_A = –40°C to +125°C				157	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C			30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 0 V	TSSOP package		0.31		pC
				SOIC package		0.67		
			V_S = –15 V to +15 V	TSSOP package		±0.9		
				SOIC package		±1.1		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB	TSSOP package		–98		dB
				SOIC package		–94		
			Adjacent channel to D, DA, DB	TSSOP package		–94		
				SOIC package		–88		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels	TSSOP package		–100		dB
				SOIC package		–96		
			Adjacent channels	TSSOP package		–88		
				SOIC package		–83		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V				2.1	3	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	MUX506			11.1	12.2	pF
			MUX507			6.4	7.5	
$C_{S(ON)}$, $C_{D(ON)}$	Output on-capacitance	f = 1 MHz, V_S = 0 V	MUX506			13.5	15	pF
			MUX507			8.7	10.2	
POWER SUPPLY								
	V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V,				45	59	µA
			T_A = –40°C to +85°C				62	
			T_A = –40°C to +125°C				85	
	V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V,				26	34	µA
			T_A = –40°C to +85°C				37	
			T_A = –40°C to +125°C				58	

(2) Specified by design; not subject to production testing.

6.6 Electrical Characteristics: Single Supply

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = –1 mA			235	340	Ω
			T_A = –40°C to +85°C			390	
			T_A = –40°C to +125°C			430	
ΔR_{ON}	On-resistance match	V_S = 10 V, I_S = –1 mA			7	20	Ω
			T_A = –40°C to +85°C			35	
			T_A = –40°C to +125°C			40	
	On-resistance drift	V_S = 10 V			1.07		Ω/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(1)		–1	0.001	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–25		25	
$I_{D(OFF)}$	Output off leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(1)		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–25		25	
$I_{D(ON)}$	Output on leakage current	Switch state is on, V_D = 1 V and 10 V, V_S = floating		–1	0.02	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–50		50	
LOGIC INPUT							
V_{IH}	Logic voltage high			2.0			V
V_{IL}	Logic voltage low					0.8	V
I_D	Input current					0.1	µA

(1) When V_S is 1 V, V_D is 10 V, and vice versa.

Electrical Characteristics: Single Supply (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SWITCH DYNAMIC CHARACTERISTICS(2)								
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF				90	145	ns
			T_A = –40°C to +85°C				145	
			T_A = –40°C to +125°C				149	
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF				66	84	ns
			T_A = –40°C to +85°C				94	
			T_A = –40°C to +125°C				102	
t_t	Transition time	V_S = 8 V, C_L= 35 pF				107	147	ns
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF,	T_A = –40°C to +85°C				153	
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF,	T_A = –40°C to +125°C				155	
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C			30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 6 V	TSSOP package		0.12		pC
				SOIC package		0.38		
			V_S = 0 V to 12 V	TSSOP		±0.17		
				SOIC package		±0.48		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB	TSSOP package		–97		dB
				SOIC package		–94		
			Adjacent channel to D, DA, DB	TSSOP package		–94		
				SOIC package		–88		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels	TSSOP package		–100		dB
				SOIC package		–99		
			Adjacent channels	TSSOP		-88		
				SOIC package		-83		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V				2.4	3.4	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	MUX506			14	15.4	pF
			MUX507			7.8	9.1	
$C_{S(ON)}$, $C_{D(ON)}$	Output on-capacitance	f = 1 MHz, V_S = 6 V	MUX506			16.2	18	pF
			MUX507			9.9	11.6	
POWER SUPPLY								
	V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S= 0 V, V_{EN} = 3.3 V				41	59	µA
			T_A = –40°C to +85°C				62	
			T_A = –40°C to +125°C				83	
	V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V				22	34	µA
			T_A = –40°C to +85°C				37	
			T_A = –40°C to +125°C				57	

(2) Specified by design, not subject to production test.

6.7 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

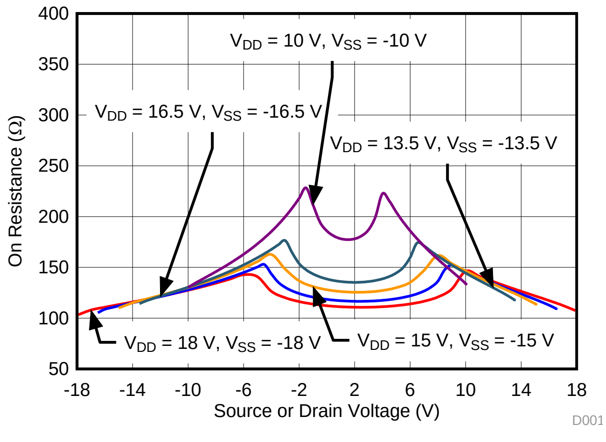


図 1. On-Resistance vs Source or Drain Voltage

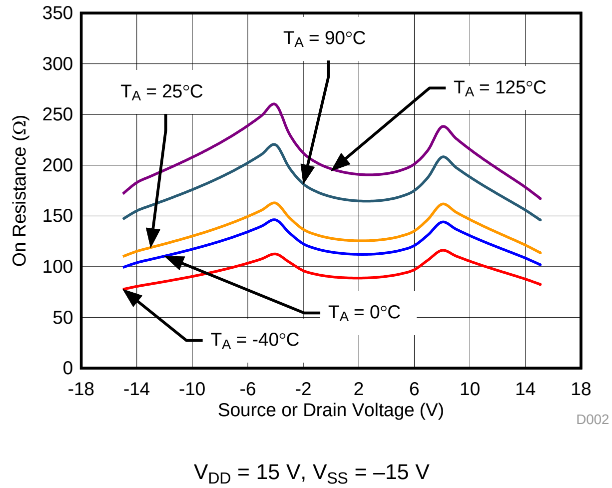


図 2. On-Resistance vs Source or Drain Voltage

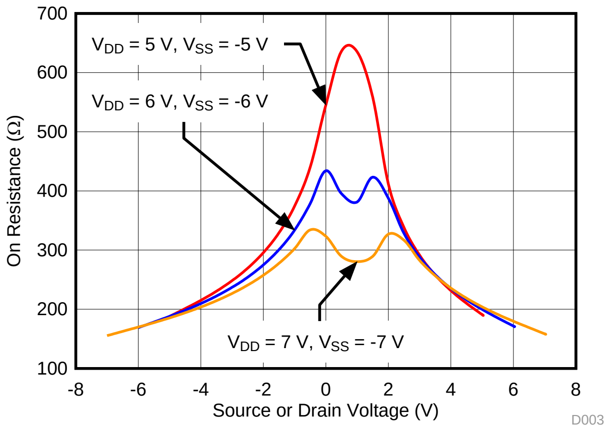


図 3. On-Resistance vs Source or Drain Voltage

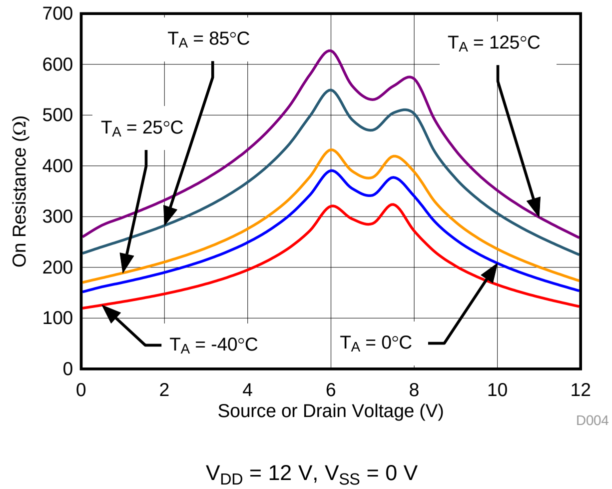


図 4. On-Resistance vs Source or Drain Voltage

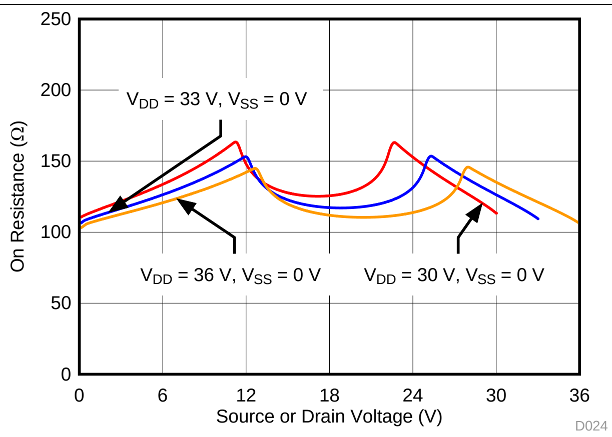


図 5. On-Resistance vs Source or Drain Voltage

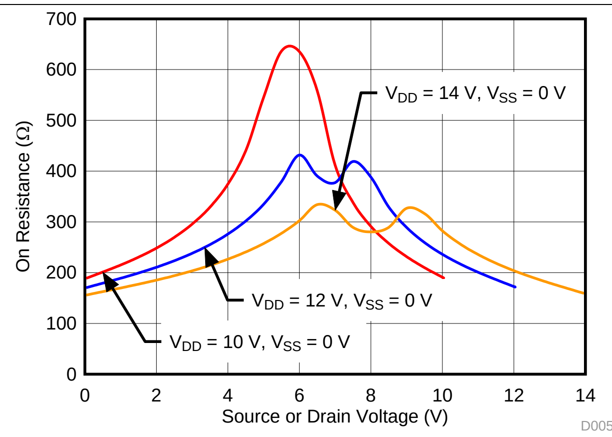
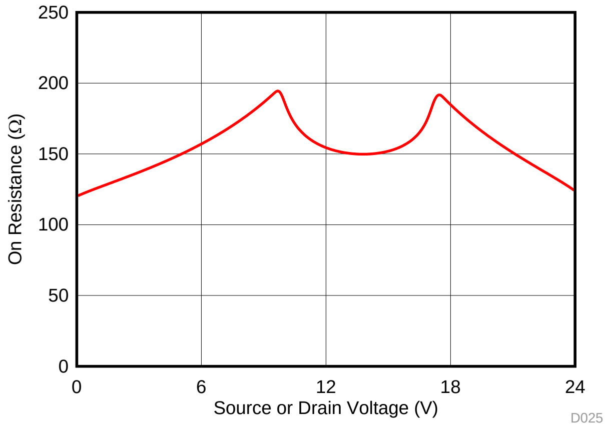


図 6. On-Resistance vs Source or Drain Voltage

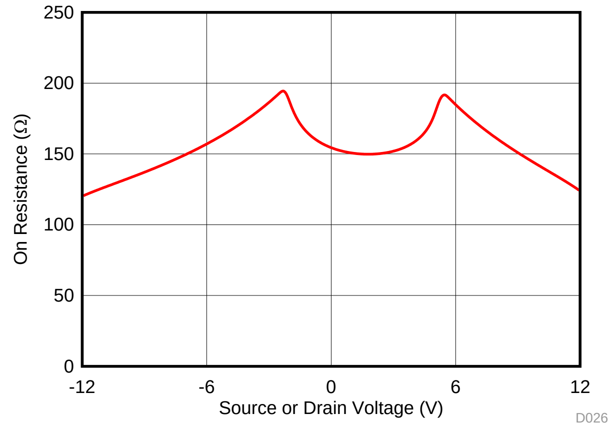
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



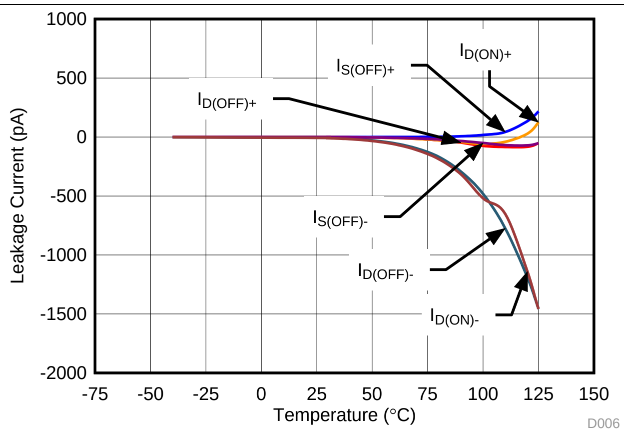
V_{DD} = 24 V, V_{SS} = 0 V

図 7. On-Resistance vs Source or Drain Voltage



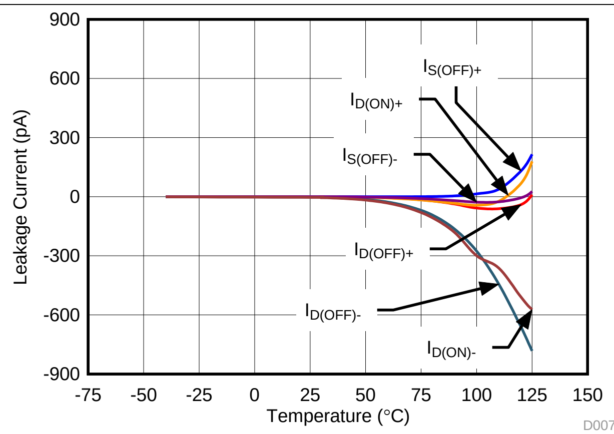
V_{DD} = 12 V, V_{SS} = –12 V

図 8. On-Resistance vs Source or Drain Voltage



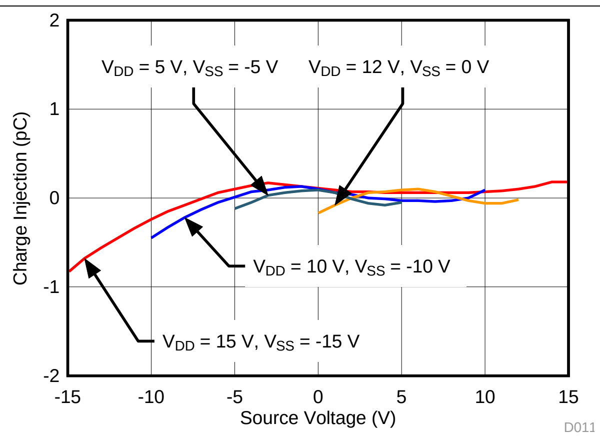
V_{DD} = 15 V, V_{SS} = –15 V

図 9. Leakage Current vs Temperature



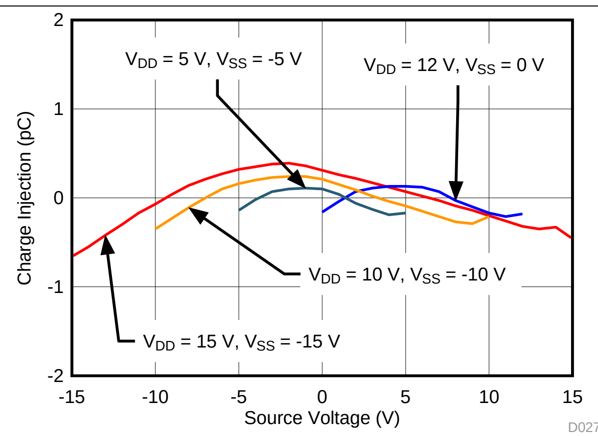
V_{DD} = 12 V, V_{SS} = 0 V

図 10. Leakage Current vs Temperature



MUX506, source-to-drain

図 11. Charge Injection vs Source Voltage



MUX507, source-to-drain

図 12. Charge Injection vs Source Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

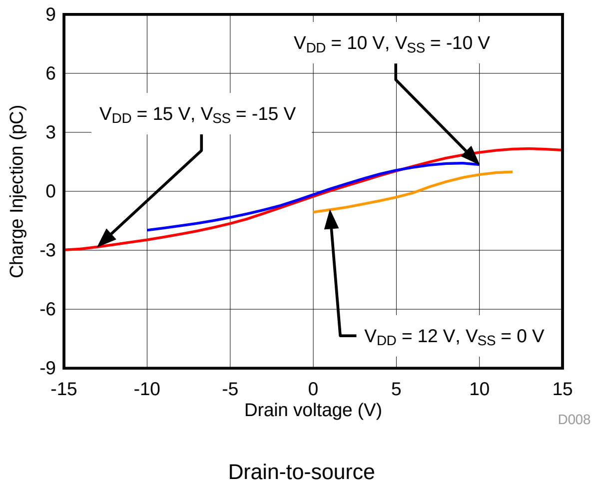


図 13. Charge Injection vs Drain Voltage

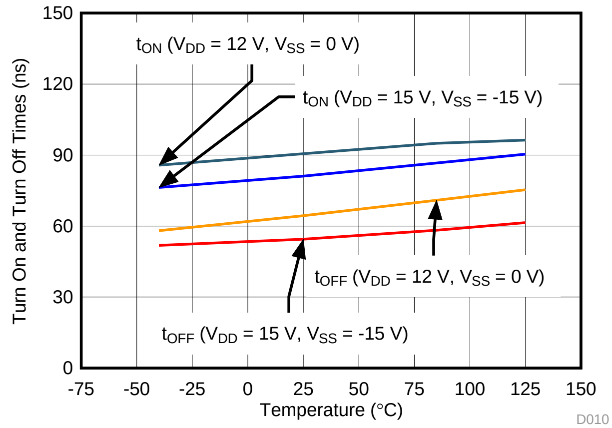


図 14. Turn-On and Turn-Off Times vs Temperature

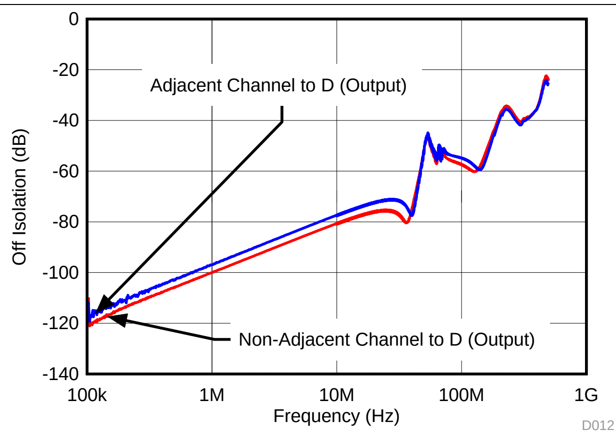


図 15. Off Isolation vs Frequency

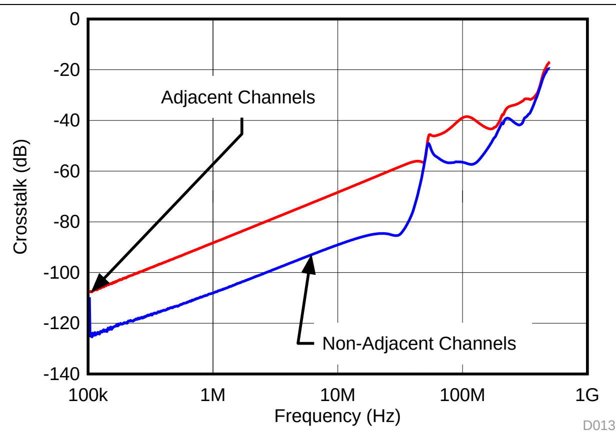


図 16. Crosstalk vs Frequency

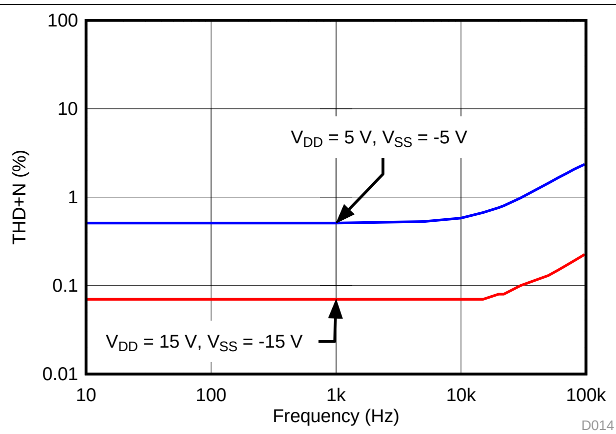


図 17. THD+N vs Frequency

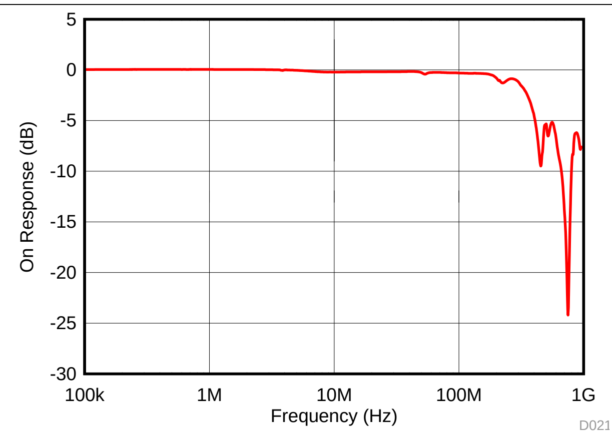
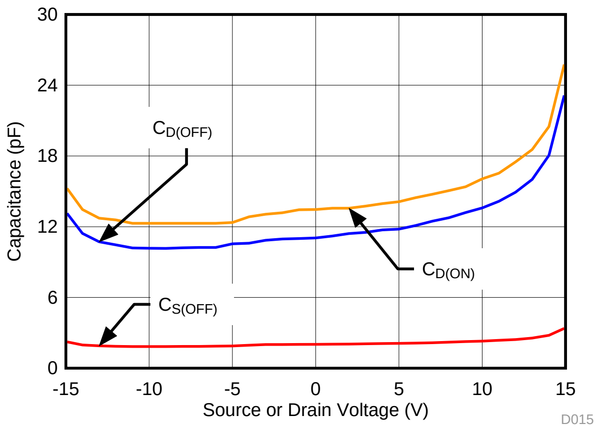


図 18. On Response vs Frequency

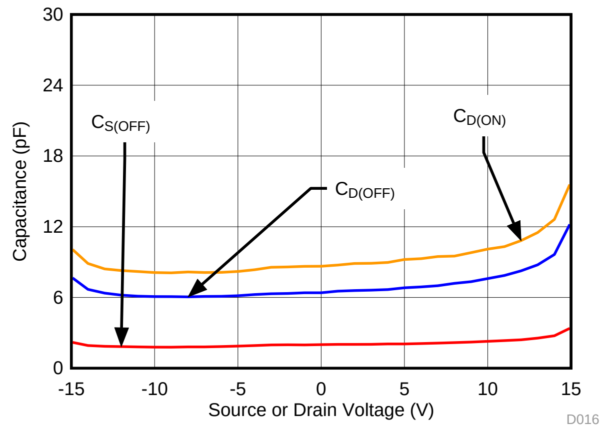
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



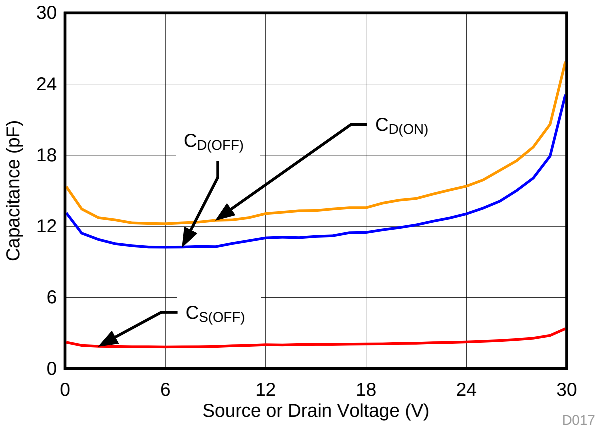
MUX506, V_{DD} = 15 V, V_{SS} = –15 V

図 19. Capacitance vs Source Voltage



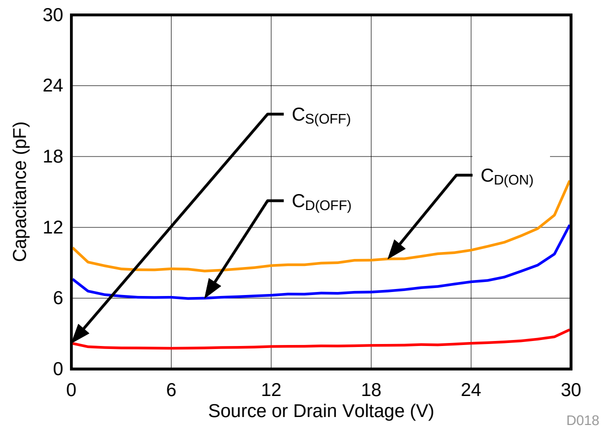
MUX507, V_{DD} = 15 V, V_{SS} = –15 V

図 20. Capacitance vs Source Voltage



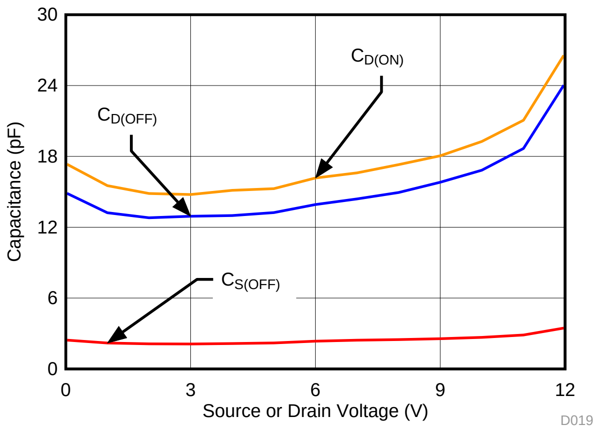
MUX506, V_{DD} = 30 V, V_{SS} = 0 V

図 21. Capacitance vs Source Voltage



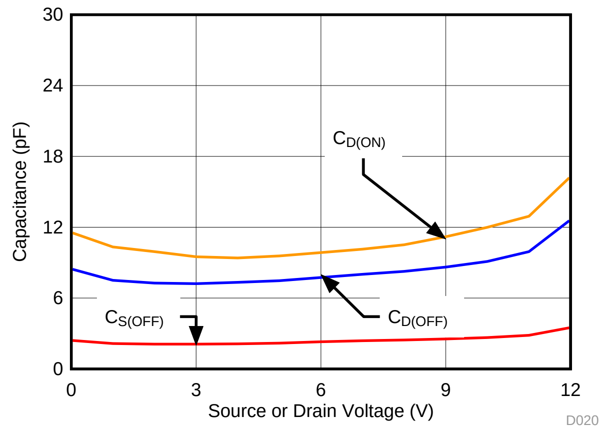
MUX507, V_{DD} = 30 V, V_{SS} = 0 V

図 22. Capacitance vs Source Voltage



MUX506, V_{DD} = 12 V, V_{SS} = 0 V

図 23. Capacitance vs Source Voltage



MUX507, V_{DD} = 12 V, V_{SS} = 0 V

図 24. Capacitance vs Source Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

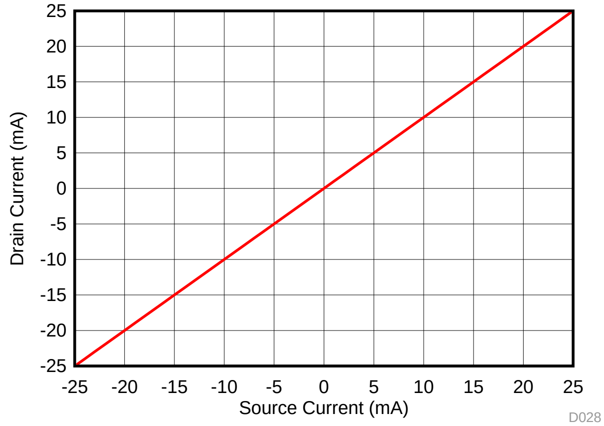


図 25. Source Current vs Drain Current

7 Parameter Measurement Information

7.1 Truth Tables

表 1. MUX506

EN	A3	A2	A1	A0	ON-CHANNEL
0	X(1)	X(1)	X(1)	X(1)	All channels are off
1	0	0	0	0	Channel 1
1	0	0	0	1	Channel 2
1	0	0	1	0	Channel 3
1	0	0	1	1	Channel 4
1	0	1	0	0	Channel 5
1	0	1	0	1	Channel 6
1	0	1	1	0	Channel 7
1	0	1	1	1	Channel 8
1	1	0	0	0	Channel 9
1	1	0	0	1	Channel 10
1	1	0	1	0	Channel 11
1	1	0	1	1	Channel 12
1	1	1	0	0	Channel 13
1	1	1	0	1	Channel 14
1	1	1	1	0	Channel 15
1	1	1	1	1	Channel 16

(1) X denotes *don't care*..

表 2. MUX507

EN	A2	A1	A0	ON-CHANNEL
0	X(1)	X(1)	X(1)	All channels are off
1	0	0	0	Channels 1A and 1B
1	0	0	1	Channels 2A and 2B
1	0	1	0	Channels 3A and 3B
1	0	1	1	Channels 4A and 4B
1	1	0	0	Channels 5A and 5B
1	1	0	1	Channels 6A and 6B
1	1	1	0	Channels 7A and 7B
1	1	1	1	Channels 8A and 8B

(1) X denotes *don't care*.

7.2 On-Resistance

The on-resistance of the MUX50x is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 26. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 式 1:

$$R_{ON} = V / I_{CH} \quad (1)$$

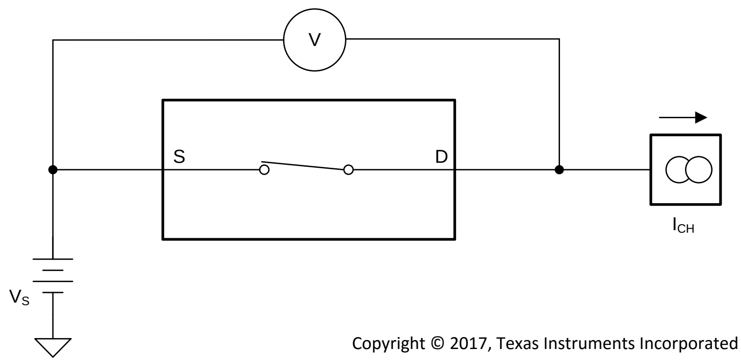


図 26. On-Resistance Measurement Setup

7.3 Off Leakage

There are two types of leakage currents associated with a switch during the OFF state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 図 27

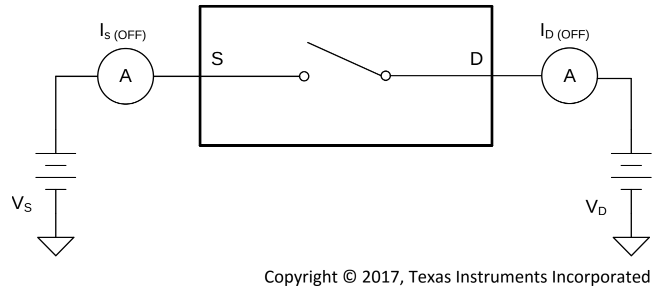


図 27. Off-Leakage Measurement Setup

7.4 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the ON state. The source pin is left floating during the measurement. 図 28 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

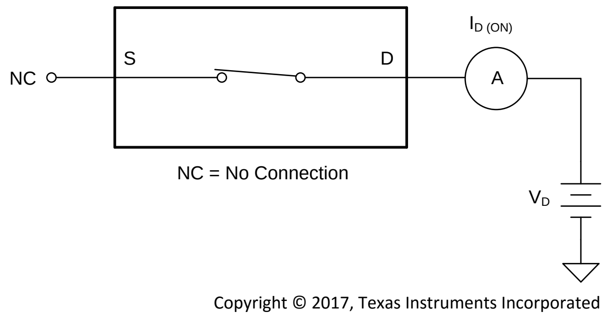


図 28. On-Leakage Measurement Setup

7.5 Transition Time

Transition time is defined as the time taken by the output of the MUX50x to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. 図 29 shows the setup used to measure transition time, denoted by the symbol t_t.

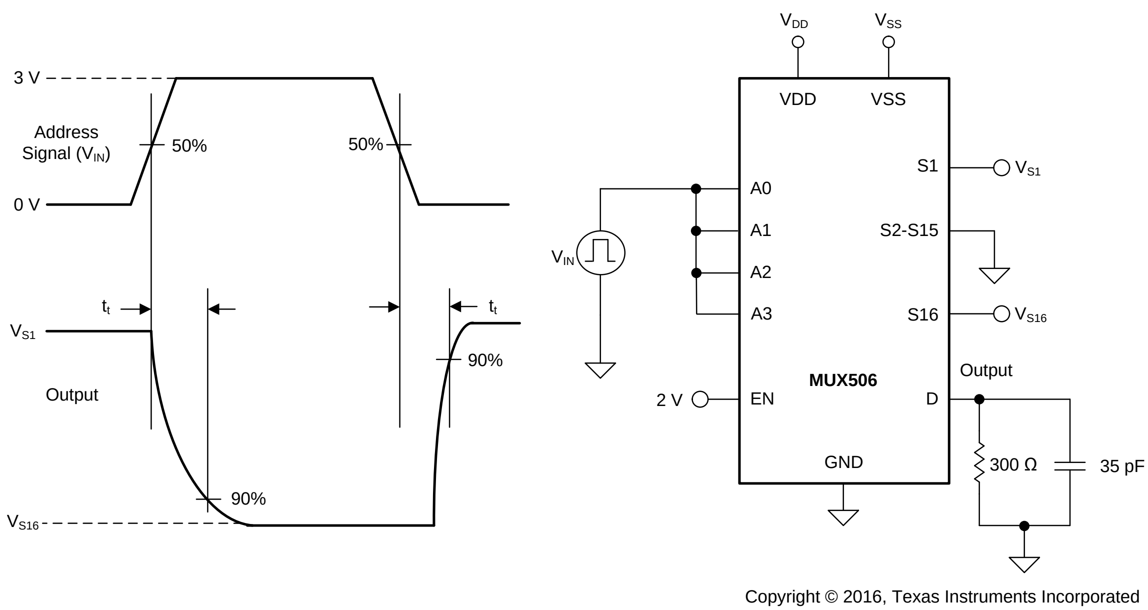


図 29. Transition-Time Measurement Setup

7.6 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the MUX50x is switching. The MUX50x output first breaks from the ON-state switch before making the connection with the next ON-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 30 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

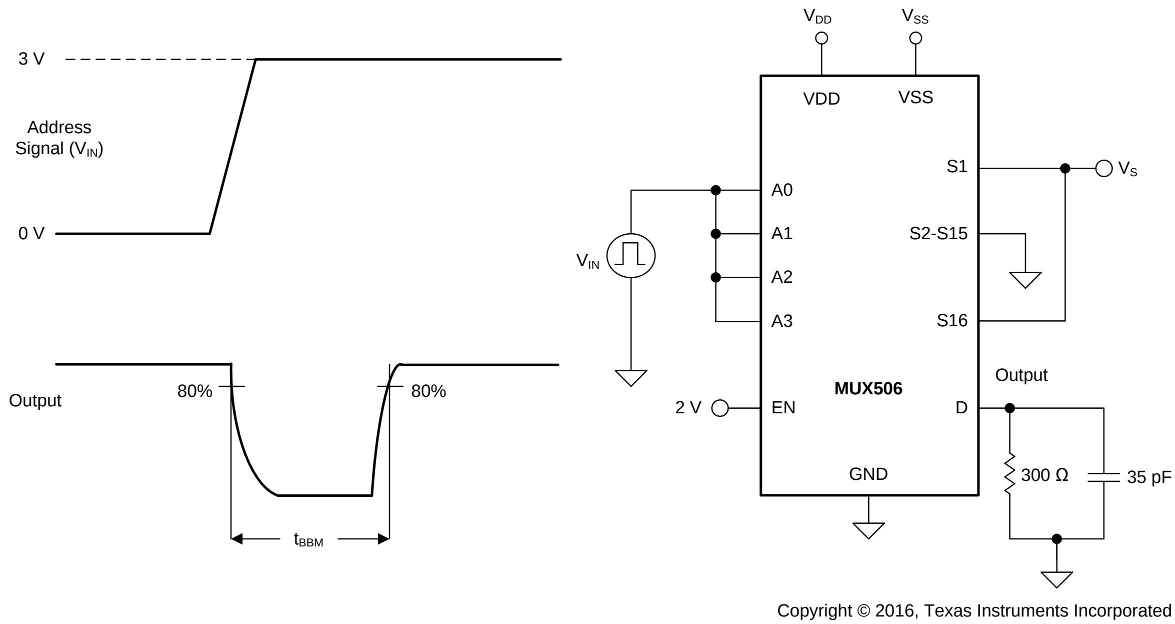


図 30. Break-Before-Make Delay Measurement Setup

7.7 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the MUX50x to rise to 90% final value after the enable signal has risen to 50% final value. 図 31 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn off time is defined as the time taken by the output of the MUX50x to fall to 10% initial value after the enable signal has fallen to 50% initial value. 図 31 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

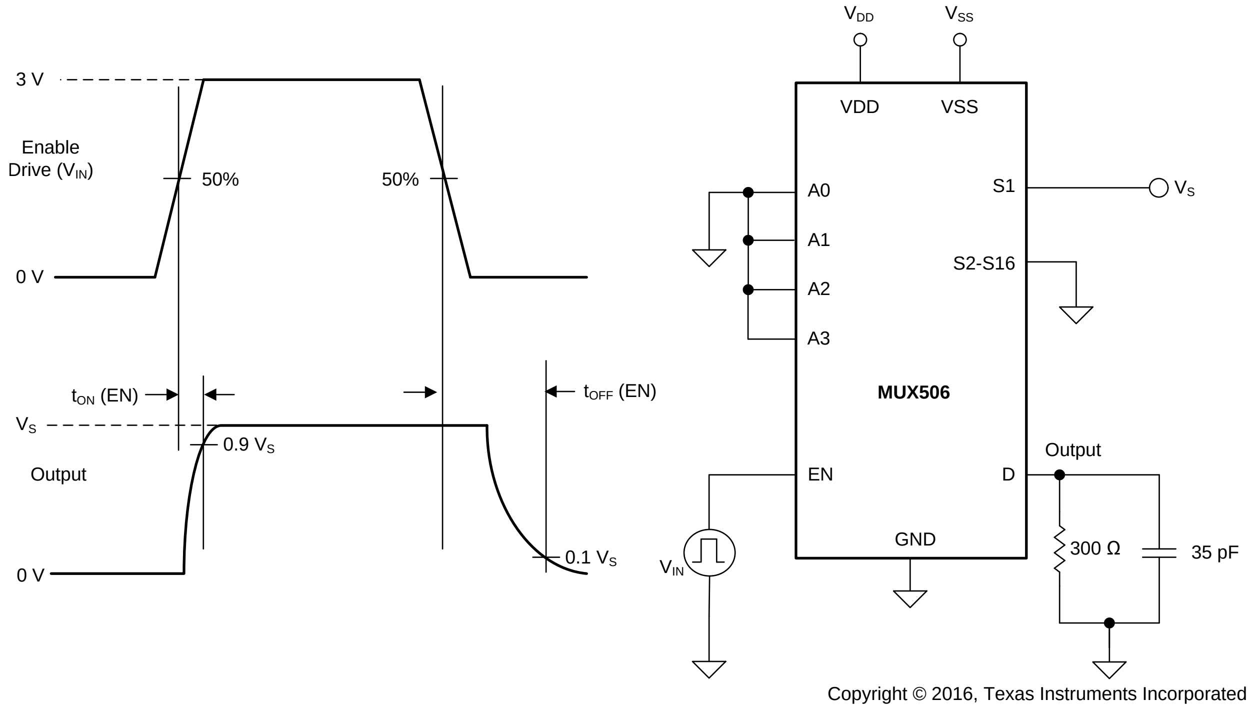


図 31. Turn-On and Turn-Off Time Measurement Setup

7.8 Charge Injection

The MUX50x have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 32 shows the setup used to measure charge injection.

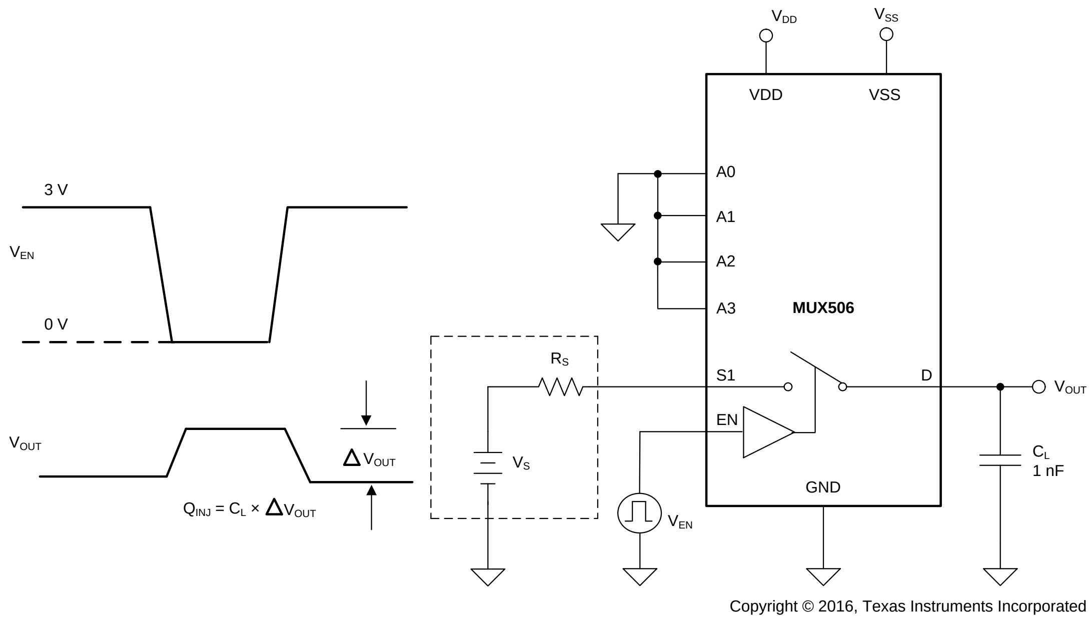


図 32. Charge-Injection Measurement Setup

7.9 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the MUX50x when a 1-V_{RMS} signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. 図 33 shows the setup used to measure off isolation. Use 式 2 to compute off isolation.

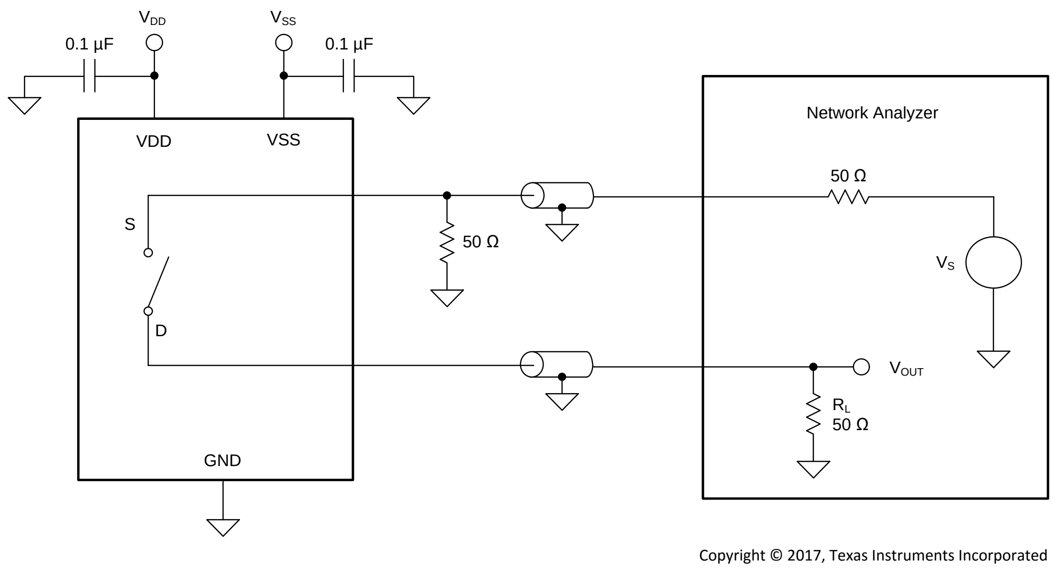


図 33. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$

7.10 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. 図 34 shows the setup used to measure channel-to-channel crosstalk. Use 式 3 to compute, channel-to-channel crosstalk.

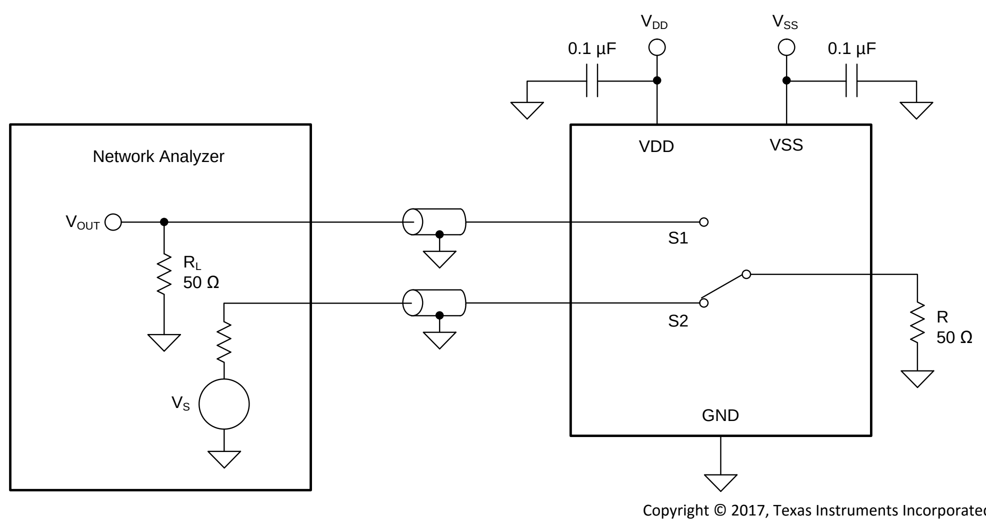


図 34. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{3}$$

7.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin of an on-channel, and the output measured at the drain pin of the MUX50x. 図 35 shows the setup used to measure bandwidth of the mux. Use 式 4 to compute the attenuation.

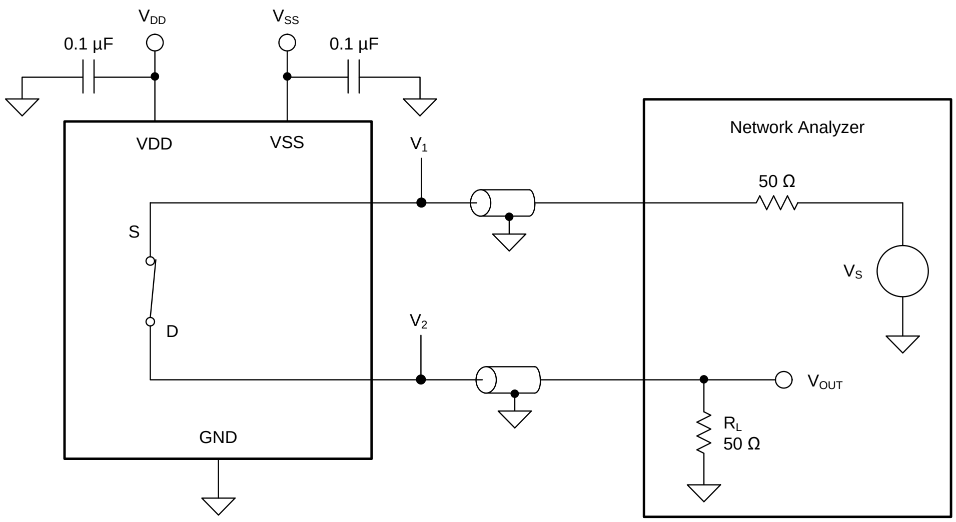


図 35. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{4}$$

7.12 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the MUX50x varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 図 36 shows the setup used to measure THD+N of the MUX50x.

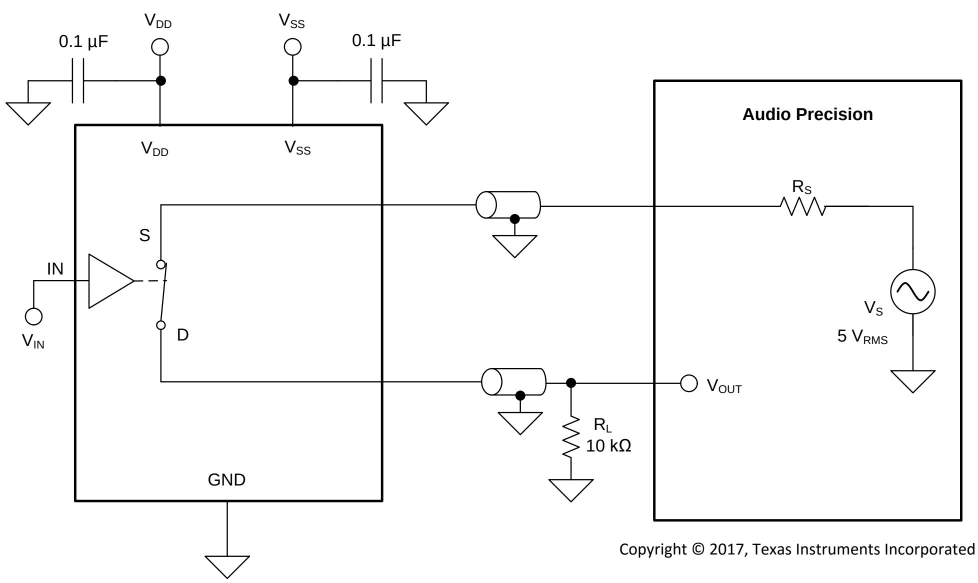


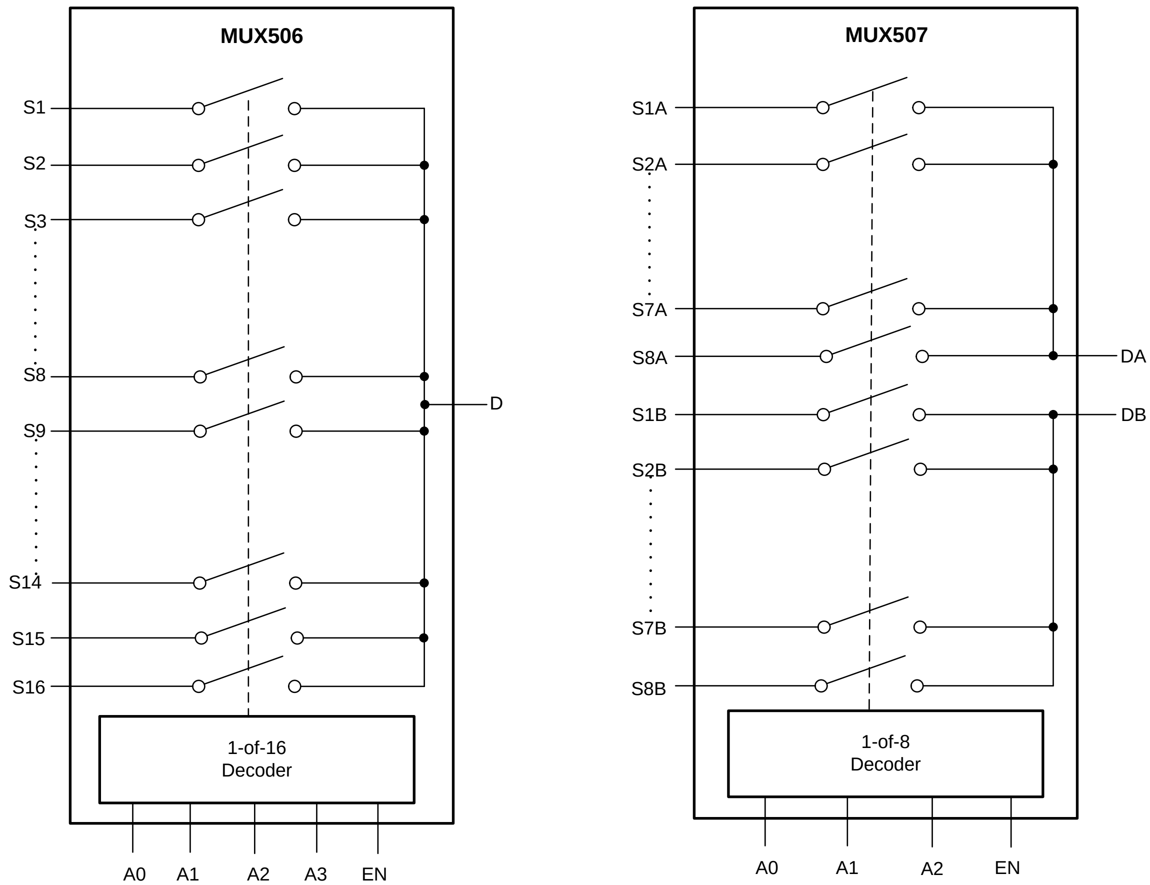
図 36. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The MUX50x are a family of analog multiplexers. The *Functional Block Diagram* section provides a top-level block diagram of both the MUX506 and MUX507. The MUX506 is a 16-channel, single-ended, analog mux. The MUX507 is an 8-channel, differential or dual 8:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Ultralow Leakage Current

The MUX50x provide extremely low on- and off-leakage currents. The MUX50x are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 図 37 shows typical leakage currents of the MUX50x versus temperature.

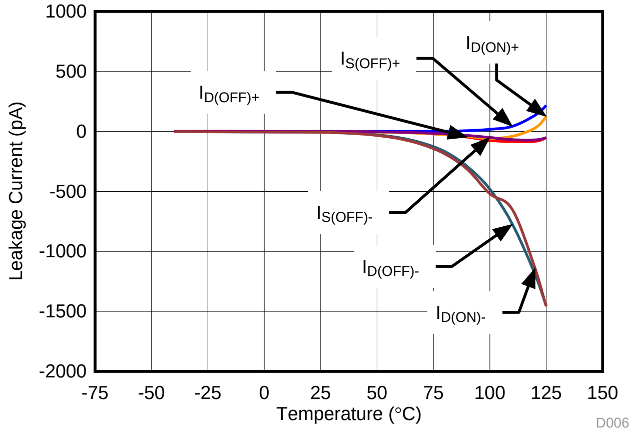


図 37. Leakage Current vs Temperature

8.3.2 Ultralow Charge Injection

The MUX50x have a simple transmission gate topology, as shown in 図 38. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

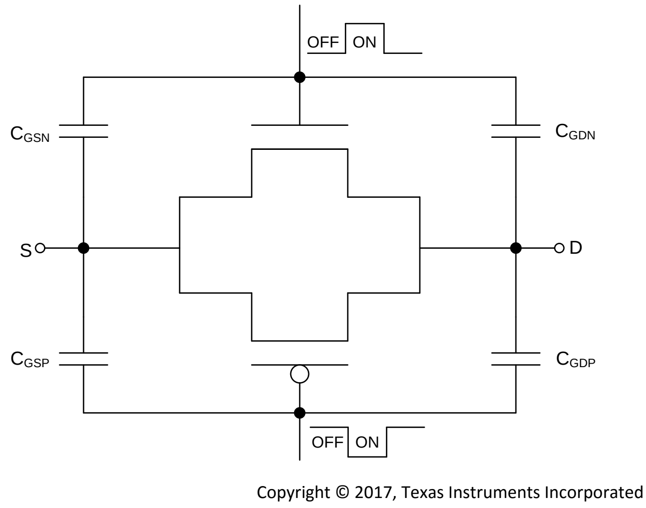


図 38. Transmission Gate Topology

Feature Description (continued)

The MUX50x have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 0.31 pC at V_S = 0 V, and ±0.9 pC in the full signal range, as shown in 図 39.

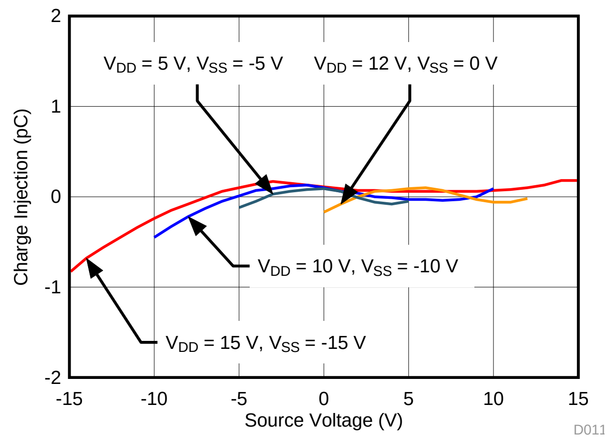


図 39. Source-to-Drain Charge Injection

The drain-to-source charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. 図 40 shows the drain-to-source charge injection across the full signal range.

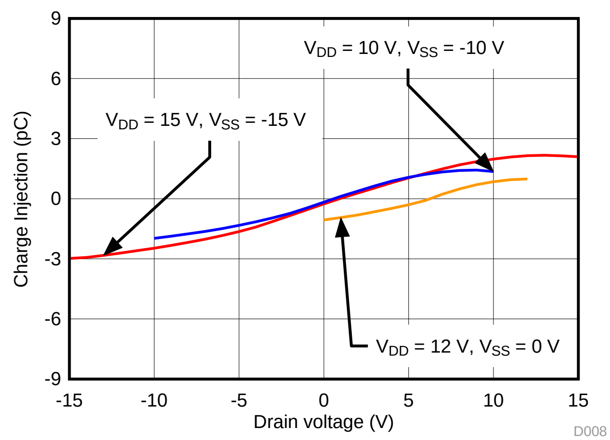


図 40. Drain-to-Source Charge Injection

Feature Description (continued)

8.3.3 Bidirectional Operation

The MUX50x are operable as both a mux and demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the MUX50x are used either as input or output. Each MUX50x channel has very similar characteristics in both directions.

8.3.4 Rail-to-Rail Operation

The valid analog signal for the MUX50x ranges from V_{SS} to V_{DD}. The input signal to the MUX50x swings from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of the MUX50x varies with input signal, as shown in 図 41

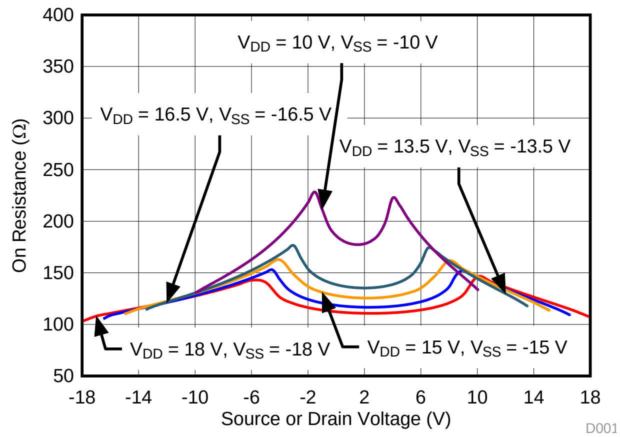


図 41. On-resistance vs Source or Drain Voltage

8.4 Device Functional Modes

When the EN pin of the MUX50x is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 36 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MUX50x family offers outstanding input/output leakage currents and ultra-low charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the MUX50x is very low. These features makes the MUX50x a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

図 42 shows a 16-bit, differential, 8-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential mux. This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the MUX507, OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

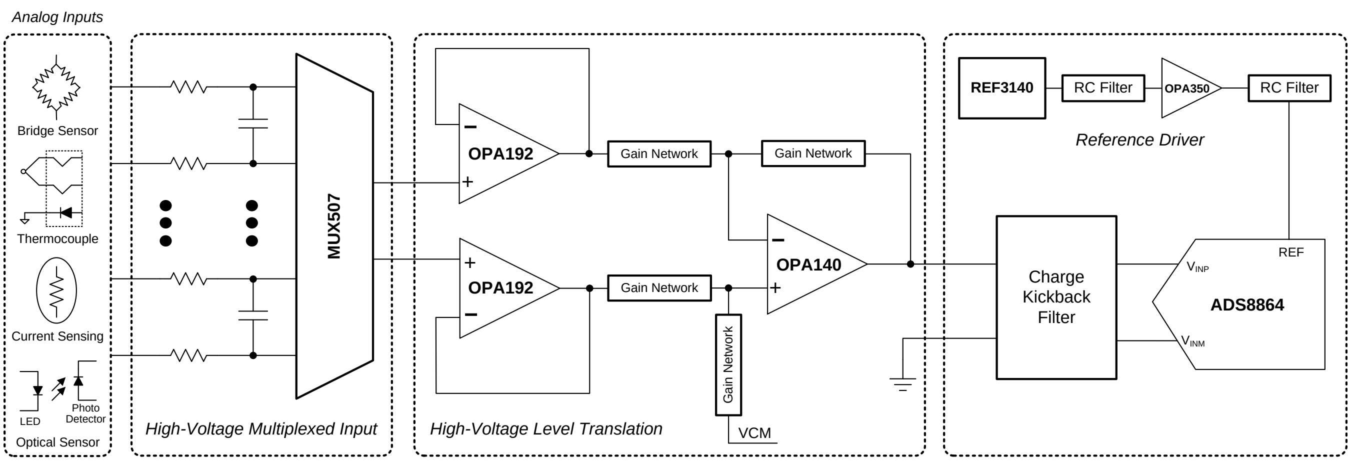


図 42. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

9.2.1 Design Requirements

The primary objective is to design a ±20 V, differential, 8-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 20 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in 図 42. The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. Detailed design considerations and component selection procedure can be found in the TI Precision Design TIPD151, *16-Bit, 400-kSPS, 4-Channel Multiplexed Data-Acquisition System for High-Voltage Inputs with Lowest Distortion*.

9.2.3 Application Curve

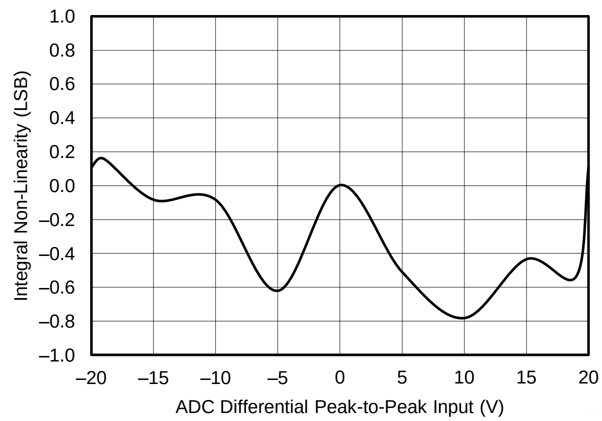


図 43. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

10 Power Supply Recommendations

The MUX50x operates across a wide supply range of ±5 V to ±18 V (10 V to 36 V in single-supply mode). The devices also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the VDD and VSS pins to ground.

The on-resistance of the MUX50x varies with supply voltage, as illustrated in 図 44

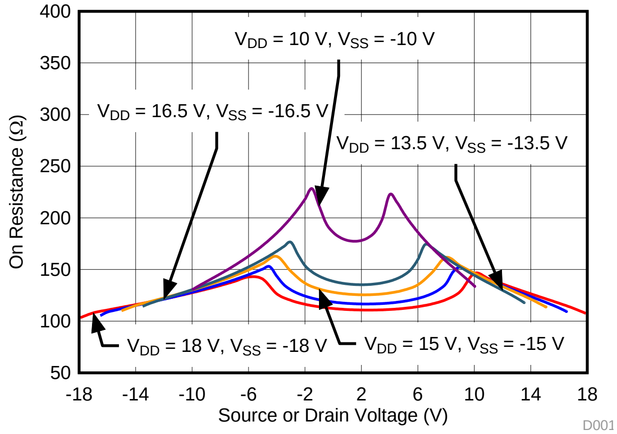


図 44. On-Resistance Variation With Supply and Input Voltage

11 Layout

11.1 Layout Guidelines

図 45 illustrates an example of a PCB layout with the MUX506IPW, and 図 46 illustrates an example of a PCB layout with MUX507IPW.

Some key considerations are:

1. Decouple the VDD and VSS pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

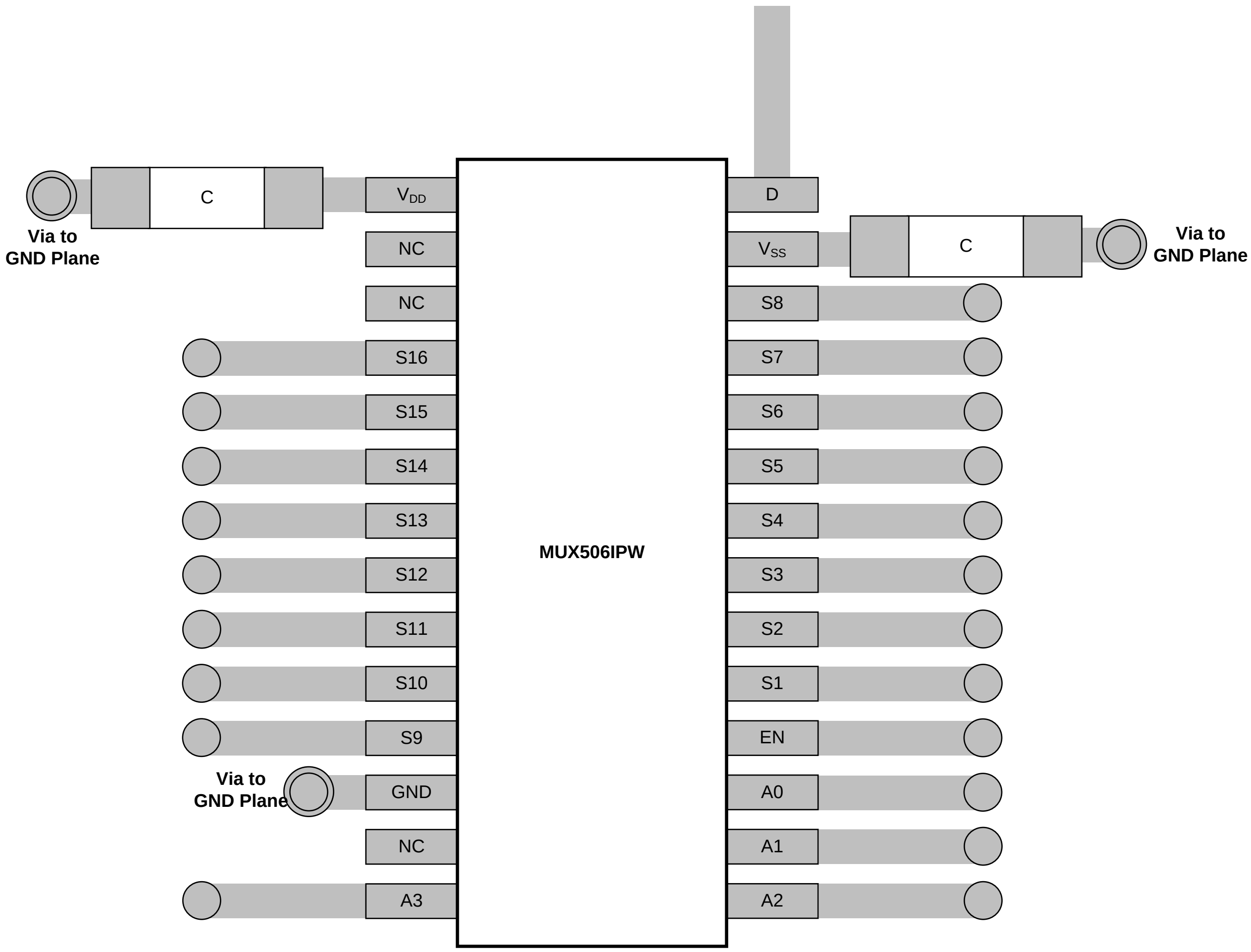


図 45. MUX506IPW Layout Example

Layout Example (continued)

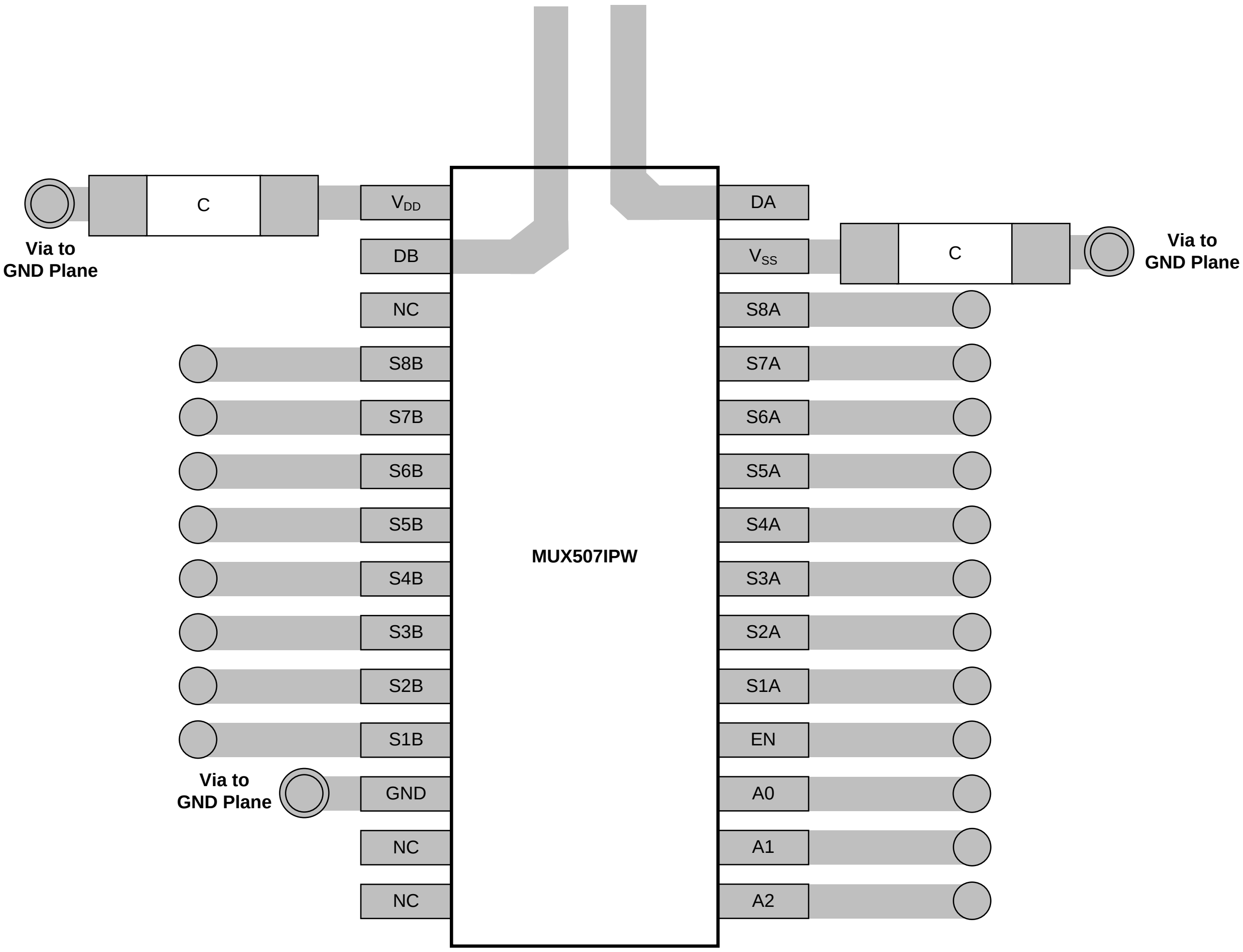


図 46. MUX507IPW Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『ADS8864 16ビット、400kSPS、シリアル・インターフェイス、microPower、小型、シングルエンド入力、SARアナログ・デジタル・コンバータ』* (SBAS572)
- *『OPAx192 36V、高精度、レール・ツー・レール入力/出力、低オフセット電圧、e-trim低入力バイアス電流オペアンプ』* (SBOS620)
- *『OPAx140高精度、低ノイズ、レール・ツー・レール出力、11MHz JFETオペアンプ』* (SBOS498)

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
MUX506	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MUX507	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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12.4 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MUX506IDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506DA
MUX506IDWR.B	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506DA
MUX506IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506A
MUX506IPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506A
MUX506IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506A
MUX506IPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506A
MUX506IPWRG4.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX506A
MUX507IDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507DA
MUX507IDWR.B	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507DA
MUX507IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507A
MUX507IPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507A
MUX507IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507A
MUX507IPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507A
MUX507IPWRG4.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MUX507A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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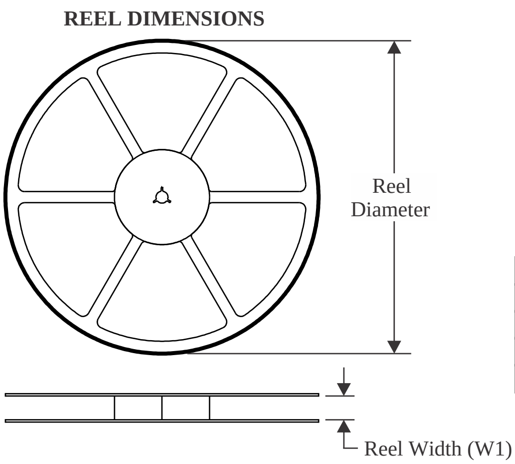
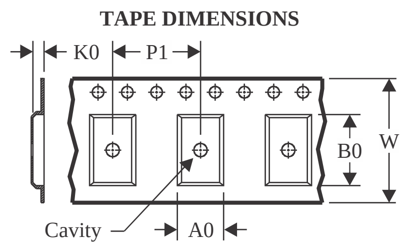
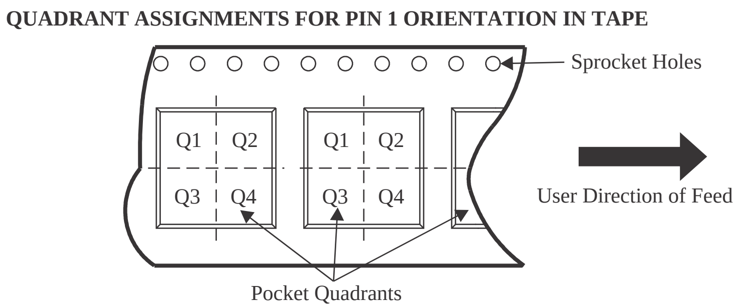
TAPE AND REEL INFORMATION





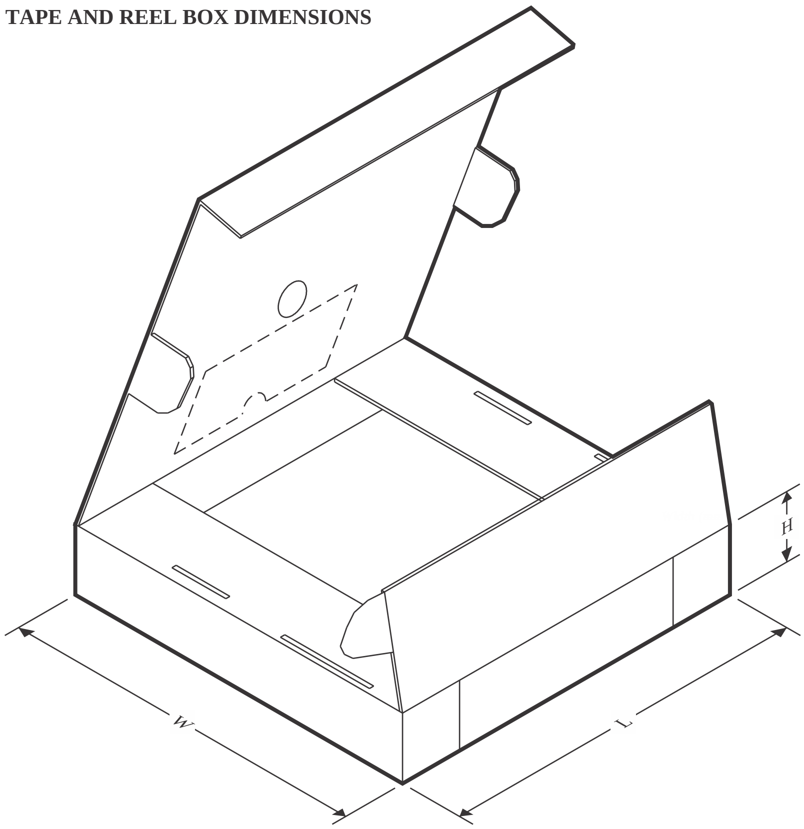
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MUX506IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MUX506IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MUX507IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MUX507IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

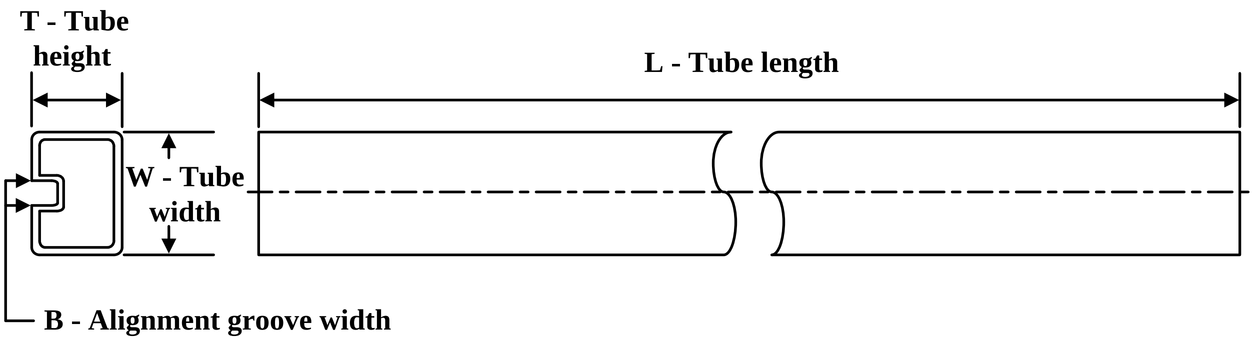
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MUX506IDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MUX506IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MUX507IDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MUX507IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0

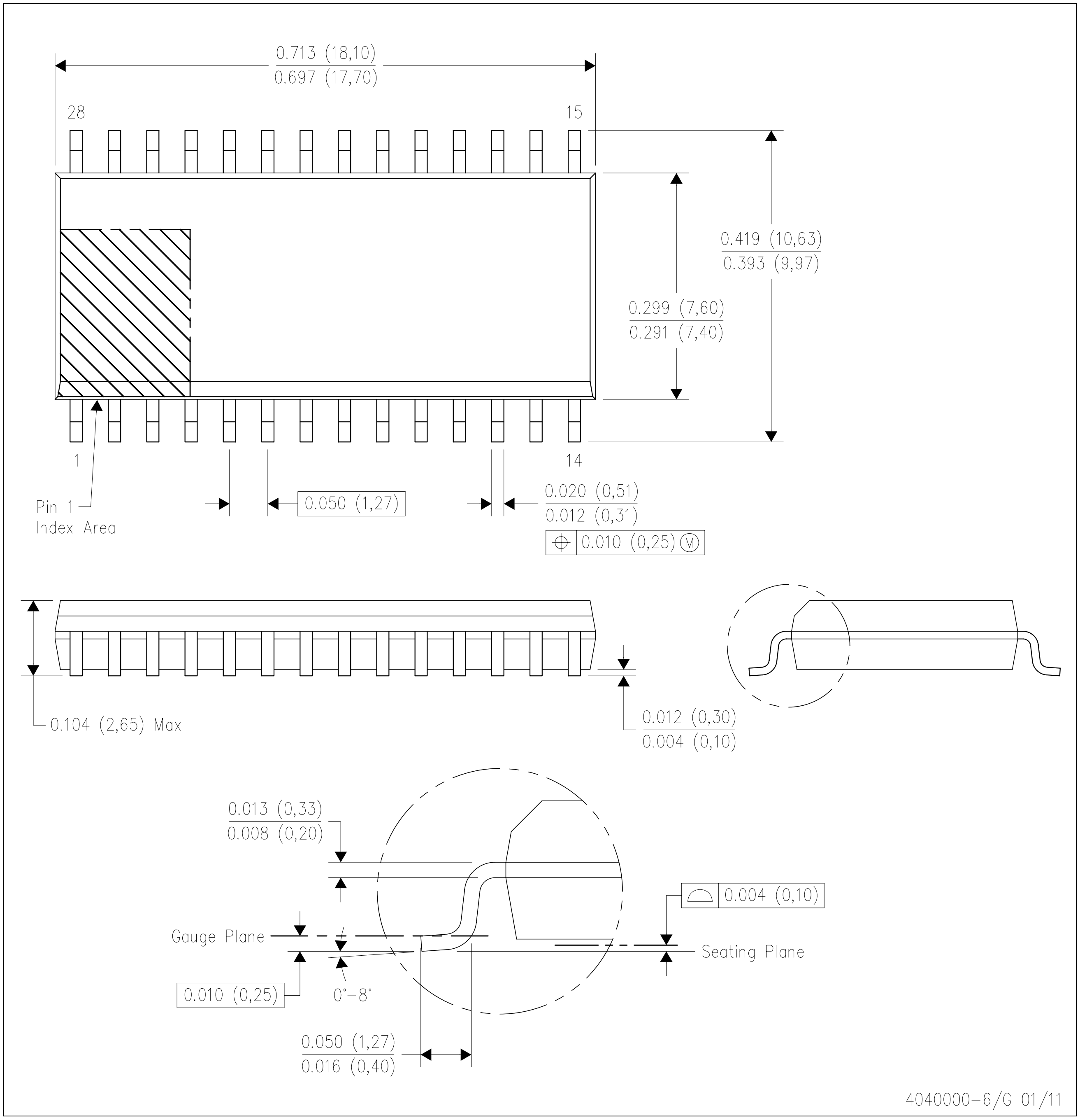
TUBE



*All dimensions are nominal

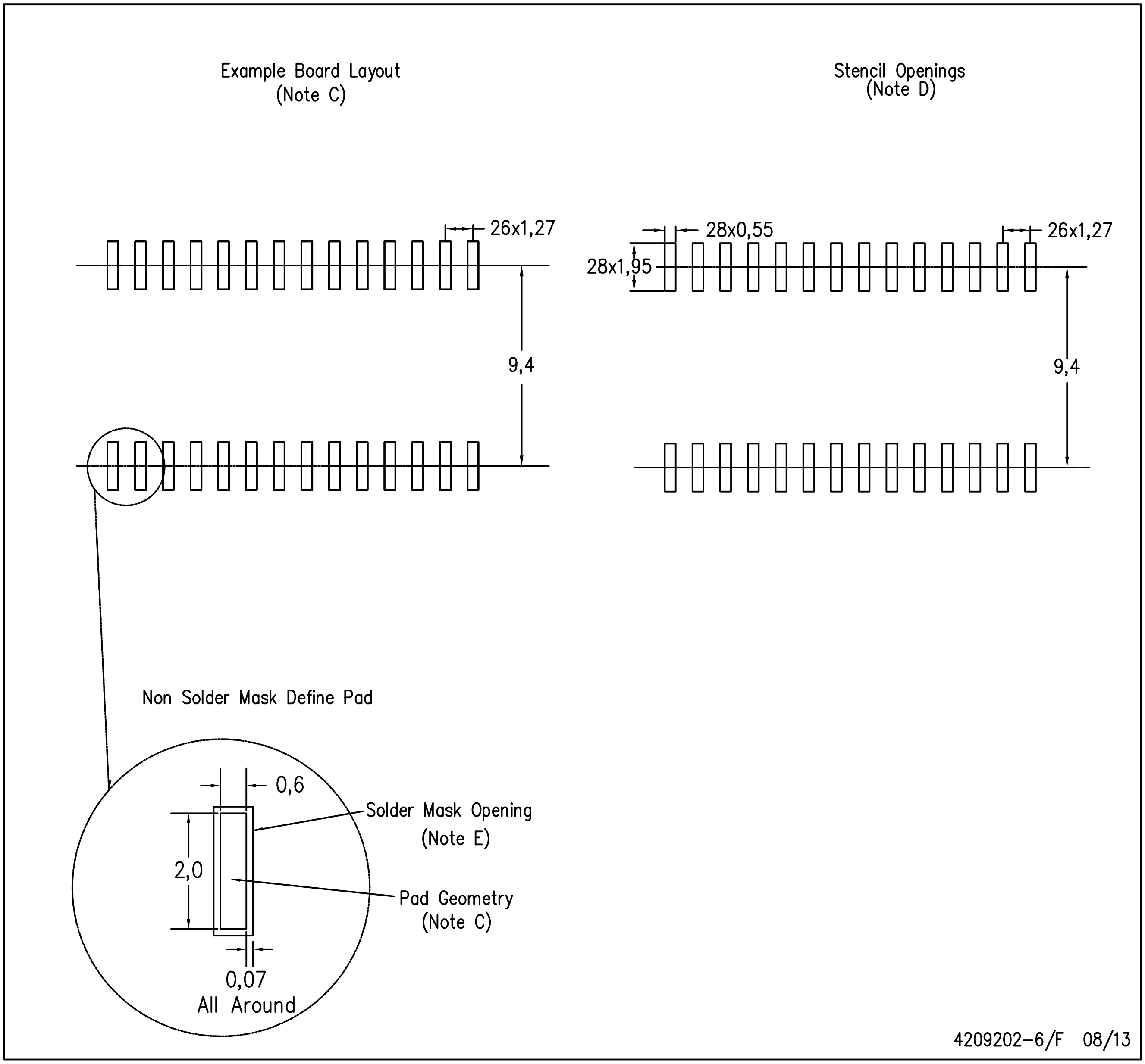
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MUX506IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MUX506IPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MUX507IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MUX507IPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



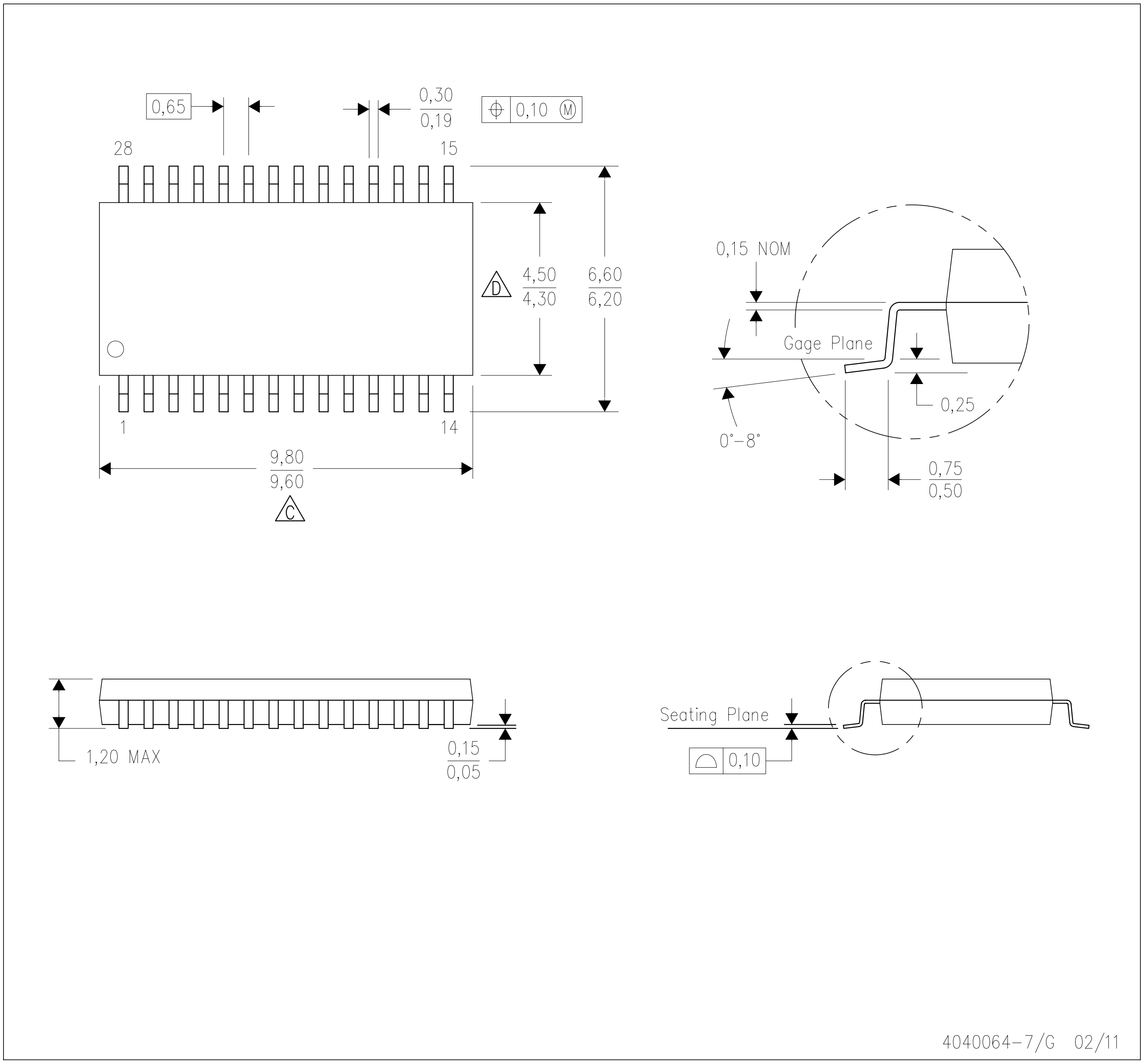
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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