MSP430FR697x(1)、MSP430FR692x(1) ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 組み込みマイクロコントローラ
  - 16ビットのRISCアーキテクチャ、最大16MHzのクロック
  - 3.6V～1.8Vの広い電源電圧範囲(最小電源電圧はSVSレベルにより制限されます。「SVS仕様」を参照)
- 最適化された超低消費電力モード
  - アクティブ・モード: 約100µA/MHz
  - スタンバイ(VLOありのLPM3): 0.4µA (標準値)
  - リアルタイム・クロック(RTC) (LPM3.5): 0.35µA (標準値) (1)
  - シャットダウン(LPM4.5): 0.02µA (標準値)
- 超低消費電力の強誘電体RAM (FRAM)
  - 最大128KBの不揮発性メモリ
  - 超低消費電力の書き込み
  - ワードあたり125nsの高速書き込み(4msで64KB)
  - ユニファイド・メモリによりプログラム、データ、ストレージを1か所に保存
  - 10^{15}回の書き込み耐久性
  - 放射耐性および非磁性
- インテリジェントなデジタル・ペリフェラル
  - 32ビットのハードウェア・マルチプライヤ(MPY)
  - 3チャネルの内蔵ダイレクト・メモリ・アクセス(DMA)
  - カレンダーおよびアラーム機能を持つRTC
  - 5つの16ビット・タイマ、それぞれに最大7つのキャプチャ/比較レジスタを搭載
  - 16ビットおよび32ビットの巡回冗長性検査(CRC16、CRC32)
- 高性能アナログ
  - 16チャネルのアナログ・コンパレータ
  - 12ビットのアナログ/デジタル・コンバータ(ADC)、基準電圧とサンプル・アンド・ホールド機能を内蔵し、最大16の外部入力チャネル
  - 最大320セグメントのコントラスト制御を搭載した内蔵LCDドライバ
- マルチファンクションの入力/出力ポート
  - P1～P10およびPJピンはすべて、外付け部品の必要なしに容量性タッチ能力をサポート
  - ビット、バイト、ワード単位でアクセス可能(ペアで)
  - ポートP1、P2、P3、P4上でLPMからウェークアップをエッジ選択可能
  - すべてのポートでプルアップおよびプルダウンをプログラム可能
- コードのセキュリティと暗号化
  - 128ビットまたは256ビットのAESセキュリティ暗号化および復号化コプロセッサ
  - 真の乱数シードによる乱数生成アルゴリズム
- シリアル通信の拡張機能
  - eUSCI_A0およびeUSCI_A1でのサポート
    - 自動ボーレート検出機能付きのUART
    - IrDAのエンコードおよびデコード
    - SPI
  - eUSCI_B0およびeUSCI_B1でのサポート
    - 複数のスレーブ・アドレッシングを持つI^2C
    - SPI
  - ハードウェアUARTまたはI^2Cブートローダー(BSL)
- 柔軟なクロック・システム
  - 固定周波数DCO、出荷時にトリムされた10の周波数を選択可能
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 32kHzの水晶振動子(LFXT)
  - 高周波数の水晶振動子(HFXT)
- 開発ツールとソフトウェア
  - 無償のプロフェッショナル開発環境: EnergyTrace++™テクノロジを使用
  - 実験および開発キット
- ファミリ製品
  - 利用可能なデバイスのバリエーションおよびパッケージ・タイプについては、「デバイスの比較」の概要を参照してください。
- モジュールの完全な説明については、*『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』*を参照してください。

(1) RTCは3.7pFの水晶振動子によりクロック供給を受けます。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

1.2 アプリケーション

- 水量メータ
- 熱メータ
- ヒート・コスト・アロケータ
- ポータブル医療用メーター
- データ・ロギング

1.3 概要

MSP430™超低消費電力(ULP) FRAMプラットフォームは、独自の組み込みFRAMと包括的な超低消費電力システム・アーキテクチャとを組み合わせ、より低いエネルギー・バジェットで性能向上を可能にした、イノベータ向けの製品です。FRAMテクノロジにより、SRAMの速度、柔軟性、耐久性と、フラッシュの安定性および信頼性の両方が、はるかに低い消費電力で得られます。

MSP430 ULP FRAMポートフォリオは、FRAM、ULP 16ビットMSP430 CPU、およびインテリジェントなペリフェラルを搭載し、各種のアプリケーションを対象とした、多様なデバイスのセットで構成されます。ULPアーキテクチャには7つの低消費電力モードがあり、エネルギーの制約が厳しいアプリケーションでバッテリ駆動時間を延長できるよう最適化されています。

製品情報(1)

型番	パッケージ	本体サイズ(2)
MSP430FR6979IPZ	LQFP (100)	14mm×14mm
MSP430FR6979IPN	LQFP (80)	12mm×12mm
MSP430FR6928IPM	LQFP (64)	10mm×10mm
MSP430FR6927IRGC	VQFN (64)	9mm×9mm

(1) 最新の製品、パッケージ、および注文情報については、9の「*付録：パッケージ・オプション*」、または www.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

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1.4 機能ブロック図

機能ブロック図を、図 1-1および図 1-2に示します。

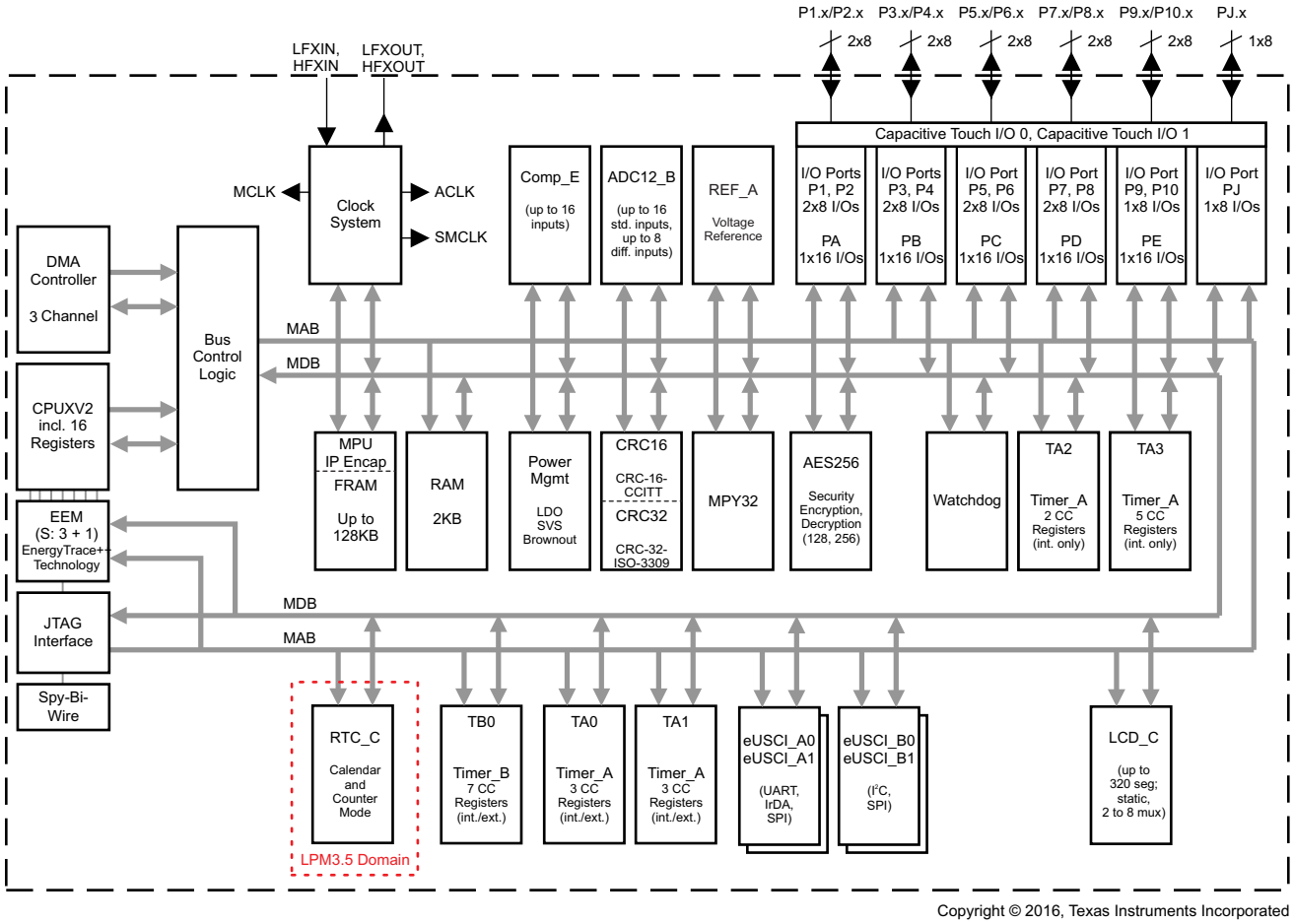
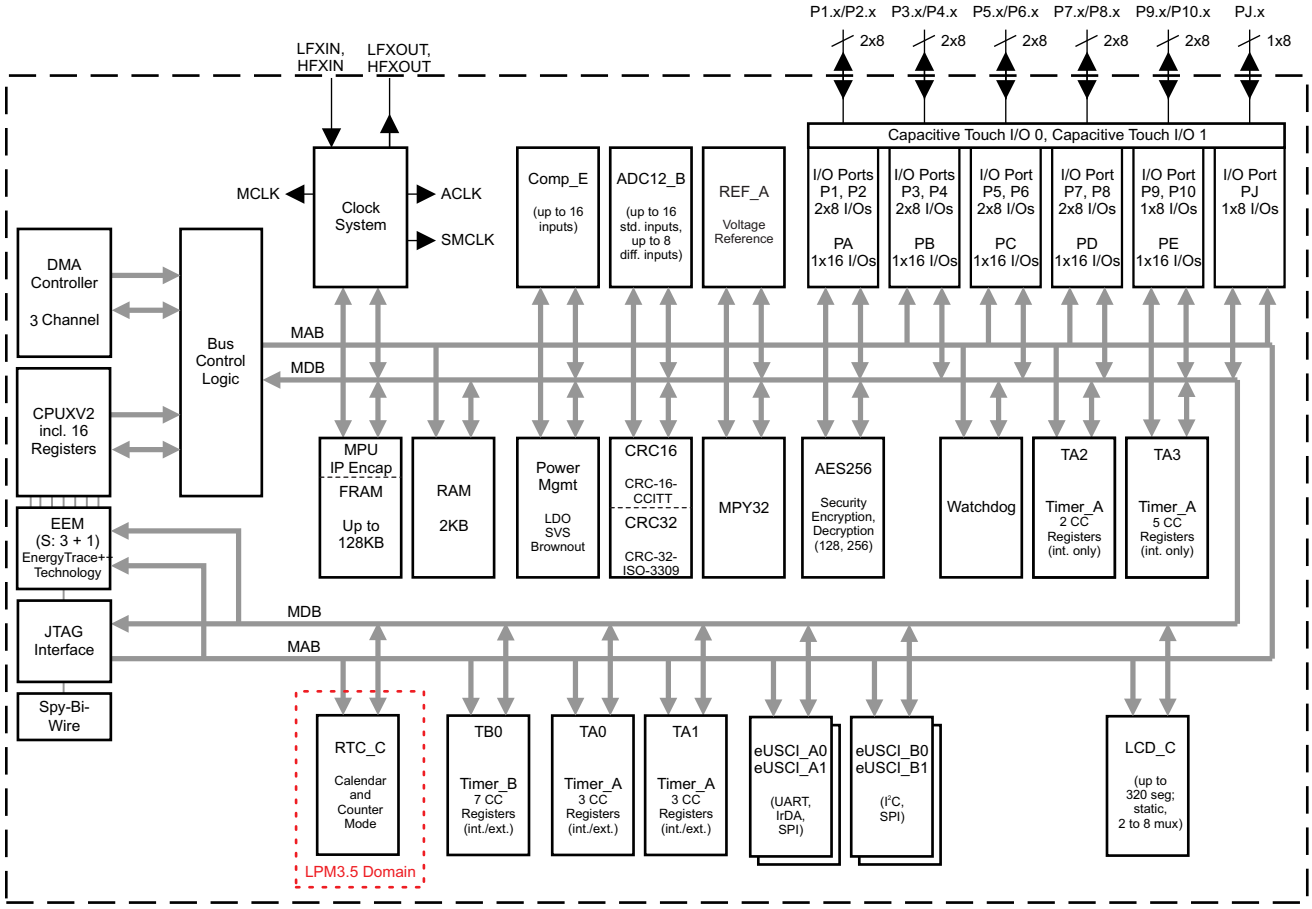


図 1-1. 機能ブロック図 – MSP430FR697x、MSP430FR697x1



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NOTE: HF水晶発振器と、対応するHFXINおよびHFXOUTピンは、MSP430FR692xデバイスには実装されていません。

図 1-2. 機能ブロック図 – MSP430FR692x(1)

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年3月10日発行分から2018年08月29日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 8
- Added note (1) to 表 5-2, *SVS*..... 39
- Changed capacitor value from 4.7 µF to 470 nF in 図 7-5, *ADC12_B Grounding and Noise Considerations* 148
- Changed capacitor value from 4.7 µF to 470 nF in the last paragraph of 7.2.1.2, *Design Requirements* 149
- 8.2、「*デバイスの項目表記*」のテキストおよび図を更新 152

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3 Device Comparison

Table 3-1 and Table 3-2 summarize the available family members.

Table 3-1. Family Members With UART BSL (1) (2)

Device	FRAM (KB)	SRAM (KB)	Clock System	Timer_A	Timer_B	eUSCI		AES	ADC12_B	LCD_C	I/O	Package Type
						A	B					
MSP430FR6979	128	2	DCO **HFXT** **LFXT**	3, 3 2, 5	7	2	2	yes	12 ext 16 ext	240 seg 320 seg	63 83	80 PN 100 PZ
MSP430FR6977	64	2	DCO **HFXT** **LFXT**	3, 3 2, 5	7	2	2	yes	12 ext 16 ext	240 seg 320 seg	63 83	80 PN 100 PZ
MSP430FR6928	96	2	DCO **LFXT**	3, 3 2, 5	7	2	2	yes	8 ext	116 seg (4 mux)	52	64 PM
MSP430FR6927	64	2	DCO **LFXT**	3, 3 2, 5	7	2	2	yes	8 ext	116 seg (4 mux)	52	64 PM 64 RGC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.

Table 3-2. Family Members With I²C BSL (1) (2)

Device	FRAM (KB)	SRAM (KB)	Clock System	Timer_A	Timer_B	eUSCI		AES	ADC12_B	LCD_C	I/O	Package Type
						A	B					
MSP430FR69791	128	2	DCO **HFXT** **LFXT**	3, 3 2, 5	7	2	2	yes	12 ext 16 ext	240 seg 320 seg	63 83	80 PN 100 PZ
MSP430FR69271	64	2	DCO **LFXT**	3, 3 2, 5	7	2	2	yes	8 ext	116 seg (4 mux)	52	64 PM 64 RGC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing and measurement microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultrasonic and performance sensing microcontrollers Ultra-low-power single-chip MCUs with integrated sensing peripherals

Companion products for MSP430FR6979 Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR6979 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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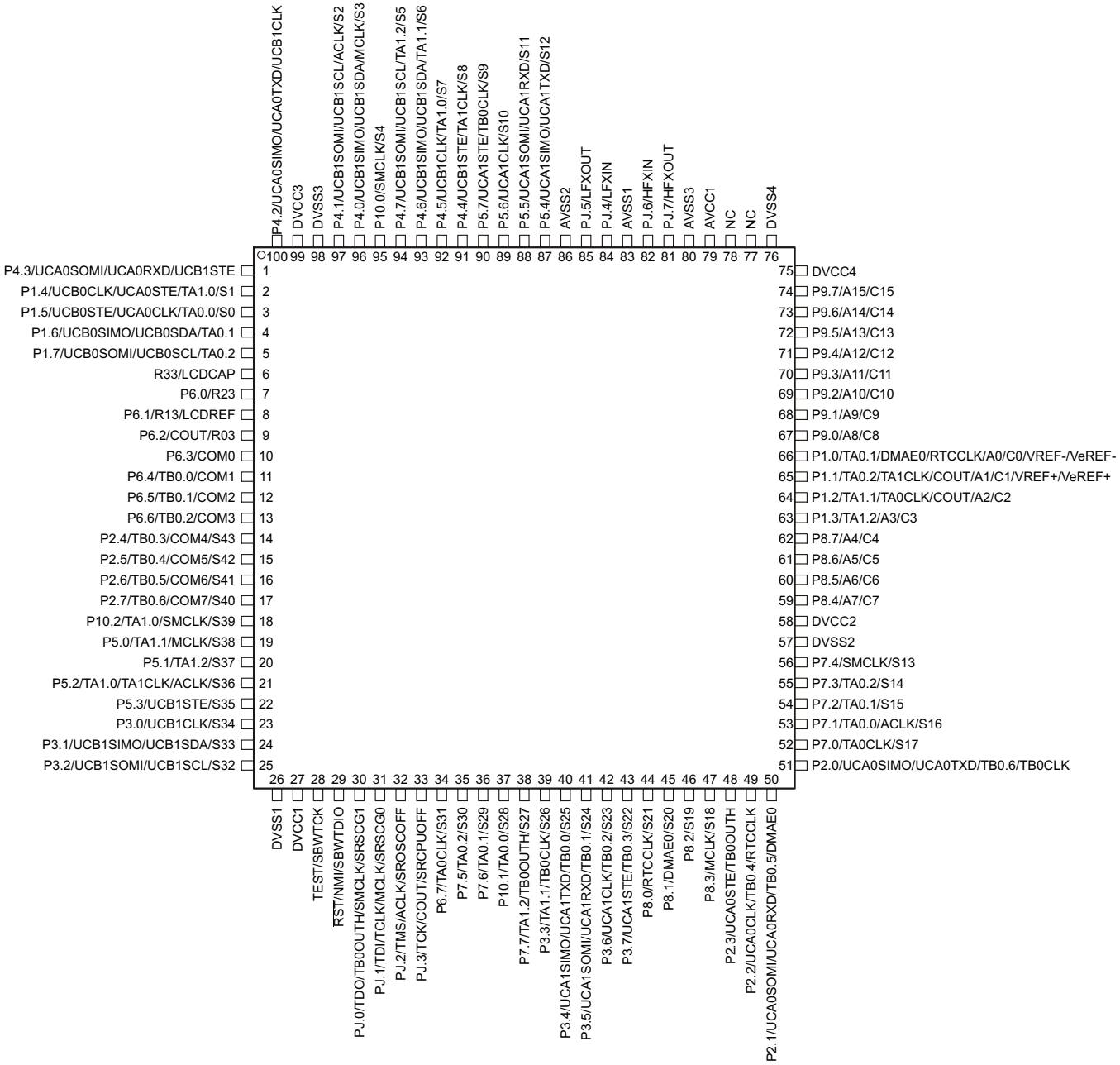
4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 100-pin PZ package for the MSP430FR697x and MSP430FR697x1 MCUs.

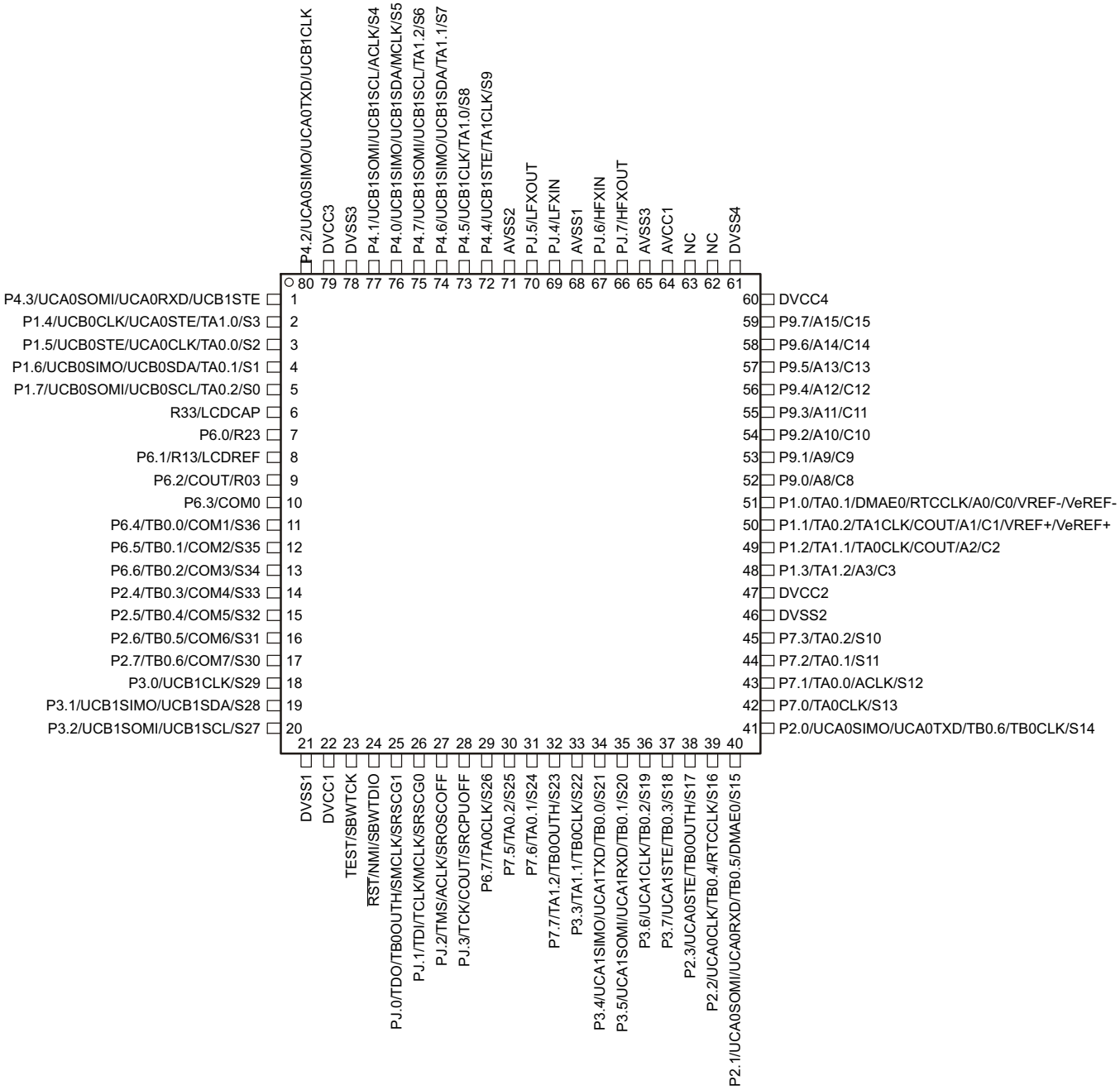


NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

NOTE: On devices with I^2C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-1. 100-Pin PZ Package (Top View) – MSP430FR697x and MSP430FR697x1

Figure 4-2 shows the pinout of the 80-pin PN package for the MSP430FR697x and MSP430FR697x1 MCUs.



NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

NOTE: On devices with I^2C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-2. 80-Pin PN Package (Top View) – MSP430FR697x and MSP430FR697x1

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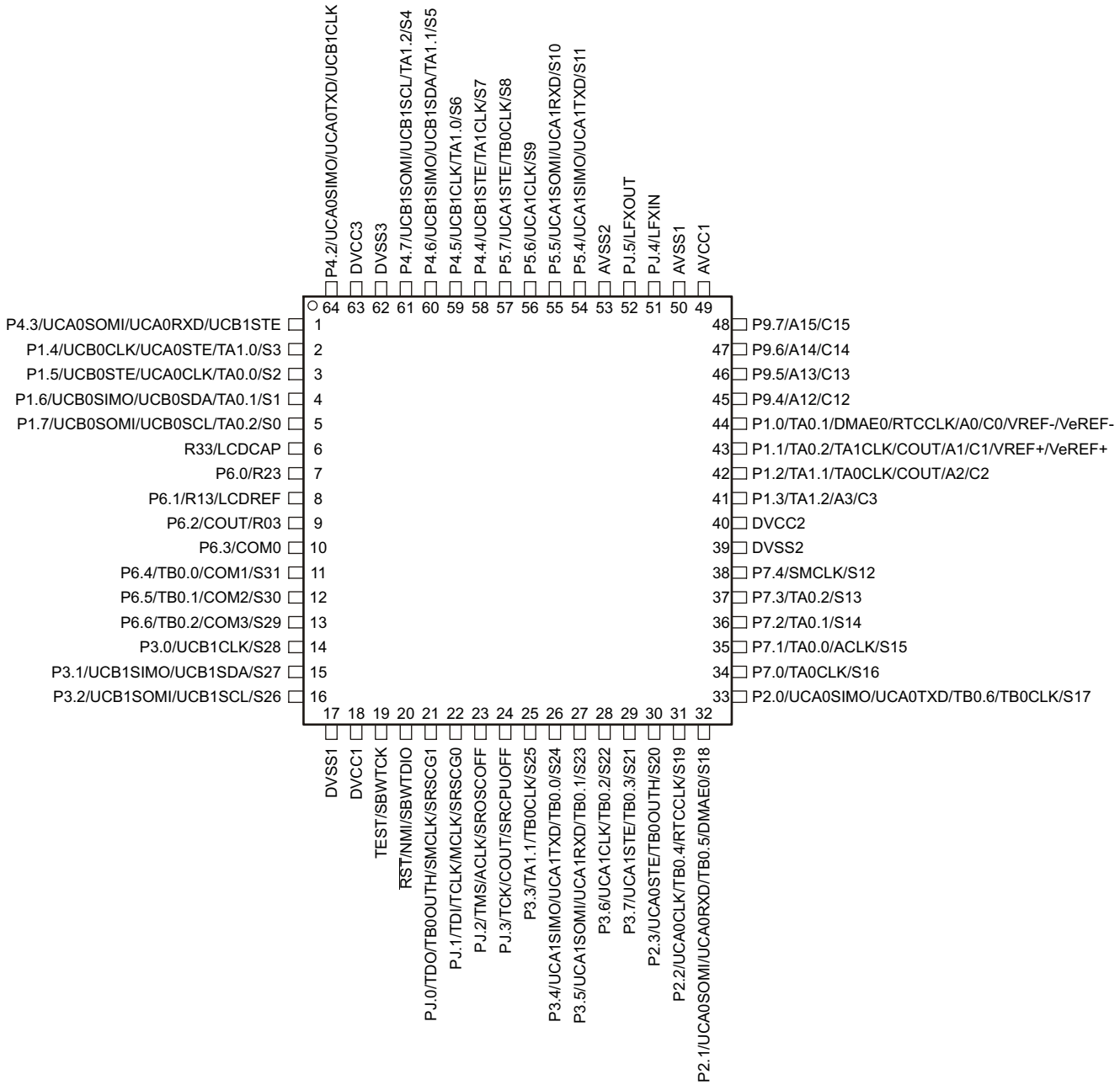
Figure 4-3 shows the pinout of the 64-pin PM and RGC packages for the MSP430FR692x, MSP430FR692x1 MCUs.



NOTE: TI recommends connecting the RGC package pad to VSS.
NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX
NOTE: On devices with I^2C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-3. 64-Pin PM or RGC Package (Top View)

4.2 Signal Descriptions

Table 4-1 and Table 4-2 describe the device signals.

Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P4.3/UCA0SOMI/UCA0RXD/ UCB1STE	1		1		General-purpose digital I/O USCI_A0: Slave out, master in (SPI mode) USCI_A0: Receive data (UART mode) USCI_B1: Slave transmit enable (SPI mode)
P1.4/UCB0CLK/UCA0STE/ TA1.0/Sx	2	S1	2	S3	General-purpose digital I/O USCI_B0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) USCI_A0: Slave transmit enable (SPI mode) Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P1.5/UCB0STE/ UCA0CLK/TA0.0/Sx	3	S0	3	S2	General-purpose digital I/O USCI_B0: Slave transmit enable (SPI mode) USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P1.6/UCB0SIMO/UCB0SDA/ TA0.1/Sx	4		4	S1	General-purpose digital I/O USCI_B0: Slave in, master out (SPI mode) USCI_B0: I^2C data (I^2C mode) BSL data (I^2C BSL) Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P1.7/UCB0SOMI/UCB0SCL/ TA0.2/Sx	5		5	S0	General-purpose digital I/O USCI_B0: Slave out, master in (SPI mode) USCI_B0: I^2C clock (I^2C mode) BSL clock (I^2C BSL) Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
R33/LCDCAP	6		6		Input/output port of most positive analog LCD voltage (V1) LCD capacitor connection
P6.0/R23	7		7		General-purpose digital I/O Input/output port of second most positive analog LCD voltage (V2)
P6.1/R13/LCDREF	8		8		General-purpose digital I/O Input/output port of third most positive analog LCD voltage (V3 or V4) External reference voltage input for regulated LCD voltage
P6.2/COUT/R03	9		9		General-purpose digital I/O Comparator output Input/output port of lowest analog LCD voltage (V5)

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Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P6.3/COM0	10		10		General-purpose digital I/O LCD common output COM0 for LCD backplane
P6.4/TB0.0/COM1/Sx	11		11	S36	General-purpose digital I/O Timer_B TB0 CCR0 capture: CCI0B input, compare: Out0 output LCD common output COM1 for LCD backplane LCD segment output (segment number is package specific)
P6.5/TB0.1/COM2/Sx	12		12	S35	General-purpose digital I/O Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output LCD common output COM2 for LCD backplane LCD segment output (segment number is package specific)
P6.6/TB0.2/COM3/Sx	13		13	S34	General-purpose digital I/O Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output LCD common output COM3 for LCD backplane LCD segment output (segment number is package specific)
P2.4/TB0.3/COM4/Sx	14	S43	14	S33	General-purpose digital I/O Timer_B TB0 CCR3 capture: CCI3A input, compare: Out3 output LCD common output COM4 for LCD backplane LCD segment output (segment number is package specific)
P2.5/TB0.4/COM5/Sx	15	S42	15	S32	General-purpose digital I/O Timer_B TB0 CCR4 capture: CCI4A input, compare: Out4 output LCD common output COM5 for LCD backplane LCD segment output (segment number is package specific)
P2.6/TB0.5/COM6/Sx	16	S41	16	S31	General-purpose digital I/O Timer_B TB0 CCR5 capture: CCI5A input, compare: Out5 output LCD common output COM6 for LCD backplane LCD segment output (segment number is package specific)
P2.7/TB0.6/COM7/Sx	17	S40	17	S30	General-purpose digital I/O Timer_B TB0 CCR6 capture: CCI6A input, compare: Out6 output LCD common output COM7 for LCD backplane LCD segment output (segment number is package specific)
P10.2/TA1.0/SMCLK/Sx	18	S39			General-purpose digital I/O Timer_A TA1 CCR0 capture: CCI0B input, compare: Out0 output SMCLK output LCD segment output (segment number is package specific)
P5.0/TA1.1/MCLK/Sx	19	S38			General-purpose digital I/O Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output MCLK output LCD segment output (segment number is package specific)
P5.1/TA1.2/Sx	20	S37			General-purpose digital I/O Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)

Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P5.2/TA1.0/TA1CLK/ACLK/Sx	21	S36			General-purpose digital I/O Timer_A TA1 CCR0 capture: CCI0B input, compare: Out0 output Timer_A TA1 clock signal TA0CLK input ACLK output LCD segment output (segment number is package specific)
P5.3/UCB1STE/Sx	22	S35			General-purpose digital I/O USCI_B1: Slave transmit enable (SPI mode) LCD segment output (segment number is package specific)
P3.0/UCB1CLK/Sx	23	S34	18	S29	General-purpose digital I/O USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) LCD segment output (segment number is package specific)
P3.1/UCB1SIMO/UCB1SDA/Sx	24	S33	19	S28	General-purpose digital I/O USCI_B1: Slave in, master out (SPI mode) USCI_B1: I^2C data (I^2C mode) LCD segment output (segment number is package specific)
P3.2/UCB1SOMI/UCB1SCL/Sx	25	S32	20	S27	General-purpose digital I/O USCI_B1: Slave out, master in (SPI mode) USCI_B1: I^2C clock (I^2C mode) LCD segment output (segment number is package specific)
DVSS1	26		21		Digital ground supply
DVCC1	27		22		Digital power supply
TEST/SBWTCK	28		23		Test mode pin - select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/SBWTDIO	29		24		Reset input, active low Nonmaskable interrupt input Spy-Bi-Wire data input/output
PJ.0/TDO/TB0OUTH/SMCLK/SRSCG1	30		25		General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input - Timer_B TB0 SMCLK output Low-power debug: CPU Status register SCG1
PJ.1/TDI/TCLK/MCLK/SRSCG0	31		26		General-purpose digital I/O Test data input or test clock input MCLK output Low-power debug: CPU Status register SCG0
PJ.2/TMS/ACLK/SROSCOFF	32		27		General-purpose digital I/O Test mode select ACLK output Low-power debug: CPU Status register OSCOFF

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Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
PJ.3/TCK/COUT/SRCPUOFF	33		28		General-purpose digital I/O Test clock Comparator output Low-power debug: CPU Status register CPUOFF
P6.7/TA0CLK/Sx	34	S31	29	S26	General-purpose digital I/O Timer_A TA0 clock signal TA0CLK input LCD segment output (segment number is package specific)
P7.5/TA0.2/Sx	35	S30	30	S25	General-purpose digital I/O Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
P7.6/TA0.1/Sx	36	S29	31	S24	General-purpose digital I/O Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P10.1/TA0.0/Sx	37	S28			General-purpose digital I/O Timer_A TA0 CCR0 capture: CCI0B input, compare: Out0 output LCD segment output (segment number is package specific)
P7.7/TA1.2/TB0OUTH/Sx	38	S27	32	S23	General-purpose digital I/O Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output Switch all PWM outputs high impedance input - Timer_B TB0 LCD segment output (segment number is package specific)
P3.3/TA1.1/TB0CLK/Sx	39	S26	33	S22	General-purpose digital I/O Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)
P3.4/UCA1SIMO/UCA1TXD/ TB0.0/Sx	40	S25	34	S21	General-purpose digital I/O USCI_A1: Slave in, master out (SPI mode) USCI_A1: Transmit data (UART mode) Timer_B TB0 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P3.5/UCA1SOMI/UCA1RXD/ TB0.1/Sx	41	S24	35	S20	General-purpose digital I/O USCI_A1: Slave out, master in (SPI mode) USCI_A1: Receive data (UART mode) Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P3.6/UCA1CLK/TB0.2/Sx	42	S23	36	S19	General-purpose digital I/O USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)

Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P3.7/UCA1STE/TB0.3/Sx	43	S22	37	S18	General-purpose digital I/O USCI_A1: Slave transmit enable (SPI mode) Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output LCD segment output (segment number is package specific)
P8.0/RTCCLK/Sx	44	S21			General-purpose digital I/O RTC clock output for calibration LCD segment output (segment number is package specific)
P8.1/DMAE0/Sx	45	S20			General-purpose digital I/O DMA external trigger input LCD segment output (segment number is package specific)
P8.2/Sx	46	S19			General-purpose digital I/O LCD segment output (segment number is package specific)
P8.3/MCLK/Sx	47	S18			General-purpose digital I/O MCLK output LCD segment output (segment number is package specific)
P2.3/UCA0STE/TB0OUTH/Sx	48		38	S17	General-purpose digital I/O USCI_A0: Slave transmit enable (SPI mode) Switch all PWM outputs high impedance input - Timer_B TB0 LCD segment output (segment number is package specific)
P2.2/UCA0CLK/TB0.4/ RTCCLK/Sx	49		39	S16	General-purpose digital I/O USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output RTC clock output for calibration LCD segment output (segment number is package specific)
P2.1/UCA0SOMI/UCA0RXD/ TB0.5/DMAE0/Sx	50		40	S15	General-purpose digital I/O USCI_A0: Slave out, master in (SPI mode) USCI_A0: Receive data (UART mode) BSL receive (UART BSL) Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output DMA external trigger input LCD segment output (segment number is package specific)
P2.0/UCA0SIMO/UCA0TXD/ TB0.6/TB0CLK/Sx	51		41	S14	General-purpose digital I/O USCI_A0: Slave in, master out (SPI mode) USCI_A0: Transmit data (UART mode) BSL transmit (UART BSL) Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)

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Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P7.0/TA0CLK/Sx	52	S17	42	S13	General-purpose digital I/O Timer_A TA0 clock signal TA0CLK input LCD segment output (segment number is package specific)
P7.1/TA0.0/ACLK/Sx	53	S16	43	S12	General-purpose digital I/O Timer_A TA0 CCR0 capture: CCI0B input, compare: Out0 output ACLK output LCD segment output (segment number is package specific)
P7.2/TA0.1/Sx	54	S15	44	S11	General-purpose digital I/O Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P7.3/TA0.2/Sx	55	S14	45	S10	General-purpose digital I/O Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
P7.4/SMCLK/Sx	56	S13			General-purpose digital I/O SMCLK output LCD segment output (segment number is package specific)
DVSS2	57		46		Digital ground supply
DVCC2	58		47		Digital power supply
P8.4/A7/C7	59				General-purpose digital I/O Analog input A7 Comparator input C7
P8.5/A6/C6	60				General-purpose digital I/O Analog input A6 Comparator input C6
P8.6/A5/C5	61				General-purpose digital I/O Analog input A5 Comparator input C5
P8.7/A4/C4	62				General-purpose digital I/O Analog input A4 Comparator input C4
P1.3/TA1.2/A3/C3	63		48		General-purpose digital I/O Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output Analog input A3 Comparator input C3
P1.2/TA1.1/TA0CLK/ COUT/A2/C2	64		49		General-purpose digital I/O Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output Timer_A TA0 clock signal TA0CLK input Comparator output Analog input A2 Comparator input C2

Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P1.1/TA0.2/TA1CLK/ COUT/A1/C1/VREF+/VeREF+	65		50		General-purpose digital I/O Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output Timer_A TA1 clock signal TA1CLK input Comparator output Analog input A1 Comparator input C1 Output of positive reference voltage Input for an external positive reference voltage to the ADC
P1.0/TA0.1/DMAE0/ RTCCLK/A0/C0/ VREF-/VeREF-	66		51		General-purpose digital I/O Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output DMA external trigger input RTC clock output for calibration Analog input A0 Comparator input C0 Output of negative reference voltage Input for an external negative reference voltage to the ADC
P9.0/A8/C8	67		52		General-purpose digital I/O Analog input A8 Comparator input C8
P9.1/A9/C9	68		53		General-purpose digital I/O Analog input A9 Comparator input C9
P9.2/A10/C10	69		54		General-purpose digital I/O Analog input A10; comparator input C10
P9.3/A11/C11	70		55		General-purpose digital I/O Analog input A11 Comparator input C11
P9.4/A12/C12	71		56		General-purpose digital I/O Analog input A12 Comparator input C12
P9.5/A13/C13	72		57		General-purpose digital I/O Analog input A13 Comparator input C13
P9.6/A14/C14	73		58		General-purpose digital I/O Analog input A14 Comparator input C14
P9.7/A15/C15	74		59		General-purpose digital I/O Analog input A15 Comparator input C15
DVCC4	75		60		Digital power supply
DVSS4	76		61		Digital ground supply

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Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
NC	77		62		No connect
NC	78		63		No connect
AVCC1	79		64		Analog power supply
AVSS3	80		65		Analog ground supply
PJ.7/HFXOUT	81		66		General-purpose digital I/O Output terminal of crystal oscillator XT2
PJ.6/HFXIN	82		67		General-purpose digital I/O Input terminal for crystal oscillator XT2
AVSS1	83		68		Analog ground supply
PJ.4/LFXIN	84		69		General-purpose digital I/O Input terminal for crystal oscillator XT1
PJ.5/LFXOUT	85		70		General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS2	86		71		Analog ground supply
P5.4/UCA1SIMO/UCA1TXD/Sx	87	S12			General-purpose digital I/O USCI_A1: Slave in, master out (SPI mode) USCI_A1: Transmit data (UART mode) LCD segment output (segment number is package specific)
P5.5/UCA1SOMI/UCA1RXD/Sx	88	S11			General-purpose digital I/O USCI_A1: Slave out, master in (SPI mode) USCI_A1: Receive data (UART mode) LCD segment output (segment number is package specific)
P5.6/UCA1CLK/Sx	89	S10			General-purpose digital I/O USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) LCD segment output (segment number is package specific)
P5.7/UCA1STE/TB0CLK/Sx	90	S9			General-purpose digital I/O USCI_A1: Slave transmit enable (SPI mode) Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)
P4.4/UCB1STE/TA1CLK/Sx	91	S8	72	S9	General-purpose digital I/O USCI_B1: Slave transmit enable (SPI mode) Timer_A TA1 clock signal TA1CLK input LCD segment output (segment number is package specific)
P4.5/UCB1CLK/TA1.0/Sx	92	S7	73	S8	General-purpose digital I/O USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)

Table 4-1. Signal Descriptions – MSP430FR697x and MSP430FR697x1 (continued)

TERMINAL					DESCRIPTION
NAME	PZ		PN		
	NO.	Seg.	NO.	Seg.	
P4.6/UCB1SIMO/UCB1SDA/ TA1.1/Sx	93	S6	74	S7	General-purpose digital I/O USCI_B1: Slave in, master out (SPI mode) USCI_B1: I^2C data (I^2C mode) Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P4.7/UCB1SOMI/UCB1SCL/ TA1.2/Sx	94	S5	75	S6	General-purpose digital I/O USCI_B1: Slave out, master in (SPI mode) USCI_B1: I^2C clock (I^2C mode) Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
P10.0/SMCLK/Sx	95	S4			General-purpose digital I/O SMCLK output LCD segment output (segment number is package specific)
P4.0/UCB1SIMO/UCB1SDA/ MCLK/Sx	96	S3	76	S5	General-purpose digital I/O USCI_B1: Slave in, master out (SPI mode) USCI_B1: I^2C data (I^2C mode) MCLK output LCD segment output (segment number is package specific)
P4.1/UCB1SOMI/UCB1SCL/ ACLK/Sx	97	S2	77	S4	General-purpose digital I/O USCI_B1: Slave out, master in (SPI mode) USCI_B1: I^2C clock (I^2C mode) ACLK output LCD segment output (segment number is package specific)
DVSS3	98		78		Digital ground supply
DVCC3	99		79		Digital power supply
P4.2/UCA0SIMO/UCA0TXD/ UCB1CLK	100		80		General-purpose digital I/O USCI_A0: Slave in, master out (SPI mode) USCI_A0: Transmit data (UART mode) USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)

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Table 4-2. Signal Descriptions – MSP430FR692x(1)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
P4.3/UCA0SOMI/UCA0RXD/ UCB1STE	1		General-purpose digital I/O USCI_A0: Slave out, master in (SPI mode) USCI_A0: Receive data (UART mode) USCI_B1: Slave transmit enable (SPI mode)
P1.4/UCB0CLK/UCA0STE/TA1.0/ Sx	2	S3	General-purpose digital I/O USCI_B0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) USCI_A0: Slave transmit enable (SPI mode) Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P1.5/UCB0STE/UCA0CLK/TA0.0/ Sx	3	S2	General-purpose digital I/O USCI_B0: Slave transmit enable (SPI mode) USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P1.6/UCB0SIMO/UCB0SDA/TA0.1/ Sx	4	S1	General-purpose digital I/O USCI_B0: Slave in, master out (SPI mode) USCI_B0: I^2C data (I^2C mode) BSL data (I^2C BSL) Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P1.7/UCB0SOMI/UCB0SCL/TA0.2/ Sx	5	S0	General-purpose digital I/O USCI_B0: Slave out, master in (SPI mode) USCI_B0: I^2C clock (I^2C mode) BSL clock (I^2C BSL) Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
R33/LCDCAP	6		Input/output port of most positive analog LCD voltage (V1) LCD capacitor connection
P6.0/R23	7		General-purpose digital I/O Input/output port of second most positive analog LCD voltage (V2)
P6.1/R13/LCDREF	8		General-purpose digital I/O Input/output port of third most positive analog LCD voltage (V3 or V4) External reference voltage input for regulated LCD voltage
P6.2/COUT/R03	9		General-purpose digital I/O Comparator output Input/output port of lowest analog LCD voltage (V5)
P6.3/COM0	10		General-purpose digital I/O LCD common output COM0 for LCD backplane

Table 4-2. Signal Descriptions – MSP430FR692x(1) (continued)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
P6.4/TB0.0/COM1/Sx	11	S31	General-purpose digital I/O Timer_B TB0 CCR0 capture: CCI0B input, compare: Out0 output LCD common output COM1 for LCD backplane LCD segment output (segment number is package specific)
P6.5/TB0.1/COM2/Sx	12	S30	General-purpose digital I/O Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output LCD common output COM2 for LCD backplane LCD segment output (segment number is package specific)
P6.6/TB0.2/COM3/Sx	13	S29	General-purpose digital I/O Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output LCD common output COM3 for LCD backplane LCD segment output (segment number is package specific)
P3.0/UCB1CLK/Sx	14	S28	General-purpose digital I/O USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) LCD segment output (segment number is package specific)
P3.1/UCB1SIMO/UCB1SDA/Sx	15	S27	General-purpose digital I/O USCI_B1: Slave in, master out (SPI mode) USCI_B1: I^2C data (I^2C mode) LCD segment output (segment number is package specific)
P3.2/UCB1SOMI/UCB1SCL/Sx	16	S26	General-purpose digital I/O USCI_B1: Slave out, master in (SPI mode) USCI_B1: I^2C clock (I^2C mode) LCD segment output (segment number is package specific)
DVSS1	17		Digital ground supply
DVCC1	18		Digital power supply
TEST/SBWTCK	19		Test mode pin - select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/SBWTDIO	20		Reset input, active low Nonmaskable interrupt input Spy-Bi-Wire data input/output
PJ.0/TDO/TB0OUTH/SMCLK/ SRSCG1	21		General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input - Timer_B TB0 SMCLK output Low-power debug: CPU Status register SCG1
PJ.1/TDI/TCLK/MCLK/SRSCG0	22		General-purpose digital I/O Test data input or test clock input MCLK output Low-power debug: CPU Status register SCG0

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Table 4-2. Signal Descriptions – MSP430FR692x(1) (continued)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
PJ.2/TMS/ACLK/SROSCOFF	23		General-purpose digital I/O Test mode select ACLK output Low-power debug: CPU Status register OSCOFF
PJ.3/TCK/COUT/SRCPUOFF	24		General-purpose digital I/O Test clock Comparator output Low-power debug: CPU Status register CPUOFF
P3.3/TA1.1/TB0CLK/Sx	25	S25	General-purpose digital I/O Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)
P3.4/UCA1SIMO/UCA1TXD/ TB0.0/Sx	26	S24	General-purpose digital I/O USCI_A1: Slave in, master out (SPI mode) USCI_A1: Transmit data (UART mode) Timer_B TB0 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P3.5/UCA1SOMI/UCA1RXD/ TB0.1/Sx	27	S23	General-purpose digital I/O USCI_A1: Slave out, master in (SPI mode) USCI_A1: Receive data (UART mode) Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P3.6/UCA1CLK/TB0.2/Sx	28	S22	General-purpose digital I/O USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
P3.7/UCA1STE/TB0.3/Sx	29	S21	General-purpose digital I/O USCI_A1: Slave transmit enable (SPI mode) Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output LCD segment output (segment number is package specific)
P2.3/UCA0STE/TB0OUTH/Sx	30	S20	General-purpose digital I/O USCI_A0: Slave transmit enable (SPI mode) Switch all PWM outputs high impedance input - Timer_B TB0 LCD segment output (segment number is package specific)
P2.2/UCA0CLK/TB0.4/RTCCLK/Sx	31	S19	General-purpose digital I/O USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output RTC clock output for calibration LCD segment output (segment number is package specific)

Table 4-2. Signal Descriptions – MSP430FR692x(1) (continued)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
P2.1/UCA0SOMI/UCA0RXD/ TB0.5/DMAE0/Sx	32	S18	General-purpose digital I/O USCI_A0: Slave out, master in (SPI mode), Receive data (UART mode) BSL receive (UART BSL) Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output DMA external trigger input LCD segment output (segment number is package specific)
P2.0/UCA0SIMO/UCA0TXD/ TB0.6/TB0CLK/Sx	33	S17	General-purpose digital I/O USCI_A0: Slave in, master out (SPI mode) USCI_A0: Transmit data (UART mode) BSL transmit (UART BSL) Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)
P7.0/TA0CLK/Sx	34	S16	General-purpose digital I/O Timer_A TA0 clock signal TA0CLK input LCD segment output (segment number is package specific)
P7.1/TA0.0/ACLK/Sx	35	S15	General-purpose digital I/O Timer_A TA0 CCR0 capture: CCI0B input, compare: Out0 output ACLK output LCD segment output (segment number is package specific)
P7.2/TA0.1/Sx	36	S14	General-purpose digital I/O Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P7.3/TA0.2/Sx	37	S13	General-purpose digital I/O Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
P7.4/SMCLK/Sx	38	S12	General-purpose digital I/O SMCLK output LCD segment output (segment number is package specific)
DVSS2	39		Digital ground supply
DVCC2	40		Digital power supply
P1.3/TA1.2/A3/C3	41		General-purpose digital I/O Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output Analog input A3 Comparator input C3

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Table 4-2. Signal Descriptions – MSP430FR692x(1) (continued)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
P1.2/TA1.1/TA0CLK/COUT/A2/C2	42		General-purpose digital I/O Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output Timer_A TA0 clock signal TA0CLK input Comparator output Analog input A2 Comparator input C2
P1.1/TA0.2/TA1CLK/COUT/A1/C1/VREF+/VeREF+	43		General-purpose digital I/O Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output Timer_A TA1 clock signal TA1CLK input Comparator output Analog input A1 Comparator input C1 Output of positive reference voltage Input for an external positive reference voltage to the ADC
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/VREF-/VeREF-	44		General-purpose digital I/O Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output DMA external trigger input RTC clock output for calibration Analog input A0 Comparator input C0 Output of negative reference voltage Input for an external negative reference voltage to the ADC
AVCC1	49		Analog power supply
AVSS1	50		Analog ground supply
PJ.4/LFXIN	51		General-purpose digital I/O Input terminal for crystal oscillator XT1
PJ.5/LFXOUT	52		General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS2	53		Analog ground supply
P5.4/UCA1SIMO/UCA1TXD/Sx	54	S11	General-purpose digital I/O USCI_A1: Slave in, master out (SPI mode) USCI_A1: Transmit data (UART mode) LCD segment output (segment number is package specific)
P5.5/UCA1SOMI/UCA1RXD/Sx	55	S10	General-purpose digital I/O USCI_A1: Slave out, master in (SPI mode) USCI_A1: Receive data (UART mode) LCD segment output (segment number is package specific)
P5.6/UCA1CLK/Sx	56	S9	General-purpose digital I/O USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) LCD segment output (segment number is package specific)

Table 4-2. Signal Descriptions – MSP430FR692x(1) (continued)

TERMINAL			DESCRIPTION
NAME	PM RGC		
	NO.	Seg.	
P5.7/UCA1STE/TB0CLK/Sx	57	S8	General-purpose digital I/O USCI_A1: Slave transmit enable (SPI mode) Timer_B TB0 clock signal TB0CLK input LCD segment output (segment number is package specific)
P4.4/UCB1STE/TA1CLK/Sx	58	S7	General-purpose digital I/O USCI_B1: Slave transmit enable (SPI mode) Timer_A TA1 clock signal TA1CLK input LCD segment output (segment number is package specific)
P4.5/UCB1CLK/TA1.0/Sx	59	S6	General-purpose digital I/O USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output (segment number is package specific)
P4.6/UCB1SIMO/UCB1SDA/ TA1.1/Sx	60	S5	General-purpose digital I/O USCI_B1: Slave in, master out (SPI mode) USCI_B1: I^2C data (I^2C mode) Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output LCD segment output (segment number is package specific)
P4.7/UCB1SOMI/UCB1SCL/ TA1.2/Sx	61	S4	General-purpose digital I/O USCI_B1: Slave out, master in (SPI mode) USCI_B1: I^2C clock (I^2C mode) Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output LCD segment output (segment number is package specific)
DVSS3	62		Digital ground supply
DVCC3	63		Digital power supply
P4.2/UCA0SIMO/UCA0TXD/ UCB1CLK	64		General-purpose digital I/O USCI_A0: Slave in, master out (SPI mode) USCI_A0: Transmit data (UART mode) USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)
Thermal pad	Pad		RGC package only. QFN package exposed thermal pad. TI recommends connection to V_{SS}.

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4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 6.11.23.

4.4 Connection of Unused Pins

Table 4-3 lists the correct termination of all unused pins.

Table 4-3. Connection of Unused Pins(1)

PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
AVSS	DV_{SS}	
Px.0 to Px.7	Open	Set to port function, output direction (PxDIR.n = 1)
R33/LCDCAP	DV_{SS} or DV_{CC}	If the pin is not used, it can be tied to either supply.
$\overline{RST}$/NMI	DV_{CC} or V_{CC}	47-kΩ pullup or internal pullup selected with 2.2-nF (10-nF(2)) pulldown
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If not used as JTAG pins, these pins should be switched to port function, output direction. When used as JTAG pins, these pins should remain open.
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.1	V
Voltage difference between DVCC and AVCC pins(2)		±0.3	V
Voltage applied to any pin (3)	–0.3	V_{CC} + 0.3 V (4.1 Max)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg}(4)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(3) All voltages referenced to V_{SS}.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C unless otherwise noted.

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins(1) (2) (3)		1.8(4)		3.6	V
V_{SS}	Supply voltage applied at all DSS and AVSS pins			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Capacitor value at DVCC (5)		$1_{-20\%}$			µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(6)	No FRAM wait states (NWAITSx = 0)	0		8(7)	MHz
		With FRAM wait states (NWAITSx = 1)(8)	0		16(9)	
f_{ACLK}	Maximum ACLK frequency				50	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(9)	MHz

(1) TI recommends powering the DVCC and AVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between DVCC and AVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(2) See 表 5-1 for additional important information.
(3) Modules may have a different supply voltage range specification. See the specification of each module in this data sheet.
(4) The minimum supply voltage is defined by the supervisor SVS levels. See 表 5-2 for the exact values.
(5) Connect a low-ESR capacitor with at least the value specified and a maximum tolerance of 20% as close as possible to the DVCC pin.
(6) Modules may have a different maximum input clock specification. See the specification of each module in this data sheet.
(7) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
(8) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
(9) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock sources with a larger typical value is used, the clock must be divided in the clock system.

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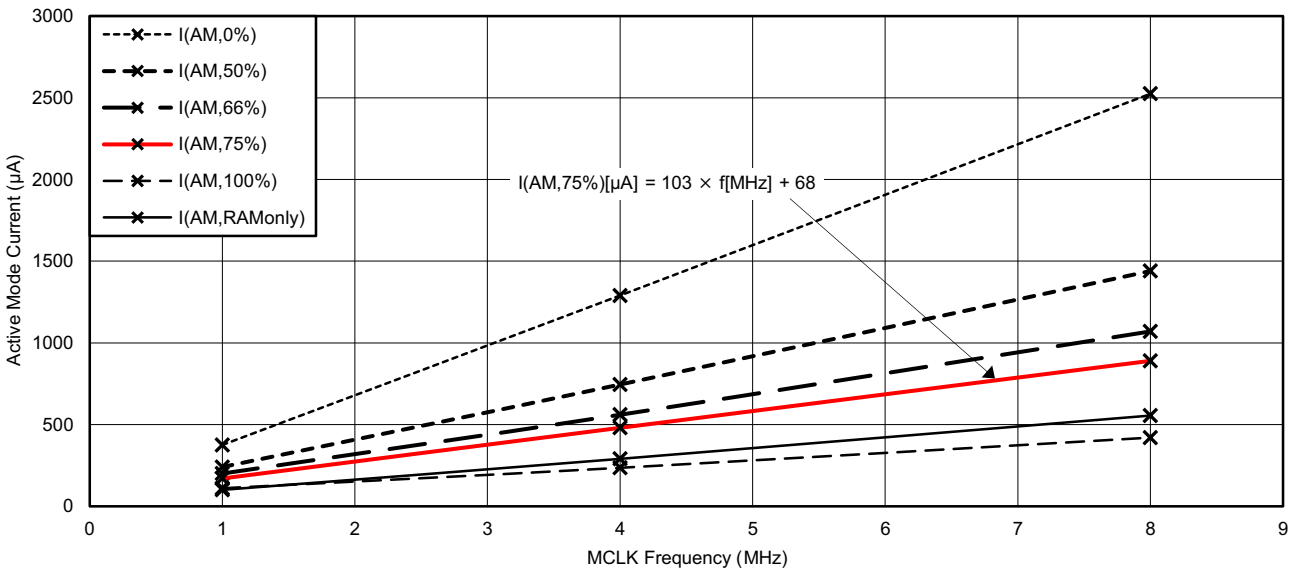
5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		4 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		12 MHz 1 WAIT STATE (NWAITSx = 1)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM_UNI}$ (Unified memory)(3)	FRAM	3.0 V	210		640		1220		1475		1845		µA
$I_{AM, FRAM}$(0%)(4) (5)	FRAM 0% cache hit ratio	3.0 V	375		1290		2525		2100		2675		µA
$I_{AM, FRAM}$(50%)(4) (5)	FRAM 50% cache hit ratio	3.0 V	240		745		1440		1575		1990		µA
$I_{AM, FRAM}$(66%)(4) (5)	FRAM 66% cache hit ratio	3.0 V	200		560		1070		1300		1620		µA
$I_{AM, FRAM}$(75%)(4) (5)	FRAM 75% cache hit ratio	3.0 V	170	255	480		890	1085	1155	1310	1420	1620	µA
$I_{AM, FRAM}$(100%(4) (5)	FRAM 100% cache hit ratio	3.0 V	110		235		420		640		730		µA
$I_{AM, RAM}$ (6) (5)	RAM	3.0 V	130		320		585		890		1070		µA
$I_{AM, RAM\ only}$ (7) (5)	RAM	3.0 V	100	180	290		555		860		1040	1300	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, f_{DCO} = 24 MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO} / 2$.
At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.
The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff} = f_{MCLK}$ / [wait states × (1 – cache hit ratio) + 1]
For example, with 1 wait state and 75% cache hit ratio $f_{MCKL,eff} = f_{MCLK}$ / [1 × (1 – 0.75) + 1] = f_{MCLK} / 1.25.
(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
(5) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 5.4.
(6) Program and data reside entirely in RAM. All execution is from RAM.
(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

5.5 Typical Characteristics, Active Mode Supply Currents



I(AM, cache hit ratio): Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
I(AM, RAMonly): Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

Figure 5-1. Typical Active Mode Supply Currents, No Wait States

5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})										UNIT
		1 MHz		4 MHz		8 MHz		12 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2.2 V	75		105		165		250		230		µA
	3.0 V	85	120	115		175		260		240	275	
I_{LPM1}	2.2 V	40		65		130		215		195		µA
	3.0 V	40	65	65		130		215		195	220	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} at specified frequency, except for 12 MHz: here f_{DCO} = 24 MHz and f_{SMCLK} = f_{DCO} / 2.

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5.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		V_{CC}	TEMPERATURE (T_A)								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM2,XT12}$	Low-power mode 2, 12-pF crystal (2) (3) (4)	2.2 V	0.6		1.2		3.1		8.8		µA
		3.0 V	0.6		1.2	2.2	3.1		8.8	20.8	
$I_{LPM2,XT3.7}$	Low-power mode 2, 3.7-pF crystal (2) (5) (4)	2.2 V	0.5		1.1		3.0		8.7		µA
		3.0 V	0.5		1.1		3.0		8.7		
$I_{LPM2,VLO}$	Low-power mode 2, VLO, includes SVS (6)	2.2 V	0.3		0.9		2.8		8.5		µA
		3.0 V	0.3		0.9	2.0	2.8		8.5	20.5	
$I_{LPM3,XT12}$	Low-power mode 3, 12-pF crystal, excludes SVS (2) (3) (7)	2.2 V	0.5		0.7		1.2		2.5		µA
		3.0 V	0.5		0.7	1.0	1.2		2.5	6.4	
$I_{LPM3,XT3.7}$	Low-power mode 3, 3.7-pF crystal, excludes SVS (2) (5) (8) (also see Figure 5-2)	2.2 V	0.4		0.6		1.1		2.4		µA
		3.0 V	0.4		0.6		1.1		2.4		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS (9)	2.2 V	0.3		0.4		0.9		2.2		µA
		3.0 V	0.3		0.4	0.8	0.9		2.2	6.1	
$I_{LPM3,VLO,RAMoff}$	Low-power mode 3, VLO, excludes SVS, RAM powered-down completely (10)	2.2 V	0.3		0.4		0.8		2.1		µA
		3.0 V	0.3		0.4	0.7	0.8		2.1	5.2	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
(4) Low-power mode 2, crystal oscillator test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 2, VLO test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 3, 12-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(8) Low-power mode 3, 3.7-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(9) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(10) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). RAM disabled (RCCTL0 = 5A55h). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

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Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) [(1)]

PARAMETER		V_{CC}	TEMPERATURE (T_A)								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM4,SVS}$	Low-power mode 4, includes SVS[(11)]	2.2 V	0.4		0.5		0.9		2.3		µA
		3.0 V	0.4		0.5	0.8	0.9		2.3	6.2	
I_{LPM4}	Low-power mode 4, excludes SVS[(12)]	2.2 V	0.2		0.3		0.7		2.0		µA
		3.0 V	0.2		0.3	0.6	0.7		2.0	6.0	
$I_{LPM4,RAMoff}$	Low-power mode 4, excludes SVS, RAM powered-down completely[(13)]	2.2 V	0.2		0.3		0.7		1.9		µA
		3.0 V	0.2		0.3	0.6	0.7		1.9	5.1	
$I_{IDLE,GroupA}$	Additional idle current if one or more modules from Group A (see 表 6-3) are activated in LPM3 or LPM4	3.0V			0.02				0.3	1.2	µA
$I_{IDLE,GroupB}$	Additional idle current if one or more modules from Group B (see 表 6-3) are activated in LPM3 or LPM4	3.0V			0.02				0.3	1.2	µA
$I_{IDLE,GroupC}$	Additional idle current if one or more modules from Group C (see 表 6-3) are activated in LPM3 or LPM4	3.0V			0.02				0.38	1.5	µA
$I_{IDLE,GroupD}$	Additional idle current if one or more modules from Group D (see 表 6-3) are activated in LPM3 or LPM4	3.0V			0.015				0.25	1.0	µA

(11) Low-power mode 4 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(12) Low-power mode 4 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(13) Low-power mode 4 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

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5.8 Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	TEMPERATURE (T_A)								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT12}$ LCD, ext. bias	Low-power mode 3 (LPM3) current,12-pF crystal, LCD 4-mux mode, external biasing, excludes SVS(1) (2)	3.0 V	0.7		0.9		1.5		3.1		µA
$I_{LPM3,XT12}$ LCD, int. bias	Low-power mode 3 (LPM3) current, 12-pF crystal, LCD 4-mux mode, internal biasing, charge pump disabled, excludes SVS(1) (3)	3.0 V	2.0		2.2	2.9	2.8		4.4	9.3	µA
$I_{LPM3,XT12}$ LCD,CP	Low-power mode 3 (LPM3) current,12-pF crystal, LCD 4-mux mode, internal biasing, charge pump enabled, 1/3 bias, excludes SVS(1) (4)	2.2 V	5.0		5.2		5.8		7.4		µA
		3.0 V	4.5		4.7		5.3		6.9		

(1) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current - idle current of Group containing LCD module already included. See the idle currents specified for the respective peripheral groups.

(2) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.

(3) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ...=0, odd segments S1, S3, ... = 1. No LCD panel load.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD}= 3 V typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ...=0, odd segments S1, S3, ... = 1. No LCD panel load. C_{LCDCAP} = 10 µF

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5.9 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,XT12}$	Low-power mode 3.5, 12-pF crystal including SVS[2] [3] [4]	2.2 V	0.4		0.45		0.55		0.75		µA
		3.0 V	0.4		0.45	0.7	0.55		0.75	1.6	
$I_{LPM3.5,XT3.7}$	Low-power mode 3.5, 3.7-pF crystal excluding SVS[2] [5] [6]	2.2 V	0.3		0.35		0.4		0.65		µA
		3.0 V	0.3		0.35		0.4		0.65		
$I_{LPM4.5,SVS}$	Low-power mode 4.5, including SVS[7]	2.2 V	0.2		0.2		0.25		0.35		µA
		3.0 V	0.2		0.2	0.4	0.25		0.35	0.7	
$I_{LPM4.5}$	Low-power mode 4.5, excluding SVS[8]	2.2 V	0.02		0.02		0.03		0.14		µA
		3.0 V	0.02		0.02		0.03		0.13	0.5	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
(4) Low-power mode 3.5, 1-pF crystal including SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:
Current for RTC clocked by XT1 included.Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 4.5 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 4.5 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

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5.10 Typical Characteristics, Low-Power Mode Supply Currents

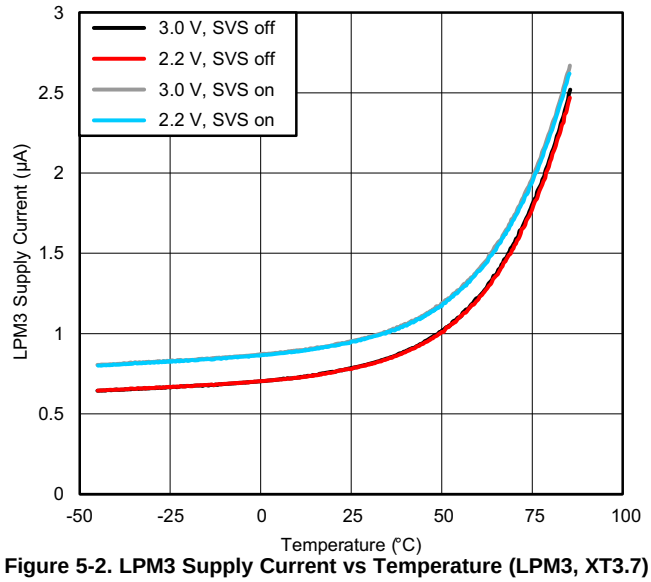

Figure 5-2. LPM3 Supply Current vs Temperature (LPM3, XT3.7)

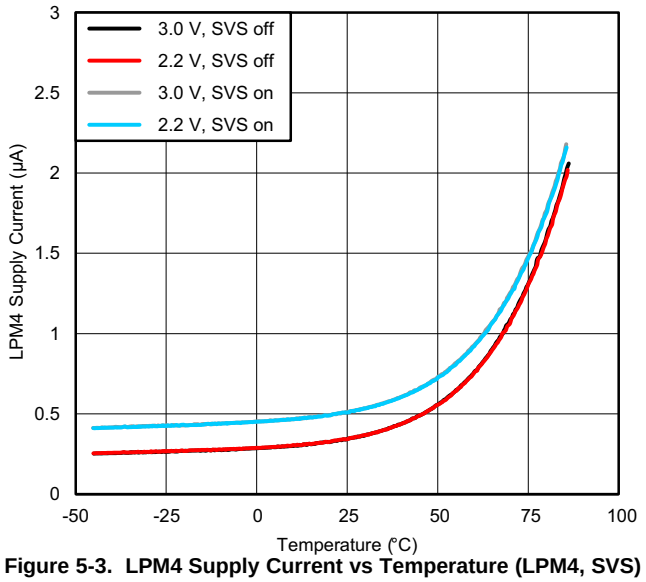

Figure 5-3. LPM4 Supply Current vs Temperature (LPM4, SVS)

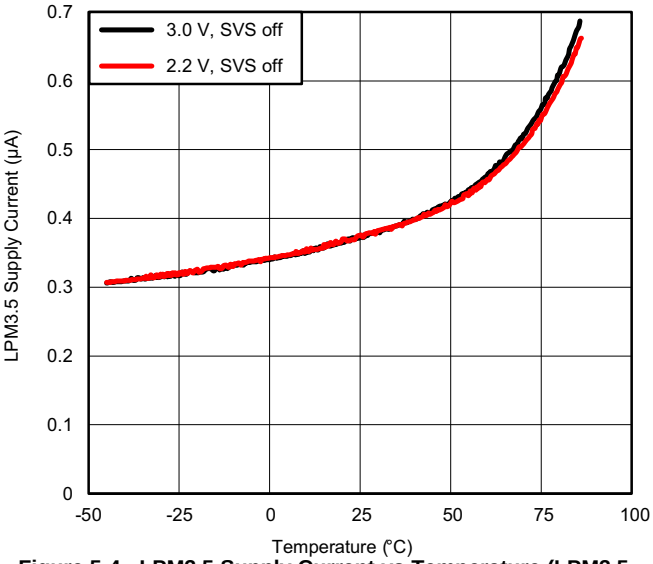

Figure 5-4. LPM3.5 Supply Current vs Temperature (LPM3.5, XT3.7)

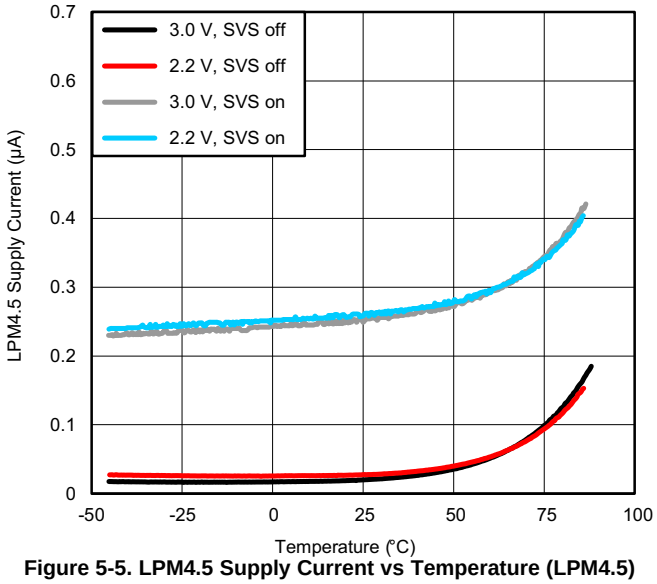

Figure 5-5. LPM4.5 Supply Current vs Temperature (LPM4.5)

5.11 Typical Characteristics, Current Consumption per Module[(1)]

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		3		µA/MHz
Timer_B		Module input clock		5		µA/MHz
eUSCI_A	UART mode	Module input clock		5.5		µA/MHz
eUSCI_A	SPI mode	Module input clock		3.5		µA/MHz
eUSCI_B	SPI mode	Module input clock		3.5		µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock		3.5		µA/MHz
RTC_C		32 kHz		100		nA
MPY	Only from start to end of operation	MCLK		25		µA/MHz
AES	Only from start to end of operation	MCLK		21		µA/MHz
CRC16	Only from start to end of operation	MCLK		2.5		µA/MHz
CRC32	Only from start to end of operation	MCLK		2.5		µA/MHz

(1) LCD_C: See Section 5.8. For other module currents not listed here, see the module-specific parameter sections.

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5.12 Thermal Resistance Characteristics

THERMAL METRIC[1]		PACKAGE	VALUE[2]	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air[3]	LQFP-100 (PZ)	49.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[4]		9.7	°C/W
θ_{JB}	Junction-to-board thermal resistance[5]		26.0	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		25.7	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[6]		N/A	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air[3]	LQFP-80 (PN)	49.5	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[4]		14.7	°C/W
θ_{JB}	Junction-to-board thermal resistance[5]		24.1	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		23.8	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.7	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[6]		N/A	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air[3]	LQFP-64 (PM)	55.3	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[4]		16.8	°C/W
θ_{JB}	Junction-to-board thermal resistance[5]		26.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		26.5	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.8	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[6]		N/A	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air[3]	VQFN-64 (RGC)	29.2	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[4]		13.9	°C/W
θ_{JB}	Junction-to-board thermal resistance[5]		8.1	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		8.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[6]		1.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) N/A = not applicable
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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5.13 Timing and Switching Characteristics

5.13.1 Power Supply Sequencing

TI recommends powering the AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

At power up, the device does not start executing code before the supply voltage reached V_{SVSH+} if the supply rises monotonically to this level.

表 5-1 lists the power ramp requirements.

表 5-1. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{VCC_BOR-}	Brownout power-down level(1)(2)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s(3)	0.7	1.66	V
		$\lvert dDV_{CC}/d_t \rvert > 300$ V/s(3)	0		
V_{VCC_BOR+}	Brownout power-up level(2)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s(4)	0.79	1.68	V

(1) In case of a supply voltage brownout, the device supply voltages must ramp down to the specified brownout power-down level (V_{VCC_BOR-}) before the voltage is ramped up again to ensure a reliable device start-up and performance according to the data sheet including the correct operation of the on-chip SVS module.
(2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
(3) The brownout levels are measured with a slowly changing supply. With faster slopes, the MIN level required to reset the device properly can decrease to 0 V. Use the graph in 図 5-6 to estimate the V_{VCC_BOR-} level based on the down slope of the supply voltage. After removing V_{CC}, the down slope can be estimated based on the current consumption and the capacitance on DVCC: dV/dt = I/C where dV/dt = slope, I = current, C = capacitance.
(4) The brownout levels are measured with a slowly changing supply.

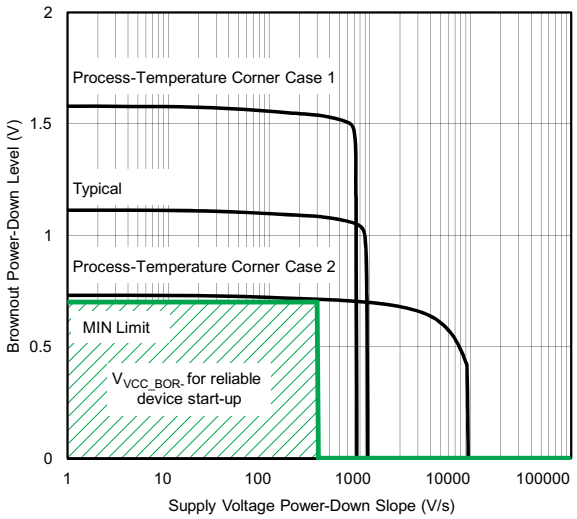

図 5-6. Brownout Power-Down Level vs Supply Voltage Down Slope

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表 5-2 lists the characteristics of the SVS.

表 5-2. SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes			170	300	nA
V_{SVSH-}	SVS_H power-down level(1)		1.75	1.80	1.85	V
V_{SVSH+}	SVS_H power-up level(1)		1.77	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis		40		120	mV
$t_{PD,SVSH,\ AM}$	SVS_H propagation delay, active mode	dV_{Vcc}/dt = –10 mV/µs			10	µs

(1) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

5.13.2 Reset Timing

Table 5-11 lists the input requirements for the $\overline{RST}$ signal.

表 5-3. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$(1)	2.2 V, 3.0 V	2		µs

(1) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

5.13.3 Clock Specifications

Table 5-4 lists the characteristics of the LFXT.

Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC.LFXT}$	Current consumption	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF, ESR ≈ 44 kΩ	3.0 V		180		nA
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, T_A = 25°C, $C_{L,eff}$ = 6 pF, ESR ≈ 40 kΩ			185		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 9 pF, ESR ≈ 40 kΩ			225		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF, ESR ≈ 40 kΩ			330		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0			32768		Hz
DC_{LFXT}	LFXT oscillator duty cycle	Measured at ACLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(2) (3)		10.5	32.768	50	kHz
$DC_{LFXT, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals(4)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			300		
C_{LFXIN}	Integrated load capacitance at LFXIN terminal(5) (6)				2		pF
C_{LFXOUT}	Integrated load capacitance at LFXOUT terminal(5) (6)				2		pF

(1) To improve EMI on the LFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
- Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {3}, 9 pF ≤ $C_{L,eff}$ ≤ 12.5 pF

(5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} are the total capacitance at the LFXIN and LFXOUT terminals, respectively.

(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

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Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,LFXT}$	Start-up time(7)	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF	3.0 V		800		ms
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF	3.0 V		1000		
$f_{Fault,LFXT}$	Oscillator fault frequency(8) (9)			0		3500	Hz

(7) Includes start-up counter of 1024 clock cycles.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the HFXT.

Table 5-5. High-Frequency Crystal Oscillator, HFXT(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1(2) T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}	3.0 V		75		µA
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			120		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			190		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			250		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1(2)(3)		4		8	MHz
		HFXTBYPASS = 0, HFFREQ = 2(3)		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3(3)		16.01		24	
DC_{HFXT}	HFXT oscillator duty cycle	Measured at SMCLK, f_{HFXT} = 16 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0(4)(3)		0.9		4	MHz
		HFXTBYPASS = 1, HFFREQ = 1(4)(3)		4.01		8	
		HFXTBYPASS = 1, HFFREQ = 2(4)(3)		8.01		16	
		HFXTBYPASS = 1, HFFREQ = 3(4)(3)		16.01		24	
$DC_{HFXT, SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1		40%		60%	

(1) To improve EMI on the HFXT oscillator, observe the following guidelines.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.

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Table 5-5. High-Frequency Crystal Oscillator, HFXT[1] (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,HFXT}$	Start-up time[5]	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		1.6		ms
		f_{OSC} = 24 MHz , HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		0.6		
C_{HFXIN}	Integrated load capacitance at HFXIN terminal[6] [7]				2		pF
C_{HFXOUT}	Integrated load capacitance at HFXOUT terminal[6] [7]				2		pF
$f_{Fault,HFXT}$	Oscillator fault frequency[8] [9]			0		800	kHz

(5) Includes start-up counter of 1024 clock cycles.
(6) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} are the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0			1	±3.5%	MHz
$f_{DCO2.7}$	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1			2.667	±3.5%	MHz
$f_{DCO3.5}$	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2			3.5	±3.5%	MHz
f_{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3			4	±3.5%	MHz
$f_{DCO5.3}$	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1			5.333	±3.5%	MHz
f_{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2			7	±3.5%	MHz
f_{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3			8	±3.5%	MHz
f_{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4			16	±3.5%(1)	MHz
f_{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5			21	±3.5%(1)	MHz
f_{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6			24	±3.5%(1)	MHz
$f_{DCO,DC}$	Duty cycle	Measured at SMCLK, divide by 1, no external divide, all DCORSEL/DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6		48%	50%	52%	
$t_{DCO,\ JITTER}$	DCO jitter	Based on f_{signal} = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74 dB SNR due to jitter (that is, it is limited by ADC performance).			2	3	ns
df_{DCO}/dT	DCO temperature drift(2)		3.0 V		0.01		%/ºC

(1) After a wakeup from LPM1, LPM2, LPM3, or LPM4, the DCO frequency f_{DCO} might exceed the specified frequency range for a few clock cycles by up to 5% before settling into the specified steady-state frequency range.
(2) Calculated using the box method: (MAX(–40ºC to 85ºC) – MIN(–40ºC to 85ºC)) / MIN(–40ºC to 85ºC) / (85ºC – (–40ºC))

Table 5-7 lists the characteristics of the VLO.

Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption			100		nA
f_{VLO}	VLO frequency	Measured at ACLK	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)		0.2		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)		0.7		%/V
$f_{VLO,DC}$	Duty cycle	Measured at ACLK	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

Table 5-8. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled		25		µA
f_{MODOSC}	MODOSC frequency		4.0	4.8	5.4	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift (1)			0.08		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift (2)			1.4		%/V
DC_{MODOSC}	Duty cycle	Measured at SMCLK, divide by 1	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

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5.13.4 Wake-up Characteristics

Table 5-9 lists the wake-up times.

Table 5-9. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wakeup				6	10	µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		2.2 V, 3.0 V			400 + 1.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM1}$	Wake-up time from LPM1 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM2}$	Wake-up time from LPM2 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (1)		2.2 V, 3.0 V		7	10	µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode (1)		2.2 V, 3.0 V		7	10	µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		2.2 V, 3.0 V		250	375	µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	2.2 V, 3.0 V		250	375	µs
		SVSHE = 0	2.2 V, 3.0 V		1	1.5	ms
$t_{WAKE-UP-RST}$	Wake-up time from a $\overline{RST}$ pin triggered reset to active mode (2)		2.2 V, 3.0 V		250	375	µs
$t_{WAKE-UP-BOR}$	Wake-up time from power-up to active mode (2)		2.2 V, 3.0 V		1	1.5	ms

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge. MCLK is sourced by the DCO and the MCLK divider is set to divide-by-1 (DIVMx = 000b, $f_{MCLK} = f_{DCO}$). This time includes the activation of the FRAM during wakeup.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10 lists the typical charge consumed during wakeup from various low-power modes.

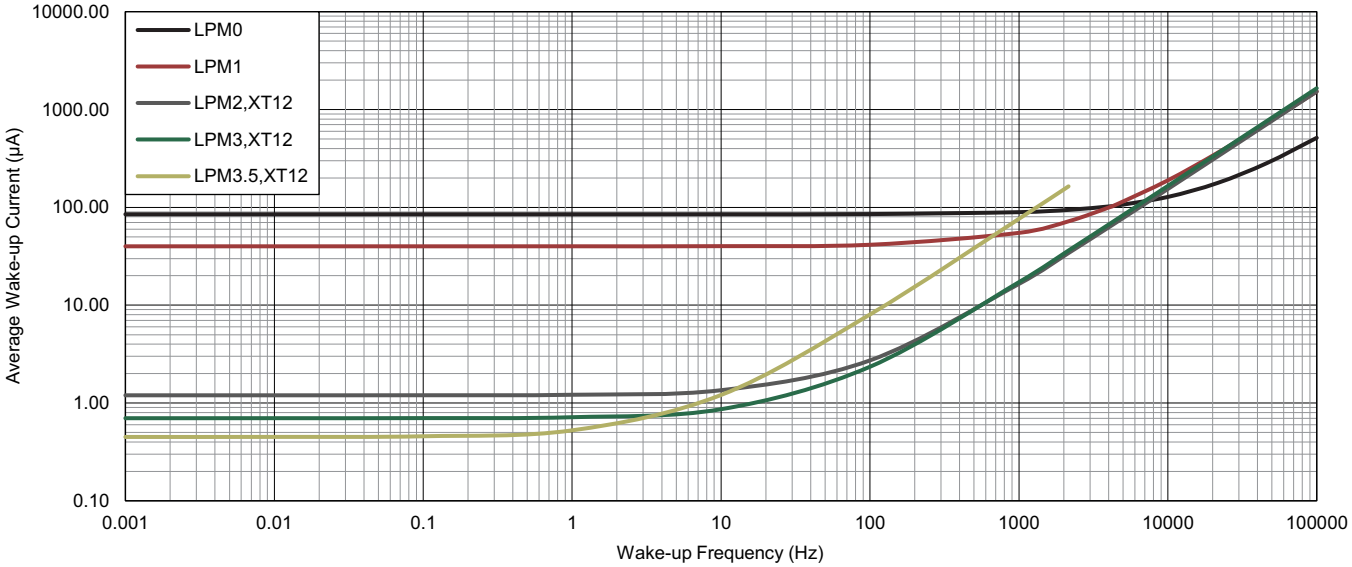
Table 5-10. Typical Wake-up Charge (1)

also see Figure 5-7 and Figure 5-8

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Q_{WAKE-UP\ FRAM}$	Charge used for activating the FRAM in AM or during wake-up from LPM0 if previously disabled by the FRAM controller.			15.1		nAs
$Q_{WAKE-UP\ LPM0}$	Charge used for wake-up from LPM0 to active mode (with FRAM active)			4.4		nAs
$Q_{WAKE-UP\ LPM1}$	Charge used for wake-up from LPM1 to active mode (with FRAM active)			15.1		nAs
$Q_{WAKE-UP\ LPM2}$	Charge used for wake-up from LPM2 to active mode (with FRAM active)			15.3		nAs
$Q_{WAKE-UP\ LPM3}$	Charge used for wake-up from LPM3 to active mode (with FRAM active)			16.5		nAs
$Q_{WAKE-UP\ LPM4}$	Charge used for wake-up from LPM4 to active mode (with FRAM active)			16.5		nAs
$Q_{WAKE-UP\ LPM3.5}$	Charge used for wake-up from LPM3.5 to active mode (2)			76		nAs
$Q_{WAKE-UP\ LPM4.5}$	Charge used for wake-up from LPM4.5 to active mode (2)	SVSHE = 1		77		nAs
		SVSHE = 0		77.5		
$Q_{WAKE-UP-RESET}$	Charge used for reset from $\overline{RST}$ or BOR event to active mode (2)			75		nAs

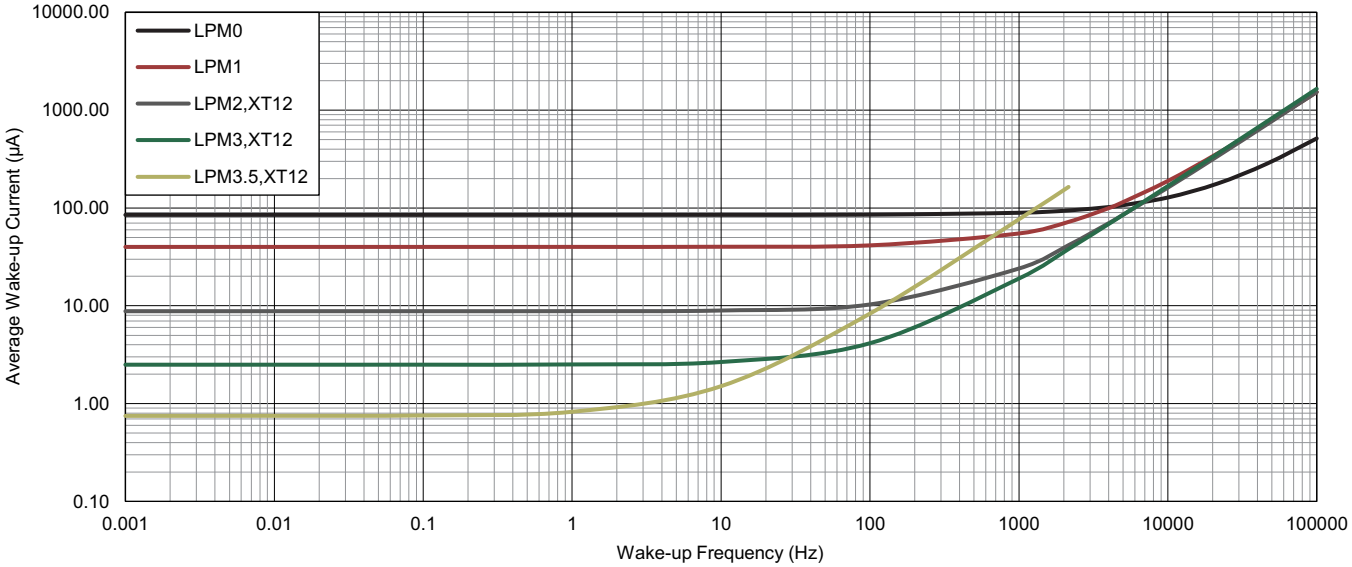
(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).
(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

5.13.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-7. Average LPM Currents vs Wake-up Frequency at 25°C



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-8. Average LPM Currents vs Wake-up Frequency at 85°C

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5.13.5 Peripherals

5.13.5.1 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

Table 5-11. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	1.2		1.65	V
			3.0 V	1.65		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.00	V
			3.0 V	0.75		1.35	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2.2 V	0.44		0.98	V
			3.0 V	0.60		1.30	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions (1)	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance input leakage current	See (2) (3)	2.2 V, 3.0 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag) (4)	Ports with interrupt capability (see 1.4 and Section 4.2)	2.2 V, 3.0 V	20			ns
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$ (5)		2.2 V, 3.0 V	2			µs

(1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN or PJ.5/LFXOUT.
(2) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It might be set by trigger signals shorter than $t_{(int)}$.
(5) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

Table 5-12 lists the characteristics of the digital outputs.

Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-9, Figure 5-10, Figure 5-11, and Figure 5-12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA (1)	2.2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3 mA (2)		V_{CC} – 0.60		V_{CC}	
		$I_{(OHmax)}$ = –2 mA (1)	3.0 V	V_{CC} – 0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA (2)		V_{CC} – 0.60		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA (1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA (2)		V_{SS}		V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA (1)	3.0 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)		V_{SS}		V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with load) (3)	C_L = 20 pF, R_L (4) (5)	2.2 V	16			MHz
			3.0 V	16			
f_{Port_CLK}	Clock output frequency (3)	ACLK, MCLK, or SMCLK at configured output port, C_L = 20 pF (5)	2.2 V	16			MHz
			3.0 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit - it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
(5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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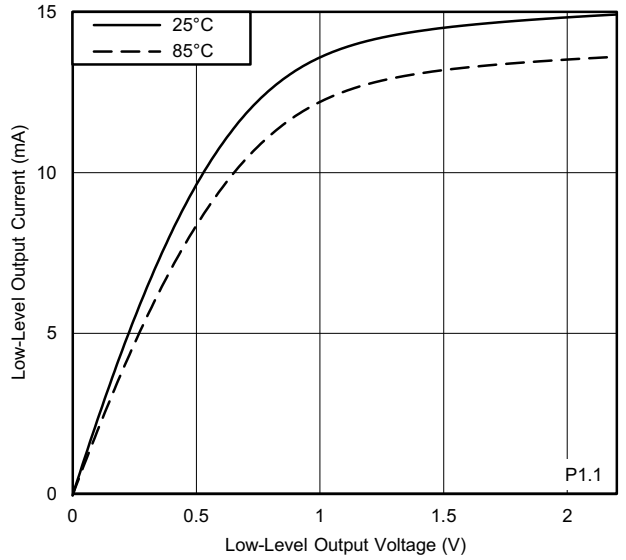
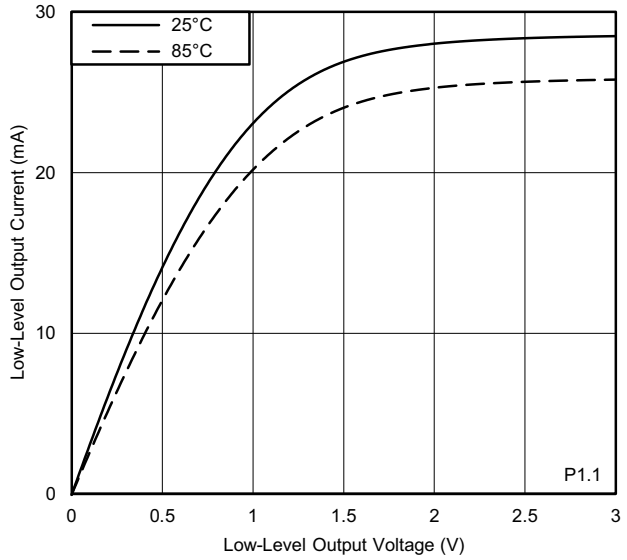
5.13.5.1.1 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V



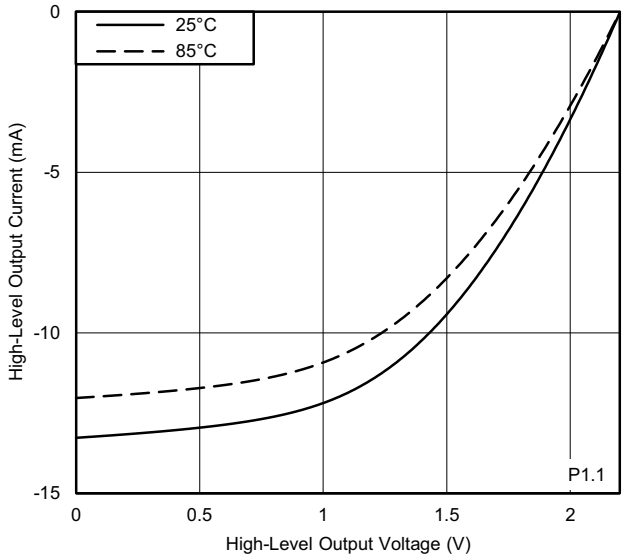
V_{CC} = 2.2 V

Figure 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage



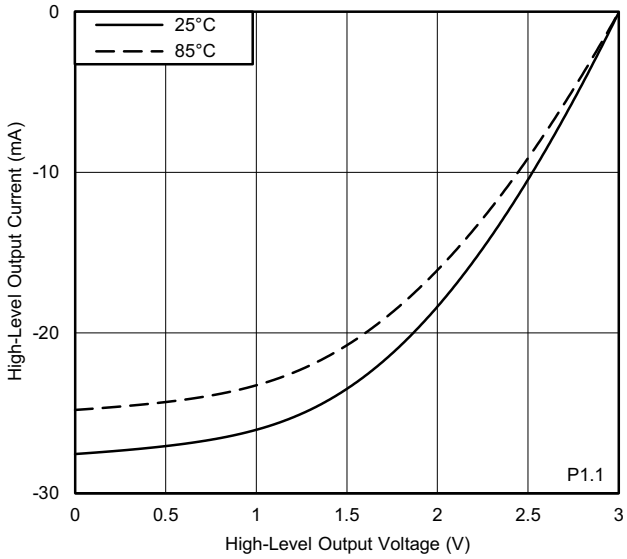
V_{CC} = 3.0 V

Figure 5-10. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.2 V

Figure 5-11. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3.0 V

Figure 5-12. Typical High-Level Output Current vs High-Level Output Voltage

Table 5-13 lists the frequencies of the pin oscillator.

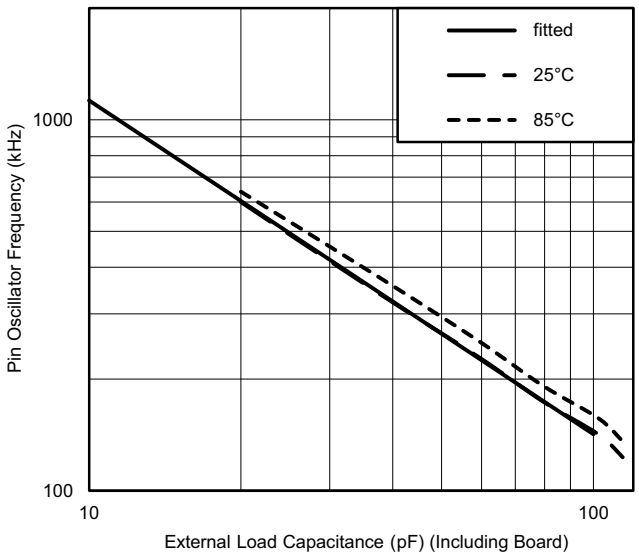
Table 5-13. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-13 and Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{Px.y}$	Pin-oscillator frequency	Px.y, C_L = 10 pF(1)	3.0 V		1200		kHz
		Px.y, C_L = 20 pF(1)			650		

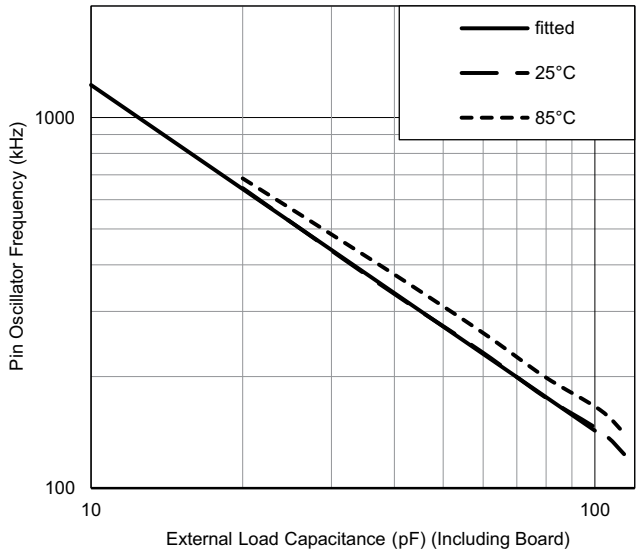
(1) C_L is the external load capacitance connected from the output to V_{SS} and includes all parasitic effects such as PCB traces.

5.13.5.1.2 Typical Characteristics, Pin-Oscillator Frequency



V_{CC} = 2.2 V One output active at a time.

Figure 5-13. Typical Oscillation Frequency vs Load Capacitance



V_{CC} = 3.0 V One output active at a time.

Figure 5-14. Typical Oscillation Frequency vs Load Capacitance

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5.13.5.2 Timer_A and Timer_B

Table 5-14 lists the characteristics of the Timer_A.

Table 5-14. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Table 5-15 lists the characteristics of the Timer_B.

Table 5-15. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

5.13.5.3 eUSCI

Table 5-16 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-16. eUSCI (UART Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

Table 5-17 lists the characteristics of the eUSCI in UART mode.

Table 5-17. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2.2 V, 3.0 V	5		30	ns
		UCGLITx = 1		20		90	
		UCGLITx = 2		35		160	
		UCGLITx = 3		50		220	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-18. eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		16	MHz

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Table 5-19 lists the characteristics of the eUSCI in SPI master mode.

Table 5-19. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1			UCxCLK cycles
$t_{STE,LAG}$	STE lag time, last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1			UCxCLK cycles
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			60	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			80	ns
$t_{SU,MI}$	SOMI input data setup time		2.2 V	40			ns
			3.0 V	40			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3.0 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			10	ns
			3.0 V			10	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V		0		ns
			3.0 V		0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-15 and Figure 5-16.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-15 and Figure 5-16.

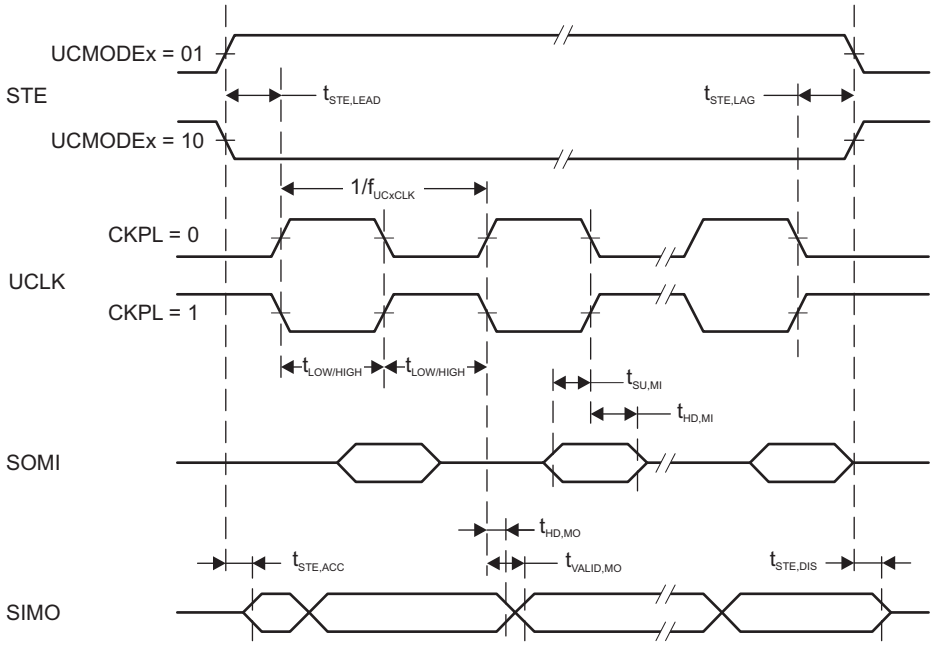

Figure 5-15. SPI Master Mode, CKPH = 0

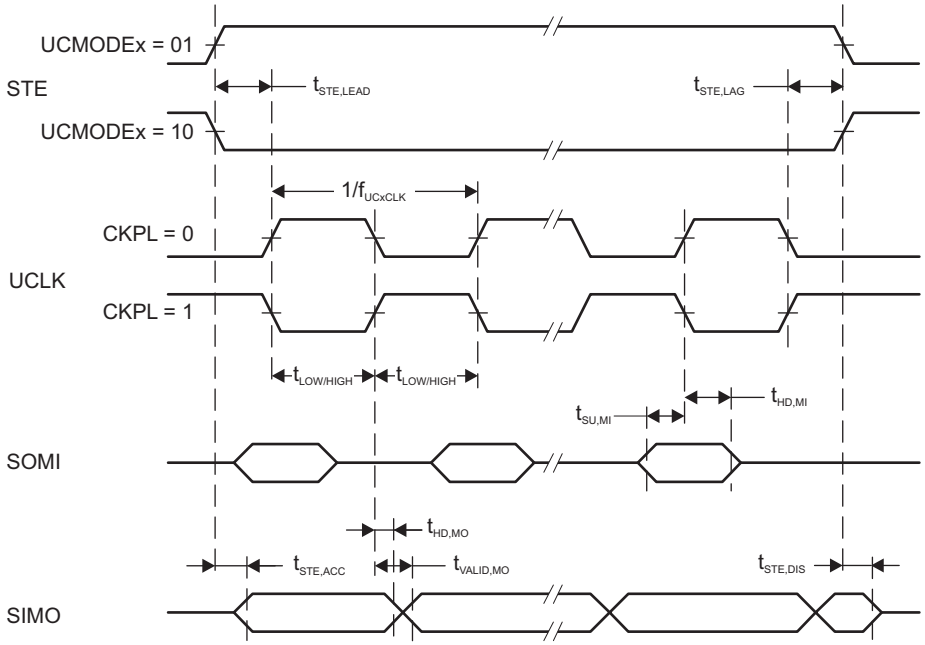

Figure 5-16. SPI Master Mode, CKPH = 1

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Table 5-20 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-20. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.2 V	45		ns
			3.0 V	40		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2.2 V	2		ns
			3.0 V	3		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.2 V		45	ns
			3.0 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.2 V		50	ns
			3.0 V		45	
$t_{SU,SI}$	SIMO input data setup time		2.2 V	4		ns
			3.0 V	4		
$t_{HD,SI}$	SIMO input data hold time		2.2 V	7		ns
			3.0 V	7		
$t_{VALID,SO}$	SOMI output data valid time[2]	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		35	ns
			3.0 V		35	
$t_{HD,SO}$	SOMI output data hold time[3]	C_L = 20 pF	2.2 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-17 and Figure 5-18.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams inFigure 5-17 and Figure 5-18.

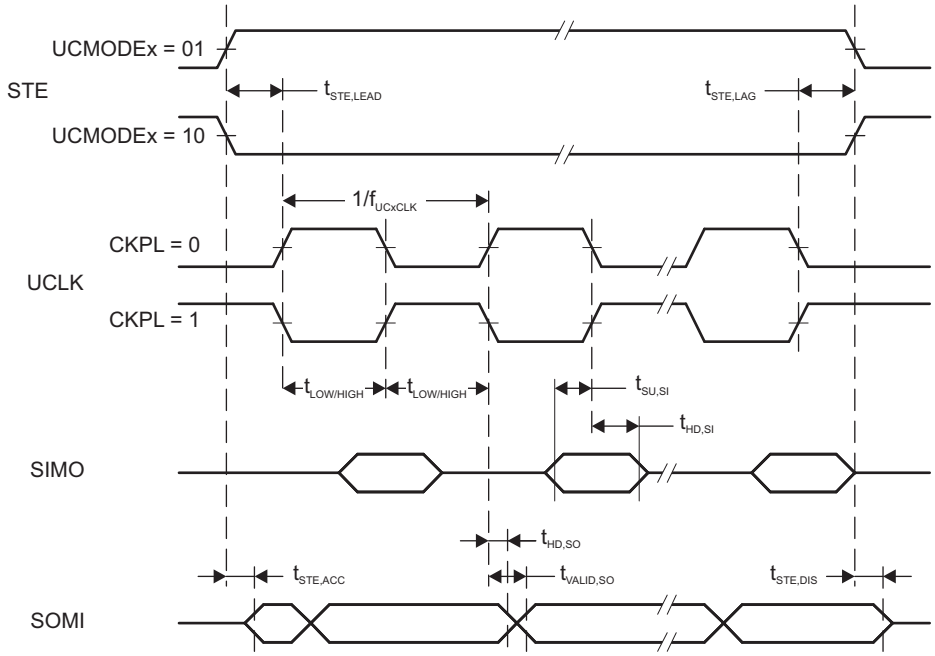

Figure 5-17. SPI Slave Mode, CKPH = 0

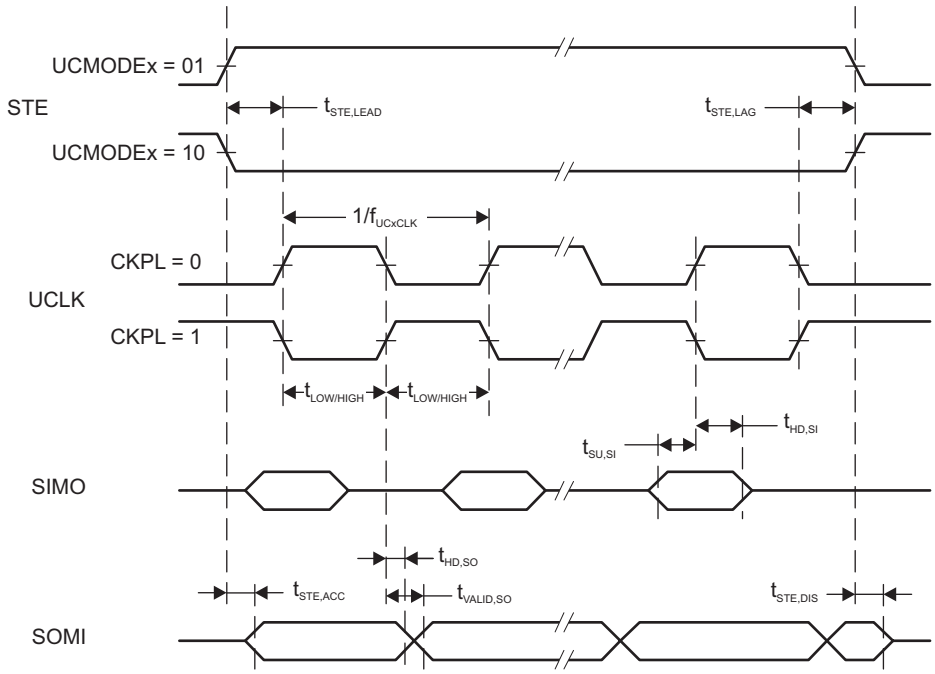

Figure 5-18. SPI Slave Mode, CKPH = 1

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Table 5-21 lists the characteristics of the eUSCI in I²C mode.

Table 5-21. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3.0 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3.0 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3.0 V	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100 kHz		4.7			µs
		f_{SCL} > 100 kHz		1.3			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3.0 V	50		250	ns
		UCGLITx = 1		25		125	
		UCGLITx = 2		12.5		62.5	
		UCGLITx = 3		6.3		31.5	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2.2 V, 3.0 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

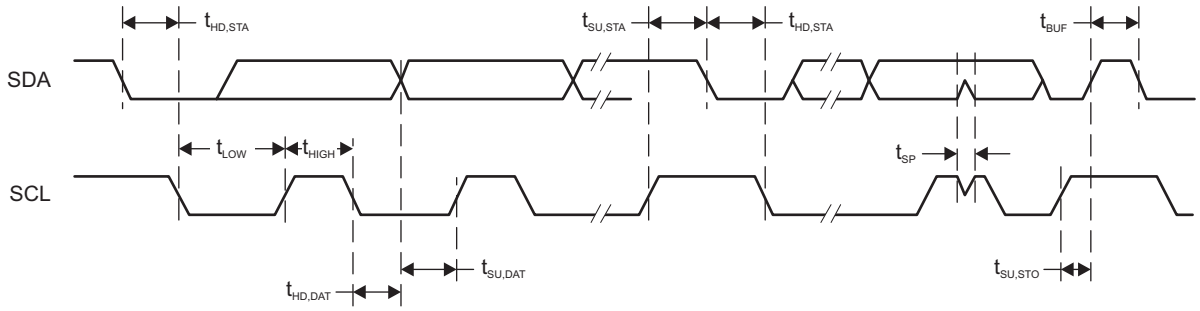

Figure 5-19. I²C Mode Timing

5.13.5.4 LCD Controller

Table 5-22 lists the operating conditions of the LCD_C.

Table 5-22. LCD_C, Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{CC,LCD_C,CP\ en,3.6}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.6 V	LCDCPEN = 1, 0000b < VLCDx ≤ 1111b (charge pump enabled, V_{LCD} ≤ 3.6 V)	2.2		3.6	V
$V_{CC,LCD_C,CP\ en,3.3}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.3 V	LCDCPEN = 1, 0000b < VLCDx ≤ 1100b (charge pump enabled, V_{LCD} ≤ 3.3 V)	2.0		3.6	V
$V_{CC,LCD_C,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD_C,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD_C,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.0		3.6	V
V_{LCDCAP}	External LCD voltage at LCDCAP, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.4		3.6	V
C_{LCDCAP}	Capacitor value on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000b (charge pump enabled)	$4.7_{-20\%}$	4.7	$10_{+20\%}$	µF
$f_{ACLK,in}$	ACLK input frequency range		30	32.768	40	kHz
f_{LCD}	LCD frequency range	f_{FRAME} = 1/(2 × mux) × f_{LCD} with mux = 1 (static) to 8	0		1024	Hz
$f_{FRAME,4mux}$	LCD frame frequency range	$f_{FRAME,4mux}$(MAX) = 1/(2 × 4) × f_{LCD}(MAX) = 1/(2 × 4) × 1024 Hz			128	Hz
$f_{FRAME,8mux}$	LCD frame frequency range	$f_{FRAME,8mux}$(MAX) = 1/(2 × 4) × f_{LCD}(MAX) = 1/(2 × 8) × 1024 Hz			64	Hz
C_{Panel}	Panel capacitance	f_{LCD} = 1024 Hz, all common lines equally loaded			10000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT = 1	2.4		V_{CC}+0.2	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	V_{R03} + 2/3 × (V_{R33}-V_{R03})	V_{R33}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	V_{R03} + 1/3 × (V_{R33} – V_{R03})	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1	V_{R03}	V_{R03} + 1/2 × (V_{R33} – V_{R03})	V_{R33}	V
V_{R03}	Analog input voltage at R03	R0EXT = 1	V_{SS}			V
V_{LCD}-V_{R03}	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT = 1	2.4		V_{CC}+0.2	V
V_{LCDREF}	External LCD reference voltage applied at LCDREF	VLCDREFx = 01	0.8	1.0	1.2	V

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Table 5-23 lists the characteristics of the LCD_C.

Table 5-23. LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{LCD,0}$	LCD voltage	VLCDx = 0000, VLCDEXT = 0	2.4 V to 3.6 V		V_{CC}		V
$V_{LCD,1}$		LCDCPEN = 1, VLCDx = 0001b	2 V to 3.6 V	2.49	2.60	2.72	
$V_{LCD,2}$		LCDCPEN = 1, VLCDx = 0010b	2 V to 3.6 V		2.66		
$V_{LCD,3}$		LCDCPEN = 1, VLCDx = 0011b	2 V to 3.6 V		2.72		
$V_{LCD,4}$		LCDCPEN = 1, VLCDx = 0100b	2 V to 3.6 V		2.78		
$V_{LCD,5}$		LCDCPEN = 1, VLCDx = 0101b	2 V to 3.6 V		2.84		
$V_{LCD,6}$		LCDCPEN = 1, VLCDx = 0110b	2 V to 3.6 V		2.90		
$V_{LCD,7}$		LCDCPEN = 1, VLCDx = 0111b	2 V to 3.6 V		2.96		
$V_{LCD,8}$		LCDCPEN = 1, VLCDx = 1000b	2 V to 3.6 V		3.02		
$V_{LCD,9}$		LCDCPEN = 1, VLCDx = 1001b	2 V to 3.6 V		3.08		
$V_{LCD,10}$		LCDCPEN = 1, VLCDx = 1010b	2 V to 3.6 V		3.14		
$V_{LCD,11}$		LCDCPEN = 1, VLCDx = 1011b	2 V to 3.6 V		3.20		
$V_{LCD,12}$		LCDCPEN = 1, VLCDx = 1100b	2 V to 3.6 V		3.26		
$V_{LCD,13}$		LCDCPEN = 1, VLCDx = 1101b	2.2 V to 3.6 V		3.32		
$V_{LCD,14}$		LCDCPEN = 1, VLCDx = 1110b	2.2 V to 3.6 V		3.38		
$V_{LCD,15}$		LCDCPEN = 1, VLCDx = 1111b	2.2 V to 3.6 V	3.32	3.44	3.6	
$V_{LCD,7,0.8}$	LCD voltage with external reference of 0.8 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 0.8 V	2 V to 3.6 V		2.96 × 0.8 V		V
$V_{LCD,7,1.0}$	LCD voltage with external reference of 1.0 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 1.0 V	2 V to 3.6 V		2.96 × 1.0 V		V
$V_{LCD,7,1.2}$	LCD voltage with external reference of 1.2 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 1.2 V	2.2 V to 3.6 V		2.96 × 1.2 V		V
ΔV_{LCD}	Voltage difference between consecutive VLCDx settings	$\Delta V_{LCD} = V_{LCD,x} - V_{LCD,x-1}$ with x = 0010b to 1111b		40	60	80	mV
$I_{CC,Peak,CP}$	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111b external, with decoupling capacitor on DVCC supply ≥ 1 µF	2.2 V		600		µA
$t_{LCD,CP,on}$	Time to charge C_{LCD} when discharged	C_{LCD} = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111b	2.2 V		100	500	ms
$I_{CP,Load}$	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111b	2.2 V	50			µA
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	LCDCPEN = 0, I_{LOAD} = ±10 µA	2.2 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	LCDCPEN = 0, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

5.13.5.5 ADC

表 5-24 lists the input requirements of the ADC.

表 5-24. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{(Ax)}$	Analog input voltage range(1)	All ADC12 analog input pins Ax		0		AVCC	V
$I_{(ADC12_B)}$ single-ended mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		145	199	µA
			2.2 V		140	190	
$I_{(ADC12_B)}$ differential mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx= 0, ADC12DIV = 0	3.0 V		175	245	µA
			2.2 V		170	230	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		10	15	pF
R_I	Input MUX ON resistance	0 V ≤ $V_{(Ax)}$ ≤ AVCC	>2 V		0.5	4	kΩ
			<2 V		1	10	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter $I_{(ADC12_B)}$.
(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminals is from AVCC.

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Table 5-25 lists the timing parameters of the ADC.

Table 5-25. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	Frequency for specified performance	For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0. If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here.		0.45		5.4	MHz
$f_{ADC12CLK}$	Frequency for reduced performance	Linearity parameters have reduced performance			32.768		kHz
$f_{ADC12OSC}$	Internal oscillator(1)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK		4	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK, ADC12WINC = 0		2.6		3.5	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			See (2)		
$t_{ADC12ON}$	Turnon settling time of the ADC	See (3)				100	ns
$t_{ADC12OFF}$	Time ADC must be off before it can be turned on again	$t_{ADC12OFF}$ must be met to make sure that $t_{ADC12ON}$ time holds.		100			ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 4 kΩ, C_I = 15 pF, C_{pext}= 8 pF(4)	All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF)	1			µs
			Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12VRSEL= 0x0, 0x2, 0x4, 0x6, 0xC, 0xE)	See (5)			µs

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(2) 14 × 1 / $f_{ADC12CLK}$. If ADC12WINC = 1, then 15 × 1 / $f_{ADC12CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB: $t_{sample} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{pext})$, $R_S < 10$ kΩ, where n = ADC resolution = 12, R_S= external source resistance, C_{pext} = external parasitic capacitance.
(5) 6 × 1 / $f_{ADC12CLK}$

Table 5-26 lists the linearity parameters of the ADC when using an external reference.

Table 5-26. 12-Bit ADC, Linearity Parameters With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
E_I	Integral linearity error (INL) for differential input	$1.2\ V \le V_{R+} - V_{R-} \le AV_{CC}$			±1.8	LSB
E_I	Integral linearity error (INL) for single ended inputs	$1.2\ V \le V_{R+} - V_{R-} \le AV_{CC}$			±2.2	LSB
E_D	Differential linearity error (DNL)		–0.99		+1.0	LSB
E_O	Offset error(2) (3)	ADC12VRSEL = 0x2 or 0x4 without TLV calibration, TLV calibration data can be used to improve the parameter(4)		±0.5	±1.5	mV
$E_{G,ext}$	Gain error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), V_{R+} = 2.5 V, V_{R-} = AVSS		±0.8	±2.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±1	±20	
$E_{T,ext}$	Total unadjusted error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), V_{R+} = 2.5 V, V_{R-} = AVSS		±1.4	±3.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±1.4	±21.0	

(1) See Table 5-28 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.
(3) Offset increases as I_R drop increases when V_{R-} is AVSS.
(4) For details, see the device descriptor in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

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Table 5-27 lists the dynamic performance characteristics of the ADC with differential inputs and an external reference.

Table 5-27. 12-Bit ADC, Dynamic Performance for Differential Inputs With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise	V_{R+} = 2.5 V, V_{R-} = AVSS	68	71		dB
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.7	11.2		bits

(1) See Table 5-28 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-28 lists the dynamic performance characteristics of the ADC with differential inputs and an internal reference.

Table 5-28. 12-Bit ADC, Dynamic Performance for Differential Inputs With Internal Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.3	10.7		Bits

(1) See Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-29 lists the dynamic performance characteristics of the ADC with single-ended inputs and an external reference.

Table 5-29. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise	V_{R+} = 2.5 V, V_{R-} = AVSS	64	68		dB
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.2	10.7		bits

(1) See Table 5-30 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-30 lists the dynamic performance characteristics of the ADC with single-ended inputs and an internal reference.

Table 5-30. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With Internal Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	9.4	10.4		bits

(1) See Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-31 lists the dynamic performance characteristics of the ADC using a 32.678-kHz clock.

Table 5-31. 12-Bit ADC, Dynamic Performance With 32.768-kHz Clock

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
ENOB	Effective number of bits(1)	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, V_{R+} = 2.5 V, V_{R-} = AVSS	10	bits

(1) ENOB = (SINAD – 1.76) / 6.02

Table 5-32 lists the characteristics of the temperature sensor and built-in $V_{1/2}$ of the ADC.

Table 5-32. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1) (2) (also see Figure 5-20)	ADC12ON = 1, ADC12TCMAP = 1, T_A = 0°C		700		mV
TC_{SENSOR}	See (2)	ADC12ON = 1, ADC12TCMAP = 1		2.5		mV/°C
$t_{SENSOR(sample)}$	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected(3)	ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤ 1 LSB	30			µs
$V_{1/2}$	AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel	ADC12ON = 1, ADC12BATMAP = 1	47.5%	50%	52.5%	
$I_{V\ 1/2}$	Current for battery monitor during sample time	ADC12ON = 1, ADC12BATMAP = 1		38	63	µA
$t_{V\ 1/2\ (sample)}$	Sample time required if ADC12BATMAP = 1 and channel MAX is selected(4)	ADC12ON = 1, ADC12BATMAP = 1	1.7			µs

(1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times$ (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V1/2(sample)}$; no additional on time is needed.

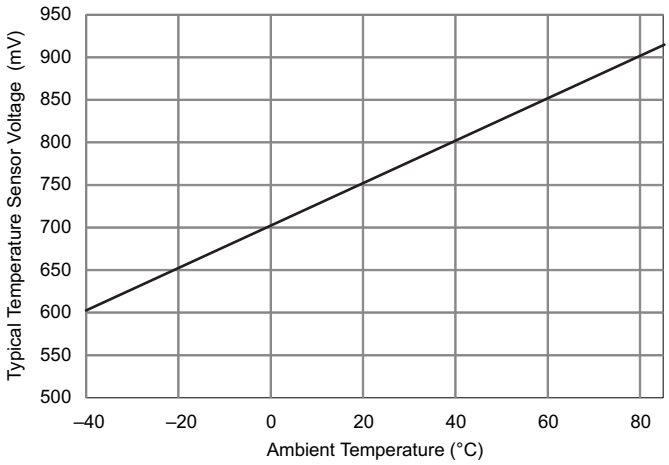

Figure 5-20. Typical Temperature Sensor Voltage

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Table 5-33 lists the external reference requirements for the ADC.

Table 5-33. 12-Bit ADC, External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R+}	Positive external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
V_{R-}	Negative external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	0		1.2	V
$V_{R+} - V_{R-}$	Differential external reference voltage input	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
I_{VeREF+}, I_{VeREF-}	Static input current, singled-ended input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 0, ADC12PWRMD = 0			±10	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 0, ADC12PWRMD = 01			±2.5	
I_{VeREF+}, I_{VeREF-}	Static input current, differential input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 1, ADC12PWRMD = 0			±20	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 1, ADC12PWRMD = 1			±5	
I_{VeREF+}	Peak input current with single-ended input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 0			1.5	mA
I_{VeREF+}	Peak input current with differential input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 1			3	mA
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	See (2)	10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

(2) Connect two decoupling capacitors, 10 µF and 470 nF, to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. Also see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

5.13.5.6 Reference

Table 5-34 lists the characteristics of the built-in voltage reference.

Table 5-34. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V		2.0	±1.5%	
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V		1.2	±1.8%	
Noise	RMS noise at VREF(1)	From 0.1 Hz to 10 Hz, REFVSEL = {0}			110	600	µV
$V_{OS_BUF_INT}$	VREF ADC BUF_INT buffer offset(2)	T_A = 25°C , ADC ON, REFVSEL = {0}, REFON = 1, REFOUT = 0		–12		+12	mV
$V_{OS_BUF_EXT}$	VREF ADC BUF_EXT buffer offset(2)	T_A = 25°C, REFVSEL = {0} , REFOUT = 1, REFON = 1 or ADC ON		–12		+12	mV
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal(3)	REFON = 1	3 V		8	15	µA
$I_{REF+_ADC_BUF}$	Operating supply current into AVCC terminal(3)	ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0,	3 V		225	355	µA
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0			1030	1660	
		ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			120	185	
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			545	895	
		ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}			1085	1780	
$I_{O(VREF+)}$	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1		–1000		+10	µA
ΔVout/ΔIo (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or –1000 µA, AV_{CC} = $AV_{CC(min)}$ for each reference level, REFON = REFOUT = 1				2500	µV/mA
$C_{VREF+/-}$	Capacitance at VREF+ and VREF- terminals	REFON = REFOUT = 1		0		100	pF
TC_{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T_A = –40°C to 85°C(4)			18	50	ppm/K
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC(min)}$ to $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1			120	400	µV/V
PSRR_AC	Power supply rejection ratio (AC)	dAV_{CC}= 0.1 V at 1 kHz			3.0		mV/V
t_{SETTLE}	Settling time of reference voltage(5)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1			75	80	µs

(1) Internal reference noise affects ADC performance when ADC uses internal reference. See *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal versus external reference.
(2) Buffer offset affects ADC gain error and thus total unadjusted error.
(3) The internal reference current is supplied through the AVCC terminal.
(4) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(5) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

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5.13.5.7 Comparator

Table 5-35 lists the characteristics of the comparator.

Table 5-35. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{AVCC_COMP}	Comparator operating supply current into AVCC, excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3.0 V		11	20	µA
		CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)			9	17	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 30°C				0.5	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 85°C				1.3	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, including REF module current	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 0	2.2 V, 3.0 V		12	15	µA
		CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 1			5	7	
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.8 V	1.17	1.2	1.23	V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.92	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.8 V	1.10	1.2	1.245	
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.90	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.35	2.5	2.60	
V_{IC}	Common-mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CEPWRMD = 00		–32		32	mV
		CEPWRMD = 01		–32		32	
		CEPWRMD = 10		–30		30	
C_{IN}	Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			9		pF
		CEPWRMD = 10			9		
R_{SIN}	Series input resistance	On (switch closed)			1	3	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			260	330	ns
		CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			350	460	
		CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV				15	µs
$t_{PD,filter}$	Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			700	1000	ns
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.0	1.8	µs
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2.0	3.5	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4.0	7.0	
t_{EN_CMP}	Comparator enable time	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00			0.9	1.5	µs
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01			0.9	1.5	
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10			15	100	
$t_{EN_CMP_VREF}$	Comparator and reference ladder and reference voltage enable time	CEON = 0 → 1, CEREFLX = 10, CERSx = 10 or 11, CEREF0 = CEREF1 = 0x0F, Overdrive ≥ 20 mV			350	1500	µs
V_{CE_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.13.5.8 FRAM Controller

Table 5-36 lists the characteristics of the FRAM.

Table 5-36. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J = 70°C	40			
		T_J = 85°C	10			
I_{WRITE}	Current to write into FRAM		I_{READ} (1)			nA
I_{ERASE}	Erase current		n/a (2)			nA
t_{WRITE}	Write time		t_{READ} (3)			ns
t_{READ}	Read time	NWAITSx = 0	1 / f_{SYSTEM} (4)			ns
		NWAITSx = 1	2 / f_{SYSTEM} (4)			

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption numbers $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.13.6 Emulation and Debug

Table 5-37 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

Table 5-37. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{JTAG}	Supply current adder when JTAG active (but not clocked)	2.2 V, 3.0 V		40	100	µA
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3.0 V			110	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2.2 V	0		16	MHz
		3.0 V	0		16	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f_{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f_{SYSTEM})				16	MHz
$t_{TCLK,Low/High}$	TCLK low or high clock pulse duration, no FRAM access				25	ns
$f_{TCLK,FRAM}$	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f_{SYSTEM} with no FRAM wait states)				4	MHz
$t_{TCLK,FRAM,Low/High}$	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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6 Detailed Description

6.1 Overview

The TI MSP430FR697x and MSP430FR692x families of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes, is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430FR697x devices are microcontroller configurations with up to five 16-bit timers, Comparator, eUSCIs that support UART, SPI, and I^2C, a hardware multiplier, an AES accelerator, DMA, an RTC module with alarm capabilities, up to 83 I/O pins, a high-performance 12-bit ADC, and an LCD module with contrast control for displays with up to 320 segments (8-mux).

The MSP430FR692x devices are microcontroller configurations with up to five 16-bit timers, Comparator, eUSCIs that support UART, SPI, and I^2C, a hardware multiplier, an AES accelerator, DMA, an RTC module with alarm capabilities, up to 52 I/O pins, a high-performance 12-bit ADC, and an LCD module with contrast control for displays with up to 116 segments (4-mux).

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.3 Operating Modes

The MSP430FR697x(1) and MSP430FR692x(1) MCUs have one active mode and seven software selectable low-power modes of operation (see 表 6-1). An interrupt event can wake up the device from a low-power mode (LPM0 to LPM4), service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

表 6-1. Operating Modes

MODE	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF (1)	CPU OFF (2)	CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
Maximum system clock	16 MHz		16 MHz	16 MHz	50 kHz	50 kHz	0 (3)	50 kHz	0 (3)	
Typical current consumption, T_A = 25°C	103 µA/MHz	65 µA/MHz	75 µA at 1 MHz	40 µA at 1 MHz	0.9 µA	0.4 µA	0.3 µA	0.35 µA	0.2 µA	0.02 µA
Typical wake-up time	N/A		instant.	6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-up events	N/A		all	all	LF I/O Comp	LF I/O Comp	I/O Comp	RTC I/O	I/O	
CPU	**on**		off	off	off	off	off	reset	reset	
FRAM	**on**	off(1)	standby (or off (1))	off	off	off	off	off	off	
High-frequency peripherals(4)	**available**		**available**	**available**	off	off	off	reset	reset	
Low-frequency peripherals(4)	**available**		**available**	**available**	**available**	**available** (5)	off	RTC	reset	
Unclocked peripherals(4)	**available**		**available**	**available**	**available**	**available** (5)	**available** (5)	reset	reset	
MCLK	**on** ($16MHz_{MAX}$)		off	off	off	off	off	off	off	
SMCLK	opt. (6) ($16MHz_{MAX}$)		opt. (6) ($16MHz_{MAX}$)	opt. (6) ($16MHz_{MAX}$)	off	off	off	off	off	
ACLK	**on** ($50\ kHz_{MAX}$)		**on** ($50\ kHz_{MAX}$)	**on** ($50\ kHz_{MAX}$)	**on** ($50\ kHz_{MAX}$)	**on** ($50\ kHz_{MAX}$)	off	off	off	
External clock	optional ($16MHz_{MAX}$)		optional ($16MHz_{MAX}$)	optional ($16MHz_{MAX}$)	optional ($50\ kHz_{MAX}$)	optional ($50\ kHz_{MAX}$)	optional ($50\ kHz_{MAX}$)	off	off	
Full retention	**yes**		**yes**	**yes**	**yes**	**yes** (7)	**yes** (7)	no	no	
SVS	always		always	always	opt. (8)	opt. (8)	opt. (8)	opt. (8)	on (9)	off (10)
Brownout	**always**		**always**	**always**	**always**	**always**	**always**	**always**	**always**	

(1) FRAM disabled in FRAM controller
(2) Disabling the FRAM through the FRAM controller decreases the LPM current consumption, but the wake-up time can increase. If the wake-up is for FRAM access (for example, to fetch an interrupt vector), wake-up time is increased. If the wake-up is for an operation other than FRAM access (for example, DMA transfer to RAM), wake-up time is not increased.
(3) All clocks disabled
(4) See 表 6-2 for a detailed description of peripherals in high-frequency, low-frequency, or unclocked state.
(5) See 6.3.1, which describes the use of peripherals in LPM3 and LPM4.
(6) Controlled by SMCLKOFF
(7) Using the RAM controller, the RAM can be completely powered down to save leakage; however, all data are lost.
(8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
(9) SVSHE = 1
(10) SVSHE = 0

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6.3.1 Peripherals in Low-Power Modes

Peripherals can be in different states that impact the achievable power modes of the device. The states depend on the operational modes of the peripherals (see 表 6-2). The states are:

- A peripheral is in a *high-frequency state* if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a *low-frequency state* if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an *unclocked state* if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode and instead enters a power mode that still supports the current state of the peripherals, unless an external clock is used. If an external clock is used, the application must ensure that the correct frequency range for the requested power mode is selected.

表 6-2. Peripheral States

PERIPHERAL	IN HIGH-FREQUENCY STATE(1)	IN LOW-FREQUENCY STATE(2)	IN UNCLOCKED STATE(3)
WDT	Clocked by SMCLK	Clocked by ACLK	Not applicable
DMA(4)	Not applicable	Not applicable	Waiting for a trigger
RTC_C	Not applicable	Clocked by LFXT	Not applicable
LCD_C	Not applicable	Clocked by ACLK or VLOCLK	Not applicable
Timer_A, TAx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz.	Clocked by external clock ≤50 kHz.
Timer_B, TBx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Ax in UART mode	Clocked by SMCLK	Clocked by ACLK	Waiting for first edge of START bit
eUSCI_Ax in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Ax in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Bx in I^2C master mode	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Not applicable
eUSCI_Bx in I^2C slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Waiting for START condition or clocked by external clock ≤50 kHz
eUSCI_Bx in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Bx in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
ADC12_B	Clocked by SMCLK or by MODOSC	Clocked by ACLK	Waiting for a trigger
REF_A	Not applicable	Not applicable	Always
COMP_E	Not applicable	Not applicable	Always
CRC(5)	Not applicable	Not applicable	Not applicable
MPY(5)	Not applicable	Not applicable	Not applicable
AES(5)	Not applicable	Not applicable	Not applicable

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz.
(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.
(3) Peripherals are in a state that does not require or does not use an internal clock.
(4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode will cause a temporary transition into active mode for the time of the transfer.
(5) Operates only during active mode and will delay the transition into a low-power mode until its operation is completed.

6.3.1.1 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are even operational in LPM4 because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder certain peripherals are group together. To achieve optimal current consumption try to use modules within one group and to limit the number of groups with active modules. 表 6-3 lists the group for each peripheral. Modules not listed in this table are either already included in the standard LPM3 current consumption specifications or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C). See the I_{IDLE} parameters in Section 5.7 for details.

表 6-3. Peripheral Groups

GROUP A	GROUP B	GROUP C	GROUP D
Timer TA0	Timer TA1	Timer TA2	Timer TA3
Comparator		Timer B0	LCD_C
ADC12_B		eUSCI_A0	eUSCI_A1
REF_A		eUSCI_B0	
		eUSCI_B1	

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6.4 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are in the address range 0FFFFh to 0FF80h. 図 6-1 summarizes the content of this address range.

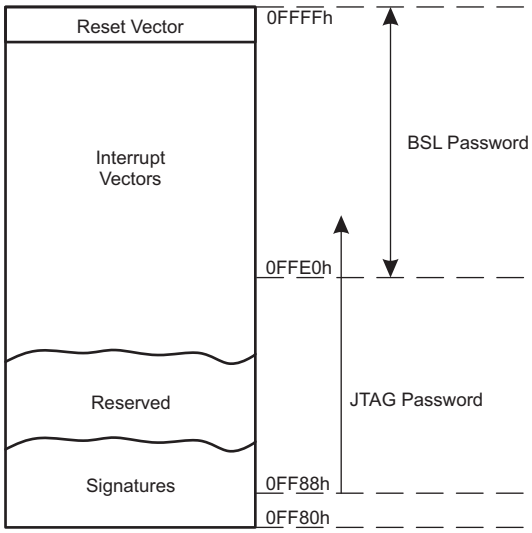

図 6-1. Interrupt Vectors, Signatures, and Passwords

The power-up start address or reset vector is located at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 6-4 shows the device-specific interrupt vector locations.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as the BSL password (if enabled by the corresponding signature).

The signatures are located at 0FF80h and extend to higher addresses. Signatures are evaluated during device start-up. 表 6-5 shows the device-specific signature locations.

A JTAG password can be programmed starting at address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide* for details.

表 6-4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, Brownout, Supply Supervisor External Reset $\overline{\text{RST}}$ Watchdog time-out (watchdog mode) WDT, FRCTL MPU, CS, PMM password violation FRAM uncorrectable bit error detection MPU segment violation FRAM access time error Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG ACCTEIFG PMMPORIFG, PMMBORIFG (SYSRSTIV) (1) (2)	Reset	0FFFEh	Highest
System NMI Vacant memory access JTAG mailbox FRAM bit error detection MPU segment violation	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV) (1) (3)	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator fault	NMIIFG, OFIFG (SYSUNIV) (1) (3)	(Non)maskable	0FFFAh	
Comparator_E	Comparator_E interrupt flags (CEIV) (1)	Maskable	0FFF8h	
Timer_B TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
Timer_B TB0	TB0CCR1.CCIFG to TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV) (1)	Maskable	0FFF4h	
Watchdog timer (interval timer mode)	WDTIFG	Maskable	0FFF2h	
eUSCI_A0 receive or transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG:UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV) (1)	Maskable	0FFEEh	
eUSCI_B0 receive or transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV) (1)	Maskable	0FFECh	
ADC12_B	ADC12IFG0 to ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC12OVIFG, ADC12TOVIFG (ADC12IV) (1)	Maskable	0FFEAh	
Timer_A TA0	TA0CCR0.CCIFG	Maskable	0FFE8h	
Timer_A TA0	TA0CCR1.CCIFG to TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV) (1)	Maskable	0FFE6h	
eUSCI_A1 receive or transmit	UCA1IFG:UCRXIFG, UCTXIFG (SPI mode) UCA1IFG:UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV) (1)	Maskable	0FFE4h	
eUSCI_B1 receive or transmit)	UCB1IFG: UCRXIFG, UCTXIFG (SPI mode) UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB1IV) (1)	Maskable	0FFE2h	

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

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表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV)(1)	Maskable	0FFE0h	
Timer_A TA1	TA1CCR0.CCIFG	Maskable	0FFDEh	
Timer_A TA1	TA1CCR1.CCIFG to TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV)(1)	Maskable	0FFDCh	
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)	Maskable	0FFDAh	
Timer_A TA2	TA2CCR0.CCIFG	Maskable	0FFD8h	
Timer_A TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV)(1)	Maskable	0FFD6h	
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) (1)	Maskable	0FFD4h	
Timer_A TA3	TA3CCR0.CCIFG	Maskable	0FFD2h	
Timer_A TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV)(1)	Maskable	0FFD0h	
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV) (1)	Maskable	0FFCEh	
I/O Port P4	P4IFG.0 to P4IFG.7 (P4IV) (1)	Maskable	0FFCCh	
LCD_C	LCD_C interrupt flags (LCDCIV) (1)	Maskable	0FFCAh	
RTC_C	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (1)	Maskable	0FFC8h	
AES	AESRDYIFG	Maskable	0FFC6h	Lowest

表 6-5. Signatures

SIGNATURE	WORD ADDRESS
IP Encapsulation Signature2	0FF8Ah
IP Encapsulation Signature1 (1)	0FF88h
BSL Signature2	0FF86h
BSL Signature1	0FF84h
JTAG Signature2	0FF82h
JTAG Signature1	0FF80h

(1) Must not contain 0AAAAh if used as JTAG password and IP encapsulation functionality is not desired.

6.5 Bootloader (BSL)

The BSL enables programming of the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I^2C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by an user-defined password. 表 6-6 lists the BSL pin requirements. BSL entry requires a specific entry sequence on the $\overline{RST}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see *MSP430 Programming With the Bootloader (BSL)*.

表 6-6. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{RST}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Devices with UART BSL (FRxxxx): Data transmit
P2.1	Devices with UART BSL (FRxxxx): Data receive
P1.6	Devices with I^2C BSL (FRxxxx1): Data
P1.7	Devices with I^2C BSL (FRxxxx1): Clock
VCC	Power supply
VSS	Ground supply

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{RST}$/NMI/SBWTDIO signal is required to interface with MSP430 development tools and device programmers. 表 6-7 lists the JTAG pin requirements. For details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on the JTAG implementation in MSP MCUs, see *MSP430 Programming With the JTAG Interface*.

表 6-7. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{RST}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-8 lists the Spy-Bi-Wire interface pin requirements. For details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on the SBW implementation in MSP MCUs, see *MSP430 Programming With the JTAG Interface*.

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表 6-8. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

注

Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "FRAM Controller (FRCTRL)" chapter, section "Wait State Control" of the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the memory protection unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see *MSP430 FRAM Technology – How To and Best Practices*.

6.8 RAM

The RAM is made up of one sector. The sector can be completely powered down in LPM3 and LPM4 to save leakage; however, all data is lost during shutdown.

6.9 Tiny RAM

The Tiny RAM can be used to hold data or a very small stack if the complete RAM is powered down in LPM3 and LPM4.

6.10 Memory Protection Unit Including IP Encapsulation

The FRAM can be protected from inadvertent CPU execution, read or write access by the MPU. Features of the MPU include:

- IP Encapsulation with programmable boundaries (prevents reads from "outside" like JTAG or non-IP software) in steps of 1KB.
- Main memory partitioning programmable up to three segments in steps of 1KB.
- The access rights of each segment (main and information memory) can be individually selected.
- Access violation flags with interrupt capability for easy servicing of access violations.

6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

6.11.1 Digital I/O

Up to eleven 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all pins of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive touch functionality is supported on all pins of ports P1 to P10 and PJ.
- No cross-currents during start-up

注

Configuration of Digital I/Os After BOR Reset

To prevent any cross-currents during start-up of the device all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section of the *Digital I/O* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

6.11.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal digitally controlled oscillator DCO, a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

6.11.3 Power-Management Module (PMM)

The primary functions of the PMM are:

- Supply regulated voltages to the core logic
- Supervise voltages that are connected to the device (at DVCC pins)
- Give reset signals to the device during power on and power off

6.11.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

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6.11.5 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock (RTC) with the following features implemented:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

6.11.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-9 lists the clocks that can be used by the WDT.

注

In watchdog mode, the watchdog timer prevents entry into LPM3.5 or LPM4.5 because this would deactivate the watchdog.

表 6-9. WDT_A Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODCLK

6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These system functions include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-10 lists the interrupt vector registers of the SYS module.

表 6-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGPIFG encapsulated IP memory segment violation (PUC)	26h	
		MPUSEGIIFG information memory segment violation (PUC)	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
		ACCTEIFG access time error (PUC)(1)	30h	
		Reserved	32h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		Reserved	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		MPUSEGPIFG encapsulated IP memory segment violation	08h	
		MPUSEGIIFG information memory segment violation	0Ah	
		MPUSEG1IFG segment 1 memory violation	0Ch	
		MPUSEG2IFG segment 2 memory violation	0Eh	
		MPUSEG3IFG segment 3 memory violation	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

(1) Indicates incorrect wait state settings.

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6.11.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-11 lists the triggers that can be used to start DMA operation.

表 6-11. DMA Trigger Assignments(1)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG
6	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	AES Trigger 0	AES Trigger 0	AES Trigger 0
12	AES Trigger 1	AES Trigger 1	AES Trigger 1
13	AES Trigger 2	AES Trigger 2	AES Trigger 2
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
18	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)
19	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)
20	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)
21	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)
22	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)
23	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)
24	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)
25	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)
26	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no trigger is generated.

6.11.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3 pin or 4 pin) and I^2C.

Two eUSCI_A modules and one or two eUSCI_B module are implemented.

6.11.10 Timer_A TA0, Timer_A TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. TA0 and TA1 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-12 and 表 6-13). TA0 and TA1 have extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-12. Timer_A TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.2 or P6.7 or P7.0	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.2 or P6.7 or P7.0	$\overline{\text{TA0CLK}}$	INCLK				
P1.5	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.5
P7.1 or P10.1	TA0.0	CCI0B				P7.1
	DV_{SS}	GND				P10.1
	DV_{CC}	V_{CC}				
P1.0 or P1.6 or P7.2 or P7.6	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.0
						P1.6
	COUT (internal)	CCI1B				P7.2
						P7.6
	DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {1}
	DV_{CC}	V_{CC}				
P1.1 or P1.7 or P7.3 or P7.5	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.1
	ACLK (internal)	CCI2B				P1.7
	DV_{SS}	GND				P7.3
	DV_{CC}	V_{CC}				P7.5

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表 6-13. Timer_A TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.1 or P4.4 or P5.2	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.1 or P4.4 or P5.2	$\overline{\text{TA1CLK}}$	INCLK				
P1.4 or P4.5	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.4
P5.2 or P10.2	TA1.0	CCI0B				P4.5
	DV_{SS}	GND				P5.2
	DV_{CC}	V_{CC}				P10.2
P1.2 or P3.3 or P4.6 or P5.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	P1.2
						P4.6
	COUT (internal)	CCI1B				P3.3
						P5.0
	DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {4}
	DV_{CC}	V_{CC}				
P1.3 or P4.7 or P5.1 or P7.7	TA1.2	CCI2A	CCR2	TA2	TA1.2	P1.3
	ACLK (internal)	CCI2B				P4.7
	DV_{SS}	GND				P5.1
	DV_{CC}	V_{CC}				P7.7

6.11.11 Timer_A TA2

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers each and with internal connections only. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-14). TA2 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-14. Timer_A TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 0 (internal)	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
From Capacitive Touch I/O 0 (internal)	CCI1A	CCR1	TA1	ADC12 (internal) ADC12SHSx = {5}
COUT (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

6.11.12 Timer_A TA3

TA3 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers each and with internal connections only. TA3 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-15). TA3 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-15. Timer_A TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 1 (internal)	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
From Capacitive Touch I/O 1 (internal)	CCI1A	CCR1	TA1	ADC12 (internal) ADC12SHSx = {6}
COUT (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
DV_{SS}	CCI2A	CCR2	TA2	
DV_{SS}	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
DV_{SS}	CCI3A	CCR3	TA3	
DV_{SS}	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
DV_{SS}	CCI4A	CCR4	TA4	
DV_{SS}	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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6.11.13 Timer_B TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers each. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-16). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-16. Timer_B TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.0 or P3.3 or P5.7	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.0 or P3.3 or P5.7	$\overline{\text{TB0CLK}}$	INCLK				
P3.4	TB0.0	CCI0A	CCR0	TB0	TB0.0	P3.4
P6.4	TB0.0	CCI0B				P6.4
	DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {2}
	DV_{CC}	V_{CC}				
P3.5 or P6.5	TB0.1	CCI1A	CCR1	TB1	TB0.1	P3.5
	COUT (internal)	CCI1B				P6.5
	DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {3}
	DV_{CC}	V_{CC}				
P3.6 or P6.6	TB0.2	CCI2A	CCR2	TB2	TB0.2	P3.6
	ACLK (internal)	CCI2B				P6.6
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
P2.4	TB0.3	CCI3A	CCR3	TB3	TB0.3	P2.4
P3.7	TB0.3	CCI3B				P3.7
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
P2.5	TB0.4	CCI4A	CCR4	TB4	TB0.4	P2.5
P2.2	TB0.4	CCI4B				P2.2
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
P2.6	TB0.5	CCI5A	CCR5	TB5	TB0.5	P2.6
P2.1	TB0.5	CCI5B				P2.1
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
P2.7	TB0.6	CCI6A	CCR6	TB6	TB0.6	P2.7
P2.0	TB0.6	CCI6B				P2.0
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				

6.11.14 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-17 lists the external trigger sources. 表 6-18 lists the available multiplexing between internal and external analog inputs.

表 6-17. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	Timer_A TA0 CCR1 output
010	2	Timer_B TB0 CCR0 output
011	3	Timer_B TB0 CCR1 output
100	4	Timer_A TA1 CCR1 output
101	5	Timer_A TA2 CCR1 output
110	6	Timer_A TA3 CCR1 output
111	7	Reserved (DVSS)

表 6-18. ADC12_B External and Internal Signal Mapping

CONTROL BIT	EXTERNAL (CONTROL BIT = 0)	INTERNAL (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery Monitor
ADC12TCMAP	A30	Temperature Sensor
ADC12CH0MAP	A29	N/A (1)
ADC12CH1MAP	A28	N/A (1)
ADC12CH2MAP	A27	N/A (1)
ADC12CH3MAP	A26	N/A (1)

(1) N/A = No internal signal available on this device.

6.11.15 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.11.16 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 signature is based on the CRC-CCITT standard.

6.11.17 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard.

6.11.18 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

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6.11.19 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.11.20 Shared Reference (REF_A)

The reference module (REF_A) generates all critical reference voltages that can be used by the various analog peripherals in the device.

6.11.21 LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static and 2-mux to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

To reduce system noise, the charge pump can be temporarily disabled. 表 6-19 lists the available automatic charge pump disable options.

表 6-19. LCD Automatic Charge Pump Disable Bits (LCDCPDISx)

CONTROL BIT	DESCRIPTION
LCDCPDIS0	LCD charge pump disable during ADC12 conversion 0b = LCD charge pump not automatically disabled during conversion 1b = LCD charge pump automatically disabled during conversion
LCDCPDIS1 to LCDCPDIS7	No functionality

6.11.22 Embedded Emulation

6.11.22.1 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.11.22.2 EnergyTrace++™ Technology

These MCUs implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.

- COMP is on.
- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- eUSCI_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.
- LCD: timing generator is active.

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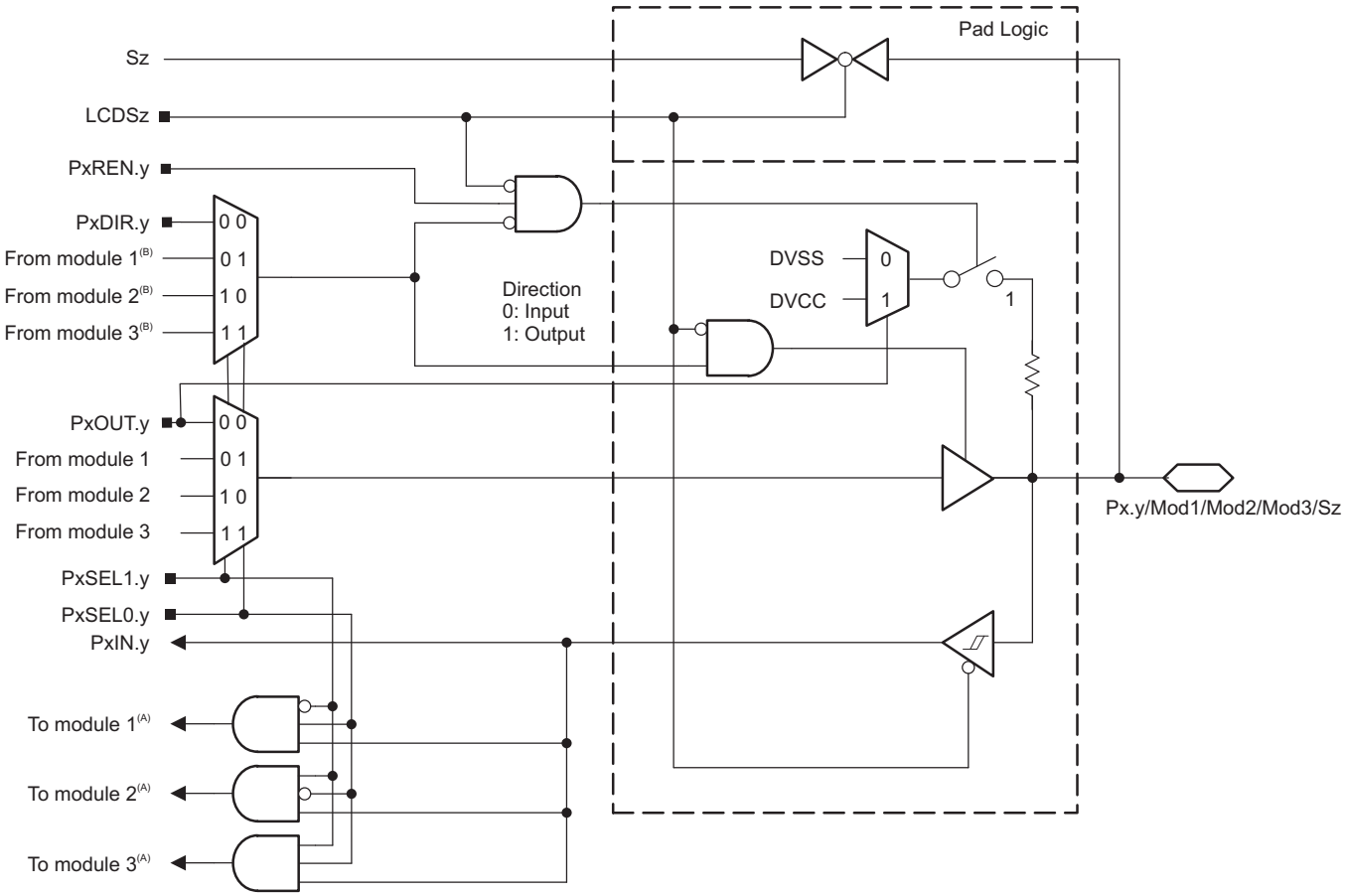
6.11.23 Input/Output Diagrams

6.11.23.1 Digital I/O Functionality – Ports P1 to P10

The port pins provide the following features:

- Interrupt and wakeup from LPMx.5 capability for ports P1, P2, P3, and P4
- Capacitive touch functionality (see 6.11.23.2)
- Up to three digital module input or output functions
- LCD segment functionality (not all pins, package dependent)

図 6-2 shows the features and the corresponding control logic (not including the capacitive touch logic). It is applicable for all port pins P1.0 to P10.2 unless a dedicated diagram is available in the following sections. The module functions provided per pin and whether the direction is controlled by the module or by the port direction register for the selected secondary function are described in the pin function tables.

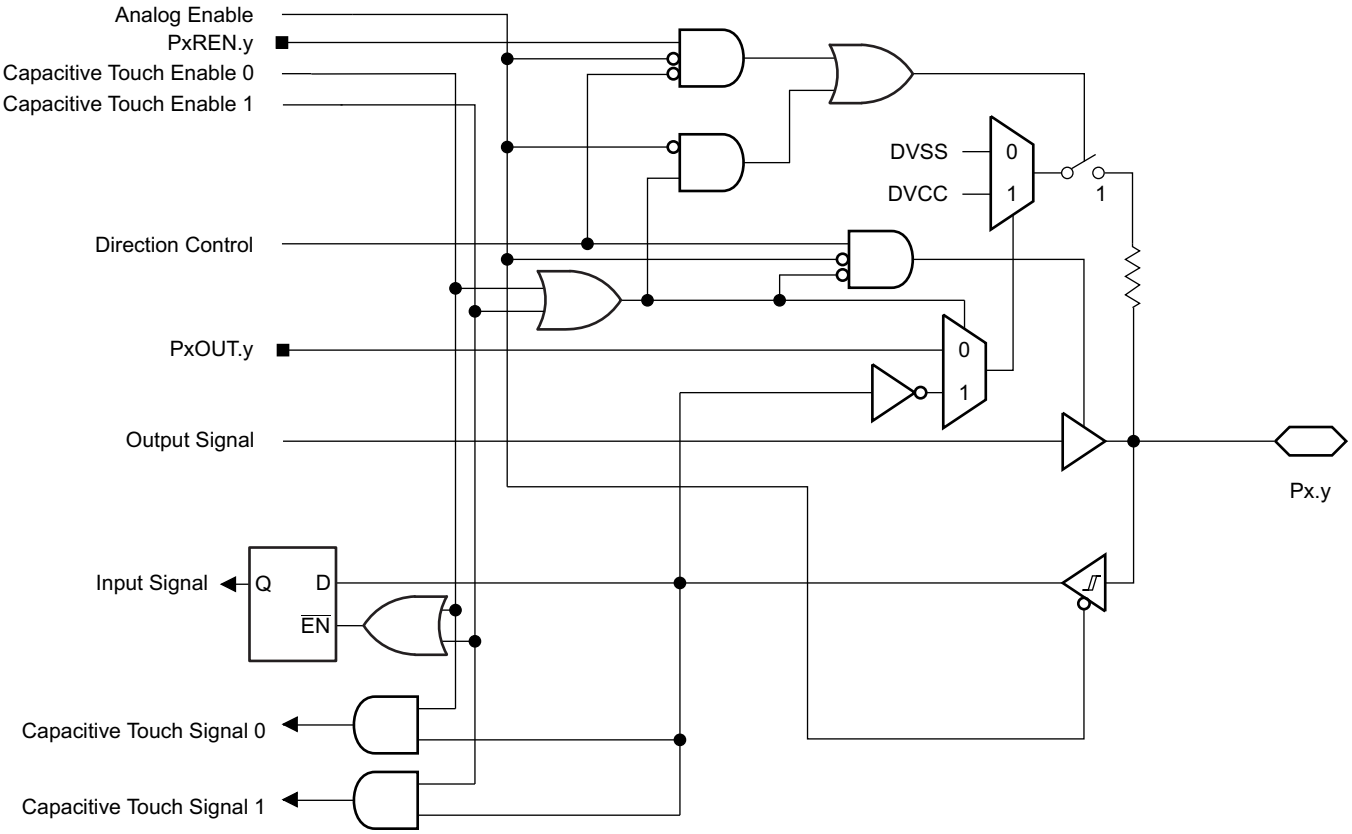


A. The inputs from several pins toward a module are ORed together.
B. The direction is controlled either by the connected module or by the corresponding PxDIR.y bit. See the pin function tables.
NOTE: Functional representation only.

図 6-2. General Port Pin Diagram

6.11.23.2 Capacitive Touch Functionality Ports P1 to P10 and PJ

図 6-3 shows the Capacitive Touch functionality that all port pins provide. The Capacitive Touch functionality is controlled using the Capacitive Touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*. The Capacitive Touch functionality is not shown in the other pin diagrams.



NOTE: Functional representation only.

図 6-3. Capacitive Touch I/O Diagram

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6.11.23.3 Port P1 (P1.0 to P1.3) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-20 summarizes the selection of the pin function.

表 6-20. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/ VREF-/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		TA0.CCI1A	0	0	1
		TA0.1	1		
		DMAE0	0	1	0
		RTCCLK (2)	1		
		A0, C0, VREF-, VeREF- (3) (4)	X	1	1
P1.1/TA0.2/TA1CLK/COUT/A1/C1/ VREF+/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TA1CLK	0	1	0
		COUT (5)	1		
		A1, C1, VREF+, VeREF+ (3) (4)	X	1	1
P1.2/TA1.1/TA0CLK/COUT/A2/C2	2	P1.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		TA0CLK	0	1	0
		COUT (6)	1		
		A2, C2 (3) (4)	X	1	1
P1.3/TA1.2/A3/C3	3	P1.3 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		N/A	0	1	0
			1		
		A3, C3 (3) (4)	X	1	1

(1) X = Don't care
(2) Do not use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternative RTCCLK output pin.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(5) Do not use this pin as COUT output if the TA1CLK functionality is used on any other pin. Select an alternative COUT output pin.
(6) Do not use this pin as COUT output if the TA0CLK functionality is used on any other pin. Select an alternative COUT output pin.

6.11.23.4 Port P1 (P1.4 to P1.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-21 summarizes the selection of the pin function.

表 6-21. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	LCDSz
P1.4/UCB0CLK/UCA0STE/TA1.0/Sz	4	P1.4 (I/O)	I: 0; O: 1	0	0	0
		UCB0CLK	X (2)	0	1	0
		UCA0STE	X (3)	1	0	0
		TA1.CCI0A	0	1	1	0
		TA1.0	1			
		Sz (4)	X	X	X	1
P1.5/UCB0STE/UCA0CLK/TA0.0/Sz	5	P1.5 (I/O)	I: 0; O: 1	0	0	0
		UCB0STE	X (2)	0	1	0
		UCA0CLK	X (3)	1	0	0
		TA0.CCI0A	0	1	1	0
		TA0.0	1			
		Sz (4)	X	X	X	1
P1.6/UCB0SIMO/UCB0SDA/TA0.1/Sz	6	P1.6 (I/O)	I: 0; O: 1	0	0	0
		UCB0SIMO/UCB0SDA	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		TA0.CCI1A	0	1	1	0
		TA0.1	1			
		Sz (4)	X	X	X	1
P1.7/UCB0SOMI/UCB0SCL/TA0.2/Sz	7	P1.7 (I/O)	I: 0; O: 1	0	0	0
		UCB0SOMI/UCB0SCL	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		TA0.CCI2A	0	1	1	0
		TA0.2	1			
		Sz (4)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Direction controlled by eUSCI_A0 module.
(4) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

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6.11.23.5 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-22 summarizes the selection of the pin function.

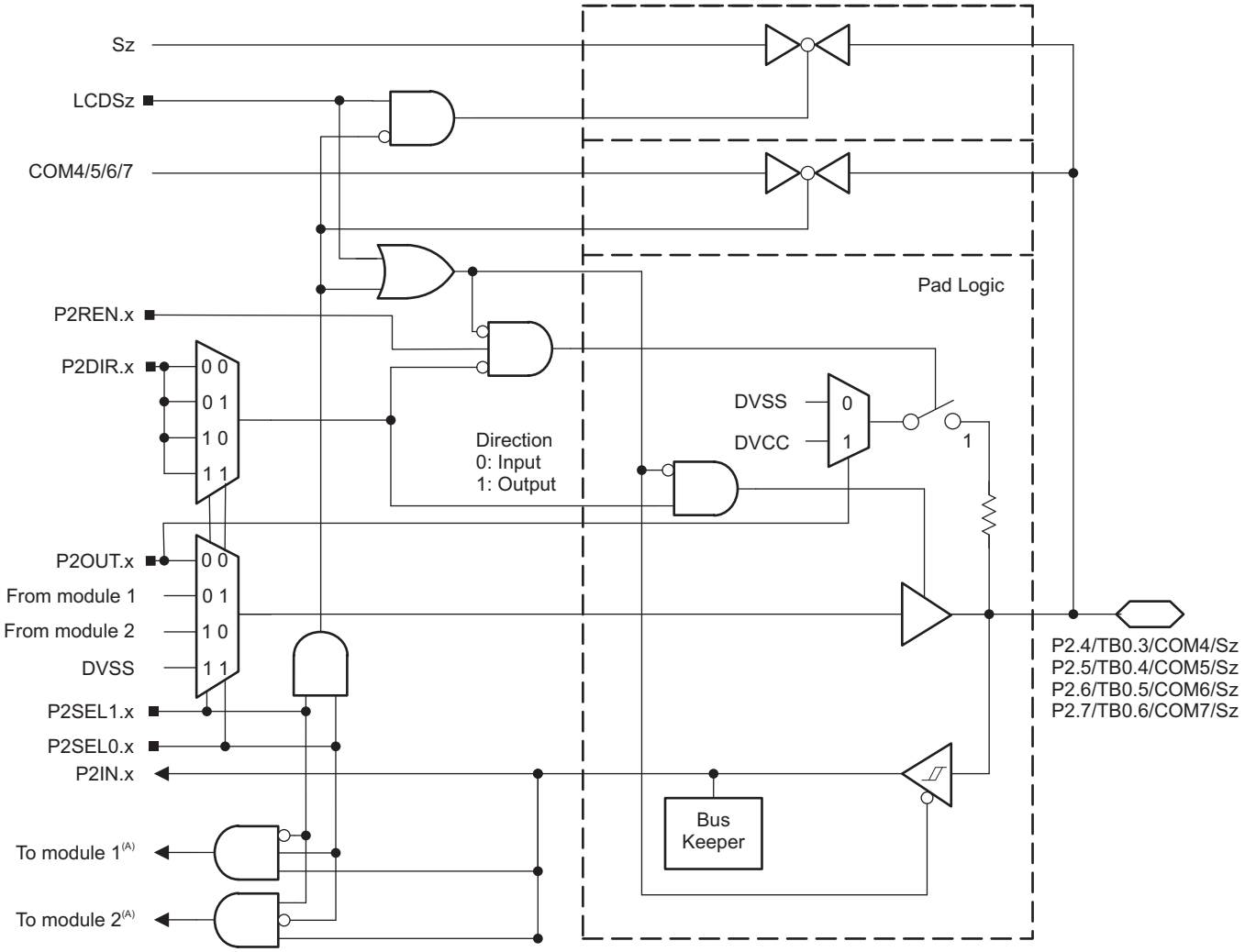
表 6-22. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	LCDSz
P2.0/UCA0SIMO/UCA0TXD/TB0.6/TB0CLK/Sz	0	P2.0 (I/O)	I: 0; O: 1	0	0	0
		UCA0SIMO/UCA0TXD	X (2)	0	1	0
		TB0.CCI6B	0	1	0	0
		TB0.6	1			
		TB0CLK	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P2.1/UCA0SOMI/UCA0RXD/TB0.5/DMAE0/Sz	1	P2.1 (I/O)	I: 0; O: 1	0	0	0
		UCA0SOMI/UCA0RXD	X (2)	0	1	0
		TB0.CCI5B	0	1	0	0
		TB0.5	1			
		DMA0E	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P2.2/UCA0CLK/TB0.4/RTCCLK/Sz	2	P2.2 (I/O)	I: 0; O: 1	0	0	0
		UCA0CLK	X (2)	0	1	0
		TB0.CCI4B	0	1	0	0
		TB0.4	1			
		N/A	0	1	1	0
		RTCCLK	1			
		Sz (3)	X	X	X	1
P2.3/UCA0STE/TB0OUTH/Sz	3	P2.3 (I/O)	I: 0; O: 1	0	0	0
		UCA0STE	X (2)	0	1	0
		TB0OUTH	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.6 Port P2 (P2.4 to P2.7) Input/Output With Schmitt Trigger

図 6-4 shows the port diagram. 表 6-23 summarizes the selection of the pin function.



A. The inputs from several pins toward a module are ORed together.
NOTE: Functional representation only.

図 6-4. Port P2 (P2.4 to P2.7) Diagram

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表 6-23. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	LCDSz
P2.4/TB0.3/COM4/Sz	4	P2.4 (I/O)	I: 0; O: 1	0	0	0
		TB0.CCI3A	0	0	1	0
		TB0.3	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM4	X	1	1	0
		Sz (2)	X	X	X	1
P2.5/TB0.4/COM5/Sz	5	P2.5 (I/O)	I: 0; O: 1	0	0	0
		TB0.CCI4A	0	0	1	0
		TB0.4	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM5	X	1	1	0
		Sz (2)	X	X	X	1
P2.6/TB0.5/COM6/Sx	6	P2.6 (I/O)	I: 0; O: 1	0	0	0
		TB0.CCI5A	0	0	1	0
		TB0.5	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM6	X	1	1	0
		Sz (2)	X	X	X	1
P2.7/TB0.6/COM7/Sx	7	P2.7 (I/O)	I: 0; O: 1	0	0	0
		TB0.CCI6A	0	0	1	0
		TB0.6	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM7	X	1	1	0
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.7 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-24 and 表 6-25 summarize the selection of the pin function.

表 6-24. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	LCDSz
P3.0/UCB1CLK/Sz	0	P3.0 (I/O)	I: 0; O: 1	0	0	0
		UCB1CLK	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P3.1/UCB1SIMO/UCB1SDA/Sz	1	P3.1 (I/O)	I: 0; O: 1	0	0	0
		UCB1SIMO/UCB1SDA	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P3.2/UCB1SOMI/UCB1SCL/Sz	2	P3.2 (I/O)	I: 0; O: 1	0	0	0
		UCB1SOMI/UCB1SCL	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
			0	1	1	0
			1			
		Sz (3)	X	X	X	1
P3.3/TA1.1/TB0CLK/Sz	3	P3.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TA1.CCI1A	0	1	0	0
		TA1.1	1			
		TB0CLK	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

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表 6-25. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	LCDSz
P3.4/UCA1SIMO/UCA1TXD/TB0.0/Sz	4	P3.4 (I/O)	I: 0; O: 1	0	0	0
		UCA1SIMO/UCA1TXD	X (2)	0	1	0
		TB0CCI0A	0	1	0	0
		TB0.0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P3.5/UCA1SOMI/UCA1RXD/TB0.1/Sz	5	P3.5 (I/O)	I: 0; O: 1	0	0	0
		UCA1SOMI/UCA1RXD	X (2)	0	1	0
		TB0CCI1A	0	1	0	0
		TB0.1	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P3.6/UCA1CLK/TB0.2/Sz	6	P3.6 (I/O)	I: 0; O: 1	0	0	0
		UCA1CLK	X (2)	0	1	0
		TB0CCI2A	0	1	0	0
		TB0.2	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P3.7/UCA1STE/TB0.3/Sz	7	P3.7 (I/O)	I: 0; O: 1	0	0	0
		UCA1STE	X (2)	0	1	0
		TB0CCI3B	0	1	0	0
		TB0.3	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.8 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-26 and 表 6-27 summarize the selection of the pin function.

表 6-26. Port P4 (P4.0 to P4.3) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P4DIR.x	P4SEL1.x	P4SEL0.x	LCDSz
P4.0/UCB1SIMO/UCB1SDA/MCLK/Sz	0	P4.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SIMO/UCB1SDA	X (2)	1	0	0
		N/A	0	1	1	0
		MCLK	1			
		Sz (3)	X	X	X	1
P4.1/UCB1SOMI/UCB1SCL/ACLK/Sz	1	P4.1 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SOMI/UCB1SCL	X (2)	1	0	0
		N/A	0	1	1	0
		ACLK	1			
		Sz (3)	X	X	X	1
P4.2/UCA0SIMO/UCA0TXD/UCB1CLK/Sz	2	P4.2 (I/O)	I: 0; O: 1	0	0	0
		UCA0SIMO/UCA0TXD	X (4)	0	1	0
		UCB1CLK	X (2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P4.3/UCA0SOMI/UCA0RXD/UCB1STE/Sz	3	P4.3 (I/O)	I: 0; O: 1	0	0	0
		UCA0SOMI/UCA0RXD	X (4)	0	1	0
		UCB1STE	X (2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.
(4) Direction controlled by eUSCI_A0 module.

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表 6-27. Port P4 (P4.4 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P4DIR.x	P4SEL1.x	P4SEL0.x	LCDSz
P4.4/UCB1STE/TA1CLK/Sz	4	P4.4 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1STE	X (2)	1	0	0
		TA1CLK	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P4.5/UCB1CLK/TA1.0/Sz	5	P4.5 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1CLK	X (2)	1	0	0
		TA1CCI0A	0	1	1	0
		TA1.0	1			
		Sz (3)	X	X	X	1
P4.6/UCB1SIMO/UCB1SDA/TA1.1/Sz	6	P4.6 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SIMO/UCB1SDA	X (2)	1	0	0
		TA1CCI1A	0	1	1	0
		TA1.1	1			
		Sz (3)	X	X	X	1
P4.7/UCB1SOMI/UCB1SCL/TA1.2/Sz	7	P4.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SOMI/UCB1SCL	X (2)	1	0	0
		TA1CCI2A	0	1	1	0
		TA1.2	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.9 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-28 and 表 6-29 summarize the selection of the pin function.

表 6-28. Port P5 (P5.0 to P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P5DIR.x	P5SEL1.x	P5SEL0.x	LCDSz
P5.0/TA1.1/MCLK/Sz	0	P5.0 (I/O)	I: 0; O: 1	0	0	0
		TA1CCI1A	0	0	1	0
		TA1.1	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		MCLK	1			
		Sz (2)	X	X	X	1
P5.1/TA1.2/Sz	1	P5.1 (I/O)	I: 0; O: 1	0	0	0
		TA1CCI2A	0	0	1	0
		TA1.2	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		N/A	1			
		Sz (2)	X	X	X	1
P5.2/TA1.0/TA1CLK/ACLK/Sz	2	P5.2 (I/O)	I: 0; O: 1	0	0	0
		TA1CCI0B	0	0	1	0
		TA1.0	1			
		TA1CLK	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		ACLK	1			
		Sz (2)	X	X	X	1
P5.3/UCB1STE/Sz	3	P5.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1STE	X (3)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.
(3) Direction controlled by eUSCI_B1 module.

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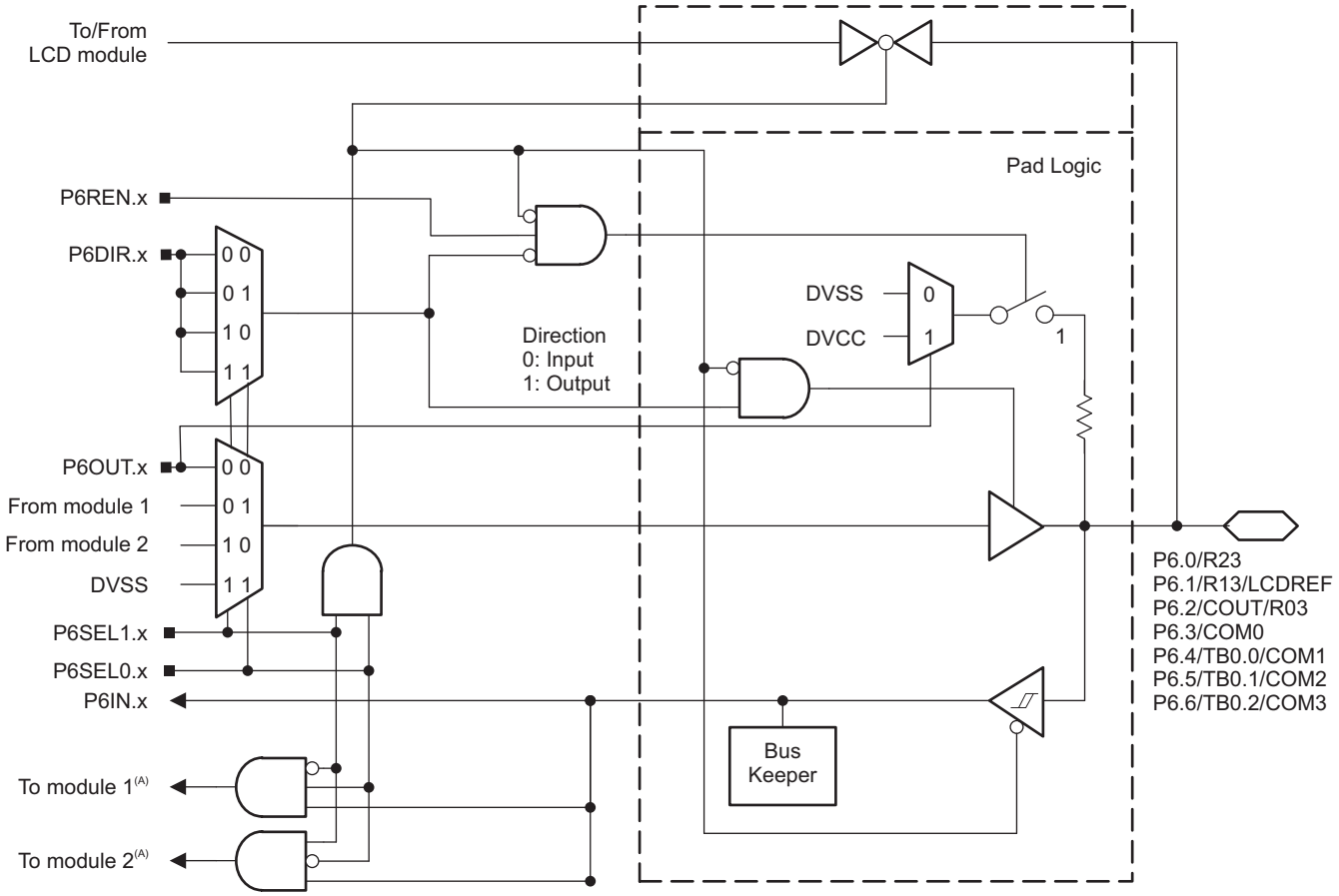
表 6-29. Port P5 (P5.4 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P5DIR.x	P5SEL1.x	P5SEL0.x	LCDSz
P5.4/UCA1SIMO/UCA1TXD/Sz	4	P5.4 (I/O)	I: 0; O: 1	0	0	0
		UCA1SIMO/UCA1TXD	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.5/UCA1SOMI/UCA1RXD/Sz	5	P5.5 (I/O)	I: 0; O: 1	0	0	0
		UCA1SOMI/UCA1RXD	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.6/UCA1CLK/Sz	6	P5.6 (I/O)	I: 0; O: 1	0	0	0
		UCA1CLK	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.7/UCA1STE/TB0CLK/Sz	7	P5.7 (I/O)	I: 0; O: 1	0	0	0
		UCA1STE	X (2)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		TB0CLK	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.10 Port P6 (P6.0 to P6.6) Input/Output With Schmitt Trigger

図 6-5 shows the port diagram. 表 6-30 and 表 6-31 summarize the selection of the pin function.



A. The inputs from several pins toward a module are ORed together.
NOTE: Functional representation only.

図 6-5. Port P6 (P6.0 to P6.6) Diagram

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表 6-30. Port P6 (P6.0 to P6.2) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.0/R23	0	P6.0 (I/O)	I: 0; O: 1	0	0	–
		N/A	0	0	1	–
		Internally tied to DVSS	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		R23 (2)	X	1	1	–
P6.1/R13/LCDREF	1	P6.1 (I/O)	I: 0; O: 1	0	0	–
		N/A	0	0	1	–
		Internally tied to DVSS	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		R13/LCDREF (2)	X	1	1	–
P6.2/COUT/R03	2	P6.2 (I/O)	I: 0; O: 1	0	0	–
		N/A	0	0	1	–
		COUT	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		R03 (2)	X	1	1	–

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

表 6-31. Port P6 (P6.3 to P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.3/COM0	3	P6.3 (I/O)	I: 0; O: 1	0	0	–
		N/A	0	0	1	–
		Internally tied to DVSS	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		COM0 (2)	X	1	1	–
P6.4/TB0.0/COM1	4	P6.4 (I/O)	I: 0; O: 1	0	0	–
		TB0CCI0B	0	0	1	–
		TB0.0	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		COM1 (2)	X	1	1	–
P6.5/TB0.1/COM2	5	P6.5 (I/O)	I: 0; O: 1	0	0	–
		TB0CCI1A	0	0	1	–
		TB0.1	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		COM2 (2)	X	1	1	–
P6.6/TB0.2/COM3	6	P6.6 (I/O)	I: 0; O: 1	0	0	–
		TB0CCI2A	0	0	1	–
		TB0.2	1			
		N/A	0	1	0	–
		Internally tied to DVSS	1			
		COM3 (2)	X	1	1	–

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.11.23.11 Port P6 (P6.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-32 summarizes the selection of the pin function.

表 6-32. Port P6 (P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.7/TA0CLK/Sz	7	P6.7 (I/O)	I: 0; O: 1	0	0	0
		TA0CLK	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.12 Port P7 (P7.0 to P7.7) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-33 and 表 6-34 summarize the selection of the pin function.

表 6-33. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	LCDSz
P7.0/TA0CLK/Sz	0	P7.0 (I/O)	I: 0; O: 1	0	0	0
		TA0CLK	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P7.1/TA0.0/ACLK/Sz	1	P7.1 (I/O)	I: 0; O: 1	0	0	0
		TA0CCI0B	0	0	1	0
		TA0.0	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		ACLK	1			
		Sz (2)	X	X	X	1
P7.2/TA0.1/Sz	2	P7.2 (I/O)	I: 0; O: 1	0	0	0
		TA0CCI1A	0	0	1	0
		TA0.1	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		N/A	1			
		Sz (2)	X	X	X	1
P7.3/TA0.2/Sz	3	P7.3 (I/O)	I: 0; O: 1	0	0	0
		TA0CCI2A	0	0	1	0
		TA0.2	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

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表 6-34. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	LCDSz
P7.4/SMCLK/Sz	4	P7.4 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		SMCLK	1			
		Sz (2)	X	X	X	1
P7.5/TA0.2/Sz	5	P7.5 (I/O)	I: 0; O: 1	0	0	0
		TA0CCI2A	0	0	1	0
		TA0.2	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P7.6/TA0.1/Sz	6	P7.6 (I/O)	I: 0; O: 1	0	0	0
		TA0CCI1A	0	0	1	0
		TA0.1	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P7.7/TA1.2/TB0OUTH/Sz	7	P7.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TA1.CCI2A	0	1	0	0
		TA1.2	1			
		TB0OUTH	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.13 Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-35 summarizes the selection of the pin function.

表 6-35. Port P8 (P8.0 to P8.3) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P8DIR.x	P8SEL1.x	P8SEL0.x	LCDSz
P8.0/RTCCLK/Sz	0	P8.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		RTCCLK	1			
		Sz (2)	X	X	X	1
P8.1/DMAE0/Sz	1	P8.1 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		DMA0E	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P8.2/Sz	2	P8.2 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P8.3/MCLK/Sz	3	P8.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		MCLK	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

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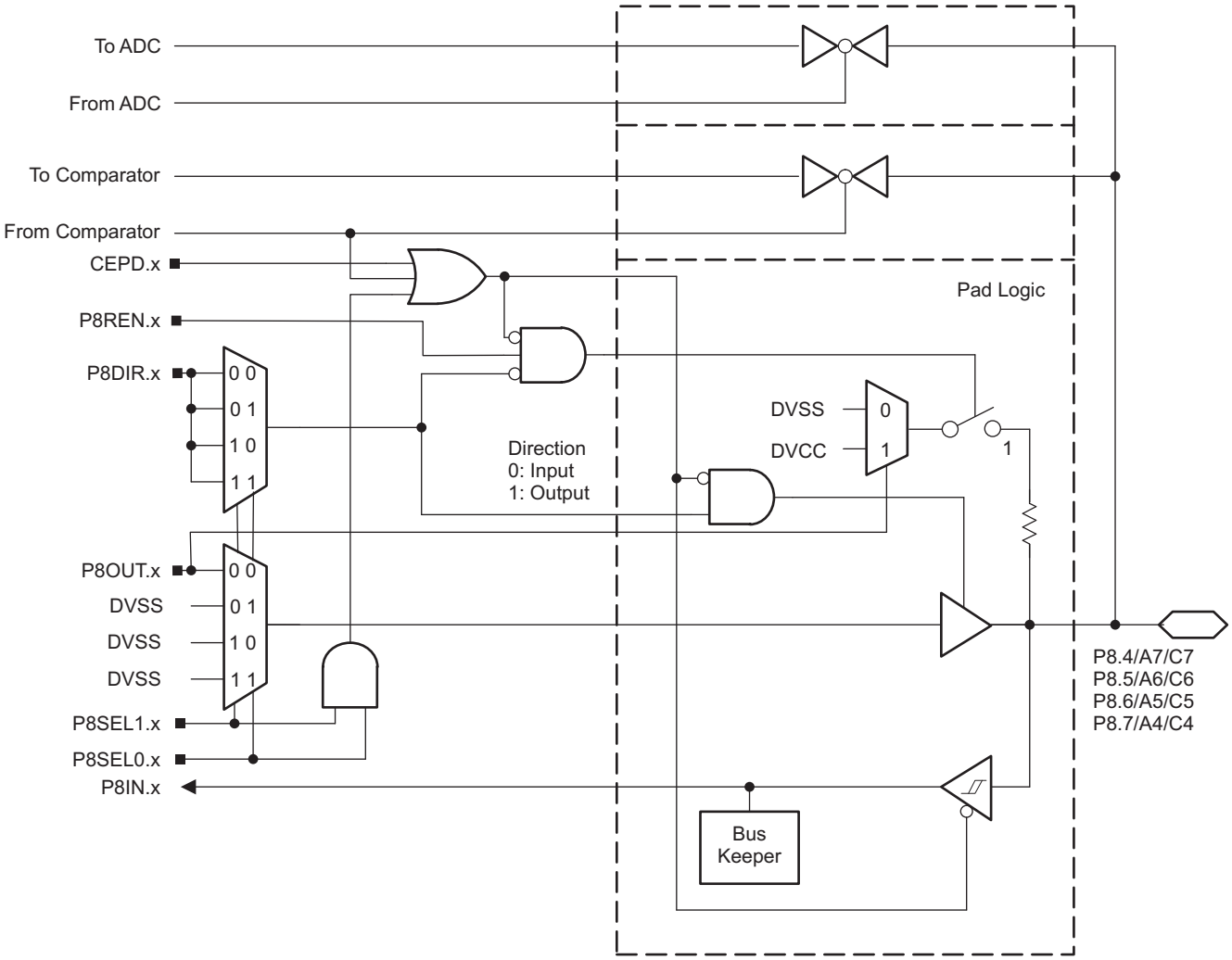
6.11.23.14 Port P8 (P8.4 to P8.7) Input/Output With Schmitt Trigger

図 6-6 shows the port diagram. 表 6-36 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-6. Port P8 (P8.4 to P8.7) Diagram

表 6-36. Port P8 (P8.4 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.4/A7/C7	4	P8.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A7/C7 (2) (3)	X	1	1
P8.5/A6/C6	5	P8.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A6/C6 (2) (3)	X	1	1
P8.6/A5/C5	6	P8.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A5/C5 (2) (3)	X	1	1
P8.7/A4/C4	7	P8.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A4/C4 (2) (3)	X	1	1

(1) X = Don't care
(2) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

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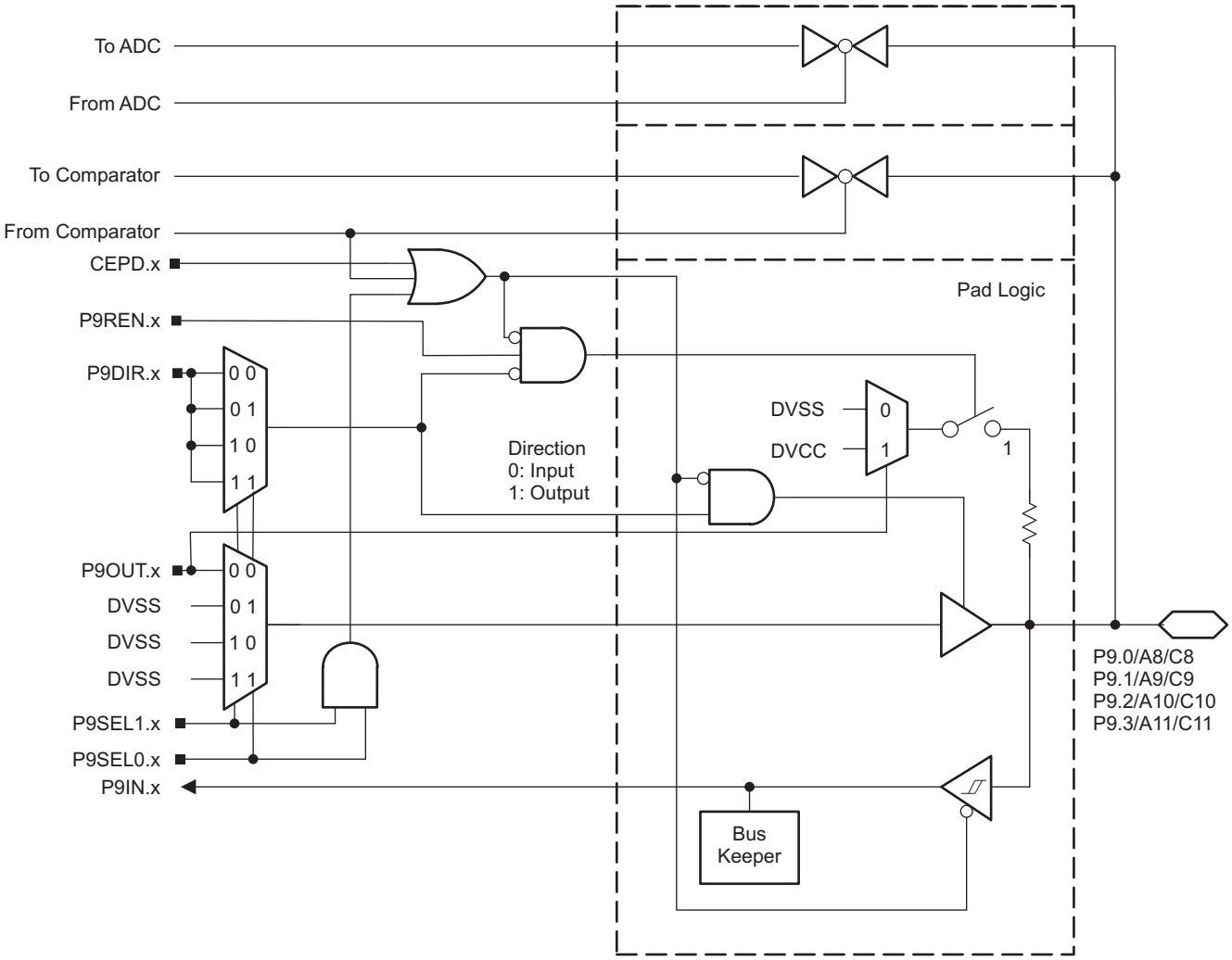
6.11.23.15 Port P9 (P9.0 to P9.3) Input/Output With Schmitt Trigger

図 6-7 shows the port diagram. 表 6-37 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-7. Port P9 (P9.0 to P9.3) Diagram

表 6-37. Port P9 (P9.0 to P9.3) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.0/A8/C8	0	P9.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A (2)	X	1	0
		A8/C8 (2)(3)	X	1	1
P9.1/A9/C9	1	P9.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A (2)	X	1	0
		A9/C9 (2)(3)	X	1	1
P9.2/A10/C10	2	P9.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A (2)	X	1	0
		A10/C10 (2)(3)	X	1	1
P9.3/A11/C11	3	P9.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A (2)	X	1	0
		A11/C11 (2) (3)	X	1	1

(1) X = Don't care
(2) Setting P9SEL1.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

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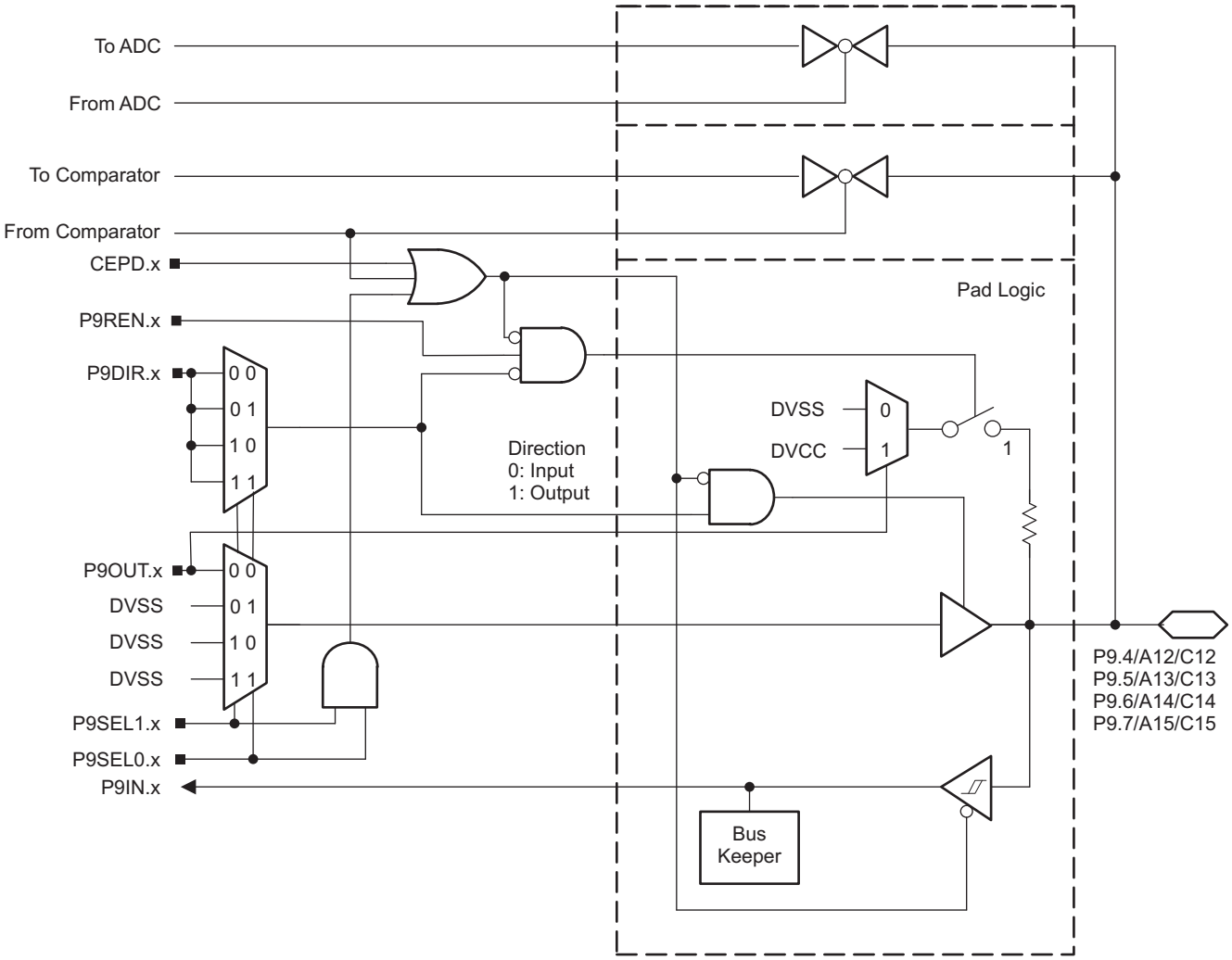
6.11.23.16 Port P9 (P9.4 to P9.7) Input/Output With Schmitt Trigger

図 6-8 shows the port diagram. 表 6-38 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-8. Port P9 (P9.4 to P9.7) Diagram

表 6-38. Port P9 (P9.4 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.4/A12/C12	4	P9.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A12/C12 (2) (3)	X	1	1
P9.5/A13/C13	5	P9.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A13/C13 (2) (3)	X	1	1
P9.6/A14/C14	6	P9.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A14/C14 (2) (3)	X	1	1
P9.7/A15/C15	7	P9.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A15/C15 (2) (3)	X	1	1

(1) X = Don't care
(2) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

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6.11.23.17 Port P10 (P10.0 to P10.2) Input/Output With Schmitt Trigger

For the pin diagram, see 図 6-2. 表 6-39 summarizes the selection of the pin function.

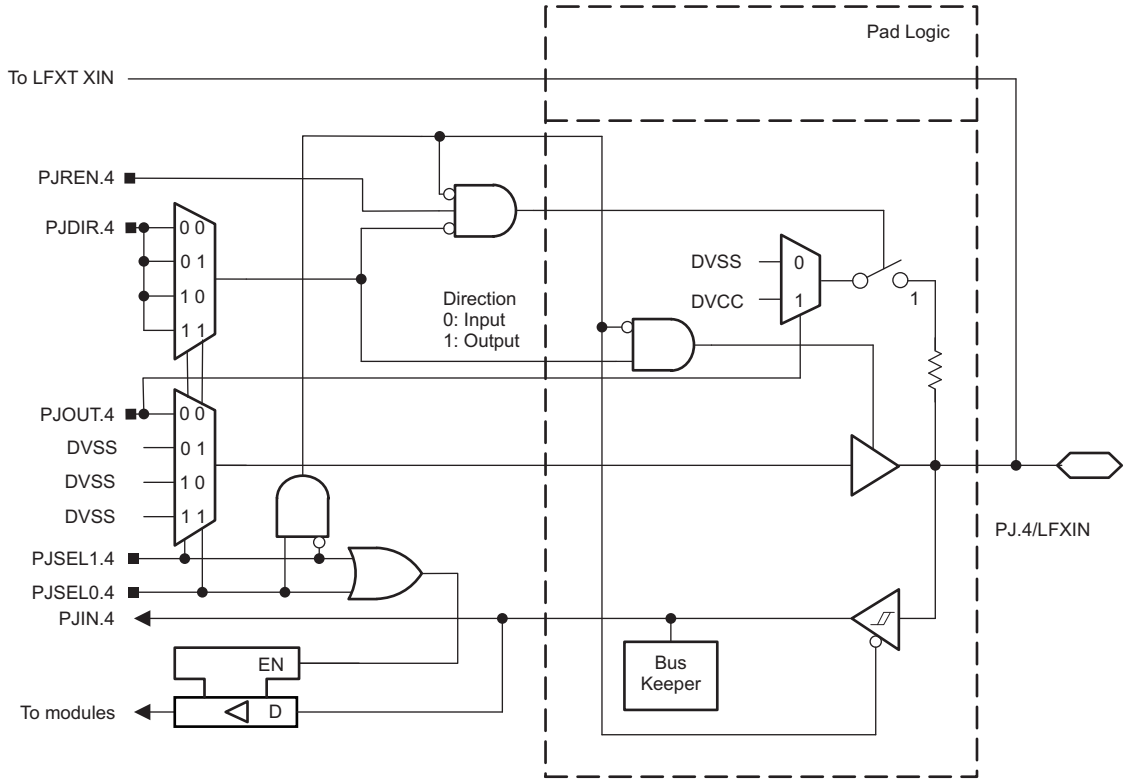
表 6-39. Port P10 (P10.0 to P10.2) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)			
			P10DIR.x	P10SEL1.x	P10SEL0.x	LCDSz
P10.0/SMCLK/Sz	0	P10.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		SMCLK	1			
		Sz (2)	X	X	X	1
P10.1/TA0.0/Sz	1	P10.1 (I/O)	I: 0; O: 1	0	0	0
		TA0.CCI0B	0	0	1	0
		TA0.0	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P10.2/TA1.0/SMCLK/Sz	2	P10.2 (I/O)	I: 0; O: 1	0	0	0
		TA1.CCI0B	0	0	1	0
		TA1.0	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		SMCLK	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

6.11.23.18 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

図 6-9 and 図 6-10 show the port diagrams. 表 6-40 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-9. Port PJ (PJ.4) Diagram

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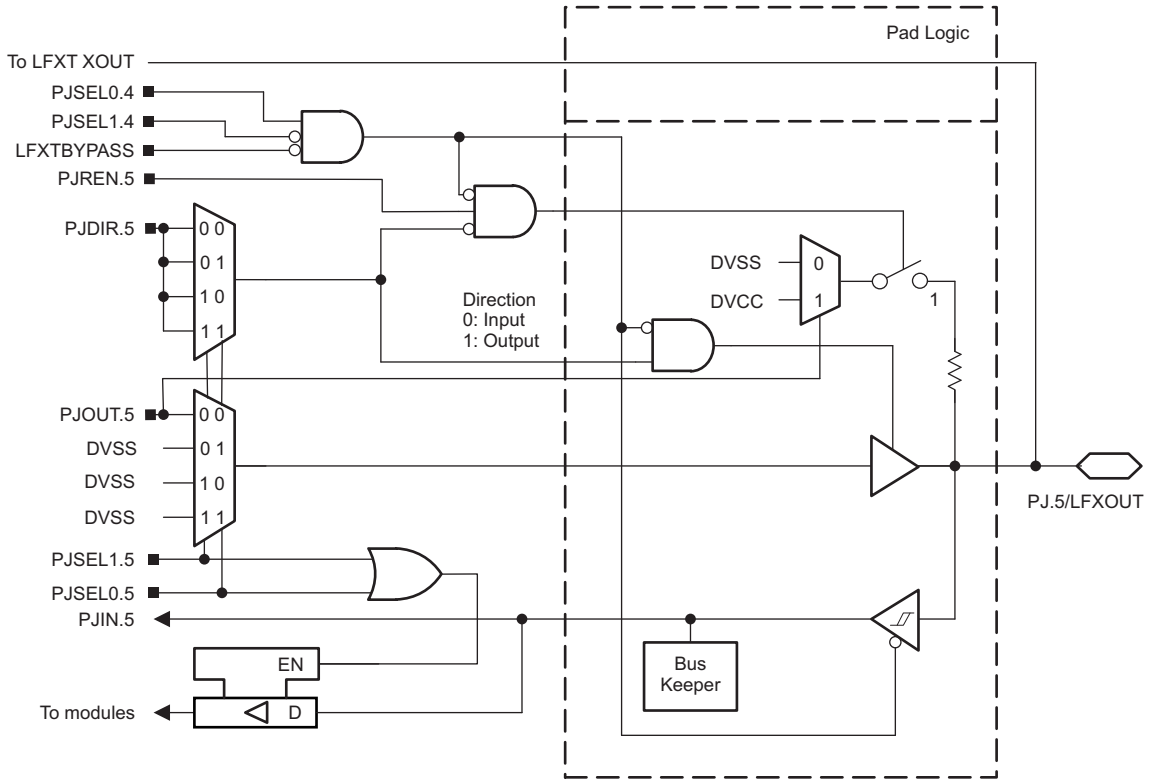

NOTE: Functional representation only.

図 6-10. Port PJ (PJ.5) Diagram

表 6-40. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	LFXT BYPASS
PJ.4/LFXIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		LFXIN crystal mode (2)	X	X	X	0	1	0
		LFXIN bypass mode (2)	X	X	X	0	1	1
PJ.5/LFXOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		Internally tied to DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		LFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
(4) With PJSEL0.5 = 1 or PJSEL1.5 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

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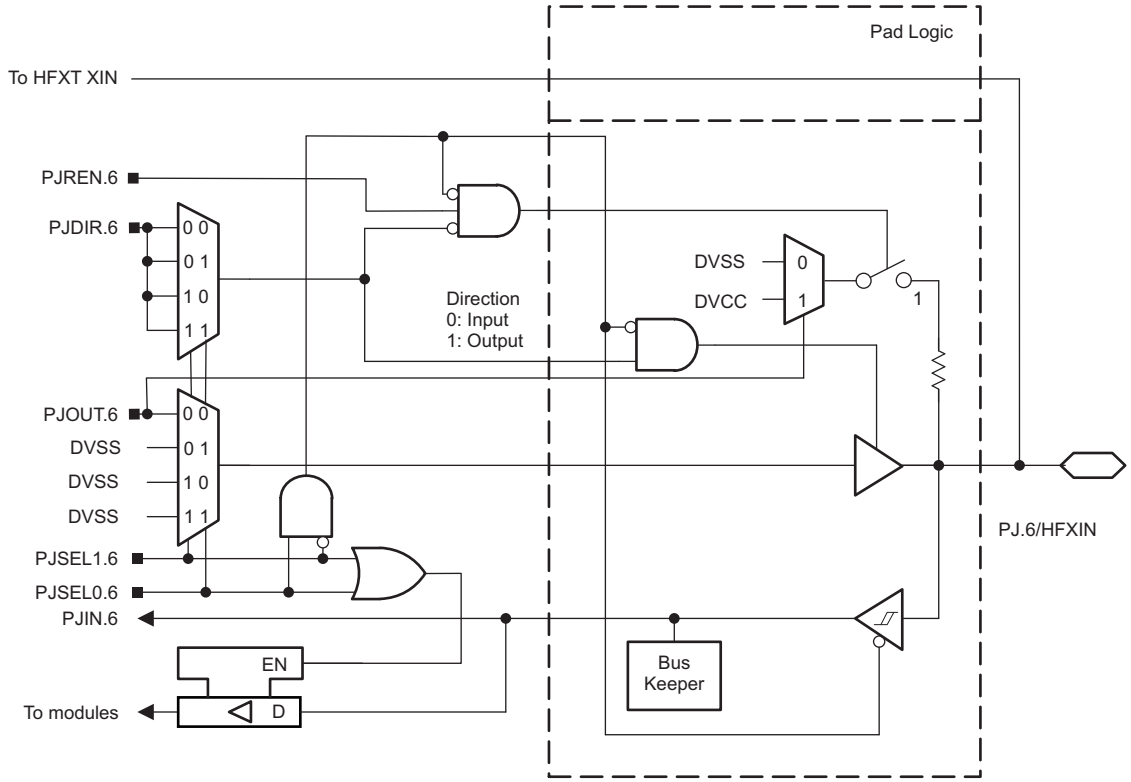
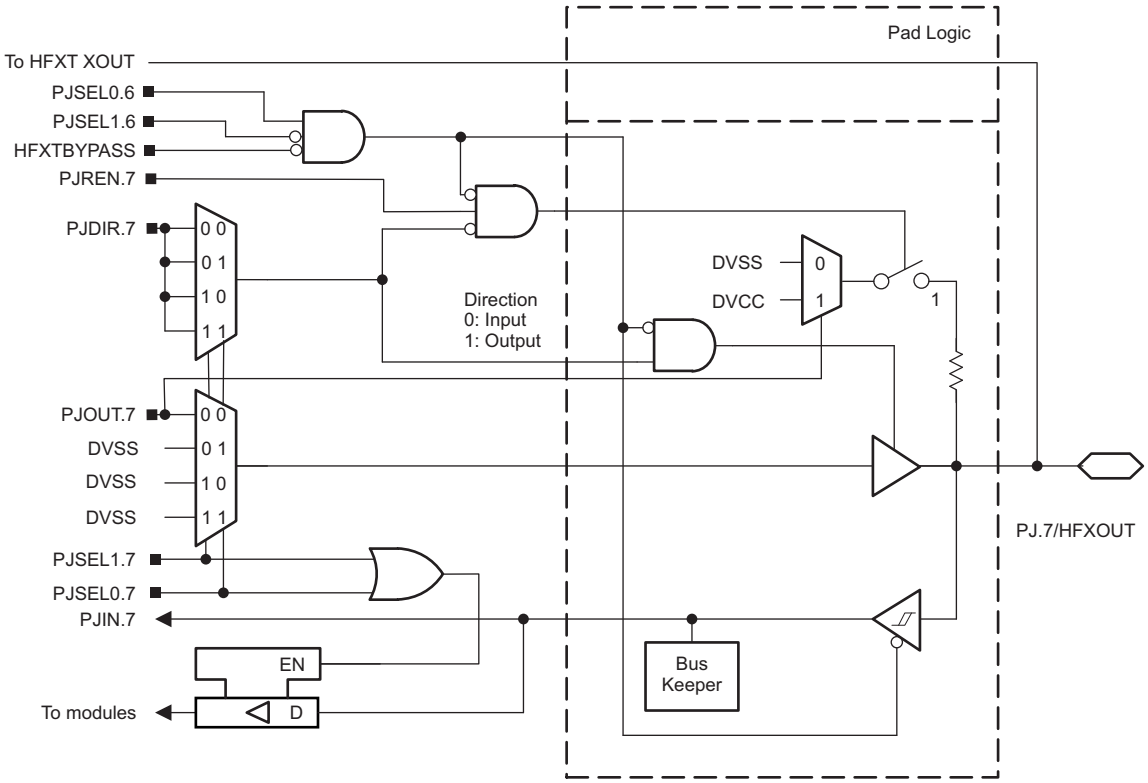
6.11.23.19 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

図 6-11 and 図 6-12 show the port diagrams. 表 6-41 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-11. Port PJ (PJ.6) Diagram



NOTE: Functional representation only.

図 6-12. Port PJ (PJ.7) Diagram

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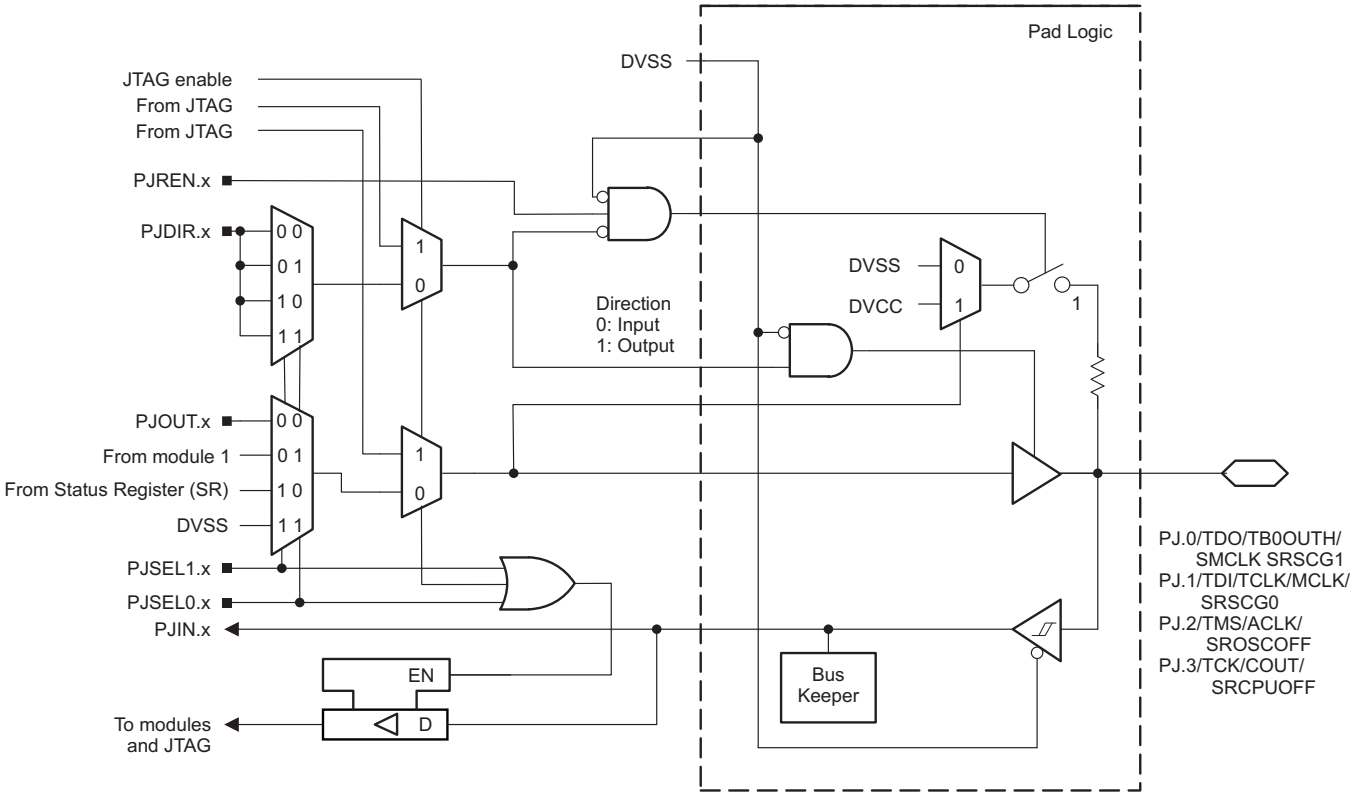
表 6-41. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)					
			PJDIR.x	PJSEL1.7	PJSEL0.7	PJSEL1.6	PJSEL0.6	HFXT BYPASS
PJ.6/HFXIN	6	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		HFXIN crystal mode (2)	X	X	X	0	1	0
		HFXIN bypass mode (2)	X	X	X	0	1	1
PJ.7/HFXOUT	7	PJ.7 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		Internally tied to DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		HFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are don't care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.
(3) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.
(4) With PJSEL0.7 = 1 or PJSEL1.7 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

6.11.23.20 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

図 6-13 shows the port diagram. 表 6-42 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-13. Port PJ (PJ.0 to PJ.3) Diagram

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表 6-42. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)		
			PJDIR.x	PJSEL1.x	PJSEL0.x
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1	0	PJ.0 (I/O) (2)	I: 0; O: 1	0	0
		TDO (3)	X	X	X
		TB0OUTH	0	0	1
		SMCLK (4)	1		
		N/A	0	1	0
		CPU Status Register Bit SCG1	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.1/TDI/TCLK/ MCLK/SRSCG0	1	PJ.1 (I/O) (2)	I: 0; O: 1	0	0
		TDI/TCLK (3) (5)	X	X	X
		N/A	0	0	1
		MCLK	1		
		N/A	0	1	0
		CPU Status Register Bit SCG0	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.2/TMS/ACLK/ SROSCOFF	2	PJ.2 (I/O) (2)	I: 0; O: 1	0	0
		TMS (3) (5)	X	X	X
		N/A	0	0	1
		ACLK	1		
		N/A	0	1	0
		CPU Status Register Bit OSCOFF	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.3/TCK/COUT/ SRCPUOFF	3	PJ.3 (I/O) (2)	I: 0; O: 1	0	0
		TCK (3) (5)	X	X	X
		N/A	0	0	1
		COUT	1		
		N/A	0	1	0
		CPU Status Register Bit CPUOFF	1		
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made through the SYS module or by the Spy-Bi-Wire 4-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPD.x bits have an effect in these cases.
(4) Do not use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternative SMCLK output pin.
(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.12 Device Descriptors (TLV)

表 6-43 summarizes the Device IDs. 表 6-44 lists the contents of the device descriptor tag-length-value (TLV) structure for each device type.

表 6-43. Device ID

DEVICE	DEVICE ID	
	01A05h	01A04h
MSP430FR6979	081h	0AEh
MSP430FR6977	081h	0ACh
MSP430FR6928	081h	0B3h
MSP430FR6927	081h	0B2h
MSP430FR69791	081h	0AEh
MSP430FR69271	081h	0B2h

表 6-44. Device Descriptor Table(1)

DESCRIPTION		MSP430FRxxxx (UART BSL)		MSP430FRxxxx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Info Block	Info length	01A00h	06h	01A00h	06h
	CRC length	01A01h	06h	01A01h	06h
	CRC value	01A02h	Per unit	01A02h	Per unit
		01A03h	Per unit	01A03h	Per unit
	Device ID	01A04h	See 表 6-43.	01A04h	See 表 6-43.
	Device ID	01A05h		01A05h	
	Hardware revision	01A06h	Per unit	01A06h	Per unit
	Firmware revision	01A07h	Per unit	01A07h	Per unit
Die Record	Die record tag	01A08h	08h	01A08h	08h
	Die record length	01A09h	0Ah	01A09h	0Ah
	Lot/wafer ID	01A0Ah	Per unit	01A0Ah	Per unit
		01A0Bh	Per unit	01A0Bh	Per unit
		01A0Ch	Per unit	01A0Ch	Per unit
		01A0Dh	Per unit	01A0Dh	Per unit
	Die X position	01A0Eh	Per unit	01A0Eh	Per unit
		01A0Fh	Per unit	01A0Fh	Per unit
	Die Y position	01A10h	Per unit	01A10h	Per unit
		01A11h	Per unit	01A11h	Per unit
	Test results	01A12h	Per unit	01A12h	Per unit
		01A13h	Per unit	01A13h	Per unit

(1) NA = Not applicable
Per unit = Content can differ from device to device

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表 6-44. Device Descriptor Table[1] (continued)

DESCRIPTION		MSP430FRxxxx (UART BSL)		MSP430FRxxxx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
ADC12B Calibration	ADC12B calibration tag	01A14h	11h	01A14h	11h
	ADC12B calibration length	01A15h	10h	01A15h	10h
	ADC gain factor[2]	01A16h	Per unit	01A16h	Per unit
		01A17h	Per unit	01A17h	Per unit
	ADC offset[3]	01A18h	Per unit	01A18h	Per unit
		01A19h	Per unit	01A19h	Per unit
	ADC 1.2-V reference Temperature sensor 30°C	01A1Ah	Per unit	01A1Ah	Per unit
		01A1Bh	Per unit	01A1Bh	Per unit
	ADC 1.2-V reference Temperature sensor 85°C	01A1Ch	Per unit	01A1Ch	Per unit
		01A1Dh	Per unit	01A1Dh	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	Per unit	01A1Eh	Per unit
		01A1Fh	Per unit	01A1Fh	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	Per unit	01A20h	Per unit
		01A21h	Per unit	01A21h	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	Per unit	01A22h	Per unit
		01A23h	Per unit	01A23h	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	Per unit	01A24h	Per unit
		01A25h	Per unit	01A25h	Per unit
REF Calibration	REF calibration tag	01A26h	12h	01A26h	12h
	REF calibration length	01A27h	06h	01A27h	06h
	REF 1.2-V reference	01A28h	Per unit	01A28h	Per unit
		01A29h	Per unit	01A29h	Per unit
	REF 2.0-V reference	01A2Ah	Per unit	01A2Ah	Per unit
		01A2Bh	Per unit	01A2Bh	Per unit
	REF 2.5-V reference	01A2Ch	Per unit	01A2Ch	Per unit
		01A2Dh	Per unit	01A2Dh	Per unit

(2) ADC gain: The gain correction factor is measured using the internal voltage reference with REFOUT = 0. Other settings (for example, with REFOUT = 1) can result in different correction factors.
(3) ADC offset: The offset correction factor is measured using the internal 2.5-V reference.

表 6-44. Device Descriptor Table[1] (continued)

DESCRIPTION		MSP430FRxxxx (UART BSL)		MSP430FRxxxx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Random Number	128-bit random number tag	01A2Eh	15h	01A2Eh	15h
	Random number length	01A2Fh	10h	01A2Fh	10h
	128-bit random number[4]	01A30h	Per unit	01A30h	Per unit
		01A31h	Per unit	01A31h	Per unit
		01A32h	Per unit	01A32h	Per unit
		01A33h	Per unit	01A33h	Per unit
		01A34h	Per unit	01A34h	Per unit
		01A35h	Per unit	01A35h	Per unit
		01A36h	Per unit	01A36h	Per unit
		01A37h	Per unit	01A37h	Per unit
		01A38h	Per unit	01A38h	Per unit
		01A39h	Per unit	01A39h	Per unit
		01A3Ah	Per unit	01A3Ah	Per unit
		01A3Bh	Per unit	01A3Bh	Per unit
		01A3Ch	Per unit	01A3Ch	Per unit
		01A3Dh	Per unit	01A3Dh	Per unit
		01A3Eh	Per unit	01A3Eh	Per unit
		01A3Fh	Per unit	01A3Fh	Per unit
BSL Configuration	BSL tag	01A40h	1Ch	01A40h	1Ch
	BSL length	01A41h	02h	01A41h	02h
	BSL interface	01A42h	00h	01A42h	01h
	BSL interface configuration	01A43h	00h	01A43h	48h

(4) 128-bit random number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

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6.13 Memory

表 6-45 summarizes the memory map.

表 6-45. Memory Organization(1)

		MSP430FRxxx9(1)	MSP430FRxxx8(1)	MSP430FRxxx7(1)
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Total Size	127KB 00FFFFh–00FF80h 023FFFh–004400h	95KB 00FFFFh–00FF80h 01BFFFh–004400h	63KB 00FFFFh–00FF80h 013FFFh–004400h
RAM	Sect 1	2KB 0023FFh–001C00h	2KB 0023FFh–001C00h	2KB 0023FFh–001C00h
Boot memory (ROM)		256 B 001BFFh–001B00h	256 B 001BFFh–001B00h	256 B 001BFFh–001B00h
Device Descriptor Info (TLV)		256 B 001AFFh–001A00h	256 B 001AFFh–001A00h	256 B 001AFFh–001A00h
Information memory (FRAM)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootloader (BSL) memory (ROM)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–000020h	4KB 000FFFh–000020h	4KB 000FFFh–000020h
Tiny RAM	Size	26 B 000001Fh–000006h	26 B 000001Fh–000006h	26 B 000001Fh–000006h
Reserved (Read Only)	Size	6 B 000005h–000000h	6 B 000005h–000000h	6 B 000005h–000000h

(1) All address space not listed is considered vacant memory.

6.13.1 Peripheral File Map

表 6-46 lists the base address for each available peripheral. 表 6-47 through 表 6-81 list the registers and their offsets for each peripheral.

表 6-46. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see 表 6-47)	0100h	000h–01Fh
PMM (see 表 6-48)	0120h	000h–01Fh
FRAM Control (see 表 6-49)	0140h	000h–00Fh
CRC16 (see 表 6-50)	0150h	000h–007h
RAM Controller (see 表 6-51)	0158h	000h–001h
Watchdog Timer (see 表 6-52)	015Ch	000h–001h
CS (see 表 6-53)	0160h	000h–00Fh
SYS (see 表 6-54)	0180h	000h–01Fh
Shared Reference (see 表 6-55)	01B0h	000h–001h
Port P1, P2 (see 表 6-56)	0200h	000h–01Fh
Port P3, P4 (see 表 6-57)	0220h	000h–01Fh
Port P5, P6 (see 表 6-58)	0240h	000h–01Fh
Port P7, P8 (see 表 6-59)	0260h	000h–01Fh
Port P9, P10 (see 表 6-60)	0280h	000h–01Fh
Port PJ (see 表 6-61)	0320h	000h–01Fh
Timer_A TA0 (see 表 6-62)	0340h	000h–02Fh
Timer_A TA1 (see 表 6-63)	0380h	000h–02Fh
Timer_B TB0 (see 表 6-64)	03C0h	000h–02Fh
Timer_A TA2 (see 表 6-65)	0400h	000h–02Fh
Capacitive Touch I/O 0 (see 表 6-66)	0430h	000h–00Fh
Timer_A TA3 (see 表 6-67)	0440h	000h–02Fh
Capacitive Touch I/O 1 (see 表 6-68)	0470h	000h–00Fh
Real-Time Clock (RTC_C) (see 表 6-69)	04A0h	000h–01Fh
32-Bit Hardware Multiplier (see 表 6-70)	04C0h	000h–02Fh
DMA General Control (see 表 6-71)	0500h	000h–00Fh
DMA Channel 0 (see 表 6-71)	0510h	000h–00Fh
DMA Channel 1 (see 表 6-71)	0520h	000h–00Fh
DMA Channel 2 (see 表 6-71)	0530h	000h–00Fh
MPU (see 表 6-72)	05A0h	000h–00Fh
eUSCI_A0 (see 表 6-73)	05C0h	000h–01Fh
eUSCI_A1 (see 表 6-74)	05E0h	000h–01Fh
eUSCI_B0 (see 表 6-75)	0640h	000h–02Fh
eUSCI_B1 (see 表 6-76)	0680h	000h–02Fh
ADC12_B (see 表 6-77)	0800h	000h–09Fh
Comparator_E (see 表 6-78)	08C0h	000h–00Fh
CRC32 (see 表 6-79)	0980h	000h–02Fh
AES (see 表 6-80)	09C0h	000h–00Fh
LCD_C (see 表 6-81)	0A00h	000h–05Fh

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表 6-47. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 6-48. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

表 6-49. FRAM Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

表 6-50. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

表 6-51. RAM Controller Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM controller control 0	RCCTL0	00h

表 6-52. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 6-53. CS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch

表 6-54. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
JTAG mailbox control	SYSJMBC	06h

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表 6-54. SYS Registers (Base Address: 0180h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

表 6-55. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

表 6-56. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

表 6-57. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh

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表 6-57. Port P3, P4 Registers (Base Address: 0220h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

表 6-58. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P5 selection 1	P5SEL1	0Ch
Reserved		0Eh
Port P5 complement selection	P5SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 selection 0	P6SEL0	0Bh
Port P6 selection 1	P6SEL1	0Dh
Port P6 complement selection	P6SELC	17h
Reserved		1Eh
Reserved		19h
Reserved		1Bh
Reserved		1Dh

表 6-59. Port P7, P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 resistor enable	P7REN	06h

表 6-59. Port P7, P8 Registers (Base Address: 0260h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 selection 0	P7SEL0	0Ah
Port P7 selection 1	P7SEL1	0Ch
Reserved		0Eh
Port P7 complement selection	P7SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 resistor enable	P8REN	07h
Port P8 selection 0	P8SEL0	0Bh
Port P8 selection 1	P8SEL1	0Dh
Port P8 complement selection	P8SELC	17h
Reserved		1Eh
Reserved		19h
Reserved		1Bh
Reserved		1Dh

表 6-60. Port P9, P10 Registers (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 resistor enable	P9REN	06h
Port P9 selection 0	P9SEL0	0Ah
Port P9 selection 1	P9SEL1	0Ch
Reserved		0Eh
Port P9 complement selection	P9SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch
Port P10 input	P10IN	01h
Port P10 output	P10OUT	03h
Port P10 direction	P10DIR	05h
Port P10 resistor enable	P10REN	07h
Port P10 selection 0	P10SEL0	0Bh
Port P10 selection 1	P10SEL1	0Dh
Port P10 complement selection	P10SELC	17h
Reserved		1Eh
Reserved		19h
Reserved		1Bh
Reserved		1Dh

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表 6-61. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ selection 0	PJSEL0	0Ah
Port PJ selection 1	PJSEL1	0Ch
Port PJ complement selection	PJSELC	16h

表 6-62. Timer_A TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

表 6-63. Timer_A TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

表 6-64. Timer_B TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah

表 6-64. Timer_B TB0 Registers (Base Address: 03C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

表 6-65. Timer_A TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

表 6-66. Capacitive Touch I/O 0 Registers (Base Address: 0430h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 0 control	CAPTIO0CTL	0Eh

表 6-67. Timer_A TA3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
Capture/compare control 2	TA3CCTL2	06h
Capture/compare control 3	TA3CCTL3	08h
Capture/compare control 4	TA3CCTL4	0Ah
TA3 counter	TA3R	10h
Capture/compare 0	TA3CCR0	12h
Capture/compare 1	TA3CCR1	14h
Capture/compare 2	TA3CCR2	16h
Capture/compare 3	TA3CCR3	18h
Capture/compare 4	TA3CCR4	1Ah
TA3 expansion 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

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表 6-68. Capacitive Touch I/O 1 Registers (Base Address: 0470h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 1 control	CAPTIO1CTL	0Eh

表 6-69. RTC_C Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC password	RTCPWD	01h
RTC control 1	RTCCTL1	02h
RTC control 3	RTCCTL3	03h
RTC offset calibration	RTCOCAL	04h
RTC temperature compensation	RTCTCMP	06h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter 1	RTCSEC/RTCNT1	10h
RTC minutes/counter 2	RTCMIN/RTCNT2	11h
RTC hours/counter 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year	RTCYEAR	16h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion	BIN2BCD	1Ch
BCD-to-Binary conversion	BCD2BIN	1Eh

表 6-70. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh

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表 6-70. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

表 6-71. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

表 6-72. MPU Control Registers (Base Address: 05A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU control 0	MPUCTL0	00h
MPU control 1	MPUCTL1	02h
MPU segmentation border 2	MPUSEGB2	04h
MPU segmentation border 1	MPUSEGB1	06h
MPU access management	MPUSAM	08h
MPU IP control 0	MPUIPC0	0Ah
MPU IP encapsulation segment border 2	MPUIPSEGB2	0Ch
MPU IP encapsulation segment border 1	MPUIPSEGB1	0Eh

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表 6-73. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI _A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status word	UCA0STATW	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

表 6-74. eUSCI_A1 Registers (Base Address:05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI _A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status word	UCA1STATW	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

表 6-75. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch

表 6-75. eUSCI_B0 Registers (Base Address: 0640h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

表 6-76. eUSCI_B1 Registers (Base Address: 0680h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB1CTLW0	00h
eUSCI_B control word 1	UCB1CTLW1	02h
eUSCI_B bit rate 0	UCB1BR0	06h
eUSCI_B bit rate 1	UCB1BR1	07h
eUSCI_B status word	UCB1STATW	08h
eUSCI_B byte counter threshold	UCB1TBCNT	0Ah
eUSCI_B receive buffer	UCB1RXBUF	0Ch
eUSCI_B transmit buffer	UCB1TXBUF	0Eh
eUSCI_B I2C own address 0	UCB1I2COA0	14h
eUSCI_B I2C own address 1	UCB1I2COA1	16h
eUSCI_B I2C own address 2	UCB1I2COA2	18h
eUSCI_B I2C own address 3	UCB1I2COA3	1Ah
eUSCI_B received address	UCB1ADDRX	1Ch
eUSCI_B address mask	UCB1ADDMASK	1Eh
eUSCI_B I2C slave address	UCB1I2CSA	20h
eUSCI_B interrupt enable	UCB1IE	2Ah
eUSCI_B interrupt flags	UCB1IFG	2Ch
eUSCI_B interrupt vector word	UCB1IV	2Eh

表 6-77. ADC12_B Registers (Base Address: 0800h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B control 0	ADC12CTL0	00h
ADC12_B control 1	ADC12CTL1	02h
ADC12_B control 2	ADC12CTL2	04h
ADC12_B control 3	ADC12CTL3	06h
ADC12_B window comparator low threshold	ADC12LO	08h
ADC12_B window comparator high threshold	ADC12HI	0Ah
ADC12_B interrupt flag 0	ADC12IFGR0	0Ch
ADC12_B Interrupt flag 1	ADC12IFGR1	0Eh
ADC12_B interrupt flag 2	ADC12IFGR2	10h
ADC12_B interrupt enable 0	ADC12IER0	12h
ADC12_B interrupt enable 1	ADC12IER1	14h
ADC12_B interrupt enable 2	ADC12IER2	16h
ADC12_B interrupt vector	ADC12IV	18h
ADC12_B memory control 0	ADC12MCTL0	20h
ADC12_B memory control 1	ADC12MCTL1	22h
ADC12_B memory control 2	ADC12MCTL2	24h
ADC12_B memory control 3	ADC12MCTL3	26h
ADC12_B memory control 4	ADC12MCTL4	28h

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表 6-77. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B memory control 5	ADC12MCTL5	2Ah
ADC12_B memory control 6	ADC12MCTL6	2Ch
ADC12_B memory control 7	ADC12MCTL7	2Eh
ADC12_B memory control 8	ADC12MCTL8	30h
ADC12_B memory control 9	ADC12MCTL9	32h
ADC12_B memory control 10	ADC12MCTL10	34h
ADC12_B memory control 11	ADC12MCTL11	36h
ADC12_B memory control 12	ADC12MCTL12	38h
ADC12_B memory control 13	ADC12MCTL13	3Ah
ADC12_B memory control 14	ADC12MCTL14	3Ch
ADC12_B memory control 15	ADC12MCTL15	3Eh
ADC12_B memory control 16	ADC12MCTL16	40h
ADC12_B memory control 17	ADC12MCTL17	42h
ADC12_B memory control 18	ADC12MCTL18	44h
ADC12_B memory control 19	ADC12MCTL19	46h
ADC12_B memory control 20	ADC12MCTL20	48h
ADC12_B memory control 21	ADC12MCTL21	4Ah
ADC12_B memory control 22	ADC12MCTL22	4Ch
ADC12_B memory control 23	ADC12MCTL23	4Eh
ADC12_B memory control 24	ADC12MCTL24	50h
ADC12_B memory control 25	ADC12MCTL25	52h
ADC12_B memory control 26	ADC12MCTL26	54h
ADC12_B memory control 27	ADC12MCTL27	56h
ADC12_B memory control 28	ADC12MCTL28	58h
ADC12_B memory control 29	ADC12MCTL29	5Ah
ADC12_B memory control 30	ADC12MCTL30	5Ch
ADC12_B memory control 31	ADC12MCTL31	5Eh
ADC12_B memory 0	ADC12MEM0	60h
ADC12_B memory 1	ADC12MEM1	62h
ADC12_B memory 2	ADC12MEM2	64h
ADC12_B memory 3	ADC12MEM3	66h
ADC12_B memory 4	ADC12MEM4	68h
ADC12_B memory 5	ADC12MEM5	6Ah
ADC12_B memory 6	ADC12MEM6	6Ch
ADC12_B memory 7	ADC12MEM7	6Eh
ADC12_B memory 8	ADC12MEM8	70h
ADC12_B memory 9	ADC12MEM9	72h
ADC12_B memory 10	ADC12MEM10	74h
ADC12_B memory 11	ADC12MEM11	76h
ADC12_B memory 12	ADC12MEM12	78h
ADC12_B memory 13	ADC12MEM13	7Ah
ADC12_B memory 14	ADC12MEM14	7Ch
ADC12_B memory 15	ADC12MEM15	7Eh
ADC12_B memory 16	ADC12MEM16	80h
ADC12_B memory 17	ADC12MEM17	82h
ADC12_B memory 18	ADC12MEM18	84h
ADC12_B memory 19	ADC12MEM19	86h

表 6-77. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B memory 20	ADC12MEM20	88h
ADC12_B memory 21	ADC12MEM21	8Ah
ADC12_B memory 22	ADC12MEM22	8Ch
ADC12_B memory 23	ADC12MEM23	8Eh
ADC12_B memory 24	ADC12MEM24	90h
ADC12_B memory 25	ADC12MEM25	92h
ADC12_B memory 26	ADC12MEM26	94h
ADC12_B memory 27	ADC12MEM27	96h
ADC12_B memory 28	ADC12MEM28	98h
ADC12_B memory 29	ADC12MEM29	9Ah
ADC12_B memory 30	ADC12MEM30	9Ch
ADC12_B memory 31	ADC12MEM31	9Eh

表 6-78. Comparator_E Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control 0	CECTL0	00h
Comparator control 1	CECTL1	02h
Comparator control 2	CECTL2	04h
Comparator control 3	CECTL3	06h
Comparator interrupt	CEINT	0Ch
Comparator interrupt vector word	CEIV	0Eh

表 6-79. CRC32 Registers (Base Address: 0980h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC32 data input	CRC32DIW0	00h
Reserved		02h
Reserved		04h
CRC32 data input reverse	CRC32DIRBW0	06h
CRC32 initialization and result word 0	CRC32INIRESW0	08h
CRC32 initialization and result word 1	CRC32INIRESW1	0Ah
CRC32 result reverse word 1	CRC32RESRW1	0Ch
CRC32 result reverse word 0	CRC32RESRW1	0Eh
CRC16 data input	CRC16DIW0	10h
Reserved		12h
Reserved		14h
CRC16 data input reverse	CRC16DIRBW0	16h
CRC16 initialization and result word 0	CRC16INIRESW0	18h
Reserved		1Ah
Reserved		1Ch
CRC16 result reverse word 0	CRC16RESRW1	1Eh
Reserved		20h
Reserved		22h
Reserved		24h
Reserved		26h
Reserved		28h
Reserved		2Ah
Reserved		2Ch

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表 6-79. CRC32 Registers (Base Address: 0980h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Reserved		2Eh

表 6-80. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
AES accelerator control 0	AESACTL0	00h
AES accelerator control 1	AESACTL1	02h
AES accelerator status	AESASTAT	04h
AES accelerator key	AESAKEY	06h
AES accelerator data in	AESADIN	008h
AES accelerator data out	AESADOUT	00Ah
AES accelerator XORed data in	AESAXDIN	00Ch
AES accelerator XORed data in (no trigger)	AESAXIN	00Eh

表 6-81. LCD_C Registers (Base Address: 0A00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_C control 0	LCDCCTL0	000h
LCD_C control 1	LCDCCTL1	002h
LCD_C blinking control	LCDCBLKCTL	004h
LCD_C memory control	LCDCMEMCTL	006h
LCD_C voltage control	LCDCVCTL	008h
LCD_C port control 0	LCDCPCTL0	00Ah
LCD_C port control 1	LCDCPCTL1	00Ch
LCD_C port control 2	LCDCPCTL2	00Eh
LCD_C charge pump control	LCDCCPCTL	012h
LCD_C interrupt vector	LCDCIV	01Eh
Static and 2 to 4 mux modes		
LCD_C memory 1	LCDM1	020h
LCD_C memory 2	LCDM2	021h
LCD_C memory 3	LCDM3	022h
LCD_C memory 4	LCDM4	023h
LCD_C memory 5	LCDM5	024h
LCD_C memory 6	LCDM6	025h
LCD_C memory 7	LCDM7	026h
LCD_C memory 8	LCDM8	027h
LCD_C memory 9	LCDM9	028h
LCD_C memory 10	LCDM10	029h
LCD_C memory 11	LCDM11	02Ah
LCD_C memory 12	LCDM12	02Bh
LCD_C memory 13	LCDM13	02Ch
LCD_C memory 14	LCDM14	02Dh
LCD_C memory 15	LCDM15	02Eh
LCD_C memory 16	LCDM16	02Fh
LCD_C memory 17	LCDM17	030h
LCD_C memory 18	LCDM18	031h
LCD_C memory 19	LCDM19	032h
LCD_C memory 20	LCDM20	033h
LCD_C memory 21	LCDM21	034h

表 6-81. LCD_C Registers (Base Address: 0A00h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_C memory 22	LCDM22	035h
Reserved		036h
Reserved		037h
LCD_C blinking memory 1	LCDBM1	040h
LCD_C blinking memory 2	LCDBM2	041h
LCD_C blinking memory 3	LCDBM3	042h
LCD_C blinking memory 4	LCDBM4	043h
LCD_C blinking memory 5	LCDBM5	044h
LCD_C blinking memory 6	LCDBM6	045h
LCD_C blinking memory 7	LCDBM7	046h
LCD_C blinking memory 8	LCDBM8	047h
LCD_C blinking memory 9	LCDBM9	048h
LCD_C blinking memory 10	LCDBM10	049h
LCD_C blinking memory 11	LCDBM11	04Ah
LCD_C blinking memory 12	LCDBM12	04Bh
LCD_C blinking memory 13	LCDBM13	04Ch
LCD_C blinking memory 14	LCDBM14	04Dh
LCD_C blinking memory 15	LCDBM15	04Eh
LCD_C blinking memory 16	LCDBM16	04Fh
LCD_C blinking memory 17	LCDBM17	050h
LCD_C blinking memory 18	LCDBM18	051h
LCD_C blinking memory 19	LCDBM19	052h
LCD_C blinking memory 20	LCDBM20	053h
LCD_C blinking memory 21	LCDBM21	054h
LCD_C blinking memory 22	LCDBM22	055h
Reserved		056h
Reserved		057h
5 to 8 mux modes		
LCD_C memory 1	LCDM1	020h
LCD_C memory 2	LCDM2	021h
LCD_C memory 3	LCDM3	022h
LCD_C memory 4	LCDM4	023h
LCD_C memory 5	LCDM5	024h
LCD_C memory 6	LCDM6	025h
LCD_C memory 7	LCDM7	026h
LCD_C memory 8	LCDM8	027h
LCD_C memory 9	LCDM9	028h
LCD_C memory 10	LCDM10	029h
LCD_C memory 11	LCDM11	02Ah
LCD_C memory 12	LCDM12	02Bh
LCD_C memory 13	LCDM13	02Ch
LCD_C memory 14	LCDM14	02Dh
LCD_C memory 15	LCDM15	02Eh
LCD_C memory 16	LCDM16	02Fh
LCD_C memory 17	LCDM17	030h
LCD_C memory 18	LCDM18	031h
LCD_C memory 19	LCDM19	032h

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表 6-81. LCD_C Registers (Base Address: 0A00h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_C memory 20	LCDM20	033h
LCD_C memory 21	LCDM21	034h
LCD_C memory 22	LCDM22	035h
LCD_C memory 23	LCDM23	036h
LCD_C memory 24	LCDM24	037h
LCD_C memory 25	LCDM25	038h
LCD_C memory 26	LCDM26	039h
LCD_C memory 27	LCDM27	03Ah
LCD_C memory 28	LCDM28	03Bh
LCD_C memory 29	LCDM29	03Ch
LCD_C memory 30	LCDM30	03Dh
LCD_C memory 31	LCDM31	03Eh
LCD_C memory 32	LCDM32	03Fh
LCD_C memory 33	LCDM33	040h
LCD_C memory 34	LCDM34	041h
LCD_C memory 35	LCDM35	042h
LCD_C memory 36	LCDM36	043h
LCD_C memory 37	LCDM37	044h
LCD_C memory 38	LCDM38	045h
LCD_C memory 39	LCDM39	046h
LCD_C memory 40	LCDM40	047h
LCD_C memory 41	LCDM41	048h
LCD_C memory 42	LCDM42	049h
LCD_C memory 43	LCDM43	04Ah

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in 6.12.

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in 6.12.

6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in *MSP430 Programming With the JTAG Interface*.

7 Applications, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

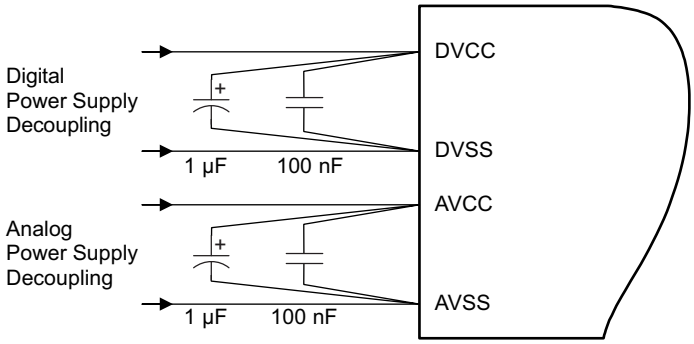

図 7-1. Power Supply Decoupling

7.1.2 External Oscillator

Depending on the device variant (see Section 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, terminate them according to Section 4.4.

図 7-2 shows a typical connection diagram.

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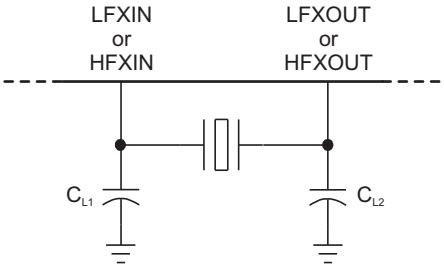


図 7-2. Typical Crystal Connection

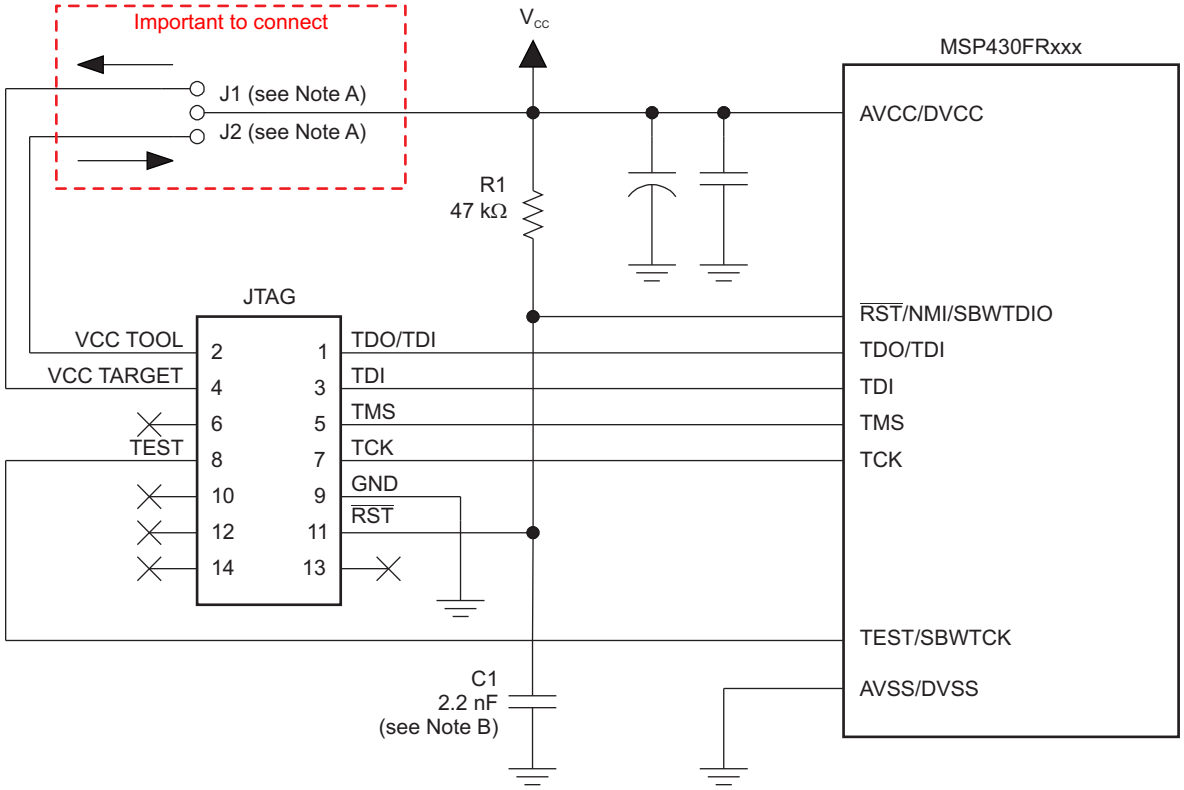
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 図 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 図 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 図 7-3 and 図 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.



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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
B. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-3. Signal Connections for 4-Wire JTAG Communication

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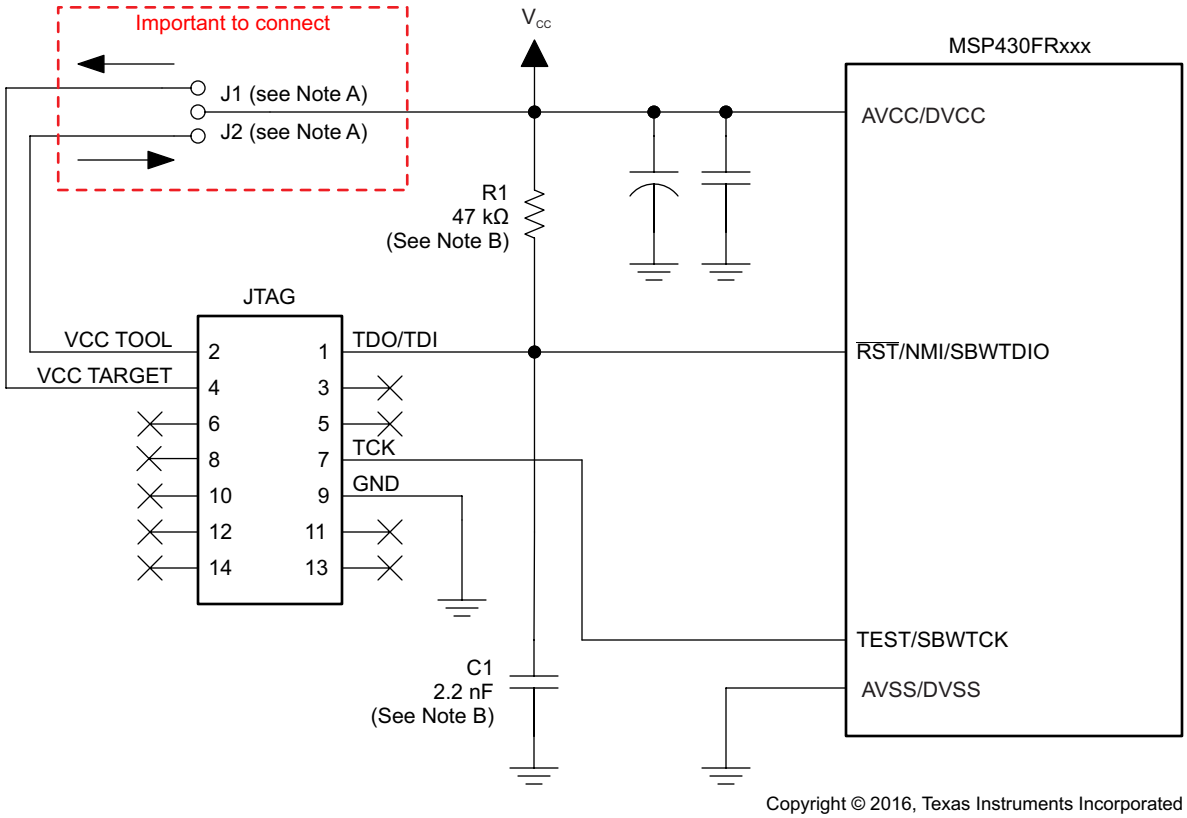

A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

See the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.4.

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- See *Circuit Board Layout Techniques* for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.7 Do's and Don'ts

TI recommends powering the AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC12_B Peripheral

7.2.1.1 Partial Schematic

図 7-5 shows the recommended decoupling circuit when an external voltage reference is used.

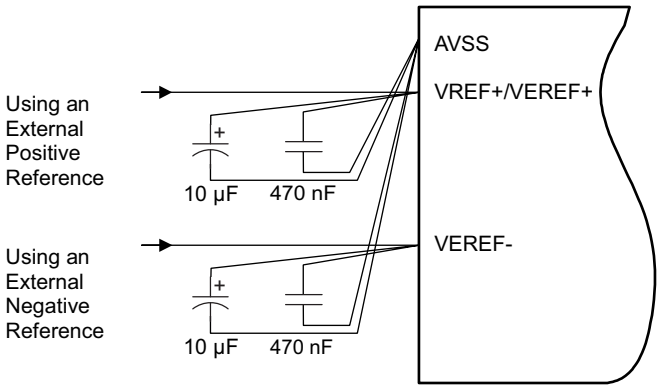

図 7-5. ADC12_B Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 7.1.1 combined with the connections shown in 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

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図 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the Reference module's $I_{O(VREF+)}$ specification.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 470-nF bypass capacitor is used to filter out any high-frequency noise.

7.2.1.3 Detailed Design Procedure

For additional design information, see *Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC*.

7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see 図 7-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

7.2.2 LCD_C Peripheral

7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, there is flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU, which (assuming that the correct choices are made) can be advantageous for the PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for an example of connecting a 4-mux LCD with 40 segment lines that has a total of 4 × 40 = 160 individually addressable LCD segments to an MSP430FR6989, see the *Water Meter Reference Design for Two LC Sensors, Using Extended Scan Interface (ESI)*.

7.2.2.2 Design Requirements

Due to the flexibility of the LCD_C peripheral module to accommodate various segment-based LCDs, selecting the correct display for the application in combination with determining specific design requirements is often an iterative process. There can be well defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use, and which are required by other application functions, and what the power budget is, to name just a few. TI recommends reviewing the LCD_C peripheral module chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* during the initial design requirements and decision process. 表 7-1 is a brief overview over different choices that can be made and their effects.

表 7-1. LCD Features and Use Cases

OPTION OR FEATURE	IMPACT OR USE CASE
Multiplexed LCD	• Enable displays with more segments • Use fewer device pins • LCD contrast decreases as mux level increases • Power consumption increases with mux level • Requires multiple intermediate bias voltages
Static LCD	• Limited number of segments that can be addressed • Use a relatively large number of device pins • Use the least amount of power • Use only V_{CC} and GND to drive LCD signals
Internal bias generation	• Simpler solution – no external circuitry • Independent of V_{LCD} source • Somewhat higher power consumption
External bias generation	• Requires external resistor ladder divider • Resistor size depends on display • Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load) • External resistor ladder divider can be stabilized through capacitors to reduce ripple
Internal charge pump	• Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications) • Programmable voltage levels allow software-driven contrast control • Requires an external capacitor on the LCDCAP pin • Higher current consumption than simply using V_{CC} for the LCD driver

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7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_C peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is recommended:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, the segment Sx and common COMx signals are connected to respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_C module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_C module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCDMx register. And consecutive segments are mapped to consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing of the most convenient memory layout needs to be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see the *LCD_C Controller* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

For additional design information, see *Designing With MSP430 and Segment LCDs*.

7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the V_{SS} pins of the MCU.

For an example layout of connecting a 4-mux LCD with 40 segments to an MSP430FR6989 and using the charge pump feature, see the *Water Meter Reference Design for Two LC Sensors, Using Extended Scan Interface (ESI)*.

8 デバイスおよびドキュメントのサポート

8.1 使い始めと次の手順

MSP430ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「Getting Started」ページを参照してください。

8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

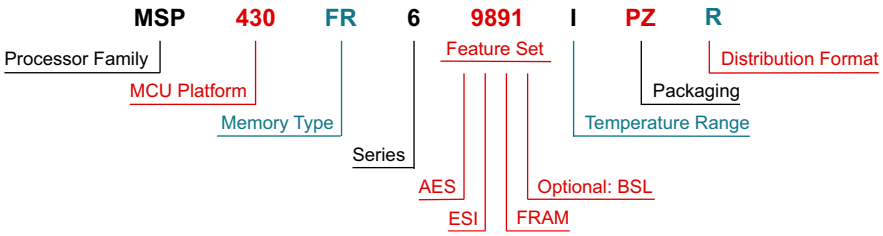
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon			
MCU Platform	430 = TI's 16-bit MSP430 Low-Power Microcontroller Platform			
Memory Type	FR = FRAM			
Series	6 = FRAM 6 Series up to 16 MHz with LCD 5 = FRAM 5 Series up to 16 MHz without LCD			
Feature Set	**First Digit: AES** 9 = AES 8 = No AES	**Second Digit: Extended Scan Interface** 8 = ESI 7 = No ESI 2 = No ESI, LCD, 64 pins	**Third Digit: FRAM (KB)** 9 = 128 8 = 96 7 = 64 6 = 48	**Optional Fourth Digit: BSL** 1 = I^2C No value = UART
Temperature Range	I = –40°C to 85°C			
Packaging	www.ti.com/packaging			
Distribution Format	T = Small reel R = Large reel No markings = Tube or tray			

NOTE: この図は、利用可能な機能とオプションの完全なリストではなく、与えられたデバイスまたはファミリについて、これらの機能とオプションのすべてが利用できることを示すものでもありません。

図 8-1. デバイスの項目表記 - 型番の読み方

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8.3 ツールとソフトウェア

表 8-1 は、MSP430FR697x(1)およびMSP430FR692x(1)マイクロコントローラでサポートされるデバッグ機能の一覧です。利用可能な機能の詳細については、『*MSP430用Code Composer Studio ユーザー・ガイド*』を参照してください。

表 8-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式 JTAG	2線式 JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMX.5デバッグ・サポート	EnergyTrace++テクノロジ
MSP430Xv2	○	○	3	○	○	×	×	○	○

EnergyTrace™ テクノロジは、Code Composer Studioのバージョン6.0およびそれ以降でサポートされています。これには特化したデバッガ回路が必要で、第2世代のオンボードeZ-FETフラッシュ・エミュレーション・ツール、および第2世代のスタンドアロンMSP-FET JTAGエミュレータでサポートされています。詳細情報については、以下を参照してください。

『拡張エミュレーション・モジュール(EEM)とCode Composer Studioバージョン6による高度なデバッグ』

『MSP430™の高度な電力最適化: ULP Advisor™およびEnergyTrace™テクノロジ』

設計キットと評価モジュール

MSP430FR6989 LaunchPad™ 開発キット MSP-EXP430FR6989 LaunchPad開発キットは、MSP40FR6989マイクロコントローラ(MCU)用の使いやすい評価モジュール(EVM)です。プログラミング、デバッグ、エネルギー測定のためのオンボード・エミュレーションなど、超低消費電力のMSP430FRx FRAMマイクロコントローラ・プラットフォームの開発を始めるために必要な、すべての機能が付属しています。

MSP430FRxx FRAM MCU用のMSP-TS430PZ100D 100ピン・ターゲット開発ボード MSP-TS430PZ100D はスタンドアロンの 100 ピン ZIF ソケット・ターゲット・ボードで、JTAG インターフェイスまたは Spy Bi-Wire (2 線式の JTAG) プロトコルによりシステム内の MSP430 をプログラムおよびデバッグするために使用できます。

MSP430FRxx FRAM MCU用の、100ピンのターゲット開発ボードとMSP-FETプログラマ・バンドル MSP-FET430U100D は、スタンドアロンの 100 ピン ZIF ソケット・ターゲット・ボードである MSP-TS430PZ100D を搭載し、MSP-FET プログラマ/デバッガを実装したバンドルです。このバンドルは、JTAG インターフェイスや Spy-Bi-Wire (2線式 JTAG) プロトコルを使用して、システム内の MSP430 MCU をプログラムおよびデバッグするために使用できます。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存の MSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSP ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430WareソフトウェアはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430FR5x8x、MSP430FR692x、MSP430FR6x7x、MSP430FR6x8xのコード例 すべてのMSPデバイス用に、内蔵の各ペリフェラルをさまざまなアプリケーションの要求に応じて構成するためのCコードの例が用意されています。

MSP超低消費電力マイクロコントローラ用FRAM組み込みソフトウェア・ユーティリティ TI FRAMユーティリティ・ソフトウェアは、組み込みソフトウェア・ユーティリティのコレクションとして成長するように設計されており、超低消費電力と、ほぼ無限のFRAM書き込み耐性を活用できます。このユーティリティは MSP430FRxx FRAMマイクロコントローラで利用でき、アプリケーション開発を始めるために役立つコード例が用意されています。

拡張スキャン・インターフェイス(ESI)を使用する流量計構成用のFlowESI GUI 単純なグラフィカル・インターフェイスの指示に従い、3つまでのLCセンサを拡張スキャン・インターフェイス・モジュールと接続できます。このツールは、完全な機能を持つCCSおよびIARプロジェクト、またはカスタム・プロジェクトに組み込めるソースコードを提供します。

MSP430 Touch Pro GUI MSP430 Touch Pro Tool は、静電容量式タッチ・ボタン、スライダ、およびホイールの設計を検証するために使用できる、PCベースのツールです。このツールでは、CapTouchセンサ・データを受信して視覚化することで、ユーザーはボタン、スライダ、およびホイールの設計を迅速かつ簡単に評価、診断、およびチューニングできるようになります。

MSP430 Touch Power Designer GUI MSP430 Capacitive Touch Power Designerを使用すると、与えられたMSP430容量性タッチ・システムの平均消費電流の推定値を計算できます。動作電圧、周波数、ボタン数、ボタン・ゲート時間といったシステム・パラメータを入力することで、特定のデバイス・ファミリの特定の静電容量式タッチ構成の消費電力を数分で推定できます。

MSPマイクロコントローラ用のデジタル信号処理(DSP)ライブラリ TIのデジタル信号処理ライブラリは、MSP430およびMSP432マイクロコントローラで固定小数点数に対して多くの一般的な信号処理操作を実行するための、高度に最適化された関数のセットです。この関数セットは一般に、高い処理能力を必要とする変換を最小の消費電力、超高精度、リアルタイムで実行するアプリケーション向けに使用されます。このライブラリは、MSP固有のハードウェアを最適に使用して固定小数点演算を行い、大幅な性能向上を実現します。

MSPドライバ・ライブラリ MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTraceテクノロジ MSP430マイクロコントローラ用のEnergyTraceテクノロジは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

IEC60730ソフトウェア・パッケージ IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ 低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

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コマンドライン・プログラマ　MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ　MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

MSP-GANG量産プログラマ　MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8 つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

8.4 ドキュメントのサポート

以下のドキュメントにはMSP430FR697x(1)およびMSP430FR692x(1) MCUについて記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでご利用の製品のフォルダへ移動します(製品フォルダへのリンクについては、8.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR6979正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR69791正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6977正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6928正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6927正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR69271正誤表』 には、機能仕様に対する既知の例外が記載されています。

ユーザー・ガイド

『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL) ユーザー・ガイド』MSP430 MCUに搭載されたブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430 MCUの組み込みメモリと通信できます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』　このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『MSP430 FRAMテクノロジ - ハウツーとベスト・プラクティス』 FRAMは不揮発性メモリ・テクノロジで、SRAMと同様に動作し、多くの新しいアプリケーションを可能にすると同時に、ファームウェアの設計方法に変革をもたらすものです。このアプリケーション・レポートでは、組み込みソフトウェア開発の観点から、MSP430のFRAMテクノロジを使用する方法と、そのベスト・プラクティスについて概説しています。特定用途向けのコード、定数、データ容量の制限、FRAMの使用に従って、アプリケーションのエネルギー消費を最適化するようメモリ・レイアウトを実装する方法について解説します。

『MSP430 32kHz水晶発振器』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430FR6979	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR69791	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6977	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6928	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6927	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR69271	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商標

EnergyTrace++, MSP430, EnergyTrace, LaunchPad, MSP430Ware, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.
Microsoft is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

8.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR69271IPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR69271IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69271
MSP430FR6927IPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6927IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6927
MSP430FR6928IPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6928
MSP430FR6928IPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6928
MSP430FR6928IPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6928
MSP430FR6928IPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6928
MSP430FR6977IPN	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6977
MSP430FR6977IPN.A	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6977

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR6977IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6977
MSP430FR6977IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6977
MSP430FR69791IPN	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPN.A	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPNR	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPNR.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR69791IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR69791
MSP430FR6979IPN	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPN.A	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPNR	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPNR.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979
MSP430FR6979IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6979

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

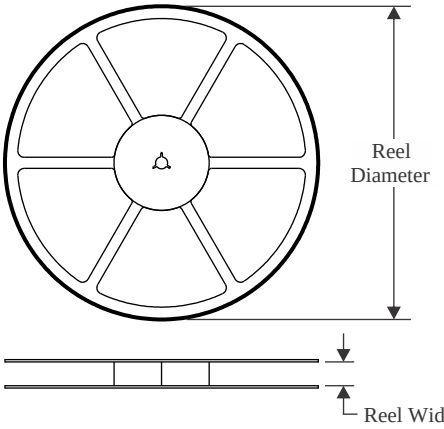
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

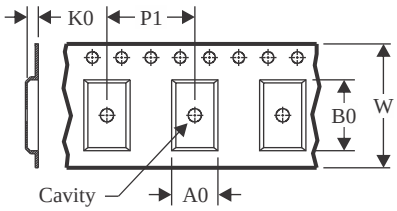
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

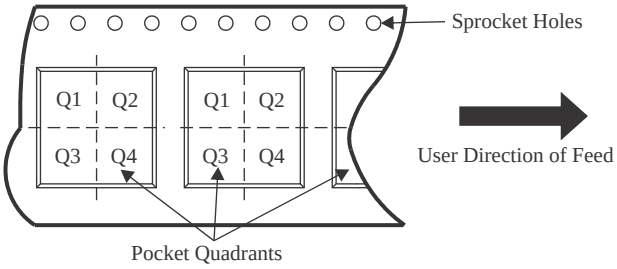


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

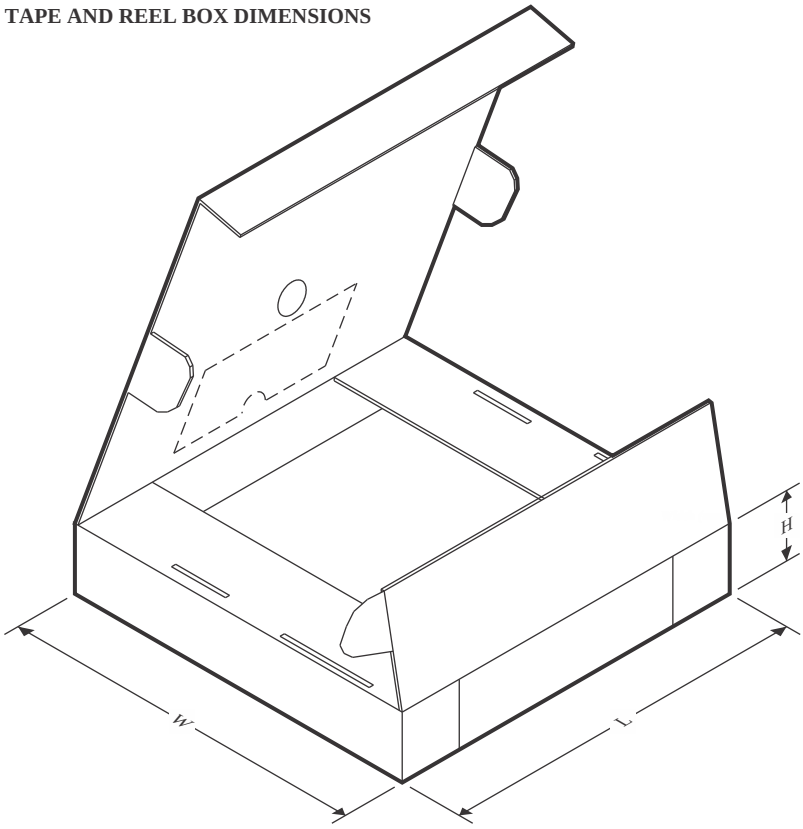
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR69271IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR69271IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR69271IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR6927IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR6927IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR6927IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR6928IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR69791IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430FR69791IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR6979IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430FR6979IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2

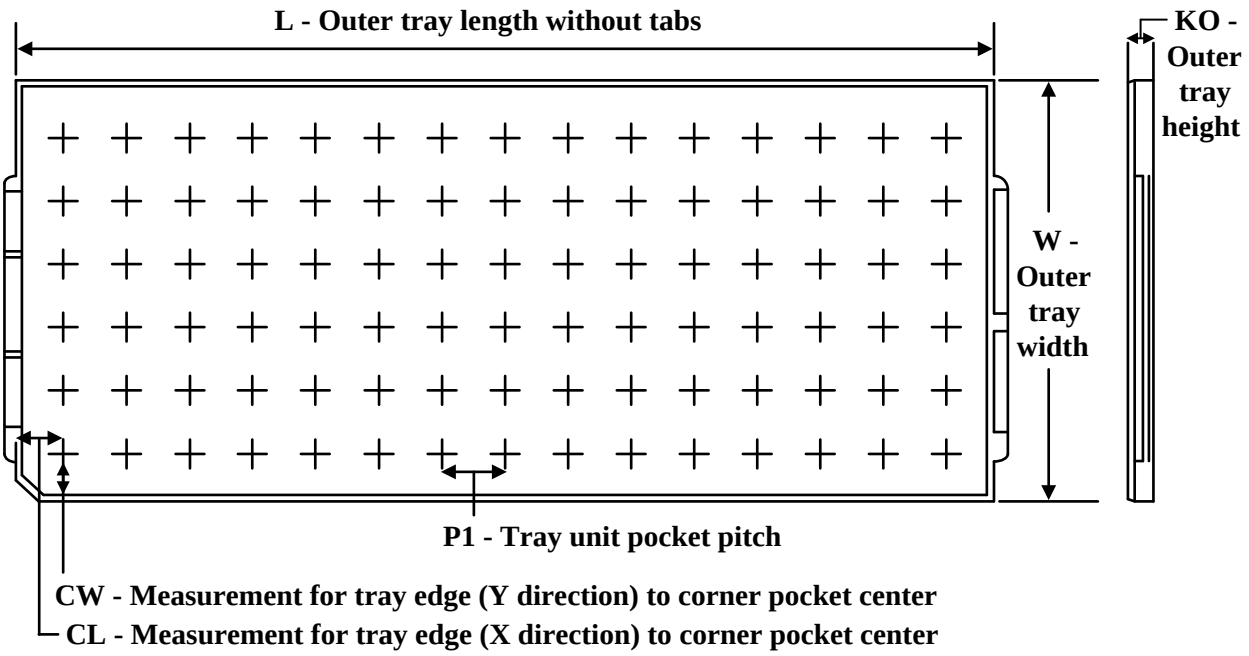
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR69271IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR69271IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR69271IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430FR6927IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR6927IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR6927IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430FR6928IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR69791IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430FR69791IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR6979IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430FR6979IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0

TRAY

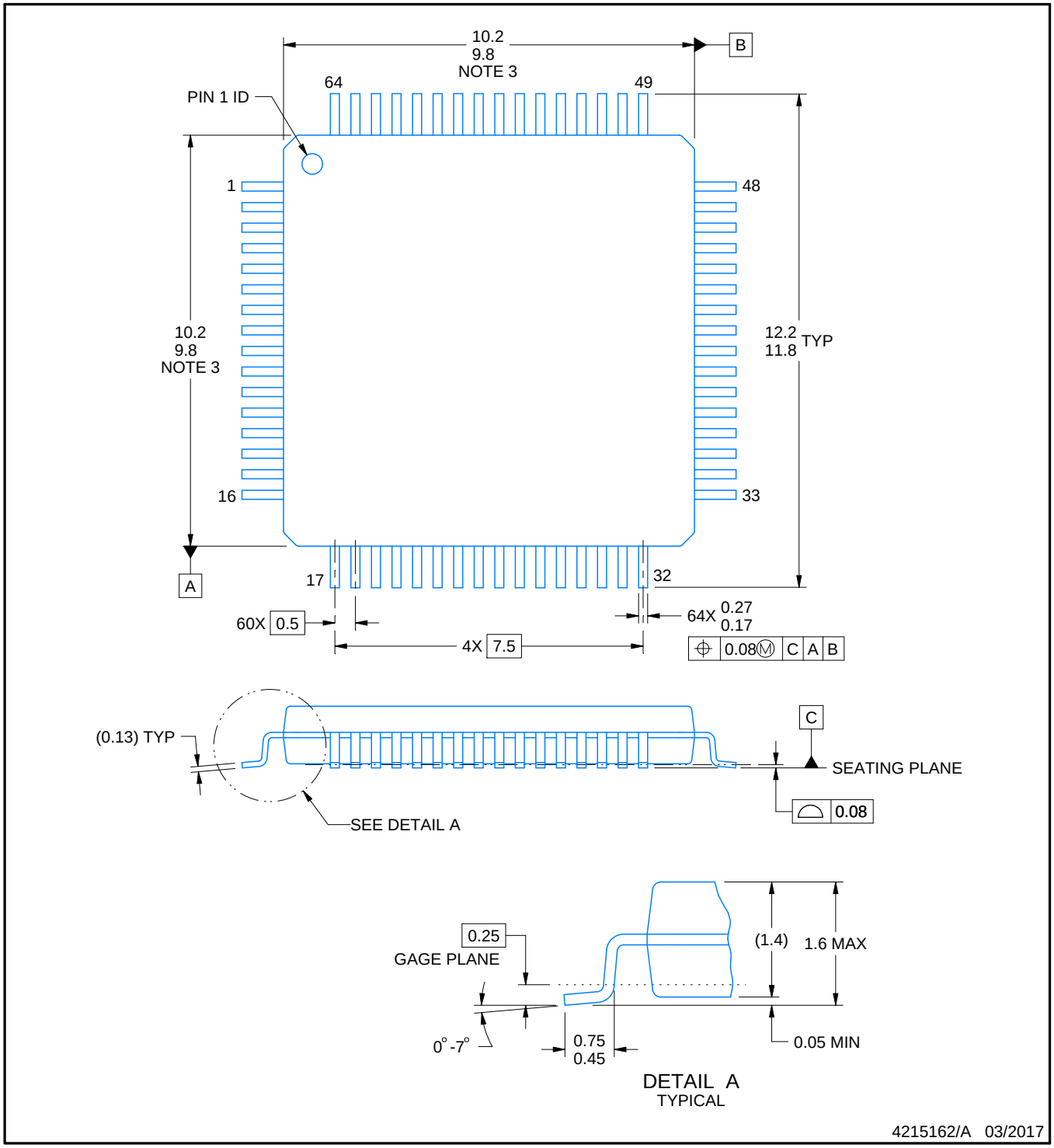


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

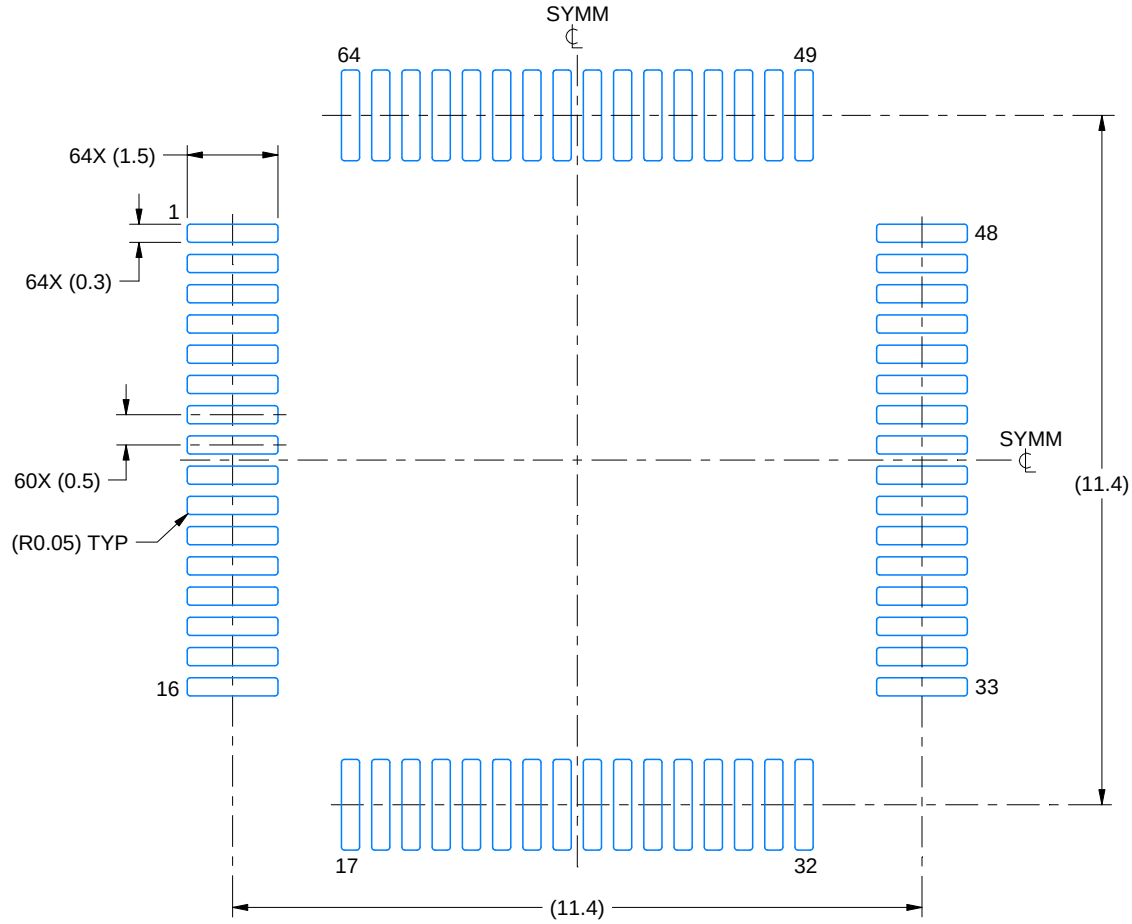
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FR69271IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR69271IPM.A	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR6927IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR6927IPM.A	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR6928IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR6928IPM.A	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430FR6977IPN	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR6977IPN.A	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR6977IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6977IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR69791IPN	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR69791IPN.A	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR69791IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR69791IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6979IPN	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR6979IPN.A	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
MSP430FR6979IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FR6979IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

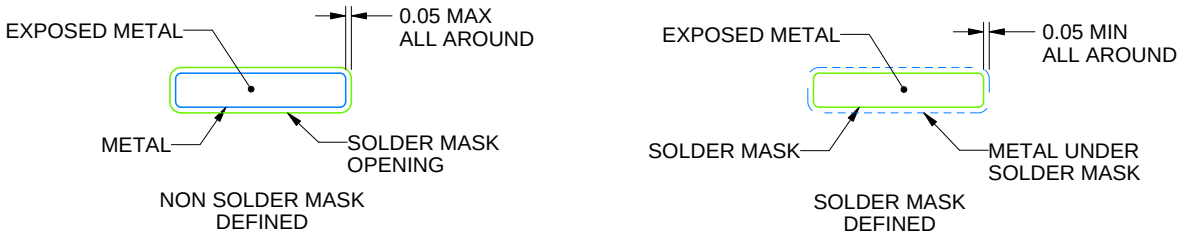


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

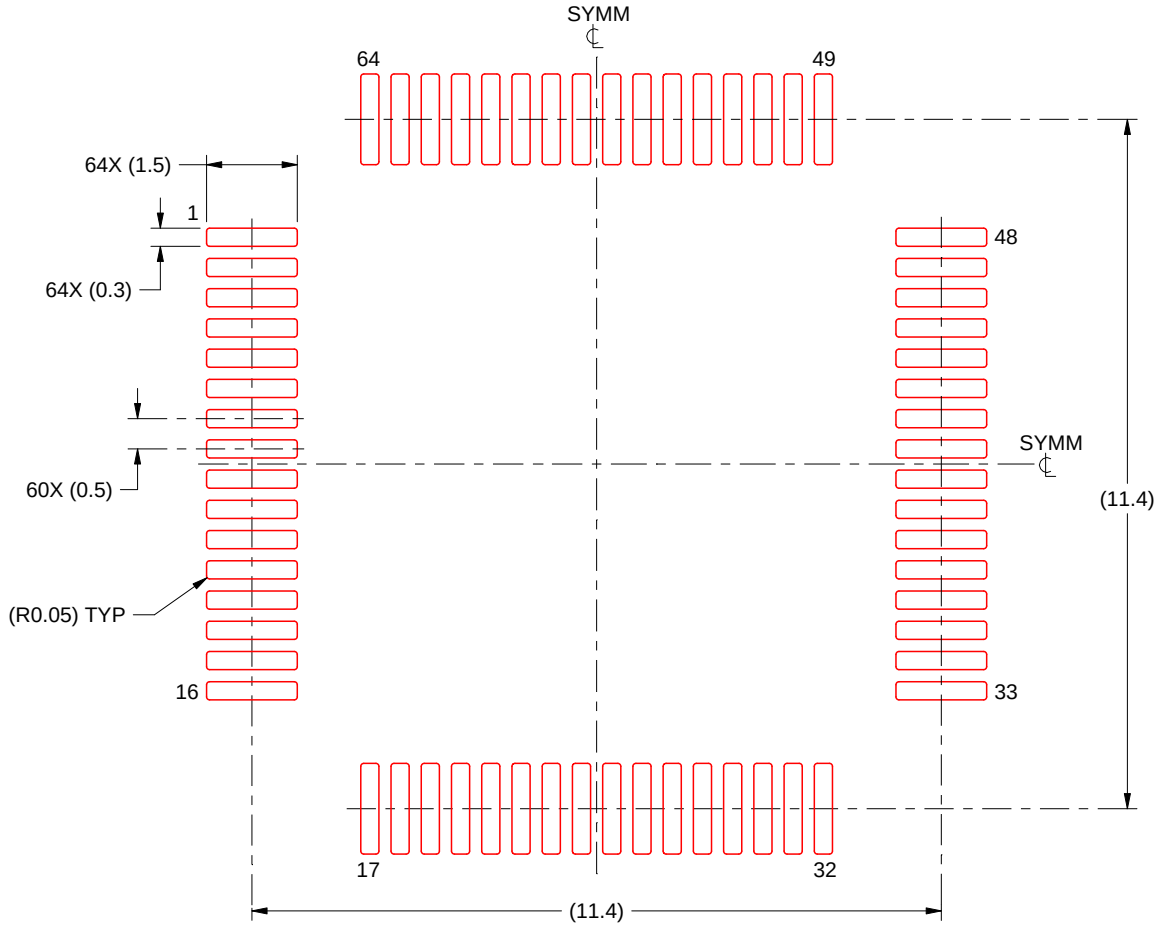


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

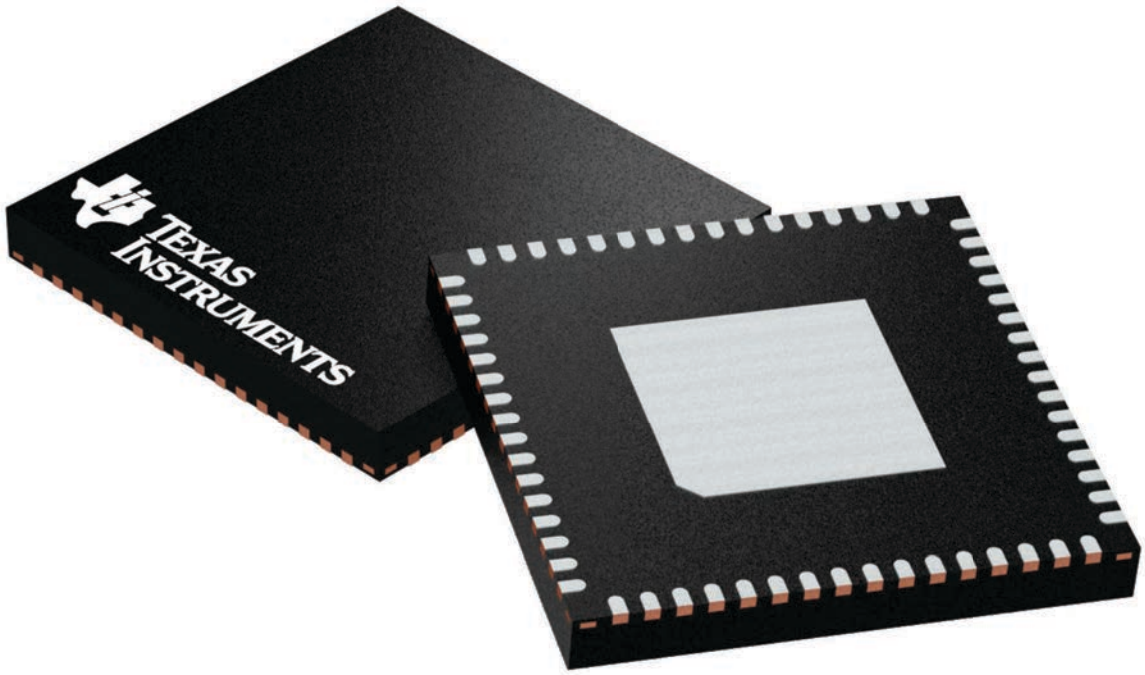
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

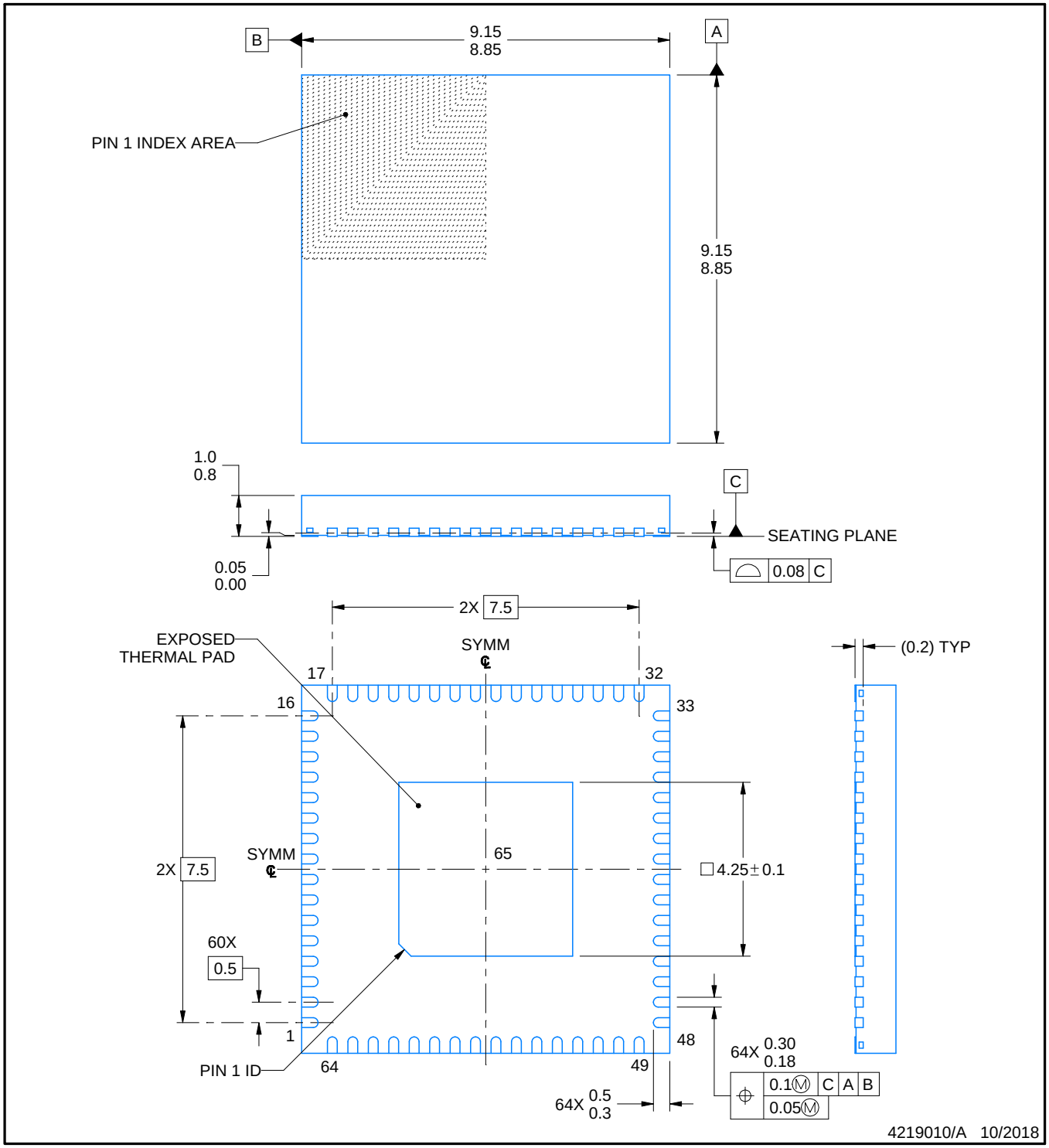
4224597/A

PACKAGE OUTLINE

RGC0064B

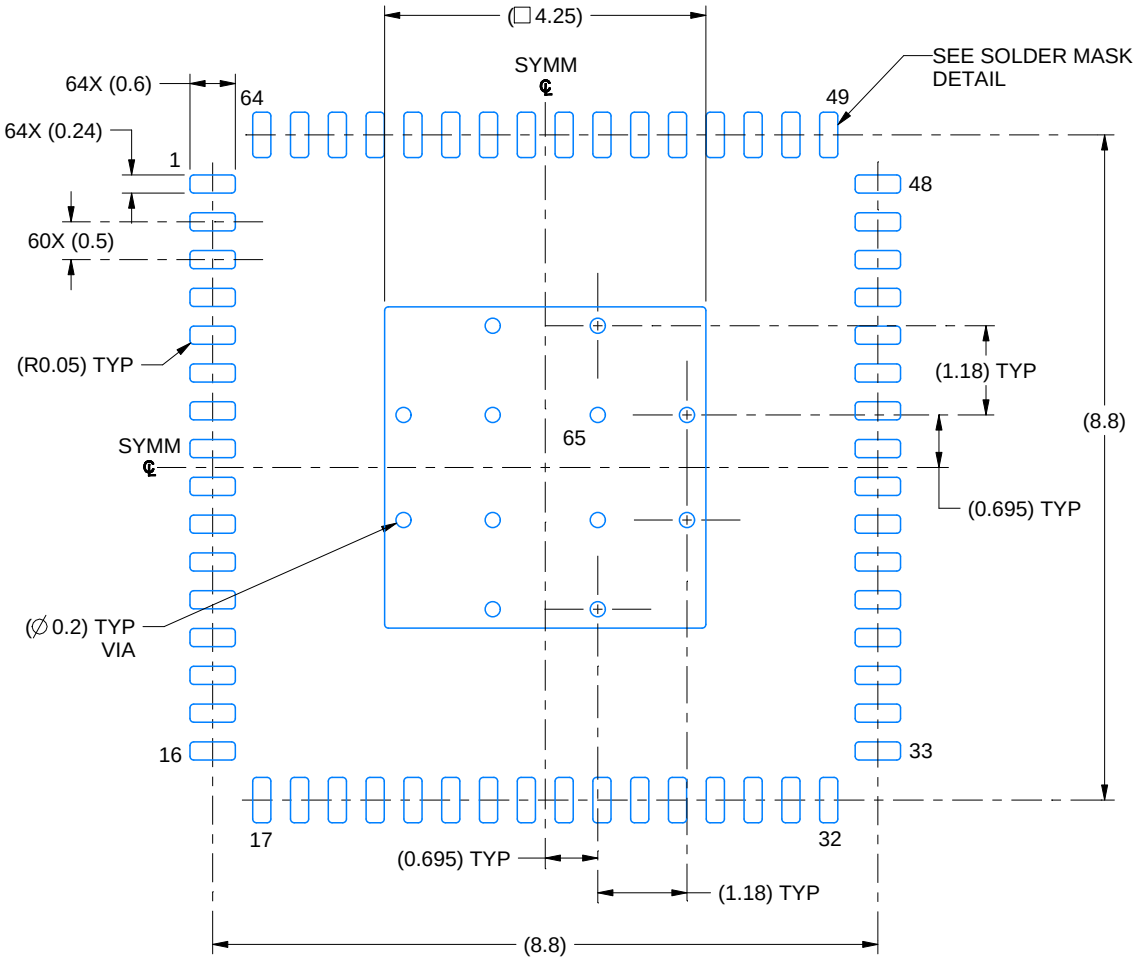
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

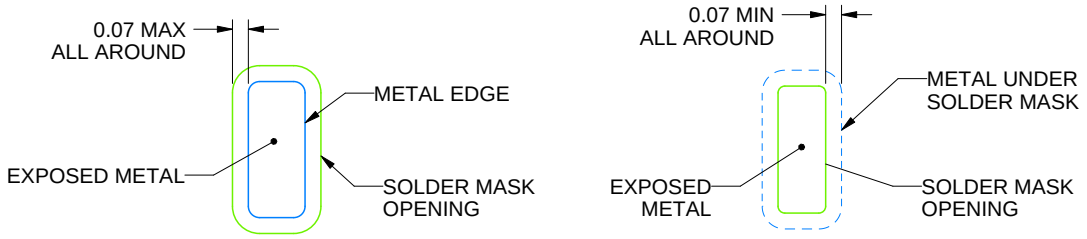


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

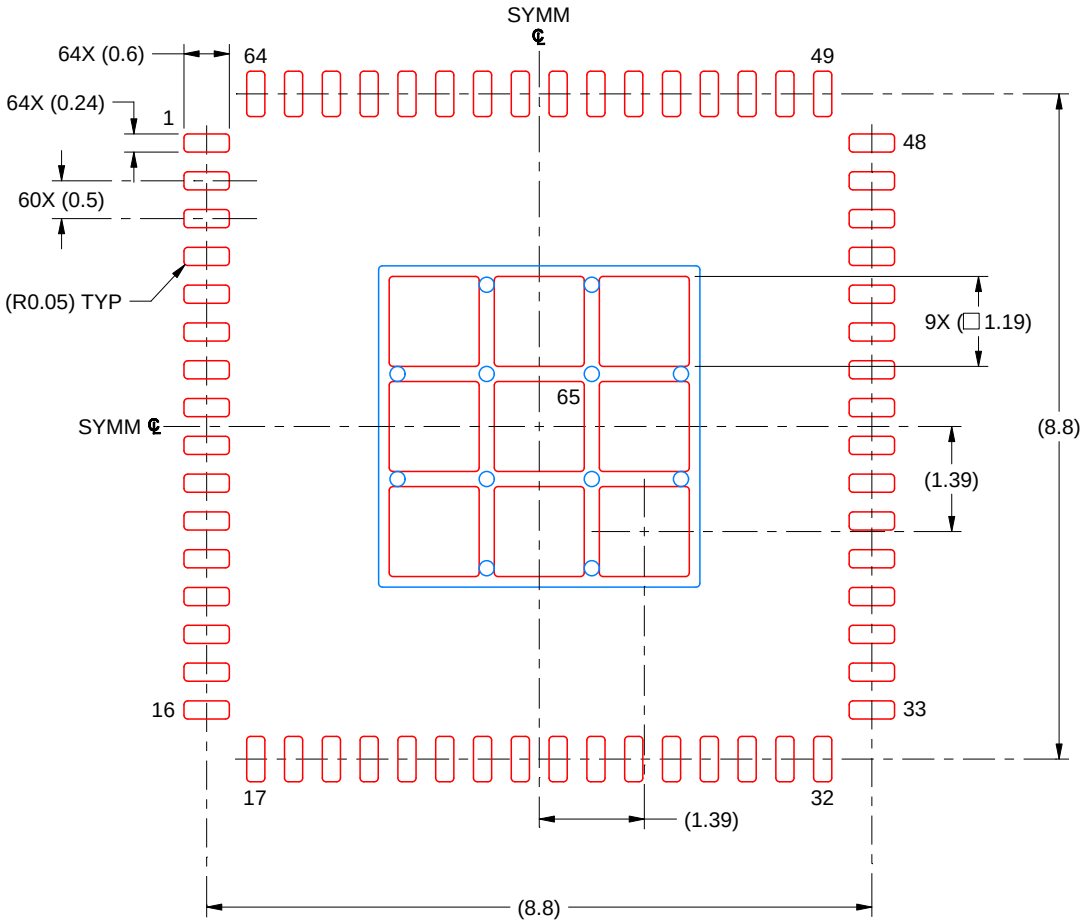
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



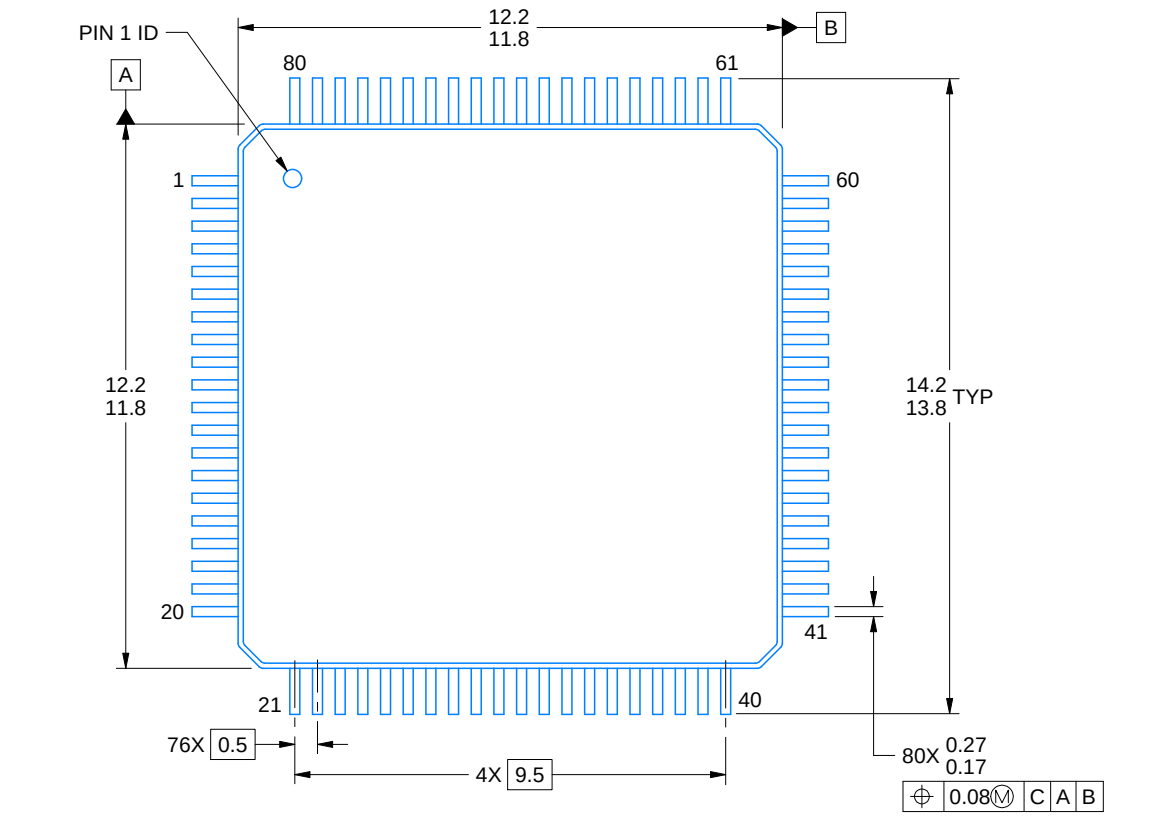
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

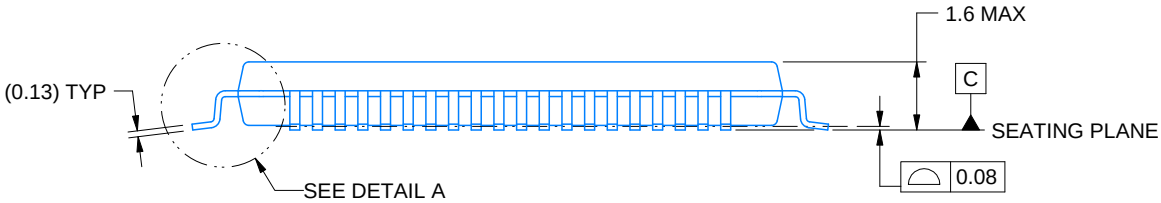
EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

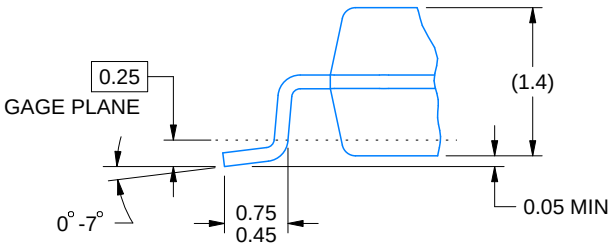
4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





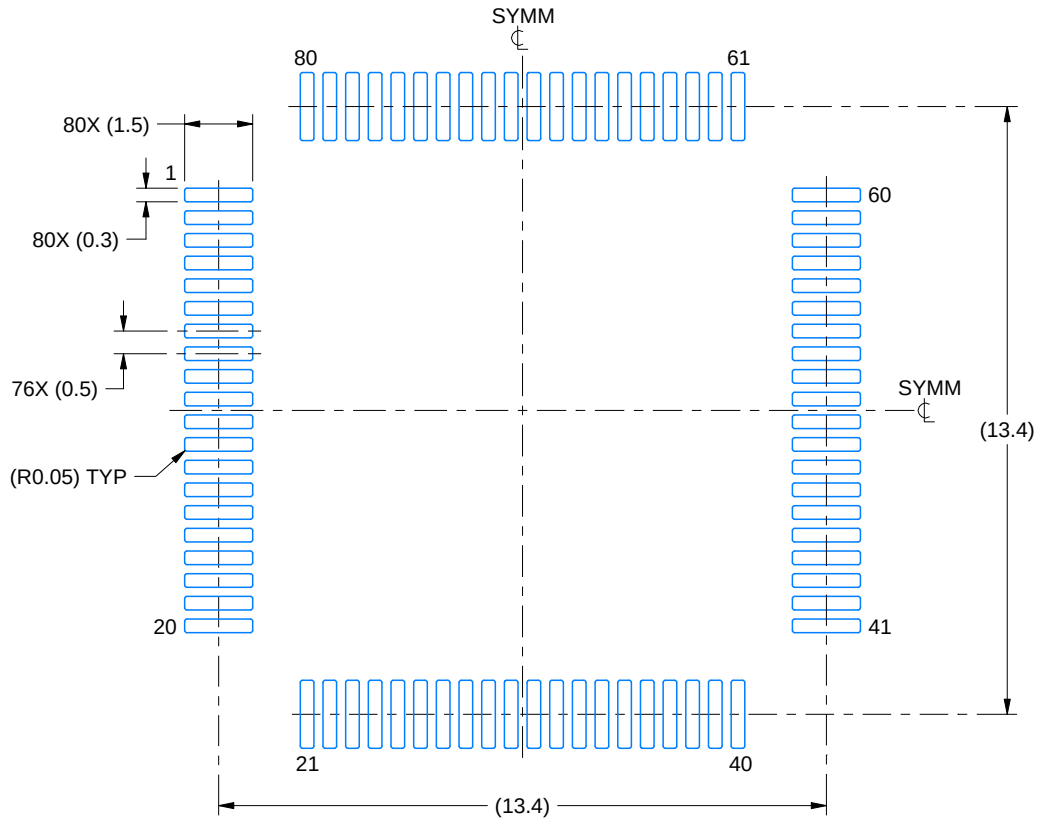


DETAIL A
TYPICAL

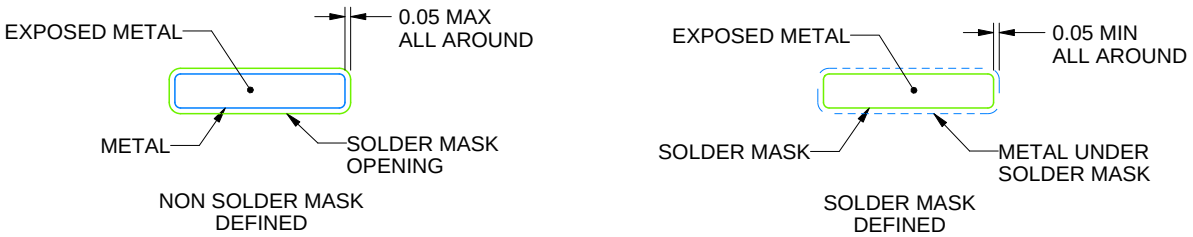
4215166/A 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

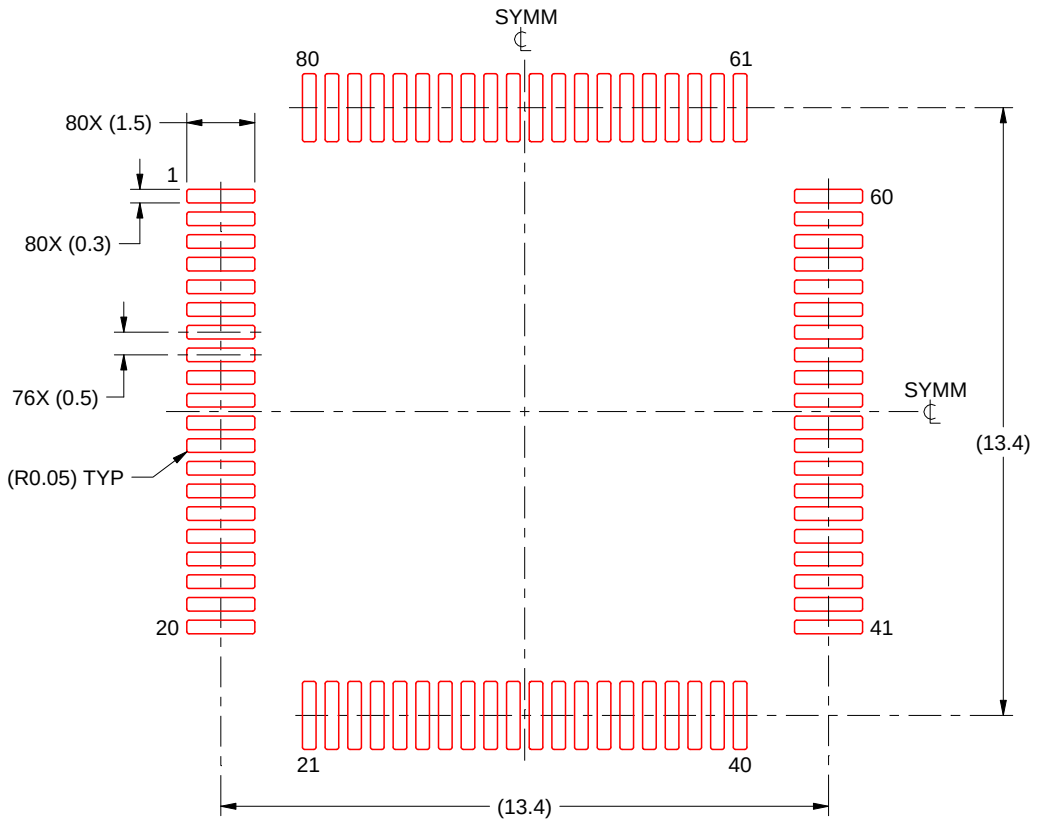


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

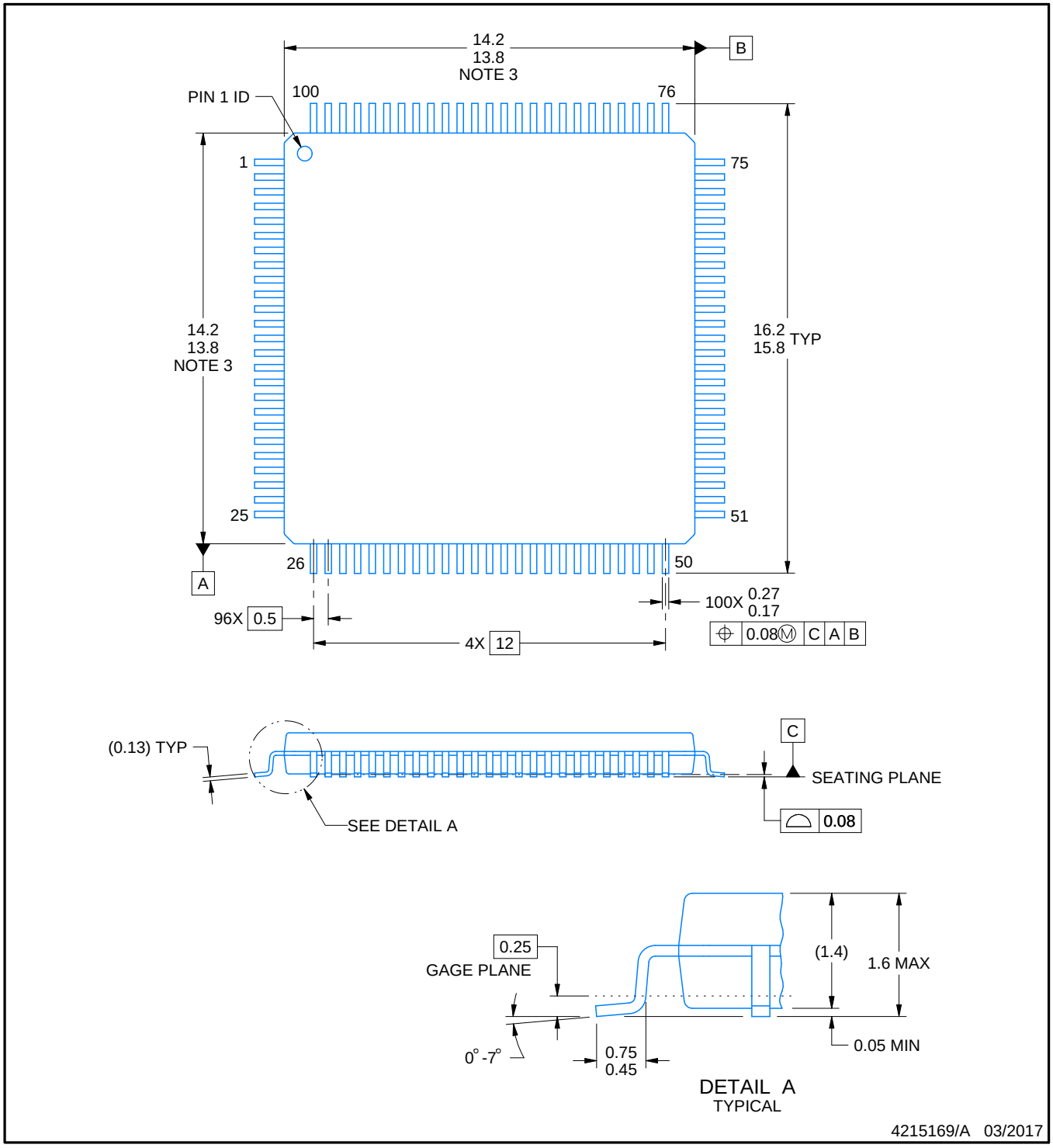


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

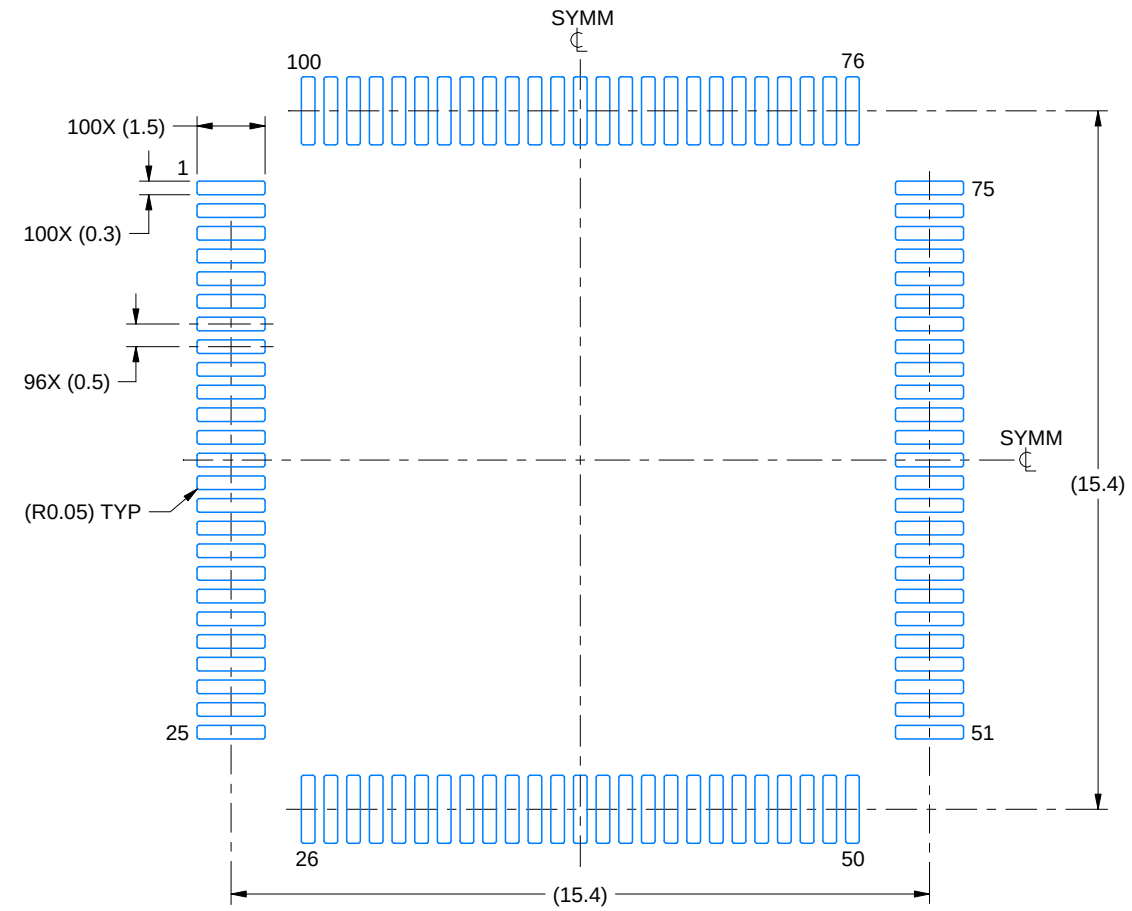
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

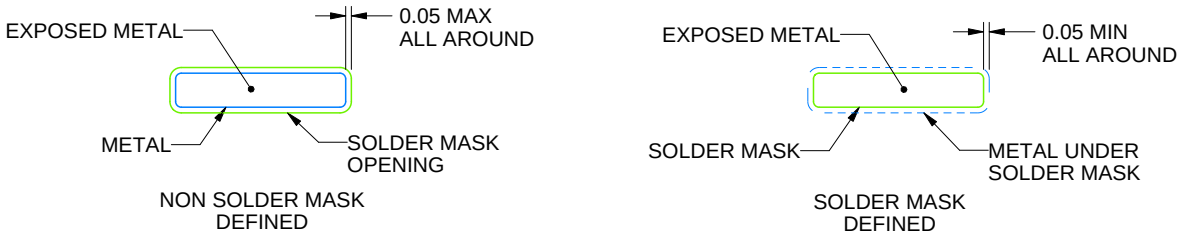


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

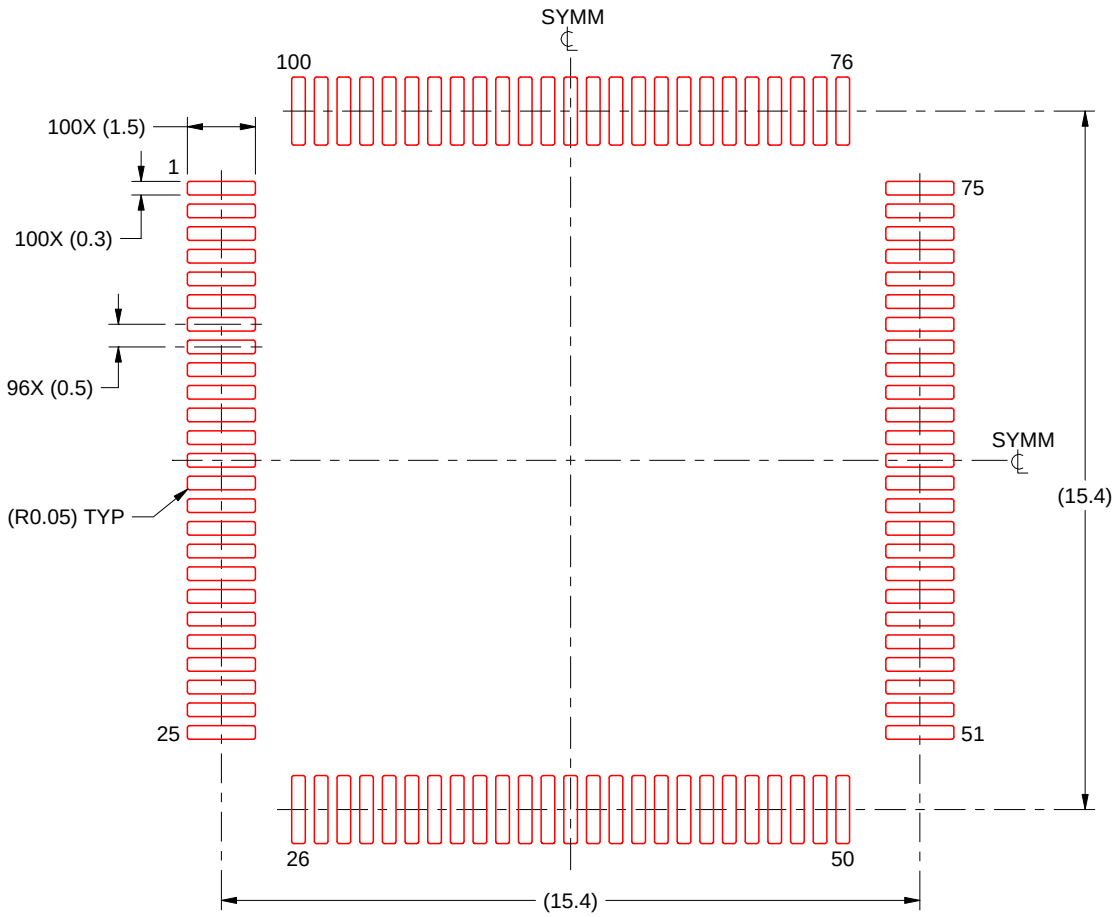


SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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