



# MSP430FR597x(1)、MSP430FR592x(1)、MSP430FR587x(1) ミクスト・シグナル・マイクロコントローラ

## 1 デバイスの概要

### 1.1 特長

- 組み込みマイクロコントローラ
  - 16ビットのRISCアーキテクチャ、最高クロック 16MHz
  - 3.6V~1.8Vの広い電源電圧範囲(最小電源電圧はSVSレベルにより制限されます。「[SVS仕様](#)」を参照)
- 最適化された超低消費電力モード
  - アクティブ・モード: 約100µA/MHz
  - スタンバイ(VLOありのLPM3): 0.4µA (標準値)
  - リアルタイム・クロック(RTC) (LPM3.5): 0.35µA (標準値)<sup>(1)</sup>
  - シャットダウン(LPM4.5): 0.04µA (標準値)
- 超低消費電力の強誘電体RAM (FRAM)
  - 最大64KBの不揮発性メモリ
  - 超低消費電力の書き込み
  - ワードあたり125nsの高速書き込み(4msで64KB)
  - ユニファイド・メモリによりプログラム、データ、ストレージを1か所に保存
  - 10<sup>15</sup>回の書き込み耐久性
  - 放射耐性および非磁性
- インテリジェントなデジタル・ペリフェラル
  - 32ビットのハードウェア・マルチプライヤ(MPY)
  - 3チャンネルの内蔵ダイレクト・メモリ・アクセス(DMA)
  - カレンダーおよびアラーム機能を持つRTC
  - 5つの16ビット・タイマ、それぞれに最大7つのキャプチャ/比較レジスタを搭載
  - 16ビットおよび32ビットの巡回冗長性検査(CRC16、CRC32)
- 高性能アナログ
  - 最大8チャンネルのアナログ・コンパレータ
  - 12ビットのアナログ/デジタル・コンバータ(ADC)、基準電圧とサンプル・アンド・ホールド機能を内蔵し、最大8の外部入力チャンネル
- コードのセキュリティと暗号化
  - 128ビットまたは256ビットのAESセキュリティ暗号化および復号化コプロセッサ(MSP430FR59xx(1)のみ)
- 真の乱数シードによる乱数生成アルゴリズム
- ロック可能なメモリ・セグメントによるIPカプセル化とセキュアなストレージ
- マルチファンクションの入力/出力ポート
  - すべてのピンが外付け部品なしで静電容量式タッチ機能をサポート
  - ビット、バイト、ワード単位でアクセス可能(ペアで)
  - ポートP1~P4上で、LPMからウェイクアップをエッジ選択可能
  - すべてのポートでプルアップおよびプルダウンをプログラム可能
- シリアル通信の拡張機能
  - eUSCI\_A0およびeUSCI\_A1でのサポート
    - 自動ボーレート検出機能付きのUART
    - IrDAのエンコードおよびデコード
    - 最高10Mbpsの速度のSPI
  - eUSCI\_B0およびeUSCI\_B1でのサポート
    - 複数のスレーブ・アドレッシングを持つI<sup>2</sup>C
    - SPI、最高10Mbpsの速度
- 柔軟なクロック・システム
  - 固定周波数DCO、出荷時にトリムされた10の周波数を選択可能
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 32kHzの水晶振動子(LFXT)
  - 高周波数の水晶振動子(HFXT)
- 開発ツールとソフトウェア
  - 無償のプロフェッショナル開発環境、[EnergyTrace++™](#)テクノロジーによる電力プロファイリングとデバッグに対応
  - マイクロコントローラ開発基板を利用可能
- ファミリ製品
  - 利用可能なバリエーションとパッケージについては、「[デバイスの比較](#)」の概要を参照してください。
- モジュールの完全な説明については、[『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』](#)を参照してください。

(1) RTCは3.7pFの水晶振動子によりクロック供給を受けます。



## 1.2 アプリケーション

- 計量
- 環境発電のセンサ・ノード
- ウェアラブル・エレクトロニクス
- センサ管理
- データ・ロギング

## 1.3 概要

MSP430FRxx FRAMマイクロコントローラ・ファミリは、組み込み不揮発性FRAM、16ビットCPU、および各種のペリフェラルのセットを搭載した、いくつかのデバイスで構成され、非常に低消費電力で、さまざまなアプリケーションを対象としています。アーキテクチャ、FRAM、ペリフェラルと7つの低消費電力モードを組み合わせ、携帯型/ワイヤレスのセンシング機器で長いバッテリー駆動時間を実現するように最適化されています。FRAMは新しい不揮発性メモリで、SRAMの速度、柔軟性、耐久性と、フラッシュの安定性および信頼性を両立させ、しかも総合的な消費電力が低い製品です。

製品情報<sup>(1)</sup>

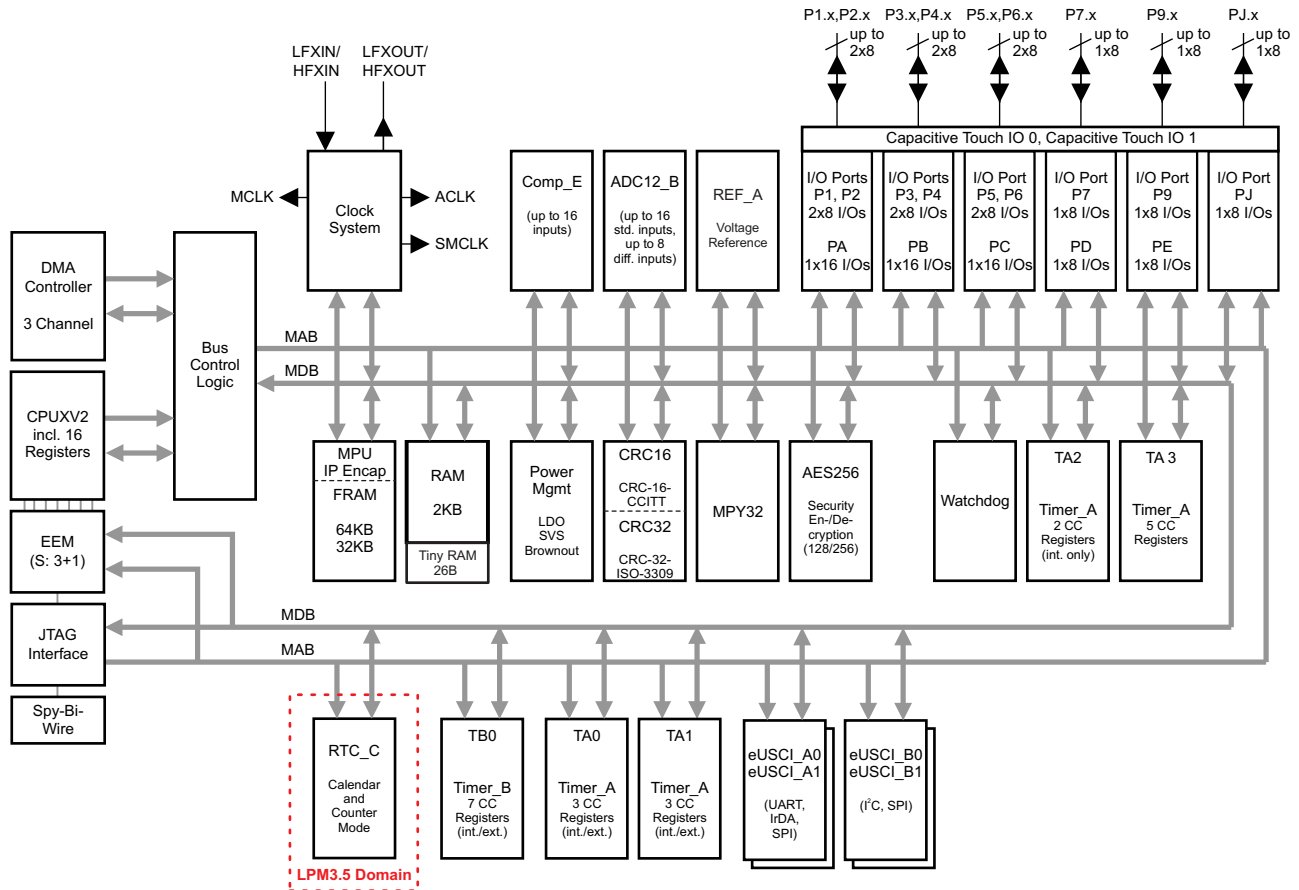
| 型番               | パッケージ      | 本体サイズ <sup>(2)</sup> |
|------------------|------------|----------------------|
| MSP430FR5972IPMR | LQFP (64)  | 10mm×10mm            |
| MSP430FR5972IRGC | VQFN (64)  | 9mm×9mm              |
| MSP430FR5922IG56 | TSSOP (56) | 6.1mm×14mm           |

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については 9 の「付録: パッケージ・オプション」または [www.ti.com](http://www.ti.com) の TI Web サイトを参照してください。

(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9 の「メカニカル・データ」を参照してください。

## 1.4 機能ブロック図

機能ブロック図を、図 1-1 に示します。



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NOTE: MSP430FR587xおよびMSP430FR587x1デバイスにはAES256が実装されていません。

NOTE: MSP430FR592xおよびMSP430FR592x1デバイスにはHFXINとHFXOUTが実装されていません。

図 1-1. 機能ブロック図

## Table of Contents

|          |                                                                                             |                            |      |                                                         |                     |
|----------|---------------------------------------------------------------------------------------------|----------------------------|------|---------------------------------------------------------|---------------------|
| <b>1</b> | <b>デバイスの概要</b>                                                                              | <b><a href="#">1</a></b>   |      |                                                         |                     |
| 1.1      | 特長                                                                                          | <a href="#">1</a>          |      |                                                         |                     |
| 1.2      | アプリケーション                                                                                    | <a href="#">2</a>          |      |                                                         |                     |
| 1.3      | 概要                                                                                          | <a href="#">2</a>          |      |                                                         |                     |
| 1.4      | 機能ブロック図                                                                                     | <a href="#">3</a>          |      |                                                         |                     |
| <b>2</b> | <b>改訂履歴</b>                                                                                 | <b><a href="#">5</a></b>   |      |                                                         |                     |
| <b>3</b> | <b>Device Comparison</b>                                                                    | <b><a href="#">6</a></b>   |      |                                                         |                     |
| 3.1      | Related Products                                                                            | <a href="#">8</a>          |      |                                                         |                     |
| <b>4</b> | <b>Terminal Configuration and Functions</b>                                                 | <b><a href="#">9</a></b>   |      |                                                         |                     |
| 4.1      | Pin Diagrams                                                                                | <a href="#">9</a>          |      |                                                         |                     |
| 4.2      | Pin Attributes                                                                              | <a href="#">12</a>         |      |                                                         |                     |
| 4.3      | Signal Descriptions                                                                         | <a href="#">17</a>         |      |                                                         |                     |
| 4.4      | Pin Multiplexing                                                                            | <a href="#">23</a>         |      |                                                         |                     |
| 4.5      | Buffer Type                                                                                 | <a href="#">23</a>         |      |                                                         |                     |
| 4.6      | Connection of Unused Pins                                                                   | <a href="#">23</a>         |      |                                                         |                     |
| <b>5</b> | <b>Specifications</b>                                                                       | <b><a href="#">24</a></b>  |      |                                                         |                     |
| 5.1      | Absolute Maximum Ratings                                                                    | <a href="#">24</a>         |      |                                                         |                     |
| 5.2      | ESD Ratings                                                                                 | <a href="#">24</a>         |      |                                                         |                     |
| 5.3      | Recommended Operating Conditions                                                            | <a href="#">24</a>         |      |                                                         |                     |
| 5.4      | Active Mode Supply Current Into $V_{CC}$ Excluding External Current                         | <a href="#">25</a>         |      |                                                         |                     |
| 5.5      | Typical Characteristics - Active Mode Supply Currents                                       | <a href="#">26</a>         |      |                                                         |                     |
| 5.6      | Low-Power Mode (LPM0, LPM1) Supply Currents Into $V_{CC}$ Excluding External Current        | <a href="#">26</a>         |      |                                                         |                     |
| 5.7      | Low-Power Mode LPM2, LPM3, LPM4 Supply Currents (Into $V_{CC}$ ) Excluding External Current | <a href="#">27</a>         |      |                                                         |                     |
| 5.8      | Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$ ) Excluding External Current           | <a href="#">29</a>         |      |                                                         |                     |
| 5.9      | Typical Characteristics, Low-Power Mode Supply Currents                                     | <a href="#">30</a>         |      |                                                         |                     |
| 5.10     | Typical Characteristics, Current Consumption per Module                                     | <a href="#">31</a>         |      |                                                         |                     |
| 5.11     | Thermal Resistance Characteristics                                                          | <a href="#">31</a>         |      |                                                         |                     |
|          |                                                                                             |                            | 5.12 | Timing and Switching Characteristics                    | <a href="#">32</a>  |
| <b>6</b> | <b>Detailed Description</b>                                                                 | <b><a href="#">58</a></b>  |      |                                                         |                     |
|          |                                                                                             |                            | 6.1  | Overview                                                | <a href="#">58</a>  |
|          |                                                                                             |                            | 6.2  | CPU                                                     | <a href="#">58</a>  |
|          |                                                                                             |                            | 6.3  | Operating Modes                                         | <a href="#">59</a>  |
|          |                                                                                             |                            | 6.4  | Interrupt Vector Table and Signatures                   | <a href="#">61</a>  |
|          |                                                                                             |                            | 6.5  | Bootloader (BSL)                                        | <a href="#">64</a>  |
|          |                                                                                             |                            | 6.6  | JTAG Operation                                          | <a href="#">64</a>  |
|          |                                                                                             |                            | 6.7  | FRAM                                                    | <a href="#">65</a>  |
|          |                                                                                             |                            | 6.8  | RAM                                                     | <a href="#">65</a>  |
|          |                                                                                             |                            | 6.9  | Tiny RAM                                                | <a href="#">65</a>  |
|          |                                                                                             |                            | 6.10 | Memory Protection Unit (MPU) Including IP Encapsulation | <a href="#">65</a>  |
|          |                                                                                             |                            | 6.11 | Peripherals                                             | <a href="#">66</a>  |
|          |                                                                                             |                            | 6.12 | Device Descriptors (TLV)                                | <a href="#">101</a> |
|          |                                                                                             |                            | 6.13 | Memory                                                  | <a href="#">104</a> |
|          |                                                                                             |                            | 6.14 | Identification                                          | <a href="#">118</a> |
| <b>7</b> | <b>Applications, Implementation, and Layout</b>                                             | <b><a href="#">119</a></b> |      |                                                         |                     |
|          |                                                                                             |                            | 7.1  | Device Connection and Layout Fundamentals               | <a href="#">119</a> |
|          |                                                                                             |                            | 7.2  | Peripheral- and Interface-Specific Design Information   | <a href="#">123</a> |
| <b>8</b> | <b>デバイスおよびドキュメントのサポート</b>                                                                   | <b><a href="#">125</a></b> |      |                                                         |                     |
|          |                                                                                             |                            | 8.1  | 使い始めと次の手順                                               | <a href="#">125</a> |
|          |                                                                                             |                            | 8.2  | デバイスの項目表記                                               | <a href="#">125</a> |
|          |                                                                                             |                            | 8.3  | ツールとソフトウェア                                              | <a href="#">126</a> |
|          |                                                                                             |                            | 8.4  | ドキュメントのサポート                                             | <a href="#">128</a> |
|          |                                                                                             |                            | 8.5  | 関連リンク                                                   | <a href="#">129</a> |
|          |                                                                                             |                            | 8.6  | Community Resources                                     | <a href="#">129</a> |
|          |                                                                                             |                            | 8.7  | 商標                                                      | <a href="#">130</a> |
|          |                                                                                             |                            | 8.8  | 静電気放電に関する注意事項                                           | <a href="#">130</a> |
|          |                                                                                             |                            | 8.9  | Export Control Notice                                   | <a href="#">130</a> |
|          |                                                                                             |                            | 8.10 | Glossary                                                | <a href="#">130</a> |
| <b>9</b> | <b>メカニカル、パッケージ、および注文情報</b>                                                                  | <b><a href="#">131</a></b> |      |                                                         |                     |

## 2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 2017年1月25日発行分から2018年08月30日発行分への変更                                                                                                | Page                |
|----------------------------------------------------------------------------------------------------------------------------------|---------------------|
| • Updated <a href="#">Section 3.1, Related Products</a> .....                                                                    | <a href="#">8</a>   |
| • Added note (1) to <a href="#">表 5-2, SVS</a> .....                                                                             | <a href="#">32</a>  |
| • Changed capacitor value from 4.7 $\mu$ F to 470 nF in <a href="#">図 7-5, ADC12_B Grounding and Noise Considerations</a> .....  | <a href="#">123</a> |
| • Changed capacitor value from 4.7 $\mu$ F to 470 nF in the last paragraph of <a href="#">7.2.1.2, Design Requirements</a> ..... | <a href="#">124</a> |
| • <a href="#">8.2, 「デバイスの項目表記」</a> のテキストと図を更新 .....                                                                              | <a href="#">125</a> |

### 3 Device Comparison

Table 3-1 and Table 3-2 summarize the available family members.

**Table 3-1. Device Comparison – Family Members With UART BSL**

| DEVICE       | FRAM<br>(KB) | SRAM<br>(KB) | CLOCK<br>SYSTEM     | Timer_A <sup>(1)</sup>                        | Timer_B <sup>(2)</sup> | eUSCI            |                  | AES | ADC12_B | I/O            | PACKAGE                   |
|--------------|--------------|--------------|---------------------|-----------------------------------------------|------------------------|------------------|------------------|-----|---------|----------------|---------------------------|
|              |              |              |                     |                                               |                        | A <sup>(3)</sup> | B <sup>(4)</sup> |     |         |                |                           |
| MSP430FR5972 | 64           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | yes | 8 ext   | 51             | 64 PM<br>64 RGC           |
| MSP430FR5872 | 64           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | no  | 8 ext   | 51             | 64 PM<br>64 RGC           |
| MSP430FR5970 | 32           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | yes | 8 ext   | 51             | 64 PM<br>64 RGC           |
| MSP430FR5922 | 64           | 2            | DCO<br>LFXT         | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | yes | 8 ext   | 51<br>46 (DGG) | 64 PM<br>64 RGC<br>56 DGG |
| MSP430FR5870 | 32           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | no  | 8 ext   | 51             | 64 PM<br>64 RGC           |

- (1) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) eUSCI\_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (4) eUSCI\_B supports I<sup>2</sup>C with multiple slave addresses and SPI.
- (5) Timer\_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (6) Timer\_A TA2 provides only internal capture/compare inputs and only internal PWM outputs (if any).
- (7) Timer\_A TA3 provides only internal capture/compare inputs and only internal PWM outputs (if any) for FR592x(1) with RGC and PM packages. For FR592x(1) with DGG package and all other devices, Timer\_A TA3 provides internal, external capture/compare inputs and internal, external PWM outputs (if any).

Table 3-2. Device Comparison – Family Members With I<sup>2</sup>C BSL

| DEVICE        | FRAM<br>(KB) | SRAM<br>(KB) | CLOCK<br>SYSTEM     | Timer_A <sup>(1)</sup>                        | Timer_B <sup>(2)</sup> | eUSCI            |                  | AES | ADC12_B | I/O            | PACKAGE                   |
|---------------|--------------|--------------|---------------------|-----------------------------------------------|------------------------|------------------|------------------|-----|---------|----------------|---------------------------|
|               |              |              |                     |                                               |                        | A <sup>(3)</sup> | B <sup>(4)</sup> |     |         |                |                           |
| MSP430FR59721 | 64           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | yes | 8 ext   | 51             | 64 PM<br>64 RGC           |
| MSP430FR59221 | 64           | 2            | DCO<br>LFXT         | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | yes | 8 ext   | 51<br>46 (DGG) | 64 PM<br>64 RGC<br>56 DGG |
| MSP430FR58721 | 64           | 2            | DCO<br>HFXT<br>LFXT | 3, 3 <sup>(5)</sup><br>2, 5 <sup>(6)(7)</sup> | 7                      | 2                | 2                | no  | 8 ext   | 51             | 64 PM<br>64 RGC           |

- (1) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) eUSCI\_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (4) eUSCI\_B supports I<sup>2</sup>C with multiple slave addresses and SPI.
- (5) Timer\_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (6) Timer\_A TA2 provides only internal capture/compare inputs and only internal PWM outputs (if any).
- (7) Timer\_A TA3 provides only internal capture/compare inputs and only internal PWM outputs (if any) for FR592x(1) with RGC and PM packages. For FR592x(1) with DGG package and all other devices, Timer\_A TA3 provides internal, external capture/compare inputs and internal, external PWM outputs (if any).

### 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**TI 16-bit and 32-bit microcontrollers** High-performance, low-power solutions to enable the autonomous future

**Products for MSP430 ultra-low-power sensing and measurement microcontrollers** One platform. One ecosystem. Endless possibilities.

**Products for MSP430 ultrasonic and performance sensing microcontrollers** Ultra-low-power single-chip MCUs with integrated sensing peripherals

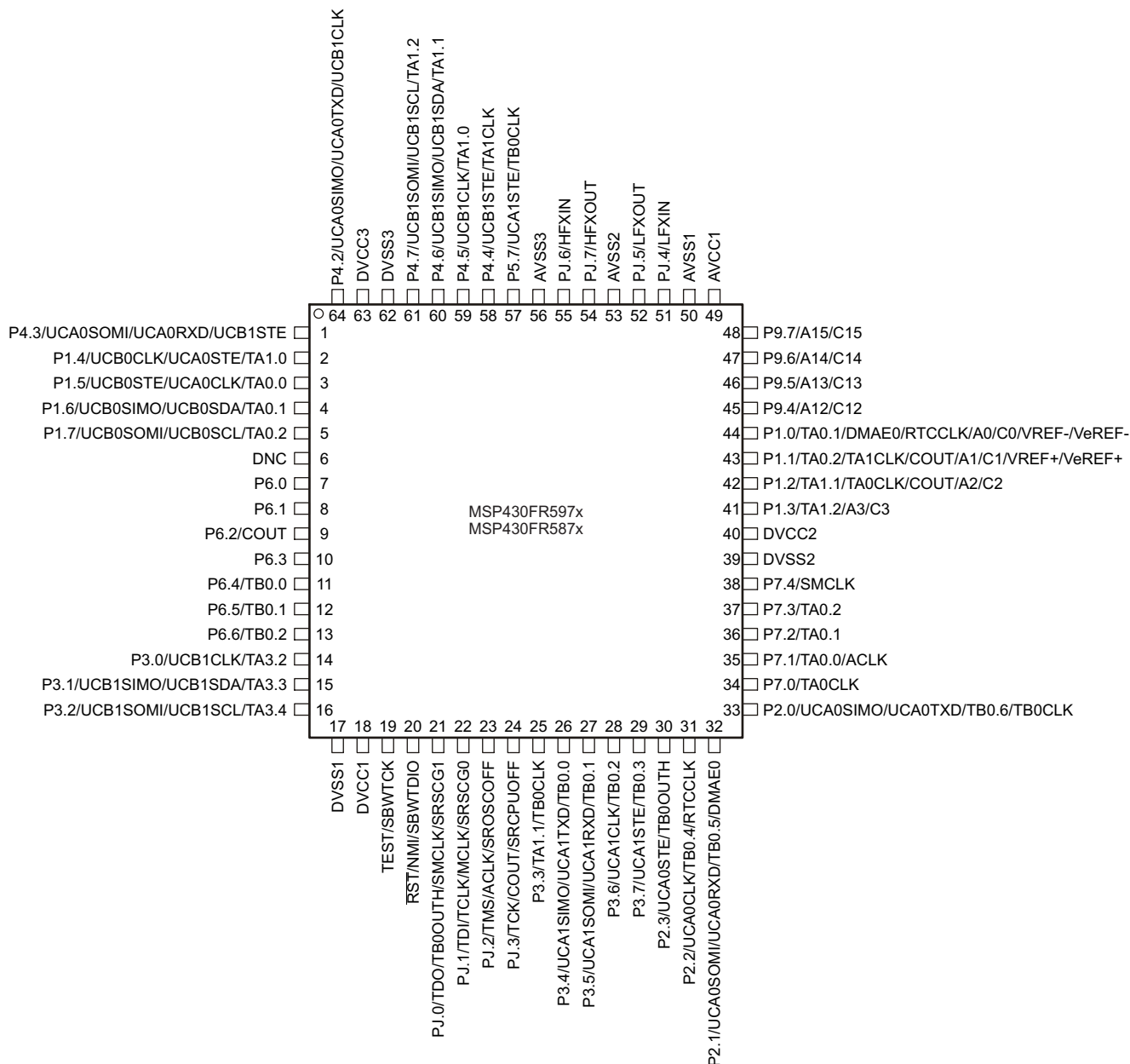
**Companion Products for MSP430FR5972** Review products that are frequently purchased or used with this product.

**Reference Designs for MSP430FR5972** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at [ti.com/tidesigns](http://ti.com/tidesigns).

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 64-pin PM and RGC packages of the MSP430FR597x(1) and MSP430FR587x(1) MCUs.



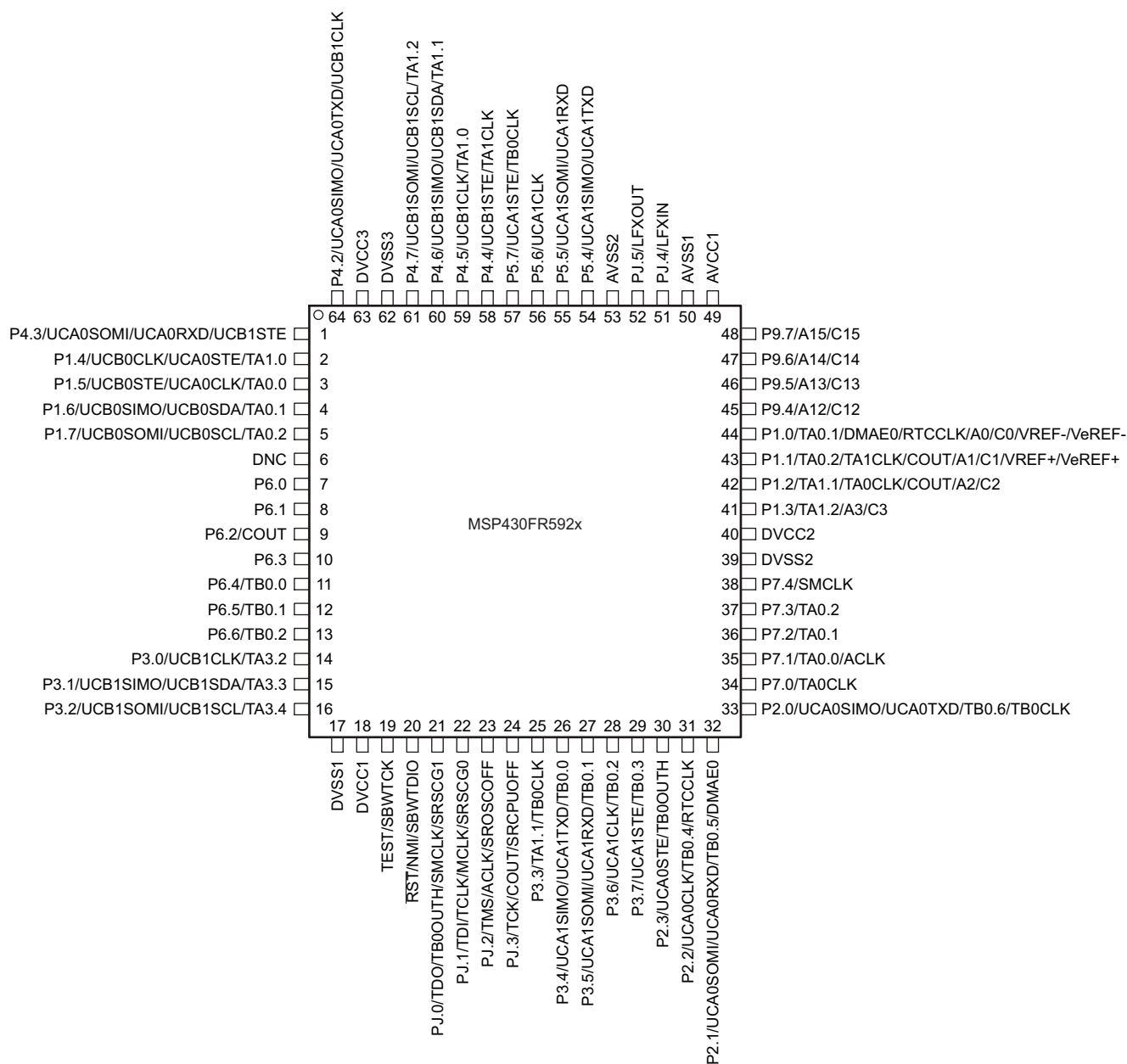
On devices with UART BSL: P2.0: BSL\_TX; P2.1: BSL\_RX

On devices with I<sup>2</sup>C BSL: P1.6: BSL\_DAT; P1.7: BSL\_CLK

NOTE: TI recommends connecting the RGC package thermal pad to VSS.

**Figure 4-1. 64-Pin PM and RGC Packages (Top View) – MSP430FR597x(1), MSP430FR587x(1)**

Figure 4-2 shows the pinout for the 64-pin PM and RGC packages of the MSP430FR592x(1) MCUs.

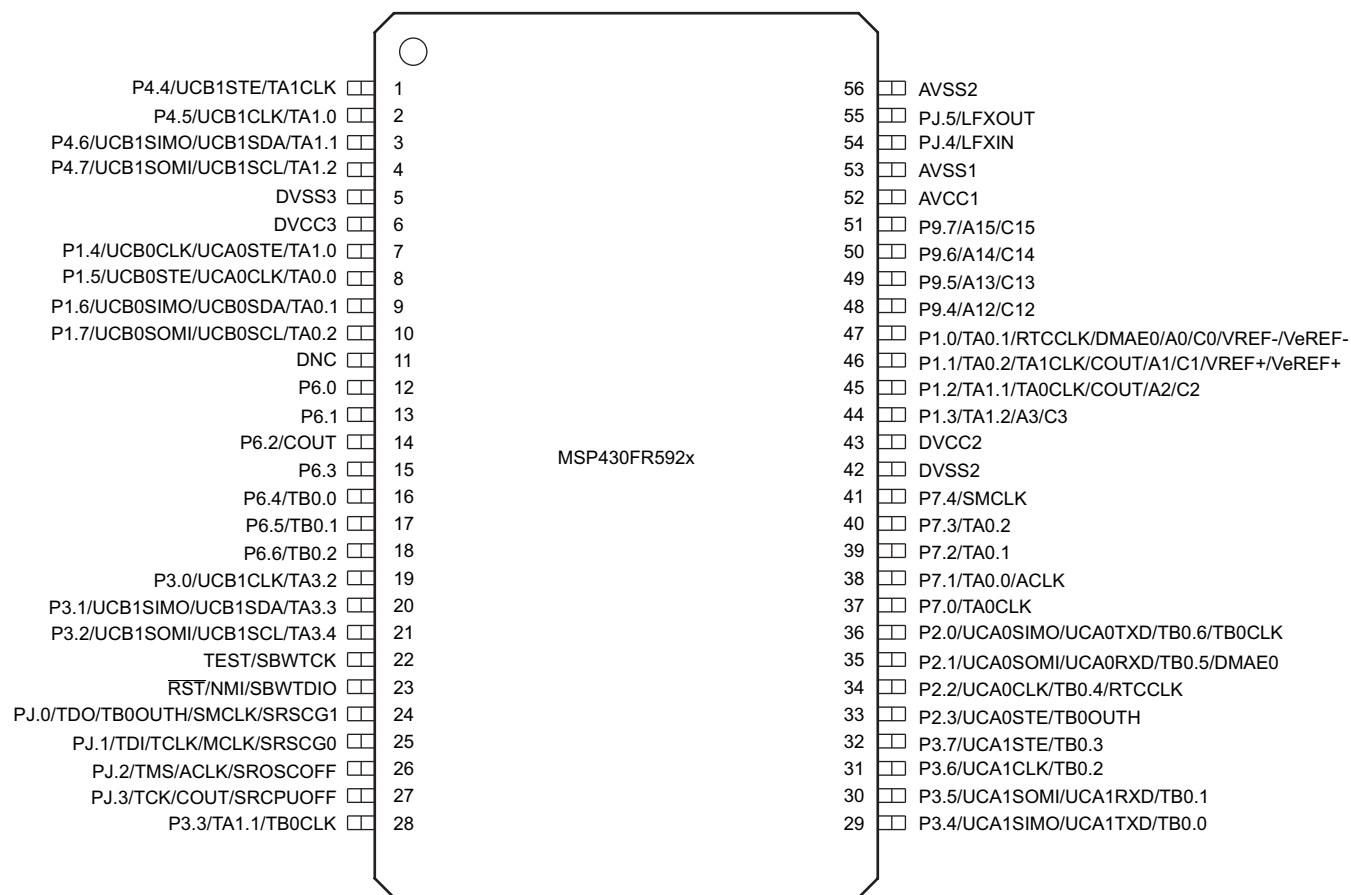


- A. On devices with UART BSL: P2.0: BSL\_TX; P2.1: BSL\_RX  
On devices with I<sup>2</sup>C BSL: P1.6: BSL\_DAT; P1.7: BSL\_CLK

NOTE: TI recommends connecting the RGC package thermal pad to VSS.

**Figure 4-2. 64-Pin PM and RGC Packages (Top View) – MSP430FR592x(1)**

Figure 4-3 shows the pinout for the 56-pin DGG package of the MSP430FR592x(1) MCUs.



- A. On devices with UART BSL: P2.0: BSL\_TX; P2.1: BSL\_RX  
On devices with I<sup>2</sup>C BSL: P1.6: BSL\_DAT; P1.7: BSL\_CLK

**Figure 4-3. 56-Pin DGG Package (Top View) – MSP430FR592x(1)**

## 4.2 Pin Attributes

Table 4-1 lists the attributes of each pin.

**Table 4-1. Pin Attributes**

| FR597x(1),<br>FR587x(1) | FR592x(1) |         | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL<br>TYPE <sup>(3)</sup> | BUFFER<br>TYPE <sup>(4)</sup> | POWER<br>SOURCE | RESET<br>STATE<br>AFTER<br>BOR <sup>(5)</sup> |
|-------------------------|-----------|---------|--------------------------------|-------------------------------|-------------------------------|-----------------|-----------------------------------------------|
|                         | PM, RGC   | DGG     |                                |                               |                               |                 |                                               |
|                         | PIN NO.   | PIN NO. |                                |                               |                               |                 |                                               |
| 1                       | 1         |         | P4.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0RXD                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 2                       | 2         | 7       | P1.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB0CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 3                       | 3         | 8       | P1.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB0STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA0.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 4                       | 4         | 9       | P1.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB0SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB0SDA                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | BSL_DAT                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA0.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 5                       | 5         | 10      | P1.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB0SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB0SCL                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | BSL_CLK                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA0.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 6                       | 6         | 11      | DNC <sup>(6)</sup>             | –                             | –                             | –               | –                                             |
| 7                       | 7         | 12      | P6.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
| 8                       | 8         | 13      | P6.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
| 9                       | 9         | 14      | P6.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | COUT                           | O                             | LVC MOS                       | DVCC            | –                                             |
| 10                      | 10        | 15      | P6.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
| 11                      | 11        | 16      | P6.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TB0.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 12                      | 12        | 17      | P6.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TB0.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 13                      | 13        | 18      | P6.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TB0.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |

(1) Signals names with (RD) denote the reset default pin name.

(2) To determine the pin mux encodings for each pin, see the [Port I/O Diagrams](#) section.

(3) Signal Types: I = Input, O = Output, I/O = Input or Output.

(4) Buffer Types: LVC MOS, Analog, or Power (see [Table 4-3](#) for details)

(5) Reset States:

OFF = High impedance with Schmitt-trigger inputs and pullup or pulldown (if available) disabled

N/A = Not applicable

(6) DNC = Do not connect

**Table 4-1. Pin Attributes (continued)**

| FR597x(1),<br>FR587x(1) | FR592x(1) |         | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL<br>TYPE <sup>(3)</sup> | BUFFER<br>TYPE <sup>(4)</sup> | POWER<br>SOURCE | RESET<br>STATE<br>AFTER<br>BOR <sup>(5)</sup> |
|-------------------------|-----------|---------|--------------------------------|-------------------------------|-------------------------------|-----------------|-----------------------------------------------|
|                         | PM, RGC   | DGG     |                                |                               |                               |                 |                                               |
|                         | PIN NO.   | PIN NO. |                                |                               |                               |                 |                                               |
| 14                      | 14        | 19      | P3.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA3.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 15                      | 15        | 20      | P3.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1SDA                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA3.3                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 16                      | 16        | 21      | P3.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1SCL                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA3.4                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 17                      | 17        |         | DVSS1                          | P                             | Power                         | –               | N/A                                           |
| 18                      | 18        |         | DVCC1                          | P                             | Power                         | –               | N/A                                           |
| 19                      | 19        | 22      | TEST                           | I                             | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | SBWTCK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 20                      | 20        | 23      | RST                            | I                             | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | NMI                            | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SBWTDIO                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 21                      | 21        | 24      | PJ.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TDO                            | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0OUTH                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SMCLK                          | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SRSCG1                         | O                             | LVC MOS                       | DVCC            | –                                             |
| 22                      | 22        | 25      | PJ.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TDI                            | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TCLK                           | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | MCLK                           | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SRSCG0                         | O                             | LVC MOS                       | DVCC            | –                                             |
| 23                      | 23        | 26      | PJ.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TMS                            | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | ACLK                           | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SROSCOFF                       | O                             | LVC MOS                       | DVCC            | –                                             |
| 24                      | 24        | 27      | PJ.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TCK                            | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | COUT                           | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | SRCPUOFF                       | O                             | LVC MOS                       | DVCC            | –                                             |
| 25                      | 25        | 28      | P3.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA1.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 26                      | 26        | 29      | P3.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA1TXD                        | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |

**Table 4-1. Pin Attributes (continued)**

| FR597x(1),<br>FR587x(1) | FR592x(1) |         | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL<br>TYPE <sup>(3)</sup> | BUFFER<br>TYPE <sup>(4)</sup> | POWER<br>SOURCE | RESET<br>STATE<br>AFTER<br>BOR <sup>(5)</sup> |
|-------------------------|-----------|---------|--------------------------------|-------------------------------|-------------------------------|-----------------|-----------------------------------------------|
|                         | PM, RGC   | DGG     |                                |                               |                               |                 |                                               |
|                         | PIN NO.   | PIN NO. |                                |                               |                               |                 |                                               |
| 27                      | 27        | 30      | P3.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA1RXD                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 28                      | 28        | 31      | P3.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 29                      | 29        | 32      | P3.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.3                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 30                      | 30        | 33      | P2.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0OUTH                        | I                             | LVC MOS                       | DVCC            | –                                             |
| 31                      | 31        | 34      | P2.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.4                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | RTCCLK                         | O                             | LVC MOS                       | DVCC            | –                                             |
| 32                      | 32        | 35      | P2.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0RXD                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | BSL_RX                         | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.5                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | DMAE0                          | I                             | LVC MOS                       | DVCC            | –                                             |
| 33                      | 33        | 36      | P2.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0TXD                        | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | BSL_TX                         | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0.6                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 34                      | 34        | 37      | P7.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 35                      | 35        | 38      | P7.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | ACLK                           | O                             | LVC MOS                       | DVCC            | –                                             |
| 36                      | 36        | 39      | P7.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 37                      | 37        | 40      | P7.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 38                      | 38        | 41      | P7.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | SMCLK                          | O                             | LVC MOS                       | DVCC            | –                                             |
| 39                      | 39        | 42      | DVSS2                          | P                             | Power                         | –               | N/A                                           |
| 40                      | 40        | 43      | DVCC2                          | P                             | Power                         | –               | N/A                                           |

**Table 4-1. Pin Attributes (continued)**

| FR597x(1),<br>FR587x(1) | FR592x(1) |         | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL<br>TYPE <sup>(3)</sup> | BUFFER<br>TYPE <sup>(4)</sup> | POWER<br>SOURCE | RESET<br>STATE<br>AFTER<br>BOR <sup>(5)</sup> |
|-------------------------|-----------|---------|--------------------------------|-------------------------------|-------------------------------|-----------------|-----------------------------------------------|
|                         | PM, RGC   | DGG     |                                |                               |                               |                 |                                               |
|                         | PIN NO.   | PIN NO. |                                |                               |                               |                 |                                               |
| 41                      | 41        | 44      | P1.3 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA1.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | A3                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C3                             | I                             | Analog                        | AVCC            | –                                             |
| 42                      | 42        | 45      | P1.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA1.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA0CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | COUT                           | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | A2                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C2                             | I                             | Analog                        | AVCC            | –                                             |
| 43                      | 43        | 46      | P1.1 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | COUT                           | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | A1                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C1                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | VREF+                          | O                             | Analog                        | AVCC            | –                                             |
|                         |           |         | VeREF+                         | I                             | Analog                        | –               | –                                             |
| 44                      | 44        | 47      | P1.0 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | TA0.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | DMAE0                          | I                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | RTCCLK                         | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | A0                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C0                             | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | VREF-                          | O                             | Analog                        | AVCC            | –                                             |
|                         |           |         | VeREF-                         | I                             | Analog                        | –               | –                                             |
| 45                      | 45        | 48      | P9.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | A12                            | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C12                            | I                             | Analog                        | AVCC            | –                                             |
| 46                      | 46        | 49      | P9.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | A13                            | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C13                            | I                             | Analog                        | AVCC            | –                                             |
| 47                      | 47        | 50      | P9.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | A14                            | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C14                            | I                             | Analog                        | AVCC            | –                                             |
| 48                      | 48        | 51      | P9.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | A15                            | I                             | Analog                        | AVCC            | –                                             |
|                         |           |         | C15                            | I                             | Analog                        | AVCC            | –                                             |
| 49                      | 49        | 52      | AVCC1                          | P                             | Power                         | –               | N/A                                           |
| 50                      | 50        | 53      | AVSS1                          | P                             | Power                         | –               | N/A                                           |
| 51                      | 51        | 54      | PJ.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | LFXIN                          | I                             | Analog                        | AVCC            | –                                             |
| 52                      | 52        | 55      | PJ.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | LFXOUT                         | O                             | Analog                        | AVCC            | –                                             |
| 53                      | 53        | 56      | AVSS2                          | P                             | Power                         | –               | N/A                                           |

**Table 4-1. Pin Attributes (continued)**

| FR597x(1),<br>FR587x(1) | FR592x(1) |         | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL<br>TYPE <sup>(3)</sup> | BUFFER<br>TYPE <sup>(4)</sup> | POWER<br>SOURCE | RESET<br>STATE<br>AFTER<br>BOR <sup>(5)</sup> |
|-------------------------|-----------|---------|--------------------------------|-------------------------------|-------------------------------|-----------------|-----------------------------------------------|
|                         | PM, RGC   | DGG     |                                |                               |                               |                 |                                               |
|                         | PIN NO.   | PIN NO. |                                |                               |                               |                 |                                               |
| 54                      |           |         | PJ.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | HFXOUT                         | O                             | Analog                        | AVCC            | –                                             |
| 55                      |           |         | PJ.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | HFXIN                          | I                             | Analog                        | AVCC            | –                                             |
| 56                      |           |         | AVSS3                          | P                             | Power                         | –               | N/A                                           |
|                         | 54        |         | P5.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA1TXD                        | O                             | LVC MOS                       | DVCC            | –                                             |
|                         | 55        |         | P5.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA1RXD                        | I                             | LVC MOS                       | DVCC            | –                                             |
|                         | 56        |         | P5.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 57                      | 57        |         | P5.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA1STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TB0CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 58                      | 58        | 1       | P4.4 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1STE                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1CLK                         | I                             | LVC MOS                       | DVCC            | –                                             |
| 59                      | 59        | 2       | P4.5 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1.0                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 60                      | 60        | 3       | P4.6 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1SDA                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1.1                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 61                      | 61        | 4       | P4.7 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCB1SOMI                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1SCL                        | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | TA1.2                          | I/O                           | LVC MOS                       | DVCC            | –                                             |
| 62                      | 62        | 5       | DVSS3                          | P                             | Power                         | –               | N/A                                           |
| 63                      | 63        | 6       | DVCC3                          | P                             | Power                         | –               | N/A                                           |
| 64                      | 64        |         | P4.2 (RD)                      | I/O                           | LVC MOS                       | DVCC            | OFF                                           |
|                         |           |         | UCA0SIMO                       | I/O                           | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCA0TXD                        | O                             | LVC MOS                       | DVCC            | –                                             |
|                         |           |         | UCB1CLK                        | I/O                           | LVC MOS                       | DVCC            | –                                             |

## 4.3 Signal Descriptions

Table 4-2 describes the signals.

**Table 4-2. Signal Descriptions**

| FUNCTION               | SIGNAL NAME | FR597x(1),<br>FR587x(1) | FR592x(1)           |                      | SIGNAL<br>TYPE | DESCRIPTION                                                 |
|------------------------|-------------|-------------------------|---------------------|----------------------|----------------|-------------------------------------------------------------|
|                        |             | PM, RGC                 | PM,<br>RGC          | DGG                  |                |                                                             |
|                        |             | PIN NO.                 | PIN NO.             | PIN NO.              |                |                                                             |
| ADC                    | A0          | 44                      | 44                  | 47                   | I              | Analog input A0                                             |
|                        | A1          | 43                      | 43                  | 46                   | I              | Analog input A1                                             |
|                        | A2          | 42                      | 42                  | 45                   | I              | Analog input A2                                             |
|                        | A3          | 41                      | 41                  | 44                   | I              | Analog input A3                                             |
|                        | A12         | 45                      | 45                  | 48                   | I              | Analog input A12                                            |
|                        | A13         | 46                      | 46                  | 49                   | I              | Analog input A13                                            |
|                        | A14         | 47                      | 47                  | 50                   | I              | Analog input A14                                            |
|                        | A15         | 48                      | 48                  | 51                   | I              | Analog input A15                                            |
|                        | VREF+       | 43                      | 43                  | 46                   | O              | Output of positive reference voltage                        |
|                        | VREF-       | 44                      | 44                  | 47                   | O              | Output of negative reference voltage                        |
|                        | VeREF+      | 43                      | 43                  | 46                   | I              | Input for an external positive reference voltage to the ADC |
|                        | VeREF-      | 44                      | 44                  | 47                   | I              | Input for an external negative reference voltage to the ADC |
| BSL (I <sup>2</sup> C) | BSL_CLK     | 5                       | 5                   | 10                   | I              | BSL Clock (I <sup>2</sup> C BSL)                            |
|                        | BSL_DAT     | 4                       | 4                   | 9                    | I              | BSL Data (I <sup>2</sup> C BSL)                             |
| BSL (UART)             | BSL_RX      | 32                      | 32                  | 35                   | I              | BSL Receive (UART BSL)                                      |
|                        | BSL_TX      | 33                      | 33                  | 36                   | O              | BSL Transmit (UART BSL)                                     |
| Clock                  | ACLK        | 23<br>35                | 23<br>35            | 26<br>38             | O              | ACLK output                                                 |
|                        | HFXIN       | 55                      |                     |                      | I              | Input terminal of crystal oscillator XT2                    |
|                        | HFXOUT      | 54                      |                     |                      | O              | Output terminal for crystal oscillator XT2                  |
|                        | LFXIN       | 51                      | 51                  | 54                   | I              | Input terminal for crystal oscillator XT1                   |
|                        | LFXOUT      | 52                      | 52                  | 55                   | O              | Output terminal of crystal oscillator XT1                   |
|                        | MCLK        | 22                      | 22                  | 25                   | O              | MCLK output                                                 |
|                        | RTCCLK      | 31<br>44                | 31<br>44            | 34<br>47             | O              | RTC clock output for calibration                            |
|                        | SMCLK       | 21<br>38                | 21<br>38            | 24<br>41             | O              | SMCLK output                                                |
| Comparator             | C0          | 44                      | 44                  | 47                   | I              | Comparator input C0                                         |
|                        | C1          | 43                      | 43                  | 46                   | I              | Comparator input C1                                         |
|                        | C2          | 42                      | 42                  | 45                   | I              | Comparator input C2                                         |
|                        | C3          | 41                      | 41                  | 44                   | I              | Comparator input C3                                         |
|                        | C12         | 45                      | 45                  | 48                   | I              | Comparator input C12                                        |
|                        | C13         | 46                      | 46                  | 49                   | I              | Comparator input C13                                        |
|                        | C14         | 47                      | 47                  | 50                   | I              | Comparator input C14                                        |
|                        | C15         | 48                      | 48                  | 51                   | I              | Comparator input C15                                        |
|                        | COUT        | 9<br>24<br>42<br>43     | 9<br>24<br>42<br>43 | 14<br>27<br>45<br>46 | O              | Comparator output                                           |
| DMA                    | DMAE0       | 32<br>44                | 32<br>44            | 32<br>44             | I              | DMA external trigger input                                  |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | FR597x(1),<br>FR587x(1) | FR592x(1)  |         | SIGNAL<br>TYPE | DESCRIPTION                                                                  |
|----------|-------------|-------------------------|------------|---------|----------------|------------------------------------------------------------------------------|
|          |             | PM, RGC                 | PM,<br>RGC | DGG     |                |                                                                              |
|          |             | PIN NO.                 | PIN NO.    | PIN NO. |                |                                                                              |
| DNC      | DNC         | 6                       | 6          | 22      | –              | Do Not Connect (DNC). TI strongly recommends leaving this pin not connected. |
| Debug    | SBWTCK      | 19                      | 19         | 23      | I              | Spy-Bi-Wire input clock                                                      |
|          | SBWTDIO     | 20                      | 20         | 27      | I/O            | Spy-Bi-Wire data input/output                                                |
|          | SRCPUOFF    | 24                      | 24         | 26      | O              | Low-power debug: CPU status register CPUOFF                                  |
|          | SROSCOFF    | 23                      | 23         | 25      | O              | Low-power debug: CPU status register OSCOFF                                  |
|          | SRSCG0      | 22                      | 22         | 24      | O              | Low-power debug: CPU status register SCG0                                    |
|          | SRSCG1      | 21                      | 21         | 27      | O              | Low-power debug: CPU status register SCG1                                    |
|          | TCK         | 24                      | 24         | 25      | I              | Test clock                                                                   |
|          | TCLK        | 22                      | 22         | 25      | I              | Test clock input                                                             |
|          | TDI         | 22                      | 22         | 24      | I              | Test data input                                                              |
|          | TDO         | 21                      | 21         | 22      | O              | Test data output port                                                        |
|          | TEST        | 19                      | 19         | 26      | I              | Test mode pin - select digital I/O on JTAG pins                              |
|          | TMS         | 23                      | 23         | 23      | I              | Test mode select                                                             |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | FR597x(1),<br>FR587x(1) | FR592x(1)  |         | SIGNAL<br>TYPE | DESCRIPTION                 |
|----------|-------------|-------------------------|------------|---------|----------------|-----------------------------|
|          |             | PM, RGC                 | PM,<br>RGC | DGG     |                |                             |
|          |             | PIN NO.                 | PIN NO.    | PIN NO. |                |                             |
| GPIO     | P1.0        | 44                      | 44         | 47      | I/O            | General-purpose digital I/O |
|          | P1.1        | 43                      | 43         | 46      | I/O            | General-purpose digital I/O |
|          | P1.2        | 42                      | 42         | 45      | I/O            | General-purpose digital I/O |
|          | P1.3        | 41                      | 41         | 44      | I/O            | General-purpose digital I/O |
|          | P1.4        | 2                       | 2          | 7       | I/O            | General-purpose digital I/O |
|          | P1.5        | 3                       | 3          | 8       | I/O            | General-purpose digital I/O |
|          | P1.6        | 4                       | 4          | 9       | I/O            | General-purpose digital I/O |
|          | P1.7        | 5                       | 5          | 10      | I/O            | General-purpose digital I/O |
|          | P2.0        | 33                      | 33         | 36      | I/O            | General-purpose digital I/O |
|          | P2.1        | 32                      | 32         | 35      | I/O            | General-purpose digital I/O |
|          | P2.2        | 31                      | 31         | 34      | I/O            | General-purpose digital I/O |
|          | P2.3        | 30                      | 30         | 33      | I/O            | General-purpose digital I/O |
|          | P3.0        | 14                      | 14         | 19      | I/O            | General-purpose digital I/O |
|          | P3.1        | 15                      | 15         | 20      | I/O            | General-purpose digital I/O |
|          | P3.2        | 16                      | 16         | 21      | I/O            | General-purpose digital I/O |
|          | P3.3        | 25                      | 25         | 28      | I/O            | General-purpose digital I/O |
|          | P3.4        | 26                      | 26         | 29      | I/O            | General-purpose digital I/O |
|          | P3.5        | 27                      | 27         | 30      | I/O            | General-purpose digital I/O |
|          | P3.6        | 28                      | 28         | 31      | I/O            | General-purpose digital I/O |
|          | P3.7        | 29                      | 29         | 32      | I/O            | General-purpose digital I/O |
|          | P4.2        | 64                      | 64         |         | I/O            | General-purpose digital I/O |
|          | P4.3        | 1                       | 1          |         | I/O            | General-purpose digital I/O |
|          | P4.4        | 58                      | 58         | 1       | I/O            | General-purpose digital I/O |
|          | P4.5        | 59                      | 59         | 2       | I/O            | General-purpose digital I/O |
|          | P4.6        | 60                      | 60         | 3       | I/O            | General-purpose digital I/O |
|          | P4.7        | 61                      | 61         | 4       | I/O            | General-purpose digital I/O |
|          | P5.4        |                         | 54         |         | I/O            | General-purpose digital I/O |
|          | P5.5        |                         | 55         |         | I/O            | General-purpose digital I/O |
|          | P5.6        |                         | 56         |         | I/O            | General-purpose digital I/O |
|          | P5.7        | 57                      | 57         |         | I/O            | General-purpose digital I/O |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | FR597x(1),<br>FR587x(1) | FR592x(1)  |         | SIGNAL<br>TYPE | DESCRIPTION                                             |
|------------------|-------------|-------------------------|------------|---------|----------------|---------------------------------------------------------|
|                  |             | PM, RGC                 | PM,<br>RGC | DGG     |                |                                                         |
|                  |             | PIN NO.                 | PIN NO.    | PIN NO. |                |                                                         |
| GPIO             | P6.0        | 7                       | 7          | 12      | I/O            | General-purpose digital I/O                             |
|                  | P6.1        | 8                       | 8          | 13      | I/O            | General-purpose digital I/O                             |
|                  | P6.2        | 9                       | 9          | 14      | I/O            | General-purpose digital I/O                             |
|                  | P6.3        | 10                      | 10         | 15      | I/O            | General-purpose digital I/O                             |
|                  | P6.4        | 11                      | 11         | 16      | I/O            | General-purpose digital I/O                             |
|                  | P6.5        | 12                      | 12         | 17      | I/O            | General-purpose digital I/O                             |
|                  | P6.6        | 13                      | 13         | 18      | I/O            | General-purpose digital I/O                             |
|                  | P7.0        | 34                      | 34         | 37      | I/O            | General-purpose digital I/O                             |
|                  | P7.1        | 35                      | 35         | 38      | I/O            | General-purpose digital I/O                             |
|                  | P7.2        | 36                      | 36         | 39      | I/O            | General-purpose digital I/O                             |
|                  | P7.3        | 37                      | 37         | 40      | I/O            | General-purpose digital I/O                             |
|                  | P7.4        | 38                      | 38         | 41      | I/O            | General-purpose digital I/O                             |
|                  | P9.4        | 45                      | 45         | 48      | I/O            | General-purpose digital I/O                             |
|                  | P9.5        | 46                      | 46         | 49      | I/O            | General-purpose digital I/O                             |
|                  | P9.6        | 47                      | 47         | 50      | I/O            | General-purpose digital I/O                             |
|                  | P9.7        | 48                      | 48         | 51      | I/O            | General-purpose digital I/O                             |
|                  | PJ.0        | 21                      | 21         | 24      | I/O            | General-purpose digital I/O                             |
|                  | PJ.1        | 22                      | 22         | 25      | I/O            | General-purpose digital I/O                             |
|                  | PJ.2        | 23                      | 23         | 26      | I/O            | General-purpose digital I/O                             |
|                  | PJ.3        | 24                      | 24         | 27      | I/O            | General-purpose digital I/O                             |
|                  | PJ.4        | 51                      | 51         | 54      | I/O            | General-purpose digital I/O                             |
|                  | PJ.5        | 52                      | 52         | 55      | I/O            | General-purpose digital I/O                             |
|                  | PJ.6        | 55                      | 55         |         | I/O            | General-purpose digital I/O                             |
|                  | PJ.7        | 54                      | 54         |         | I/O            | General-purpose digital I/O                             |
| I <sup>2</sup> C | UCB0SCL     | 5                       | 5          | 10      | I/O            | USCI_B0: I <sup>2</sup> C clock (I <sup>2</sup> C mode) |
|                  | UCB0SDA     | 4                       | 4          | 9       | I/O            | USCI_B0: I <sup>2</sup> C data (I <sup>2</sup> C mode)  |
|                  | UCB1SCL     | 16<br>61                | 16<br>61   | 21<br>4 | I/O            | USCI_B1: I <sup>2</sup> C clock (I <sup>2</sup> C mode) |
|                  | UCB1SDA     | 15<br>60                | 15<br>60   | 20<br>3 | I/O            | USCI_B1: I <sup>2</sup> C data (I <sup>2</sup> C mode)  |
| Power            | AVCC1       | 49                      | 49         | 52      | P              | Analog power supply                                     |
|                  | AVSS1       | 50                      | 50         | 53      | P              | Analog ground supply                                    |
|                  | AVSS2       | 53                      | 53         | 56      | P              | Analog ground supply                                    |
|                  | AVSS3       | 56                      |            |         | P              | Analog ground supply                                    |
|                  | DVCC1       | 18                      | 18         |         | P              | Digital power supply                                    |
|                  | DVCC2       | 40                      | 40         | 43      | P              | Digital power supply                                    |
|                  | DVCC3       | 63                      | 63         | 6       | P              | Digital power supply                                    |
|                  | DVSS1       | 17                      | 17         |         | P              | Digital ground supply                                   |
|                  | DVSS2       | 39                      | 39         | 42      | P              | Digital ground supply                                   |
|                  | DVSS3       | 62                      | 62         | 5       | P              | Digital ground supply                                   |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME             | FR597x(1),<br>FR587x(1) | FR592x(1)      |         | SIGNAL<br>TYPE | DESCRIPTION                                                                            |
|----------|-------------------------|-------------------------|----------------|---------|----------------|----------------------------------------------------------------------------------------|
|          |                         | PM, RGC                 | PM,<br>RGC     | DGG     |                |                                                                                        |
|          |                         | PIN NO.                 | PIN NO.        | PIN NO. |                |                                                                                        |
| SPI      | UCA0CLK                 | 3<br>31                 | 3<br>31        | 8<br>34 | I/O            | USCI_A0: Clock signal input (SPI slave mode),<br>Clock signal output (SPI master mode) |
|          | UCA0SIMO                | 33<br>64                | 33<br>64       | 36      | I/O            | USCI_A0: Slave in, master out (SPI mode)                                               |
|          | UCA0SOMI                | 1<br>32                 | 1<br>32        | 35      | I/O            | USCI_A0: Slave out, master in (SPI mode)                                               |
|          | UCA0STE                 | 2<br>30                 | 2<br>30        | 7<br>33 | I/O            | USCI_A0: Slave transmit enable (SPI mode)                                              |
|          | UCA1CLK                 | 28                      | 28<br>56       | 31      | I/O            | USCI_A1: Clock signal input (SPI slave mode),<br>Clock signal output (SPI master mode) |
|          | UCA1SIMO                | 26                      | 26<br>54       | 29      | I/O            | USCI_A1: Slave in, master out (SPI mode)                                               |
|          | UCA1SOMI                | 27                      | 27<br>55       | 30      | I/O            | USCI_A1: Slave out, master in (SPI mode)                                               |
|          | UCA1STE                 | 29<br>57                | 29<br>57       | 32      | I/O            | USCI_A1: Slave transmit enable (SPI mode)                                              |
|          | UCB0CLK                 | 2                       | 2              | 7       | I/O            | USCI_B0: Clock signal input (SPI slave mode),<br>Clock signal output (SPI master mode) |
|          | UCB0SIMO                | 4                       | 4              | 9       | I/O            | USCI_B0: Slave in, master out (SPI mode)                                               |
|          | UCB0SOMI                | 5                       | 5              | 10      | I/O            | USCI_B0: Slave out, master in (SPI mode)                                               |
|          | UCB0STE                 | 3                       | 3              | 8       | I/O            | USCI_B0: Slave transmit enable (SPI mode)                                              |
|          | UCB1CLK                 | 14<br>59<br>64          | 14<br>59<br>64 | 19<br>2 | I/O            | USCI_B1: Clock signal input (SPI slave mode),<br>Clock signal output (SPI master mode) |
|          | UCB1SIMO                | 15<br>60                | 15<br>60       | 3<br>20 | I/O            | USCI_B1: Slave in, master out (SPI mode)                                               |
|          | UCB1SOMI                | 16<br>61                | 16<br>61       | 21<br>4 | I/O            | USCI_B1: Slave out, master in (SPI mode)                                               |
|          | UCB1STE                 | 1<br>58                 | 1<br>58        | 1       | I/O            | USCI_B1: Slave transmit enable (SPI mode)                                              |
| System   | NMI                     | 20                      | 20             | 23      | I              | Nonmaskable interrupt input                                                            |
|          | $\overline{\text{RST}}$ | 20                      | 20             | 23      | I              | Reset input active low                                                                 |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION    | SIGNAL NAME | FR597x(1),<br>FR587x(1) | FR592x(1)      |                | SIGNAL<br>TYPE | DESCRIPTION                                                                                       |
|-------------|-------------|-------------------------|----------------|----------------|----------------|---------------------------------------------------------------------------------------------------|
|             |             | PM, RGC                 | PM,<br>RGC     | DGG            |                |                                                                                                   |
|             |             | PIN NO.                 | PIN NO.        | PIN NO.        |                |                                                                                                   |
| Timer_A     | TA0.0       | 3<br>35                 | 3<br>35        | 8<br>38        | I/O            | Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output                                       |
|             | TA0.1       | 4<br>36<br>44           | 4<br>36<br>44  | 9<br>39<br>47  | I/O            | Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output                                       |
|             | TA0.2       | 5<br>37<br>43           | 5<br>37<br>43  | 10<br>40<br>46 | I/O            | Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output                                       |
|             | TA0CLK      | 34<br>42                | 34<br>42       | 37<br>45       | I              | Timer_A TA0 clock signal TA0CLK input                                                             |
|             | TA1.0       | 2<br>59                 | 2<br>59        | 7<br>2         | I/O            | Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output                                       |
|             | TA1.1       | 25<br>42<br>60          | 25<br>42<br>60 | 28<br>45<br>3  | I/O            | Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output                                       |
|             | TA1.2       | 41<br>61                | 41<br>61       | 44<br>4        | I/O            | Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output                                       |
|             | TA1CLK      | 43<br>58                | 43<br>58       | 46<br>1        | I              | Timer_A TA1 clock signal TA1CLK input                                                             |
|             | TA3.2       | 14                      | 14             | 19             | I/O            | Timer_A TA3 CCR2 capture: CCI2B input, compare: Out2 output                                       |
|             | TA3.3       | 15                      | 15             | 20             | I/O            | Timer_A TA3 CCR3 capture: CCI3B input, compare: Out3 output                                       |
|             | TA3.4       | 16                      | 16             | 21             | I/O            | Timer_A TA3 CCR4 capture: CCI4B input, compare: Out4 output                                       |
| Timer_B     | TB0.0       | 11<br>26                | 11<br>26       | 16<br>29       | I/O            | Timer_B TB0 CCR0 capture: CCI0B input, compare: Out0 output                                       |
|             | TB0.1       | 12<br>27                | 12<br>27       | 17<br>30       | I/O            | Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output                                       |
|             | TB0.2       | 13<br>28                | 13<br>28       | 18<br>31       | I/O            | Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output                                       |
|             | TB0.3       | 29                      | 29             | 32             | I/O            | Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output                                       |
|             | TB0.4       | 31                      | 31             | 34             | I/O            | Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output                                       |
|             | TB0.5       | 32                      | 32             | 35             | I/O            | Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output                                       |
|             | TB0.6       | 33                      | 33             | 36             | I/O            | Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output                                       |
|             | TB0CLK      | 25<br>33<br>57          | 25<br>33<br>57 | 28<br>36       | I              | Timer_B TB0 clock signal TB0CLK input                                                             |
|             | TB0OUTH     | 21<br>30                | 21<br>30       | 24<br>33       | I              | Switch all PWM outputs high impedance input - Timer_B TB0                                         |
| UART        | UCA0RXD     | 1<br>32                 | 1<br>32        | 35             | I              | USCI_A0: Receive data (UART mode)                                                                 |
|             | UCA0TXD     | 33<br>64                | 33<br>64       | 36             | O              | USCI_A0: Transmit data (UART mode)                                                                |
|             | UCA1RXD     | 27                      | 27             | 30             | I              | USCI_A1: Receive data (UART mode)                                                                 |
|             | UCA1TXD     | 26                      | 26             | 29             | O              | USCI_A1: Transmit data (UART mode)                                                                |
| Thermal Pad |             |                         |                |                |                | RGC package only. VQFN package exposed thermal pad. TI recommends connection to V <sub>SS</sub> . |

## 4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [6.11.22](#).

## 4.5 Buffer Type

[Table 4-3](#) describes the buffer types that are referenced in [Section 4.2](#).

**Table 4-3. Buffer Type**

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD     | NOMINAL PU OR PD STRENGTH ( $\mu$ A) | OUTPUT DRIVE STRENGTH (mA)           | OTHER CHARACTERISTICS                                       |
|------------------------|-----------------|------------|--------------|--------------------------------------|--------------------------------------|-------------------------------------------------------------|
| LVC MOS                | 3.0 V           | $Y^{(1)}$  | Programmable | See <a href="#">Table 5-11</a>       | See <a href="#">Section 5.12.5.1</a> |                                                             |
| Analog                 | 3.0 V           | N          | N/A          | N/A                                  | N/A                                  | See analog modules in <a href="#">Section 5</a> for details |
| Power (DVCC)           | 3.0 V           | N          | N/A          | N/A                                  | N/A                                  | SVS enables hysteresis on DVCC                              |
| Power (AVCC)           | 3.0 V           | N          | N/A          | N/A                                  | N/A                                  |                                                             |

(1) Only for Input pins.

## 4.6 Connection of Unused Pins

[Table 4-4](#) lists the correct termination of all unused pins.

**Table 4-4. Connection of Unused Pins<sup>(1)</sup>**

| PIN                                          | POTENTIAL                           | COMMENT                                                                                                                                                                                                         |
|----------------------------------------------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AVCC                                         | DV <sub>CC</sub>                    |                                                                                                                                                                                                                 |
| AVSS                                         | DV <sub>SS</sub>                    |                                                                                                                                                                                                                 |
| Px.0 to Px.7                                 | Open                                | Switched to port function, output direction (PxDIR.n = 1)                                                                                                                                                       |
| RST/NMI                                      | DV <sub>CC</sub> or V <sub>CC</sub> | 47-k $\Omega$ pullup or internal pullup selected with 10-nF (2.2 nF <sup>(2)</sup> ) pulldown                                                                                                                   |
| PJ.0/TDO<br>PJ.1/TDI<br>PJ.2/TMS<br>PJ.3/TCK | Open                                | The JTAG pins are shared with general-purpose I/O function (PJ.x). If these pins are not used, they should be set to port function and output direction. When used as JTAG pins, these pins should remain open. |
| TEST                                         | Open                                | This pin always has an internal pulldown enabled.                                                                                                                                                               |

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                              | MIN  | MAX                                    | UNIT |
|--------------------------------------------------------------|------|----------------------------------------|------|
| Voltage applied at DVCC and AVCC pins to V <sub>SS</sub>     | –0.3 | 4.1                                    | V    |
| Voltage difference between DVCC and AVCC pins <sup>(2)</sup> |      | ±0.3                                   | V    |
| Voltage applied to any pin <sup>(3)</sup>                    | –0.3 | V <sub>CC</sub> + 0.3<br>(4.1 Maximum) | V    |
| Diode current at any device pin                              |      | ±2                                     | mA   |
| Storage temperature, T <sub>stg</sub> <sup>(4)</sup>         | –40  | 125                                    | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (3) All voltages referenced to V<sub>SS</sub>.
- (4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 5.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

### 5.3 Recommended Operating Conditions

Typical data are based on V<sub>CC</sub> = 3.0 V, T<sub>A</sub> = 25°C (unless otherwise noted)

|                     |                                                                         | MIN                                                | NOM | MAX               | UNIT              |
|---------------------|-------------------------------------------------------------------------|----------------------------------------------------|-----|-------------------|-------------------|
| V <sub>CC</sub>     | Supply voltage applied at all DVCC and AVCC pins <sup>(1) (2) (3)</sup> | 1.8 <sup>(4)</sup>                                 |     | 3.6               | V                 |
| V <sub>SS</sub>     | Supply voltage applied at all DVSS and AVSS pins                        |                                                    | 0   |                   | V                 |
| T <sub>A</sub>      | Operating free-air temperature                                          | –40                                                |     | 85                | °C                |
| T <sub>J</sub>      | Operating junction temperature                                          | –40                                                |     | 85                | °C                |
| C <sub>DVCC</sub>   | Capacitor value at DVCC <sup>(5)</sup>                                  | 1 <sub>–20%</sub>                                  |     |                   | μF                |
| f <sub>SYSTEM</sub> | Processor frequency (maximum MCLK frequency) <sup>(6)</sup>             | No FRAM wait states (NWAITSx = 0)                  |     | 0                 | 8 <sup>(7)</sup>  |
|                     |                                                                         | With FRAM wait states (NWAITSx = 1) <sup>(8)</sup> |     | 0                 | 16 <sup>(9)</sup> |
| f <sub>ACLK</sub>   | Maximum ACLK frequency                                                  |                                                    |     | 50                | kHz               |
| f <sub>SMCLK</sub>  | Maximum SMCLK frequency                                                 |                                                    |     | 16 <sup>(9)</sup> | MHz               |

- (1) TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/μs). Following the data sheet recommendation for capacitor C<sub>DVCC</sub> should limit the slopes accordingly.
- (3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (4) The minimum supply voltage is defined by the supervisor SVS levels. See the PMM SVS threshold parameters in [Table 5-2](#) for the exact values.
- (5) As decoupling capacitor for each supply pin pair (DVCC and DVSS, AVCC and AVSS), a low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pairs.
- (6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (7) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
- (8) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
- (9) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock source with a higher typical value is used, the clock must be divided in the clock system.

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                 | EXECUTION MEMORY             | V <sub>CC</sub> | FREQUENCY (f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |     |                                                     |     |                                                     |      |                                                      |      |                                                      |      | UNIT |
|-----------------------------------------------------------|------------------------------|-----------------|-----------------------------------------------------|-----|-----------------------------------------------------|-----|-----------------------------------------------------|------|------------------------------------------------------|------|------------------------------------------------------|------|------|
|                                                           |                              |                 | 1 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 4 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 8 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |      | 12 MHz<br>1 WAIT STATES<br>(NWAITS <sub>x</sub> = 1) |      | 16 MHz<br>1 WAIT STATES<br>(NWAITS <sub>x</sub> = 1) |      |      |
|                                                           |                              |                 | TYP                                                 | MAX | TYP                                                 | MAX | TYP                                                 | MAX  | TYP                                                  | MAX  | TYP                                                  | MAX  |      |
| I <sub>AM, FRAM_UNI</sub> (Unified memory) <sup>(3)</sup> | FRAM                         | 3.0 V           | 210                                                 |     | 640                                                 |     | 1220                                                |      | 1475                                                 |      | 1845                                                 |      | μA   |
| I <sub>AM, FRAM(0%)</sub> <sup>(4) (5)</sup>              | FRAM<br>0% cache hit ratio   | 3.0 V           | 370                                                 |     | 1280                                                |     | 2510                                                |      | 2080                                                 |      | 2650                                                 |      | μA   |
| I <sub>AM, FRAM(50%)</sub> <sup>(4) (5)</sup>             | FRAM<br>50% cache hit ratio  | 3.0 V           | 240                                                 |     | 745                                                 |     | 1440                                                |      | 1575                                                 |      | 1990                                                 |      | μA   |
| I <sub>AM, FRAM(66%)</sub> <sup>(4) (5)</sup>             | FRAM<br>66% cache hit ratio  | 3.0 V           | 200                                                 |     | 560                                                 |     | 1070                                                |      | 1300                                                 |      | 1620                                                 |      | μA   |
| I <sub>AM, FRAM(75%)</sub> <sup>(4) (5)</sup>             | FRAM<br>75% cache hit ratio  | 3.0 V           | 170                                                 | 255 | 480                                                 |     | 890                                                 | 1085 | 1155                                                 | 1310 | 1420                                                 | 1620 | μA   |
| I <sub>AM, FRAM(100%)</sub> <sup>(4) (5)</sup>            | FRAM<br>100% cache hit ratio | 3.0 V           | 110                                                 |     | 235                                                 |     | 420                                                 |      | 640                                                  |      | 730                                                  |      | μA   |
| I <sub>AM, RAM</sub> <sup>(6) (5)</sup>                   | RAM                          | 3.0 V           | 130                                                 |     | 320                                                 |     | 585                                                 |      | 890                                                  |      | 1070                                                 |      | μA   |
| I <sub>AM, RAM only</sub> <sup>(7) (5)</sup>              | RAM                          | 3.0 V           | 100                                                 | 180 | 290                                                 |     | 555                                                 |      | 860                                                  |      | 1040                                                 | 1300 | μA   |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = f_{SMCLK} = f_{DCO}$  at specified frequency, except for 12 MHz. For 12 MHz,  $f_{DCO} = 24$  MHz and  $f_{MCLK} = f_{SMCLK} = f_{DCO}/2$ .

At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ( $f_{MCLK,eff}$ ) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.

The following equation can be used to compute  $f_{MCLK,eff}$ :

$f_{MCLK,eff} = f_{MCLK} / [\text{wait states} \times (1 - \text{cache hit ratio}) + 1]$

For example, with 1 wait state and 75% cache hit ratio  $f_{MCLK,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$ .

(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.

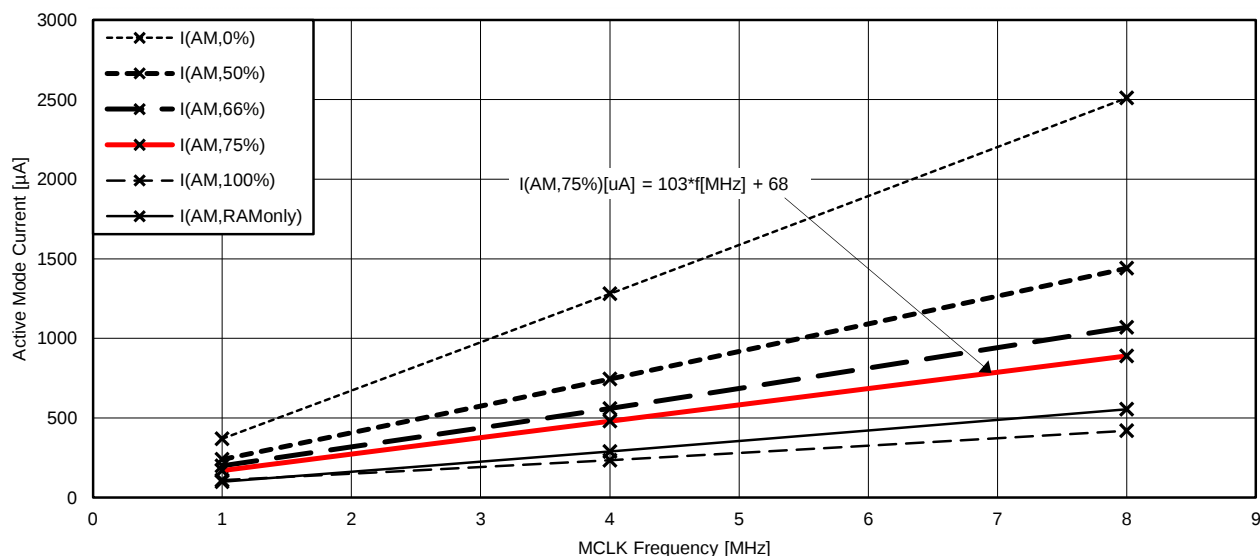
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

(5) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 5.4.

(6) Program and data reside entirely in RAM. All execution is from RAM.

(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

## 5.5 Typical Characteristics - Active Mode Supply Currents



NOTE:  $I(AM, \text{cache hit ratio})$ : Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

NOTE:  $I(AM, RAMOnly)$ : Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

Figure 5-1. Typical Active Mode Supply Currents, No Wait States

## 5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

| PARAMETER         | V <sub>CC</sub> | FREQUENCY (f <sub>SMCLK</sub> ) |     |       |     |       |     |        |     |        |     | UNIT |
|-------------------|-----------------|---------------------------------|-----|-------|-----|-------|-----|--------|-----|--------|-----|------|
|                   |                 | 1 MHz                           |     | 4 MHz |     | 8 MHz |     | 12 MHz |     | 16 MHz |     |      |
|                   |                 | TYP                             | MAX | TYP   | MAX | TYP   | MAX | TYP    | MAX | TYP    | MAX |      |
| I <sub>LPM0</sub> | 2.2 V           | 75                              |     | 105   |     | 165   |     | 250    |     | 230    |     | μA   |
|                   | 3.0 V           | 80                              | 120 | 115   |     | 175   |     | 260    |     | 240    | 275 |      |
| I <sub>LPM1</sub> | 2.2 V           | 40                              |     | 65    |     | 130   |     | 215    |     | 195    |     | μA   |
|                   | 3.0 V           | 40                              | 65  | 65    |     | 130   |     | 215    |     | 195    | 220 |      |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = 0$  MHz,  $f_{SMCLK} = f_{DCO}$  at specified frequency - except for 12 MHz: here  $f_{DCO} = 24$  MHz and  $f_{SMCLK} = f_{DCO}/2$ .

## 5.7 Low-Power Mode LPM2, LPM3, LPM4 Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER                                                                                                    | $V_{CC}$ | -40°C |     | 25°C |     | 60°C |     | 85°C |      | UNIT    |
|--------------------------------------------------------------------------------------------------------------|----------|-------|-----|------|-----|------|-----|------|------|---------|
|                                                                                                              |          | TYP   | MAX | TYP  | MAX | TYP  | MAX | TYP  | MAX  |         |
| $I_{LPM2,XT12}$ Low-power mode 2, 12-pF crystal <sup>(2) (3) (4)</sup>                                       | 2.2 V    | 0.8   |     | 1.2  |     | 3.1  |     | 8.8  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.8   |     | 1.2  | 2.2 | 3.1  |     | 8.8  | 17   |         |
| $I_{LPM2,XT3.7}$ Low-power mode 2, 3.7-pF crystal <sup>(2) (5) (4)</sup>                                     | 2.2 V    | 0.7   |     | 1.1  |     | 3.0  |     | 8.7  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.7   |     | 1.1  |     | 3.0  |     | 8.7  |      |         |
| $I_{LPM2,VLO}$ Low-power mode 2, VLO, includes SVS <sup>(6)</sup>                                            | 2.2 V    | 0.5   |     | 0.9  |     | 2.8  |     | 8.5  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.5   |     | 0.9  | 2.0 | 2.8  |     | 8.5  | 16.7 |         |
| $I_{LPM3,XT12}$ Low-power mode 3, 12-pF crystal, includes SVS <sup>(2) (3) (7)</sup>                         | 2.2 V    | 0.7   |     | 0.9  |     | 1.2  |     | 2.5  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.7   |     | 0.9  | 1.2 | 1.2  |     | 2.5  | 6.4  |         |
| $I_{LPM3,XT3.7}$ Low-power mode 3, 3.7-pF crystal, excludes SVS <sup>(2) (5) (8)</sup> (also see Figure 5-2) | 2.2 V    | 0.6   |     | 0.7  |     | 1.1  |     | 2.4  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.6   |     | 0.7  |     | 1.1  |     | 2.4  |      |         |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS <sup>(9)</sup>                                            | 2.2 V    | 0.35  |     | 0.4  |     | 0.9  |     | 1.8  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.35  |     | 0.4  | 0.8 | 0.9  |     | 1.8  | 6.1  |         |
| $I_{LPM3,VLO, RAMoff}$ Low-power mode 3, VLO, excludes SVS, RAM powered down completely <sup>(10)</sup>      | 2.2 V    | 0.35  |     | 0.4  |     | 0.8  |     | 1.7  |      | $\mu A$ |
|                                                                                                              | 3.0 V    | 0.35  |     | 0.4  | 0.7 | 0.8  |     | 1.7  | 5.2  |         |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- (2) Not applicable for devices with HF crystal oscillator only.
- (3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
- (4) Low-power mode 2, crystal oscillator test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.  
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),  
 $f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz
- (5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (6) Low-power mode 2, VLO test conditions:  
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.  
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),  
 $f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{VLO}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz
- (7) Low-power mode 3, 12-pF crystal, includes SVS test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz  
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (8) Low-power mode 3, 3.7-pF crystal, excludes SVS test conditions:  
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz  
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (9) Low-power mode 3, VLO, excludes SVS test conditions:  
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{VLO}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz  
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
- (10) Low-power mode 3, VLO, excludes SVS, RAM powered down completely test conditions:  
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).  
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),  
 $f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{VLO}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz  
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

## Low-Power Mode LPM2, LPM3, LPM4 Supply Currents (Into $V_{CC}$ ) Excluding External Current (*continued*)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER                                                                                                               | $V_{CC}$ | –40°C |     | 25°C |      | 60°C |     | 85°C |     | UNIT    |
|-------------------------------------------------------------------------------------------------------------------------|----------|-------|-----|------|------|------|-----|------|-----|---------|
|                                                                                                                         |          | TYP   | MAX | TYP  | MAX  | TYP  | MAX | TYP  | MAX |         |
| $I_{LPM4,SVS}$ Low-power mode 4, includes SVS <sup>(11)</sup>                                                           | 2.2 V    | 0.45  |     | 0.55 |      | 0.9  |     | 1.8  |     | $\mu A$ |
|                                                                                                                         | 3.0 V    | 0.45  |     | 0.55 | 0.8  | 0.9  |     | 1.8  | 6.2 |         |
| $I_{LPM4}$ Low-power mode 4, excludes SVS <sup>(12)</sup>                                                               | 2.2 V    | 0.25  |     | 0.4  |      | 0.7  |     | 1.6  |     | $\mu A$ |
|                                                                                                                         | 3.0 V    | 0.25  |     | 0.4  | 0.65 | 0.7  |     | 1.6  | 4.6 |         |
| $I_{LPM4,RAMoff}$ Low-power mode 4, excludes SVS, RAM powered down completely <sup>(13)</sup>                           | 2.2 V    | 0.25  |     | 0.4  |      | 0.7  |     | 1.4  |     | $\mu A$ |
|                                                                                                                         | 3.0 V    | 0.25  |     | 0.4  | 0.65 | 0.7  |     | 1.4  | 4.6 |         |
| $I_{IDLE,GroupA}$ Additional idle current if one or more modules from Group A (see 6.3.2) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |      |      |     | 0.4  | 1.0 | $\mu A$ |
| $I_{IDLE,GroupB}$ Additional idle current if one or more modules from Group B (see 6.3.2) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |      |      |     | 0.4  | 1.0 | $\mu A$ |
| $I_{IDLE,GroupC}$ Additional idle current if one or more modules from Group C (see 6.3.2) are activated in LPM3 or LPM4 | 3.0 V    |       |     | 0.02 |      |      |     | 0.3  | 0.8 | $\mu A$ |

(11) Low-power mode 4, includes SVS test conditions:

Current for brownout and SVS included (SVSHE = 1).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),

$f_{XT1}$  = 0 Hz,  $f_{ACLK}$  = 0 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(12) Low-power mode 4, excludes SVS test conditions:

Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),

$f_{XT1}$  = 0 Hz,  $f_{ACLK}$  = 0 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(13) Low-power mode 4, excludes SVS, RAM powered down completely test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),

$f_{XT1}$  = 0 Hz,  $f_{ACLK}$  = 0 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

## 5.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                                  | $V_{CC}$ | –40°C |     | 25°C |      | 60°C |     | 85°C |     | UNIT    |
|--------------------------------------------------------------------------------------------|----------|-------|-----|------|------|------|-----|------|-----|---------|
|                                                                                            |          | TYP   | MAX | TYP  | MAX  | TYP  | MAX | TYP  | MAX |         |
| $I_{LPM3.5,XT12}$ Low-power mode 3.5, 12-pF crystal including SVS <sup>(2) (3) (4)</sup>   | 2.2 V    | 0.45  |     | 0.5  |      | 0.6  |     | 0.75 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.45  |     | 0.5  | 0.75 | 0.6  |     | 0.75 | 1.4 |         |
| $I_{LPM3.5,XT3.7}$ Low-power mode 3.5, 3.7-pF crystal excluding SVS <sup>(2) (5) (6)</sup> | 2.2 V    | 0.3   |     | 0.35 |      | 0.4  |     | 0.65 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.3   |     | 0.35 |      | 0.4  |     | 0.65 |     |         |
| $I_{LPM4.5,SVS}$ Low-power mode 4.5, including SVS <sup>(7)</sup>                          | 2.2 V    | 0.2   |     | 0.3  |      | 0.35 |     | 0.4  |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.2   |     | 0.3  | 0.5  | 0.35 |     | 0.4  | 0.7 |         |
| $I_{LPM4.5}$ Low-power mode 4.5, excluding SVS <sup>(8)</sup>                              | 2.2 V    | 0.03  |     | 0.04 |      | 0.06 |     | 0.14 |     | $\mu A$ |
|                                                                                            | 3.0 V    | 0.03  |     | 0.04 |      | 0.06 |     | 0.14 | 0.5 |         |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- (2) Not applicable for devices with HF crystal oscillator only.
- (3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
- (4) Low-power mode 3.5, 1-pF crystal including SVS test conditions:  
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1}$  = 32768 Hz,  $f_{ACLK}$  =  $f_{XT1}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz
- (5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (6) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:  
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1}$  = 32768 Hz,  $f_{ACLK}$  =  $f_{XT1}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz
- (7) Low-power mode 4.5 including SVS test conditions:  
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1}$  = 0 Hz,  $f_{ACLK}$  = 0 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz
- (8) Low-power mode 4.5 excluding SVS test conditions:  
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1}$  = 0 Hz,  $f_{ACLK}$  = 0 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

## 5.9 Typical Characteristics, Low-Power Mode Supply Currents

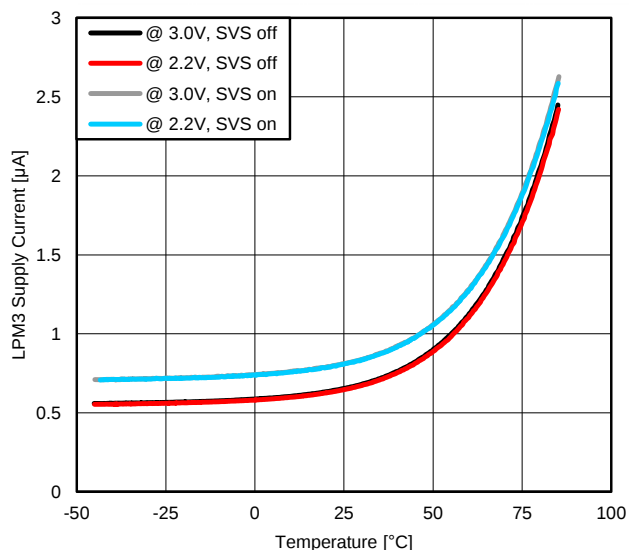


Figure 5-2. LPM3 Supply Current vs Temperature (LPM3,XT3.7)

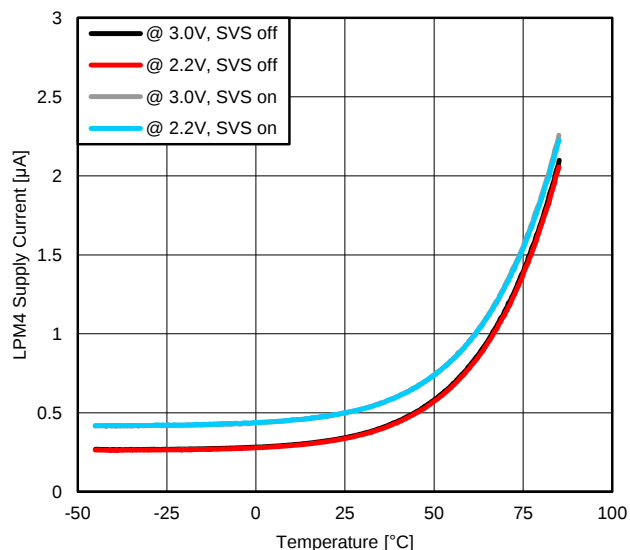


Figure 5-3. LPM4 Supply Current vs Temperature (LPM4,SVS)

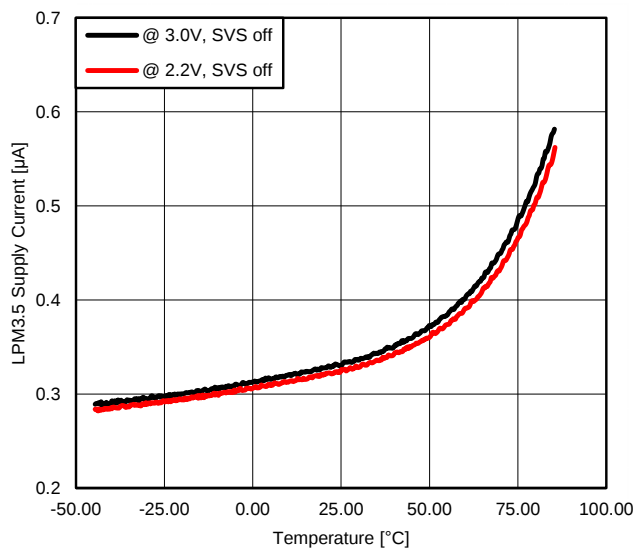


Figure 5-4. LPM3.5 Supply Current vs Temperature (LPM3.5,XT3.7)

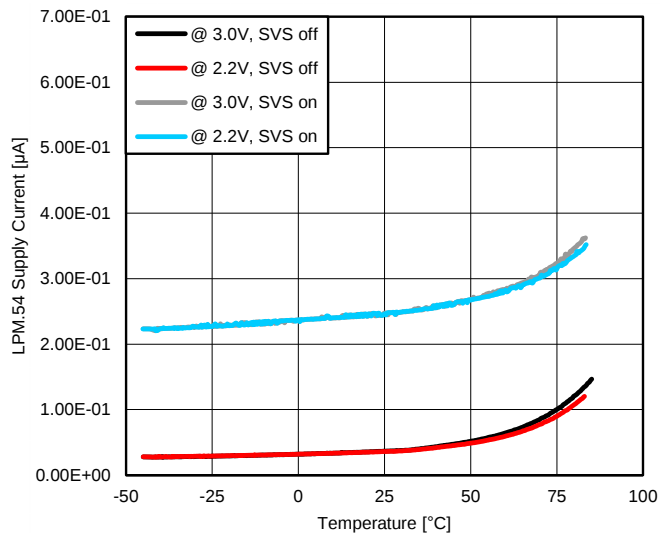


Figure 5-5. LPM4.5 Supply Current vs Temperature (LPM4.5)

## 5.10 Typical Characteristics, Current Consumption per Module

| MODULE  | TEST CONDITIONS                     | REFERENCE CLOCK    | MIN | TYP | MAX | UNIT   |
|---------|-------------------------------------|--------------------|-----|-----|-----|--------|
| Timer_A |                                     | Module input clock |     | 3   |     | μA/MHz |
| Timer_B |                                     | Module input clock |     | 5   |     | μA/MHz |
| eUSCI_A | UART mode                           | Module input clock |     | 5.5 |     | μA/MHz |
| eUSCI_A | SPI mode                            | Module input clock |     | 3.5 |     | μA/MHz |
| eUSCI_B | SPI mode                            | Module input clock |     | 3.5 |     | μA/MHz |
| eUSCI_B | I <sup>2</sup> C mode, 100 kbaud    | Module input clock |     | 3.5 |     | μA/MHz |
| RTC_C   |                                     | 32 kHz             |     | 100 |     | nA     |
| MPY     | Only from start to end of operation | MCLK               |     | 25  |     | μA/MHz |
| AES     | Only from start to end of operation | MCLK               |     | 21  |     | μA/MHz |
| CRC16   | Only from start to end of operation | MCLK               |     | 2.5 |     | μA/MHz |
| CRC32   | Only from start to end of operation | MCLK               |     | 2.5 |     | μA/MHz |

## 5.11 Thermal Resistance Characteristics<sup>(1)</sup>

| PARAMETER                                                                         | PACKAGE        | VALUE <sup>(1)</sup> | UNIT |
|-----------------------------------------------------------------------------------|----------------|----------------------|------|
| $\theta_{JA}$ Junction-to-ambient thermal resistance, still air <sup>(2)</sup>    | TSSOP-56 (DGG) | 57.7                 | °C/W |
| $\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance <sup>(3)</sup>       |                | 15.1                 | °C/W |
| $\theta_{JB}$ Junction-to-board thermal resistance <sup>(4)</sup>                 |                | 26.5                 | °C/W |
| $\Psi_{JB}$ Junction-to-board thermal characterization parameter                  |                | 26.2                 | °C/W |
| $\Psi_{JT}$ Junction-to-top thermal characterization parameter                    |                | 0.5                  | °C/W |
| $\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance <sup>(5)</sup> |                | N/A                  | °C/W |
| $\theta_{JA}$ Junction-to-ambient thermal resistance, still air <sup>(2)</sup>    | QFP-64 (PN)    | 59.3                 | °C/W |
| $\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance <sup>(3)</sup>       |                | 19.5                 | °C/W |
| $\theta_{JB}$ Junction-to-board thermal resistance <sup>(4)</sup>                 |                | 30.8                 | °C/W |
| $\Psi_{JB}$ Junction-to-board thermal characterization parameter                  |                | 30.5                 | °C/W |
| $\Psi_{JT}$ Junction-to-top thermal characterization parameter                    |                | 1.0                  | °C/W |
| $\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance <sup>(5)</sup> |                | N/A                  | °C/W |
| $\theta_{JA}$ Junction-to-ambient thermal resistance, still air <sup>(2)</sup>    | QFN-64 (RGC)   | 29.6                 | °C/W |
| $\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance <sup>(3)</sup>       |                | 15.8                 | °C/W |
| $\theta_{JB}$ Junction-to-board thermal resistance <sup>(4)</sup>                 |                | 8.5                  | °C/W |
| $\Psi_{JB}$ Junction-to-board thermal characterization parameter                  |                | 8.5                  | °C/W |
| $\Psi_{JT}$ Junction-to-top thermal characterization parameter                    |                | 0.2                  | °C/W |
| $\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance <sup>(5)</sup> |                | 1.2                  | °C/W |

(1) N/A = not applicable

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## 5.12 Timing and Switching Characteristics

### 5.12.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

表 5-1 lists the reset power ramp requirements.

**表 5-1. Brownout and Device Reset Power Ramp Requirements**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                      | TEST CONDITIONS                                           | MIN  | MAX  | UNIT |
|----------------------------------------------------------------|-----------------------------------------------------------|------|------|------|
| V <sub>VCC_BOR-</sub> Brownout power-down level <sup>(1)</sup> | dV <sub>CC</sub> /d <sub>t</sub>   < 3 V/s <sup>(2)</sup> | 0.73 | 1.66 | V    |
| V <sub>VCC_BOR+</sub> Brownout power-up level <sup>(1)</sup>   | dV <sub>CC</sub> /d <sub>t</sub>   < 3 V/s <sup>(2)</sup> | 0.79 | 1.68 | V    |

- (1) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/μs). Following the data sheet recommendation for capacitor C<sub>DVCC</sub> should limit the slopes accordingly.
- (2) The brownout levels are measured with a slowly changing supply.

表 5-2 lists the characteristics of the SVS.

**表 5-2. SVS**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                   | TEST CONDITIONS                   | MIN  | TYP  | MAX  | UNIT |
|-----------------------------------------------------------------------------|-----------------------------------|------|------|------|------|
| I <sub>SVSH,LPM</sub> SVS <sub>H</sub> current consumption, low power modes |                                   |      | 170  | 300  | nA   |
| V <sub>SVSH-</sub> SVS <sub>H</sub> power-down level <sup>(1)</sup>         |                                   | 1.75 | 1.80 | 1.85 | V    |
| V <sub>SVSH+</sub> SVS <sub>H</sub> power-up level <sup>(1)</sup>           |                                   | 1.77 | 1.88 | 1.99 | V    |
| V <sub>SVSH_hys</sub> SVS <sub>H</sub> hysteresis                           |                                   | 40   |      | 120  | mV   |
| t <sub>PD,SVSH, AM</sub> SVS <sub>H</sub> propagation delay, active mode    | dV <sub>VCC</sub> /dt = -10 mV/μs |      |      | 10   | μs   |

- (1) For additional information, see the [Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design](#).

### 5.12.2 Reset Timing

Table 5-11 lists the required reset input timing.

**表 5-3. Reset Input**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                  | V <sub>CC</sub> | MIN | MAX | UNIT |
|--------------------------------------------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>(RST)</sub> External reset pulse duration on $\overline{\text{RST}}$ <sup>(1)</sup> | 2.2 V, 3.0 V    | 2   |     | μs   |

- (1) Not applicable if the  $\overline{\text{RST}}$ /NMI pin is configured as NMI.

### 5.12.3 Clock Specifications

Table 5-4 lists the characteristics of the LFXT.

**Table 5-4. Low-Frequency Crystal Oscillator, LFXT<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              | TEST CONDITIONS                                                                                                                      | V <sub>CC</sub> | MIN     | TYP    | MAX | UNIT |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------|--------|-----|------|
| I <sub>VCC,LFXT</sub>  | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {0},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 3.7 pF, ESR ≈ 44 kΩ  | 3.0 V           | 180     |        |     | nA   |
|                        | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {1},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 6 pF, ESR ≈ 40 kΩ    |                 | 185     |        |     |      |
|                        | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {2},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 9 pF, ESR ≈ 40 kΩ    |                 | 225     |        |     |      |
|                        | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {3},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12.5 pF, ESR ≈ 40 kΩ |                 | 330     |        |     |      |
| f <sub>LFXT</sub>      | LFXT oscillator crystal frequency                                                                                                    |                 | 32768   |        |     | Hz   |
| DC <sub>LFXT</sub>     | LFXT oscillator duty cycle                                                                                                           |                 | 30% 70% |        |     |      |
| f <sub>LFXT,SW</sub>   | LFXT oscillator logic-level square-wave input frequency                                                                              |                 | 10.5    | 32.768 | 50  | kHz  |
| DC <sub>LFXT, SW</sub> | LFXT oscillator logic-level square-wave input duty cycle                                                                             |                 | 30% 70% |        |     |      |
| OA <sub>LFXT</sub>     | LFXTBYPASS = 0, LFXTDRIVE = {1},<br>f <sub>LFXT</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF                                          |                 | 210     |        |     | kΩ   |
|                        | LFXTBYPASS = 0, LFXTDRIVE = {3},<br>f <sub>LFXT</sub> = 32768 Hz, C <sub>L,eff</sub> = 12.5 pF                                       |                 | 300     |        |     |      |
| C <sub>LFXIN</sub>     | Integrated load capacitance at LFXIN terminal <sup>(5) (6)</sup>                                                                     |                 | 2       |        |     | pF   |
| C <sub>LFXOUT</sub>    | Integrated load capacitance at LFXOUT terminal <sup>(5) (6)</sup>                                                                    |                 | 2       |        |     | pF   |

- (1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
  - Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by DC<sub>LFXT, SW</sub>.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  - For LFXTDRIVE = {0}, C<sub>L,eff</sub> = 3.7 pF
  - For LFXTDRIVE = {1}, C<sub>L,eff</sub> = 6 pF
  - For LFXTDRIVE = {2}, 6 pF ≤ C<sub>L,eff</sub> ≤ 9 pF
  - For LFXTDRIVE = {3}, 9 pF ≤ C<sub>L,eff</sub> ≤ 12.5 pF
- (5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C<sub>L,eff</sub> can be computed as C<sub>IN</sub> × C<sub>OUT</sub> / (C<sub>IN</sub> + C<sub>OUT</sub>), where C<sub>IN</sub> and C<sub>OUT</sub> is the total capacitance at the LFXIN and LFXOUT terminals, respectively.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

**Table 5-4. Low-Frequency Crystal Oscillator, LFXT<sup>(1)</sup> (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                             | TEST CONDITIONS                                                                                                        | V <sub>CC</sub> | MIN | TYP  | MAX  | UNIT |
|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|------|------|
| t <sub>START,LFXT</sub> Start-up time <sup>(7)</sup>                  | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {0},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 3.7 pF | 3.0 V           |     | 800  |      | ms   |
|                                                                       | f <sub>OSC</sub> = 32768 Hz<br>LFXTBYPASS = 0, LFXTDRIVE = {3},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12.5 pF | 3.0 V           |     | 1000 |      |      |
| f <sub>Fault,LFXT</sub> Oscillator fault frequency <sup>(8) (9)</sup> |                                                                                                                        |                 | 0   |      | 3500 | Hz   |

(7) Includes start-up counter of 1024 clock cycles.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the HFXT.

**Table 5-5. High-Frequency Crystal Oscillator, HFXT<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                     | TEST CONDITIONS                                                                                                                                                                     | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-----|-----|------|
| I <sub>DVCC,HFXT</sub> HFXT oscillator crystal current HF mode at typical ESR | f <sub>OSC</sub> = 4 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 0,<br>HFFREQ = 1 <sup>(2)</sup> ,<br>T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub> | 3.0 V           |       | 75  |     | μA   |
|                                                                               | f <sub>OSC</sub> = 8 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 1,<br>HFFREQ = 1<br>T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                  |                 |       | 120 |     |      |
|                                                                               | f <sub>OSC</sub> = 16 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 2,<br>HFFREQ = 2,<br>T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                |                 |       | 190 |     |      |
|                                                                               | f <sub>OSC</sub> = 24 MHz<br>HFXTBYPASS = 0, HFXTDRIVE = 3,<br>HFFREQ = 3,<br>T <sub>A</sub> = 25°C,<br>C <sub>L,eff</sub> = 18 pF, typical ESR, C <sub>shunt</sub>                 |                 |       | 250 |     |      |
| f <sub>HFXT</sub> HFXT oscillator crystal frequency, crystal mode             | HFXTBYPASS = 0, HFFREQ = 1 <sup>(2) (3)</sup>                                                                                                                                       |                 | 4     |     | 8   | MHz  |
|                                                                               | HFXTBYPASS = 0, HFFREQ = 2 <sup>(3)</sup>                                                                                                                                           |                 | 8.01  |     | 16  |      |
|                                                                               | HFXTBYPASS = 0, HFFREQ = 3 <sup>(3)</sup>                                                                                                                                           |                 | 16.01 |     | 24  |      |
| DC <sub>HFXT</sub> HFXT oscillator duty cycle                                 | Measured at SMCLK,<br>f <sub>HFXT</sub> = 16 MHz                                                                                                                                    |                 | 40%   | 50% | 60% |      |

(1) To improve EMI on the HFXT oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

**Table 5-5. High-Frequency Crystal Oscillator, HFXT<sup>(1)</sup> (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                    | TEST CONDITIONS                                                                                                                  | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-----|-----|------|
| f <sub>HFXT,SW</sub><br>HFXT oscillator logic-level square-wave input frequency, bypass mode | HFXTBYPASS = 1, HFFREQ = 0 <sup>(4)</sup><br>(3)                                                                                 |                 | 0.9   |     | 4   | MHz  |
|                                                                                              | HFXTBYPASS = 1, HFFREQ = 1 <sup>(4)</sup><br>(3)                                                                                 |                 | 4.01  |     | 8   |      |
|                                                                                              | HFXTBYPASS = 1, HFFREQ = 2 <sup>(4)</sup><br>(3)                                                                                 |                 | 8.01  |     | 16  |      |
|                                                                                              | HFXTBYPASS = 1, HFFREQ = 3 <sup>(4)</sup><br>(3)                                                                                 |                 | 16.01 |     | 24  |      |
| DC <sub>HFXT,SW</sub><br>HFXT oscillator logic-level square-wave input duty cycle            | HFXTBYPASS = 1                                                                                                                   |                 | 40%   |     | 60% |      |
| OA <sub>HFXT</sub><br>Oscillation allowance for HFXT crystals <sup>(5)</sup>                 | HFXTBYPASS = 0,<br>HFXTDRIVE = 0, HFFREQ = 1 <sup>(2)</sup> ,<br>f <sub>HFXT,HF</sub> = 4 MHz, C <sub>L,eff</sub> = 16 pF        |                 |       | 450 |     | Ω    |
|                                                                                              | HFXTBYPASS = 0,<br>HFXTDRIVE = 1, HFFREQ = 1,<br>f <sub>HFXT,HF</sub> = 8 MHz, C <sub>L,eff</sub> = 16 pF                        |                 |       | 320 |     |      |
|                                                                                              | HFXTBYPASS = 0,<br>HFXTDRIVE = 2, HFFREQ = 2,<br>f <sub>HFXT,HF</sub> = 16 MHz, C <sub>L,eff</sub> = 16 pF                       |                 |       | 200 |     |      |
|                                                                                              | HFXTBYPASS = 0,<br>HFXTDRIVE = 3, HFFREQ = 3,<br>f <sub>HFXT,HF</sub> = 24 MHz, C <sub>L,eff</sub> = 16 pF                       |                 |       | 200 |     |      |
| t <sub>START,HFXT</sub> Start-up time <sup>(6)</sup>                                         | f <sub>OSC</sub> = 4 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 0,<br>HFFREQ = 1,<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 16 pF  | 3.0 V           |       | 1.6 |     | ms   |
|                                                                                              | f <sub>OSC</sub> = 24 MHz,<br>HFXTBYPASS = 0, HFXTDRIVE = 3,<br>HFFREQ = 3,<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 16 pF | 3.0 V           |       | 0.6 |     |      |
| C <sub>HFXIN</sub><br>Integrated load capacitance at HFXIN terminal <sup>(7) (8)</sup>       |                                                                                                                                  |                 |       | 2   |     | pF   |
| C <sub>HFXOUT</sub><br>Integrated load capacitance at HFXOUT terminal <sup>(7) (8)</sup>     |                                                                                                                                  |                 |       | 2   |     | pF   |
| f <sub>Fault,HFXT</sub><br>Oscillator fault frequency <sup>(9) (10)</sup>                    |                                                                                                                                  |                 | 0     |     | 800 | kHz  |

(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by DC<sub>HFXT, SW</sub>.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes start-up counter of 1024 clock cycles.

(7) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C<sub>L,eff</sub> can be computed as C<sub>IN</sub> × C<sub>OUT</sub> / (C<sub>IN</sub> + C<sub>OUT</sub>), where C<sub>IN</sub> and C<sub>OUT</sub> is the total capacitance at the HFXIN and HFXOUT terminals, respectively.

(8) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.

(10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-6 lists the characteristics of the DCO.

**Table 5-6. DCO**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                |                                      | TEST CONDITIONS                                                                                                                                                           | V <sub>CC</sub> | MIN | TYP   | MAX                  | UNIT |
|--------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-------|----------------------|------|
| f <sub>DCO1</sub>        | DCO frequency range 1 MHz, trimmed   | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0<br>DCORSEL = 1, DCOFSEL = 0                                                                                      |                 |     | 1     | ±3.5%                | MHz  |
| f <sub>DCO2.7</sub>      | DCO frequency range 2.7 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1                                                                                                                  |                 |     | 2.667 | ±3.5%                | MHz  |
| f <sub>DCO3.5</sub>      | DCO frequency range 3.5 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2                                                                                                                  |                 |     | 3.5   | ±3.5%                | MHz  |
| f <sub>DCO4</sub>        | DCO frequency range 4 MHz, trimmed   | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3                                                                                                                  |                 |     | 4     | ±3.5%                | MHz  |
| f <sub>DCO5.3</sub>      | DCO frequency range 5.3 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4<br>DCORSEL = 1, DCOFSEL = 1                                                                                      |                 |     | 5.333 | ±3.5%                | MHz  |
| f <sub>DCO7</sub>        | DCO frequency range 7 MHz, trimmed   | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5<br>DCORSEL = 1, DCOFSEL = 2                                                                                      |                 |     | 7     | ±3.5%                | MHz  |
| f <sub>DCO8</sub>        | DCO frequency range 8 MHz, trimmed   | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6<br>DCORSEL = 1, DCOFSEL = 3                                                                                      |                 |     | 8     | ±3.5%                | MHz  |
| f <sub>DCO16</sub>       | DCO frequency range 16 MHz, trimmed  | Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4                                                                                                                  |                 |     | 16    | ±3.5% <sup>(1)</sup> | MHz  |
| f <sub>DCO21</sub>       | DCO frequency range 21 MHz, trimmed  | Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5                                                                                                                  |                 |     | 21    | ±3.5% <sup>(1)</sup> | MHz  |
| f <sub>DCO24</sub>       | DCO frequency range 24 MHz, trimmed  | Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6                                                                                                                  |                 |     | 24    | ±3.5% <sup>(1)</sup> | MHz  |
| f <sub>DCO,DC</sub>      | Duty cycle                           | Measured at SMCLK, divide by 1, No external divide, all DCORSEL and DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6                         |                 | 48% | 50%   | 52%                  |      |
| t <sub>DCO, JITTER</sub> | DCO jitter                           | Based on f <sub>signal</sub> = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74-dB SNR due to jitter; that is, it is limited by ADC performance. |                 |     | 2     | 3                    | ns   |
| df <sub>DCO</sub> /dT    | DCO temperature drift <sup>(2)</sup> |                                                                                                                                                                           | 3.0 V           |     | 0.01  |                      | %/°C |

(1) After a wakeup from LPM1, LPM2, LPM3 or LPM4, the DCO frequency f<sub>DCO</sub> might exceed the specified frequency range for a few clocks cycles by up to 5% before settling into the specified steady state frequency range.

(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

Table 5-7 lists the characteristics of the VLO.

**Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| I <sub>VLO</sub>                    | Current consumption                |                                 |                 |     | 100 |     | nA   |
| f <sub>VLO</sub>                    | VLO frequency                      | Measured at ACLK                |                 | 6   | 9.4 | 14  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at ACLK <sup>(1)</sup> |                 |     | 0.2 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> |                 |     | 0.7 |     | %/V  |
| f <sub>VLO,DC</sub>                 | Duty cycle                         | Measured at ACLK                |                 | 40% | 50% | 60% |      |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

**Table 5-8. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                      | TEST CONDITIONS                | MIN | TYP  | MAX | UNIT    |
|----------------------|------------------------------------------------------|--------------------------------|-----|------|-----|---------|
| $I_{MODOSC}$         | Current consumption                                  | Enabled                        |     | 25   |     | $\mu A$ |
| $f_{MODOSC}$         | MODOSC frequency                                     |                                | 4.0 | 4.8  | 5.4 | MHz     |
| $f_{MODOSC}/dT$      | MODOSC frequency temperature drift <sup>(1)</sup>    |                                |     | 0.08 |     | %/°C    |
| $f_{MODOSC}/dV_{CC}$ | MODOSC frequency supply voltage drift <sup>(2)</sup> |                                |     | 1.4  |     | %/V     |
| $DC_{MODOSC}$        | Duty cycle                                           | Measured at SMCLK, divide by 1 | 40% | 50%  | 60% |         |

(1) Calculated using the box method:  $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$

(2) Calculated using the box method:  $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

## 5.12.4 Wake-up Characteristics

Table 5-9 lists the device wake-up times.

**Table 5-9. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS                                                                                                                                     | V <sub>CC</sub>                 | MIN          | TYP                             | MAX | UNIT |
|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|--------------|---------------------------------|-----|------|
| t <sub>WAKE-UP FRAM</sub>   | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected |                                 |              | 6                               | 10  | μs   |
| t <sub>WAKE-UP LPM0</sub>   | Wake-up time from LPM0 to active mode                                                                                                               | MCLKREQEN = 1 <sup>(1)</sup>    | 2.2 V, 3.0 V | 400 ns + 1.5 / f <sub>DCO</sub> |     |      |
|                             |                                                                                                                                                     | MCLKREQEN = 0 <sup>(1)(2)</sup> | 2.2 V, 3.0 V | 400 ns + 2.5 / f <sub>DCO</sub> |     |      |
| t <sub>WAKE-UP LPM1</sub>   | Wake-up time from LPM1 to active mode <sup>(1)</sup>                                                                                                | 2.2 V, 3.0 V                    |              | 6                               |     | μs   |
| t <sub>WAKE-UP LPM2</sub>   | Wake-up time from LPM2 to active mode <sup>(1)</sup>                                                                                                | 2.2 V, 3.0 V                    |              | 6                               |     | μs   |
| t <sub>WAKE-UP LPM3</sub>   | Wake-up time from LPM3 to active mode <sup>(1)</sup>                                                                                                | 2.2 V, 3.0 V                    |              | 7                               | 10  | μs   |
| t <sub>WAKE-UP LPM4</sub>   | Wake-up time from LPM4 to active mode <sup>(1)</sup>                                                                                                | 2.2 V, 3.0 V                    |              | 7                               | 10  | μs   |
| t <sub>WAKE-UP LPM3.5</sub> | Wake-up time from LPM3.5 to active mode <sup>(3)</sup>                                                                                              | 2.2 V, 3.0 V                    |              | 250                             | 350 | μs   |
| t <sub>WAKE-UP LPM4.5</sub> | Wake-up time from LPM4.5 to active mode <sup>(3)</sup>                                                                                              | SVSHE = 1                       | 2.2 V, 3.0 V | 250                             | 350 | μs   |
|                             |                                                                                                                                                     | SVSHE = 0                       | 2.2 V, 3.0 V | 0.4                             | 0.8 | ms   |
| t <sub>WAKE-UP-RST</sub>    | Wake-up time from a $\overline{\text{RST}}$ pin triggered reset to active mode <sup>(3)</sup>                                                       | 2.2 V, 3.0 V                    |              | 250                             | 350 | μs   |
| t <sub>WAKE-UP-BOR</sub>    | Wake-up time from power-up to active mode <sup>(3)</sup>                                                                                            | 2.2 V, 3.0 V                    |              | 0.5                             | 1.0 | ms   |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge with MCLKREQEN = 1. This time includes the activation of the FRAM during wakeup.
- (2) With MCLKREQEN = 0, the MCLK is gated one additional one clock cycle (wake from LPM0, LPM1, LPM2, LPM3, and LPM4). The device wake-up time is not affected by the status of the MCLKREQEN bit.
- (3) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

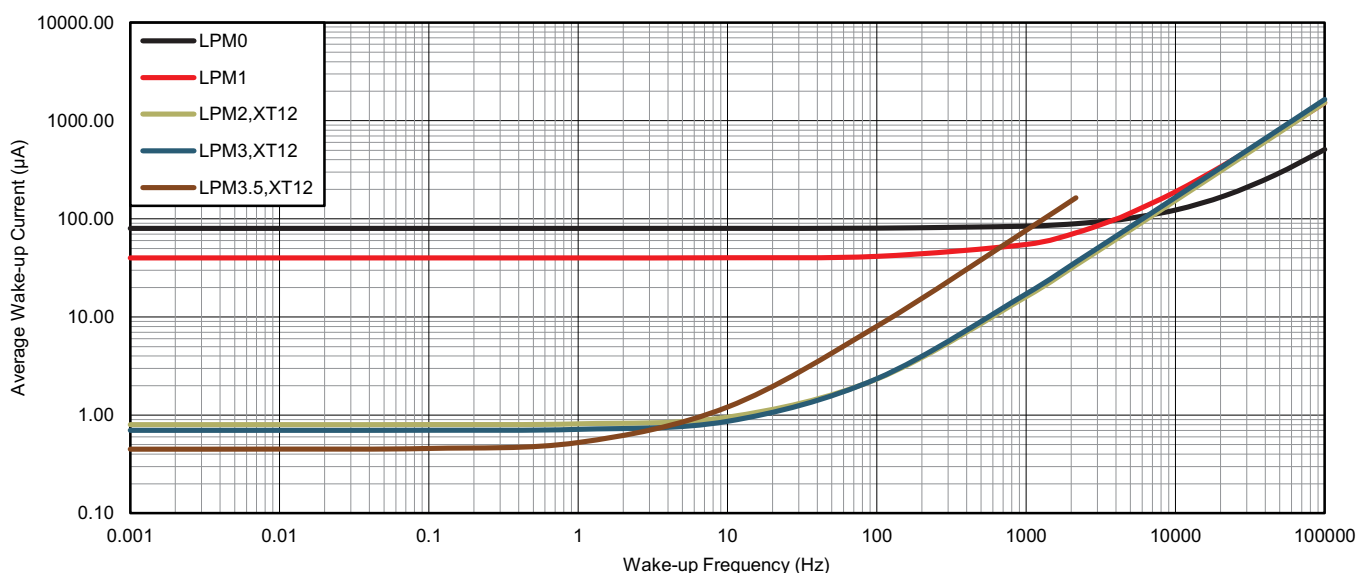
Table 5-10 lists the typical charge required for wakeup.

**Table 5-10. Typical Wake-up Charge<sup>(1)</sup>**

| PARAMETER                   | TEST CONDITIONS                                                                                                     | MIN       | TYP  | MAX | UNIT |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------|-----------|------|-----|------|
| Q <sub>WAKE-UP FRAM</sub>   | Charge used for activating the FRAM in AM or during wakeup from LPM0 if previously disabled by the FRAM controller. |           | 15.1 |     | nAs  |
| Q <sub>WAKE-UP LPM0</sub>   | Charge used to wake up from LPM0 to active mode (with FRAM active)                                                  |           | 4.4  |     | nAs  |
| Q <sub>WAKE-UP LPM1</sub>   | Charge used to wake up from LPM1 to active mode (with FRAM active)                                                  |           | 15.1 |     | nAs  |
| Q <sub>WAKE-UP LPM2</sub>   | Charge used to wake up from LPM2 to active mode (with FRAM active)                                                  |           | 15.3 |     | nAs  |
| Q <sub>WAKE-UP LPM3</sub>   | Charge used to wake up from LPM3 to active mode (with FRAM active)                                                  |           | 16.5 |     | nAs  |
| Q <sub>WAKE-UP LPM4</sub>   | Charge used to wake up from LPM4 to active mode (with FRAM active)                                                  |           | 16.5 |     | nAs  |
| Q <sub>WAKE-UP LPM3.5</sub> | Charge used to wake up from LPM3.5 to active mode <sup>(2)</sup>                                                    |           | 76   |     | nAs  |
| Q <sub>WAKE-UP LPM4.5</sub> | Charge used to wake up from LPM4.5 to active mode <sup>(2)</sup>                                                    | SVSHE = 1 | 77   |     | nAs  |
|                             |                                                                                                                     | SVSHE = 0 | 77.5 |     |      |
| Q <sub>WAKE-UP-RESET</sub>  | Charge used for reset from $\overline{\text{RST}}$ or BOR event to active mode <sup>(2)</sup>                       |           | 75   |     | nAs  |

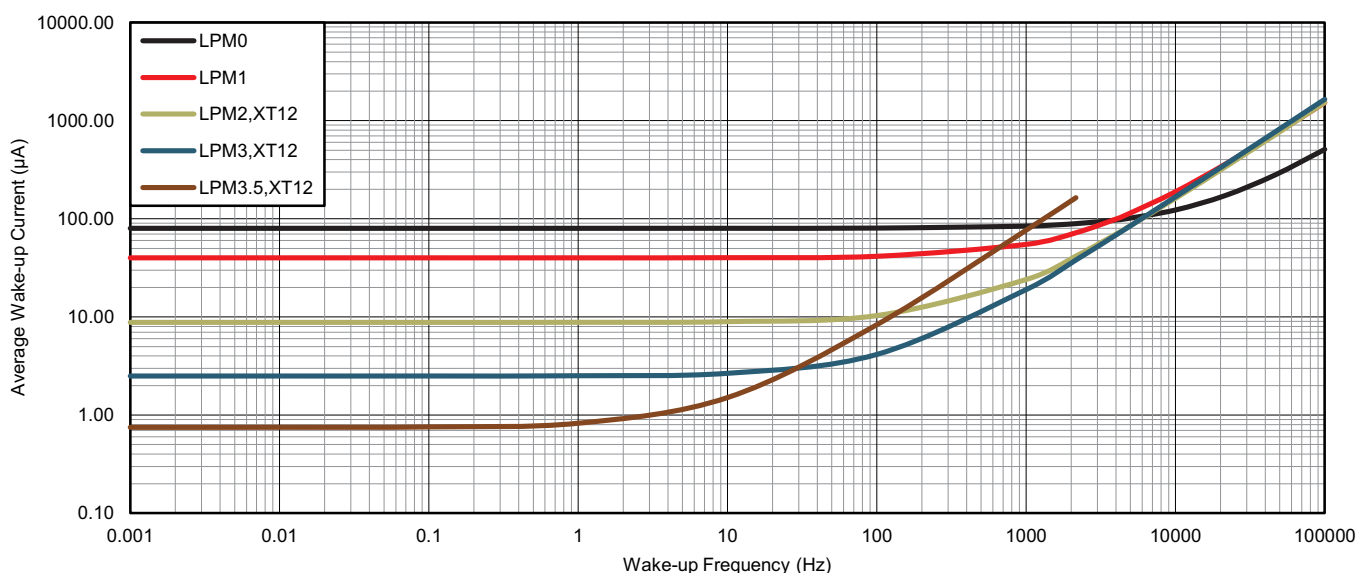
- (1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).
- (2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

#### 5.12.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-6. Average LPM Currents vs Wake-up Frequency at 25°C



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-7. Average LPM Currents vs Wake-up Frequency at 85°C

## 5.12.5 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

**Table 5-11. Digital Inputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                                  | TEST CONDITIONS                                                                                  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|------------------------|--------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub>       | Positive-going input threshold voltage                                                           |                                                                                                  | 2.2 V           | 1.2  |     | 1.65 | V    |
|                        |                                                                                                  |                                                                                                  | 3.0 V           | 1.65 |     | 2.25 |      |
| V <sub>IT–</sub>       | Negative-going input threshold voltage                                                           |                                                                                                  | 2.2 V           | 0.55 |     | 1.00 | V    |
|                        |                                                                                                  |                                                                                                  | 3.0 V           | 0.75 |     | 1.35 |      |
| V <sub>hys</sub>       | Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )                                  |                                                                                                  | 2.2 V           | 0.44 |     | 0.98 | V    |
|                        |                                                                                                  |                                                                                                  | 3.0 V           | 0.60 |     | 1.30 |      |
| R <sub>Pull</sub>      | Pullup or pulldown resistor                                                                      | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I,dig</sub>     | Input capacitance, digital only port pins                                                        | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                             |                 |      | 3   |      | pF   |
| C <sub>I,ana</sub>     | Input capacitance, port pins with shared analog functions <sup>(1)</sup>                         | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                             |                 |      | 5   |      | pF   |
| I <sub>Ikg(Px.y)</sub> | High-impedance input leakage current                                                             | See <sup>(2)(3)</sup>                                                                            | 2.2 V,<br>3.0 V | –20  |     | +20  | nA   |
| t <sub>(int)</sub>     | External interrupt timing (external trigger pulse duration to set interrupt flag) <sup>(4)</sup> | Ports with interrupt capability (see block diagram and terminal function descriptions).          | 2.2 V,<br>3.0 V | 20   |     |      | ns   |
| t <sub>(RST)</sub>     | External reset pulse duration on $\overline{\text{RST}}$ <sup>(5)</sup>                          |                                                                                                  | 2.2 V,<br>3.0 V | 2    |     |      | μs   |

- (1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and PJ.5/LFXOUT.
- (2) The input leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pins, unless otherwise noted.
- (3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
- (4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.
- (5) Not applicable if the  $\overline{\text{RST}}$ /NMI pin is configured as NMI.

Table 5-12 lists the characteristics of the digital outputs.

**Table 5-12. Digital Outputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                           | TEST CONDITIONS                                                                         | V <sub>CC</sub> | MIN                    | TYP | MAX                    | UNIT |
|-------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----------------|------------------------|-----|------------------------|------|
| V <sub>OH</sub> High-level output voltage                                           | I <sub>(OHmax)</sub> = –1 mA <sup>(1)</sup>                                             | 2.2 V           | V <sub>CC</sub> – 0.25 |     | V <sub>CC</sub>        | V    |
|                                                                                     | I <sub>(OHmax)</sub> = –3 mA <sup>(2)</sup>                                             |                 | V <sub>CC</sub> – 0.60 |     | V <sub>CC</sub>        |      |
|                                                                                     | I <sub>(OHmax)</sub> = –2 mA <sup>(1)</sup>                                             | 3.0 V           | V <sub>CC</sub> – 0.25 |     | V <sub>CC</sub>        |      |
|                                                                                     | I <sub>(OHmax)</sub> = –6 mA <sup>(2)</sup>                                             |                 | V <sub>CC</sub> – 0.60 |     | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage                                            | I <sub>(OLmax)</sub> = 1 mA <sup>(1)</sup>                                              | 2.2 V           | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.25 | V    |
|                                                                                     | I <sub>(OLmax)</sub> = 3 mA <sup>(2)</sup>                                              |                 | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.60 |      |
|                                                                                     | I <sub>(OLmax)</sub> = 2 mA <sup>(1)</sup>                                              | 3.0 V           | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.25 |      |
|                                                                                     | I <sub>(OLmax)</sub> = 6 mA <sup>(2)</sup>                                              |                 | V <sub>SS</sub>        |     | V <sub>SS</sub> + 0.60 |      |
| f <sub>Px,y</sub> Port output frequency (with load) <sup>(3)</sup>                  | C <sub>L</sub> = 20 pF, R <sub>L</sub> <sup>(4)</sup> <sup>(5)</sup>                    | 2.2 V           | 16                     |     |                        | MHz  |
|                                                                                     |                                                                                         | 3.0 V           | 16                     |     |                        |      |
| f <sub>Port_CLK</sub> Clock output frequency <sup>(3)</sup>                         | ACLK, MCLK, or SMCLK at configured output port<br>C <sub>L</sub> = 20 pF <sup>(5)</sup> | 2.2 V           | 16                     |     |                        | MHz  |
|                                                                                     |                                                                                         | 3.0 V           | 16                     |     |                        |      |
| t <sub>rise,dig</sub> Port output rise time, digital only port pins                 | C <sub>L</sub> = 20 pF                                                                  | 2.2 V           |                        | 4   | 15                     | ns   |
|                                                                                     |                                                                                         | 3.0 V           |                        | 3   | 15                     |      |
| t <sub>fall,dig</sub> Port output fall time, digital only port pins                 | C <sub>L</sub> = 20 pF                                                                  | 2.2 V           |                        | 4   | 15                     | ns   |
|                                                                                     |                                                                                         | 3.0 V           |                        | 3   | 15                     |      |
| t <sub>rise,ana</sub> Port output rise time, port pins with shared analog functions | C <sub>L</sub> = 20 pF                                                                  | 2.2 V           |                        | 6   | 15                     | ns   |
|                                                                                     |                                                                                         | 3.0 V           |                        | 4   | 15                     |      |
| t <sub>fall,ana</sub> Port output fall time, port pins with shared analog functions | C <sub>L</sub> = 20 pF                                                                  | 2.2 V           |                        | 6   | 15                     | ns   |
|                                                                                     |                                                                                         | 3.0 V           |                        | 4   | 15                     |      |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
- (3) The port can output frequencies at least up to the specified limit. It might support higher frequencies.
- (4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider. C<sub>L</sub> = 20 pF is connected from the output to V<sub>SS</sub>.
- (5) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

### 5.12.5.1 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V

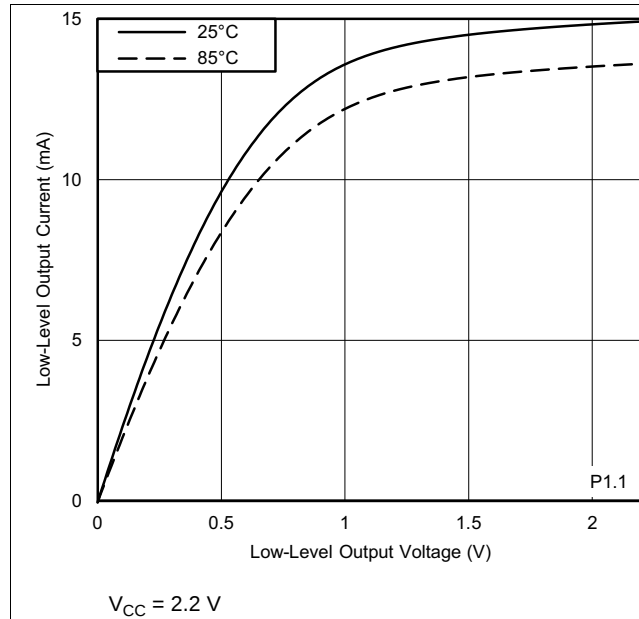


Figure 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

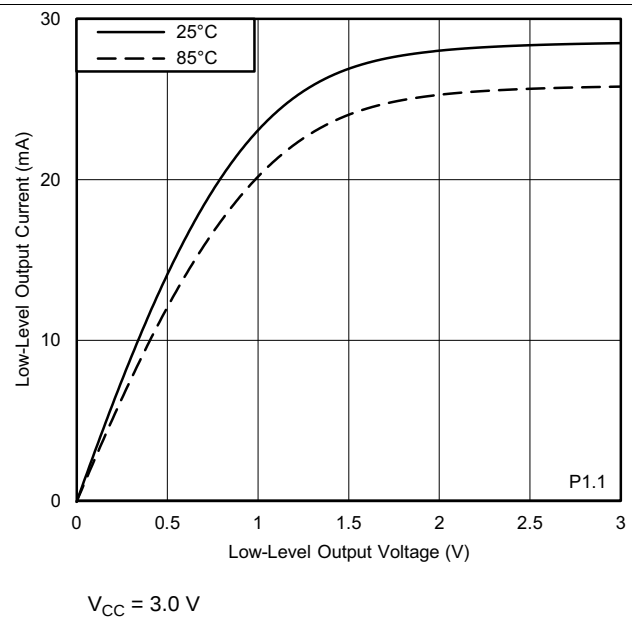


Figure 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage

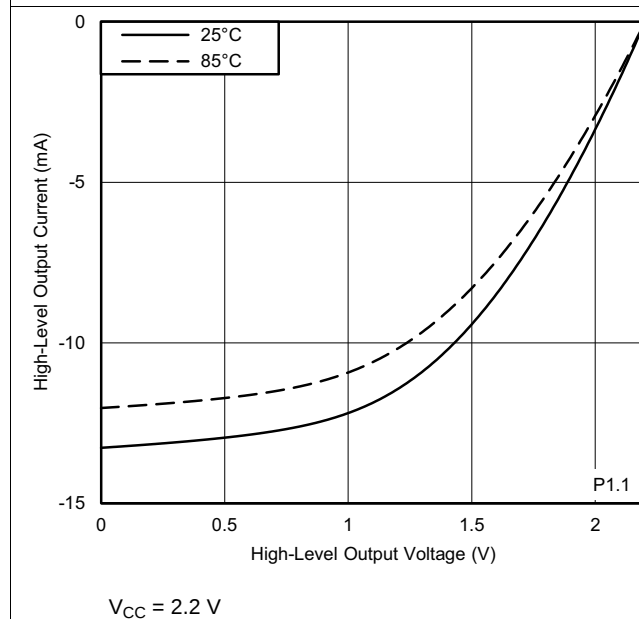


Figure 5-10. Typical High-Level Output Current vs High-Level Output Voltage

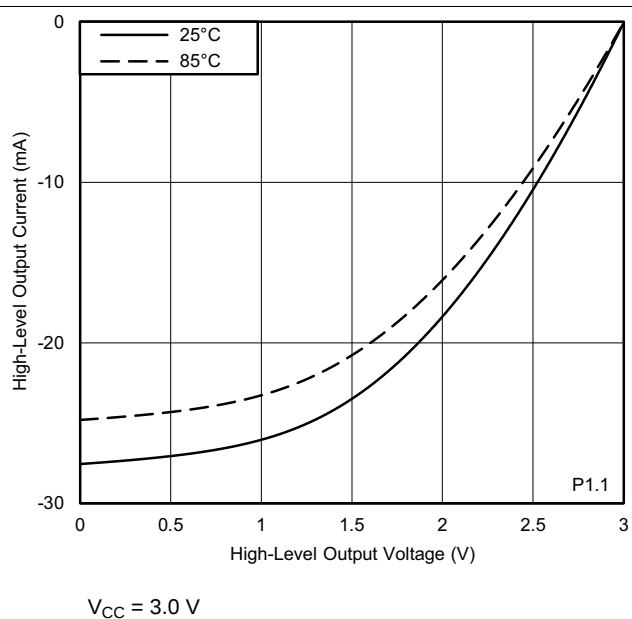


Figure 5-11. Typical High-Level Output Current vs High-Level Output Voltage

Table 5-13 lists the characteristics of the pin oscillator.

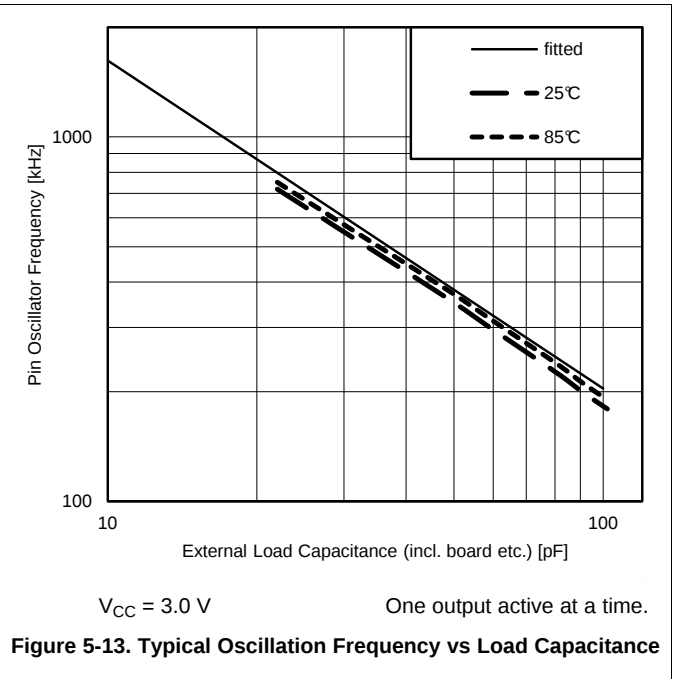
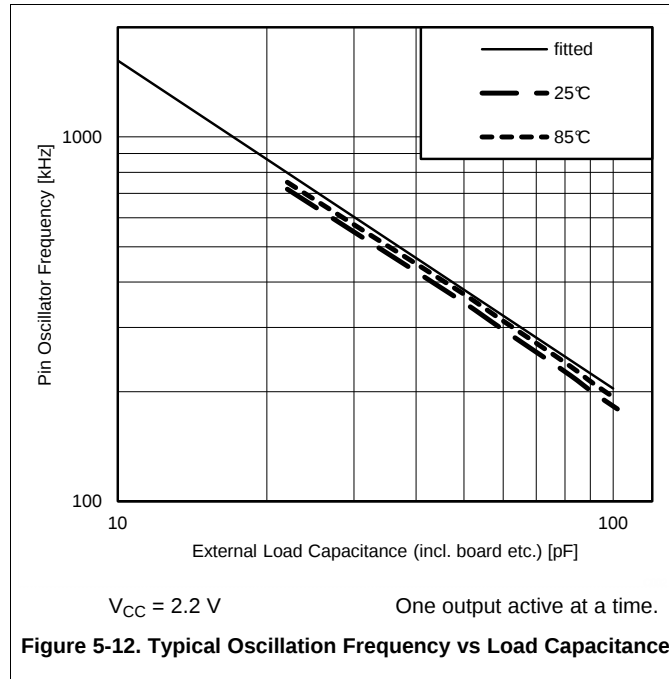
**Table 5-13. Pin-Oscillator Frequency, Ports Px**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                   | TEST CONDITIONS                             | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|---------------------------------------------|---------------------------------------------|-----------------|-----|------|-----|------|
| f <sub>OPx,y</sub> Pin-oscillator frequency | Px.y, C <sub>L</sub> = 10 pF <sup>(1)</sup> | 3.0 V           |     | 1200 |     | kHz  |
|                                             | Px.y, C <sub>L</sub> = 20 pF <sup>(1)</sup> | 3.0 V           |     | 650  |     | kHz  |

(1) C<sub>L</sub> is the external load capacitance connected from the output to V<sub>SS</sub> and includes all parasitic effects such as PCB traces.

### 5.12.5.2 Typical Characteristics, Pin-Oscillator Frequency



### 5.12.6 Timer\_A and Timer\_B

Table 5-14 lists the characteristics of the Timer\_A.

**Table 5-14. Timer\_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS                                                       | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------------------------------|-----------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| f <sub>TA</sub> Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 2.2 V,<br>3.0 V |     |     | 16  | MHz  |
| t <sub>TA,cap</sub> Timer_A capture timing    | All capture inputs, minimum pulse duration required for capture       | 2.2 V,<br>3.0 V | 20  |     |     | ns   |

Table 5-15 lists the characteristics of the Timer\_B.

**Table 5-15. Timer\_B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS                                                       | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------------------------------|-----------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| f <sub>TB</sub> Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | 2.2 V,<br>3.0 V |     |     | 16  | MHz  |
| t <sub>TB,cap</sub> Timer_B capture timing    | All capture inputs, minimum pulse duration required for capture       | 2.2 V,<br>3.0 V | 20  |     |     | ns   |

### 5.12.7 eUSCI

Table 5-16 lists the supported clock frequencies for the eUSCI in UART mode.

**Table 5-16. eUSCI (UART Mode) Clock Frequency**

| PARAMETER                                                              | CONDITIONS                                                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|------------------------------------------------------------------------|------------------------------------------------------------------|-----------------|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency                         | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% |                 |     | 16  | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals baud rate in MBaud) |                                                                  |                 |     | 4   | MHz  |

Table 5-17 lists the characteristics of the eUSCI in UART mode.

**Table 5-17. eUSCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------|-----------------|-----------------|-----|-----|-----|------|
| t <sub>t</sub> UART receive deglitch time <sup>(1)</sup> | UCGLITx = 0     | 2.2 V,<br>3.0 V | 5   |     | 30  | ns   |
|                                                          | UCGLITx = 1     |                 | 20  |     | 90  |      |
|                                                          | UCGLITx = 2     |                 | 35  |     | 160 |      |
|                                                          | UCGLITx = 3     |                 | 50  |     | 220 |      |

- (1) Pulses on the UART receive input (UCxRX) that are shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum usable baud rate. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequencies for the eUSCI in SPI master mode.

**Table 5-18. eUSCI (SPI Master Mode) Clock Frequency**

| PARAMETER                                      | CONDITIONS                                     | V <sub>CC</sub> | MIN | MAX | UNIT |
|------------------------------------------------|------------------------------------------------|-----------------|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency | Internal: SMCLK, ACLK<br>Duty cycle = 50% ±10% |                 |     | 16  | MHz  |

Table 5-19 lists the characteristics of the eUSCI in SPI master mode.

**Table 5-19. eUSCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                  | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX | UNIT          |
|----------------------------------------------------------------------------|----------------------------------------------------|-----------------|-----|-----|-----|---------------|
| t <sub>STE,LEAD</sub> STE lead time, STE active to clock                   | UCSTEM = 1, UCMODEx = 01 or 10                     |                 | 1   |     |     | UCxCLK cycles |
| t <sub>STE,LAG</sub> STE lag time, last clock to STE inactive              | UCSTEM = 1, UCMODEx = 01 or 10                     |                 | 1   |     |     |               |
| t <sub>STE,ACC</sub> STE access time, STE active to SIMO data out          | UCSTEM = 0, UCMODEx = 01 or 10                     | 2.2 V,<br>3.0 V |     |     | 60  | ns            |
| t <sub>STE,DIS</sub> STE disable time, STE inactive to SOMI high impedance | UCSTEM = 0, UCMODEx = 01 or 10                     | 2.2 V,<br>3.0 V |     |     | 80  | ns            |
| t <sub>SU,MI</sub> SOMI input data setup time                              |                                                    | 2.2 V           | 40  |     |     | ns            |
|                                                                            |                                                    | 3.0 V           | 40  |     |     |               |
| t <sub>HD,MI</sub> SOMI input data hold time                               |                                                    | 2.2 V           | 0   |     |     | ns            |
|                                                                            |                                                    | 3.0 V           | 0   |     |     |               |
| t <sub>VALID,MO</sub> SIMO output data valid time <sup>(2)</sup>           | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |     |     | 10  | ns            |
|                                                                            |                                                    | 3.0 V           |     |     | 10  |               |
| t <sub>HD,MO</sub> SIMO output data hold time <sup>(3)</sup>               | C <sub>L</sub> = 20 pF                             | 2.2 V           |     | 0   |     | ns            |
|                                                                            |                                                    | 3.0 V           |     | 0   |     |               |

- (1)  $f_{UCxCLK} = 1 / 2t_{LO/HI}$  with  $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$ . For the slave parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-14 and Figure 5-15.
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-14 and Figure 5-15.

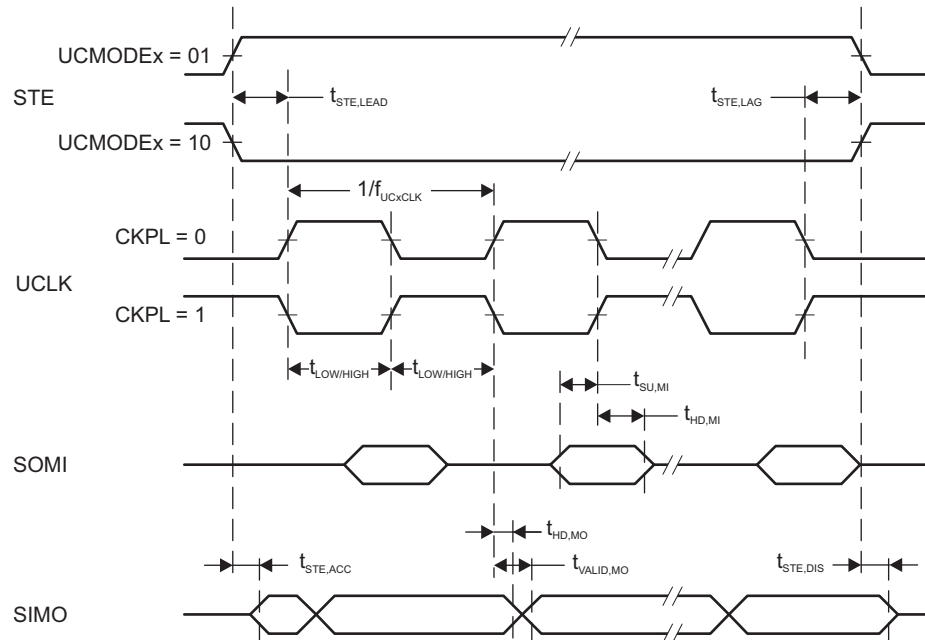


Figure 5-14. SPI Master Mode, CKPH = 0

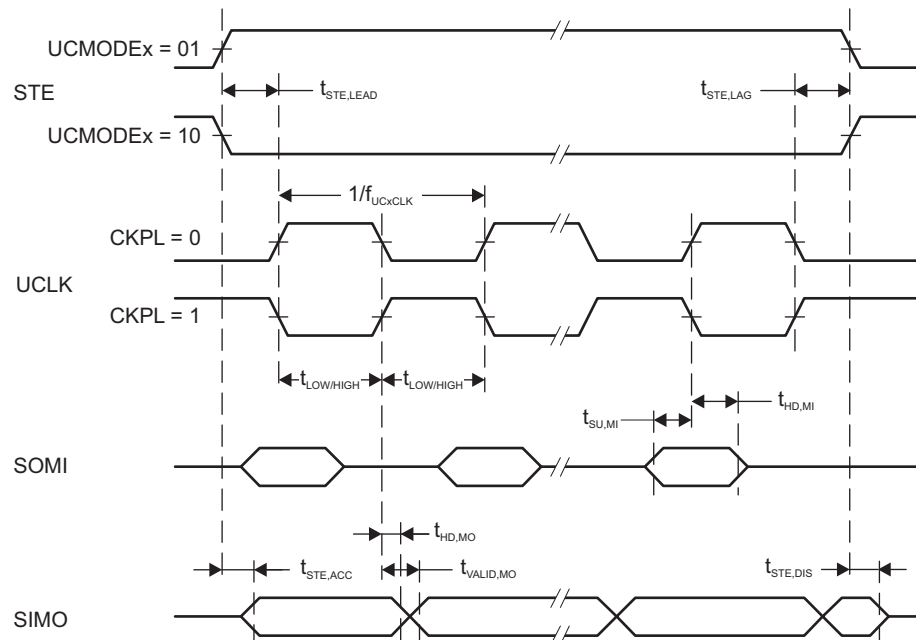


Figure 5-15. SPI Master Mode, CKPH = 1

Table 5-20 lists the characteristics of the eUSCI in SPI slave mode.

**Table 5-20. eUSCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                  | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------|----------------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> STE lead time, STE active to clock                   |                                                    | 2.2 V           | 50  |     |     | ns   |
|                                                                            |                                                    | 3.0 V           | 40  |     |     |      |
| t <sub>STE,LAG</sub> STE lag time, last clock to STE inactive              |                                                    | 2.2 V           | 2   |     |     | ns   |
|                                                                            |                                                    | 3.0 V           | 3   |     |     |      |
| t <sub>STE,ACC</sub> STE access time, STE active to SOMI data out          |                                                    | 2.2 V           |     |     | 50  | ns   |
|                                                                            |                                                    | 3.0 V           |     |     | 40  |      |
| t <sub>STE,DIS</sub> STE disable time, STE inactive to SOMI high impedance |                                                    | 2.2 V           |     |     | 50  | ns   |
|                                                                            |                                                    | 3.0 V           |     |     | 45  |      |
| t <sub>SU,SI</sub> SIMO input data setup time                              |                                                    | 2.2 V           | 4   |     |     | ns   |
|                                                                            |                                                    | 3.0 V           | 4   |     |     |      |
| t <sub>HD,SI</sub> SIMO input data hold time                               |                                                    | 2.2 V           | 7   |     |     | ns   |
|                                                                            |                                                    | 3.0 V           | 7   |     |     |      |
| t <sub>VALID,SO</sub> SOMI output data valid time <sup>(2)</sup>           | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |     |     | 35  | ns   |
|                                                                            |                                                    | 3.0 V           |     |     | 35  |      |
| t <sub>HD,SO</sub> SOMI output data hold time <sup>(3)</sup>               | C <sub>L</sub> = 20 pF                             | 2.2 V           | 0   |     |     | ns   |
|                                                                            |                                                    | 3.0 V           | 0   |     |     |      |

- (1)  $f_{UCXCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$ .  
For the master parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$  see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-16](#) and [Figure 5-17](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-16](#) and [Figure 5-17](#).

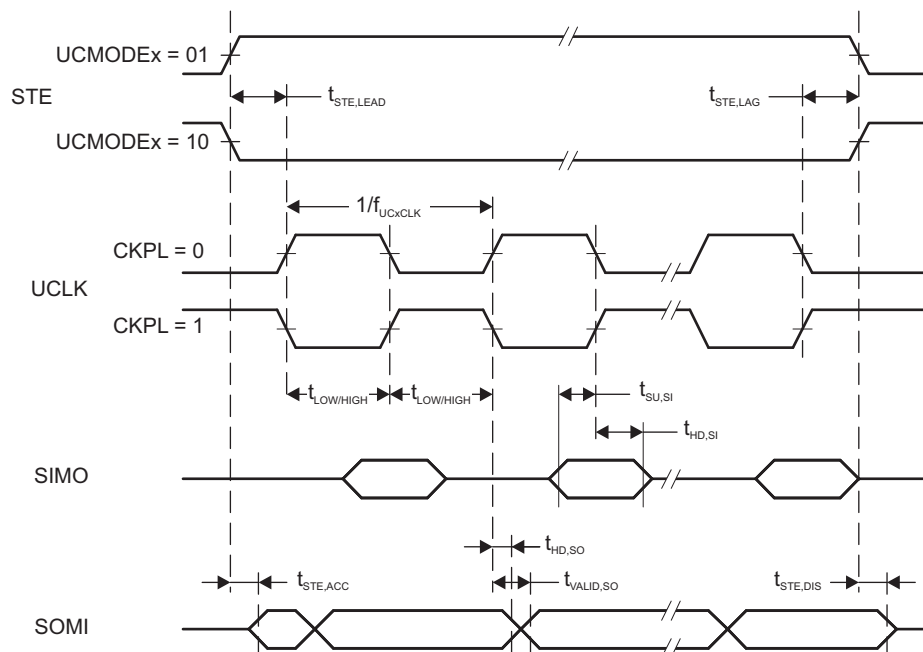


Figure 5-16. SPI Slave Mode, CKPH = 0

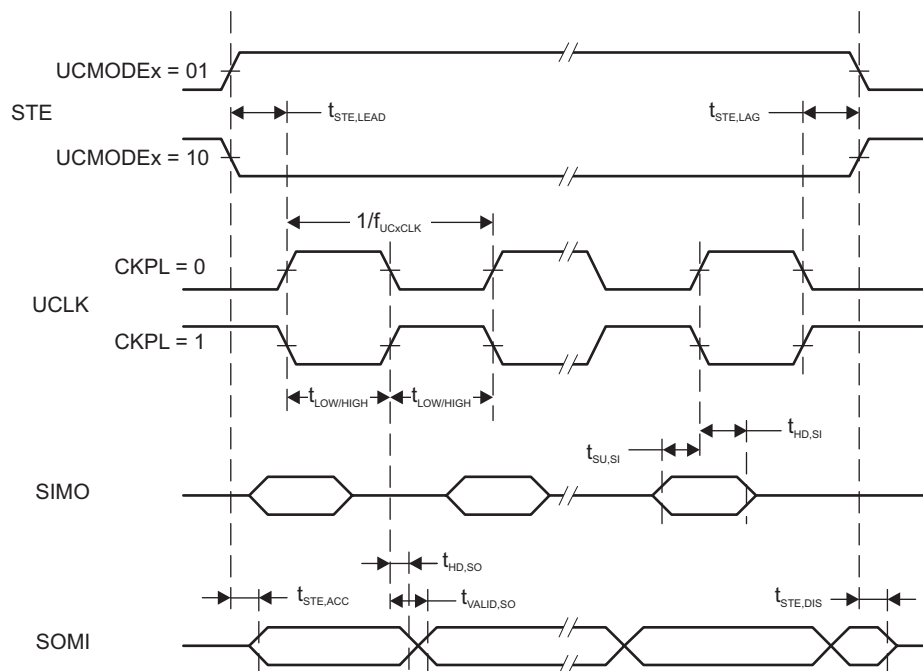


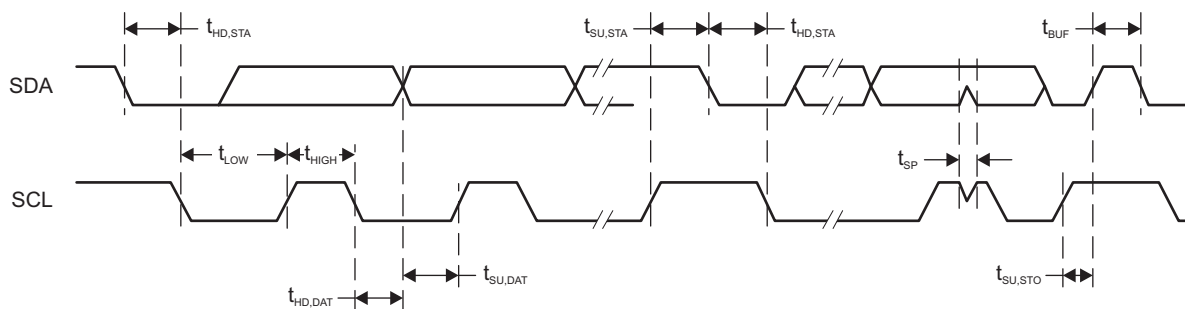
Figure 5-17. SPI Slave Mode, CKPH = 1

Table 5-21 lists the characteristics of the eUSCI in I<sup>2</sup>C mode.

**Table 5-21. eUSCI (I<sup>2</sup>C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-18)

| PARAMETER            | TEST CONDITIONS                                                                                 | V <sub>CC</sub> | MIN                        | TYP | MAX  | UNIT |
|----------------------|-------------------------------------------------------------------------------------------------|-----------------|----------------------------|-----|------|------|
| f <sub>eUSCI</sub>   | eUSCI input clock frequency<br>Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% |                 |                            |     | 16   | MHz  |
| f <sub>SCL</sub>     | SCL clock frequency                                                                             | 2.2 V, 3.0 V    | 0                          |     | 400  | kHz  |
| t <sub>HD,STA</sub>  | Hold time (repeated) START                                                                      | 2.2 V, 3.0 V    | f <sub>SCL</sub> = 100 kHz |     | 4.0  | μs   |
|                      |                                                                                                 |                 | f <sub>SCL</sub> > 100 kHz |     | 0.6  |      |
| t <sub>SU,STA</sub>  | Setup time for a repeated START                                                                 | 2.2 V, 3.0 V    | f <sub>SCL</sub> = 100 kHz |     | 4.7  | μs   |
|                      |                                                                                                 |                 | f <sub>SCL</sub> > 100 kHz |     | 0.6  |      |
| t <sub>HD,DAT</sub>  | Data hold time                                                                                  | 2.2 V, 3.0 V    | 0                          |     |      | ns   |
| t <sub>SU,DAT</sub>  | Data setup time                                                                                 | 2.2 V, 3.0 V    | 100                        |     |      | ns   |
| t <sub>SU,STO</sub>  | Setup time for STOP                                                                             | 2.2 V, 3.0 V    | f <sub>SCL</sub> = 100 kHz |     | 4.0  | μs   |
|                      |                                                                                                 |                 | f <sub>SCL</sub> > 100 kHz |     | 0.6  |      |
| t <sub>BUF</sub>     | Bus free time between a STOP and START condition                                                |                 | f <sub>SCL</sub> = 100 kHz |     | 4.7  | us   |
|                      |                                                                                                 |                 | f <sub>SCL</sub> > 100 kHz |     | 1.3  |      |
| t <sub>SP</sub>      | Pulse duration of spikes suppressed by input filter                                             | 2.2 V, 3.0 V    | UCGLITx = 0                |     | 50   | ns   |
|                      |                                                                                                 |                 | UCGLITx = 1                |     | 25   |      |
|                      |                                                                                                 |                 | UCGLITx = 2                |     | 12.5 |      |
|                      |                                                                                                 |                 | UCGLITx = 3                |     | 6.3  |      |
| t <sub>TIMEOUT</sub> | Clock low time-out                                                                              | 2.2 V, 3.0 V    | UCCLTOx = 1                |     | 27   | ms   |
|                      |                                                                                                 |                 | UCCLTOx = 2                |     | 30   |      |
|                      |                                                                                                 |                 | UCCLTOx = 3                |     | 33   |      |



**Figure 5-18. I<sup>2</sup>C Mode Timing**

## 5.12.8 ADC12

Table 5-22 lists the power supply and input range conditions for the ADC.

**Table 5-22. 12-Bit ADC, Power Supply and Input Range Conditions**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                          | V <sub>CC</sub> | MIN | NOM | MAX  | UNIT |
|-------------------------------------------|--------------------------------------------------------------------------|-----------------|-----|-----|------|------|
| V(Ax) Analog input voltage <sup>(1)</sup> | All ADC12 analog input pins Ax                                           |                 | 0   |     | AVCC | V    |
| I(ADC12_B) single-ended mode              | Operating supply current into AVCC plus DVCC terminal <sup>(2) (3)</sup> | 3.0 V           |     | 145 | 199  | μA   |
|                                           |                                                                          | 2.2 V           |     | 140 | 190  |      |
| I(ADC12_B) differential mode              | Operating supply current into AVCC and DVCC terminals <sup>(2) (3)</sup> | 3.0 V           |     | 175 | 245  | μA   |
|                                           |                                                                          | 2.2 V           |     | 170 | 230  |      |
| C <sub>I</sub> Input capacitance          | Only one terminal Ax can be selected at one time                         | 2.2 V           |     | 10  | 15   | pF   |
| R <sub>I</sub> Input MUX ON resistance    | 0 V ≤ V(Ax) ≤ AVCC                                                       | >2 V            |     | 0.5 | 4    | kΩ   |
|                                           |                                                                          | <2 V            |     | 1   | 10   |      |

(1) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results.

(2) The internal reference supply current is not included in current consumption parameter I(ADC12\_B).

(3) Typically about 60% of the total current into the AVCC and DVCC terminal is from AVCC.

Table 5-23 lists the timing parameter for the ADC.

**Table 5-23. 12-Bit ADC, Timing Parameters**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                | TEST CONDITIONS                                                                                                                            | MIN  | TYP    | MAX | UNIT |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------|--------|-----|------|
| f <sub>ADC12CLK</sub> Specified performance                              | For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0, If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here | 0.45 |        | 5.4 | MHz  |
| f <sub>ADC12CLK</sub> Reduced performance                                | Linearity parameters have reduced performance                                                                                              |      | 32.768 |     | kHz  |
| f <sub>ADC12OSC</sub> Internal oscillator <sup>(1)</sup>                 | ADC12DIV = 0, f <sub>ADC12CLK</sub> = f <sub>ADC12OSC</sub> from MODCLK                                                                    | 4    | 4.8    | 5.4 | MHz  |
| t <sub>CONVERT</sub> Conversion time                                     | REFON = 0, Internal oscillator, f <sub>ADC12CLK</sub> = f <sub>ADC12OSC</sub> from MODCLK, ADC12WINC = 0                                   | 2.6  |        | 3.5 | μs   |
|                                                                          | External f <sub>ADC12CLK</sub> from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0                                                                    |      | (2)    |     |      |
| t <sub>ADC12ON</sub> Turnon settling time of the ADC                     | See <sup>(3)</sup>                                                                                                                         |      |        | 100 | ns   |
| t <sub>ADC12OFF</sub> Time ADC must be off before can be turned on again | t <sub>ADC12OFF</sub> must be met to make sure t <sub>ADC12ON</sub> time holds                                                             | 100  |        |     | ns   |

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(2)  $14 \times 1 / f_{\text{ADC12CLK}}$ . If ADC12WINC = 1, then  $15 \times 1 / f_{\text{ADC12CLK}}$

(3) The condition is that the error in a conversion started after t<sub>ADC12ON</sub> is less than ±0.5 LSB. The reference and input signals are already settled.

**Table 5-23. 12-Bit ADC, Timing Parameters (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                         | TEST CONDITIONS                                                                                                                                                                                                                                                                          | MIN | TYP | MAX | UNIT          |
|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_{\text{Sample}}$ Sampling time | $R_S = 400\ \Omega$ , $R_I = 4\ \text{k}\Omega$ , $C_I = 15\ \text{pF}$ , $C_{\text{pext}} = 8\ \text{pF}$ <sup>(4)</sup><br>All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12 VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF) | 1   |     |     | $\mu\text{s}$ |
|                                   | Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12 VRSEL = 0x0, 0x2, 0x4, 0x6, 0xC, 0xE)                                                                                                                                                                               | (5) |     |     | $\mu\text{s}$ |

(4) Approximately 10 Tau ( $\tau$ ) are needed to get an error of less than  $\pm 0.5$  LSB:  $t_{\text{sample}} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{\text{pext}})$ ,  $R_S < 10\ \text{k}\Omega$ , where  $n$  = ADC resolution = 12,  $R_S$  = external source resistance,  $C_{\text{pext}}$  = external parasitic capacitance.

(5)  $6 \times (1 / f_{\text{ADC12CLK}})$

Table 5-24 lists the linearity parameters of the ADC when using an external reference.

**Table 5-24. 12-Bit ADC, Linearity Parameters With External Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                    | TEST CONDITIONS                                                                                                                                                                                                                      | MIN   | TYP       | MAX        | UNIT |
|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----------|------------|------|
| Resolution Number of no missing code output-code bits        |                                                                                                                                                                                                                                      | 12    |           |            | bits |
| $E_I$ Integral linearity error (INL) for differential input  | $1.2\ \text{V} \leq V_{R+} - V_{R-} \leq AV_{CC}$                                                                                                                                                                                    |       |           | $\pm 1.8$  | LSB  |
| $E_I$ Integral linearity error (INL) for single ended inputs | $1.2\ \text{V} \leq V_{R+} - V_{R-} \leq AV_{CC}$                                                                                                                                                                                    |       |           | $\pm 2.2$  | LSB  |
| $E_D$ Differential linearity error (DNL)                     |                                                                                                                                                                                                                                      | -0.99 |           | +1.0       | LSB  |
| $E_O$ Offset error <sup>(2) (3)</sup>                        | ADC12 VRSEL = 0x2 or 0x4 without TLV calibration, TLV calibration data can be used to improve the parameter <sup>(4)</sup>                                                                                                           |       | $\pm 0.5$ | $\pm 1.5$  | mV   |
| $E_{G,\text{ext}}$ Gain error                                | With external voltage reference without internal buffer (ADC12 VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter <sup>(4)</sup> , $V_{R+} = 2.5\ \text{V}$ , $V_{R-} = AV_{SS}$ |       | $\pm 0.8$ | $\pm 2.5$  | LSB  |
|                                                              | With external voltage reference with internal buffer (ADC12 VRSEL = 0x3), $V_{R+} = 2.5\ \text{V}$ , $V_{R-} = AV_{SS}$                                                                                                              |       | $\pm 1$   | $\pm 20$   |      |
| $E_{T,\text{ext}}$ Total unadjusted error                    | With external voltage reference without internal buffer (ADC12 VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter <sup>(4)</sup> , $V_{R+} = 2.5\ \text{V}$ , $V_{R-} = AV_{SS}$ |       | $\pm 1.4$ | $\pm 3.5$  | LSB  |
|                                                              | With external voltage reference with internal buffer (ADC12 VRSEL = 0x3), $V_{R+} = 2.5\ \text{V}$ , $V_{R-} = AV_{SS}$                                                                                                              |       | $\pm 1.4$ | $\pm 21.0$ |      |

(1) See Table 5-26 and Table 5-32 for more information on internal reference performance and see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

(2) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.

(3) Offset increases as  $I_R$  drop increases when  $V_{R-}$  is  $AV_{SS}$ .

(4) For details, see the device descriptor table section in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

[Table 5-25](#) lists the differential dynamic performance characteristics of the ADC with an external reference.

**Table 5-25. 12-Bit ADC, Dynamic Performance for Differential Inputs With External Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                         | TEST CONDITIONS                                  | MIN  | TYP  | MAX | UNIT |
|-----------|-----------------------------------------|--------------------------------------------------|------|------|-----|------|
| SNR       | Signal-to-noise ratio                   | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 68   | 71   |     | dB   |
| ENOB      | Effective number of bits <sup>(2)</sup> | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 10.7 | 11.2 |     | bits |

- (1) See [Table 5-26](#) and [Table 5-32](#) for more information on internal reference performance and see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

- (2)  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$

[Table 5-26](#) lists the differential dynamic performance characteristics of the ADC with an internal reference.

**Table 5-26. 12-Bit ADC, Dynamic Performance for Differential Inputs With Internal Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                         | TEST CONDITIONS                                  | MIN  | TYP  | MAX | UNIT |
|-----------|-----------------------------------------|--------------------------------------------------|------|------|-----|------|
| ENOB      | Effective number of bits <sup>(2)</sup> | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 10.3 | 10.7 |     | Bits |

- (1) See [Table 5-32](#) for more information on internal reference performance and see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

- (2)  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$

[Table 5-27](#) lists the single-ended dynamic performance characteristics of the ADC with an external reference.

**Table 5-27. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With External Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                         | TEST CONDITIONS                                  | MIN  | TYP  | MAX | UNIT |
|-----------|-----------------------------------------|--------------------------------------------------|------|------|-----|------|
| SNR       | Signal-to-noise ratio                   | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 64   | 68   |     | dB   |
| ENOB      | Effective number of bits <sup>(2)</sup> | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 10.2 | 10.7 |     | bits |

- (1) See [Table 5-28](#) and [Table 5-32](#) for more information on internal reference performance and see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

- (2)  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$

[Table 5-28](#) lists the single-ended dynamic performance characteristics of the ADC with an internal reference.

**Table 5-28. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With Internal Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                         | TEST CONDITIONS                                  | MIN | TYP  | MAX | UNIT |
|-----------|-----------------------------------------|--------------------------------------------------|-----|------|-----|------|
| ENOB      | Effective number of bits <sup>(2)</sup> | $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ | 9.4 | 10.4 |     | bits |

- (1) See [Table 5-32](#) for more information on internal reference performance and see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

- (2)  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$

[Table 5-29](#) lists the dynamic performance characteristics of the ADC with using a 32.768-kHz clock.

**Table 5-29. 12-Bit ADC, Dynamic Performance With 32.768-kHz Clock**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                         | TEST CONDITIONS                                                                                                               | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| ENOB      | Effective number of bits <sup>(1)</sup> | Reduced performance with $f_{\text{ADC12CLK}}$ from ACLK LFXT at 32.768 kHz, $V_{R+} = 2.5\text{ V}$ , $V_{R-} = \text{AVSS}$ |     | 10  |     | bits |

- (1)  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$

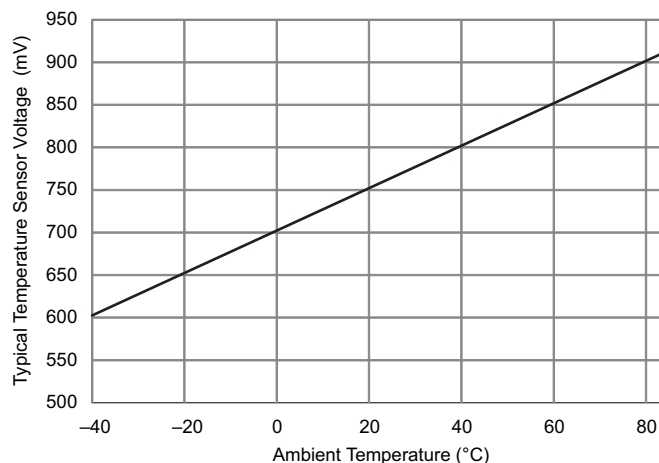
Table 5-30 lists the temperature sensor and built-in  $V_{1/2}$  characteristics.

**Table 5-30. 12-Bit ADC, Temperature Sensor and Built-In  $V_{1/2}$**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                             | TEST CONDITIONS                                                           | $V_{CC}$ | MIN   | TYP | MAX   | UNIT                 |
|------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|----------|-------|-----|-------|----------------------|
| $V_{SENSOR}$           | See <sup>(1)</sup> <sup>(2)</sup>                                                           | ADC12ON = 1, ADC12TCMAP = 1,<br>$T_A = 0^\circ\text{C}$ (see Figure 5-19) |          |       | 700 |       | mV                   |
| $TC_{SENSOR}$          | See <sup>(2)</sup>                                                                          | ADC12ON = 1, ADC12TCMAP = 1                                               |          |       | 2.5 |       | mV/ $^\circ\text{C}$ |
| $t_{SENSOR(sample)}$   | Sample time required if<br>ADCTCMAP = 1 and channel<br>(MAX – 1) is selected <sup>(3)</sup> | ADC12ON = 1, ADC12TCMAP = 1,<br>Error of conversion result $\leq 1$ LSB   |          |       | 30  |       | $\mu\text{s}$        |
| $V_{1/2}$              | AVCC voltage divider for<br>ADC12BATMAP = 1 on MAX input<br>channel                         | ADC12ON = 1, ADC12BATMAP = 1                                              |          | 47.5% | 50% | 52.5% |                      |
| $I_{V\ 1/2}$           | current for battery monitor during<br>sample time                                           | ADC12ON = 1, ADC12BATMAP = 1                                              |          |       | 38  | 72    | $\mu\text{A}$        |
| $t_{V\ 1/2\ (sample)}$ | Sample time required if<br>ADC12BATMAP = 1 and channel<br>MAX is selected <sup>(4)</sup>    | ADC12ON = 1, ADC12BATMAP = 1                                              |          |       | 1.7 |       | $\mu\text{s}$        |

- (1) The temperature sensor offset can be as much as  $\pm 30^\circ\text{C}$ . TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for  $30^\circ\text{C} \pm 3^\circ\text{C}$  and  $85^\circ\text{C} \pm 3^\circ\text{C}$  for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} * (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$ , where  $TC_{SENSOR}$  and  $V_{SENSOR}$  can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 250 k $\Omega$ . The sample time required includes the sensor on-time  $t_{SENSOR(on)}$ .
- (4) The on-time  $t_{V\ 1/2(on)}$  is included in the sampling time  $t_{V\ 1/2\ (sample)}$ ; no additional on time is needed.



**Figure 5-19. Typical Temperature Sensor Voltage**

Table 5-31 lists the external reference characteristics of the ADC.

**Table 5-31. 12-Bit ADC, External Reference<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                    |                                                                                        | TEST CONDITIONS                                                                                                                                                    | MIN | MAX       | UNIT          |
|------------------------------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------|---------------|
| $V_{R+}$                     | Positive external reference voltage input<br>VeREF+ or VeREF- based on ADC12 VRSEL bit | $V_{R+} > V_{R-}$                                                                                                                                                  | 1.2 | $AV_{CC}$ | V             |
| $V_{R-}$                     | Negative external reference voltage input<br>VeREF+ or VeREF- based on ADC12 VRSEL bit | $V_{R+} > V_{R-}$                                                                                                                                                  | 0   | 1.2       | V             |
| $(V_{R+} - V_{R-})$          | Differential external reference voltage input                                          | $V_{R+} > V_{R-}$                                                                                                                                                  | 1.2 | $AV_{CC}$ | V             |
| $I_{VeREF+}$<br>$I_{VeREF-}$ | Static input current singled ended input mode                                          | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 1h$ ,<br>$ADC12DIF = 0$ , $ADC12PWRMD = 0$  |     | $\pm 10$  | $\mu\text{A}$ |
|                              |                                                                                        | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 8h$ ,<br>$ADC12DIF = 0$ , $ADC12PWRMD = 01$ |     | $\pm 2.5$ |               |
| $I_{VeREF+}$<br>$I_{VeREF-}$ | Static input current differential input mode                                           | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 1h$ ,<br>$ADC12DIF = 1$ , $ADC12PWRMD = 0$  |     | $\pm 20$  | $\mu\text{A}$ |
|                              |                                                                                        | $1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $V_{eREF-} = 0\text{ V}$<br>$f_{ADC12CLK} = 5\text{ MHz}$ , $ADC12SHTx = 8h$ ,<br>$ADC12DIF = 1$ , $ADC12PWRMD = 1$  |     | $\pm 5$   |               |
| $I_{VeREF+}$                 | Peak input current with single ended input                                             | $0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $ADC12DIF = 0$                                                                                                         |     | 1.5       | mA            |
| $I_{VeREF+}$                 | Peak input current with differential input                                             | $0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$ , $ADC12DIF = 1$                                                                                                         |     | 3         | mA            |
| $C_{VeREF+/-}$               | Capacitance at VeREF+ or VeREF- terminal                                               | See <sup>(2)</sup>                                                                                                                                                 | 10  |           | $\mu\text{F}$ |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance,  $C_i$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) Two decoupling capacitors, 10  $\mu\text{F}$  and 470 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC12\_B. See also the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

## 5.12.9 REF Module

Table 5-32 lists the characteristics of the built-in voltage reference.

**Table 5-32. REF, Built-In Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                  | TEST CONDITIONS                                            | V <sub>CC</sub>                                                                                                                | MIN | TYP   | MAX   | UNIT  |
|--------------------------------------------|------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----|-------|-------|-------|
| V <sub>REF+</sub>                          | REFVSEL = {2} for 2.5 V, REFON = 1                         | 2.7 V                                                                                                                          |     | 2.5   | ±1.5% | V     |
|                                            | REFVSEL = {1} for 2.0 V, REFON = 1                         | 2.2 V                                                                                                                          |     | 2.0   | ±1.5% |       |
|                                            | REFVSEL = {0} for 1.2 V, REFON = 1                         | 1.8 V                                                                                                                          |     | 1.2   | ±1.8% |       |
| Noise                                      | RMS noise at VREF <sup>(1)</sup>                           | From 0.1 Hz to 10 Hz, REFVSEL = {0}                                                                                            |     | 110   | 600   | μV    |
| V <sub>OS_BUF_INT</sub>                    | VREF ADC BUF_INT buffer offset <sup>(2)</sup>              | T <sub>A</sub> = 25°C, ADC ON, REFVSEL = {0}, REFON = 1, REFOUT = 0                                                            |     | –12   | +12   | mV    |
| V <sub>OS_BUF_EXT</sub>                    | VREF ADC BUF_EXT buffer offset <sup>(2)</sup>              | T <sub>A</sub> = 25°C, REFVSEL = {0}, REFOUT = 1, REFON = 1 or ADC ON                                                          |     | –12   | +12   | mV    |
| AV <sub>CC(min)</sub>                      | AVCC minimum voltage, Positive built-in reference active   | REFVSEL = {0} for 1.2 V                                                                                                        |     | 1.8   |       | V     |
|                                            |                                                            | REFVSEL = {1} for 2.0 V                                                                                                        |     | 2.2   |       |       |
|                                            |                                                            | REFVSEL = {2} for 2.5 V                                                                                                        |     | 2.7   |       |       |
| I <sub>REF+</sub>                          | Operating supply current into AVCC terminal <sup>(3)</sup> | REFON = 1                                                                                                                      | 3 V | 8     | 15    | μA    |
| I <sub>REF+_ADC_BUF</sub>                  | Operating supply current into AVCC terminal <sup>(3)</sup> | ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0,                                                                       | 3 V | 225   | 355   | μA    |
|                                            |                                                            | ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0                                                                        |     | 1030  | 1660  |       |
|                                            |                                                            | ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1                                                                        |     | 120   | 185   |       |
|                                            |                                                            | ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1                                                                        |     | 545   | 895   |       |
|                                            |                                                            | ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}                                                                            |     | 1085  | 1780  |       |
| I <sub>O(VREF+)</sub>                      | VREF maximum load current, VREF+ terminal                  | REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1                                             |     | –1000 | +10   | μA    |
| ΔV <sub>out</sub> /ΔI <sub>O</sub> (VREF+) | Load-current regulation, VREF+ terminal                    | REFVSEL = {0, 1, 2}, I <sub>O(VREF+)</sub> = +10 μA or –1000 μA, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1 |     |       | 2500  | μV/mA |
| C <sub>VREF+/-</sub>                       | Capacitance at VREF+ and VREF- terminals                   | REFON = REFOUT = 1                                                                                                             |     | 0     | 100   | pF    |
| TC <sub>REF+</sub>                         | Temperature coefficient of built-in reference              | REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T <sub>A</sub> = –40°C to 85°C <sup>(4)</sup>                                         |     | 18    | 50    | ppm/K |
| PSRR <sub>DC</sub>                         | Power supply rejection ratio (DC)                          | AVCC = AVCC(min) to AVCC(max), T <sub>A</sub> = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1                                  |     | 120   | 400   | μV/V  |
| PSRR <sub>AC</sub>                         | Power supply rejection ratio (AC)                          | dAVCC = 0.1 V at 1 kHz                                                                                                         |     | 3.0   |       | mV/V  |
| t <sub>SETTLE</sub>                        | Settling time of reference voltage <sup>(5)</sup>          | AVCC = AVCC(min) to AVCC(max), REFVSEL = {0, 1, 2}, REFON = 0 → 1                                                              |     | 75    | 80    | μs    |

(1) Internal reference noise affects ADC performance when ADC uses internal reference. See [Designing With the MSP430FR59xx and MSP430FR58xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

(2) Buffer offset affects ADC gain error and thus total unadjusted error.

(3) The internal reference current is supplied through the AVCC terminal.

(4) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).

(5) The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB.

## 5.12.10 Comparator

Table 5-33 lists the characteristics of the comparator.

**Table 5-33. Comparator\_E**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS                                                                         | V <sub>CC</sub> | MIN                  | TYP                | MAX                  | UNIT |
|--------------------------|-----------------------------------------------------------------------------------------|-----------------|----------------------|--------------------|----------------------|------|
| I <sub>AVCC_COMP</sub>   | CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)                                               | 2.2 V, 3.0 V    | 11                   |                    | 20                   | μA   |
|                          | CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)                                             |                 | 9                    |                    | 17                   |      |
|                          | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T <sub>A</sub> = 30°C                        |                 |                      |                    | 0.5                  |      |
|                          | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T <sub>A</sub> = 85°C                        |                 |                      |                    | 1.3                  |      |
| I <sub>AVCC_REF</sub>    | CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 0                             | 2.2 V, 3.0 V    | 12                   |                    | 15                   | μA   |
|                          | CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 1                             |                 | 5                    |                    | 7                    |      |
| V <sub>REF</sub>         | CERSx = 11, CEREFLx = 01, CEREFACC = 0                                                  | 1.8 V           | 1.17                 | 1.2                | 1.23                 | V    |
|                          | CERSx = 11, CEREFLx = 10, CEREFACC = 0                                                  | 2.2 V           | 1.92                 | 2.0                | 2.08                 |      |
|                          | CERSx = 11, CEREFLx = 11, CEREFACC = 0                                                  | 2.7 V           | 2.40                 | 2.5                | 2.60                 |      |
|                          | CERSx = 11, CEREFLx = 01, CEREFACC = 1                                                  | 1.8 V           | 1.10                 | 1.2                | 1.245                |      |
|                          | CERSx = 11, CEREFLx = 10, CEREFACC = 1                                                  | 2.2 V           | 1.90                 | 2.0                | 2.08                 |      |
|                          | CERSx = 11, CEREFLx = 11, CEREFACC = 1                                                  | 2.7 V           | 2.35                 | 2.5                | 2.60                 |      |
| V <sub>IC</sub>          | Common-mode input range                                                                 |                 | 0                    |                    | V <sub>CC</sub> – 1  | V    |
| V <sub>OFFSET</sub>      | CEPWRMD = 00                                                                            |                 | –32                  |                    | 32                   | mV   |
|                          | CEPWRMD = 01                                                                            |                 | –32                  |                    | 32                   |      |
|                          | CEPWRMD = 10                                                                            |                 | –30                  |                    | 30                   |      |
| C <sub>IN</sub>          | CEPWRMD = 00 or CEPWRMD = 01                                                            |                 |                      | 9                  |                      | pF   |
|                          | CEPWRMD = 10                                                                            |                 |                      | 9                  |                      |      |
| R <sub>SIN</sub>         | On (switch closed)                                                                      |                 |                      | 1                  | 3                    | kΩ   |
|                          | Off (switch open)                                                                       |                 | 50                   |                    |                      | MΩ   |
| t <sub>PD</sub>          | CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV                                                |                 |                      | 260                | 330                  | ns   |
|                          | CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV                                                |                 |                      | 350                | 460                  |      |
|                          | CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV                                                |                 |                      |                    | 15                   | μs   |
| t <sub>PD,filter</sub>   | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 00                             |                 |                      | 700                | 1000                 | ns   |
|                          | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 01                             |                 |                      | 1.0                | 1.8                  |      |
|                          | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 10                             |                 |                      | 2.0                | 3.5                  |      |
|                          | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 11                             |                 |                      | 4.0                | 7.0                  |      |
| t <sub>EN_CMP</sub>      | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00                     |                 |                      | 0.9                | 1.5                  | μs   |
|                          | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01                     |                 |                      | 0.9                | 1.5                  |      |
|                          | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10                     |                 |                      | 15                 | 100                  |      |
| t <sub>EN_CMP_VREF</sub> | CEON = 0 → 1, CEREFLx = 10, CERSx = 10 or 11, CEREF0 = CEREF1 = 0x0F, Overdrive ≥ 20 mV |                 |                      | 350                | 1500                 | μs   |
| V <sub>CE_REF</sub>      | VIN = reference into resistor ladder, n = 0 to 31                                       |                 | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V    |

### 5.12.11 FRAM Controller

Table 5-34 lists the characteristics of the FRAM.

**Table 5-34. FRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                |                            | TEST CONDITIONS       | MIN              | TYP                                    | MAX | UNIT   |
|--------------------------|----------------------------|-----------------------|------------------|----------------------------------------|-----|--------|
| Read and write endurance |                            |                       | 10 <sup>15</sup> |                                        |     | cycles |
| t <sub>Retention</sub>   | Data retention duration    | T <sub>J</sub> = 25°C | 100              |                                        |     | years  |
|                          |                            | T <sub>J</sub> = 70°C | 40               |                                        |     |        |
|                          |                            | T <sub>J</sub> = 85°C | 10               |                                        |     |        |
| I <sub>WRITE</sub>       | Current to write into FRAM |                       |                  | I <sub>READ</sub> <sup>(1)</sup>       |     | nA     |
| I <sub>ERASE</sub>       | Erase current              |                       |                  | N/A <sup>(2)</sup>                     |     | nA     |
| t <sub>WRITE</sub>       | Write time                 |                       |                  | t <sub>READ</sub> <sup>(3)</sup>       |     | ns     |
| t <sub>READ</sub>        | Read time, NWAITSx = 0     |                       |                  | 1 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     | ns     |
|                          | Read time, NWAITSx = 1     |                       |                  | 2 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     |        |

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I<sub>READ</sub> is included in the active mode current consumption numbers I<sub>AM,FRAM</sub>.

(2) N/A = not applicable. FRAM does not require a special erase sequence.

(3) Writing into FRAM is as fast as reading.

(4) The maximum read (and write) speed is specified by f<sub>SYSTEM</sub> using the appropriate wait state settings (NWAITSx).

### 5.12.12 Emulation and Debug

Table 5-35 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

**Table 5-35. JTAG and Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                       |                                                                                                                         | TEST CONDITIONS | MIN  | TYP | MAX | UNIT |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----|-----|------|
| I <sub>JTAG</sub>               | Supply current adder when JTAG active (but not clocked)                                                                 | 2.2 V, 3.0 V    |      | 40  | 100 | μA   |
| f <sub>SBW</sub>                | Spy-Bi-Wire input frequency                                                                                             | 2.2 V, 3.0 V    | 0    |     | 10  | MHz  |
| t <sub>SBW,Low</sub>            | Spy-Bi-Wire low clock pulse duration                                                                                    | 2.2 V, 3.0 V    | 0.04 |     | 15  | μs   |
| t <sub>SBW,En</sub>             | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup>                                    | 2.2 V, 3.0 V    |      |     | 110 | μs   |
| t <sub>SBW,Rst</sub>            | Spy-Bi-Wire return to normal operation time                                                                             |                 | 15   |     | 100 | μs   |
| f <sub>TCK</sub>                | TCK input frequency, 4-wire JTAG <sup>(2)</sup>                                                                         | 2.2 V           | 0    |     | 16  | MHz  |
|                                 |                                                                                                                         | 3.0 V           | 0    |     | 16  | MHz  |
| R <sub>internal</sub>           | Internal pulldown resistance on TEST                                                                                    | 2.2 V, 3.0 V    | 20   | 35  | 50  | kΩ   |
| f <sub>TCLK</sub>               | TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f <sub>SYSTEM</sub> )                                |                 |      |     | 16  | MHz  |
| t <sub>TCLK,Low/High</sub>      | TCLK low or high clock pulse duration, no FRAM access                                                                   |                 |      |     | 25  | ns   |
| f <sub>TCLK,FRAM</sub>          | TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f <sub>SYSTEM</sub> with no FRAM wait states) |                 |      |     | 4   | MHz  |
| t <sub>TCLK,FRAM,Low/High</sub> | TCLK low or high clock pulse duration, including FRAM accesses                                                          |                 |      |     | 100 | ns   |

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the t<sub>SBW,En</sub> time after the first transition of the TEST/SBW/TCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

## 6 Detailed Description

### 6.1 Overview

The Texas Instruments MSP430FR597x(1) and MSP430FR587x(1) family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The devices are microcontroller configurations with up to five 16-bit timers, a comparator, eUSCs that support UART, SPI, and I<sup>2</sup>C, a hardware multiplier, an AES accelerator, DMA, an RTC module with alarm capabilities, up to 52 I/O pins, and a high-performance 12-bit ADC.

### 6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. CPUxV2 can also operate on address-word data (20-bit).

### 6.3 Operating Modes

The device has one active mode and seven software selectable low-power modes of operation (see 表 6-1). An interrupt event can wake up the device from low-power modes LPM0 to LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

表 6-1. Operating Modes

| MODE                                 | AM                  |                                 | LPM0                             | LPM1                | LPM2                     | LPM3                     | LPM4                     | LPM3.5                  | LPM4.5            |                      |
|--------------------------------------|---------------------|---------------------------------|----------------------------------|---------------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------|----------------------|
|                                      | Active              | Active, FRAM Off <sup>(1)</sup> | CPU Off <sup>(2)</sup>           | CPU Off             | Standby                  | Standby                  | Off                      | RTC Only                | Shutdown With SVS | Shutdown Without SVS |
| Maximum system clock                 | 16 MHz              |                                 | 16 MHz                           | 16 MHz              | 50 kHz                   | 50 kHz                   | 0 <sup>(3)</sup>         | 50 kHz                  | 0 <sup>(3)</sup>  |                      |
| Typical current consumption, 25°C    | 103 µA/MHz          | 65 µA/MHz                       | 75 µA at 1 MHz                   | 40 µA at 1 MHz      | 0.9 µA                   | 0.4 µA                   | 0.3 µA                   | 0.35 µA                 | 0.2 µA            | 0.02 µA              |
| Typical wake-up time                 | N/A                 |                                 | instant.                         | 6 µs                | 6 µs                     | 7 µs                     | 7 µs                     | 250 µs                  | 250 µs            | 1000 µs              |
| Wake-up events                       | N/A                 |                                 | all                              | all                 | LF<br>RTC<br>I/O<br>Comp | LF<br>RTC<br>I/O<br>Comp | I/O<br>Comp              | RTC<br>I/O              | I/O               |                      |
| CPU                                  | on                  |                                 | off                              | off                 | off                      | off                      | off                      | reset                   | reset             |                      |
| FRAM                                 | on                  | off <sup>(1)</sup>              | standby (or off <sup>(1)</sup> ) | off                 | off                      | off                      | off                      | off                     | off               |                      |
| High-frequency peripherals           | available           |                                 | available                        | available           | off                      | off                      | off                      | reset                   | reset             |                      |
| Low-frequency peripherals            | available           |                                 | available                        | available           | available                | available <sup>(4)</sup> | off                      | RTC                     | reset             |                      |
| Unclocked peripherals <sup>(5)</sup> | available           |                                 | available                        | available           | available                | available <sup>(4)</sup> | available <sup>(4)</sup> | reset                   | reset             |                      |
| MCLK                                 | on                  |                                 | off                              | off                 | off                      | off                      | off                      | off                     | off               |                      |
| SMCLK                                | opt. <sup>(6)</sup> |                                 | opt. <sup>(6)</sup>              | opt. <sup>(6)</sup> | off                      | off                      | off                      | off                     | off               |                      |
| ACLK                                 | on                  |                                 | on                               | on                  | on                       | on                       | off                      | off                     | off               |                      |
| Full retention                       | yes                 |                                 | yes                              | yes                 | yes                      | yes <sup>(7)</sup>       | yes <sup>(7)</sup>       | no                      | no                |                      |
| SVS                                  | always              |                                 | always                           | always              | optional <sup>(8)</sup>  | optional <sup>(8)</sup>  | optional <sup>(8)</sup>  | optional <sup>(8)</sup> | on <sup>(9)</sup> | off <sup>(10)</sup>  |
| Brownout                             | always              |                                 | always                           | always              | always                   | always                   | always                   | always                  | always            |                      |

(1) FRAM disabled in FRAM controller

(2) Disabling the FRAM through the FRAM controller decreases the LPM current consumption, but the wake-up time can increase. If the wakeup is for FRAM access (for example, to fetch an interrupt vector), wake-up time is increased. If the wakeup is for an operation that does not access FRAM (for example, DMA transfer to RAM), wake-up time is not increased.

(3) All clocks disabled

(4) See 6.3.2, which describes the use of peripherals in LPM3 and LPM4.

(5) "Unclocked peripherals" are peripherals that do not require a clock source to operate; for example, the comparator and REF, or the eUSCI when operated as an SPI slave.

(6) Controlled by SMCLKOFF

(7) Using the RAM Controller, the RAM can be completely powered down to save leakage; however, all data is lost.

(8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS not included in typical current consumption.

(9) SVSHE = 1

(10) SVSHE = 0

### 6.3.1 Peripherals in Low-Power Modes

Peripherals can be in different states that affect which power mode the device can enter. The states depend on the operational modes of the peripherals (see 表 6-2). The states are:

- A peripheral is in a "high-frequency state" if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a "low-frequency state" if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an "unlocked state" if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode. The device instead enters a power mode that still supports the current state of the peripherals, except if an external clock is used. If an external clock is used, the application must use the correct frequency range for the requested power mode.

表 6-2. Peripheral States

| PERIPHERAL                                           | IN HIGH-FREQUENCY STATE <sup>(1)</sup>                | IN LOW-FREQUENCY STATE <sup>(2)</sup>                | IN UNLOCKED STATE <sup>(3)</sup>                                 |
|------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------------------|
| WDT                                                  | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| DMA <sup>(4)</sup>                                   | Not applicable                                        | Not applicable                                       | Waiting for a trigger                                            |
| RTC_C                                                | Not applicable                                        | Clocked by LFXT                                      | Not applicable                                                   |
| Timer_A TA <sub>x</sub>                              | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz                                |
| Timer_B TB <sub>x</sub>                              | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz                                |
| eUSCI_A <sub>x</sub> in UART mode                    | Clocked by SMCLK                                      | Clocked by ACLK                                      | Waiting for first edge of START bit.                             |
| eUSCI_A <sub>x</sub> in SPI master mode              | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| eUSCI_A <sub>x</sub> in SPI slave mode               | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Clocked by external clock ≤50 kHz                                |
| eUSCI_B <sub>x</sub> in I <sup>2</sup> C master mode | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Not applicable                                                   |
| eUSCI_B <sub>x</sub> in I <sup>2</sup> C slave mode  | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Waiting for START condition or clocked by external clock ≤50 kHz |
| eUSCI_B <sub>x</sub> in SPI master mode              | Clocked by SMCLK                                      | Clocked by ACLK                                      | Not applicable                                                   |
| eUSCI_B <sub>x</sub> in SPI slave mode               | Clocked by external clock >50 kHz                     | Clocked by external clock ≤50 kHz                    | Clocked by external clock ≤50 kHz                                |
| ADC12_B                                              | Clocked by SMCLK or by MODOSC                         | Clocked by ACLK                                      | Waiting for a trigger                                            |
| REF_A                                                | Not applicable                                        | Not applicable                                       | Always                                                           |
| COMP_E                                               | Not applicable                                        | Not applicable                                       | Always                                                           |
| CRC <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |
| MPY <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |
| AES <sup>(5)</sup>                                   | Not applicable                                        | Not applicable                                       | Not applicable                                                   |

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz.

(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.

(3) Peripherals are in a state that does not require or does not use an internal clock.

(4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode causes a temporary transition into active mode for the time of the transfer.

(5) This peripheral operates during active mode only and delays the transition into a low-power mode until its operation is completed.

### 6.3.2 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are even operational in LPM4 because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder, certain peripherals are group together. To achieve optimal current consumption, try to use modules within one group and to limit the number of groups with active modules. 表 6-3 lists the grouping. Modules not listed in this table are either already included in the standard LPM3 current consumption specifications or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C); see the  $I_{IDLE}$  current parameters in [Section 5.7](#) for details.

**表 6-3. Peripheral Groups**

| Group A    | Group B   | Group C   |
|------------|-----------|-----------|
| Timer TA0  | Timer TA2 | Timer TA3 |
| Timer TA1  | Timer B0  | eUSCI_A1  |
| Comparator | eUSCI_A0  |           |
| ADC12_B    | eUSCI_B0  |           |
| REF_A      | eUSCI_B1  |           |

### 6.4 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address, and signatures are in the address range 0FFFFh to 0FF80h. 表 6-4 summarizes the content of this address range.

The power-up start address or reset vector is at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh extending to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature)

The signatures are at 0FF80h extending to higher addresses. Signatures are evaluated during device start-up. Starting from address 0FF88h extending to higher addresses a JTAG password can be programmed. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password.

See the chapter *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#) for details.

**表 6-4. Interrupt Sources, Flags, Vectors, and Signatures**

| INTERRUPT SOURCE                                                                                                                                                                                                                                                                                            | INTERRUPT FLAG                                                                                                                                                                                                                                  | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|----------|
| <b>System Reset</b><br>Power-up, Brownout, Supply Supervisor<br>External Reset $\overline{\text{RST}}$<br>Watchdog time-out (watchdog mode)<br>WDT, FRCTL MPU, CS, PMM password violation<br>FRAM uncorrectable bit error detection<br>FRAM access time error<br>MPU segment violation<br>Software POR, BOR | SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>WDTPW, FRCTLPW, MPUW, CSPW, PMMPW<br>UBDIFG<br>ACCTEIFG<br>MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>PMMPORIFG, PMMBORIFG<br>(SYSRSTIV) <sup>(1) (2)</sup>                                                        | Reset            | 0FFFEh       | Highest  |
| <b>System NMI</b><br>Vacant memory access<br>JTAG mailbox<br>FRAM bit error detection<br>MPU segment violation                                                                                                                                                                                              | VMAIFG<br>JMBNIFG, JMBOUTIFG<br>CBDIFG, UBDIFG<br>MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>(SYSSNIV) <sup>(1) (3)</sup>                                                                                                                            | (Non)maskable    | 0FFFCh       |          |
| <b>User NMI</b><br>External NMI<br>Oscillator Fault                                                                                                                                                                                                                                                         | NMIFG, OFIFG<br>(SYSUNIV) <sup>(1) (3)</sup>                                                                                                                                                                                                    | (Non)maskable    | 0FFFAh       |          |
| Comparator_E                                                                                                                                                                                                                                                                                                | Comparator_E interrupt flags (CEIV) <sup>(1)</sup>                                                                                                                                                                                              | Maskable         | 0FFF8h       |          |
| Timer_B TB0                                                                                                                                                                                                                                                                                                 | TB0CCR0.CCIFG                                                                                                                                                                                                                                   | Maskable         | 0FFF6h       |          |
| Timer_B TB0                                                                                                                                                                                                                                                                                                 | TB0CCR1.CCIFG to TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV) <sup>(1)</sup>                                                                                                                                                                             | Maskable         | 0FFF4h       |          |
| Watchdog Timer (Interval Timer Mode)                                                                                                                                                                                                                                                                        | WDTIFG                                                                                                                                                                                                                                          | Maskable         | 0FFF2h       |          |
| Reserved                                                                                                                                                                                                                                                                                                    | Reserved                                                                                                                                                                                                                                        | Maskable         | 0FFF0h       |          |
| eUSCI_A0 Receive or Transmit                                                                                                                                                                                                                                                                                | UCA0IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCA0IFG: UCSTTIFG, UCTXPTIFG, UCRXIFG, UCTXIFG (UART mode)<br>(UCA0IV) <sup>(1)</sup>                                                                                                                   | Maskable         | 0FFEEh       |          |
| eUSCI_B0 Receive or Transmit                                                                                                                                                                                                                                                                                | UCB0IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode)<br>(UCB0IV) <sup>(1)</sup> | Maskable         | 0FFEC h      |          |
| ADC12_B                                                                                                                                                                                                                                                                                                     | ADC12IFG0 to ADC12IFG31<br>ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC12OVIFG, ADC12TOVIFG<br>(ADC12IV) <sup>(1) (4)</sup>                                                                                                             | Maskable         | 0FFEAh       |          |
| Timer_A TA0                                                                                                                                                                                                                                                                                                 | TA0CCR0.CCIFG                                                                                                                                                                                                                                   | Maskable         | 0FFE8h       |          |
| Timer_A TA0                                                                                                                                                                                                                                                                                                 | TA0CCR1.CCIFG to TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV) <sup>(1)</sup>                                                                                                                                                                             | Maskable         | 0FFE6h       |          |
| eUSCI_A1 receive or transmit                                                                                                                                                                                                                                                                                | UCA1IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCA1IFG: UCSTTIFG, UCTXPTIFG, UCRXIFG, UCTXIFG (UART mode)<br>(UCA1IV) <sup>(1)</sup>                                                                                                                   | Maskable         | 0FFE4h       |          |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space

(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(4) Only on devices with ADC, otherwise reserved.

**表 6-4. Interrupt Sources, Flags, Vectors, and Signatures (continued)**

| INTERRUPT SOURCE                                           | INTERRUPT FLAG                                                                                                                                                                                                                                           | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|----------|
| eUSCI_B1 receive or transmit<br>(Reserved on MSP430FR592x) | UCB1IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG,<br>UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1,<br>UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3,<br>UCTXIFG3, UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode)<br>(UCB1IV) <sup>(1)</sup> | Maskable         | 0FFE2h       |          |
| DMA                                                        | DMA0CTL.DMAIFG, DMA1CTL.DMAIFG,<br>DMA2CTL.DMAIFG<br>(DMAIV) <sup>(1)</sup>                                                                                                                                                                              | Maskable         | 0FFE0h       |          |
| Timer_A TA1                                                | TA1CCR0.CCIFG                                                                                                                                                                                                                                            | Maskable         | 0FFDEh       |          |
| Timer_A TA1                                                | TA1CCR1.CCIFG to TA1CCR2.CCIFG,<br>TA1CTL.TAIFG<br>(TA1IV) <sup>(1)</sup>                                                                                                                                                                                | Maskable         | 0FFDCh       |          |
| I/O Port P1                                                | P1IFG.0 to P1IFG.7<br>(P1IV) <sup>(1)</sup>                                                                                                                                                                                                              | Maskable         | 0FFDAh       |          |
| Timer_A TA2                                                | TA2CCR0.CCIFG                                                                                                                                                                                                                                            | Maskable         | 0FFD8h       |          |
| Timer_A TA2                                                | TA2CCR1.CCIFG<br>TA2CTL.TAIFG<br>(TA2IV) <sup>(1)</sup>                                                                                                                                                                                                  | Maskable         | 0FFD6h       |          |
| I/O Port P2                                                | P2IFG.0 to P2IFG.3<br>(P2IV) <sup>(1)</sup>                                                                                                                                                                                                              | Maskable         | 0FFD4h       |          |
| Timer_A TA3                                                | TA3CCR0.CCIFG                                                                                                                                                                                                                                            | Maskable         | 0FFD2h       |          |
| Timer_A TA3                                                | TA3CCR1.CCIFG<br>TA3CTL.TAIFG<br>(TA3IV) <sup>(1)</sup>                                                                                                                                                                                                  | Maskable         | 0FFD0h       |          |
| I/O Port P3                                                | P3IFG.0 to P3IFG.7<br>(P3IV) <sup>(1)</sup>                                                                                                                                                                                                              | Maskable         | 0FFCEh       |          |
| I/O Port P4                                                | P4IFG.2 to P4IFG.7<br>(P4IV) <sup>(1)</sup>                                                                                                                                                                                                              | Maskable         | 0FFCCh       |          |
| Reserved                                                   |                                                                                                                                                                                                                                                          |                  | 0FFCAh       |          |
| RTC_C                                                      | RTCRDYIFG, RTCTEVIFG, RTCAIFG,<br>RT0PSIFG, RT1PSIFG, RTCOFIFG<br>(RTCIV) <sup>(1)</sup>                                                                                                                                                                 | Maskable         | 0FFC8h       |          |
| AES                                                        | AESRDYIFG                                                                                                                                                                                                                                                | Maskable         | 0FFC6h       | Lowest   |
| Reserved                                                   | Reserved <sup>(5)</sup>                                                                                                                                                                                                                                  |                  | 0FFC4h       |          |
|                                                            |                                                                                                                                                                                                                                                          |                  | ⋮            |          |
|                                                            |                                                                                                                                                                                                                                                          |                  | 0FF8Ch       |          |
| Signatures <sup>(6)</sup>                                  | IP Encapsulation Signature2 <sup>(5)</sup>                                                                                                                                                                                                               |                  | 0FF8Ah       |          |
|                                                            | IP Encapsulation Signature1 <sup>(5) (7)</sup>                                                                                                                                                                                                           |                  | 0FF88h       |          |
|                                                            | BSL Signature2                                                                                                                                                                                                                                           |                  | 0FF86h       |          |
|                                                            | BSL Signature1                                                                                                                                                                                                                                           |                  | 0FF84h       |          |
|                                                            | JTAG Signature2                                                                                                                                                                                                                                          |                  | 0FF82h       |          |
|                                                            | JTAG Signature1                                                                                                                                                                                                                                          |                  | 0FF80h       |          |

(5) May contain a JTAG password required to enable JTAG access to the device.

(6) Signatures are evaluated during device start-up. See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#) for details.

(7) Must not contain 0AAAAh if used as JTAG password.

## 6.5 Bootloader (BSL)

The BSL enables programming of the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I<sup>2</sup>C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins as shown in 表 6-5. BSL entry requires a specific entry sequence on the  $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$  and  $\text{TEST}/\text{SBWTCK}$  pins. For complete description of the features of the BSL and its implementation, see [MSP430 FRAM Device Bootloader \(BSL\) User's Guide](#).

**表 6-5. BSL Pin Requirements and Functions**

| DEVICE SIGNAL                                     | BSL FUNCTION                                       |
|---------------------------------------------------|----------------------------------------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal                              |
| $\text{TEST}/\text{SBWTCK}$                       | Entry sequence signal                              |
| BSL_TX                                            | Devices with UART BSL (FRxxxx): Data transmit      |
| BSL_RX                                            | Devices with UART BSL (FRxxxx): Data receive       |
| BSL_DAT                                           | Devices with I <sup>2</sup> C BSL (FRxxxx1): Data  |
| BSL_CLK                                           | Devices with I <sup>2</sup> C BSL (FRxxxx1): Clock |
| VCC                                               | Power supply                                       |
| VSS                                               | Ground supply                                      |

## 6.6 JTAG Operation

### 6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The  $\text{TEST}/\text{SBWTCK}$  pin is used to enable the JTAG signals. In addition to these signals, the  $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$  is required to interface with MSP430 development tools and device programmers. 表 6-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**表 6-6. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL                                     | DIRECTION | FUNCTION                    |
|---------------------------------------------------|-----------|-----------------------------|
| PJ.3/TCK                                          | IN        | JTAG clock input            |
| PJ.2/TMS                                          | IN        | JTAG state control          |
| PJ.1/TDI/TCLK                                     | IN        | JTAG data input, TCLK input |
| PJ.0/TDO                                          | OUT       | JTAG data output            |
| $\text{TEST}/\text{SBWTCK}$                       | IN        | Enable JTAG pins            |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN        | External reset              |
| VCC                                               |           | Power supply                |
| VSS                                               |           | Ground supply               |

### 6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#).

**表 6-7. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL  | DIRECTION | FUNCTION                      |
|----------------|-----------|-------------------------------|
| TEST/SBWTCK    | IN        | Spy-Bi-Wire clock input       |
| RST/NMI/SBWDIO | IN, OUT   | Spy-Bi-Wire data input/output |
| VCC            |           | Power supply                  |
| VSS            |           | Ground supply                 |

## 6.7 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait-state generation
- Error correction coding (ECC)

### 注

#### Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "Wait State Control" section of the "FRAM Controller (FRCTRL)" chapter in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see [MSP430™ FRAM Technology – How To and Best Practices](#)

## 6.8 RAM

The RAM is made up of one sector. The sector can be completely powered down in LPM3 and LPM4 to save leakage; however, all data is lost during shutdown.

## 6.9 Tiny RAM

Twenty-six bytes of Tiny RAM are provided in addition to the complete RAM (see [表 6-36](#)). This memory is always available even in LPM3 and LPM4, while the complete RAM can be powered down in LPM3 and LPM4. Tiny RAM can be used to hold data or a very small stack when the complete RAM is powered down in LPM3 and LPM4. Tiny RAM is not available in LPMx.5.

## 6.10 Memory Protection Unit (MPU) Including IP Encapsulation

The FRAM can be protected by the MPU from inadvertent CPU execution and read or write access. Features of the MPU include:

- IP encapsulation with programmable boundaries (prevents reads from "outside" like JTAG or non-IP software) in steps of 1KB.
- Main memory partitioning that can be configured in up to three segments in steps of 1KB.
- The access rights for each main and information memory segment can be individually selected.
- Access violation flags with interrupt capability for easy servicing of access violations.

## 6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

### 6.11.1 Digital I/O

There are up to nine 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all pins of ports P1 to P4.
- Read and write access to port control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive touch functionality is supported on all pins of ports P1 to P7, P9, and PJ.

#### 注

##### Configuration of Digital I/Os After BOR Reset

To prevent any cross-currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details see the "Digital I/O" chapter, section "Configuration After Reset" in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

### 6.11.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal DCO, a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

### 6.11.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes the supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a safe level. SVS circuitry is available on the primary and core supplies.

### 6.11.4 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.11.5 Real-Time Clock (RTC\_C)

The RTC\_C module contains an integrated real-time clock (RTC) with the following features implemented:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates for months with fewer than 31 days and includes leap year correction. The RTC\_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

### 6.11.6 Watchdog Timer (WDT\_A)

The primary function of the WDT\_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-8 lists the clocks that the WDT\_A module can use.

**表 6-8. WDT\_A Clocks**

| WDTSEL | NORMAL OPERATION<br>(WATCHDOG AND INTERVAL TIMER MODE) |
|--------|--------------------------------------------------------|
| 00     | SMCLK                                                  |
| 01     | ACLK                                                   |
| 10     | VLOCLK                                                 |
| 11     | LFMODOSC                                               |

### 6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These system functions include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). Also included is a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application. 表 6-9 lists the SYS module interrupt vector registers.

**表 6-9. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT                                           | VALUE      | PRIORITY |
|---------------------------|---------|-----------------------------------------------------------|------------|----------|
| SYSRSTIV, System Reset    | 019Eh   | No interrupt pending                                      | 00h        |          |
|                           |         | Brownout (BOR)                                            | 02h        | Highest  |
|                           |         | RSTIFG $\overline{\text{RST}}$ /NMI (BOR)                 | 04h        |          |
|                           |         | PMMSWBOR software BOR (BOR)                               | 06h        |          |
|                           |         | LPmX.5 wakeup (BOR)                                       | 08h        |          |
|                           |         | Security violation (BOR)                                  | 0Ah        |          |
|                           |         | Reserved                                                  | 0Ch        |          |
|                           |         | SVSHIFG SVSH event (BOR)                                  | 0Eh        |          |
|                           |         | Reserved                                                  | 10h        |          |
|                           |         | Reserved                                                  | 12h        |          |
|                           |         | PMMSWPOR software POR (POR)                               | 14h        |          |
|                           |         | WDTIFG watchdog time-out (PUC)                            | 16h        |          |
|                           |         | WDTPW password violation (PUC)                            | 18h        |          |
|                           |         | FRCTLPW password violation (PUC)                          | 1Ah        |          |
|                           |         | Uncorrectable FRAM bit error detection (PUC)              | 1Ch        |          |
|                           |         | Peripheral area fetch (PUC)                               | 1Eh        |          |
|                           |         | PMMPW PMM password violation (PUC)                        | 20h        |          |
|                           |         | MPUPW MPU password violation (PUC)                        | 22h        |          |
|                           |         | CSPW CS password violation (PUC)                          | 24h        |          |
|                           |         | MPUSEGPIFG encapsulated IP memory segment violation (PUC) | 26h        |          |
|                           |         | MPUSEGIIFG information memory segment violation (PUC)     | 28h        |          |
|                           |         | MPUSEG1IFG segment 1 memory violation (PUC)               | 2Ah        |          |
|                           |         | MPUSEG2IFG segment 2 memory violation (PUC)               | 2Ch        |          |
|                           |         | MPUSEG3IFG segment 3 memory violation (PUC)               | 2Eh        |          |
|                           |         | ACCTEIFG access time error (PUC)                          | 30h        |          |
|                           |         | Reserved                                                  | 32h to 3Eh | Lowest   |
| SYSSNIV, System NMI       | 019Ch   | No interrupt pending                                      | 00h        |          |
|                           |         | Reserved                                                  | 02h        | Highest  |
|                           |         | Uncorrectable FRAM bit error detection                    | 04h        |          |
|                           |         | Reserved                                                  | 06h        |          |
|                           |         | MPUSEGPIFG encapsulated IP memory segment violation       | 08h        |          |
|                           |         | MPUSEGIIFG information memory segment violation           | 0Ah        |          |
|                           |         | MPUSEG1IFG segment 1 memory violation                     | 0Ch        |          |
|                           |         | MPUSEG2IFG segment 2 memory violation                     | 0Eh        |          |
|                           |         | MPUSEG3IFG segment 3 memory violation                     | 10h        |          |
|                           |         | VMAIFG vacant memory access                               | 12h        |          |
|                           |         | JMBINIFG JTAG mailbox input                               | 14h        |          |
|                           |         | JMBOUTIFG JTAG mailbox output                             | 16h        |          |
|                           |         | Correctable FRAM bit error detection                      | 18h        |          |
|                           |         | Reserved                                                  | 1Ah to 1Eh | Lowest   |
| SYSUNIV, User NMI         | 019Ah   | No interrupt pending                                      | 00h        |          |
|                           |         | NMIIFG NMI pin                                            | 02h        | Highest  |
|                           |         | OFIFG oscillator fault                                    | 04h        |          |
|                           |         | Reserved                                                  | 06h        |          |
|                           |         | Reserved                                                  | 08h        |          |
|                           |         | Reserved                                                  | 0Ah to 1Eh | Lowest   |

### 6.11.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12\_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-10 lists the available DMA triggers.

**表 6-10. DMA Trigger Assignments <sup>(1)</sup>**

| TRIGGER | CHANNEL 0                                        | CHANNEL 1                                        | CHANNEL 2                                        |
|---------|--------------------------------------------------|--------------------------------------------------|--------------------------------------------------|
| 0       | DMAREQ                                           | DMAREQ                                           | DMAREQ                                           |
| 1       | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    | TA0CCR0 CCIFG                                    |
| 2       | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    | TA0CCR2 CCIFG                                    |
| 3       | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    | TA1CCR0 CCIFG                                    |
| 4       | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    | TA1CCR2 CCIFG                                    |
| 5       | TA2 CCR0 CCIFG                                   | TA2 CCR0 CCIFG                                   | TA2 CCR0 CCIFG                                   |
| 6       | TA3 CCR0 CCIFG                                   | TA3 CCR0 CCIFG                                   | TA3 CCR0 CCIFG                                   |
| 7       | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    | TB0CCR0 CCIFG                                    |
| 8       | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    | TB0CCR2 CCIFG                                    |
| 9       | Reserved                                         | Reserved                                         | Reserved                                         |
| 10      | Reserved                                         | Reserved                                         | Reserved                                         |
| 11      | AES Trigger 0 <sup>(2)</sup>                     | AES Trigger 0 <sup>(2)</sup>                     | AES Trigger 0 <sup>(2)</sup>                     |
| 12      | AES Trigger 1 <sup>(2)</sup>                     | AES Trigger 1 <sup>(2)</sup>                     | AES Trigger 1 <sup>(2)</sup>                     |
| 13      | AES Trigger 2 <sup>(2)</sup>                     | AES Trigger 2 <sup>(2)</sup>                     | AES Trigger 2 <sup>(2)</sup>                     |
| 14      | UCA0RXIFG                                        | UCA0RXIFG                                        | UCA0RXIFG                                        |
| 15      | UCA0TXIFG                                        | UCA0TXIFG                                        | UCA0TXIFG                                        |
| 16      | UCA1RXIFG                                        | UCA1RXIFG                                        | UCA1RXIFG                                        |
| 17      | UCA1TXIFG                                        | UCA1TXIFG                                        | UCA1TXIFG                                        |
| 18      | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 (I <sup>2</sup> C) |
| 19      | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 (I <sup>2</sup> C) |
| 20      | UCB0RXIFG1 (I <sup>2</sup> C)                    | UCB0RXIFG1 (I <sup>2</sup> C)                    | UCB0RXIFG1 (I <sup>2</sup> C)                    |
| 21      | UCB0TXIFG1 (I <sup>2</sup> C)                    | UCB0TXIFG1 (I <sup>2</sup> C)                    | UCB0TXIFG1 (I <sup>2</sup> C)                    |
| 22      | UCB0RXIFG2 (I <sup>2</sup> C)                    | UCB0RXIFG2 (I <sup>2</sup> C)                    | UCB0RXIFG2 (I <sup>2</sup> C)                    |
| 23      | UCB0TXIFG2 (I <sup>2</sup> C)                    | UCB0TXIFG2 (I <sup>2</sup> C)                    | UCB0TXIFG2 (I <sup>2</sup> C)                    |
| 24      | UCB1RXIFG (SPI)<br>UCB1RXIFG0 (I <sup>2</sup> C) | UCB1RXIFG (SPI)<br>UCB1RXIFG0 (I <sup>2</sup> C) | UCB1RXIFG (SPI)<br>UCB1RXIFG0 (I <sup>2</sup> C) |
| 25      | UCB1TXIFG (SPI)<br>UCB1TXIFG0 (I <sup>2</sup> C) | UCB1TXIFG (SPI)<br>UCB1TXIFG0 (I <sup>2</sup> C) | UCB1TXIFG (SPI)<br>UCB1TXIFG0 (I <sup>2</sup> C) |
| 26      | ADC12 end of conversion <sup>(3)</sup>           | ADC12 end of conversion <sup>(3)</sup>           | ADC12 end of conversion <sup>(3)</sup>           |
| 27      | Reserved                                         | Reserved                                         | Reserved                                         |
| 28      | Reserved                                         | Reserved                                         | Reserved                                         |
| 29      | MPY ready                                        | MPY ready                                        | MPY ready                                        |
| 30      | DMA2IFG                                          | DMA0IFG                                          | DMA1IFG                                          |
| 31      | DMAE0                                            | DMAE0                                            | DMAE0                                            |

(1) If a reserved trigger source is selected, no trigger is generated.

(2) Only on devices with AES. Reserved on devices without AES.

(3) Only on devices with ADC. Reserved on devices without ADC.

### 6.11.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I<sup>2</sup>C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI\_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI\_Bn module provides support for SPI (3 or 4 pin) and I<sup>2</sup>C.

Two eUSCI\_A modules and two eUSCI\_B modules are implemented.

### 6.11.10 Timer\_A TA0, Timer\_A TA1

TA0 and TA1 are 16-bit timers/counters (Timer\_A type) with three capture/compare registers each. TA0 and TA1 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-11 and 表 6-12). TA0 and TA1 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-11. Timer\_A TA0 Signal Connections**

| INPUT PORT PIN       | DEVICE INPUT SIGNAL         | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                    |
|----------------------|-----------------------------|---------------------|--------------|----------------------|----------------------|----------------------------------------------------|
| P1.2 or P7.0         | TA0CLK                      | TACLK               | Timer        | N/A                  | N/A                  |                                                    |
|                      | ACLK (internal)             | ACLK                |              |                      |                      |                                                    |
|                      | SMCLK (internal)            | SMCLK               |              |                      |                      |                                                    |
| P1.2 or P7.0         | $\overline{\text{TA0CLK}}$  | INCLK               |              |                      |                      |                                                    |
| P1.5                 | TA0.0                       | CCI0A               | CCR0         | TA0                  | TA0.0                | P1.5                                               |
| P7.1                 | TA0.0                       | CCI0B               |              |                      |                      | P7.1                                               |
|                      | DV <sub>SS</sub>            | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>            | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P1.0 or P1.6 or P7.2 | TA0.1                       | CCI1A               | CCR1         | TA1                  | TA0.1                | P1.0                                               |
|                      | COU <sub>T</sub> (internal) | CCI1B               |              |                      |                      | P1.6                                               |
|                      | DV <sub>SS</sub>            | GND                 |              |                      |                      | P7.2                                               |
|                      | DV <sub>CC</sub>            | V <sub>CC</sub>     |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {1} |
| P1.1 or P1.7 or P7.3 | TA0.2                       | CCI2A               | CCR2         | TA2                  | TA0.2                | P1.1                                               |
|                      | ACLK (internal)             | CCI2B               |              |                      |                      | P1.7                                               |
|                      | DV <sub>SS</sub>            | GND                 |              |                      |                      | P7.3                                               |
|                      | DV <sub>CC</sub>            | V <sub>CC</sub>     |              |                      |                      |                                                    |

(1) Only on devices with ADC

**表 6-12. Timer\_A TA1 Signal Connections**

| INPUT PORT PIN       | DEVICE INPUT SIGNAL        | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                    |
|----------------------|----------------------------|---------------------|--------------|----------------------|----------------------|----------------------------------------------------|
| P1.1 or P4.4         | TA1CLK                     | TACLK               | Timer        | N/A                  | N/A                  |                                                    |
|                      | ACLK (internal)            | ACLK                |              |                      |                      |                                                    |
|                      | SMCLK (internal)           | SMCLK               |              |                      |                      |                                                    |
| P1.1 or P4.4         | $\overline{\text{TA1CLK}}$ | INCLK               |              |                      |                      |                                                    |
| P1.4 or P4.5         | TA1.0                      | CCI0A               | CCR0         | TA0                  | TA1.0                | P1.4                                               |
|                      | DV <sub>SS</sub>           | CCI0B               |              |                      |                      | P4.5                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P1.2 or P3.3 or P4.6 | TA1.1                      | CCI1A               | CCR1         | TA1                  | TA1.1                | P1.2                                               |
|                      | COUT (internal)            | CCI1B               |              |                      |                      | P4.6                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      | P3.3                                               |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {4} |
| P1.3 or P4.7         | TA1.2                      | CCI2A               | CCR2         | TA2                  | TA1.2                | P1.3                                               |
|                      | ACLK (internal)            | CCI2B               |              |                      |                      | P4.7                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |

(1) Only on devices with ADC

#### 6.11.11 Timer\_A TA2

TA2 is a 16-bit timer/counter (Timer\_A type) with two capture/compare registers each and with internal connections only. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-13). TA2 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-13. Timer\_A TA2 Signal Connections**

| DEVICE INPUT SIGNAL                    | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL                               |
|----------------------------------------|-------------------|--------------|----------------------|----------------------------------------------------|
| COUT (internal)                        | TACLK             | Timer        | N/A                  |                                                    |
| ACLK (internal)                        | ACLK              |              |                      |                                                    |
| SMCLK (internal)                       | SMCLK             |              |                      |                                                    |
| From Capacitive Touch I/O 0 (internal) | INCLK             |              |                      |                                                    |
| TA3 CCR0 output (internal)             | CCI0A             | CCR0         | TA0                  | TA3 CCI0A input                                    |
| ACLK (internal)                        | CCI0B             |              |                      |                                                    |
| DV <sub>SS</sub>                       | GND               |              |                      |                                                    |
| DV <sub>CC</sub>                       | V <sub>CC</sub>   |              |                      |                                                    |
| From Capacitive Touch I/O 0 (internal) | CCI1A             | CCR1         | TA1                  | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {5} |
| COUT (internal)                        | CCI1B             |              |                      |                                                    |
| DV <sub>SS</sub>                       | GND               |              |                      |                                                    |
| DV <sub>CC</sub>                       | V <sub>CC</sub>   |              |                      |                                                    |

(1) Only on devices with ADC

### 6.11.12 Timer\_A TA3

TA3 is a 16-bit timer/counter (Timer\_A type) with five capture/compare registers each and with internal connections only. TA3 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-14](#)). TA3 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-14. Timer\_A TA3 Signal Connections**

| DEVICE INPUT SIGNAL                                 | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL                                            |
|-----------------------------------------------------|-------------------|--------------|----------------------|-----------------------------------------------------------------|
| COUT (internal)                                     | TACLK             | Timer        | N/A                  |                                                                 |
| ACLK (internal)                                     | ACLK              |              |                      |                                                                 |
| SMCLK (internal)                                    | SMCLK             |              |                      |                                                                 |
| From Capacitive Touch I/O 1 (internal)              | INCLK             |              |                      |                                                                 |
| TA2 CCR0 output (internal)                          | CCI0A             | CCR0         | TA0                  | TA2 CCI0A input                                                 |
| ACLK (internal)                                     | CCI0B             |              |                      |                                                                 |
| DV <sub>SS</sub>                                    | GND               |              |                      |                                                                 |
| DV <sub>CC</sub>                                    | V <sub>CC</sub>   |              |                      |                                                                 |
| From Capacitive Touch I/O 1 (internal)              | CCI1A             | CCR1         | TA1                  | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {6}              |
| COUT (internal)                                     | CCI1B             |              |                      |                                                                 |
| DV <sub>SS</sub>                                    | GND               |              |                      |                                                                 |
| DV <sub>CC</sub>                                    | V <sub>CC</sub>   |              |                      |                                                                 |
| DV <sub>SS</sub>                                    | CCI2A             | CCR2         | TA2                  |                                                                 |
| P3.0<br>DV <sub>SS</sub> (FR592x(1) 64-pin package) | CCI2B             |              |                      | P3.0 (Note: Not available for FR592x(1) 64-pin package devices) |
| DV <sub>SS</sub>                                    | GND               |              |                      |                                                                 |
| DV <sub>CC</sub>                                    | V <sub>CC</sub>   |              |                      |                                                                 |
| DV <sub>SS</sub>                                    | CCI3A             | CCR3         | TA3                  |                                                                 |
| P3.1<br>DV <sub>SS</sub> (FR592x(1) 64-pin package) | CCI3B             |              |                      | P3.1 (Note: Not available for FR592x(1) 64-pin package devices) |
| DV <sub>SS</sub>                                    | GND               |              |                      |                                                                 |
| DV <sub>CC</sub>                                    | V <sub>CC</sub>   |              |                      |                                                                 |
| DV <sub>SS</sub>                                    | CCI4A             | CCR4         | TA4                  |                                                                 |
| P3.2<br>DV <sub>SS</sub> (FR592x(1) 64-pin package) | CCI4B             |              |                      | P3.2 (Note: Not available for FR592x(1) 64-pin package devices) |
| DV <sub>SS</sub>                                    | GND               |              |                      |                                                                 |
| DV <sub>CC</sub>                                    | V <sub>CC</sub>   |              |                      |                                                                 |

(1) Only on devices with ADC.

### 6.11.13 Timer\_B TB0

TB0 is a 16-bit timer/counter (Timer\_B type) with seven capture/compare registers each. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-15). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-15. Timer\_B TB0 Signal Connections**

| INPUT PORT PIN       | DEVICE INPUT SIGNAL        | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN                                    |
|----------------------|----------------------------|---------------------|--------------|----------------------|----------------------|----------------------------------------------------|
| P2.0 or P3.3 or P5.7 | TB0CLK                     | TBCLK               | Timer        | N/A                  | N/A                  |                                                    |
|                      | ACLK (internal)            | ACLK                |              |                      |                      |                                                    |
|                      | SMCLK (internal)           | SMCLK               |              |                      |                      |                                                    |
| P2.0 or P3.3 or P5.7 | $\overline{\text{TB0CLK}}$ | INCLK               | CCR0         | TB0                  | TB0.0                |                                                    |
| P3.4                 | TB0.0                      | CCI0A               |              |                      |                      | P3.4                                               |
| P6.4                 | TB0.0                      | CCI0B               |              |                      |                      | P6.4                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {2} |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.5 or P6.5         | TB0.1                      | CCI1A               | CCR1         | TB1                  | TB0.1                | P3.5                                               |
|                      | COUT (internal)            | CCI1B               |              |                      |                      | P6.5                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      | ADC12 (internal) <sup>(1)</sup><br>ADC12SHSx = {3} |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
| P3.6 or P6.6         | TB0.2                      | CCI2A               | CCR2         | TB2                  | TB0.2                | P3.6                                               |
|                      | ACLK (internal)            | CCI2B               |              |                      |                      | P6.6                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
|                      | DV <sub>SS</sub>           | CCI3A               | CCR3         | TB3                  | TB0.3                |                                                    |
| P3.7                 | TB0.3                      | CCI3B               |              |                      |                      | P3.7                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
|                      | DV <sub>SS</sub>           | CCI4A               | CCR4         | TB4                  | TB0.4                |                                                    |
| P2.2                 | TB0.4                      | CCI4B               |              |                      |                      | P2.2                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
|                      | DV <sub>SS</sub>           | CCI5A               | CCR5         | TB5                  | TB0.5                |                                                    |
| P2.1                 | TB0.5                      | CCI5B               |              |                      |                      | P2.1                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |
|                      | DV <sub>SS</sub>           | CCI6A               | CCR6         | TB6                  | TB0.6                |                                                    |
| P2.0                 | TB0.6                      | CCI6B               |              |                      |                      | P2.0                                               |
|                      | DV <sub>SS</sub>           | GND                 |              |                      |                      |                                                    |
|                      | DV <sub>CC</sub>           | V <sub>CC</sub>     |              |                      |                      |                                                    |

(1) Only on devices with ADC

### 6.11.14 ADC12\_B

The ADC12\_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-16 summarizes the available external trigger sources.

表 6-17 lists the available multiplexing between internal and external analog inputs.

**表 6-16. ADC12\_B Trigger Signal Connections**

| ADC12SHSx |         | CONNECTED TRIGGER SOURCE |
|-----------|---------|--------------------------|
| BINARY    | DECIMAL |                          |
| 000       | 0       | Software (ADC12SC)       |
| 001       | 1       | Timer_A TA0 CCR1 output  |
| 010       | 2       | Timer_B TB0 CCR0 output  |
| 011       | 3       | Timer_B TB0 CCR1 output  |
| 100       | 4       | Timer_A TA1 CCR1 output  |
| 101       | 5       | Timer_A TA2 CCR1 output  |
| 110       | 6       | Timer_A TA3 CCR1 output  |
| 111       | 7       | Reserved (DVSS)          |

**表 6-17. ADC12\_B External and Internal Signal Mapping**

| CONTROL BIT | EXTERNAL<br>(CONTROL BIT = 0) | INTERNAL<br>(CONTROL BIT = 1) |
|-------------|-------------------------------|-------------------------------|
| ADC12BATMAP | A31                           | Battery monitor               |
| ADC12TCMAP  | A30                           | Temperature sensor            |
| ADC12CH0MAP | A29                           | N/A <sup>(1)</sup>            |
| ADC12CH1MAP | A28                           | N/A <sup>(1)</sup>            |
| ADC12CH2MAP | A27                           | N/A <sup>(1)</sup>            |
| ADC12CH3MAP | A26                           | N/A <sup>(1)</sup>            |

(1) N/A: No internal signal available on this device.

### 6.11.15 Comparator\_E

The primary function of the Comparator\_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 6.11.16 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 signature is based on the CRC-CCITT standard.

### 6.11.17 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard.

### 6.11.18 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the advanced encryption standard (AES) (FIPS PUB 197) in hardware.

### 6.11.19 True Random Seed

The Device Descriptor Info (TLV) (see [6.12](#)) contains a 128-bit true random seed that can be used to implement a deterministic random-number generator.

### 6.11.20 Shared Reference (REF\_A)

The REF\_A module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

### 6.11.21 Embedded Emulation

#### 6.11.21.1 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

#### 6.11.21.2 EnergyTrace++ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology lets you observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.
- COMP is on.
- AES is encrypting or decrypting.
- eUSCI\_A0 is transferring (receiving or transmitting) data.
- eUSCI\_A1 is transferring (receiving or transmitting) data.
- eUSCI\_B0 is transferring (receiving or transmitting) data.
- eUSCI\_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.

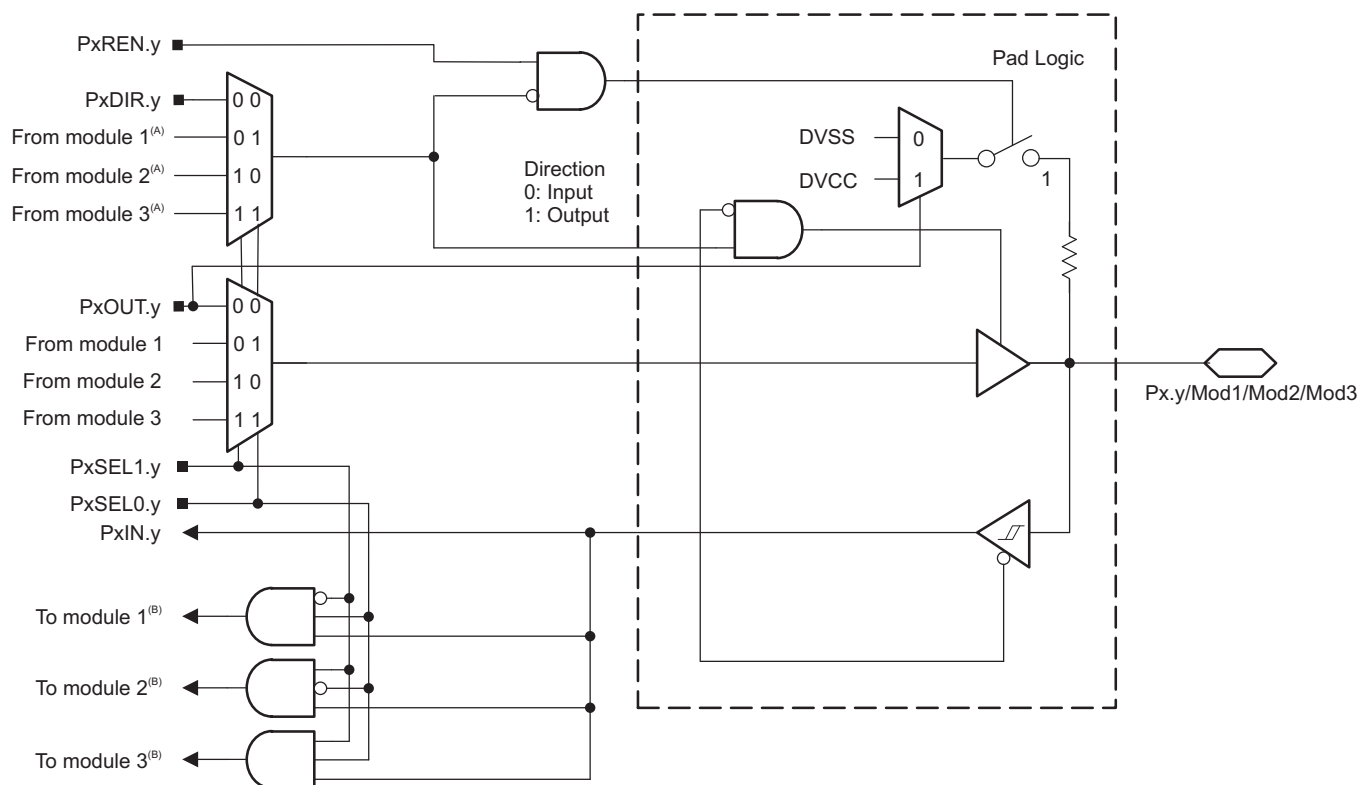
## 6.11.22 Input/Output Diagrams

### 6.11.22.1 Digital I/O Functionality Port P1 to P7 and P9

The port pins provide the following features:

- Interrupt and wakeup from LPMx.5 capability for ports P1 to P4
- Capacitive touch functionality (see 6.11.22.2)
- Up to three digital module input and/or output functions

Figure 6-1 shows the features and the corresponding control logic (besides the Capacitive Touch logic). Figure 6-1 is applicable for all port pins P1.0 to P9.7, unless a dedicated diagram is available in the following sections. The module functions provided per pin and whether the direction is controlled by the module or by the port direction register for the selected secondary function are described in the following pin function tables.



A. The direction is either controlled by connected module or by the corresponding PxDIR.y bit. See pin function tables.

B. The inputs from several pins towards a module are ORed together.

NOTE: Functional representation only.

**Figure 6-1. General Port Pin Diagram**

### 6.11.22.2 Capacitive Touch Functionality on Port P1 to P7, P9, and PJ

Figure 6-2 shows the capacitive touch functionality that is available on all port pins. The capacitive touch functionality is controlled using the capacitive touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the [MSP430FR58xx](#), [MSP430FR59xx](#), [MSP430FR68xx](#), and [MSP430FR69xx Family User's Guide](#). The capacitive touch functionality is not shown in the other pin diagrams.

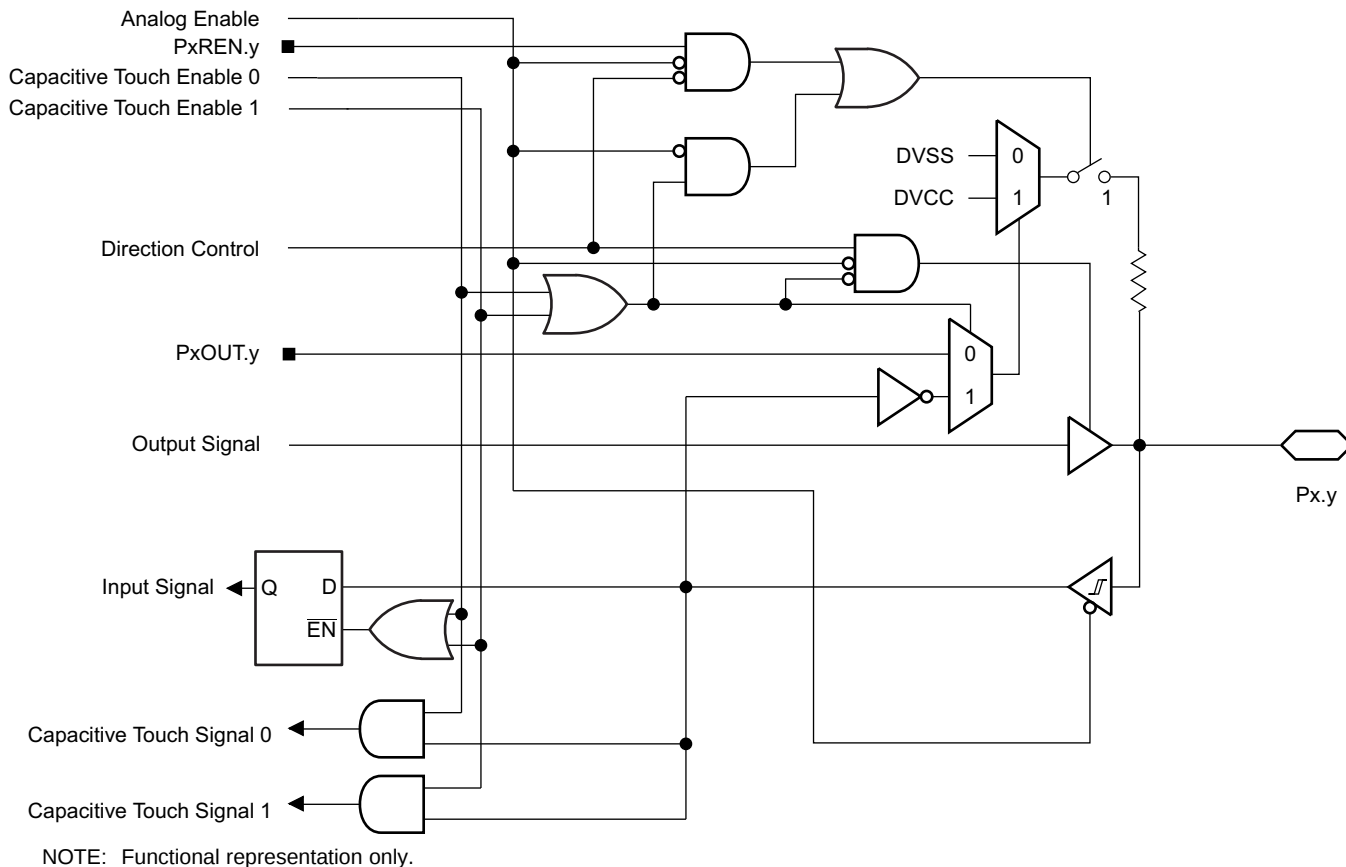
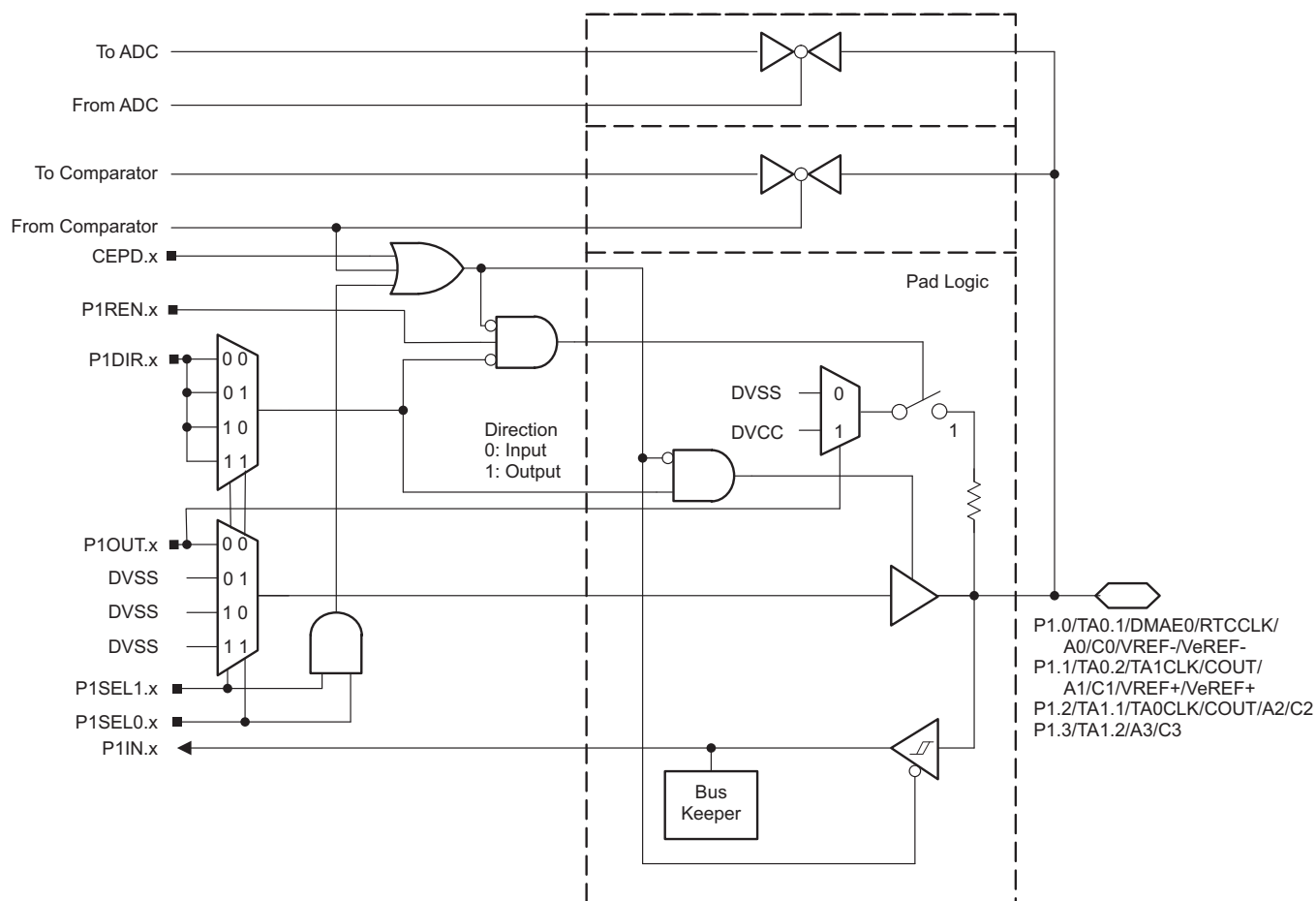


Figure 6-2. Capacitive Touch I/O Functionality

### 6.11.22.3 Port P1 (P1.0 to P1.3) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-18 summarizes the selection of the pin functions.



NOTE: Functional representation only.

Figure 6-3. Port P1 (P1.0 to P1.3) Diagram

**表 6-18. Port P1 (P1.0 to P1.3) Pin Functions**

| PIN NAME (P1.x)                                | x | FUNCTION                                 | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|------------------------------------------------|---|------------------------------------------|----------------------------------------|----------|----------|
|                                                |   |                                          | P1DIR.x                                | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/<br>VREF-/VeREF- | 0 | P1.0 (I/O)                               | I: 0; O: 1                             | 0        | 0        |
|                                                |   | TA0.CCI1A                                | 0                                      | 0        | 1        |
|                                                |   | TA0.1                                    | 1                                      |          |          |
|                                                |   | DMAE0                                    | 0                                      | 1        | 0        |
|                                                |   | RTCCLK <sup>(2)</sup>                    | 1                                      |          |          |
|                                                |   | A0, C0, VREF-, VeREF- <sup>(3) (4)</sup> | X                                      | 1        | 1        |
| P1.1/TA0.2/TA1CLK/COUT/A1/C1/<br>VREF+/VeREF+  | 1 | P1.1 (I/O)                               | I: 0; O: 1                             | 0        | 0        |
|                                                |   | TA0.CCI2A                                | 0                                      | 0        | 1        |
|                                                |   | TA0.2                                    | 1                                      |          |          |
|                                                |   | TA1CLK                                   | 0                                      | 1        | 0        |
|                                                |   | COUT <sup>(5)</sup>                      | 1                                      |          |          |
|                                                |   | A1, C1, VREF+, VeREF+ <sup>(3) (4)</sup> | X                                      | 1        | 1        |
| P1.2/TA1.1/TA0CLK/COUT/A2/C2                   | 2 | P1.2 (I/O)                               | I: 0; O: 1                             | 0        | 0        |
|                                                |   | TA1.CCI1A                                | 0                                      | 0        | 1        |
|                                                |   | TA1.1                                    | 1                                      |          |          |
|                                                |   | TA0CLK                                   | 0                                      | 1        | 0        |
|                                                |   | COUT <sup>(5)</sup>                      | 1                                      |          |          |
|                                                |   | A2, C2 <sup>(3) (4)</sup>                | X                                      | 1        | 1        |
| P1.3/TA1.2/A3/C3                               | 3 | P1.3 (I/O)                               | I: 0; O: 1                             | 0        | 0        |
|                                                |   | TA1.CCI2A                                | 0                                      | 0        | 1        |
|                                                |   | TA1.2                                    | 1                                      |          |          |
|                                                |   | N/A                                      | 0                                      | 1        | 0        |
|                                                |   | Internally tied to DVSS                  | 1                                      |          |          |
|                                                |   | A3, C3 <sup>(3) (4)</sup>                | X                                      | 1        | 1        |

- (1) X = Don't care
- (2) Do not use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternative RTCCLK output pin.
- (3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
- (5) Do not use this pin as COUT output if the TA1CLK functionality is used on any other pin. Select an alternative COUT output pin.

#### 6.11.22.4 Port P1 (P1.4 to P1.7) Input/Output With Schmitt Trigger

For the port diagram, see [Figure 6-1](#). [Table 6-19](#) summarizes the selection of the pin functions.

**表 6-19. Port P1 (P1.4 to P1.7) Pin Functions**

| PIN NAME (P1.x)             | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------|---|-------------------------|----------------------------------------|----------|----------|
|                             |   |                         | P1DIR.x                                | P1SEL1.x | P1SEL0.x |
| P1.4/UCB0CLK/UCA0STE/TA1.0  | 4 | P1.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCB0CLK                 | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | UCA0STE                 | X <sup>(3)</sup>                       | 1        | 0        |
|                             |   | TA1.CCI0A               | 0                                      | 1        | 1        |
|                             |   | TA1.0                   | 1                                      |          |          |
| P1.5/UCB0STE/UCA0CLK/TA0.0  | 5 | P1.5 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCB0STE                 | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | UCA0CLK                 | X <sup>(3)</sup>                       | 1        | 0        |
|                             |   | TA0.CCI0A               | 0                                      | 1        | 1        |
|                             |   | TA0.0                   | 1                                      |          |          |
| P1.6/UCB0SIMO/UCB0SDA/TA0.1 | 6 | P1.6 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCB0SIMO/UCB0SDA        | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | N/A                     | 0                                      | 1        | 0        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | TA0.CCI1A               | 0                                      | 1        | 1        |
|                             |   | TA0.1                   | 1                                      |          |          |
| P1.7/UCB0SOMI/UCB0SCL/TA0.2 | 7 | P1.7 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCB0SOMI/UCB0SCL        | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | N/A                     | 0                                      | 1        | 0        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | TA0.CCI2A               | 0                                      | 1        | 1        |
|                             |   | TA0.2                   | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B0 module.

(3) Direction controlled by eUSCI\_A0 module.

### 6.11.22.5 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

For the port diagram, see [Figure 6-1](#). [Table 6-20](#) summarizes the selection of the pin functions.

**表 6-20. Port P2 (P2.0 to P2.3) Pin Functions**

| PIN NAME (P2.x)                    | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|------------------------------------|---|-------------------------|----------------------------------------|----------|----------|
|                                    |   |                         | P2DIR.x                                | P2SEL1.x | P2SEL0.x |
| P2.0/UCA0SIMO/UCA0TXD/TB0.6/TB0CLK | 0 | P2.0 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                                    |   | UCA0SIMO/UCA0TXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                                    |   | TB0.CCI6B               | 0                                      | 1        | 0        |
|                                    |   | TB0.6                   | 1                                      |          |          |
|                                    |   | TB0CLK                  | 0                                      | 1        | 1        |
|                                    |   | Internally tied to DVSS | 1                                      |          |          |
| P2.1/UCA0SOMI/UCA0RXD/TB0.5/DMAE0  | 1 | P2.1 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                                    |   | UCA0SOMI/UCA0RXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                                    |   | TB0.CCI5B               | 0                                      | 1        | 0        |
|                                    |   | TB0.5                   | 1                                      |          |          |
|                                    |   | DMA0E                   | 0                                      | 1        | 1        |
|                                    |   | Internally tied to DVSS | 1                                      |          |          |
| P2.2/UCA0CLK/TB0.4/RTCCLK          | 2 | P2.2 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                                    |   | UCA0CLK                 | X <sup>(2)</sup>                       | 0        | 1        |
|                                    |   | TB0.CCI4B               | 0                                      | 1        | 0        |
|                                    |   | TB0.4                   | 1                                      |          |          |
|                                    |   | N/A                     | 0                                      | 1        | 1        |
|                                    |   | RTCCLK                  | 1                                      |          |          |
| P2.3/UCA0STE/TB0OUTH               | 3 | P2.3 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                                    |   | UCA0STE                 | X <sup>(2)</sup>                       | 0        | 1        |
|                                    |   | TB0OUTH                 | 0                                      | 1        | 0        |
|                                    |   | Internally tied to DVSS | 1                                      |          |          |
|                                    |   | N/A                     | 0                                      | 1        | 1        |
|                                    |   | Internally tied to DVSS | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A0 module.

## 6.11.22.6 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

For the port diagram, see [Figure 6-1](#). [Table 6-21](#) and [Table 6-22](#) summarize the selection of the pin functions.

**Table 6-21. Port P3 (P3.0 to P3.3) Pin Functions**

| PIN NAME (P3.x)       | x | FUNCTION                                                                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------|---|-------------------------------------------------------------------------|----------------------------------------|----------|----------|
|                       |   |                                                                         | P3DIR.x                                | P3SEL1.x | P3SEL0.x |
| P3.0/UCB1CLK          | 0 | P3.0 (I/O)                                                              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCB1CLK                                                                 | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | TA3.CCI2B (Note: not available for FR592x(1) 64-pin package devices)    | 0                                      | 1        | 0        |
|                       |   | TA3.2<br>Internally tied to DVSS (for FR292x(1) 64-pin package devices) | 1                                      |          |          |
|                       |   | N/A                                                                     | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS                                                 | 1                                      |          |          |
| P3.1/UCB1SIMO/UCB1SDA | 1 | P3.1 (I/O)                                                              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCB1SIMO/UCB1SDA                                                        | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | TA3.CCI3B (Note: not available for FR592x(1) 64-pin package devices)    | 0                                      | 1        | 0        |
|                       |   | TA3.3<br>Internally tied to DVSS (for FR592x(1) 64-pin package devices) | 1                                      |          |          |
|                       |   | N/A                                                                     | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS                                                 | 1                                      |          |          |
| P3.2/UCB1SOMI/UCB1SCL | 2 | P3.2 (I/O)                                                              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCB1SOMI/UCB1SCL                                                        | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | TA3.CCI4B (Note: not available for FR592x(1) 64-pin package devices)    | 0                                      | 1        | 0        |
|                       |   | TA3.4<br>Internally tied to DVSS (for FR592x(1) 64-pin package devices) | 1                                      |          |          |
|                       |   |                                                                         | 0                                      | 1        | 1        |
|                       |   |                                                                         | 1                                      |          |          |
| P3.3/TA1.1/TB0CLK     | 3 | P3.3 (I/O)                                                              | I: 0; O: 1                             | 0        | 0        |
|                       |   | N/A                                                                     | 0                                      | 0        | 1        |
|                       |   | Internally tied to DVSS                                                 | 1                                      |          |          |
|                       |   | TA1.CCI1A                                                               | 0                                      | 1        | 0        |
|                       |   | TA1.1                                                                   | 1                                      |          |          |
|                       |   | TB0CLK                                                                  | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS                                                 | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B1 module.

**表 6-22. Port P3 (P3.4 to P3.7) Pin Functions**

| PIN NAME (P3.x)             | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------|---|-------------------------|----------------------------------------|----------|----------|
|                             |   |                         | P3DIR.x                                | P3SEL1.x | P3SEL0.x |
| P3.4/UCA1SIMO/UCA1TXD/TB0.0 | 4 | P3.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCA1SIMO/UCA1TXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | TB0CCI0A                | 0                                      | 1        | 0        |
|                             |   | TB0.0                   | 1                                      |          |          |
|                             |   | N/A                     | 0                                      | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
| P3.5/UCA1SOMI/UCA1RXD/TB0.1 | 5 | P3.5 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCA1SOMI/UCA1RXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | TB0CCI1A                | 0                                      | 1        | 0        |
|                             |   | TB0.1                   | 1                                      |          |          |
|                             |   | N/A                     | 0                                      | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
| P3.6/UCA1CLK/TB0.2          | 6 | P3.6 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCA1CLK                 | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | TB0CCI2A                | 0                                      | 1        | 0        |
|                             |   | TB0.2                   | 1                                      |          |          |
|                             |   | N/A                     | 0                                      | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
| P3.7/UCA1STE/TB0.3          | 7 | P3.7 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | UCA1STE                 | X <sup>(2)</sup>                       | 0        | 1        |
|                             |   | TB0CCI3B                | 0                                      | 1        | 0        |
|                             |   | TB0.3                   | 1                                      |          |          |
|                             |   | N/A                     | 0                                      | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A1 module.

### 6.11.22.7 Port P4 (P4.2 to P4.7) Input/Output With Schmitt Trigger

For the port diagram, see [Figure 6-1](#). [Table 6-23](#) and [Table 6-24](#) summarize the selection of the pin functions.

**Table 6-23. Port P4 (P4.2 and P4.3) Pin Functions**

| PIN NAME (P4.x)               | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-------------------------------|---|-------------------------|----------------------------------------|----------|----------|
|                               |   |                         | P4DIR.x                                | P4SEL1.x | P4SEL0.x |
| P4.2/UCA0SIMO/UCA0TXD/UCB1CLK | 2 | P4.2 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                               |   | UCA0SIMO/UCA0TXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                               |   | UCB1CLK                 | X <sup>(3)</sup>                       | 1        | 0        |
|                               |   | N/A                     | 0                                      | 1        | 1        |
|                               |   | Internally tied to DVSS | 1                                      |          |          |
| P4.3/UCA0SOMI/UCA0RXD/UCB1STE | 3 | P4.3 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                               |   | UCA0SOMI/UCA0RXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                               |   | UCB1STE                 | X <sup>(3)</sup>                       | 1        | 0        |
|                               |   | N/A                     | 0                                      | 1        | 1        |
|                               |   | Internally tied to DVSS | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A0 module.

(3) Direction controlled by eUSCI\_B1 module.

**表 6-24. Port P4 (P4.4 to P4.7) Pin Functions**

| PIN NAME (P4.x)             | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------|---|-------------------------|----------------------------------------|----------|----------|
|                             |   |                         | P4DIR.x                                | P4SEL1.x | P4SEL0.x |
| P4.4/UCB1STE/TA1CLK         | 4 | P4.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | N/A                     | 0                                      | 0        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | UCB1STE                 | X <sup>(2)</sup>                       | 1        | 0        |
|                             |   | TA1CLK                  | 0                                      | 1        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
| P4.5/UCB1CLK/TA1.0          | 5 | P4.5 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | N/A                     | 0                                      | 0        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | UCB1CLK                 | X <sup>(2)</sup>                       | 1        | 0        |
|                             |   | TA1CCI0A                | 0                                      | 1        | 1        |
|                             |   | TA1.0                   | 1                                      |          |          |
| P4.6/UCB1SIMO/UCB1SDA/TA1.1 | 6 | P4.6 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | N/A                     | 0                                      | 0        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | UCB1SIMO/UCB1SDA        | X <sup>(2)</sup>                       | 1        | 0        |
|                             |   | TA1CCI1A                | 0                                      | 1        | 1        |
|                             |   | TA1.1                   | 1                                      |          |          |
| P4.7/UCB1SOMI/UCB1SCL/TA1.2 | 7 | P4.7 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                             |   | N/A                     | 0                                      | 0        | 1        |
|                             |   | Internally tied to DVSS | 1                                      |          |          |
|                             |   | UCB1SOMI/UCB1SCL        | X <sup>(2)</sup>                       | 1        | 0        |
|                             |   | TA1CCI2A                | 0                                      | 1        | 1        |
|                             |   | TA1.2                   | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_B1 module.

## 6.11.22.8 Port P5 (P5.4 to P5.7) Input/Output With Schmitt Trigger

For the port diagram, see [Figure 6-1](#). [Table 6-25](#) summarizes the selection of the pin functions.

**表 6-25. Port P5 (P5.4 to P5.7) Pin Functions**

| PIN NAME (P5.x)       | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------|---|-------------------------|----------------------------------------|----------|----------|
|                       |   |                         | P5DIR.x                                | P5SEL1.x | P5SEL0.x |
| P5.4/UCA1SIMO/UCA1TXD | 4 | P5.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCA1SIMO/UCA1TXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | N/A                     | 0                                      | 1        | 0        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
|                       |   | N/A                     | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
| P5.5/UCA1SOMI/UCA1RXD | 5 | P5.5 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCA1SOMI/UCA1RXD        | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | N/A                     | 0                                      | 1        | 0        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
|                       |   | N/A                     | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
| P5.6/UCA1CLK          | 6 | P5.6 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCA1CLK                 | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | N/A                     | 0                                      | 1        | 0        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
|                       |   | N/A                     | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
| P5.7/UCA1STE/TB0CLK   | 7 | P5.7 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                       |   | UCA1STE                 | X <sup>(2)</sup>                       | 0        | 1        |
|                       |   | N/A                     | 0                                      | 1        | 0        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |
|                       |   | TB0CLK                  | 0                                      | 1        | 1        |
|                       |   | Internally tied to DVSS | 1                                      |          |          |

(1) X = Don't care

(2) Direction controlled by eUSCI\_A1 module.



**表 6-26. Port P6 (P6.0 to P6.2) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|----------------------------------------|----------|----------|
|                 |   |                         | P6DIR.x                                | P6SEL1.x | P6SEL0.x |
| P6.0            | 0 | P6.0 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                     | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |
| P6.1            | 1 | P6.1 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                     | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |
| P6.2/COUT       | 2 | P6.2 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                     | 0                                      | 0        | 1        |
|                 |   | COUT                    | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |

(1) X = Don't care

**表 6-27. Port P6 (P6.3 to P6.6) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|----------------------------------------|----------|----------|
|                 |   |                         | P6DIR.x                                | P6SEL1.x | P6SEL0.x |
| P6.3            | 3 | P6.3 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                     | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |
| P6.4/TB0.0      | 4 | P6.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TB0CCI0B                | 0                                      | 0        | 1        |
|                 |   | TB0.0                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |
| P6.5/TB0.1      | 5 | P6.5 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TB0CCI1A                | 0                                      | 0        | 1        |
|                 |   | TB0.1                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |
| P6.6/TB0.2      | 6 | P6.6 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TB0CCI2A                | 0                                      | 0        | 1        |
|                 |   | TB0.2                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | X                                      | 1        | 1        |

(1) X = Don't care

**6.11.22.10 Port P7 (P7.0 to P7.4) Input/Output With Schmitt Trigger**

For the port diagram, see [Figure 6-1](#). [Table 6-28](#) and [Table 6-29](#) summarize the selection of the pin functions.

**Table 6-28. Port P7 (P7.0 to P7.3) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|----------------------------------------|----------|----------|
|                 |   |                         | P7DIR.x                                | P7SEL1.x | P7SEL0.x |
| P7.0/TA0CLK     | 0 | P7.0 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TA0CLK                  | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
| P7.1/TA0.0/ACLK | 1 | P7.1 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TA0CCI0B                | 0                                      | 0        | 1        |
|                 |   | TA0.0                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 1        |
|                 |   | ACLK                    | 1                                      |          |          |
| P7.2/TA0.1      | 2 | P7.2 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TA0CCI1A                | 0                                      | 0        | 1        |
|                 |   | TA0.1                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 1        |
|                 |   | N/A                     | 1                                      |          |          |
| P7.3/TA0.2      | 3 | P7.3 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | TA0CCI2A                | 0                                      | 0        | 1        |
|                 |   | TA0.2                   | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |

(1) X = Don't care

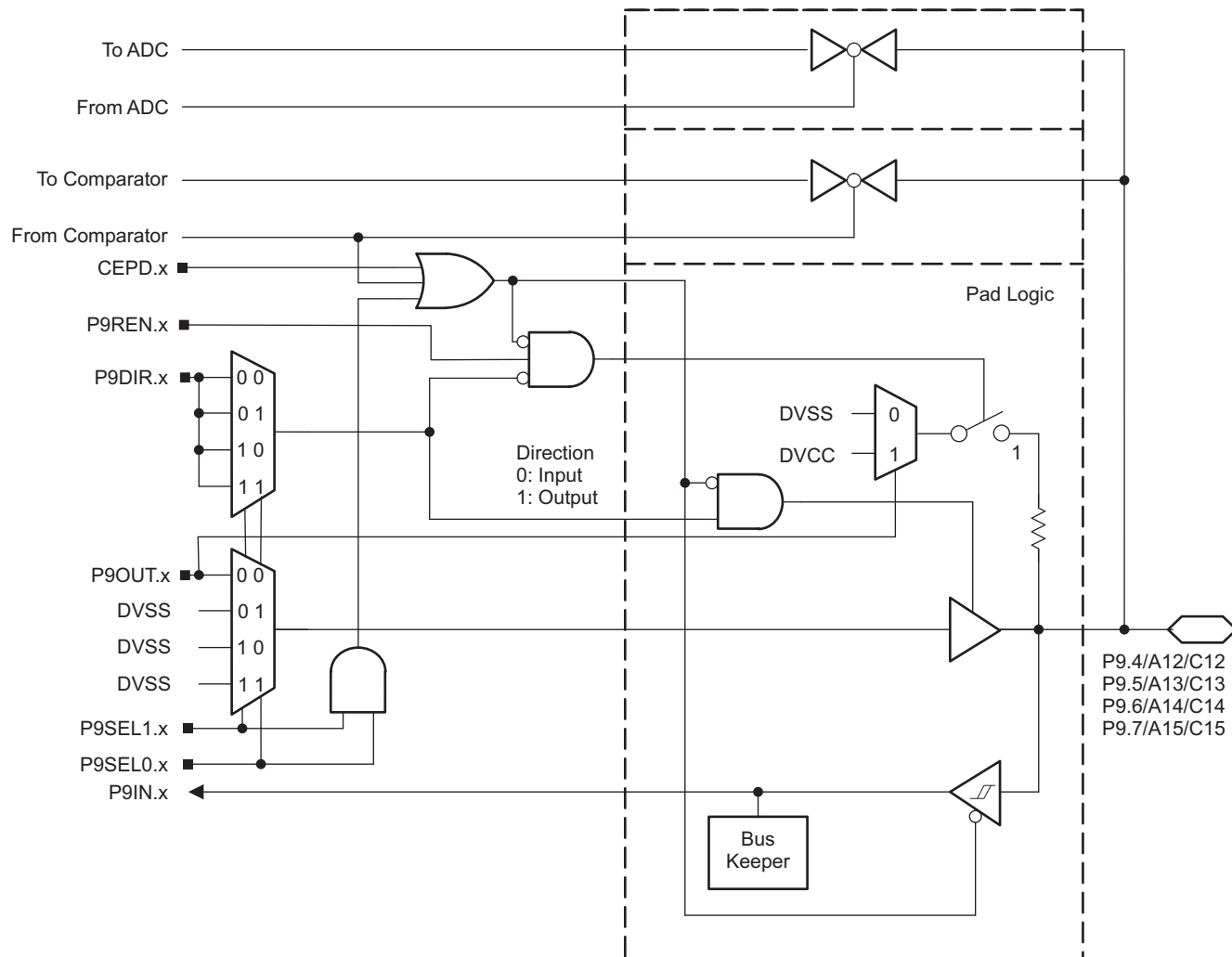
**Table 6-29. Port P7 (P7.4) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION                | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|-------------------------|----------------------------------------|----------|----------|
|                 |   |                         | P7DIR.x                                | P7SEL1.x | P7SEL0.x |
| P7.4/SMCLK      | 4 | P7.4 (I/O)              | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                     | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS | 1                                      |          |          |
|                 |   | N/A                     | 0                                      | 1        | 1        |
|                 |   | SMCLK                   | 1                                      |          |          |

(1) X = Don't care

### 6.11.22.11 Port P9 (P9.4 to P9.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-30 summarizes the selection of the pin functions.



NOTE: Functional representation only.

Figure 6-5. Port P9 (P9.4 to P9.7) Diagram

**表 6-30. Port P9 (P9.4 to P9.7) Pin Functions**

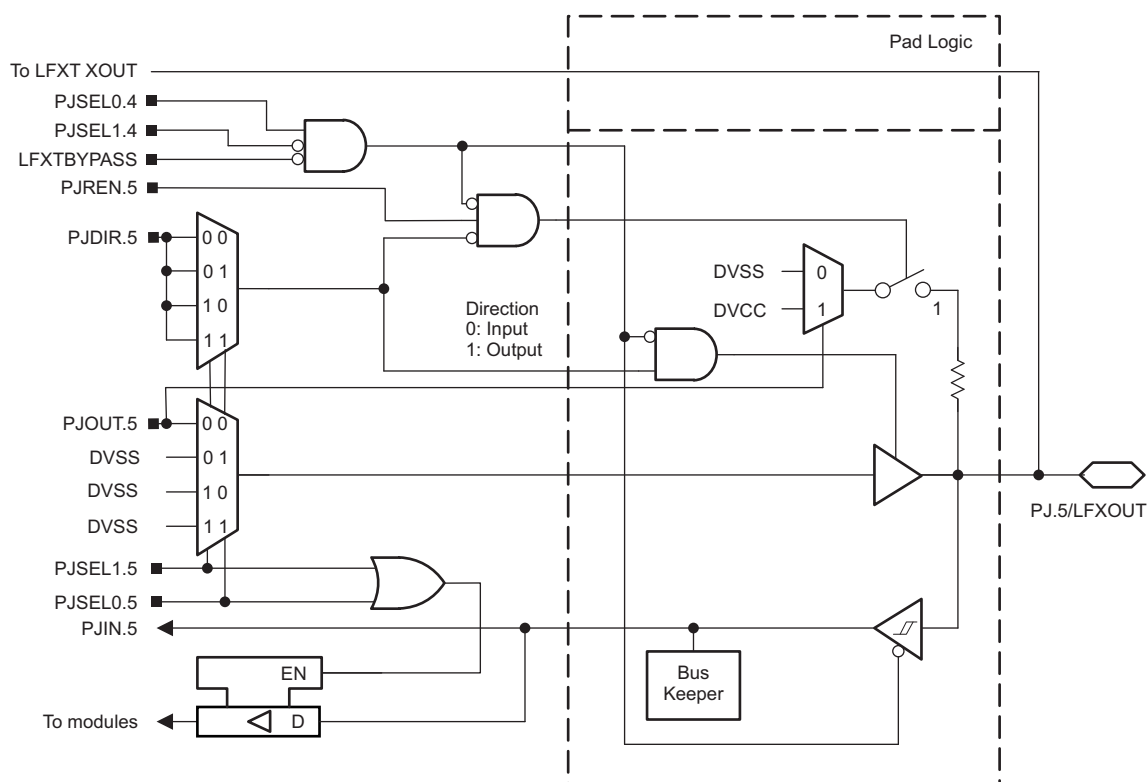
| PIN NAME (P9.x) | x | FUNCTION                   | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------|---|----------------------------|----------------------------------------|----------|----------|
|                 |   |                            | P9DIR.x                                | P9SEL1.x | P9SEL0.x |
| P9.4/A12/C12    | 4 | P9.4 (I/O)                 | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                        | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | N/A                        | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | A12/C12 <sup>(2) (3)</sup> | X                                      | 1        | 1        |
| P9.5/A13/C13    | 5 | P9.5 (I/O)                 | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                        | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | N/A                        | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | A13/C13 <sup>(2) (3)</sup> | X                                      | 1        | 1        |
| P9.6/A14/C14    | 6 | P9.6 (I/O)                 | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                        | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | N/A                        | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | A14/C14 <sup>(2) (3)</sup> | X                                      | 1        | 1        |
| P9.7/A15/C15    | 7 | P9.7 (I/O)                 | I: 0; O: 1                             | 0        | 0        |
|                 |   | N/A                        | 0                                      | 0        | 1        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | N/A                        | 0                                      | 1        | 0        |
|                 |   | Internally tied to DVSS    | 1                                      |          |          |
|                 |   | A15/C15 <sup>(2) (3)</sup> | X                                      | 1        | 1        |

(1) X = Don't care

(2) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.





NOTE: Functional representation only.

图 6-7. Port PJ (PJ.5) Diagram

**表 6-31. Port PJ (PJ.4 and PJ.5) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION                           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                    |                    |          |          |            |
|-----------------|---|------------------------------------|----------------------------------------|--------------------|--------------------|----------|----------|------------|
|                 |   |                                    | PJDIR.x                                | PJSEL1.5           | PJSEL0.5           | PJSEL1.4 | PJSEL0.4 | LFXTBYPASS |
| PJ.4/LFXIN      | 4 | PJ.4 (I/O)                         | I: 0; O: 1                             | X                  | X                  | 0        | 0        | X          |
|                 |   | N/A                                | 0                                      | X                  | X                  | 1        | X        | X          |
|                 |   | Internally tied to DVSS            | 1                                      |                    |                    |          |          |            |
|                 |   | LFXIN crystal mode <sup>(2)</sup>  | X                                      |                    |                    | 0        | 1        | 0          |
|                 |   | LFXIN bypass mode <sup>(2)</sup>   | X                                      | X                  | X                  | 0        | 1        | 1          |
| PJ.5/LFXOUT     | 5 | PJ.5 (I/O)                         | I: 0; O: 1                             | 0                  | 0                  | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | N/A                                | 0                                      | See <sup>(4)</sup> | See <sup>(4)</sup> | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | Internally tied to DVSS            | 1                                      | See <sup>(4)</sup> | See <sup>(4)</sup> | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | LFXOUT crystal mode <sup>(2)</sup> | X                                      | X                  | X                  | 0        | 1        | 0          |

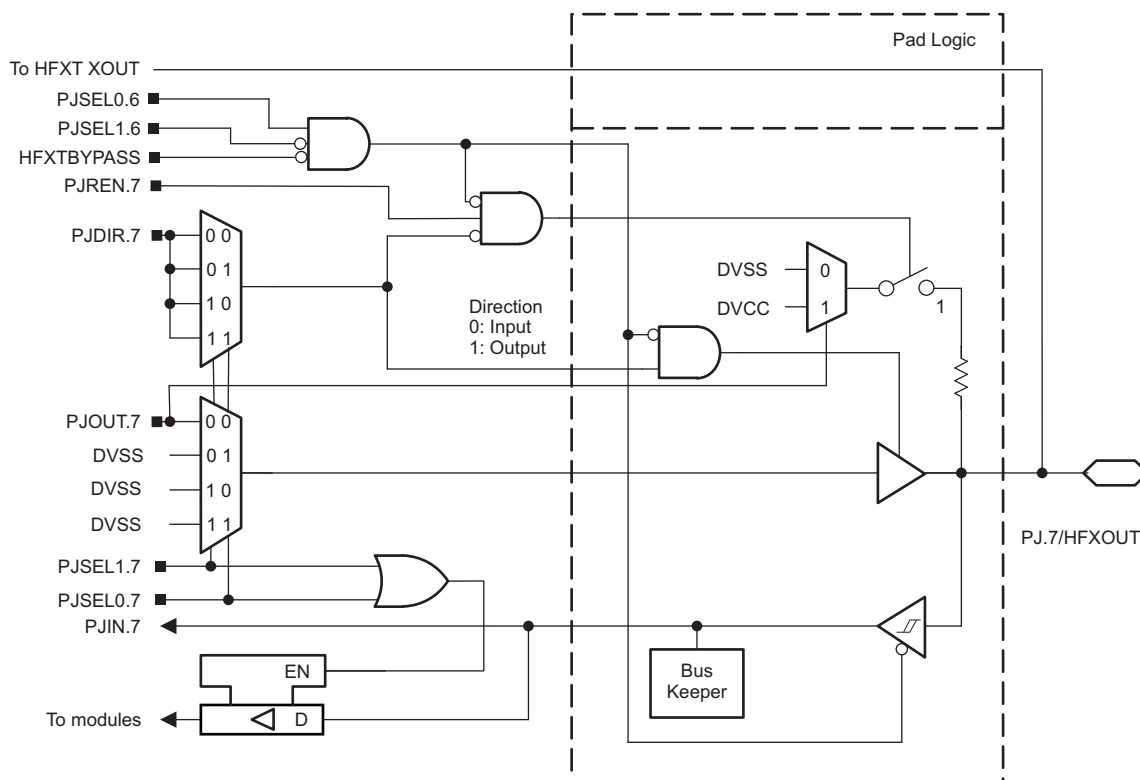
(1) X = Don't care

(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.

(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

(4) With PJSEL0.5 = 1 or PJSEL1.5 = 1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.





NOTE: Functional representation only.

图 6-9. Port PJ (PJ.7) Diagram

**表 6-32. Port PJ (PJ.6 and PJ.7) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION                           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                    |                    |          |          |            |
|-----------------|---|------------------------------------|----------------------------------------|--------------------|--------------------|----------|----------|------------|
|                 |   |                                    | PJDIR.x                                | PJSEL1.7           | PJSEL0.7           | PJSEL1.6 | PJSEL0.6 | HFXTBYPASS |
| PJ.6/HFXIN      | 6 | PJ.6 (I/O)                         | I: 0; O: 1                             | X                  | X                  | 0        | 0        | X          |
|                 |   | N/A                                | 0                                      | X                  | X                  | 1        | X        | X          |
|                 |   | Internally tied to DVSS            | 1                                      |                    |                    |          |          |            |
|                 |   | HFXIN crystal mode <sup>(2)</sup>  | X                                      | X                  | X                  | 0        | 1        | 0          |
|                 |   | HFXIN bypass mode <sup>(2)</sup>   | X                                      | X                  | X                  | 0        | 1        | 1          |
| PJ.7/HFXOUT     | 7 | PJ.7 (I/O)                         | I: 0; O: 1                             | 0                  | 0                  | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | N/A                                | 0                                      | See <sup>(4)</sup> | See <sup>(4)</sup> | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | Internally tied to DVSS            | 1                                      | See <sup>(4)</sup> | See <sup>(4)</sup> | 0        | 0        | 0          |
|                 |   |                                    |                                        |                    |                    | 1        | X        |            |
|                 |   |                                    |                                        |                    |                    | X        | X        |            |
|                 |   | HFXOUT crystal mode <sup>(2)</sup> | X                                      | X                  | X                  | 0        | 1        | 0          |

(1) X = Don't care

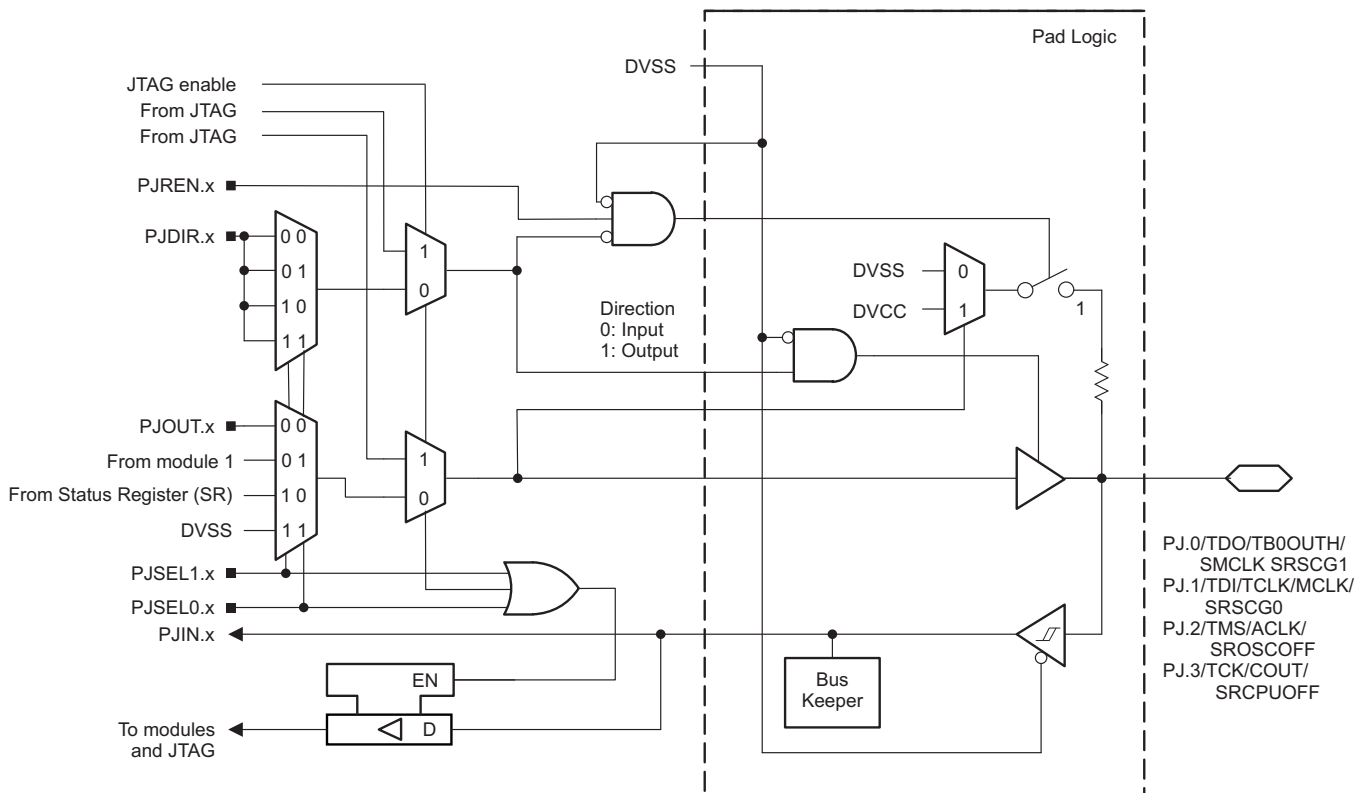
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are don't care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.

(3) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

(4) With PJSEL0.7 = 1 or PJSEL1.7 = 1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

#### 6.11.22.14 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-33 summarizes the selection of the pin functions.



NOTE: Functional representation only.

Figure 6-10. Port PJ (PJ.0 to PJ.3) Diagram

**表 6-33. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x)                   | x | FUNCTION                       | CONTROL BITS OR SIGNALS <sup>(1)</sup> |          |          |
|-----------------------------------|---|--------------------------------|----------------------------------------|----------|----------|
|                                   |   |                                | PJDIR.x                                | PJSEL1.x | PJSEL0.x |
| PJ.0/TDO/TB0OUTH/<br>SMCLK/SRSCG1 | 0 | PJ.0 (I/O) <sup>(2)</sup>      | I: 0; O: 1                             | 0        | 0        |
|                                   |   | TDO <sup>(3)</sup>             | X                                      | X        | X        |
|                                   |   | TB0OUTH                        | 0                                      | 0        | 1        |
|                                   |   | SMCLK <sup>(4)</sup>           | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 0        |
|                                   |   | CPU Status Register Bit SCG1   | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 1        |
|                                   |   | Internally tied to DVSS        | 1                                      |          |          |
| PJ.1/TDI/TCLK/MCLK/<br>SRSCG0     | 1 | PJ.1 (I/O) <sup>(2)</sup>      | I: 0; O: 1                             | 0        | 0        |
|                                   |   | TDI/TCLK <sup>(3) (5)</sup>    | X                                      | X        | X        |
|                                   |   | N/A                            | 0                                      | 0        | 1        |
|                                   |   | MCLK                           | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 0        |
|                                   |   | CPU Status Register Bit SCG0   | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 1        |
|                                   |   | Internally tied to DVSS        | 1                                      |          |          |
| PJ.2/TMS/ACLK/<br>SROSCOFF        | 2 | PJ.2 (I/O) <sup>(2)</sup>      | I: 0; O: 1                             | 0        | 0        |
|                                   |   | TMS <sup>(3) (5)</sup>         | X                                      | X        | X        |
|                                   |   | N/A                            | 0                                      | 0        | 1        |
|                                   |   | ACLK                           | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 0        |
|                                   |   | CPU Status Register Bit OSCOFF | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 1        |
|                                   |   | Internally tied to DVSS        | 1                                      |          |          |
| PJ.3/TCK/COUT/<br>SRCPUOFF        | 3 | PJ.3 (I/O) <sup>(2)</sup>      | I: 0; O: 1                             | 0        | 0        |
|                                   |   | TCK <sup>(3) (5)</sup>         | X                                      | X        | X        |
|                                   |   | N/A                            | 0                                      | 0        | 1        |
|                                   |   | COUT                           | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 0        |
|                                   |   | CPU Status Register Bit CPUOFF | 1                                      |          |          |
|                                   |   | N/A                            | 0                                      | 1        | 1        |
|                                   |   | Internally tied to DVSS        | 1                                      |          |          |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire 4-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPD.x bits have an effect in these cases.

(4) Do not use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternative SMCLK output pin.

(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

## 6.12 Device Descriptors (TLV)

表 6-34 summarizes the Device IDs. 表 6-35 list the contents of the device descriptor tag-length-value (TLV) structure.

**表 6-34. Device ID**

| DEVICE          | PACKAGE    | DEVICE ID |           |
|-----------------|------------|-----------|-----------|
|                 |            | At 01A05h | At 01A04h |
| MSP430FR5970    | PM and RGC | 82h       | 5Bh       |
| MSP430FR5972(1) | PM and RGC | 82h       | 5Dh       |
| MSP430FR5922(1) | PM and RGC | 82h       | 61h       |
|                 | DGG        | 82h       | 62h       |
| MSP430FR5870    | PM and RGC | 82h       | 5Eh       |
| MSP430FR5872(1) | PM and RGC | 82h       | 60h       |

**表 6-35. Device Descriptor Table <sup>(1)</sup>**

|            | DESCRIPTION       | MSP430FRxxxx (UART BSL) |             | MSP430FRxxxx1 (I <sup>2</sup> C BSL) |             |
|------------|-------------------|-------------------------|-------------|--------------------------------------|-------------|
|            |                   | ADDRESS                 | VALUE       | ADDRESS                              | VALUE       |
| Info Block | Info length       | 01A00h                  | 06h         | 01A00h                               | 06h         |
|            | CRC length        | 01A01h                  | 06h         | 01A01h                               | 06h         |
|            | CRC value         | 01A02h                  | Per unit    | 01A02h                               | Per unit    |
|            |                   | 01A03h                  | Per unit    | 01A03h                               | Per unit    |
|            | Device ID         | 01A04h                  | See 表 6-34. | 01A04h                               | See 表 6-34. |
|            | Device ID         | 01A05h                  |             | 01A05h                               |             |
|            | Hardware revision | 01A06h                  | Per unit    | 01A06h                               | Per unit    |
| Die Record | Firmware revision | 01A07h                  | Per unit    | 01A07h                               | Per unit    |
|            | Die record tag    | 01A08h                  | 08h         | 01A08h                               | 08h         |
|            | Die record length | 01A09h                  | 0Ah         | 01A09h                               | 0Ah         |
|            | Lot/wafer ID      | 01A0Ah                  | Per unit    | 01A0Ah                               | Per unit    |
|            |                   | 01A0Bh                  | Per unit    | 01A0Bh                               | Per unit    |
|            |                   | 01A0Ch                  | Per unit    | 01A0Ch                               | Per unit    |
|            |                   | 01A0Dh                  | Per unit    | 01A0Dh                               | Per unit    |
|            | Die X position    | 01A0Eh                  | Per unit    | 01A0Eh                               | Per unit    |
|            |                   | 01A0Fh                  | Per unit    | 01A0Fh                               | Per unit    |
|            | Die Y position    | 01A10h                  | Per unit    | 01A10h                               | Per unit    |
|            |                   | 01A11h                  | Per unit    | 01A11h                               | Per unit    |
|            | Test results      | 01A12h                  | Per unit    | 01A12h                               | Per unit    |
|            |                   | 01A13h                  | Per unit    | 01A13h                               | Per unit    |

(1) NA = Not applicable, Per unit = content can differ from device to device

表 6-35. Device Descriptor Table <sup>(1)</sup> (continued)

|                    | DESCRIPTION                                    | MSP430FRxxxx (UART BSL) |          | MSP430FRxxxx1 (I <sup>2</sup> C BSL) |          |
|--------------------|------------------------------------------------|-------------------------|----------|--------------------------------------|----------|
|                    |                                                | ADDRESS                 | VALUE    | ADDRESS                              | VALUE    |
| ADC12B Calibration | ADC12B calibration tag                         | 01A14h                  | 11h      | 01A14h                               | 11h      |
|                    | ADC12B calibration length                      | 01A15h                  | 10h      | 01A15h                               | 10h      |
|                    | ADC gain factor <sup>(2)</sup>                 | 01A16h                  | Per unit | 01A16h                               | Per unit |
|                    |                                                | 01A17h                  | Per unit | 01A17h                               | Per unit |
|                    | ADC offset <sup>(3)</sup>                      | 01A18h                  | Per unit | 01A18h                               | Per unit |
|                    |                                                | 01A19h                  | Per unit | 01A19h                               | Per unit |
|                    | ADC 1.2-V reference<br>Temperature sensor 30°C | 01A1Ah                  | Per unit | 01A1Ah                               | Per unit |
|                    |                                                | 01A1Bh                  | Per unit | 01A1Bh                               | Per unit |
|                    | ADC 1.2-V reference<br>Temperature sensor 85°C | 01A1Ch                  | Per unit | 01A1Ch                               | Per unit |
|                    |                                                | 01A1Dh                  | Per unit | 01A1Dh                               | Per unit |
|                    | ADC 2.0-V reference<br>Temperature sensor 30°C | 01A1Eh                  | Per unit | 01A1Eh                               | Per unit |
|                    |                                                | 01A1Fh                  | Per unit | 01A1Fh                               | Per unit |
|                    | ADC 2.0-V reference<br>Temperature sensor 85°C | 01A20h                  | Per unit | 01A20h                               | Per unit |
|                    |                                                | 01A21h                  | Per unit | 01A21h                               | Per unit |
| REF Calibration    | REF calibration tag                            | 01A22h                  | Per unit | 01A22h                               | Per unit |
|                    |                                                | 01A23h                  | Per unit | 01A23h                               | Per unit |
|                    | REF calibration length                         | 01A24h                  | Per unit | 01A24h                               | Per unit |
|                    |                                                | 01A25h                  | Per unit | 01A25h                               | Per unit |
|                    | REF 1.2-V reference                            | 01A26h                  | 12h      | 01A26h                               | 12h      |
|                    |                                                | 01A27h                  | 06h      | 01A27h                               | 06h      |
|                    | REF 2.0-V reference                            | 01A28h                  | Per unit | 01A28h                               | Per unit |
|                    |                                                | 01A29h                  | Per unit | 01A29h                               | Per unit |
|                    | REF 2.5-V reference                            | 01A2Ah                  | Per unit | 01A2Ah                               | Per unit |
|                    |                                                | 01A2Bh                  | Per unit | 01A2Bh                               | Per unit |
|                    | REF 2.5-V reference                            | 01A2Ch                  | Per unit | 01A2Ch                               | Per unit |
|                    |                                                | 01A2Dh                  | Per unit | 01A2Dh                               | Per unit |

(2) ADC gain: The gain correction factor is measured using the internal voltage reference with REFOUT = 0. Other settings (for example, with REFOUT = 1) can result in different correction factors.

(3) ADC offset: The offset correction factor is measured using the internal 2.5-V reference.

**表 6-35. Device Descriptor Table <sup>(4)</sup> (continued)**

|                   | DESCRIPTION                          | MSP430FRxxxx (UART BSL) |          | MSP430FRxxxx1 (I <sup>2</sup> C BSL) |          |
|-------------------|--------------------------------------|-------------------------|----------|--------------------------------------|----------|
|                   |                                      | ADDRESS                 | VALUE    | ADDRESS                              | VALUE    |
| Random Number     | 128-bit random number tag            | 01A2Eh                  | 15h      | 01A2Eh                               | 15h      |
|                   | Random number length                 | 01A2Fh                  | 10h      | 01A2Fh                               | 10h      |
|                   | 128-bit random number <sup>(4)</sup> | 01A30h                  | Per unit | 01A30h                               | Per unit |
|                   |                                      | 01A31h                  | Per unit | 01A31h                               | Per unit |
|                   |                                      | 01A32h                  | Per unit | 01A32h                               | Per unit |
|                   |                                      | 01A33h                  | Per unit | 01A33h                               | Per unit |
|                   |                                      | 01A34h                  | Per unit | 01A34h                               | Per unit |
|                   |                                      | 01A35h                  | Per unit | 01A35h                               | Per unit |
|                   |                                      | 01A36h                  | Per unit | 01A36h                               | Per unit |
|                   |                                      | 01A37h                  | Per unit | 01A37h                               | Per unit |
|                   |                                      | 01A38h                  | Per unit | 01A38h                               | Per unit |
|                   |                                      | 01A39h                  | Per unit | 01A39h                               | Per unit |
|                   |                                      | 01A3Ah                  | Per unit | 01A3Ah                               | Per unit |
|                   |                                      | 01A3Bh                  | Per unit | 01A3Bh                               | Per unit |
|                   |                                      | 01A3Ch                  | Per unit | 01A3Ch                               | Per unit |
|                   |                                      | 01A3Dh                  | Per unit | 01A3Dh                               | Per unit |
|                   |                                      | 01A3Eh                  | Per unit | 01A3Eh                               | Per unit |
|                   |                                      | 01A3Fh                  | Per unit | 01A3Fh                               | Per unit |
| BSL Configuration | BSL tag                              | 01A40h                  | 1Ch      | 01A40h                               | 1Ch      |
|                   | BSL length                           | 01A41h                  | 02h      | 01A41h                               | 02h      |
|                   | BSL interface                        | 01A42h                  | 00h      | 01A42h                               | 01h      |
|                   | BSL interface configuration          | 01A43h                  | 00h      | 01A43h                               | 48h      |

(4) 128-bit random number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

## 6.13 Memory

表 6-36 summarizes the memory map for all devices.

**表 6-36. Memory Organization<sup>(1)</sup>**

|                                                                                 |            | MSP430FR5972(1)<br>MSP430FR5922(1)<br>MSP430FR5872(1) | MSP430FR5970<br>MSP430FR5870                     |
|---------------------------------------------------------------------------------|------------|-------------------------------------------------------|--------------------------------------------------|
| Memory (FRAM)<br>Main: interrupt vectors and<br>signatures<br>Main: code memory | Total Size | 63KB<br>00FFFFh to 00FF80h<br>013FFFh to 004400h      | 32KB<br>00FFFFh to 00FF80h<br>00FF7Fh to 008000h |
| RAM                                                                             | Sect 1     | 2KB<br>0023FFh to 001C00h                             | 2KB<br>0023FFh to 001C00h                        |
| Device Descriptor Info (TLV)<br>(FRAM)                                          |            | 256 bytes<br>001AFFh to 001A00h                       | 256 bytes<br>001AFFh to 001A00h                  |
| Information memory (FRAM)                                                       | Info A     | 128 bytes<br>0019FFh to 001980h                       | 128 bytes<br>0019FFh to 001980h                  |
|                                                                                 | Info B     | 128 bytes<br>00197Fh to 001900h                       | 128 bytes<br>00197Fh to 001900h                  |
|                                                                                 | Info C     | 128 bytes<br>0018FFh to 001880h                       | 128 bytes<br>0018FFh to 001880h                  |
|                                                                                 | Info D     | 128 bytes<br>00187Fh to 001800h                       | 128 bytes<br>00187Fh to 001800h                  |
| Bootloader (BSL) memory (ROM)                                                   | BSL 3      | 512 bytes<br>0017FFh to 001600h                       | 512 bytes<br>0017FFh to 001600h                  |
|                                                                                 | BSL 2      | 512 bytes<br>0015FFh to 001400h                       | 512 bytes<br>0015FFh to 001400h                  |
|                                                                                 | BSL 1      | 512 bytes<br>0013FFh to 001200h                       | 512 bytes<br>0013FFh to 001200h                  |
|                                                                                 | BSL 0      | 512 bytes<br>0011FFh to 001000h                       | 512 bytes<br>0011FFh to 001000h                  |
| Peripherals                                                                     | Size       | 4KB<br>000FFFh to 000020h                             | 4KB<br>000FFFh to 000020h                        |
| Tiny RAM                                                                        | Size       | 26 bytes<br>000001Fh to 000006h                       | 26 bytes<br>000001Fh to 000006h                  |
| Reserved<br>(Read Only) <sup>(2)</sup>                                          | Size       | 6 bytes<br>000005h to 000000h                         | 6 bytes<br>000005h to 000000h                    |

(1) All address space not listed is considered vacant memory.

(2) Read as: D032h at 00h (Opcode: BIS.W LPM4, SR), 00F0h at 02h (Opcode: BIS.W LPM4, SR), 3FFFh at 04h (Opcode: JMP\$)

### 6.13.1 Peripheral File Map

表 6-37 lists the base address and offset range for the registers of supported peripheral modules.

**表 6-37. Peripherals**

| MODULE NAME                             | BASE ADDRESS | OFFSET ADDRESS RANGE |
|-----------------------------------------|--------------|----------------------|
| Special Functions (see 表 6-38)          | 0100h        | 000h to 01Fh         |
| PMM (see 表 6-39)                        | 0120h        | 000h to 01Fh         |
| FRAM Control (see 表 6-40)               | 0140h        | 000h to 00Fh         |
| CRC16 (see 表 6-41)                      | 0150h        | 000h to 007h         |
| RAM Controller (see 表 6-42)             | 0158h        | 000h to 001h         |
| Watchdog (see 表 6-43)                   | 015Ch        | 000h to 001h         |
| CS (see 表 6-44)                         | 0160h        | 000h to 00Fh         |
| SYS (see 表 6-45)                        | 0180h        | 000h to 01Fh         |
| Shared Reference (see 表 6-46)           | 01B0h        | 000h to 001h         |
| Port P1, P2 (see 表 6-47)                | 0200h        | 000h to 01Fh         |
| Port P3, P4 (see 表 6-48)                | 0220h        | 000h to 01Fh         |
| Port P5, P6 (see 表 6-49)                | 0240h        | 000h to 01Fh         |
| Port P7 (see 表 6-50)                    | 0260h        | 000h to 01Fh         |
| Port P9 (see 表 6-51)                    | 0280h        | 000h to 01Fh         |
| Port PJ (see 表 6-52)                    | 0320h        | 000h to 01Fh         |
| Timer_A TA0 (see 表 6-53)                | 0340h        | 000h to 02Fh         |
| Timer_A TA1 (see 表 6-54)                | 0380h        | 000h to 02Fh         |
| Timer_B TB0 (see 表 6-55)                | 03C0h        | 000h to 02Fh         |
| Timer_A TA2 (see 表 6-56)                | 0400h        | 000h to 02Fh         |
| Capacitive Touch I/O 0 (see 表 6-57)     | 0430h        | 000h to 00Fh         |
| Timer_A TA3 (see 表 6-58)                | 0440h        | 000h to 02Fh         |
| Capacitive Touch I/O 1 (see 表 6-59)     | 0470h        | 000h to 00Fh         |
| Real-Time Clock (RTC_C) (see 表 6-60)    | 04A0h        | 000h to 01Fh         |
| 32-Bit Hardware Multiplier (see 表 6-61) | 04C0h        | 000h to 02Fh         |
| DMA General Control (see 表 6-62)        | 0500h        | 000h to 00Fh         |
| DMA Channel 0 (see 表 6-62)              | 0510h        | 000h to 00Fh         |
| DMA Channel 1 (see 表 6-62)              | 0520h        | 000h to 00Fh         |
| DMA Channel 2 (see 表 6-62)              | 0530h        | 000h to 00Fh         |
| MPU Control (see 表 6-63)                | 05A0h        | 000h to 00Fh         |
| eUSCI_A0 (see 表 6-64)                   | 05C0h        | 000h to 01Fh         |
| eUSCI_A1 (see 表 6-65)                   | 05E0h        | 000h to 01Fh         |
| eUSCI_B0 (see 表 6-66)                   | 0640h        | 000h to 02Fh         |
| eUSCI_B1 (see 表 6-67)                   | 0680h        | 000h to 02Fh         |
| ADC12_B (see 表 6-68)                    | 0800h        | 000h to 09Fh         |
| Comparator_E (see 表 6-69)               | 08C0h        | 000h to 00Fh         |
| CRC32 (see 表 6-70)                      | 0980h        | 000h to 02Fh         |
| AES (see 表 6-71)                        | 09C0h        | 000h to 00Fh         |

**表 6-38. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable  | SFRIE1   | 00h    |
| SFR interrupt flag    | SFRIFG1  | 02h    |
| SFR reset pin control | SFRRPCR  | 04h    |

**表 6-39. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| PMM control 0        | PMMCTL0  | 00h    |
| PMM interrupt flags  | PMMIFG   | 0Ah    |
| PM5 control 0        | PM5CTL0  | 10h    |

**表 6-40. FRAM Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| FRAM control 0       | FRCTL0   | 00h    |
| General control 0    | GCCTL0   | 04h    |
| General control 1    | GCCTL1   | 06h    |

**表 6-41. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRCDI     | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**表 6-42. RAM Controller Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| RAM controller control 0 | RCCTL0   | 00h    |

**表 6-43. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION   | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL   | 00h    |

**表 6-44. CS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| CS control 0         | CSCTL0   | 00h    |
| CS control 1         | CSCTL1   | 02h    |
| CS control 2         | CSCTL2   | 04h    |
| CS control 3         | CSCTL3   | 06h    |
| CS control 4         | CSCTL4   | 08h    |
| CS control 5         | CSCTL5   | 0Ah    |
| CS control 6         | CSCTL6   | 0Ch    |

**表 6-45. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| System control       | SYSCTL   | 00h    |
| JTAG mailbox control | SYSJMBC  | 06h    |

**表 6-45. SYS Registers (Base Address: 0180h) (continued)**

| REGISTER DESCRIPTION        | REGISTER | OFFSET |
|-----------------------------|----------|--------|
| JTAG mailbox input 0        | SYSJMBI0 | 08h    |
| JTAG mailbox input 1        | SYSJMBI1 | 0Ah    |
| JTAG mailbox output 0       | SYSJMBO0 | 0Ch    |
| JTAG mailbox output 1       | SYSJMBO1 | 0Eh    |
| User NMI vector generator   | SYSUNIV  | 1Ah    |
| System NMI vector generator | SYSSNIV  | 1Ch    |
| Reset vector generator      | SYSRSTIV | 1Eh    |

**表 6-46. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL   | 00h    |

**表 6-47. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input                 | P1IN     | 00h    |
| Port P1 output                | P1OUT    | 02h    |
| Port P1 direction             | P1DIR    | 04h    |
| Port P1 resistor enable       | P1REN    | 06h    |
| Port P1 selection 0           | P1SEL0   | 0Ah    |
| Port P1 selection 1           | P1SEL1   | 0Ch    |
| Port P1 interrupt vector word | P1IV     | 0Eh    |
| Port P1 complement selection  | P1SELC   | 16h    |
| Port P1 interrupt edge select | P1IES    | 18h    |
| Port P1 interrupt enable      | P1IE     | 1Ah    |
| Port P1 interrupt flag        | P1IFG    | 1Ch    |
| Port P2 input                 | P2IN     | 01h    |
| Port P2 output                | P2OUT    | 03h    |
| Port P2 direction             | P2DIR    | 05h    |
| Port P2 resistor enable       | P2REN    | 07h    |
| Port P2 selection 0           | P2SEL0   | 0Bh    |
| Port P2 selection 1           | P2SEL1   | 0Dh    |
| Port P2 complement selection  | P2SELC   | 17h    |
| Port P2 interrupt vector word | P2IV     | 1Eh    |
| Port P2 interrupt edge select | P2IES    | 19h    |
| Port P2 interrupt enable      | P2IE     | 1Bh    |
| Port P2 interrupt flag        | P2IFG    | 1Dh    |

**表 6-48. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P3 input                 | P3IN     | 00h    |
| Port P3 output                | P3OUT    | 02h    |
| Port P3 direction             | P3DIR    | 04h    |
| Port P3 resistor enable       | P3REN    | 06h    |
| Port P3 selection 0           | P3SEL0   | 0Ah    |
| Port P3 selection 1           | P3SEL1   | 0Ch    |
| Port P3 interrupt vector word | P3IV     | 0Eh    |

**表 6-48. Port P3, P4 Registers (Base Address: 0220h) (continued)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P3 complement selection  | P3SELC   | 16h    |
| Port P3 interrupt edge select | P3IES    | 18h    |
| Port P3 interrupt enable      | P3IE     | 1Ah    |
| Port P3 interrupt flag        | P3IFG    | 1Ch    |
| Port P4 input                 | P4IN     | 01h    |
| Port P4 output                | P4OUT    | 03h    |
| Port P4 direction             | P4DIR    | 05h    |
| Port P4 resistor enable       | P4REN    | 07h    |
| Port P4 selection 0           | P4SEL0   | 0Bh    |
| Port P4 selection 1           | P4SEL1   | 0Dh    |
| Port P4 complement selection  | P4SELC   | 17h    |
| Port P4 interrupt vector word | P4IV     | 1Eh    |
| Port P4 interrupt edge select | P4IES    | 19h    |
| Port P4 interrupt enable      | P4IE     | 1Bh    |
| Port P4 interrupt flag        | P4IFG    | 1Dh    |

**表 6-49. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Port P5 input                | P5IN     | 00h    |
| Port P5 output               | P5OUT    | 02h    |
| Port P5 direction            | P5DIR    | 04h    |
| Port P5 resistor enable      | P5REN    | 06h    |
| Port P5 selection 0          | P5SEL0   | 0Ah    |
| Port P5 selection 1          | P5SEL1   | 0Ch    |
| Reserved                     |          | 0Eh    |
| Port P5 complement selection | P5SELC   | 16h    |
| Reserved                     |          | 18h    |
| Reserved                     |          | 1Ah    |
| Reserved                     |          | 1Ch    |
| Port P6 input                | P6IN     | 01h    |
| Port P6 output               | P6OUT    | 03h    |
| Port P6 direction            | P6DIR    | 05h    |
| Port P6 resistor enable      | P6REN    | 07h    |
| Port P6 selection 0          | P6SEL0   | 0Bh    |
| Port P6 selection 1          | P6SEL1   | 0Dh    |
| Port P6 complement selection | P6SELC   | 17h    |
| Reserved                     |          | 1Eh    |
| Reserved                     |          | 19h    |
| Reserved                     |          | 1Bh    |
| Reserved                     |          | 1Dh    |

**表 6-50. Port P7 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P7 input           | P7IN     | 00h    |
| Port P7 output          | P7OUT    | 02h    |
| Port P7 direction       | P7DIR    | 04h    |
| Port P7 resistor enable | P7REN    | 06h    |

**表 6-50. Port P7 Registers (Base Address: 0260h) (continued)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Port P7 selection 0          | P7SEL0   | 0Ah    |
| Port P7 selection 1          | P7SEL1   | 0Ch    |
| Reserved                     |          | 0Eh    |
| Port P7 complement selection | P7SELC   | 16h    |
| Reserved                     |          | 18h    |
| Reserved                     |          | 1Ah    |
| Reserved                     |          | 1Ch    |

**表 6-51. Port P9 Registers (Base Address: 0280h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Port P9 input                | P9IN     | 00h    |
| Port P9 output               | P9OUT    | 02h    |
| Port P9 direction            | P9DIR    | 04h    |
| Port P9 resistor enable      | P9REN    | 06h    |
| Port P9 selection 0          | P9SEL0   | 0Ah    |
| Port P9 selection 1          | P9SEL1   | 0Ch    |
| Reserved                     |          | 0Eh    |
| Port P9 complement selection | P9SELC   | 16h    |
| Reserved                     |          | 18h    |
| Reserved                     |          | 1Ah    |
| Reserved                     |          | 1Ch    |

**表 6-52. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Port PJ input                | PJIN     | 00h    |
| Port PJ output               | PJOUT    | 02h    |
| Port PJ direction            | PJDIR    | 04h    |
| Port PJ resistor enable      | PJREN    | 06h    |
| Port PJ selection 0          | PJSEL0   | 0Ah    |
| Port PJ selection 1          | PJSEL1   | 0Ch    |
| Port PJ complement selection | PJSELC   | 16h    |

**表 6-53. Timer\_A TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION      | REGISTER  | OFFSET |
|---------------------------|-----------|--------|
| TA0 control               | TA0CTL    | 00h    |
| Capture/compare control 0 | TA0CCCTL0 | 02h    |
| Capture/compare control 1 | TA0CCCTL1 | 04h    |
| Capture/compare control 2 | TA0CCCTL2 | 06h    |
| TA0 counter               | TA0R      | 10h    |
| Capture/compare 0         | TA0CCR0   | 12h    |
| Capture/compare 1         | TA0CCR1   | 14h    |
| Capture/compare 2         | TA0CCR2   | 16h    |
| TA0 expansion 0           | TA0EX0    | 20h    |
| TA0 interrupt vector      | TA0IV     | 2Eh    |

**表 6-54. Timer\_A TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |
| TA1 counter               | TA1R     | 10h    |
| Capture/compare 0         | TA1CCR0  | 12h    |
| Capture/compare 1         | TA1CCR1  | 14h    |
| Capture/compare 2         | TA1CCR2  | 16h    |
| TA1 expansion 0           | TA1EX0   | 20h    |
| TA1 interrupt vector      | TA1IV    | 2Eh    |

**表 6-55. Timer\_B TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control               | TB0CTL   | 00h    |
| Capture/compare control 0 | TB0CCTL0 | 02h    |
| Capture/compare control 1 | TB0CCTL1 | 04h    |
| Capture/compare control 2 | TB0CCTL2 | 06h    |
| Capture/compare control 3 | TB0CCTL3 | 08h    |
| Capture/compare control 4 | TB0CCTL4 | 0Ah    |
| Capture/compare control 5 | TB0CCTL5 | 0Ch    |
| Capture/compare control 6 | TB0CCTL6 | 0Eh    |
| TB0 counter               | TB0R     | 10h    |
| Capture/compare 0         | TB0CCR0  | 12h    |
| Capture/compare 1         | TB0CCR1  | 14h    |
| Capture/compare 2         | TB0CCR2  | 16h    |
| Capture/compare 3         | TB0CCR3  | 18h    |
| Capture/compare 4         | TB0CCR4  | 1Ah    |
| Capture/compare 5         | TB0CCR5  | 1Ch    |
| Capture/compare 6         | TB0CCR6  | 1Eh    |
| TB0 expansion 0           | TB0EX0   | 20h    |
| TB0 interrupt vector      | TB0IV    | 2Eh    |

**表 6-56. Timer\_A TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA2 control               | TA2CTL   | 00h    |
| Capture/compare control 0 | TA2CCTL0 | 02h    |
| Capture/compare control 1 | TA2CCTL1 | 04h    |
| TA2 counter               | TA2R     | 10h    |
| Capture/compare 0         | TA2CCR0  | 12h    |
| Capture/compare 1         | TA2CCR1  | 14h    |
| TA2 expansion 0           | TA2EX0   | 20h    |
| TA2 interrupt vector      | TA2IV    | 2Eh    |

**表 6-57. Capacitive Touch I/O 0 Registers (Base Address: 0430h)**

| REGISTER DESCRIPTION           | REGISTER   | OFFSET |
|--------------------------------|------------|--------|
| Capacitive touch I/O 0 control | CAPTIO0CTL | 0Eh    |

**表 6-58. Timer\_A TA3 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA3 control               | TA3CTL   | 00h    |
| Capture/compare control 0 | TA3CCTL0 | 02h    |
| Capture/compare control 1 | TA3CCTL1 | 04h    |
| Capture/compare control 2 | TA3CCTL2 | 06h    |
| Capture/compare control 3 | TA3CCTL3 | 08h    |
| Capture/compare control 4 | TA3CCTL4 | 0Ah    |
| TA3 counter               | TA3R     | 10h    |
| Capture/compare 0         | TA3CCR0  | 12h    |
| Capture/compare 1         | TA3CCR1  | 14h    |
| Capture/compare 2         | TA3CCR2  | 16h    |
| Capture/compare 3         | TA3CCR3  | 18h    |
| Capture/compare 4         | TA3CCR4  | 1Ah    |
| TA3 expansion 0           | TA3EX0   | 20h    |
| TA3 interrupt vector      | TA3IV    | 2Eh    |

**表 6-59. Capacitive Touch I/O 1 Registers (Base Address: 0470h)**

| REGISTER DESCRIPTION           | REGISTER   | OFFSET |
|--------------------------------|------------|--------|
| Capacitive touch I/O 1 control | CAPTIO1CTL | 0Eh    |

**表 6-60. RTC\_C Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION         | REGISTER       | OFFSET |
|------------------------------|----------------|--------|
| RTC control 0                | RTCCTL0        | 00h    |
| RTC password                 | RTCPWD         | 01h    |
| RTC control 1                | RTCCTL1        | 02h    |
| RTC control 3                | RTCCTL3        | 03h    |
| RTC offset calibration       | RTCOCAL        | 04h    |
| RTC temperature compensation | RTCTCMP        | 06h    |
| RTC prescaler 0 control      | RTCPS0CTL      | 08h    |
| RTC prescaler 1 control      | RTCPS1CTL      | 0Ah    |
| RTC prescaler 0              | RTCPS0         | 0Ch    |
| RTC prescaler 1              | RTCPS1         | 0Dh    |
| RTC interrupt vector word    | RTCIV          | 0Eh    |
| RTC seconds/counter 1        | RTCSEC/RTCNT1  | 10h    |
| RTC minutes/counter 2        | RTCMIN/RTCNT2  | 11h    |
| RTC hours/counter 3          | RTCHOUR/RTCNT3 | 12h    |
| RTC day of week/counter 4    | RTCDOW/RTCNT4  | 13h    |
| RTC days                     | RTCDAY         | 14h    |
| RTC month                    | RTCMON         | 15h    |
| RTC year                     | RTCYEAR        | 16h    |
| RTC alarm minutes            | RTCAMIN        | 18h    |
| RTC alarm hours              | RTCAHOUR       | 19h    |
| RTC alarm day of week        | RTCADOW        | 1Ah    |
| RTC alarm days               | RTCADAY        | 1Bh    |
| Binary-to-BCD conversion     | BIN2BCD        | 1Ch    |
| BCD-to-binary conversion     | BCD2BIN        | 1Eh    |

**表 6-61. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | REGISTER  | OFFSET |
|---------------------------------------------------------|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2                                        | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension                                   | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1                                        | RES1      | 26h    |
| 32 × 32 result 2                                        | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control 0                                         | MPY32CTL0 | 2Ch    |

**表 6-62. DMA Registers (Base Address DMA General Control: 0500h,  
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION                   | REGISTER | OFFSET |
|----------------------------------------|----------|--------|
| DMA channel 0 control                  | DMA0CTL  | 00h    |
| DMA channel 0 source address low       | DMA0SAL  | 02h    |
| DMA channel 0 source address high      | DMA0SAH  | 04h    |
| DMA channel 0 destination address low  | DMA0DAL  | 06h    |
| DMA channel 0 destination address high | DMA0DAH  | 08h    |
| DMA channel 0 transfer size            | DMA0SZ   | 0Ah    |
| DMA channel 1 control                  | DMA1CTL  | 00h    |
| DMA channel 1 source address low       | DMA1SAL  | 02h    |
| DMA channel 1 source address high      | DMA1SAH  | 04h    |
| DMA channel 1 destination address low  | DMA1DAL  | 06h    |
| DMA channel 1 destination address high | DMA1DAH  | 08h    |
| DMA channel 1 transfer size            | DMA1SZ   | 0Ah    |
| DMA channel 2 control                  | DMA2CTL  | 00h    |
| DMA channel 2 source address low       | DMA2SAL  | 02h    |
| DMA channel 2 source address high      | DMA2SAH  | 04h    |
| DMA channel 2 destination address low  | DMA2DAL  | 06h    |
| DMA channel 2 destination address high | DMA2DAH  | 08h    |
| DMA channel 2 transfer size            | DMA2SZ   | 0Ah    |
| DMA module control 0                   | DMACTL0  | 00h    |
| DMA module control 1                   | DMACTL1  | 02h    |

**表 6-62. DMA Registers (Base Address DMA General Control: 0500h,  
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 2 | DMACTL2  | 04h    |
| DMA module control 3 | DMACTL3  | 06h    |
| DMA module control 4 | DMACTL4  | 08h    |
| DMA interrupt vector | DMAIV    | 0Eh    |

**表 6-63. MPU Control Registers (Base Address: 05A0h)**

| REGISTER DESCRIPTION                  | REGISTER   | OFFSET |
|---------------------------------------|------------|--------|
| MPU control 0                         | MPUCTL0    | 00h    |
| MPU control 1                         | MPUCTL1    | 02h    |
| MPU Segmentation Border 2             | MPUSEGB2   | 04h    |
| MPU Segmentation Border 1             | MPUSEGB1   | 06h    |
| MPU access management                 | MPUSAM     | 08h    |
| MPU IP control 0                      | MPUIPC0    | 0Ah    |
| MPU IP Encapsulation Segment Border 2 | MPUIPSEGB2 | 0Ch    |
| MPU IP Encapsulation Segment Border 1 | MPUIPSEGB1 | 0Eh    |

**表 6-64. eUSCI\_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION          | REGISTER   | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA0CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA0CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA0BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA0BR1    | 07h    |
| eUSCI_A modulation control    | UCA0MCTLW  | 08h    |
| eUSCI_A status word           | UCA0STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA0RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA0TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA0ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | UCA0IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA0IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA0IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA0IV     | 1Eh    |

**表 6-65. eUSCI\_A1 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION          | REGISTER   | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0        | UCA1CTLW0  | 00h    |
| eUSCI_A control word 1        | UCA1CTLW1  | 02h    |
| eUSCI_A baud rate 0           | UCA1BR0    | 06h    |
| eUSCI_A baud rate 1           | UCA1BR1    | 07h    |
| eUSCI_A modulation control    | UCA1MCTLW  | 08h    |
| eUSCI_A status word           | UCA1STATW  | 0Ah    |
| eUSCI_A receive buffer        | UCA1RXBUF  | 0Ch    |
| eUSCI_A transmit buffer       | UCA1TXBUF  | 0Eh    |
| eUSCI_A LIN control           | UCA1ABCTL  | 10h    |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h    |

**表 6-65. eUSCI\_A1 Registers (Base Address:05E0h) (continued)**

| REGISTER DESCRIPTION          | REGISTER   | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A IrDA receive control  | UCA1IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA1IE     | 1Ah    |
| eUSCI_A interrupt flags       | UCA1IFG    | 1Ch    |
| eUSCI_A interrupt vector word | UCA1IV     | 1Eh    |

**表 6-66. eUSCI\_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION           | REGISTER    | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB0CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB0CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB0BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB0BR1     | 07h    |
| eUSCI_B status word            | UCB0STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB0TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB0RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB0TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB0I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB0I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB0I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB0I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB0ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB0ADDMASK | 1Eh    |
| eUSCI_B I2C slave address      | UCB0I2CSA   | 20h    |
| eUSCI_B interrupt enable       | UCB0IE      | 2Ah    |
| eUSCI_B interrupt flags        | UCB0IFG     | 2Ch    |
| eUSCI_B interrupt vector word  | UCB0IV      | 2Eh    |

**表 6-67. eUSCI\_B1 Registers (Base Address: 0680h)**

| REGISTER DESCRIPTION           | REGISTER    | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB1CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB1CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB1BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB1BR1     | 07h    |
| eUSCI_B status word            | UCB1STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB1TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB1RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB1TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB1I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB1I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB1I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB1I2COA3  | 1Ah    |
| eUSCI_B received address       | UCB1ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB1ADDMASK | 1Eh    |
| eUSCI_B I2C slave address      | UCB1I2CSA   | 20h    |
| eUSCI_B interrupt enable       | UCB1IE      | 2Ah    |
| eUSCI_B interrupt flags        | UCB1IFG     | 2Ch    |
| eUSCI_B interrupt vector word  | UCB1IV      | 2Eh    |

**表 6-68. ADC12\_B Registers (Base Address: 0800h)**

| REGISTER DESCRIPTION                     | REGISTER    | OFFSET |
|------------------------------------------|-------------|--------|
| ADC12_B control 0                        | ADC12CTL0   | 00h    |
| ADC12_B control 1                        | ADC12CTL1   | 02h    |
| ADC12_B control 2                        | ADC12CTL2   | 04h    |
| ADC12_B control 3                        | ADC12CTL3   | 06h    |
| ADC12_B window comparator low threshold  | ADC12LO     | 08h    |
| ADC12_B window comparator high threshold | ADC12HI     | 0Ah    |
| ADC12_B interrupt flag 0                 | ADC12IFGR0  | 0Ch    |
| ADC12_B interrupt flag 1                 | ADC12IFGR1  | 0Eh    |
| ADC12_B interrupt flag 2                 | ADC12IFGR2  | 10h    |
| ADC12_B interrupt enable 0               | ADC12IER0   | 12h    |
| ADC12_B Interrupt Enable 1               | ADC12IER1   | 14h    |
| ADC12_B interrupt enable 2               | ADC12IER2   | 16h    |
| ADC12_B interrupt vector                 | ADC12IV     | 18h    |
| ADC12_B memory control 0                 | ADC12MCTL0  | 20h    |
| ADC12_B memory control 1                 | ADC12MCTL1  | 22h    |
| ADC12_B memory control 2                 | ADC12MCTL2  | 24h    |
| ADC12_B memory control 3                 | ADC12MCTL3  | 26h    |
| ADC12_B memory control 4                 | ADC12MCTL4  | 28h    |
| ADC12_B memory control 5                 | ADC12MCTL5  | 2Ah    |
| ADC12_B memory control 6                 | ADC12MCTL6  | 2Ch    |
| ADC12_B memory control 7                 | ADC12MCTL7  | 2Eh    |
| ADC12_B memory control 8                 | ADC12MCTL8  | 30h    |
| ADC12_B memory control 9                 | ADC12MCTL9  | 32h    |
| ADC12_B memory control 10                | ADC12MCTL10 | 34h    |
| ADC12_B memory control 11                | ADC12MCTL11 | 36h    |
| ADC12_B memory control 12                | ADC12MCTL12 | 38h    |
| ADC12_B memory control 13                | ADC12MCTL13 | 3Ah    |
| ADC12_B memory control 14                | ADC12MCTL14 | 3Ch    |
| ADC12_B memory control 15                | ADC12MCTL15 | 3Eh    |
| ADC12_B memory control 16                | ADC12MCTL16 | 40h    |
| ADC12_B memory control 17                | ADC12MCTL17 | 42h    |
| ADC12_B memory control 18                | ADC12MCTL18 | 44h    |
| ADC12_B memory control 19                | ADC12MCTL19 | 46h    |
| ADC12_B memory control 20                | ADC12MCTL20 | 48h    |
| ADC12_B memory control 21                | ADC12MCTL21 | 4Ah    |
| ADC12_B memory control 22                | ADC12MCTL22 | 4Ch    |
| ADC12_B memory control 23                | ADC12MCTL23 | 4Eh    |
| ADC12_B memory control 24                | ADC12MCTL24 | 50h    |
| ADC12_B memory control 25                | ADC12MCTL25 | 52h    |
| ADC12_B memory control 26                | ADC12MCTL26 | 54h    |
| ADC12_B memory control 27                | ADC12MCTL27 | 56h    |
| ADC12_B memory control 28                | ADC12MCTL28 | 58h    |
| ADC12_B memory control 29                | ADC12MCTL29 | 5Ah    |
| ADC12_B memory control 30                | ADC12MCTL30 | 5Ch    |
| ADC12_B memory control 31                | ADC12MCTL31 | 5Eh    |
| ADC12_B memory 0                         | ADC12MEM0   | 60h    |
| ADC12_B memory 1                         | ADC12MEM1   | 62h    |

**表 6-68. ADC12\_B Registers (Base Address: 0800h) (continued)**

| REGISTER DESCRIPTION | REGISTER   | OFFSET |
|----------------------|------------|--------|
| ADC12_B memory 2     | ADC12MEM2  | 64h    |
| ADC12_B memory 3     | ADC12MEM3  | 66h    |
| ADC12_B memory 4     | ADC12MEM4  | 68h    |
| ADC12_B memory 5     | ADC12MEM5  | 6Ah    |
| ADC12_B memory 6     | ADC12MEM6  | 6Ch    |
| ADC12_B memory 7     | ADC12MEM7  | 6Eh    |
| ADC12_B memory 8     | ADC12MEM8  | 70h    |
| ADC12_B memory 9     | ADC12MEM9  | 72h    |
| ADC12_B memory 10    | ADC12MEM10 | 74h    |
| ADC12_B memory 11    | ADC12MEM11 | 76h    |
| ADC12_B memory 12    | ADC12MEM12 | 78h    |
| ADC12_B memory 13    | ADC12MEM13 | 7Ah    |
| ADC12_B memory 14    | ADC12MEM14 | 7Ch    |
| ADC12_B memory 15    | ADC12MEM15 | 7Eh    |
| ADC12_B memory 16    | ADC12MEM16 | 80h    |
| ADC12_B memory 17    | ADC12MEM17 | 82h    |
| ADC12_B memory 18    | ADC12MEM18 | 84h    |
| ADC12_B memory 19    | ADC12MEM19 | 86h    |
| ADC12_B memory 20    | ADC12MEM20 | 88h    |
| ADC12_B memory 21    | ADC12MEM21 | 8Ah    |
| ADC12_B memory 22    | ADC12MEM22 | 8Ch    |
| ADC12_B memory 23    | ADC12MEM23 | 8Eh    |
| ADC12_B memory 24    | ADC12MEM24 | 90h    |
| ADC12_B memory 25    | ADC12MEM25 | 92h    |
| ADC12_B memory 26    | ADC12MEM26 | 94h    |
| ADC12_B memory 27    | ADC12MEM27 | 96h    |
| ADC12_B memory 28    | ADC12MEM28 | 98h    |
| ADC12_B memory 29    | ADC12MEM29 | 9Ah    |
| ADC12_B memory 30    | ADC12MEM30 | 9Ch    |
| ADC12_B memory 31    | ADC12MEM31 | 9Eh    |

**表 6-69. Comparator\_E Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION             | REGISTER | OFFSET |
|----------------------------------|----------|--------|
| Comparator control 0             | CECTL0   | 00h    |
| Comparator control 1             | CECTL1   | 02h    |
| Comparator control 2             | CECTL2   | 04h    |
| Comparator control 3             | CECTL3   | 06h    |
| Comparator interrupt             | CEINT    | 0Ch    |
| Comparator interrupt vector word | CEIV     | 0Eh    |

**表 6-70. CRC32 Registers (Base Address: 0980h)**

| REGISTER DESCRIPTION                   | REGISTER      | OFFSET |
|----------------------------------------|---------------|--------|
| CRC32 data input                       | CRC32DIW0     | 00h    |
| Reserved                               |               | 02h    |
| Reserved                               |               | 04h    |
| CRC32 data input reverse               | CRC32DIRBW0   | 06h    |
| CRC32 initialization and result word 0 | CRC32INIRESW0 | 08h    |

**表 6-70. CRC32 Registers (Base Address: 0980h) (continued)**

| REGISTER DESCRIPTION                   | REGISTER      | OFFSET |
|----------------------------------------|---------------|--------|
| CRC32 initialization and result word 1 | CRC32INIRESW1 | 0Ah    |
| CRC32 result reverse word 1            | CRC32RESRW1   | 0Ch    |
| CRC32 result reverse word 0            | CRC32RESRW1   | 0Eh    |
| CRC16 data input                       | CRC16DIW0     | 10h    |
| Reserved                               |               | 12h    |
| Reserved                               |               | 14h    |
| CRC16 data input reverse               | CRC16DIRBW0   | 16h    |
| CRC16 initialization and result word 0 | CRC16INIRESW0 | 18h    |
| Reserved                               |               | 1Ah    |
| Reserved                               |               | 1Ch    |
| CRC16 result reverse word 0            | CRC16RESRW1   | 1Eh    |
| Reserved                               |               | 20h    |
| Reserved                               |               | 22h    |
| Reserved                               |               | 24h    |
| Reserved                               |               | 26h    |
| Reserved                               |               | 28h    |
| Reserved                               |               | 2Ah    |
| Reserved                               |               | 2Ch    |
| Reserved                               |               | 2Eh    |

**表 6-71. AES Accelerator Registers (Base Address: 09C0h)**

| REGISTER DESCRIPTION                       | REGISTER | OFFSET |
|--------------------------------------------|----------|--------|
| AES accelerator control 0                  | AESACTL0 | 00h    |
| Reserved                                   |          | 02h    |
| AES accelerator status                     | AESASTAT | 04h    |
| AES accelerator key                        | AESAKEY  | 06h    |
| AES accelerator data in                    | AESADIN  | 008h   |
| AES accelerator data out                   | AESADOUT | 00Ah   |
| AES accelerator XORed data in              | AESAXDIN | 00Ch   |
| AES accelerator XORed data in (no trigger) | AESAXIN  | 00Eh   |

## 6.14 Identification

### 6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see [8.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [6.12](#).

### 6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see [8.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [6.12](#).

### 6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in [MSP430 Programming With the JTAG Interface](#).

## 7 Applications, Implementation, and Layout

### 注

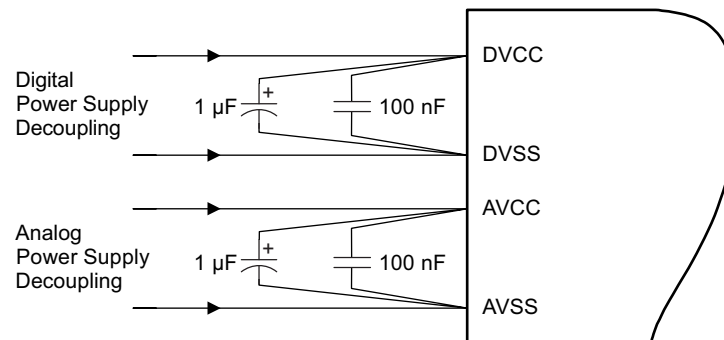
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

#### 7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1- $\mu$ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.



✎ 7-1. Power Supply Decoupling

#### 7.1.2 External Oscillator

Depending on the device variant (see [Section 3](#)), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to [Section 4.6](#).

✎ 7-2 shows a typical connection diagram.

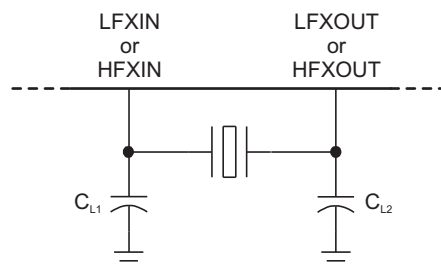


图 7-2. Typical Crystal Connection

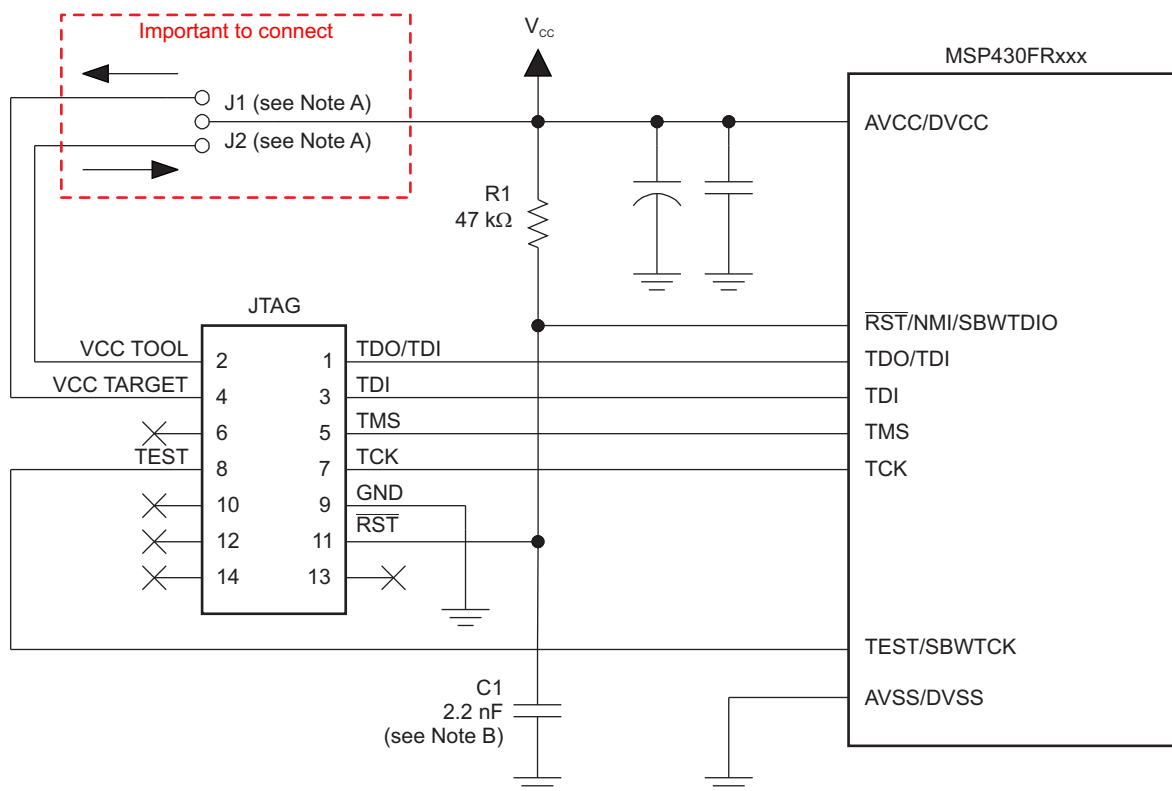
See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 图 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 图 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply  $V_{CC}$  to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a  $V_{CC}$ -sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The  $V_{CC}$ -sense feature senses the local  $V_{CC}$  present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 图 7-3 and 图 7-4 show a jumper block that supports both scenarios of supplying  $V_{CC}$  to the target board. If this flexibility is not required, the desired  $V_{CC}$  connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

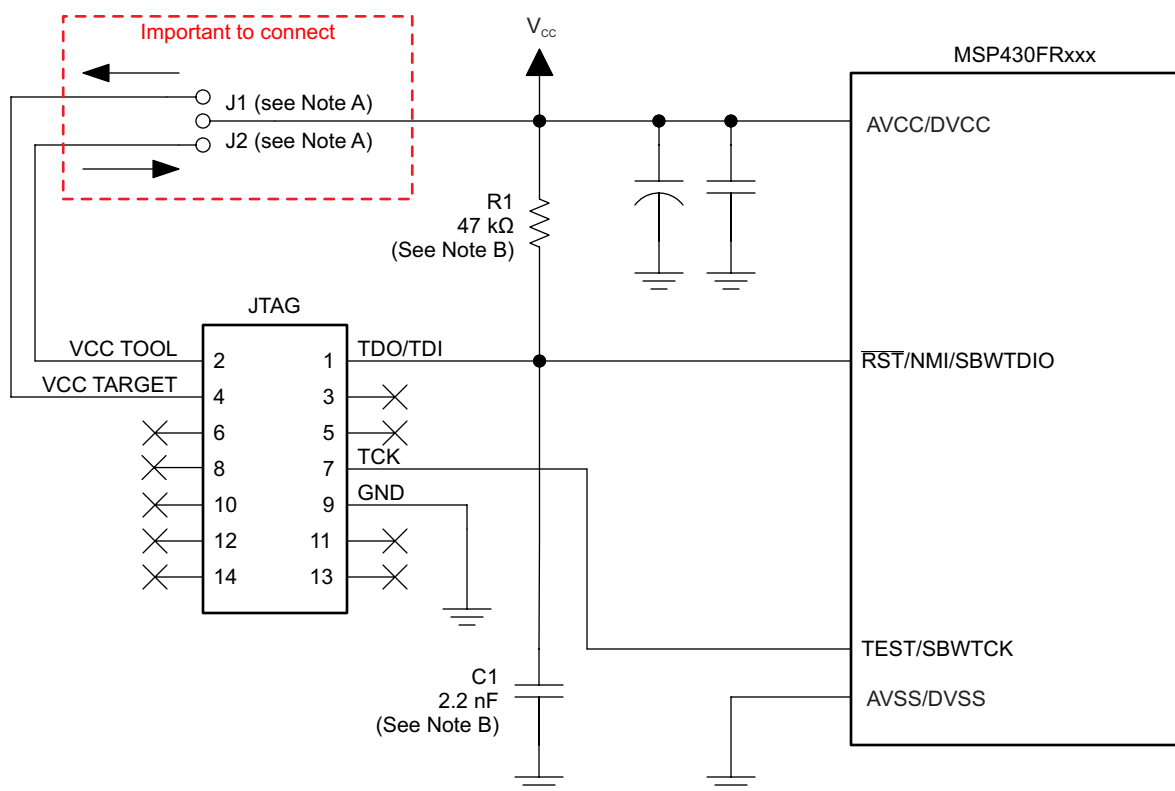
For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



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- If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- The upper limit for C1 is 2.2 nF when using current TI tools.

### 7-3. Signal Connections for 4-Wire JTAG Communication



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- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device RST/NMI/SBWTIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

#### 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the special function register (SFR) SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#) for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.6](#).

### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

### 7.1.7 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Section 5.1](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC12\_B Peripheral

#### 7.2.1.1 Partial Schematic

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the  $I_{O(VREF+)}$  specification of the REF module.

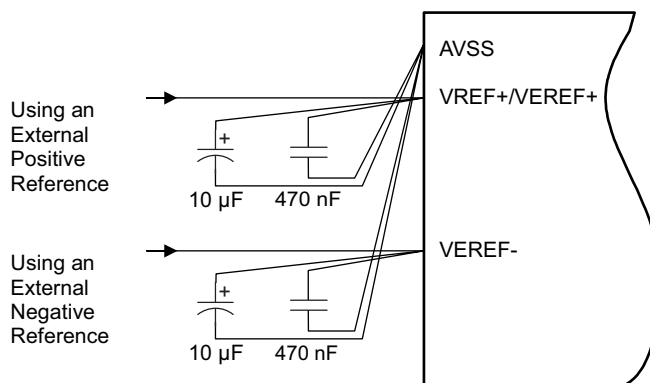


Figure 7-5. ADC12\_B Grounding and Noise Considerations

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [7.1.1](#) combined with the connections shown in [7.2.1.1](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- $\mu$ F capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 470-nF bypass capacitor is used to filter out any high-frequency noise.

### 7.2.1.3 Detailed Design Procedure

For additional design information, see [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#).

#### 7.2.1.4 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12\_B, the analog differential input signals must be routed close together to minimize the effect of noise on the resulting signal.

## 8 デバイスおよびドキュメントのサポート

### 8.1 使い始めと次の手順

MSP430™ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「[Getting Started](#)」ページを参照してください。

### 8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

**XMS** - 実験段階のデバイスで、最終的なデバイスの電氣的仕様を表しているとは限りません。

**MSP** - 完全に認定済みの量産版デバイスです。

XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。

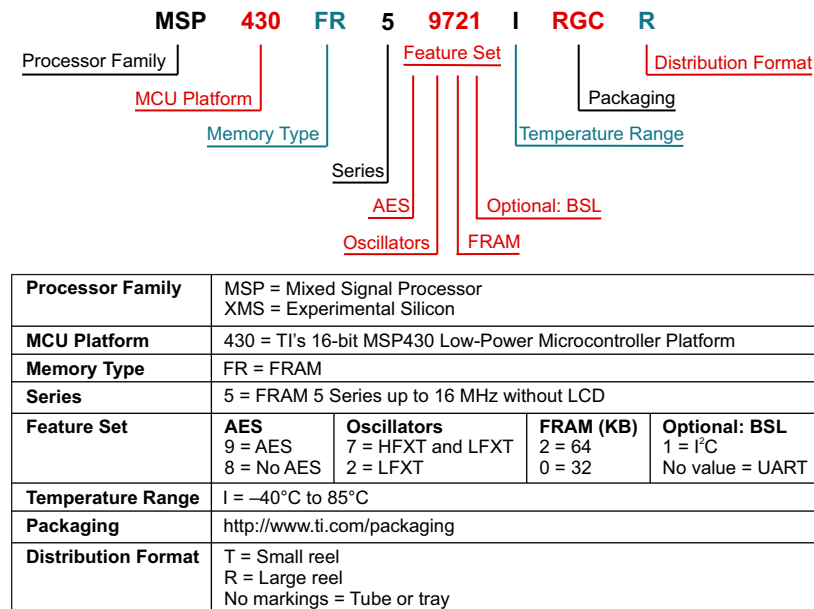


図 8-1. デバイスの項目表記

### 8.3 ツールとソフトウェア

すべてのMSPマイクロコントローラは、広範なソフトウェアおよびハードウェア開発ツールによりサポートされています。ツールは、TIおよびさまざまなサードパーティーから入手できます。すべてのツールの一覧は、『[低消費電力 MCU用の開発キットとソフトウェア](#)』で参照できます。

表 8-1は、MSP430FR597x(1)、MSP430FR592x(1)、MSP430FR587x(1) MCUのデバッグ機能の一覧です。利用可能な機能の詳細については、『[MSP430用Code Composer Studio ユーザー・ガイド](#)』を参照してください。

表 8-1. ハードウェアのデバッグ機能

| MSP430のアーキテクチャ | 4線式 JTAG | 2線式 JTAG | ブレーク・ポイント | 範囲ブレーク・ポイント | クロック制御 | 状態シーケンサ | トレース・バッファ | LPMx.5デバッグ・サポート | EnergyTrace++テクノロジー |
|----------------|----------|----------|-----------|-------------|--------|---------|-----------|-----------------|---------------------|
| MSP430Xv2      | ○        | ○        | 3         | ○           | ○      | ×       | ×         | ○               | ○                   |

#### 設計キットと評価モジュール

**MSP430FR6989 LaunchPad開発キット** MSP-EXP40FR6989 LaunchPad 開発キットは、MSP430FR6989 マイクロコントローラ(MCU)用の使いやすい評価モジュール(EVM)です。プログラミング、デバッグ、エネルギー測定のためのオンボード・エミュレーションなど、超低消費電力の MSP430FRx FRAM マイクロコントローラ・プラットフォームの開発を始めるために必要な、すべての機能が付属しています。

**MSP-TS430PM64F - MSP430 64ピンFRAMターゲット・ソケット基板** MSP-TS430PZ5X100はスタンドアロンの ZIFソケット・ターゲット・ボードで、JTAGインターフェイスまたは Spy-Bi-Wire (2線式のJTAG) プロトコルによるシステム内のMSP430 MCUのプログラムとデバッグに使用されます。

**MSP-FET430U64F - MSP430 64ピンFRAM TS基板およびMSP-FETバンドル** MSP-FET430U64Fは、MSP-FETエミュレータとスタンドアロンの64ピンZIFソケット・ターゲット基板を含むバンドルで、JTAGインターフェイスまたは Spy Bi-Wire (2線式JTAG) プロトコルにより、システム内のMSP430のプログラムおよびデバッグに使用できます。TS開発基板は、64ピンLQFPパッケージ(TIパッケージ・コード: PM)のMSP430FR6972 FRAMデバイスをサポートしています。

#### ソフトウェア

**MSP430Ware™ソフトウェア** MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSPドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430WareソフトウェアはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

**MSP430FR592x、MSP430FR5x7x、MSP430FR6x2x、MSP430FR6x7xのコード例** すべてのMSPデバイス用に、内蔵の各ペリフェラルをさまざまなアプリケーションの要求に応じて構成するためのCコードの例が用意されています。

**静電容量式タッチ・ソフトウェア・ライブラリ** MSP430 MCU で静電容量式タッチ機能を有効にするための、無償のCライブラリです。MSP430 MCU バージョンのライブラリには、ROおよびRC方式を含む、いくつかの静電容量式タッチ機能の実装が含まれています。

**MSPドライバ・ライブラリ** MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

**MSP EnergyTrace™テクノロジー** MSP430マイクロコントローラ用のEnergyTraceテクノロジーは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

**ULP (超低消費電力) Advisor** ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisor はマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力を低減するため、コードのどの部分をさらに最適化が可能か、通知と注釈により特定します。

**IEC60730ソフトウェア・パッケージ** IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

**MSP用の固定小数点算術ライブラリ** MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードヘシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

**MSP430用の浮動小数点算術ライブラリ** 低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、MSPデバイスのインテリジェントなペリフェラルを活用しており、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

## 開発ツール

**Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境** Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッグ、プロファイラなど、多数の機能が含まれています。

**コマンドライン・プログラマ** MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェルスクリプトベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

**MSP MCUプログラマおよびデバッグ** MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

**MSP-GANG量産プログラマ** MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8 つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

## 8.4 ドキュメントのサポート

以下のドキュメントにはMSP430FR597x(1)、MSP430FR592x(1)、MSP430FR587x(1) MCUについて記載されています。これらのドキュメントのコピーは、[www.ti.com](http://www.ti.com)で入手できます。

### ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、[ti.com](http://ti.com)でご利用の製品のフォルダへ移動します(製品フォルダへのリンクについては、8.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 正誤表

『MSP430FR5972正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR59721正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5922正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR59221正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5970正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5872正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR58721正誤表』には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5870正誤表』には、機能仕様に対する既知の例外が記載されています。

### ユーザー・ガイド

『MSP430FR58xx, MSP430FR59xx, MSP430FR6xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL) ユーザー・ガイド』 MSP430 MCUに搭載されたブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430 MCUの組み込みメモリと通信できます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

### アプリケーション・レポート

『MSP-EXP430FR5969でのEEMBC ULPBench使用の基礎』 ULPMark™-CP スコアを取得するため、組み込みマイクロプロセッサ・ベンチマーク・コンソーシアム (EEMBC) の ULPBench™およびEnergyMonitor を MSP430FR5969 マイクロコントローラ (MCU) で使用方法の基礎ガイドです。このドキュメントでは、ベンチマークを実行するためのターゲット評価モジュール (EVM) として、MSP-EXP430FR5969 LaunchPad 開発キットを使用します。ULPBench は EEMBC ベンチマークの 1 つであり、MCU の超低消費電力機能を測定するための業界標準手法です。

『**MSP430 FRAM**テクノロジー - ハウツーとベスト・プラクティス』 FRAMは不揮発性メモリ・テクノロジーで、SRAMと同様に動作し、多くの新しいアプリケーションを可能にすると同時に、ファームウェアの設計方法に変革をもたらすものです。このアプリケーション・レポートでは、組み込みソフトウェア開発の観点から、MSP430のFRAMテクノロジーを使用する方法と、そのベスト・プラクティスについて概説しています。アプリケーション固有のコード、定数、データ容量の要件に従ってメモリ・レイアウトを実装する方法、FRAMを使用してアプリケーションの消費エネルギーを最適化する方法、およびメモリ保護ユニット(MPU)を使用して、プログラム・コードを意図しない書き込みアクセスから保護し、アプリケーションの堅牢性を最大限に高める方法について解説されています。

『**MSP430 32kHz**水晶発振器』 適切な水晶振動子、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器に重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『**MSP430 システム・レベルESD**の考慮事項』 シリコン・テクノロジーがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まってくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

## 8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

| 製品            | プロダクト・フォルダ              | ご注文はこちら                 | 技術資料                    | ツールとソフトウェア              | サポートとコミュニティ             |
|---------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| MSP430FR5972  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR59721 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR5970  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR5922  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR59221 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR5872  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR58721 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| MSP430FR5870  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |

## 8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### TI E2E™ Community

TI's *Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

### TI Embedded Processors Wiki

*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.7 商標

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ULPMark, ULPBench are trademarks of Embedded Microprocessor Benchmark Consortium.

Microsoft is a registered trademark of Microsoft Corporation.

All other trademarks are the property of their respective owners.

## 8.8 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 8.10 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430FR5870IPMR</a>   | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5870              |
| MSP430FR5870IPMR.A                 | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5870              |
| <a href="#">MSP430FR5870IRGCR</a>  | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5870              |
| MSP430FR5870IRGCR.A                | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5870              |
| <a href="#">MSP430FR58721IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR58721             |
| MSP430FR58721IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR58721             |
| <a href="#">MSP430FR58721IRGCR</a> | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR58721             |
| MSP430FR58721IRGCR.A               | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR58721             |
| <a href="#">MSP430FR5872IPMR</a>   | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5872              |
| MSP430FR5872IPMR.A                 | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5872              |
| <a href="#">MSP430FR5872IRGCR</a>  | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5872              |
| MSP430FR5872IRGCR.A                | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5872              |
| <a href="#">MSP430FR59221IG56R</a> | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| MSP430FR59221IG56R.A               | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| <a href="#">MSP430FR59221IPMR</a>  | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| MSP430FR59221IPMR.A                | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| <a href="#">MSP430FR59221IRGCR</a> | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| MSP430FR59221IRGCR.A               | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59221             |
| <a href="#">MSP430FR5922IG56R</a>  | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| MSP430FR5922IG56R.A                | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| <a href="#">MSP430FR5922IPM</a>    | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| MSP430FR5922IPM.A                  | Active        | Production           | LQFP (PM)   64   | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| <a href="#">MSP430FR5922IPMR</a>   | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| MSP430FR5922IPMR.A                 | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| <a href="#">MSP430FR5922IRGCR</a>  | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| MSP430FR5922IRGCR.A                | Active        | Production           | VQFN (RGC)   64  | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5922              |
| <a href="#">MSP430FR5970IPMR</a>   | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5970              |
| MSP430FR5970IPMR.A                 | Active        | Production           | LQFP (PM)   64   | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5970              |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430FR5970IRGCR</a>  | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5970              |
| MSP430FR5970IRGCR.A                | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5970              |
| <a href="#">MSP430FR59721IPM</a>   | Active        | Production           | LQFP (PM)   64  | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| MSP430FR59721IPM.A                 | Active        | Production           | LQFP (PM)   64  | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| <a href="#">MSP430FR59721IPMR</a>  | Active        | Production           | LQFP (PM)   64  | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| MSP430FR59721IPMR.A                | Active        | Production           | LQFP (PM)   64  | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| <a href="#">MSP430FR59721IRGCR</a> | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| MSP430FR59721IRGCR.A               | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR59721             |
| <a href="#">MSP430FR5972IPM</a>    | Active        | Production           | LQFP (PM)   64  | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |
| MSP430FR5972IPM.A                  | Active        | Production           | LQFP (PM)   64  | 160   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |
| <a href="#">MSP430FR5972IPMR</a>   | Active        | Production           | LQFP (PM)   64  | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |
| MSP430FR5972IPMR.A                 | Active        | Production           | LQFP (PM)   64  | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |
| <a href="#">MSP430FR5972IRGCR</a>  | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |
| MSP430FR5972IRGCR.A                | Active        | Production           | VQFN (RGC)   64 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | FR5972              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

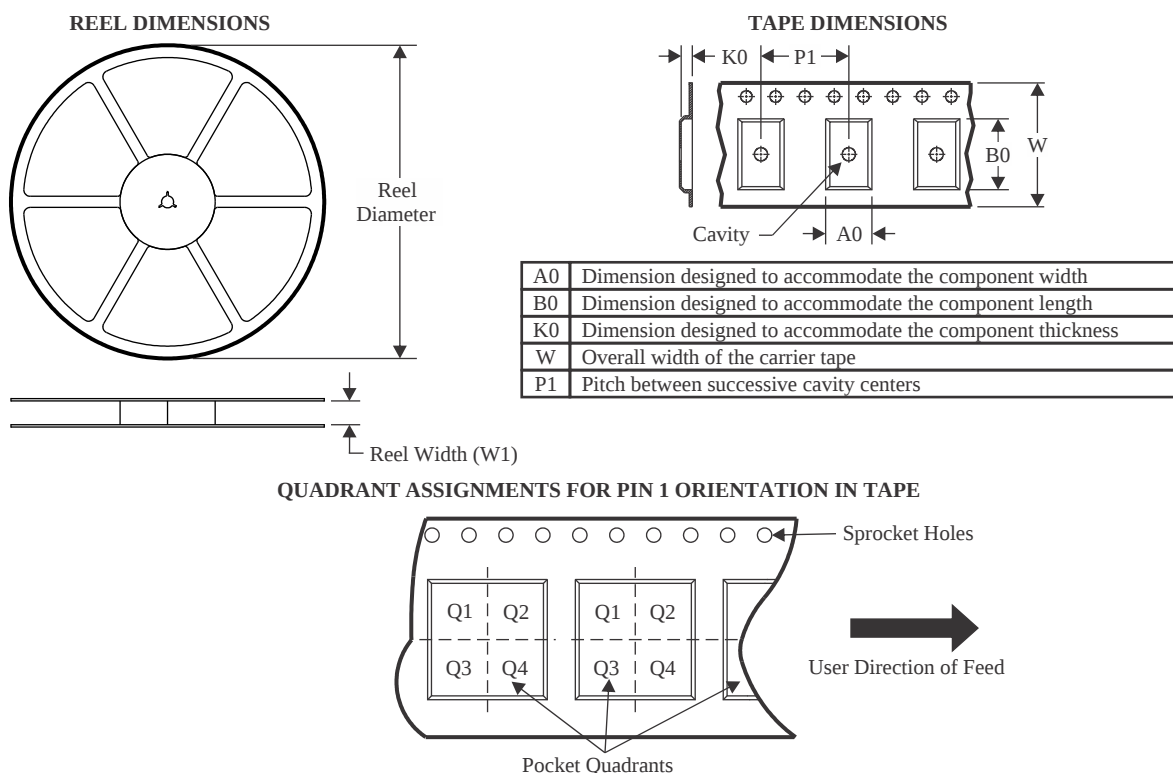
**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



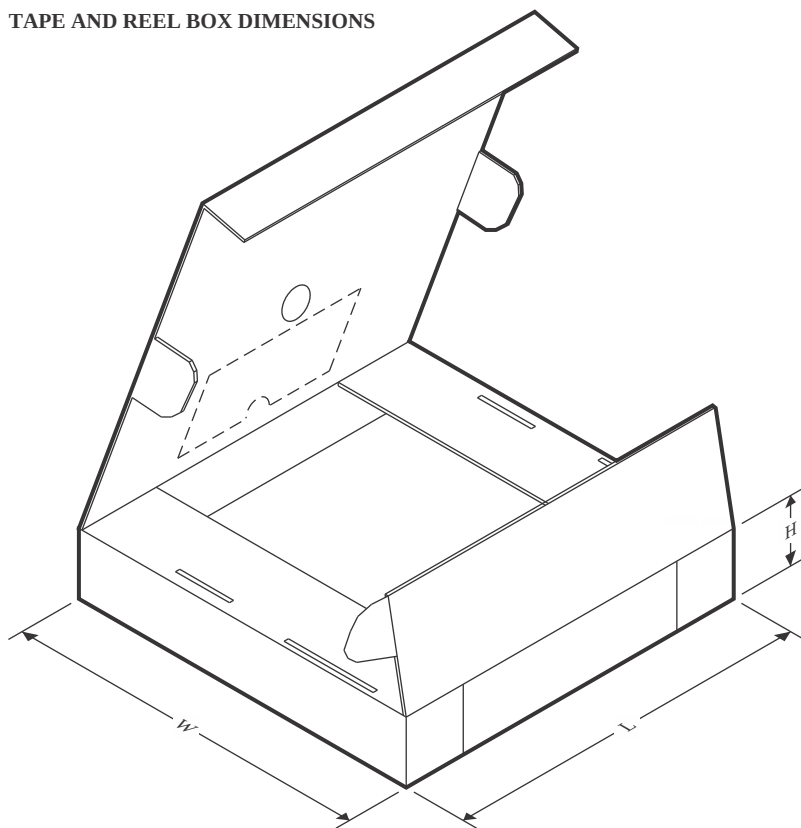
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR5870IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5870IRGCR  | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR58721IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR58721IRGCR | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5872IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5872IRGCR  | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR59221IG56R | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR59221IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR59221IRGCR | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5922IG56R  | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR5922IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5922IRGCR  | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR5970IPMR   | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5970IRGCR  | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430FR59721IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR59721IRGCR | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |

---

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR5972IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR5972IRGCR | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |

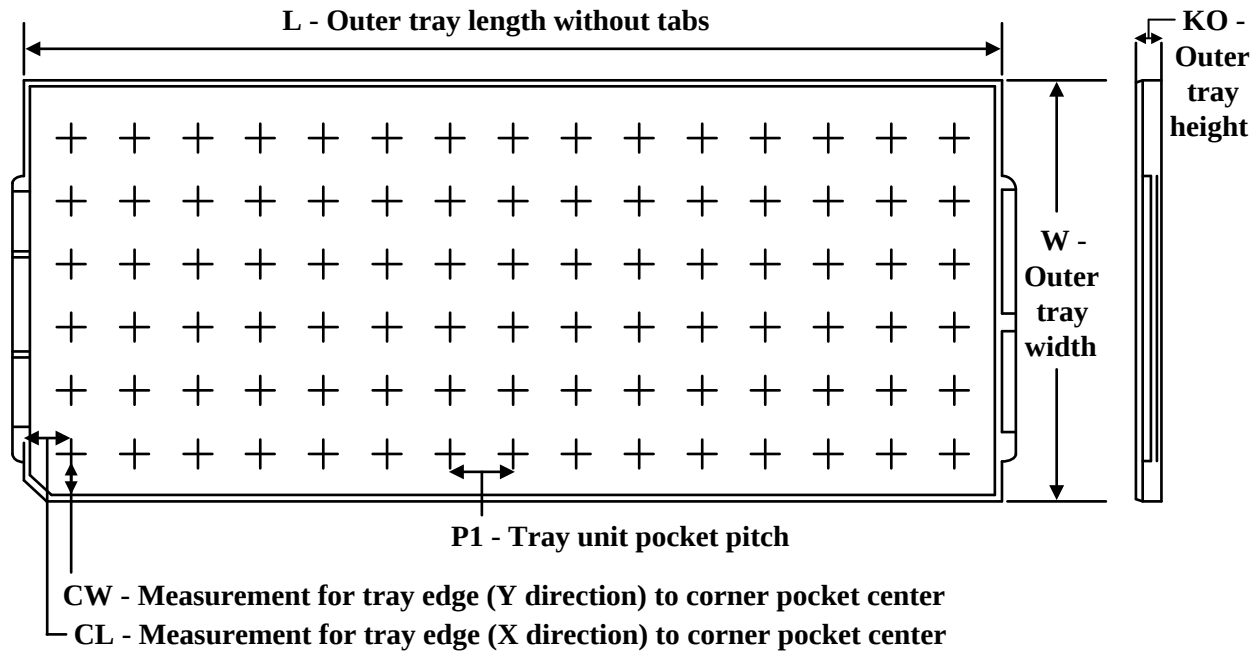
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR5870IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5870IRGCR  | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR58721IPMR  | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR58721IRGCR | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR5872IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5872IRGCR  | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR59221IG56R | TSSOP        | DGG             | 56   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR59221IPMR  | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR59221IRGCR | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR5922IG56R  | TSSOP        | DGG             | 56   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR5922IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5922IRGCR  | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR5970IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5970IRGCR  | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR59721IPMR  | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR59721IRGCR | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |
| MSP430FR5972IPMR   | LQFP         | PM              | 64   | 1000 | 336.6       | 336.6      | 41.3        |
| MSP430FR5972IRGCR  | VQFN         | RGC             | 64   | 2000 | 367.0       | 367.0      | 38.0        |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| MSP430FR5922IPM    | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5922IPM.A  | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR59721IPM   | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR59721IPM.A | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5972IPM    | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |
| MSP430FR5972IPM.A  | PM           | LQFP         | 64   | 160 | 8 X 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |

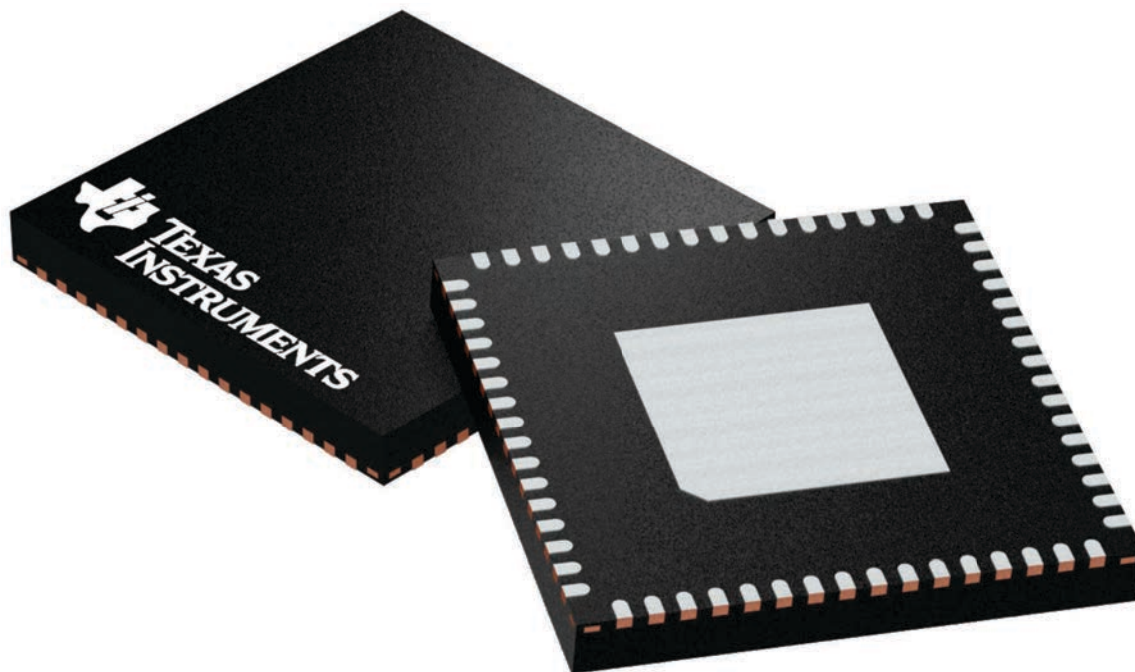
## GENERIC PACKAGE VIEW

**RGC 64**

**VQFN - 1 mm max height**

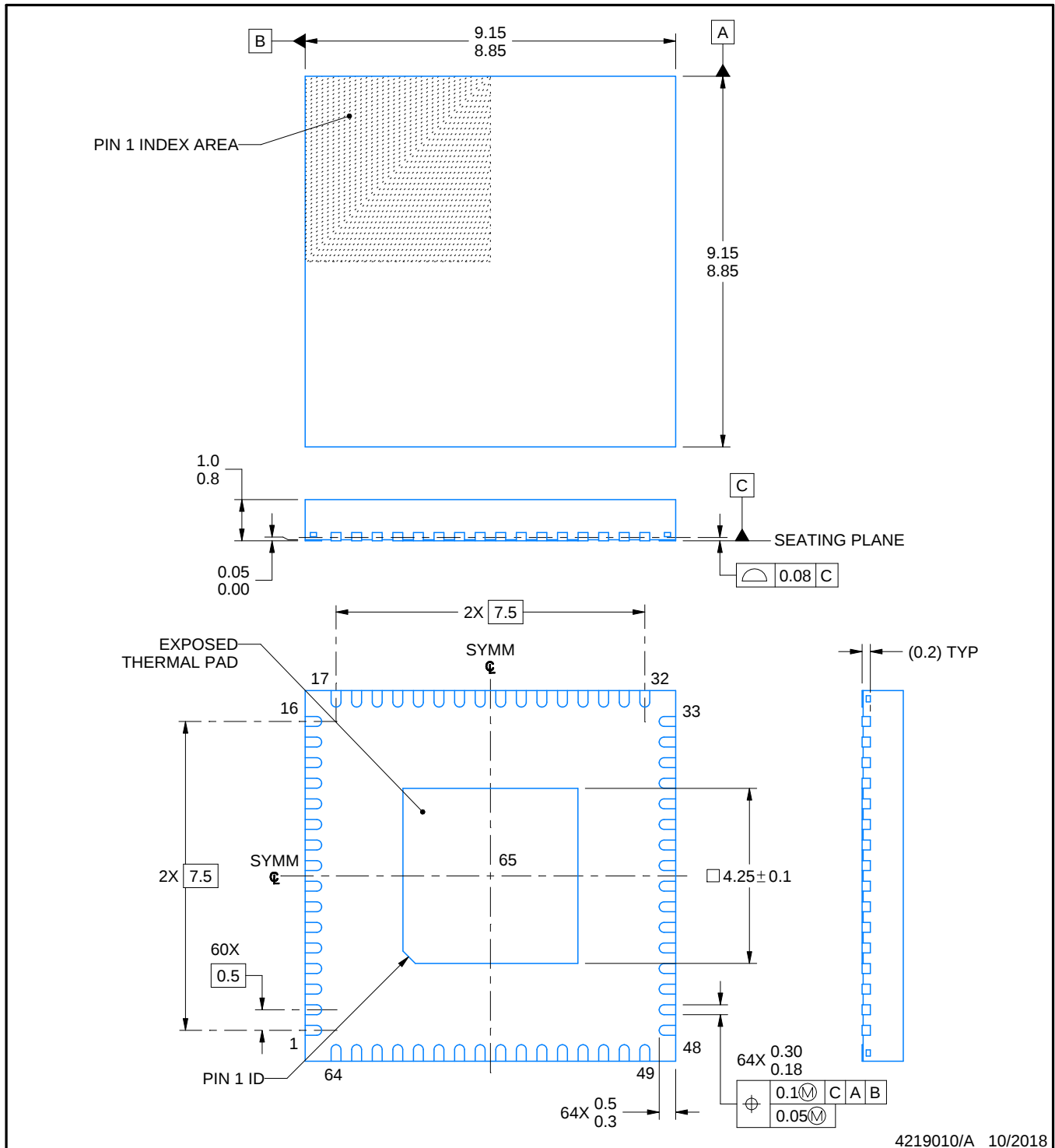
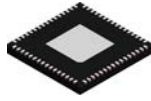
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224597/A



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

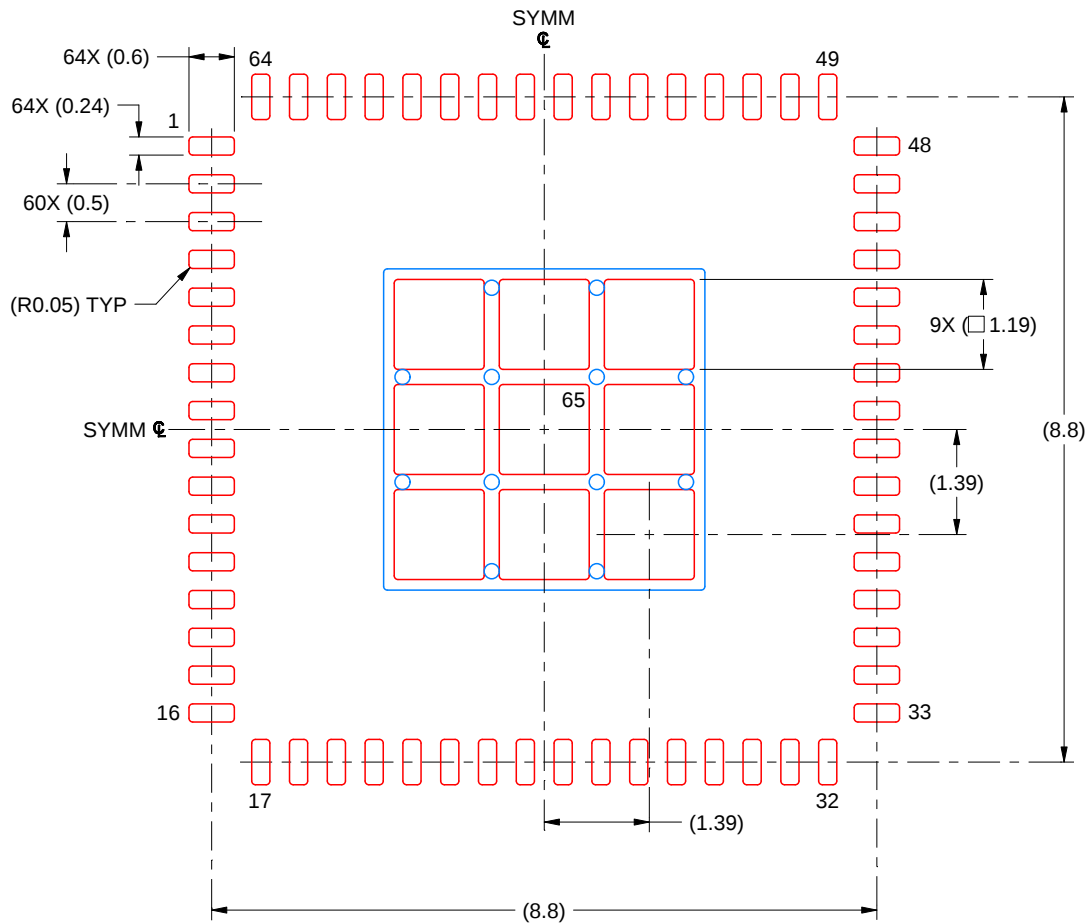


# EXAMPLE STENCIL DESIGN

RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



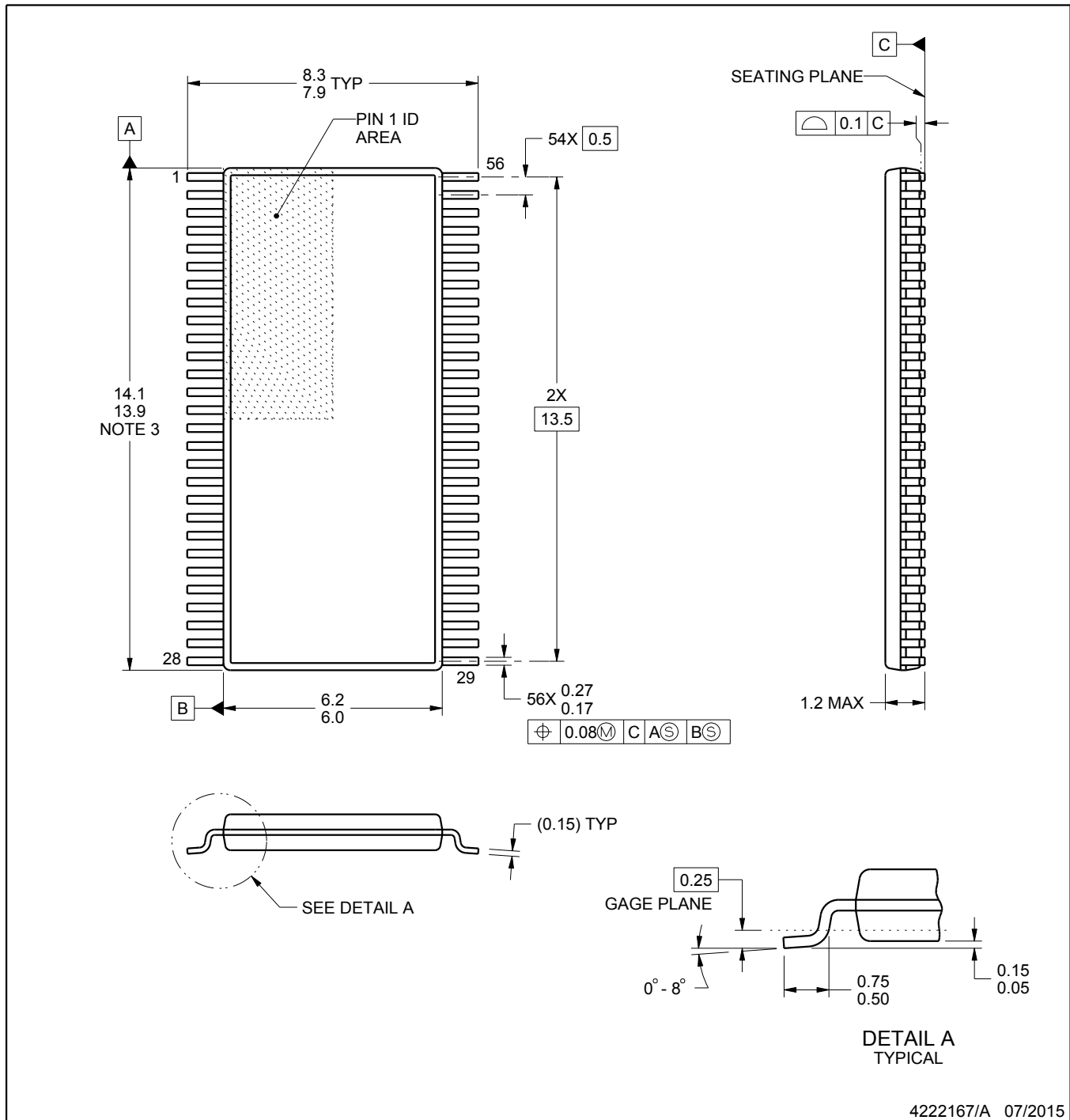
SOLDER PASTE EXAMPLE  
 BASED ON 0.125 MM THICK STENCIL  
 SCALE: 10X

EXPOSED PAD 65  
 71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4222167/A 07/2015

## NOTES:

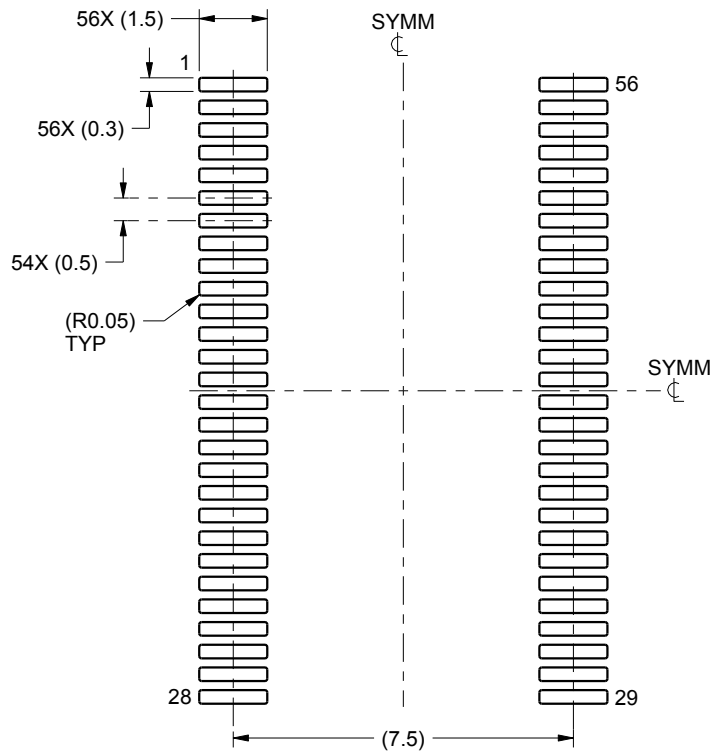
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

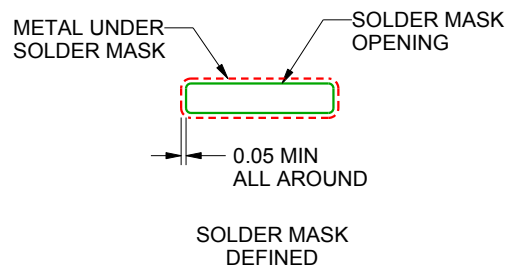
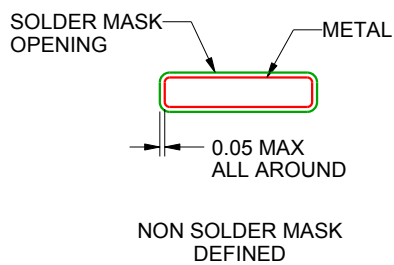
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

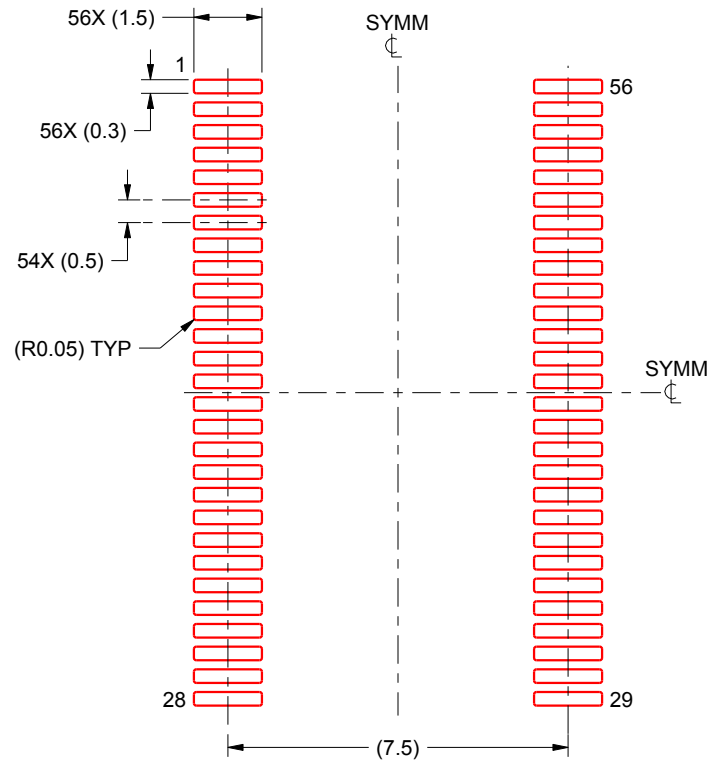
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

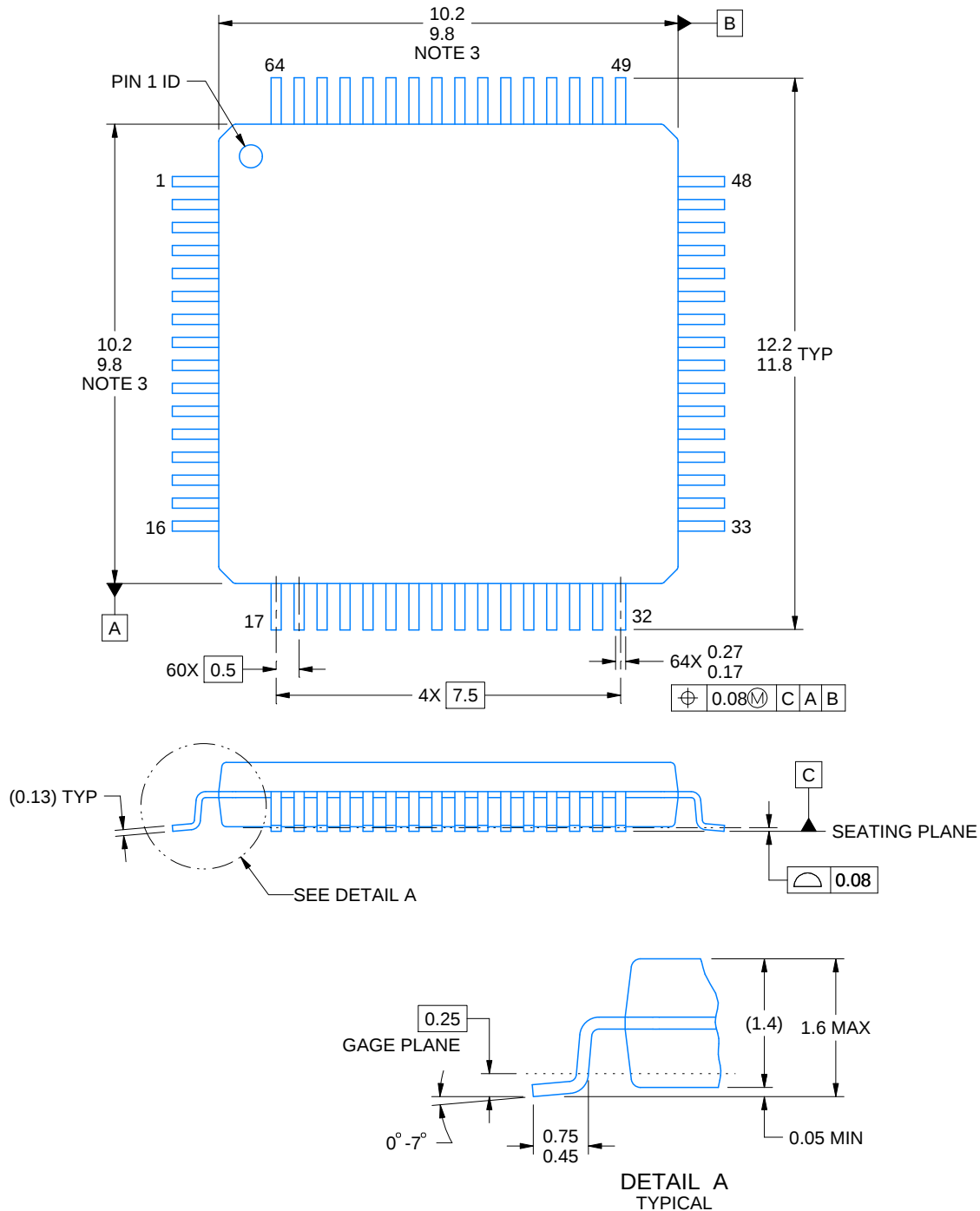
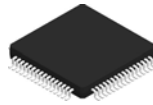


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4215162/A 03/2017

## NOTES:

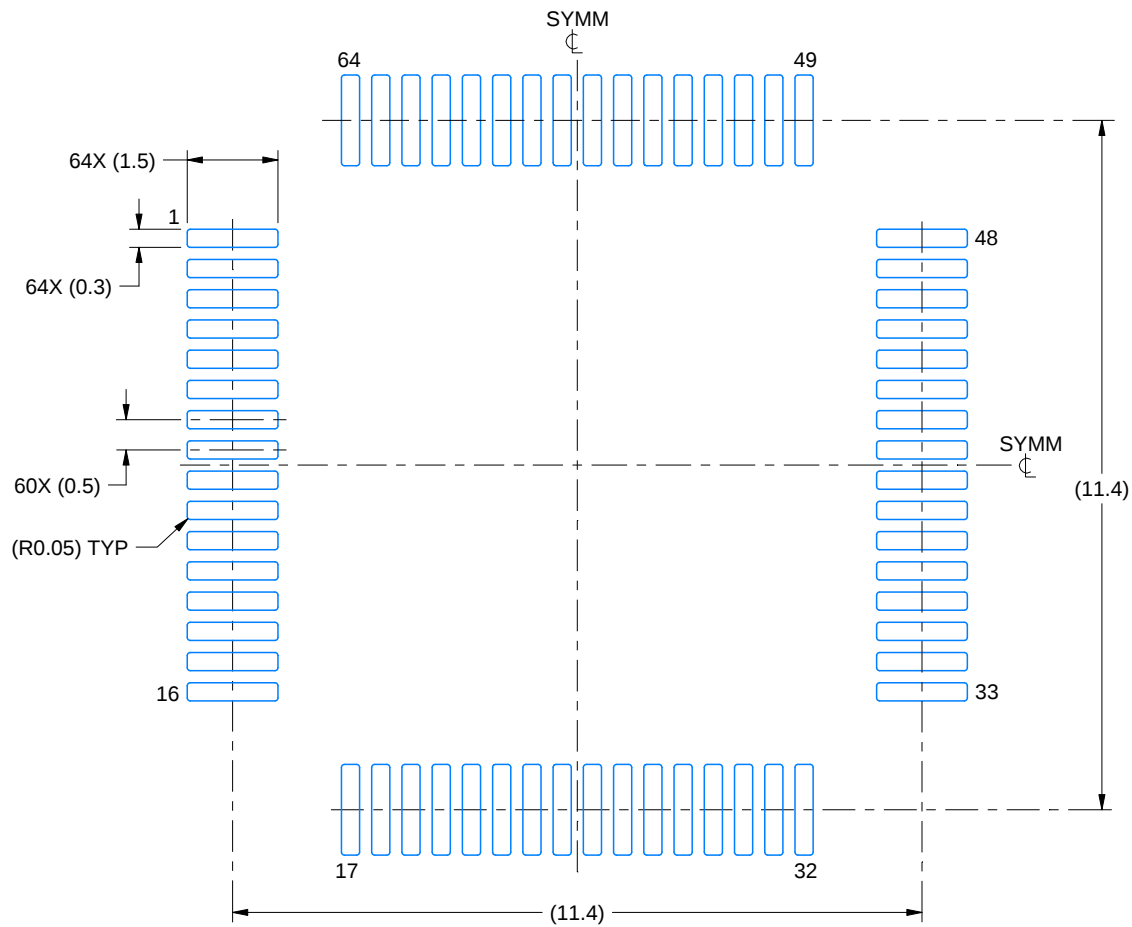
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

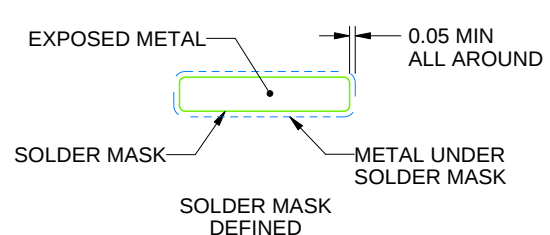
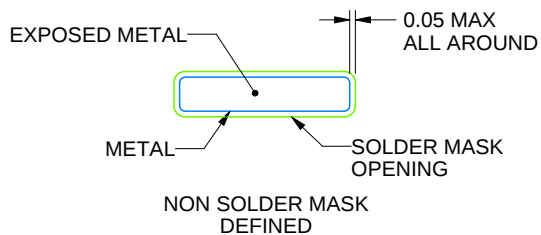
PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

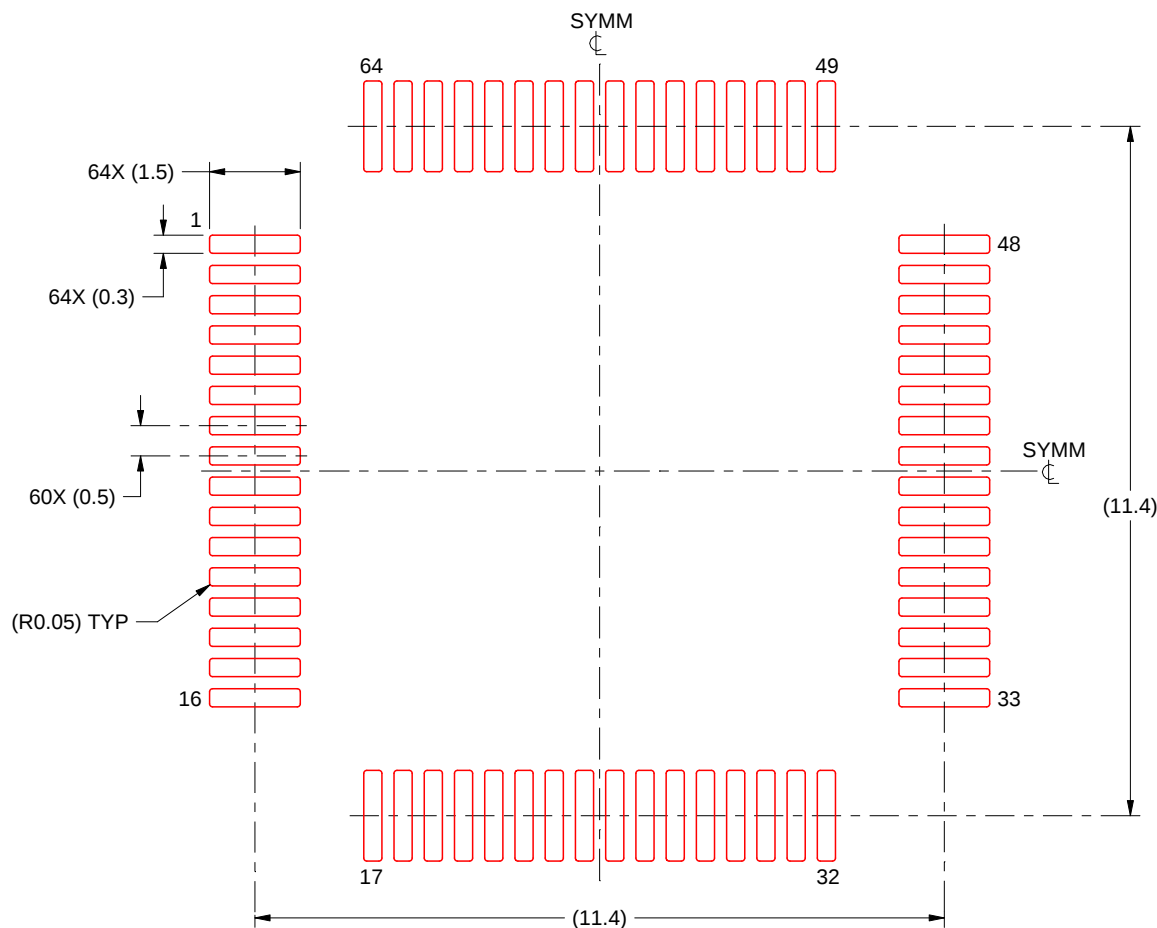
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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