# MSP430F6459-HIREL ミクスト・シグナル・マイクロコントローラ

## 1 デバイスの概要

### 1.1 特長

- 低い電源電圧範囲:
  3.6Vから最低1.8Vまで
- 非常に低い消費電力
  - アクティブ・モード(AM):
    すべてのシステム・クロックがアクティブ:
    8MHz、3V、フラッシュ・プログラム実行で
    295µA/MHz (標準値)
  - スタンバイ・モード(LPM3):
    水晶振動子によるウォッチドッグ、電源スーパーバイザが動作、すべてのRAMを保持、高速ウェークアップ:
    2.2Vで2µA、3Vで2.2µA (標準値)
  - シャットダウン、リアルタイム・クロック(RTC)モード(LPM3.5):
    シャットダウン・モード、水晶振動子によるアクティブRTC:
    3Vで1.1µA (標準値)
  - シャットダウン・モード(LPM4.5):
    3Vで0.45µA (標準値)
- スタンバイ・モードから3µs以内にウェークアップ(標準値)
- 16ビットRISCアーキテクチャ、拡張メモリ、最大20MHzのシステム・クロック
- 柔軟な電力管理システム
  - プログラム可能な、レギュレートされたコア電源電圧を持つ、完全に統合されたLDO
  - 電源電圧の管理、監視、およびブラウンアウト
- 統合クロック・システム
  - FLL制御ループによる周波数安定化
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 低周波数のトリムされた内部基準ソース(REFO)
  - 32kHzの水晶振動子(XT1)
  - 最高32MHzの高周波数水晶振動子(XT2)
- 4つの16ビット・タイマと3、5、または7本のキャプチャ/比較レジスタ
- 3つのユニバーサル・シリアル通信インターフェイス(USCI)
  - USCI_A0、USCI_A1、USCI_A2がそれぞれ次の機能をサポート
    - 自動ボーレート検出機能付きの拡張UART
    - IrDAエンコーダおよびデコーダ
    - 同期SPI
  - USCI_B0、USCI_B1、USCI_B2がそれぞれ次の機能をサポート
    - $I^2C$
    - 同期SPI
- 内部共有リファレンス、サンプル・アンド・ホールド、オートスキャン機能搭載の12ビットのA/Dコンバータ(ADC)
- 同期機能付きの2つの12ビットD/Aコンバータ(DAC)
- 電圧コンパレータ
- 最大160セグメントのコントラスト制御を搭載した内蔵LCDドライバ
- ハードウェア・マルチプライヤで32ビットの演算をサポート
- シリアルのオンボード・プログラミング、外部のプログラミング電圧不要
- 6チャネルの内部DMA
- 電源電圧バックアップ・スイッチ付きのRTCモジュール

### 1.2 アプリケーション

- アナログおよびデジタル・センサ・システム
- デジタル・モータの制御
- リモート・コントロール
- サーモスタット
- デジタル・タイマ
- ハンドヘルド・メータ

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## 1.3 概要

TI MSP430™ファミリの超低消費電力マイクロコントローラは複数のデバイスで構成され、それぞれが各種のアプリケーションを対象とする異なるペリフェラルの組となっています。このアーキテクチャは5つの低消費電力モードを持ち、携帯用測定器用途でバッテリ駆動時間を延長するよう最適化されています。このデバイスには、強力な16ビットRISC CPU、16ビット・レジスタ、およびコンスタント・ジェネレータが搭載されており、コード効率が最大限に発揮されます。デジタル制御発振器(DCO)により、低消費電力モードからアクティブ・モードへ3µs (標準値)以内でウェークアップできます。

MSP430F6459-HIRELはマイクロコントローラで、3.3V LDO、4つの16ビット・タイマ、高性能の12ビットADC、3つのUSCI、ハードウェア・マルチプライヤ、DMA、アラーム機能付きのRTCモジュール、コンパレータ、および最大74本のI/Oピンが搭載されています。

これらのデバイスの代表的なアプリケーションとして、デジタル・センサ・システム、デジタル・モータの制御、リモート・コントロール、サーモスタット、デジタル・タイマ、ハンドヘルド・メータが挙げられます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称)(2) |
|---|---|---|
| MSP430F6459-HIREL | PZ (100) | 16.0mm×16.0mm |

(1) 最新のデバイス、パッケージ、および注文情報については、9の「*付録:パッケージ・オプション*」または、www.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

## 1.4 機能ブロック図

このデバイスの機能ブロック図を、図 1-1に示します。

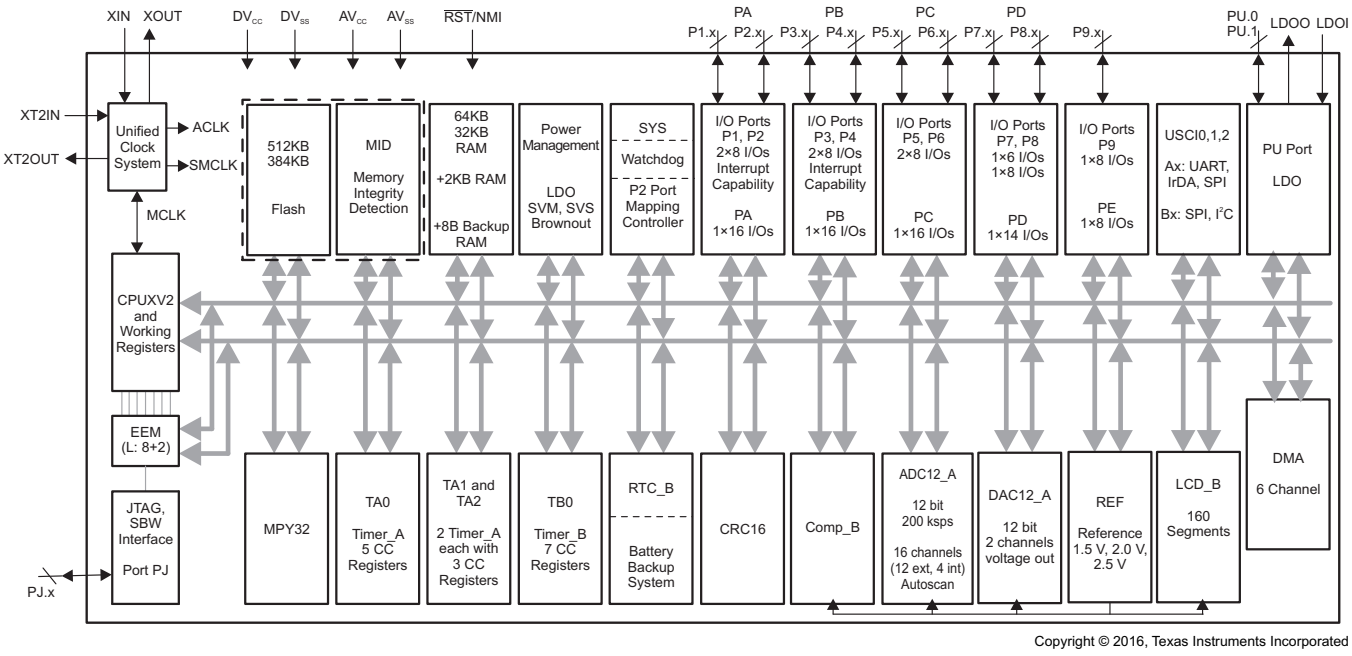


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**図 1-1. 機能ブロック図**


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## 2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 2016年7月発行のものから更新 | Page |
| --- | --- |
| • 完全なデータ・マニュアルをリリース、ステータスを量産データへ 変更 | 1 |


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# 3 Device Comparison

**Table 3-1. Device Comparison(1)(2)**

| DEVICE | FLASH (KB) | SRAM (KB)(3) | Timer_A(4) | Timer_B(5) | USCI | | ADC12_A (Ch) | DAC12_A (Ch) | Comp_B (Ch) | I/O | USB | LCD | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | CHANNEL A: UART, IrDA, SPI | CHANNEL B: SPI, $I^2C$ | | | | | | | |
| MSP430F6459 | 512 | 66 | 5, 3, 3 | 7 | 3 | 3 | 12 ext, 4 int | 2 | 12 | 74 | No | Yes | 100 PZ |

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.
(4) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(5) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

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# 4 Terminal Configuration and Functions

## 4.1 Pin Diagram

Figure 4-1 shows the pinout diagram.

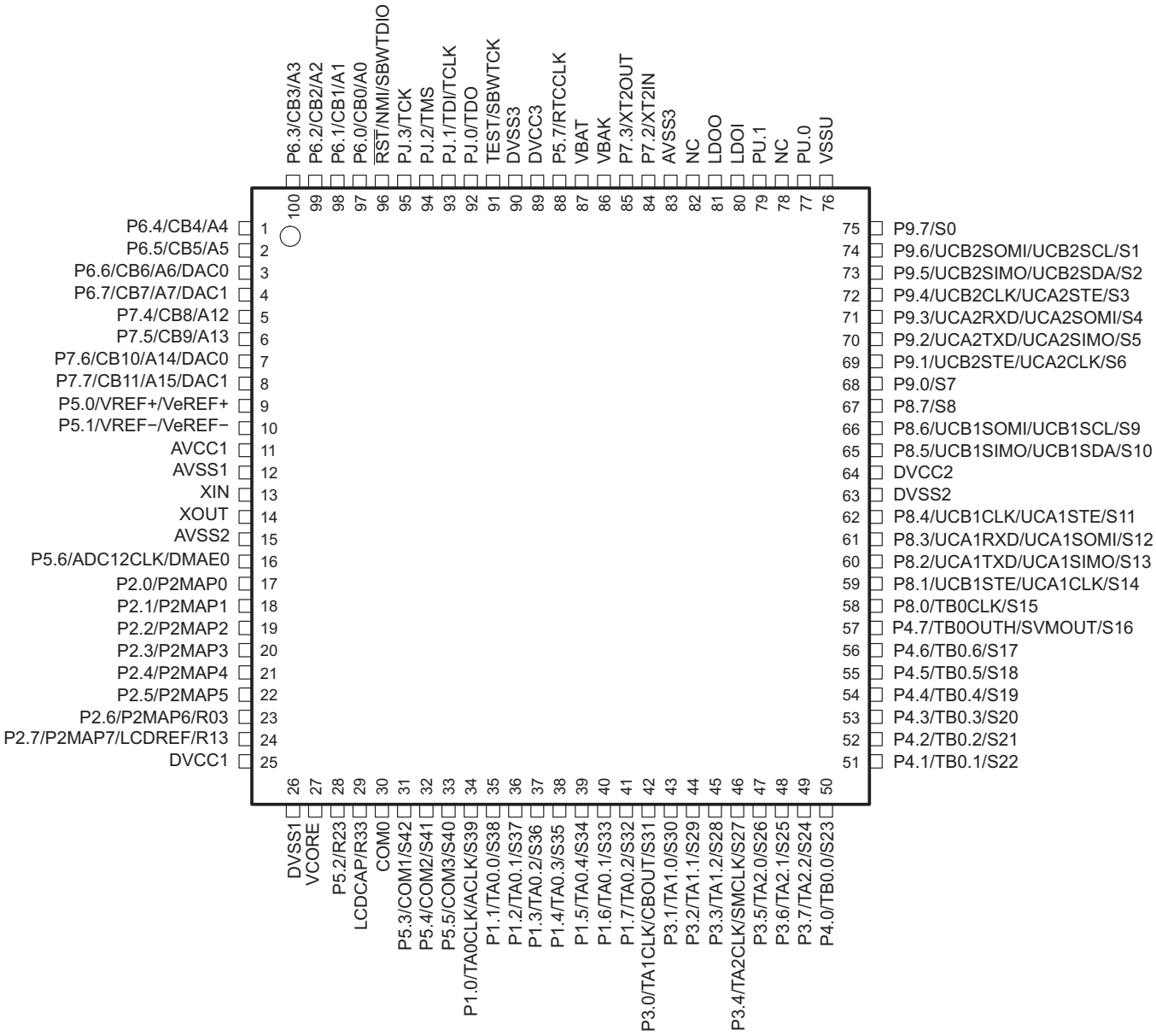


**Figure 4-1. PZ S-PQFP-G100 Package**


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## 4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

**Table 4-1. Signal Descriptions**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P6.4/CB4/A4 | 1 | I/O | General-purpose digital I/O<br>Comparator_B input CB4<br>Analog input A4 – ADC |
| P6.5/CB5/A5 | 2 | I/O | General-purpose digital I/O<br>Comparator_B input CB5<br>Analog input A5 – ADC |
| P6.6/CB6/A6/DAC0 | 3 | I/O | General-purpose digital I/O<br>Comparator_B input CB6<br>Analog input A6 – ADC<br>DAC12.0 output |
| P6.7/CB7/A7/DAC1 | 4 | I/O | General-purpose digital I/O<br>Comparator_B input CB7<br>Analog input A7 – ADC<br>DAC12.1 output |
| P7.4/CB8/A12 | 5 | I/O | General-purpose digital I/O<br>Comparator_B input CB8<br>Analog input A12 –ADC |
| P7.5/CB9/A13 | 6 | I/O | General-purpose digital I/O<br>Comparator_B input CB9<br>Analog input A13 – ADC |
| P7.6/CB10/A14/DAC0 | 7 | I/O | General-purpose digital I/O<br>Comparator_B input CB10<br>Analog input A14 – ADC<br>DAC12.0 output |
| P7.7/CB11/A15/DAC1 | 8 | I/O | General-purpose digital I/O<br>Comparator_B input CB11<br>Analog input A15 – ADC<br>DAC12.1 output |
| P5.0/VREF+/VeREF+ | 9 | I/O | General-purpose digital I/O<br>Output of reference voltage to the ADC<br>Input for an external reference voltage to the ADC |
| P5.1/VREF-/VeREF- | 10 | I/O | General-purpose digital I/O<br>Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| AVCC1 | 11 | | Analog power supply |
| AVSS1 | 12 | | Analog ground supply |
| XIN | 13 | I | Input terminal for crystal oscillator XT1 |
| XOUT | 14 | O | Output terminal of crystal oscillator XT1 |
| AVSS2 | 15 | | Analog ground supply |

(1) I = input, O = output, N/A = not available on this package offering.

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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P5.6/ADC12CLK/DMAE0 | 16 | I/O | General-purpose digital I/O<br>Conversion clock output ADC<br>DMA external trigger input |
| P2.0/P2MAP0 | 17 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output |
| P2.1/P2MAP1 | 18 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave in, master out; USCI_B0 I2C data |
| P2.2/P2MAP2 | 19 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave out, master in; USCI_B0 I2C clock |
| P2.3/P2MAP3 | 20 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable |
| P2.4/P2MAP4 | 21 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in, master out |
| P2.5/P2MAP5 | 22 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_A0 UART receive data; USCI_A0 slave out, master in |
| P2.6/P2MAP6/R03 | 23 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: no secondary function<br>Input/output port of lowest analog LCD voltage (V5) |
| P2.7/P2MAP7/LCDREF/R13 | 24 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: no secondary function<br>External reference voltage input for regulated LCD voltage<br>Input/output port of third most positive analog LCD voltage (V3 or V4) |
| DVCC1 | 25 | | Digital power supply |
| DVSS1 | 26 | | Digital ground supply |
| VCORE(2) | 27 | | Regulated core power supply (internal use only, no external current loading) |
| P5.2/R23 | 28 | I/O | General-purpose digital I/O<br>Input/output port of second most positive analog LCD voltage (V2) |
| LCDCAP/R33 | 29 | I/O | LCD capacitor connection<br>Input/output port of most positive analog LCD voltage (V1) |
| COM0 | 30 | O | LCD common output COM0 for LCD backplane |
| P5.3/COM1/S42 | 31 | I/O | General-purpose digital I/O<br>LCD common output COM1 for LCD backplane<br>LCD segment output S42 |
| P5.4/COM2/S41 | 32 | I/O | General-purpose digital I/O<br>LCD common output COM2 for LCD backplane<br>LCD segment output S41 |
| P5.5/COM3/S40 | 33 | I/O | General-purpose digital I/O<br>LCD common output COM3 for LCD backplane<br>LCD segment output S40 |

(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.


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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P1.0/TA0CLK/ACLK/S39 | 34 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 clock signal TACLK input<br>ACLK output (divided by 1, 2, 4, 8, 16, or 32)<br>LCD segment output S39 |
| P1.1/TA0.0/S38 | 35 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>BSL transmit output<br>LCD segment output S38 |
| P1.2/TA0.1/S37 | 36 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>BSL receive input<br>LCD segment output S37 |
| P1.3/TA0.2/S36 | 37 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output S36 |
| P1.4/TA0.3/S35 | 38 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR3 capture: CCI3A input compare: Out3 output<br>LCD segment output S35 |
| P1.5/TA0.4/S34 | 39 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output<br>LCD segment output S34 |
| P1.6/TA0.1/S33 | 40 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output<br>LCD segment output S33 |
| P1.7/TA0.2/S32 | 41 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output<br>LCD segment output S32 |
| P3.0/TA1CLK/CBOUT/S31 | 42 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 clock input<br>Comparator_B output<br>LCD segment output S31 |
| P3.1/TA1.0/S30 | 43 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR0: CCI0A/CCI0B input, compare: Out0 output<br>LCD segment output S30 |
| P3.2/TA1.1/S29 | 44 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR1: CCI1A/CCI1B input, compare: Out1 output<br>LCD segment output S29 |
| P3.3/TA1.2/S28 | 45 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR2: CCI2A/CCI2B input, compare: Out2 output<br>LCD segment output S28 |

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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P3.4/TA2CLK/SMCLK/S27 | 46 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 clock input<br>SMCLK output<br>LCD segment output S27 |
| P3.5/TA2.0/S26 | 47 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR0: CCI0A/CCI0B input, compare: Out0 output<br>LCD segment output S26 |
| P3.6/TA2.1/S25 | 48 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR1: CCI1A/CCI1B input, compare: Out1 output<br>LCD segment output S25 |
| P3.7/TA2.2/S24 | 49 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR2: CCI2A/CCI2B input, compare: Out2 output<br>LCD segment output S24 |
| P4.0/TB0.0/S23 | 50 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output<br>LCD segment output S23 |
| P4.1/TB0.1/S22 | 51 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output<br>LCD segment output S22 |
| P4.2/TB0.2/S21 | 52 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output<br>LCD segment output S21 |
| P4.3/TB0.3/S20 | 53 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output<br>LCD segment output S20 |
| P4.4/TB0.4/S19 | 54 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output<br>LCD segment output S19 |
| P4.5/TB0.5/S18 | 55 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output<br>LCD segment output S18 |
| P4.6/TB0.6/S17 | 56 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output<br>LCD segment output S17 |
| P4.7/TB0OUTH/SVMOUT/S16 | 57 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0: Switch all PWM outputs high impedance<br>SVM output<br>LCD segment output S16 |
| P8.0/TB0CLK/S15 | 58 | I/O | General-purpose digital I/O<br>Timer TB0 clock input<br>LCD segment output S15 |


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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P8.1/UCB1STE/UCA1CLK/S14 | 59 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave transmit enable<br>USCI_A1 clock input/output<br>LCD segment output S14 |
| P8.2/UCA1TXD/UCA1SIMO/S13 | 60 | I/O | General-purpose digital I/O<br>USCI_A1 UART transmit data<br>USCI_A1 SPI slave in, master out<br>LCD segment output S13 |
| P8.3/UCA1RXD/UCA1SOMI/S12 | 61 | I/O | General-purpose digital I/O<br>USCI_A1 UART receive data<br>USCI_A1 SPI slave out, master in<br>LCD segment output S12 |
| P8.4/UCB1CLK/UCA1STE/S11 | 62 | I/O | General-purpose digital I/O<br>USCI_B1 clock input/output<br>USCI_A1 SPI slave transmit enable<br>LCD segment output S11 |
| DVSS2 | 63 | | Digital ground supply |
| DVCC2 | 64 | | Digital power supply |
| P8.5/UCB1SIMO/UCB1SDA/S10 | 65 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave in, master out<br>USCI_B1 I2C data<br>LCD segment output S10 |
| P8.6/UCB1SOMI/UCB1SCL/S9 | 66 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave out, master in<br>USCI_B1 I2C clock<br>LCD segment output S9 |
| P8.7/S8 | 67 | I/O | General-purpose digital I/O<br>LCD segment output S8 |
| P9.0/S7 | 68 | I/O | General-purpose digital I/O<br>LCD segment output S7 |
| P9.1/UCB2STE/UCA2CLK/S6 | 69 | I/O | General-purpose digital I/O<br>USCI_B2 SPI slave transmit enable<br>USCI_A2 clock input/output<br>LCD segment output S6 |
| P9.2/UCA2TXD/UCA2SIMO/S5 | 70 | I/O | General-purpose digital I/O<br>USCI_A2 UART transmit data<br>USCI_A2 SPI slave in, master out<br>LCD segment output S5 |
| P9.3/UCA2RXD/UCA2SOMI/S4 | 71 | I/O | General-purpose digital I/O<br>USCI_A2 UART receive data<br>USCI_A2 SPI slave out, master in<br>LCD segment output S4 |

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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P9.4/UCB2CLK/UCA2STE/S3 | 72 | I/O | General-purpose digital I/O<br>USCI_B2 clock input/output<br>USCI_A2 SPI slave transmit enable<br>LCD segment output S3 |
| P9.5/UCB2SIMO/UCB2SDA/S2 | 73 | I/O | General-purpose digital I/O<br>USCI_B2 SPI slave in, master out<br>USCI_B2 I2C data<br>LCD segment output S2 |
| P9.6/UCB2SOMI/UCB2SCL/S1 | 74 | I/O | General-purpose digital I/O<br>USCI_B2 SPI slave out, master in<br>USCI_B2 I2C clock<br>LCD segment output S1 |
| P9.7/S0 | 75 | I/O | General-purpose digital I/O<br>LCD segment output S0 |
| VSSU | 76 | | PU ground supply |
| PU.0/DP | 77 | I/O | PU control register (Port U is supplied the LDOO rail) |
| NC | 78 | | Not connected |
| PU.1/DM | 79 | I/O | PU control register (Port U is supplied the LDOO rail) |
| LDOI | 80 | | LDO input |
| LDOO | 81 | | LDO output |
| NC | 82 | | Not connected |
| AVSS3 | 83 | | Analog ground supply |
| P7.2/XT2IN | 84 | I/O | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2 |
| P7.3/XT2OUT | 85 | I/O | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2 |
| VBAK | 86 | | Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see $C_{BAK}$ in Section 5.3. |
| VBAT | 87 | | Backup supply voltage. If backup voltage is not supplied, connect to DVCC externally. |
| P5.7/RTCCLK | 88 | I/O | General-purpose digital I/O<br>RTCCLK output |
| DVCC3 | 89 | | Digital power supply |
| DVSS3 | 90 | | Digital ground supply |
| TEST/SBWTCK | 91 | I | Test mode pin – select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| PJ.0/TDO | 92 | I/O | General-purpose digital I/O<br>Test data output port |
| PJ.1/TDI/TCLK | 93 | I/O | General-purpose digital I/O<br>Test data input or test clock input |
| PJ.2/TMS | 94 | I/O | General-purpose digital I/O<br>Test mode select |
| PJ.3/TCK | 95 | I/O | General-purpose digital I/O<br>Test clock |


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**Table 4-1. Signal Descriptions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 96 | I/O | Reset input active low(3)<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |
| P6.0/CB0/A0 | 97 | I/O | General-purpose digital I/O<br>Comparator_B input CB0<br>Analog input A0 – ADC |
| P6.1/CB1/A1 | 98 | I/O | General-purpose digital I/O<br>Comparator_B input CB1<br>Analog input A1 – ADC |
| P6.2/CB2/A2 | 99 | I/O | General-purpose digital I/O<br>Comparator_B input CB2<br>Analog input A2 – ADC |
| P6.3/CB3/A3 | 100 | I/O | General-purpose digital I/O<br>Comparator_B input CB3<br>Analog input A3 – ADC |
| Reserved | N/A | | Reserved BGA package balls. TI recommends connecting to ground (DVSS, AVSS). |

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | –0.3 | 4.1 | V |
| Voltage applied to any pin (excluding VCORE, VBUS, V18)(2) | –0.3 | $V_{CC}$ + 0.3 | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, $T_J$ | –40 | 105 | °C |
| Storage temperature, $T_{stg}$(3) | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

Typical values are specified at $V_{CC}$ = 3.3 V and $T_J$ = 25°C (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and flash programming (AVCC1 = DVCC1 = DVCC2 = DVCC3 = $DV_{CC}$ = $V_{CC}$)(1)(2) | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | | 3.6 | |
| $V_{SS}$ | Supply voltage (AVSS1 = AVSS2 = AVSS3 = DVSS1 = DVSS2 = DVSS3 = $V_{SS}$) | | | 0 | | V |
| $V_{BAT,RTC}$ | Backup-supply voltage with RTC operational | $T_J$ = –40°C to 105°C | 1.7 | | 3.6 | V |
| $V_{BAT,MEM}$ | Backup-supply voltage with backup memory retained | $T_J$ = –40°C to 105°C | 1.2 | | 3.6 | V |
| $T_J$ | Operating junction temperature | T version | –40 | | 105 | °C |
| $C_{BAK}$ | Capacitance at pin VBAK | | 1 | 4.7 | 10 | nF |
| $C_{VCORE}$ | Capacitor at VCORE(3) | | | 470 | | nF |
| $C_{DVCC}$ / $C_{VCORE}$ | Capacitor ratio of DVCC to VCORE | | 10 | | | |

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Table 5-11 threshold parameters for the exact values and further details.
(3) A capacitor tolerance of ±20% or better is required.


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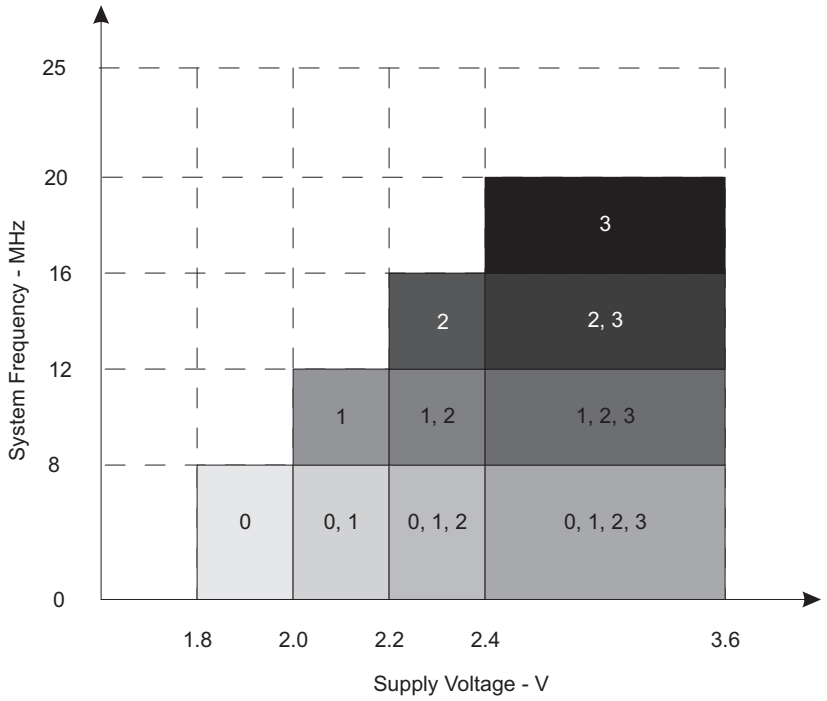
## Recommended Operating Conditions *(continued)*

Typical values are specified at $V_{CC}$ = 3.3 V and $T_J$ = 25°C (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(4)(5) (see Figure 5-1) | PMMCOREVx = 0, 1.8 V ≤ $V_{CC}$ ≤ 3.6 V (default condition) | 0 | | 8 | MHz |
| | | PMMCOREVx = 1, 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 12 | |
| | | PMMCOREVx = 2, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 16 | |
| | | PMMCOREVx = 3, 2.4 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 20 | |

(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.




NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 5-1. Frequency vs Supply Voltage**

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating junction temperature (unless otherwise noted)(1) (2) (3)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ Flash}$ | Flash | 3 V | 0 | 0.36 | 0.45 | 2.4 | 2.7 | | | | | mA |
| | | | 1 | 0.41 | | 2.7 | | 4.0 | 4.4 | | | |
| | | | 2 | 0.46 | | 2.9 | | 4.3 | | | | |
| | | | 3 | 0.51 | | 3.1 | | 4.5 | | 7.4 | | |
| $I_{AM,\ RAM}$ | RAM | 3 V | 0 | 0.18 | 0.25 | 1.0 | 1.3 | | | | | mA |
| | | | 1 | 0.20 | | 1.2 | | 1.7 | 1.9 | | | |
| | | | 2 | 0.22 | | 1.3 | | 2.0 | | | | |
| | | | 3 | 0.23 | | 1.4 | | 2.2 | | 3.6 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
$f_{ACLK}$ = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

## 5.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1) (2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | –40°C | | 25°C | | 60°C | | 105°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0(3) (4) | 2.2 V | 0 | 69 | | 73 | 95 | 79 | | 101 | 135 | µA |
| | | 3 V | 3 | 79 | | 83 | 120 | 87 | | 116 | 155 | |
| $I_{LPM2}$ | Low-power mode 2(5) (4) | 2.2 V | 0 | 6.1 | | 6.7 | 9.0 | 8.0 | | 22 | 40 | µA |
| | | 3 V | 3 | 6.5 | | 7.1 | 9.5 | 8.5 | | 24 | 42 | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode(6) (4) | 2.2 V | 0 | 1.5 | | 2.0 | 3.3 | 3.3 | | 18 | 34 | µA |
| | | | 1 | 1.7 | | 2.2 | | 3.6 | | 8.5 | | |
| | | | 2 | 1.9 | | 2.4 | | 3.8 | | 18.7 | | |
| | | 3 V | 0 | 1.8 | | 2.2 | 3.5 | 3.6 | | 18.3 | 35 | |
| | | | 1 | 1.9 | | 2.4 | | 3.8 | | 18.7 | | |
| | | | 2 | 2.1 | | 2.6 | | 4.0 | | 18.8 | | |
| | | | 3 | 2.1 | | 2.6 | 4.2 | 4.0 | | 19.4 | 37 | |
| $I_{LPM3,VLO,\ WDT}$ | Low-power mode 3, VLO mode, Watchdog enabled(7) (4) | 3 V | 0 | 1.0 | | 1.3 | 2.7 | 2.7 | | 17.2 | 34 | µA |
| | | | 1 | 1.1 | | 1.5 | | 2.8 | | 17.5 | | |
| | | | 2 | 1.1 | | 1.6 | | 2.9 | | 17.6 | | |
| | | | 3 | 1.1 | | 1.6 | 3.2 | 2.9 | | 18.2 | 35 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz
(4) Current for brownout included. Low-side supervisor and monitors disabled ($SVS_L$, $SVM_L$). High-side supervisor and monitor disabled ($SVS_H$, $SVM_H$). RAM retention enabled.
(5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
(7) Current for watchdog timer clocked by VLO included.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz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## Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current *(continued)*

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1) (2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | –40°C | | 25°C | | 60°C | | 105°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM4}$ | Low-power mode 4(8) (4) | 3 V | 0 | 0.9 | | 1.3 | 2.5 | 2.5 | | 17.1 | 34 | µA |
| | | | 1 | 1.0 | | 1.3 | | 2.6 | | 17.3 | | |
| | | | 2 | 1.0 | | 1.4 | | 2.7 | | 17.5 | | |
| | | | 3 | 1.0 | | 1.4 | 3.1 | 2.7 | | 18 | 36 | |
| $I_{LPM3.5,RTC,VCC}$ | Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin $DV_{CC}$ (9) | 3 V | | | | 0.5 | | | | 1.25 | 2.3 | µA |
| $I_{LPM3.5,RTC,VBAT}$ | Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT(10) | 3 V | | | | 0.6 | | | | 0.78 | 1.3 | µA |
| $I_{LPM3.5,RTC,TOT}$ | Total Low-power mode 3.5 (LPM3.5) current with active RTC(11) | 3 V | | 1.0 | | 1.1 | | 1.2 | | 1.93 | 3.3 | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5(12) | 3 V | | 0.4 | | 0.45 | 0.6 | 0.5 | | 1.21 | 2.4 | µA |

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz
(9) $V_{VBAT} = V_{CC} - 0.2$ V, $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active
(10) $V_{VBAT} = V_{CC} - 0.2$ V, $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK
(11) $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK
(12) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

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## 5.6 Low-Power Mode With LCD Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)(2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_J$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 60°C | | 105°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3\ LCD,\ int.\ bias}$ | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(3) (4) | 3 V | 0 | 2.7 | | 3.3 | 4.8 | 4.7 | | 18.3 | 35 | µA |
| | | | 1 | 2.9 | | 3.5 | | 5.0 | | 18.7 | | |
| | | | 2 | 3.0 | | 3.7 | | 5.2 | | 19 | | |
| | | | 3 | 3.1 | | 3.7 | 5.3 | 5.2 | | 19.3 | 37 | |
| $I_{LPM3\ LCD,CP}$ | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled(3) (5) | 2.2 V | 0 | | | 3.6 | | | | | | µA |
| | | | 1 | | | 3.7 | | | | | | |
| | | | 2 | | | 4.0 | | | | | | |
| | | 3 V | 0 | | | 3.5 | | | | | | |
| | | | 1 | | | 3.7 | | | | | | |
| | | | 2 | | | 3.8 | | | | | | |
| | | | 3 | | | 3.9 | | | | | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
Current for brownout included. Low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$) disabled. High-side supervisor ($SVS_H$) and high-side monitor ($SVM_H$) disabled. RAM retention enabled.
(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.
(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD}$ = 3 V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.


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## 5.7 Schmitt-Trigger Inputs – General-Purpose I/O(1)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 1.8 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor(2) | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

(1) The same parametrics apply to the clock input pin when the crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).
(2) Also applies to $\overline{RST}$ pin when pullup or pulldown resistor is enabled.

## 5.8 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | (1) (2) | 1.8 V, 3 V | | ±50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## 5.9 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –3 mA(1) | 1.8 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –10 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –5 mA(1) | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –15 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 3 mA(1) | 1.8 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 10 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 5 mA(1) | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 15 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

## 5.10 Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA(2) | 1.8 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA(3) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA(2) | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA(3) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

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## Outputs – General-Purpose I/O (Reduced Drive Strength) *(continued)*

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA(2) | 1.8 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA(3) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA(2) | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA(3) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

## 5.11 Thermal Resistance Characteristics for PZ Package

| PARAMETER | | PACKAGE | VALUE | UNIT |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air(1) | QFP (PZ) | 122 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance(2) | QFP (PZ) | 83 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance(3) | QFP (PZ) | 98 | °C/W |

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.


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## 5.12 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

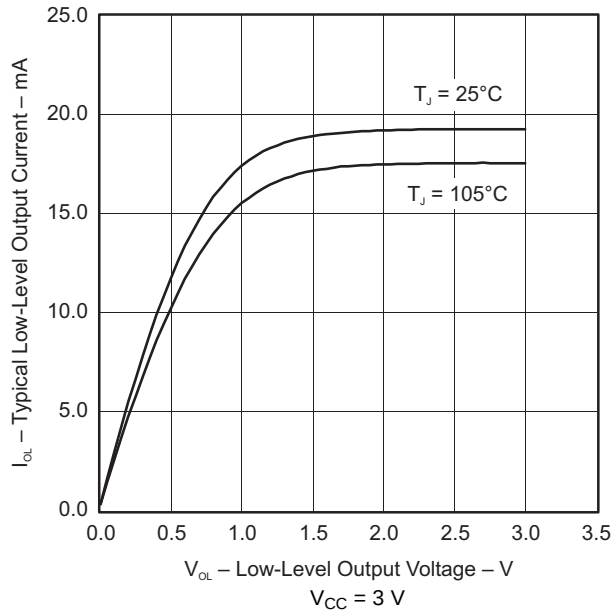


**Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage**

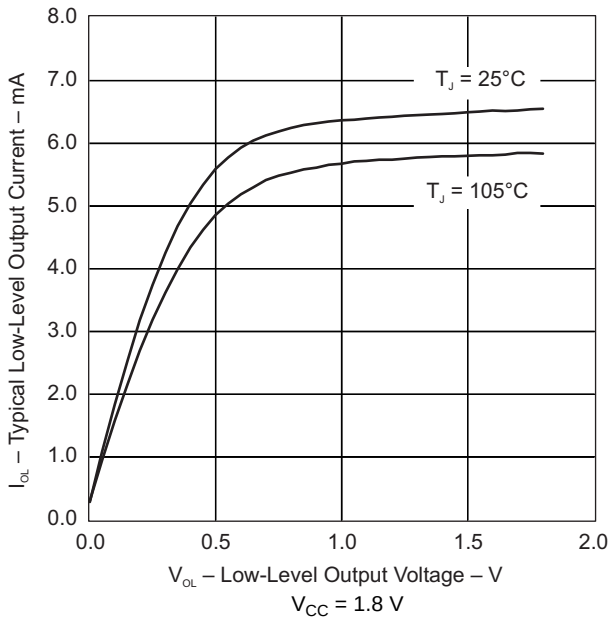


**Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage**

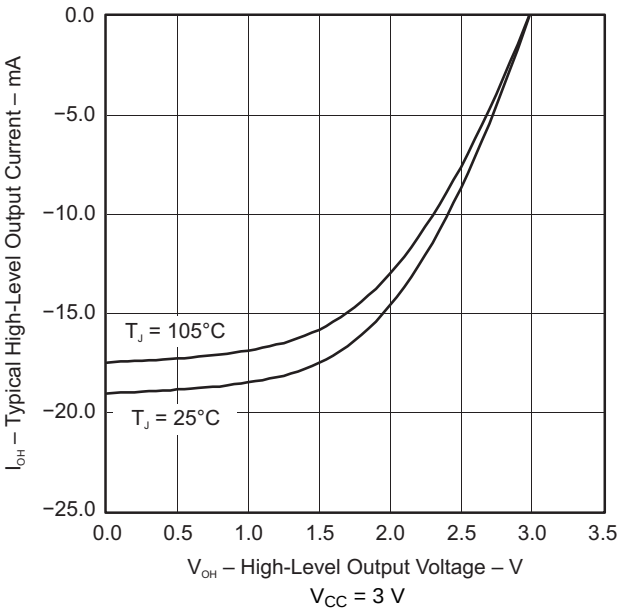


**Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage**

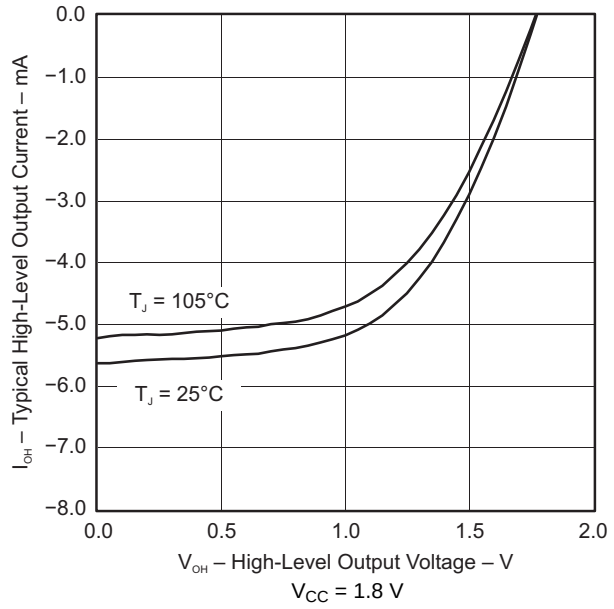


**Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage**

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## 5.13 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

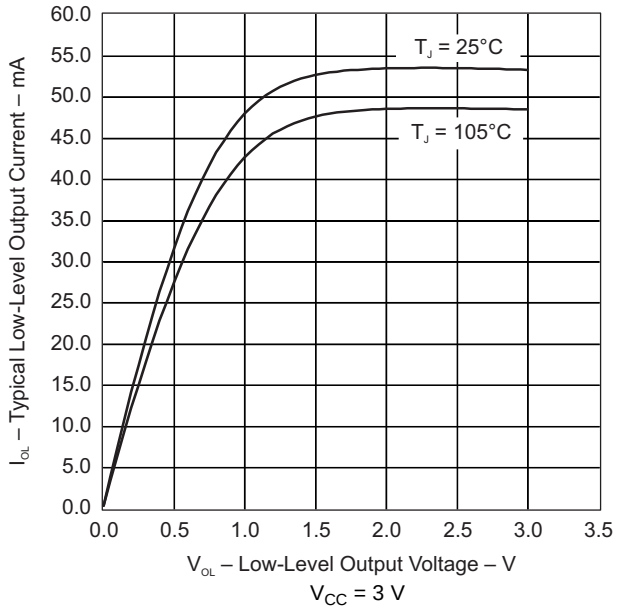


**Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage**

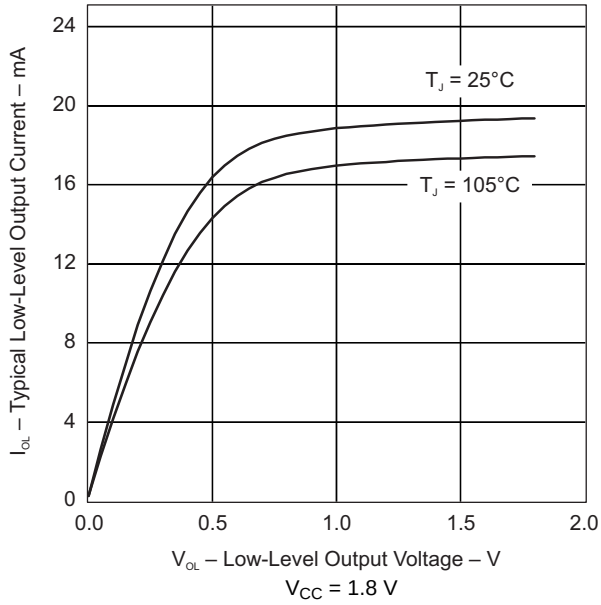


**Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage**

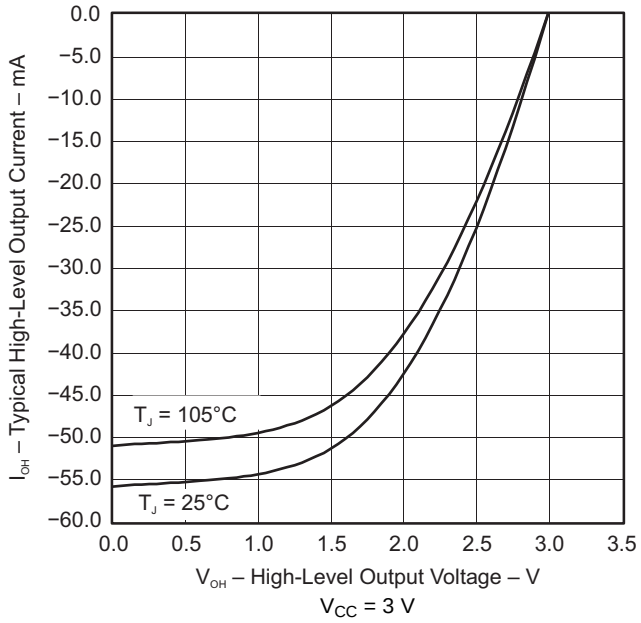


**Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage**

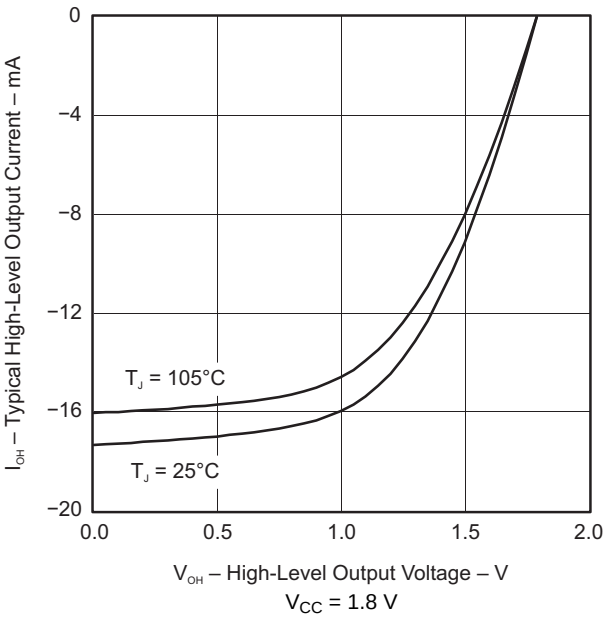


**Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage**


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## 5.14 Timing and Switching Characteristics

### 5.14.1 Power Supply Sequencing

TI recommends powering the AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

**Table 5-1. PMM, Brownout Reset (BOR)**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(DVCC\_BOR\_IT-)}$ | $BOR_H$ on voltage, $DV_{CC}$ falling level | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s | | | 1.45 | V |
| $V_{(DVCC\_BOR\_IT+)}$ | $BOR_H$ off voltage, $DV_{CC}$ rising level | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC\_BOR\_hys)}$ | $BOR_H$ hysteresis | | 60 | | 250 | mV |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | 2 | | | µs |

### 5.14.2 Clock Specifications

**Table 5-2. Inputs – Ports P1, P2, P3, and P4(1)**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing(2) | Port P1, P2, P3, P4: P1.x to P4.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

**Table 5-3. Output Frequency – Ports P1, P2, and P3**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | P3.4/TA2CLK/SMCLK/S27, $C_L$ = 20 pF, $R_L$ = 1 kΩ (1) or 3.2 kΩ(2) (3) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 8 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 20 | |
| $f_{Port\_CLK}$ | Clock output frequency | P1.0/TA0CLK/ACLK/S39, P3.4/TA2CLK/SMCLK/S27, P2.0/P2MAP0 (P2MAP0 = PM_MCLK), $C_L$ = 20 pF(3) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 8 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 20 | |

(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(3) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

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## Table 5-4. Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $T_J$ = 25°C | 3 V | | 0.075 | | µA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, $T_J$ = 25°C | | | 0.170 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_J$ = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1(2) (3) | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals(4) | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF, $T_J$ = 25°C | 3 V | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF, $T_J$ = 25°C | | | 300 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode(5) | XTS = 0, XCAPx = 0(6) | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 12.0 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode(7) | XTS = 0(8) | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $T_J$ = 25°C, $C_{L,eff}$ = 6 pF | 3 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_J$ = 25°C, $C_{L,eff}$ = 12 pF | | | 500 | | |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le 9$ pF.
- For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le 10$ pF.
- For XT1DRIVEx = 3, $C_{L,eff} \ge 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.


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## Table 5-5. Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1) (2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DVCC,XT2}$ | XT2 oscillator crystal current consumption | $f_{OSC}$ = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, $T_J$ = 25°C | 3 V | | 200 | | µA |
| | | $f_{OSC}$ = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, $T_J$ = 25°C | | | 260 | | |
| | | $f_{OSC}$ = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, $T_J$ = 25°C | | | 325 | | |
| | | $f_{OSC}$ = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, $T_J$ = 25°C | | | 450 | | |
| $f_{XT2,HF0}$ | XT2 oscillator crystal frequency, mode 0 | XT2DRIVEx = 0, XT2BYPASS = 0(3) | | 4 | | 8 | MHz |
| $f_{XT2,HF1}$ | XT2 oscillator crystal frequency, mode 1 | XT2DRIVEx = 1, XT2BYPASS = 0(3) | | 8 | | 16 | MHz |
| $f_{XT2,HF2}$ | XT2 oscillator crystal frequency, mode 2 | XT2DRIVEx = 2, XT2BYPASS = 0(3) | | 16 | | 24 | MHz |
| $f_{XT2,HF3}$ | XT2 oscillator crystal frequency, mode 3 | XT2DRIVEx = 3, XT2BYPASS = 0(3) | | 24 | | 32 | MHz |
| $f_{XT2,HF,SW}$ | XT2 oscillator logic-level square-wave input frequency | XT2BYPASS = 1(4) (3) | | 0.7 | | 32 | MHz |
| $OA_{HF}$ | Oscillation allowance for HF crystals(5) | XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF, $T_J$ = 25°C | 3 V | | 450 | | Ω |
| | | XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF, $T_J$ = 25°C | | | 320 | | |
| | | XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF, $T_J$ = 25°C | | | 200 | | |
| | | XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF, $T_J$ = 25°C | | | 200 | | |
| $t_{START,HF}$ | Start-up time | $f_{OSC}$ = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, $T_J$ = 25°C, $C_{L,eff}$ = 15 pF | 3 V | | 0.5 | | ms |
| | | $f_{OSC}$ = 20 MHz, XT2BYPASS = 0, XT2DRIVEx = 3, $T_J$ = 25°C, $C_{L,eff}$ = 15 pF | | | 0.3 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, HF mode(6) (1) | | | | 1 | | pF |
| | Duty cycle | Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz | | 40% | 50% | 60% | |
| $f_{Fault,HF}$ | Oscillator fault frequency(7) | XT2BYPASS = 1(8) | | 30 | | 300 | kHz |

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

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### Table 5-6. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

### Table 5-7. Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_J$ = 25°C | 1.8 V to 3.6 V | | 3 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | $T_J$ = 25°C | 3 V | | | ±1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | µs |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)


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**Table 5-8. DCO Frequency**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0)(1) | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31)(1) | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0)(1) | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31)(1) | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0)(1) | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31)(1) | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0)(1) | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31)(1) | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0)(1) | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31)(1) | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0)(1) | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31)(1) | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0)(1) | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31)(1) | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0)(1) | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31)(1) | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$ | 1.2 | | 2.3 | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$ | 1.02 | | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% | |
| $df_{DCO}/dT$ | DCO frequency temperature drift | $f_{DCO}$ = 1 MHz, | | 0.1 | | %/°C |
| $df_{DCO}/dV_{CC}$ | DCO frequency voltage drift | $f_{DCO}$ = 1 MHz | | 1.9 | | %/V |

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, $f_{DCO}$, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \le f_{DCO} \le f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual $f_{DCO}$ frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.


**Figure 5-10. Typical DCO Frequency**

**Table 5-9. Wake-Up Times From Low-Power Modes**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(1) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1, $f_{MCLK} \geq 4.0$ MHz | | 3 | 6.5 | µs |
| | | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1, 1 MHz < $f_{MCLK}$ < 4.0 MHz | | 4 | 8.0 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3 or LPM4 to active mode(2) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | |
| $t_{WAKE-UP\ LPM5}$ | Wake-up time from LPM3.5 or LPM4.5 to active mode(3) | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from RST or BOR event to active mode(3) | | | 2 | 3 | ms |

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). Fastest wake-up times are possible with $SVS_L$ and $SVM_L$ in full-performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for $SVS_L$ and $SVM_L$ while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). In this case, the $SVS_L$ and $SVM_L$ are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for $SVS_L$ and $SVM_L$ while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(3) This value represents the time from the wake-up event to the reset vector execution.

### 5.14.3 Peripherals

**Table 5-10. PMM, Core Voltage**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE3}$(AM) | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 21 mA | | 1.90 | | V |
| $V_{CORE2}$(AM) | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 21 mA | | 1.80 | | V |
| $V_{CORE1}$(AM) | Core voltage, active mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 17 mA | | 1.60 | | V |
| $V_{CORE0}$(AM) | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 13 mA | | 1.40 | | V |
| $V_{CORE3}$(LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.94 | | V |
| $V_{CORE2}$(LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.84 | | V |
| $V_{CORE1}$(LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.64 | | V |
| $V_{CORE0}$(LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.44 | | V |


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### Table 5-11. PMM, SVS High Side

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 1 | | 2.0 | | µA |
| $V_{(SVSH\_IT-)}$ | $SVS_H$ on voltage level(1) | SVSHE = 1, SVSHRVL = 0 | 1.59 | 1.64 | 1.69 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.84 | 1.91 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.04 | 2.11 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.16 | 2.23 | |
| $V_{(SVSH\_IT+)}$ | $SVS_H$ off voltage level(1) | SVSHE = 1, SVSMHRRL = 0 | 1.62 | 1.74 | 1.81 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.88 | 1.94 | 2.01 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.07 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.20 | 2.26 | 2.33 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVSH)}$ | $SVS_H$ propagation delay | SVSHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVSHFP = 1 | | 2.5 | | µs |
| | | SVSHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | $SVS_H$ on or off delay time | SVSHE = 0→1, SVSHFP = 1 | | 12.5 | | µs |
| | | SVSHE = 0→1, SVSHFP = 0 | | 100 | | |
| $dV_{DVCC}/dt$ | $DV_{CC}$ rise time | | 0 | | 1000 | V/s |

(1) The $SVS_H$ settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and usage.

### Table 5-12. PMM, SVM High Side

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVMH)}$ | $SVM_H$ current consumption | SVMHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 1 | | 2.0 | | µA |
| $V_{(SVMH)}$ | $SVM_H$ on or off voltage level(1) | SVMHE = 1, SVSMHRRL = 0 | 1.65 | 1.74 | 1.86 | V |
| | | SVMHE = 1, SVSMHRRL = 1 | 1.85 | 1.94 | 2.02 | |
| | | SVMHE = 1, SVSMHRRL = 2 | 2.02 | 2.14 | 2.22 | |
| | | SVMHE = 1, SVSMHRRL = 3 | 2.18 | 2.26 | 2.35 | |
| | | SVMHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVMHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVMHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.75 | | |
| $t_{pd(SVMH)}$ | $SVM_H$ propagation delay | SVMHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVMHFP = 1 | | 2.5 | | µs |
| | | SVMHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | $SVM_H$ on or off delay time | SVMHE = 0→1, SVSMFP = 1 | | 12.5 | | µs |
| | | SVMHE = 0→1, SVMHFP = 0 | | 100 | | |

(1) The $SVM_H$ settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and usage.

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### Table 5-13. PMM, SVS Low Side

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSL)}$ | $SVS_L$ current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 2.0 | | µA |
| $t_{pd(SVSL)}$ | $SVS_L$ propagation delay | SVSLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVSLFP = 1 | | 2.5 | | µs |
| | | SVSLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | $SVS_L$ on or off delay time | SVSLE = 0→1, SVSLFP = 1 | | 12.5 | | µs |
| | | SVSLE = 0→1, SVSLFP = 0 | | 100 | | |

### Table 5-14. PMM, SVM Low Side

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVML)}$ | $SVM_L$ current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 2.0 | | µA |
| $t_{pd(SVML)}$ | $SVM_L$ propagation delay | SVMLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVMLFP = 1 | | 2.5 | | µs |
| | | SVMLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | $SVM_L$ on or off delay time | SVMLE = 0→1, SVMLFP = 1 | | 12.5 | | µs |
| | | SVMLE = 0→1, SVMLFP = 0 | | 100 | | |


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### Table 5-15. Timer_A – Timers TA0, TA1, and TA2

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

### Table 5-16. Timer_B – Timer TB0

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK, ACLK<br>External: TBCLK<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

### Table 5-17. Battery Backup

over operating junction temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{VBAT}$ | Current into VBAT terminal if no primary battery is connected | VBAT = 1.7 V, DVCC not connected, RTC running | $T_J$ = –40°C | | | 0.43 | | µA |
| | | | $T_J$ = 25°C | | | 0.52 | | |
| | | | $T_J$ = 60°C | | | 0.58 | | |
| | | | $T_J$ = 105°C | | | 0.66 | | |
| | | VBAT = 2.2 V, DVCC not connected, RTC running | $T_J$ = –40°C | | | 0.50 | | |
| | | | $T_J$ = 25°C | | | 0.59 | | |
| | | | $T_J$ = 60°C | | | 0.64 | | |
| | | | $T_J$ = 105°C | | | 0.72 | | |
| | | VBAT = 3 V, DVCC not connected, RTC running | $T_J$ = –40°C | | | 0.68 | | |
| | | | $T_J$ = 25°C | | | 0.75 | | |
| | | | $T_J$ = 60°C | | | 0.79 | | |
| | | | $T_J$ = 105°C | | | 0.87 | | |
| $V_{SWITCH}$ | Switch-over level ($V_{CC}$ to VBAT) | $C_{VCC}$ = 4.7 µF | General | | | $V_{SVSH\_IT-}$ | | V |
| | | | SVSHRL = 0 | | 1.59 | | 1.69 | |
| | | | SVSHRL = 1 | | 1.79 | | 1.91 | |
| | | | SVSHRL = 2 | | 1.98 | | 2.11 | |
| | | | SVSHRL = 3 | | 2.10 | | 2.23 | |
| $R_{ON\_VBAT}$ | On-resistance of switch between VBAT and VBAK | $V_{BAT}$ = 1.8 V | | 0 V | | 0.35 | 1 | kΩ |
| $V_{BAT3}$ | VBAT to ADC input channel 12: $V_{BAT}$ divided, $V_{BAT3} \approx V_{BAT}/3$ | | | 1.8 V | | 0.6 | ±5% | V |
| | | | | 3 V | | 1.0 | ±5% | |
| | | | | 3.6 V | | 1.2 | ±5% | |
| $t_{Sample,\ VBAT3}$ | VBAT to ADC: Sampling time required if VBAT3 selected | ADC12ON = 1,<br>Error of conversion result ≤ 2 LSB | | | 1000 | | | ns |
| $V_{CHVx}$ | Charger end voltage | CHVx = 2 | | | 2.65 | 2.7 | 2.9 | V |
| $R_{CHARGE}$ | Charge limiting resistor | CHCx = 1 | | | | | 5.2 | kΩ |
| | | CHCx = 2 | | | | | 10.2 | |
| | | CHCx = 3 | | | | | 20 | |

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### Table 5-18. USCI (UART Mode)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | | | 1 | MHz |
| $t_\tau$ | UART receive deglitch time(1) | | 2.2 V | 50 | | 600 | ns |
| | | | 3 V | 50 | | 600 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

### Table 5-19. USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)
(see Figure 5-11 and )

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | SMCLK or ACLK,<br>Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $t_{SU,MI}$ | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 55 | | | ns |
| | | | 3 V | 38 | | | |
| | | PMMCOREV = 3 | 2.4 V | 30 | | | |
| | | | 3 V | 25 | | | |
| $t_{HD,MI}$ | SOMI input data hold time | PMMCOREV = 0 | 1.8 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| | | PMMCOREV = 3 | 2.4 V | 0 | | | |
| | | | 3 V | 0 | | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | | | 20 | ns |
| | | | 3 V | | | 18 | |
| | | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | | | 16 | |
| | | | 3 V | | | 15 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | –10 | | | ns |
| | | | 3 V | –8 | | | |
| | | $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | –10 | | | |
| | | | 3 V | –8 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-11 and Figure 5-12.


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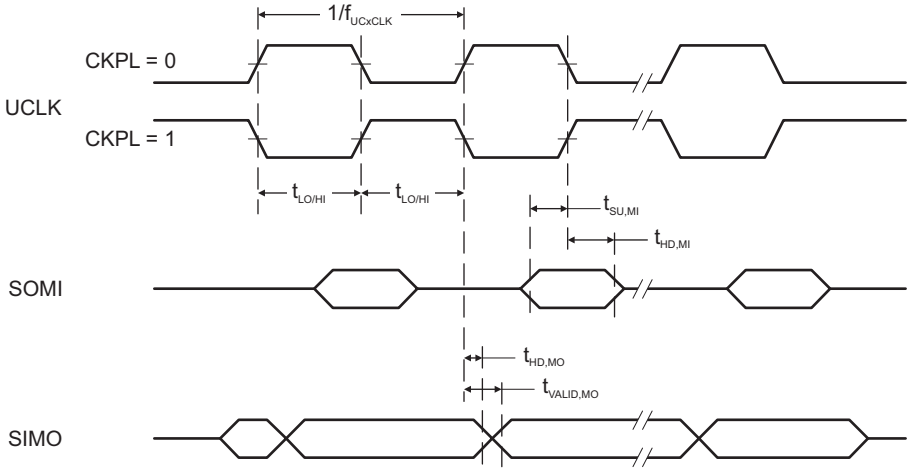


**Figure 5-11. SPI Master Mode, CKPH = 0**

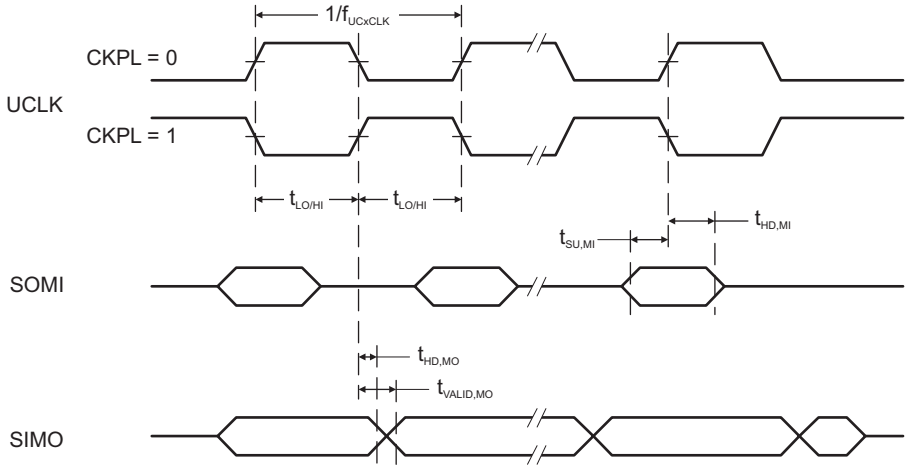


**Figure 5-12. SPI Master Mode, CKPH = 1**

**Table 5-20. USCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)
(see Figure 5-13 and Figure 5-14)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 11 | | | ns |
| | | | 3 V | 8 | | | |
| | | PMMCOREV = 3 | 2.4 V | 7 | | | |
| | | | 3 V | 6 | | | |
| $t_{STE,LAG}$ | STE lag time, last clock to STE high | PMMCOREV = 0 | 1.8 V | 1 | | | ns |
| | | | 3 V | 1 | | | |
| | | PMMCOREV = 3 | 2.4 V | 1 | | | |
| | | | 3 V | 1 | | | |
| $t_{STE,ACC}$ | STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | | | 66 | ns |
| | | | 3 V | | | 50 | |
| | | PMMCOREV = 3 | 2.4 V | | | 36 | |
| | | | 3 V | | | 30 | |
| $t_{STE,DIS}$ | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| | | PMMCOREV = 3 | 2.4 V | | | 30 | |
| | | | 3 V | | | 30 | |
| $t_{SU,SI}$ | SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| | | PMMCOREV = 3 | 2.4 V | 2 | | | |
| | | | 3 V | 2 | | | |
| $t_{HD,SI}$ | SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| | | PMMCOREV = 3 | 2.4 V | 5 | | | |
| | | | 3 V | 5 | | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | | | 76 | ns |
| | | | 3 V | | | 60 | |
| | | UCLK edge to SOMI valid, $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | | | 44 | |
| | | | 3 V | | | 40 | |
| $t_{HD,SO}$ | SOMI output data hold time(3) | $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | 12 | | | ns |
| | | | 3 V | 12 | | | |
| | | $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | 12 | | | |
| | | | 3 V | 12 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.


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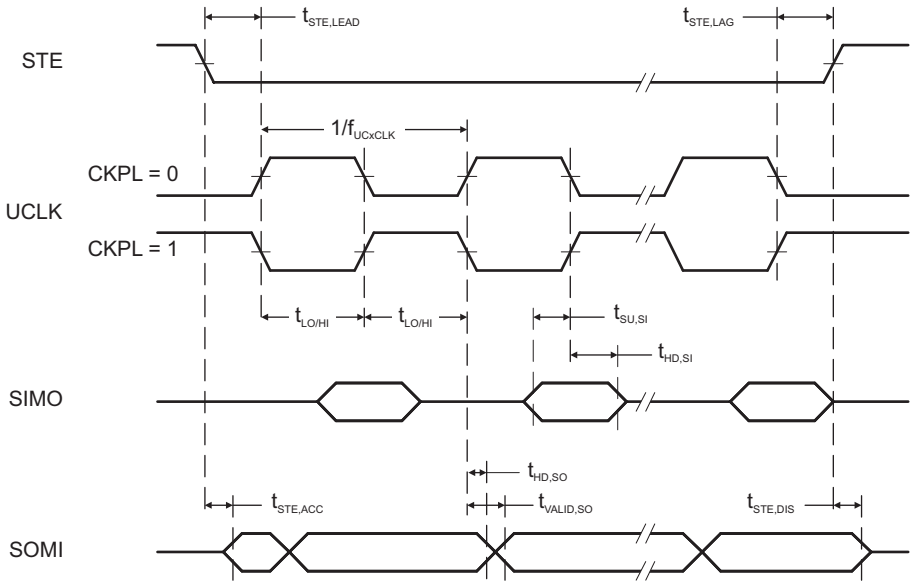


**Figure 5-13. SPI Slave Mode, CKPH = 0**

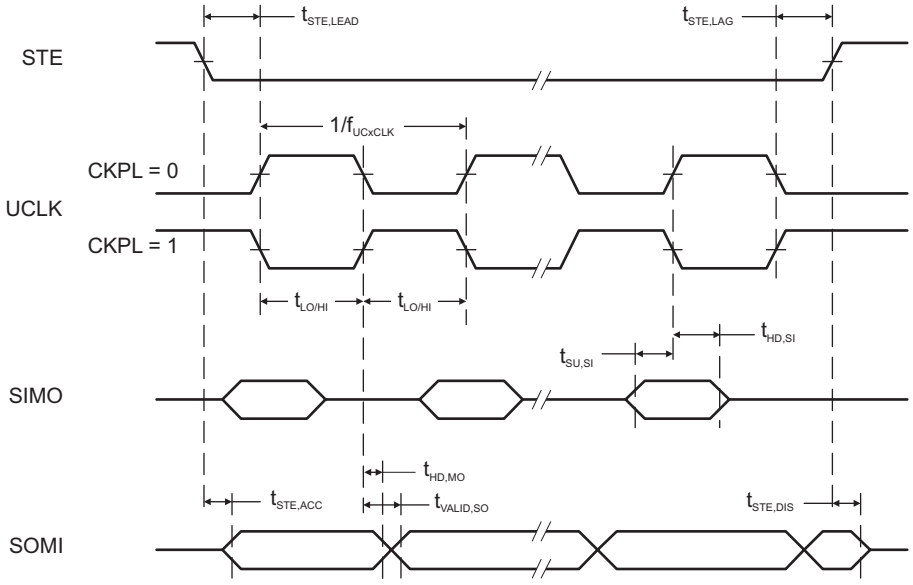


**Figure 5-14. SPI Slave Mode, CKPH = 1**

**Table 5-21. USCI ($I^2C$ Mode)**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted) (see Figure 5-15)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2.2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL} \le 100$ kHz | 2.2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL} > 100$ kHz | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL} \le 100$ kHz | 2.2 V, 3 V | 4.7 | | | µs |
| | | $f_{SCL} > 100$ kHz | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2.2 V, 3 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2.2 V, 3 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL} \le 100$ kHz | 2.2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL} > 100$ kHz | | 0.6 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | | 2.2 V | 50 | | 600 | ns |
| | | | 3 V | 50 | | 600 | |

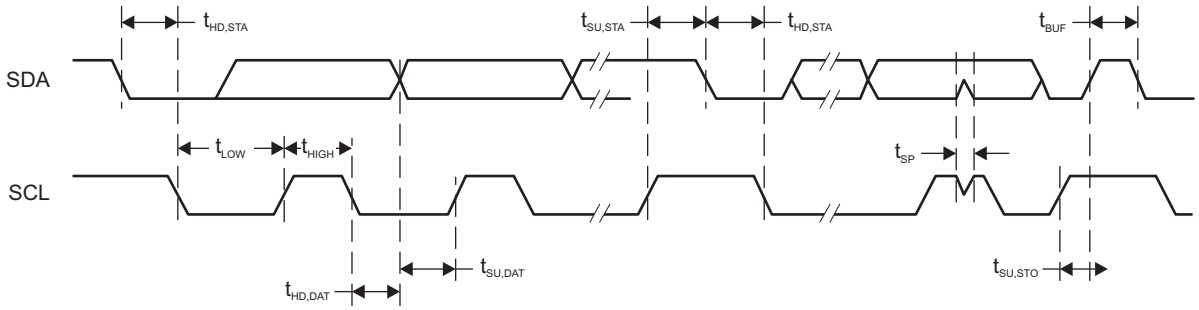


**Figure 5-15. $I^2C$ Mode Timing**


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**Table 5-22. LCD_B Operating Characteristics**

over operating junction temperature range (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC,LCD\_B,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, $V_{LCD} \le 3.6$ V) | 2.2 | | 3.6 | V |
| $V_{CC,LCD\_B,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.3$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, $V_{LCD} \le 3.3$ V) | 2.0 | | 3.6 | V |
| $V_{CC,LCD\_B,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD\_B,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD\_B,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.0 | | 3.6 | V |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | 3.6 | V |
| $C_{LCDCAP}$ | Capacitor on LCDCAP when charge pump enabled | LCDCPEN = 1, VLCDx > 0000 (charge pump enabled) | | 4.7 | 10 | µF |
| $f_{Frame}$ | LCD frame frequency range | $f_{LCD} = 2 \times mux \times f_{FRAME}$ with mux = 1 (static), 2, 3, 4 | 0 | | 100 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32 | 40 | kHz |
| $C_{Panel}$ | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF |
| $V_{R33}$ | Analog input voltage at R33 | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R13}$ | $V_{R03}$ + 2/3 × ($V_{R33}$ – $V_{R03}$) | $V_{R33}$ | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R03}$ | $V_{R03}$ + 1/3 × ($V_{R33}$ – $V_{R03}$) | $V_{R23}$ | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | $V_{R03}$ | $V_{R03}$ + 1/2 × ($V_{R33}$ – $V_{R03}$) | $V_{R33}$ | V |
| $V_{R03}$ | Analog input voltage at R03 | R0EXT = 1 | $V_{SS}$ | | | V |
| $V_{LCD}$-$V_{R03}$ | Voltage difference between $V_{LCD}$ and R03 | LCDCPEN = 0, R0EXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDREFx = 01 | 0.8 | 1.2 | 1.5 | V |

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### Table 5-23. LCD_B Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{LCD}$ | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | | $V_{CC}$ | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | | 2.59 | | |
| | | LCDCPEN = 1, VLCDx = 0010 | 2 V to 3.6 V | | 2.66 | | |
| | | LCDCPEN = 1, VLCDx = 0011 | 2 V to 3.6 V | | 2.72 | | |
| | | LCDCPEN = 1, VLCDx = 0100 | 2 V to 3.6 V | | 2.79 | | |
| | | LCDCPEN = 1, VLCDx = 0101 | 2 V to 3.6 V | | 2.85 | | |
| | | LCDCPEN = 1, VLCDx = 0110 | 2 V to 3.6 V | | 2.92 | | |
| | | LCDCPEN = 1, VLCDx = 0111 | 2 V to 3.6 V | | 2.98 | | |
| | | LCDCPEN = 1, VLCDx = 1000 | 2 V to 3.6 V | | 3.05 | | |
| | | LCDCPEN = 1, VLCDx = 1001 | 2 V to 3.6 V | | 3.10 | | |
| | | LCDCPEN = 1, VLCDx = 1010 | 2 V to 3.6 V | | 3.17 | | |
| | | LCDCPEN = 1, VLCDx = 1011 | 2 V to 3.6 V | | 3.24 | | |
| | | LCDCPEN = 1, VLCDx = 1100 | 2 V to 3.6 V | | 3.30 | | |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | | 3.36 | | |
| | | LCDCPEN = 1, VLCDx = 1110 | 2.2 V to 3.6 V | | 3.42 | | |
| | | LCDCPEN = 1, VLCDx = 1111 | 2.2 V to 3.6 V | | 3.48 | 3.6 | |
| $I_{CC,Peak,CP}$ | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | | 400 | | µA |
| $t_{LCD,CP,on}$ | Time to charge $C_{LCD}$ when discharged | $C_{LCD}$ = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 100 | 500 | ms |
| $I_{CP,Load}$ | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | µA |
| $R_{LCD,Seg}$ | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |
| $R_{LCD,COM}$ | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |

### Table 5-24. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V | | 2.2 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range(2) | All ADC12 analog input pins Ax | | 0 | | $AV_{CC}$ | V |
| $I_{ADC12\_A}$ | Operating supply current into AVCC terminal(3) | $f_{ADC12CLK}$ = 5.0 MHz(4) | 2.2 V | | 150 | 200 | µA |
| | | | 3 V | | 150 | 250 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time | 2.2 V | | 20 | 25 | pF |
| $R_I$ | Input MUX ON resistance | 0 V ≤ VIN ≤ V(AVCC) | | 10 | 200 | 1900 | Ω |

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results. If the reference voltage is supplied by an external source or if the internal voltage is used and REFOUT = 1, then decoupling capacitors are required. See Table 5-30 and Table 5-31.
(3) The internal reference supply current is not included in current consumption parameter $I_{ADC12}$.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0


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### Table 5-25. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC12CLK}$ | ADC conversion clock | For specified performance of ADC12 linearity parameters using an external reference voltage or $AV_{CC}$ as reference (1) | 2.2 V, 3 V | 0.45 | 4.8 | 5.0 | MHz |
| | | For specified performance of ADC12 linearity parameters using the internal reference (2) | | 0.45 | 2.4 | 4.0 | |
| | | For specified performance of ADC12 linearity parameters using the internal reference (3) | | 0.45 | 2.4 | 2.7 | |
| $f_{ADC12OSC}$ | Internal ADC12 oscillator (4) | ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock | 2.2 V, 3 V | 2.4 | | 3.1 | µs |
| | | External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0 | | | See (5) | | |
| $t_{Sample}$ | Sampling time | $R_S$ = 400 Ω, $R_I$ = 200 Ω, $C_I$ = 20 pF, $\tau = [R_S + R_I] \times C_I$ (6) | 2.2 V, 3 V | 1000 | | | ns |

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. $AV_{CC}$ as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) 13 × ADC12DIV × $1/f_{ADC12CLK}$
(6) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, $R_S$ = external source resistance

### Table 5-26. 12-Bit ADC, Linearity Parameters Using an External Reference Voltage

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error (1) | 1.4 V ≤ dVREF ≤ 1.6 V (2) | 2.2 V, 3 V | | | ±2 | LSB |
| | | 1.6 V < dVREF (2) | | | | ±1.7 | |
| $E_D$ | Differential linearity error (1) | See (2) | 2.2 V, 3 V | | | ±1 | LSB |
| $E_O$ | Offset error (3) | dVREF ≤ 2.2 V (2) | 2.2 V, 3 V | | ±3 | ±5.6 | LSB |
| | | dVREF > 2.2 V (2) | 2.2 V, 3 V | | ±1.5 | ±3.5 | |
| $E_G$ | Gain error (3) | See (2) | 2.2 V, 3 V | | ±1 | ±2.5 | LSB |
| $E_T$ | Total unadjusted error | dVREF ≤ 2.2 V (2) | 2.2 V, 3 V | | ±3.5 | ±7.1 | LSB |
| | | dVREF > 2.2 V (2) | 2.2 V, 3 V | | ±2 | ±5 | |

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = $V_{R+} - V_{R-}$. $V_{R+}$ < AVCC. $V_{R-}$ > AVSS. Unless otherwise mentioned dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the *MSP430F5xx and MSP430F6xx Family User's Guide* (SLAU208).
(3) Parameters are derived using a best fit curve.

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### Table 5-27. 12-Bit ADC, Linearity Parameters Using $AV_{CC}$ as Reference Voltage

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error (1) | See (2) | 2.2 V, 3 V | | | ±2.0 | LSB |
| $E_D$ | Differential linearity error (1) | See (2) | 2.2 V, 3 V | | | ±1 | LSB |
| $E_O$ | Offset error (3) | See (2) | 2.2 V, 3 V | | ±1 | ±2 | LSB |
| $E_G$ | Gain error (3) | See (2) | 2.2 V, 3 V | | ±2 | ±4 | LSB |
| $E_T$ | Total unadjusted error | See (2) | 2.2 V, 3 V | | ±2 | ±5 | LSB |

(1) Parameters are derived using the histogram method.
(2) $AV_{CC}$ as reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 0.
(3) Parameters are derived using a best fit curve.

### Table 5-28. 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS (1) | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error (2) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 4.0$ MHz | 2.2 V, 3 V | | | ±2.0 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK} \le 2.7$ MHz | | | | ±2.5 | |
| $E_D$ | Differential linearity error (2) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 4.0$ MHz | 2.2 V, 3 V | –1 | | +1.5 | LSB |
| | | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 2.7$ MHz | | | | ±1 | |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK} \le 2.7$ MHz | | –1 | | +2.5 | |
| $E_O$ | Offset error (3) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 4.0$ MHz | 2.2 V, 3 V | | ±2 | ±4 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK} \le 2.7$ MHz | | | ±2 | ±4 | |
| $E_G$ | Gain error (3) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 4.0$ MHz | 2.2 V, 3 V | | ±1 | ±2.5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK} \le 2.7$ MHz | | | | ±1% (4) | VREF |
| $E_T$ | Total unadjusted error | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK} \le 4.0$ MHz | 2.2 V, 3 V | | ±2 | ±5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK} \le 2.7$ MHz | | | | ±1% (4) | VREF |

(1) The external reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 1. dVREF = $V_{R+} - V_{R-}$.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and the total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode, the reference voltage used by the ADC12_A is not available on a pin.

### Table 5-29. 12-Bit ADC, Temperature Sensor and Built-In $V_{MID}$ (1)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | See Figure 5-16 (2) | ADC12ON = 1, INCH = 0Ah, $T_J$ = 0°C | 2.2 V | | 680 | | mV |
| | | | 3 V | | 680 | | |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected (3) | ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V | 30 | | | µs |
| | | | 3 V | 30 | | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$ | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (4) | ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V, 3 V | 1000 | | | ns |

(1) The temperature sensor is provided by the REF module. See the REF module parametric, $I_{REF+}$, regarding the current consumption of the temperature sensor.
(2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ±3°C and 105°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times$ (Temperature,°C) + $V_{SENSOR}$, where $TC_{SENSOR}$ and $V_{SENSOR}$ can be computed from the calibration values for higher accuracy. See also the *MSP430F5xx and MSP430F6xx Family User's Guide* (SLAU208).
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.


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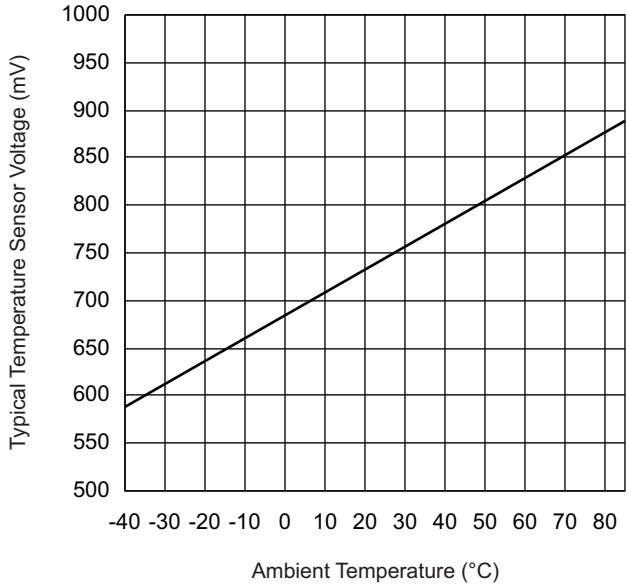


**Figure 5-16. Typical Temperature Sensor Voltage**

**Table 5-30. REF, External Reference**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (2) | | 1.4 | $AV_{CC}$ | V |
| $V_{REF-}/V_{eREF-}$ | Negative external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (3) | | 0 | 1.2 | V |
| ($V_{eREF+}$ – $V_{REF-}/V_{eREF-}$) | Differential external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (4) | | 1.4 | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VREF-/VeREF-}$ | Static input current | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksps | 2.2 V, 3 V | –32 | 32 | µA |
| | | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF-}$ = 0 V, $f_{ADC12CLK}$ = 5 MHZ, ADC12SHTx = 8h, Conversion rate 20 ksps | 2.2 V, 3 V | –1.2 | +1.2 | |
| $C_{VREF+/-}$ | Capacitance at VREF+ or VREF- terminal(5) | | | 10 | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_i$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

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## Table 5-31. REF, Built-In Reference

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, $I_{VREF+}$ = 0 A | | 3 V | | 2.5 | ±1% | V |
| | | REFVSEL = {1} for 2 V, REFON = REFOUT = 1, $I_{VREF+}$ = 0 A | | 3 V | | 2.0 | ±1% | |
| | | REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, $I_{VREF+}$ = 0 A | | 2.2 V, 3 V | | 1.5 | ±1% | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | | 2.2 | | | V |
| | | REFVSEL = {1} for 2 V | | | 2.3 | | | |
| | | REFVSEL = {2} for 2.5 V | | | 2.8 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal (2) (3) | ADC12SR = 1(4), REFON = 1, REFOUT = 0, REFBURST = 0 | | 3 V | | 70 | 100 | µA |
| | | ADC12SR = 1(4), REFON = 1, REFOUT = 1, REFBURST = 0 | | | | 0.45 | 0.75 | mA |
| | | ADC12SR = 0(4), REFON = 1, REFOUT = 0, REFBURST = 0 | | | | 210 | 310 | µA |
| | | ADC12SR = 0(4), REFON = 1, REFOUT = 1, REFBURST = 0 | | | | 0.95 | 1.7 | mA |
| $I_{L(VREF+)}$ | Load-current regulation, VREF+ terminal(5) | REFVSEL = {0, 1, 2}, $I_{VREF+}$ = +10 µA or –1000 µA, $AV_{CC}$ = $AV_{CC(min)}$ for each reference level, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1 | | | | 1500 | 2500 | µV/mA |
| $C_{VREF+}$ | Capacitance at VREF+ terminal | REFON = REFOUT = 1(6), 0 mA ≤ $I_{VREF+}$ ≤ $I_{VREF+}$(max) | | 2.2 V, 3 V | 20 | | 100 | pF |
| $TC_{REF+}$ | Temperature coefficient of built-in reference(7) | $I_{VREF+}$ is a constant in the range of 0 mA ≤ $I_{VREF+}$ ≤ –1 mA | REFOUT = 0 | 2.2 V, 3 V | | 20 | | ppm/°C |
| $TC_{REF+}$ | Temperature coefficient of built-in reference(7) | $I_{VREF+}$ is a constant in the range of 0 mA ≤ $I_{VREF+}$ ≤ –1 mA | REFOUT = 1 | 2.2 V, 3 V | | 20 | 50 | ppm/°C |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $T_J$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | | 120 | 300 | µV/V |
| PSRR_AC | Power supply rejection ratio (AC) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $T_J$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | | 1 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage(8) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFOUT = 0, REFON = 0 → 1 | | | | 75 | | µs |
| | | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $C_{VREF}$ = $C_{VREF}$(max), REFVSEL = {0, 1, 2}, REFOUT = 1, REFON = 0 → 1 | | | | 75 | | |

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal and is used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
(2) The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
(3) The temperature sensor is provided by the REF module. Its current is supplied from the AVCC terminal and is equivalent to $I_{REF+}$ with REFON = 1 and REFOUT = 0.
(4) For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.
(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace or other causes.
(6) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
(7) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C)/(105°C – (–40°C)).
(8) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.


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**Table 5-32. 12-Bit DAC, Supply Specifications**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V | | 2.20 | | 3.60 | V |
| $I_{DD}$ | Supply current, single DAC channel(1)(2) | DAC12AMPx = 2, DAC12IR = 0, DAC12IOG = 1<br>DAC12_xDAT = 0800h<br>$Ve_{REF+} = V_{REF+} = 1.5$ V | 3 V | | 65 | 110 | µA |
| | | DAC12AMPx = 2, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>$Ve_{REF+} = V_{REF+} = AV_{CC}$ | 2.2 V, 3 V | | 65 | 110 | |
| | | DAC12AMPx = 5, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>$Ve_{REF+} = V_{REF+} = AV_{CC}$ | | | 250 | 300 | |
| | | DAC12AMPx = 7, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>$Ve_{REF+} = V_{REF+} = AV_{CC}$ | | | 750 | 1000 | |
| PSRR | Power supply rejection ratio(3)(4) | DAC12_xDAT = 800h, $Ve_{REF+} = 1.5$ V,<br>$\Delta AV_{CC}$ = 100 mV | 2.2 V | | 70 | | dB |
| | | DAC12_xDAT = 800h, $Ve_{REF+} = 1.5$ V or 2.5 V,<br>$\Delta AV_{CC}$ = 100 mV | 3 V | | 70 | | |

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Table 5-35.
(3) PSRR = 20 log ($\Delta AV_{CC}$ / $\Delta V_{DAC12\_xOUT}$)
(4) The internal reference is not used.

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### Table 5-33. 12-Bit DAC, Linearity Specifications

See Figure 5-17, over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | Resolution | 12-bit monotonic | | | 12 | | | bits |
| INL | Integral nonlinearity(1) | $Ve_{REF+}$ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 2.2 V | | ±2 | ±4 | LSB |
| | | $Ve_{REF+}$ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 3 V | | ±2 | ±4 | |
| DNL | Differential nonlinearity(1) | $Ve_{REF+}$ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 2.2 V | | ±0.4 | ±1 | LSB |
| | | $Ve_{REF+}$ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 3 V | | ±0.4 | ±1 | |
| $E_O$ | Offset voltage | Without calibration(1) (2) | $Ve_{REF+}$ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±21 | mV |
| | | | $Ve_{REF+}$ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | ±21 | |
| | | With calibration(1) (2) | $Ve_{REF+}$ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±1.5 | |
| | | | $Ve_{REF+}$ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | ±1.5 | |
| $d_{E(O)}/d_T$ | Offset error temperature coefficient(1) | With calibration | | 2.2 V, 3 V | | ±10 | | µV/°C |
| $E_G$ | Gain error | $Ve_{REF+}$ = 1.5 V | | 2.2 V | | | ±2.5 | %FSR |
| | | $Ve_{REF+}$ = 2.5 V | | 3 V | | | ±2.5 | |
| $d_{E(G)}/d_T$ | Gain temperature coefficient(1) | | | 2.2 V, 3 V | | 10 | | ppm of FSR/°C |
| $t_{Offset\_Cal}$ | Time for offset calibration(3) | DAC12AMPx = 2 | | 2.2 V, 3 V | | | 165 | ms |
| | | DAC12AMPx = 3, 5 | | | | | 66 | |
| | | DAC12AMPx = 4, 6, 7 | | | | | 16.5 | |

(1) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first-order equation: y = a + bx. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (Ve_{REF+}/4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends configuring the DAC12 module before initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

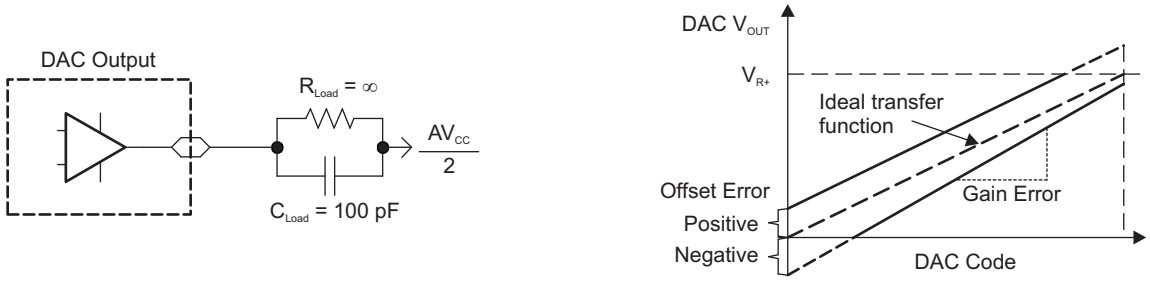


**Figure 5-17. Linearity Test Load Conditions and Gain/Offset Definition**


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**Table 5-34. 12-Bit DAC, Output Specifications**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage range(1) (see Figure 5-18) | No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2 V, 3 V | 0 | | 0.005 | V |
| | | No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | $AV_{CC}$ – 0.05 | | $AV_{CC}$ | |
| | | $R_{Load}$ = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | | 0 | | 0.1 | |
| | | $R_{Load}$ = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | $AV_{CC}$ – 0.13 | | $AV_{CC}$ | |
| $C_{L(DAC12)}$ | Maximum DAC12 load capacitance | | 2.2 V, 3 V | | | 100 | pF |
| $I_{L(DAC12)}$ | Maximum DAC12 load current | DAC12AMPx = 2, DAC12_xDAT = 0FFFh, $V_{O/P(DAC12)} > AV_{CC} – 0.3$ | 2.2 V, 3 V | –1 | | | mA |
| | | DAC12AMPx = 2, DAC12_xDAT = 0h, $V_{O/P(DAC12)} < 0.3$ V | | | | 1 | |
| $R_{O/P(DAC12)}$ | Output resistance (see Figure 5-18) | $R_{Load}$ = 3 kΩ, VO/P(DAC12) < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h | 2.2 V, 3 V | | 150 | 250 | Ω |
| | | $R_{Load}$ = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC} – 0.3$ V, DAC12_xDAT = 0FFFh | | | 150 | 250 | |
| | | $R_{Load}$ = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)} ≤ AV_{CC} – 0.3$ V | | | | 6 | |

(1) Data is valid after the offset calibration of the output amplifier.

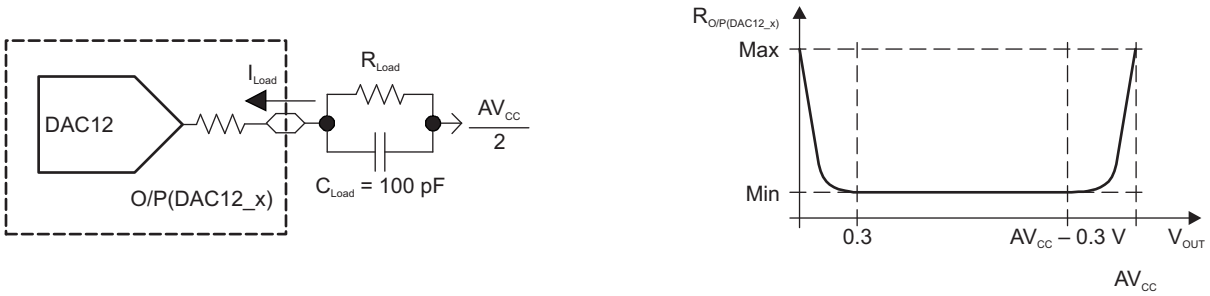


**Figure 5-18. DAC12_x Output Resistance Tests**

### Table 5-35. 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $Ve_{REF+}$ | Reference input voltage range | DAC12IR = 0 (1) (2) | 2.2 V, 3 V | | $AV_{CC}/3$ | $AV_{CC}$ + 0.2 | V |
| | | DAC12IR = 1 (3) (4) | | | $AV_{CC}$ | $AV_{CC}$ + 0.2 | |
| $Ri_{(VREF+)}$, $Ri_{(VeREF+)}$ | Reference input resistance | DAC12_0 IR = DAC12_1 IR = 0 | 2.2 V, 3 V | 20 | | | MΩ |
| | | DAC12_0 IR = 1, DAC12_1 IR = 0 | | | 52 | | kΩ |
| | | DAC12_0 IR = 0, DAC12_1 IR = 1 | | | 52 | | |
| | | DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx (5) | | | 26 | | |

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AVCC).
(2) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing ($AV_{CC}$).
(4) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

### Table 5-36. 12-Bit DAC, Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see Figure 5-19 and Figure 5-20), over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{ON}$ | DAC12 on time | DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (1) (see Figure 5-19) | DAC12AMPx = 0 → {2, 3, 4} | 2.2 V, 3 V | | 60 | 120 | µs |
| | | | DAC12AMPx = 0 → {5, 6} | | | 15 | 30 | |
| | | | DAC12AMPx = 0 → 7 | | | 6 | 12 | |
| $t_{S(FS)}$ | Settling time, full scale | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2 V, 3 V | | 100 | 200 | µs |
| | | | DAC12AMPx = 3, 5 | | | 40 | 80 | |
| | | | DAC12AMPx = 4, 6, 7 | | | 15 | 30 | |
| $t_{S(C-C)}$ | Settling time, code to code | DAC12_xDAT = 3F8h → 408h → 3F8h, BF8h → C08h → BF8h | DAC12AMPx = 2 | 2.2 V, 3 V | | 5 | | µs |
| | | | DAC12AMPx = 3, 5 | | | 2 | | |
| | | | DAC12AMPx = 4, 6, 7 | | | 1 | | |
| SR | Slew rate | DAC12_xDAT = 80h → F7Fh → 80h (2) | DAC12AMPx = 2 | 2.2 V, 3 V | 0.05 | 0.35 | | V/µs |
| | | | DAC12AMPx = 3, 5 | | 0.35 | 1.10 | | |
| | | | DAC12AMPx = 4, 6, 7 | | 1.50 | 5.20 | | |
| | Glitch energy | DAC12_xDAT = 800h → 7FFh → 800h | DAC12AMPx = 7 | 2.2 V, 3 V | | 35 | | nV-s |

(1) $R_{Load}$ and $C_{Load}$ connected to $AV_{SS}$ (not $AV_{CC}/2$) in Figure 5-19.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

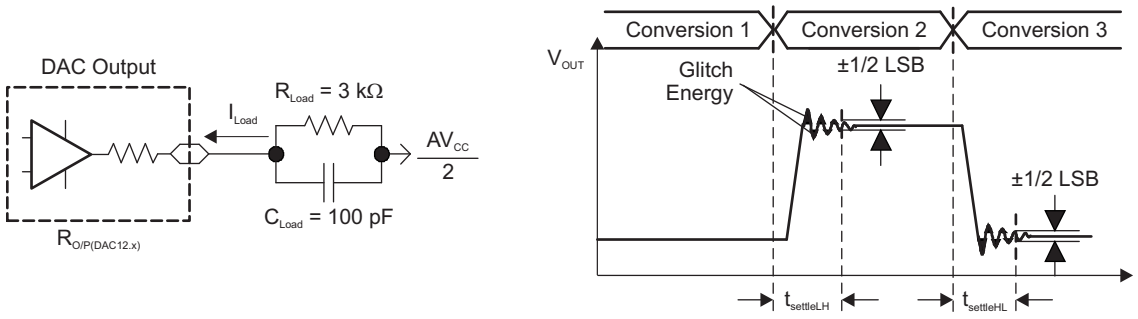


**Figure 5-19. Settling Time and Glitch Energy Testing**


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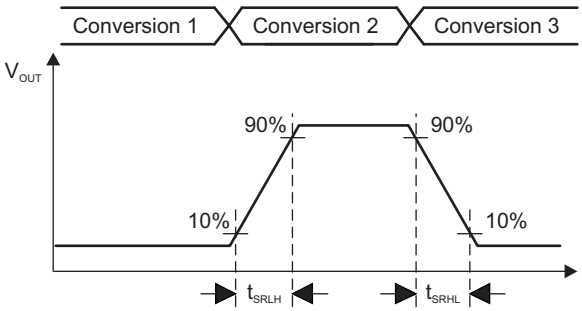


**Figure 5-20. Slew Rate Testing**

**Table 5-37. 12-Bit DAC, Dynamic Specifications (Continued)**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $BW_{-3dB}$ | 3-dB bandwidth, $V_{DC}$ = 1.5 V, $V_{AC}$ = 0.1 $V_{PP}$ (see Figure 5-21) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, $T_J$ = 25°C | 2.2 V, 3 V | 40 | | | kHz |
| | | DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, $T_J$ = 25°C | | 180 | | | |
| | | DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, $T_J$ = 25°C | | 550 | | | |
| | Channel-to-channel crosstalk(1) (see Figure 5-22) | DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, $R_{Load}$ = 3 kΩ, $f_{DAC12\_1OUT}$ = 10 kHz at 50/50 duty cycle, $T_J$ = 25°C | 2.2 V, 3 V | | –80 | | dB |
| | | DAC12_0DAT = 80h ↔ F7Fh, $R_{Load}$ = 3 kΩ, DAC12_1DAT = 800h, No load, $f_{DAC12\_0OUT}$ = 10 kHz at 50/50 duty cycle, $T_J$ = 25°C | | | –80 | | |

(1) $R_{Load}$ = 3 kΩ, $C_{Load}$ = 100 pF

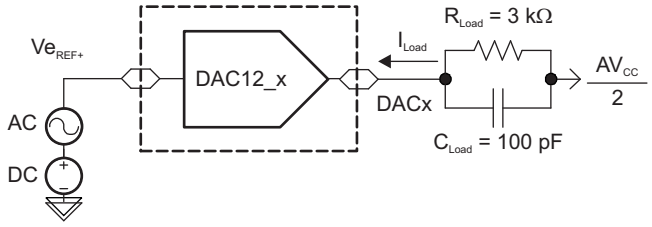


**Figure 5-21. Test Conditions for 3-dB Bandwidth Specification**

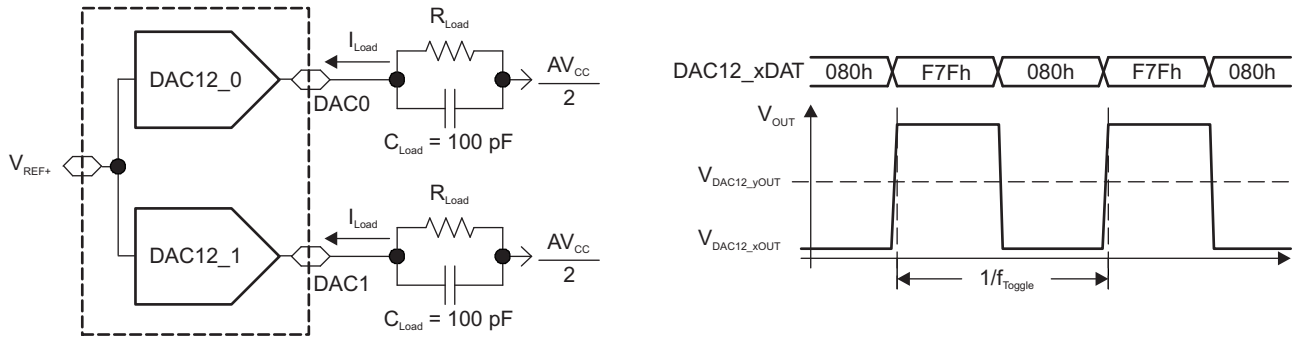


**Figure 5-22. Crosstalk Test Conditions**

**Table 5-38. Comparator_B**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 1.8 | | 3.6 | V |
| $I_{AVCC\_COMP}$ | Comparator operating supply current into AVCC terminal, Excludes reference resistor ladder | CBPWRMD = 00 | 1.8 V | | | 40 | µA |
| | | | 2.2 V | | 30 | 50 | |
| | | | 3 V | | 40 | 65 | |
| | | CBPWRMD = 01 | 2.2 V, 3 V | | 10 | 30 | |
| | | CBPWRMD = 10 | 2.2 V, 3 V | | 0.1 | 0.5 | |
| $I_{AVCC\_REF}$ | Quiescent current of local reference voltage amplifier into AVCC terminal | CBREFACC = 1, CBREFLx = 01 | | | | 22 | µA |
| $V_{IC}$ | Common mode input range | | | 0 | | $V_{CC}$ – 1 | V |
| $V_{OFFSET}$ | Input offset voltage | CBPWRMD = 00 | | | | ±20 | mV |
| | | CBPWRMD = 01, 10 | | | | ±10 | |
| $C_{IN}$ | Input capacitance | | | | 5 | | pF |
| $R_{SIN}$ | Series input resistance | ON, switch closed | | | 3 | 4 | kΩ |
| | | OFF, switch opened | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | | 450 | ns |
| | | CBPWRMD = 01, CBF = 0 | | | | 600 | |
| | | CBPWRMD = 10, CBF = 0 | | | | 50 | µs |
| $t_{PD,filter}$ | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00 | | 0.35 | 0.6 | 1.0 | µs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01 | | 0.6 | 1.0 | 1.8 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10 | | 1.0 | 1.8 | 3.4 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11 | | 1.8 | 3.4 | 6.5 | |
| $t_{EN\_CMP}$ | Comparator enable time, settling time | CBON = 0 to CBON = 1 CBPWRMD = 00, 01, 10 | | | 1 | 2 | µs |
| $t_{EN\_REF}$ | Resistor reference enable time | CBON = 0 to CBON = 1 | | | 0.3 | 1.5 | µs |
| $V_{CB\_REF}$ | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V |


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**Table 5-39. Flash Memory**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| $I_{PGM}$ | Average supply current from DVCC during program | | | 3 | 5 | mA |
| $I_{ERASE}$ | Average supply current from DVCC during erase | | | 6 | 17 | mA |
| $I_{MERASE}$, $I_{BANK}$ | Average supply current from DVCC during mass erase or bank erase | | | 6 | 17 | mA |
| $t_{CPT}$ | Cumulative program time | See (1) | | | 16 | ms |
| | Program and erase endurance | | $10^3$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | 100 | | | years |
| $t_{Word}$ | Word or byte program time | See (2) | 64 | | 85 | µs |
| $t_{Block, 0}$ | Block program time for first byte or word | See (2) | 49 | | 65 | µs |
| $t_{Block, 1–(N–1)}$ | Block program time for each additional byte or word, except for last byte or word | See (2) | 37 | | 49 | µs |
| $t_{Block, N}$ | Block program time for last byte or word | See (2) | 55 | | 73 | µs |
| $t_{Seg\ Erase}$ | Erase time for segment, mass erase, and bank erase when available | See (2) | 23 | | 32 | ms |
| $f_{MCLK,MRG}$ | MCLK frequency in marginal read mode (FCTL4.MRG0 = 1 or FCTL4.MRG1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word write, individual byte write, and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

### 5.14.4 Emulation and Debug

**Table 5-40. JTAG and Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW, En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | 2.2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency for 4-wire JTAG (2) | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

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# 6 Detailed Description

## 6.1 Overview

The MSP430F6459 is an ultra-low-power microcontroller that consists of several features which include different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications.

The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3 μs (typical).

## 6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

For further details, see the *CPUX Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU391).

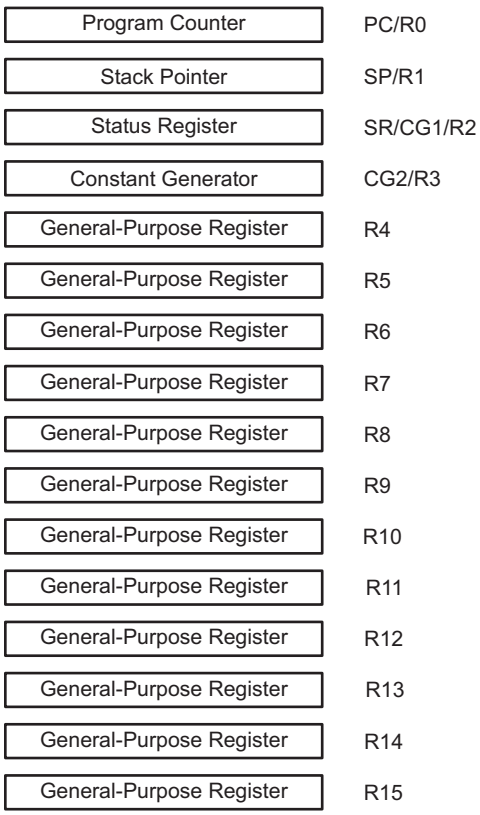


**Figure 6-1. CPU Registers**


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## 6.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 shows examples of the three types of instruction formats; Table 6-2 shows the address modes.

**Table 6-1. Instruction Word Formats**

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, unconditional or conditional | JNE | Jump-on-equal bit = 0 |

**Table 6-2. Address Mode Descriptions**

| ADDRESS MODE | S(1) | D(1) | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV &MEM, &TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect auto-increment | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

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## 6.4 Operating Modes

The MCUs have one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No data retention
  - RTC enabled and clocked by low-frequency oscillator
  - Wake-up signal from $\overline{\text{RST}}$/NMI, RTC_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up signal from $\overline{\text{RST}}$/NMI, P1, P2, P3, and P4


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## 6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-3. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power-Up, External Reset<br>Watchdog Time-out, Key Violation<br>Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV)(1) (2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>PMM<br>Vacant Memory Access<br>JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, SVMLVLRIFG, SVMHVLRIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>NMI<br>Oscillator Fault<br>Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1) (2) | (Non)maskable | 0FFFAh | 61 |
| Comp_B | Comparator B interrupt flags (CBIV)(1) (3) | Maskable | 0FFF8h | 60 |
| Timer TB0 | TB0CCR0 CCIFG0 (3) | Maskable | 0FFF6h | 59 |
| Timer TB0 | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV)(1) (3) | Maskable | 0FFF4h | 58 |
| Watchdog Interval Timer Mode | WDTIFG | Maskable | 0FFF2h | 57 |
| USCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (3) | Maskable | 0FFF0h | 56 |
| USCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (3) | Maskable | 0FFEEh | 55 |
| ADC12_A | ADC12IFG0 to ADC12IFG15 (ADC12IV)(1) (3) | Maskable | 0FFECh | 54 |
| Timer TA0 | TA0CCR0 CCIFG0(3) | Maskable | 0FFEAh | 53 |
| Timer TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (3) | Maskable | 0FFE8h | 52 |
| LDO-PWR (4) | LDOOFFIG, LDOONIFG, LDOOVLIFG | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG, DMA4IFG, DMA5IFG (DMAIV)(1) (3) | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0(3) | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (3) | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1)(3) | Maskable | 0FFDEh | 47 |
| USCI_A1 Receive or Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (3) | Maskable | 0FFDCh | 46 |
| USCI_B1 Receive or Transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (3) | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV)(1) (3) | Maskable | 0FFD8h | 44 |
| LCD_B(5) | LCD_B Interrupt Flags (LCDBIV)(1) | Maskable | 0FFD6h | 43 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1) (3) | Maskable | 0FFD4h | 42 |
| DAC12_A | DAC12_0IFG, DAC12_1IFG(1) (3) | Maskable | 0FFD2h | 41 |
| Timer TA2 | TA2CCR0 CCIFG0(3) | Maskable | 0FFD0h | 40 |
| Timer TA2 | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1) (3) | Maskable | 0FFCEh | 39 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV)(1) (3) | Maskable | 0FFCCh | 38 |
| I/O Port P4 | P4IFG.0 to P4IFG.7 (P4IV)(1) (3) | Maskable | 0FFCAh | 37 |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are in the module.
(4) Only on devices with peripheral module LDO-PWR.
(5) Only on devices with peripheral module LCD_B, otherwise reserved.

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**Table 6-3. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| USCI_A2 Receive or Transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV)(1) (3) | | 0FFC8h | 36 |
| USCI_B2 Receive or Transmit | UCB2RXIFG, UCB2TXIFG (UCB2IV)(1) (3) | | 0FFC6h | 35 |
| Reserved | Reserved(6) | | 0FFC4h | 34 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(6) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.


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## 6.6 Memory Organization

Table 6-4 summarizes the memory map.

**Table 6-4. Memory Organization(1)**

| | | DESCRIPTION |
|---|---|---|
| Memory (flash) | Total Size | 512KB |
| Main: interrupt vector | | 00FFFFh–00FF80h |
| Main: code memory | Bank 3 | 128KB<br>087FFFh-068000h |
| | Bank 2 | 128KB<br>067FFFh-48000h |
| | Bank 1 | 128KB<br>047FFFh-028000h |
| | Bank 0 | 128KB<br>027FFFh-008000h |
| MID support software (ROM) | Total Size | 1KB<br>006FFFh-006C00h |
| RAM | Sector 3 | 16KB<br>0FBFFFh-0F8000h |
| | Sector 2 | 16KB<br>0F7FFFh-0F4000h |
| | Sector 1 | 16KB<br>0F3FFFh-0F0000h |
| | Sector 0 | 16KB<br>0063FFh–002400h<br>(mirrored at address range<br>0FFFFFh-0FC000h) |
| RAM | Sector 7 | 2KB<br>0023FFh-001C00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh–001980h |
| | Info B | 128 B<br>00197Fh–001900h |
| | Info C | 128 B<br>0018FFh–001880h |
| | Info D | 128 B<br>00187Fh–001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh–001600h |
| | BSL 2 | 512 B<br>0015FFh–001400h |
| | BSL 1 | 512 B<br>0013FFh–001200h |
| | BSL 0 | 512 B<br>0011FFh–001000h |
| Peripherals | Size | 4KB<br>000FFFh–000000h |

(1) N/A = Not available

## 6.7 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory by the BSL is protected by an user-defined password. For complete description of the features of the BSL and its implementation, see *MSP430 Programming WIth the Bootloader (BSL)* (SLAU319).

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### 6.7.1 UART BSL

MSP4306459 comes preprogrammed with the UART BSL. Use of the UART BSL requires external access to six pins (see Table 6-5).

**Table 6-5. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.1 | Data transmit |
| P1.2 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |


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## 6.8 JTAG Operation

### 6.8.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the BSL and its implementation, see the *MSP430 Programming With the Bootloader User's Guide* (SLAU319).

**Table 6-6. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

### 6.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

**Table 6-7. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |

## 6.9 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

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For further information, see the *Flash Controller Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU392).

## 6.10 Memory Integrity Detection (MID)

The MID is an add-on to the MSP430 flash memory controller. MID provides additional functionality over the regular flash operation methods. Main purpose of the MID function is gaining higher reliability of flash content and overall system integrity in harsh environments and application areas requiring such features. The on-chip MID ROM contains the factory programmed MID support software. This software package provides several software functions that allow to use all MID features.

The MID functionality can be enabled for different flash memory ranges. These memory ranges are selectable by the cw0 parameter of the MID function MidEnable(). Details about address range coverage is listed in Table 6-8.

For further information, see the *MID Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU459).

**Table 6-8. Address Range Coverage of cw0 Parameter of MidEnable() Function**

| BITS OF cw0 PARAMETER | ADDRESS RANGE |
|---|---|
| cw0.15 | 087FFFh-080000h |
| cw0.14 | 07FFFFh-078000h |
| cw0.13 | 077FFFh-070000h |
| cw0.12 | 06FFFFh-068000h |
| cw0.11 | 067FFFh-060000h |
| cw0.10 | 05FFFFh-058000h |
| cw0.9 | 057FFFh-050000h |
| cw0.8 | 04FFFFh-048000h |
| cw0.7 | 047FFFh-040000h |
| cw0.6 | 03FFFFh-038000h |
| cw0.5 | 037FFFh-030000h |
| cw0.4 | 02FFFFh-028000h |
| cw0.3 | 027FFFh-020000h |
| cw0.2 | 01FFFFh-018000h |
| cw0.1 | 017FFFh-010000h |
| cw0.0 | 00FFFFh-008000h |

## 6.11 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in Section 6.6.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

For further information, see the *RAM Controller Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU393).


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## 6.12 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the battery backup system module is implemented.

There are 8 bytes of backup RAM available. It can be word-wise accessed by the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

For further information, see the *Backup RAM Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU394).

## 6.13 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

### 6.13.1 Digital I/O

There are up to nine 8-bit I/O ports implemented: P1 through P9 are complete and port PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PD).

For further information, see the *Digital I/O Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU396).

### 6.13.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2. Table 6-9 lists the available mappings, and Table 6-10 lists the default settings.

For further information, see the *Port Mapping Controller Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU397).

**Table 6-9. Port Mapping Mnemonics and Functions**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_CBOUT | – | Comparator_B output |
| | PM_TB0CLK | Timer TB0 clock input | – |
| 2 | PM_ADC12CLK | – | ADC12CLK |
| | PM_DMAE0 | DMAE0 Input | – |
| 3 | PM_SVMOUT | – | SVM output |
| | PM_TB0OUTH | Timer TB0 high impedance input TB0OUTH | – |
| 4 | PM_TB0CCR0B | Timer TB0 CCR0 capture input CCI0B | Timer TB0: TB0.0 compare output Out0 |
| 5 | PM_TB0CCR1B | Timer TB0 CCR1 capture input CCI1B | Timer TB0: TB0.1 compare output Out1 |
| 6 | PM_TB0CCR2B | Timer TB0 CCR2 capture input CCI2B | Timer TB0: TB0.2 compare output Out2 |
| 7 | PM_TB0CCR3B | Timer TB0 CCR3 capture input CCI3B | Timer TB0: TB0.3 compare output Out3 |
| 8 | PM_TB0CCR4B | Timer TB0 CCR4 capture input CCI4B | Timer TB0: TB0.4 compare output Out4 |
| 9 | PM_TB0CCR5B | Timer TB0 CCR5 capture input CCI5B | Timer TB0: TB0.5 compare output Out5 |

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**Table 6-9. Port Mapping Mnemonics and Functions (continued)**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 10 | PM_TB0CCR6B | Timer TB0 CCR6 capture input CCI6B | Timer TB0: TB0.6 compare output Out6 |
| 11 | PM_UCA0RXD | USCI_A0 UART RXD (Direction controlled by USCI - input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 12 | PM_UCA0TXD | USCI_A0 UART TXD (Direction controlled by USCI - output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 13 | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 14 | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 I2C clock (open drain and direction controlled by USCI) | |
| 15 | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| 16 | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 17 | PM_MCLK | – | MCLK |
| 18 | Reserved | Reserved for test purposes. Do not use this setting. | |
| 19 | Reserved | Reserved for test purposes. Do not use this setting. | |
| 20-30 | Reserved | None | DVSS |
| 31 (0FFh) (1) | PM_ANALOG | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.

**Table 6-10. Default Mapping**

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| P2.0/P2MAP0 | PM_UCB0STE, PM_UCA0CLK | USCI_B0 SPI slave transmit enable (direction controlled by USCI - input), USCI_A0 clock input/output (direction controlled by USCI) | |
| P2.1/P2MAP1 | PM_UCB0SIMO, PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| P2.2/P2MAP2 | PM_UCB0SOMI, PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 I2C clock (open drain and direction controlled by USCI) | |
| P2.3/P2MAP3 | PM_UCB0CLK, PM_UCA0STE | USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| P2.4/P2MAP4 | PM_UCA0TXD, PM_UCA0SIMO | USCI_A0 UART TXD (direction controlled by USCI - output), USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| P2.5/P2MAP5 | PM_UCA0RXD, PM_UCA0SOMI | USCI_A0 UART RXD (direction controlled by USCI - input), USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| P2.6/P2MAP6/ R03 | PM_NONE | – | DVSS |
| P2.7/P2MAP7/LCDREF/R13 | PM_NONE | – | DVSS |


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### 6.13.3 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

For further information, see the *UCS Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU390).

### 6.13.4 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

For further information, see the *PMM Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU388).

### 6.13.5 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

For further information, see the *MPY Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU404).

### 6.13.6 Real-Time Clock (RTC_B)

The RTC_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

The application report *Using the MSP430 RTC_B Module With Battery Backup Supply* (SLAA665) describes how to use the RTC_B with battery backup supply functionality to retain the time and keep the RTC counting through loss of main power supply, as well as how to handle correct reinitialization when the main power supply is restored.

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For further information, see the *RTC_B Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU403).

### 6.13.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

For further information, see the *WDT_A Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU399).

### 6.13.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators (see Table 6-11), bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

For further information, see the *SYS Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU387).

**Table 6-11. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | RST/NMI (BOR) | | 04h | |
| | PMMSWBOR (BOR) | | 06h | |
| | LPM3.5 or LPM4.5 wakeup (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | SVSL (POR) | | 0Ch | |
| | SVSH (POR) | | 0Eh | |
| | SVML_OVP (POR) | | 10h | |
| | SVMH_OVP (POR) | | 12h | |
| | PMMSWPOR (POR) | | 14h | |
| | WDT time-out (PUC) | | 16h | |
| | WDT key violation (PUC) | | 18h | |
| | KEYV flash key violation (PUC) | | 1Ah | |
| | Reserved | | 1Ch | |
| | Peripheral area fetch (PUC) | | 1Eh | |
| | PMM key violation (PUC) | | 20h | |
| | Reserved | | 22h to 3Eh | Lowest |


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**Table 6-11. System Module Interrupt Vector Registers (continued)**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---|---|---|---|---|
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | |
| | SVMLIFG | | 02h | Highest |
| | SVMHIFG | | 04h | |
| | DLYLIFG | | 06h | |
| | DLYHIFG | | 08h | |
| | VMAIFG | | 0Ah | |
| | JMBINIFG | | 0Ch | |
| | JMBOUTIFG | | 0Eh | |
| | SVMLVLRIFG | | 10h | |
| | SVMHVLRIFG | | 12h | |
| | Reserved | | 14h to 1Eh | Lowest |
| SYSUNIV, User NMI | No interrupt pending | 019Ah | 00h | |
| | NMIIFG | | 02h | Highest |
| | OFIFG | | 04h | |
| | ACCVIFG | | 06h | |
| | BUSIFG | | 08h | |
| | Reserved | | 0Ah to 1Eh | Lowest |
| SYSBERRIV, Bus Error | No interrupt pending | 0198h | 00h | |
| | Reserved | | 02h | Highest |
| | | | 04h | |
| | MID error | | 06h | |
| | Reserved | | 08h to 1Eh | Lowest |

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### 6.13.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

For further information, see the *DMA Controller Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU395).

**Table 6-12. DMA Trigger Assignments(1)**

| TRIGGER | CHANNEL | | | | | |
|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 |
| 0 | DMAREQ | | | | | |
| 1 | TA0CCR0 CCIFG | | | | | |
| 2 | TA0CCR2 CCIFG | | | | | |
| 3 | TA1CCR0 CCIFG | | | | | |
| 4 | TA1CCR2 CCIFG | | | | | |
| 5 | TA2CCR0 CCIFG | | | | | |
| 6 | TA2CCR2 CCIFG | | | | | |
| 7 | TBCCR0 CCIFG | | | | | |
| 8 | TBCCR2 CCIFG | | | | | |
| 9 | Reserved | | | | | |
| 10 | Reserved | | | | | |
| 11 | Reserved | | | | | |
| 12 | UCA2RXIFG | | | | | |
| 13 | UCA2TXIFG | | | | | |
| 14 | UCB2RXIFG | | | | | |
| 15 | UCB2TXIFG | | | | | |
| 16 | UCA0RXIFG | | | | | |
| 17 | UCA0TXIFG | | | | | |
| 18 | UCB0RXIFG | | | | | |
| 19 | UCB0TXIFG | | | | | |
| 20 | UCA1RXIFG | | | | | |
| 21 | UCA1TXIFG | | | | | |
| 22 | UCB1RXIFG | | | | | |
| 23 | UCB1TXIFG | | | | | |
| 24 | ADC12IFGx | | | | | |
| 25 | DAC12_0IFG | | | | | |
| 26 | DAC12_1IFG | | | | | |
| 27 | Reserved | | | | | |
| 28 | Reserved | | | | | |
| 29 | MPY ready | | | | | |
| 30 | DMA5IFG | DMA0IFG | DMA1IFG | DMA2IFG | DMA3IFG | DMA4IFG |
| 31 | DMAE0 | | | | | |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.


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### 6.13.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3-pin or 4-pin) or $I^2C$.

The MSP430F665x, MSP430F645x, MSP430F565x, MSP430F535x series includes three complete USCI modules (n = 0 to 2).

For further information, see the following User's Guides:

- *USCI UART Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU410)
- *USCI SPI Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU411)
- *USCI I2C Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU412)

### 6.13.11 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers (see Table 6-13). TA0 supports multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

For further information, see the *Timer_A Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU400).

**Table 6-13. Timer TA0 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 34-P1.0 | TA0CLK | TACLK | Timer | NA | NA | |
| | ACLK | ACLK | | | | |
| | SMCLK | SMCLK | | | | |
| 34-P1.0 | TA0CLK | $\overline{\text{TACLK}}$ | | | | |
| 35-P1.1 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 35-P1.1 |
| | $DV_{SS}$ | CCI0B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 36-P1.2 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 36-P1.2 |
| 40-P1.6 | TA0.1 | CCI1B | | | | 40-P1.6 |
| | $DV_{SS}$ | GND | | | | ADC12_A (internal) ADC12SHSx = {1} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 37-P1.3 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 37-P1.3 |
| 41-P1.7 | TA0.2 | CCI2B | | | | 41-P1.7 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 38-P1.4 | TA0.3 | CCI3A | CCR3 | TA3 | TA0.3 | 38-P1.4 |
| | $DV_{SS}$ | CCI3B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

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**Table 6-13. Timer TA0 Signal Connections (continued)**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 39-P1.5 | TA0.4 | CCI4A | CCR4 | TA4 | TA0.4 | 39-P1.5 |
| | $DV_{SS}$ | CCI4B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |


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### 6.13.12 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers (see Table 6-14). TA1 supports multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

For further information, see the *Timer_A Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU400).

**Table 6-14. Timer TA1 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 42-P3.0 | TA1CLK | TACLK | Timer | NA | NA | |
| | ACLK | ACLK | | | | |
| | SMCLK | SMCLK | | | | |
| 42-P3.0 | TA1CLK | $\overline{\text{TACLK}}$ | | | | |
| 43-P3.1 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 43-P3.1 |
| | $DV_{SS}$ | CCI0B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 44-P3.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 44-P3.2 |
| | CBOUT (internal) | CCI1B | | | | DAC12_A DAC12_0, DAC12_1 (internal) |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 45-P3.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 45-P3.3 |
| | ACLK (internal) | CCI2B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

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### 6.13.13 Timer TA2

Timer TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers (see Table 6-15). TA2 supports multiple capture/compares, PWM outputs, and interval timing. TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

For further information, see the *Timer_A Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU400).

**Table 6-15. Timer TA2 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 46-P3.4 | TA2CLK | TACLK | Timer | NA | NA | |
| | ACLK | ACLK | | | | |
| | SMCLK | SMCLK | | | | |
| 46-P3.4 | TA2CLK | $\overline{\text{TACLK}}$ | | | | |
| 47-P3.5 | TA2.0 | CCI0A | CCR0 | TA0 | TA2.0 | 47-P3.5 |
| | $DV_{SS}$ | CCI0B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 48-P3.6 | TA2.1 | CCI1A | CCR1 | TA1 | TA2.1 | 48-P3.6 |
| | CBOUT (internal) | CCI1B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 49-P3.7 | TA2.2 | CCI2A | CCR2 | TA2 | TA2.2 | 49-P3.7 |
| | ACLK (internal) | CCI2B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |


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### 6.13.14 Timer TB0

Timer TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers (see Table 6-16). TB0 supports multiple capture/compares, PWM outputs, and interval timing. TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

For further information, see the *Timer_B Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU401).

**Table 6-16. Timer TB0 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 58-P8.0 P2MAPx(1) | TB0CLK | TB0CLK | Timer | NA | NA | |
| | ACLK | ACLK | | | | |
| | SMCLK | SMCLK | | | | |
| 58-P8.0 P2MAPx(1) | TB0CLK | $\overline{\text{TB0CLK}}$ | | | | |
| 50-P4.0 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 50-P4.0 |
| P2MAPx(1) | TB0.0 | CCI0B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {2} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 51-P4.1 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 51-P4.1 |
| P2MAPx(1) | TB0.1 | CCI1B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {3} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 52-P4.2 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 52-P4.2 |
| P2MAPx(1) | TB0.2 | CCI2B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | DAC12_A DAC12_0, DAC12_1 (internal) |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 53-P4.3 | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | 53-P4.3 |
| P2MAPx(1) | TB0.3 | CCI3B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 54-P4.4 | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | 54-P4.4 |
| P2MAPx(1) | TB0.4 | CCI4B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 55-P4.5 | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | 55-P4.5 |
| P2MAPx(1) | TB0.5 | CCI5B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 56-P4.6 | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | 56-P4.6 |
| P2MAPx(1) | TB0.6 | CCI6B | | | | P2MAPx(1) |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

(1) Timer functions are selectable through the port mapping controller.

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### 6.13.15 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

For further information, see the *COMP_B Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU408).

### 6.13.16 ADC12_A

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

For further information, see the *ADC12_A Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU406).

### 6.13.17 DAC12_A

The DAC12_A module is a 12-bit, R-ladder, voltage output DAC. The DAC12_A may be used in 8-bit or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12_A modules are present, they may be grouped together for synchronous operation.

### 6.13.18 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

For further information, see the *CRC Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU398).

### 6.13.19 Voltage Reference (REF) Module

The REF module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

For further information, see the *REF Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU405).

### 6.13.20 LCD_B

The LCD_B driver generates the segment and common signals that are required to drive a liquid crystal display (LCD). The LCD_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments.

The LCD_B module is only available on the MSP430F665x and MSP430F645x devices.

For further information, see the *LCD_B Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU409).

### 6.13.21 LDO and PU Port

The integrated 3.3-V power system incorporates an integrated 3.3-V LDO regulator that allows the entire MSP430 microcontroller to be powered from nominal 5-V LDOI when it is made available for the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether.


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The Port U Pins (PU.0 and PU.1) function as general-purpose high-current I/O pins. These pins can only be configured together as either both inputs or both outputs. Port U is supplied by the LDOO rail. If the 3.3-V LDO is not being used in the system (disabled), the LDOO pin can be supplied externally.

The LDO-PWR module (LDO and PU Port) is only available on the MSP430F645x and MSP430F535x devices.

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### 6.13.22 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

For further information, see the *EEM Module (Chapter Excerpt From MSP430x5xx Family, SLAU208)* (SLAU414).

### 6.13.23 Peripheral File Map

Table 6-17 lists the base register address for each available peripheral.

**Table 6-17. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE(1) |
|---|---|---|
| Special Functions (see Table 6-18) | 0100h | 000h-01Fh |
| PMM (see Table 6-19) | 0120h | 000h-010h |
| Flash Control (see Table 6-20) | 0140h | 000h-00Fh |
| CRC16 (see Table 6-21) | 0150h | 000h-007h |
| RAM Control (see Table 6-22) | 0158h | 000h-001h |
| Watchdog (see Table 6-23) | 015Ch | 000h-001h |
| UCS (see Table 6-24) | 0160h | 000h-01Fh |
| SYS (see Table 6-25) | 0180h | 000h-01Fh |
| Shared Reference (see Table 6-26) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 6-27) | 01C0h | 000h-003h |
| Port Mapping Port P2 (see Table 6-27) | 01D0h | 000h-007h |
| Port P1, P2 (see Table 6-28) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 6-29) | 0220h | 000h-01Fh |
| Port P5, P6 (see Table 6-30) | 0240h | 000h-00Bh |
| Port P7, P8 (see Table 6-31) | 0260h | 000h-00Bh |
| Port P9 (see Table 6-32) | 0280h | 000h-00Bh |
| Port PJ (see Table 6-33) | 0320h | 000h-01Fh |
| Timer TA0 (see Table 6-34) | 0340h | 000h-02Eh |
| Timer TA1 (see Table 6-35) | 0380h | 000h-02Eh |
| Timer TB0 (see Table 6-36) | 03C0h | 000h-02Eh |
| Timer TA2 (see Table 6-37) | 0400h | 000h-02Eh |
| Battery Backup (see Table 6-38) | 0480h | 000h-01Fh |
| RTC_B (see Table 6-39) | 04A0h | 000h-01Fh |
| 32-Bit Hardware Multiplier (see Table 6-40) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 6-41) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 6-41) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 6-41) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 6-41) | 0530h | 000h-00Ah |
| DMA Channel 3 (see Table 6-41) | 0540h | 000h-00Ah |

(1) For a detailed description of the individual control register offset addresses, see the *MSP430F5xx and MSP430F6xx Family User's Guide* (SLAU208).


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**Table 6-17. Peripherals (continued)**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE(1) |
|---|---|---|
| DMA Channel 4 (see Table 6-41) | 0550h | 000h-00Ah |
| DMA Channel 5 (see Table 6-41) | 0560h | 000h-00Ah |
| USCI_A0 (see Table 6-42) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 6-43) | 05E0h | 000h-01Fh |
| USCI_A1 (see Table 6-44) | 0600h | 000h-01Fh |
| USCI_B1 (see Table 6-45) | 0620h | 000h-01Fh |
| USCI_A2 (see Table 6-46) | 0640h | 000h-01Fh |
| USCI_B2 (see Table 6-47) | 0660h | 000h-01Fh |
| ADC12_A (see Table 6-48) | 0700h | 000h-03Fh |
| DAC12_A (see Table 6-49) | 0780h | 000h-01Fh |
| Comparator_B (see Table 6-50) | 08C0h | 000h-00Fh |
| LDO-PWR; LDO and Port U configuration (see Table 6-51) (2) | 0900h | 000h-014h |
| LCD_B control (see Table 6-52) (3) | 0A00h | 000h-05Fh |

(2) Only on devices with peripheral module LDO-PWR.
(3) Only on devices with peripheral module LCD_B.

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**Table 6-18. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 6-19. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

**Table 6-20. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

**Table 6-21. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC result | CRC16INIRES | 04h |

**Table 6-22. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RAM control 0 | RCCTL0 | 00h |

**Table 6-23. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**Table 6-24. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |


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**Table 6-25. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**Table 6-26. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**Table 6-27. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01D0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port mapping password | PMAPPWD | 00h |
| Port mapping control | PMAPCTL | 02h |
| Port P2.0 mapping | P2MAP0 | 00h |
| Port P2.1 mapping | P2MAP1 | 01h |
| Port P2.2 mapping | P2MAP2 | 02h |
| Port P2.3 mapping | P2MAP3 | 03h |
| Port P2.4 mapping | P2MAP4 | 04h |
| Port P2.5 mapping | P2MAP5 | 05h |
| Port P2.6 mapping | P2MAP6 | 06h |
| Port P2.7 mapping | P2MAP7 | 07h |

**Table 6-28. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |

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**Table 6-28. Port P1, P2 Registers (Base Address: 0200h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**Table 6-29. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

**Table 6-30. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pullup/pulldown enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pullup/pulldown enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |


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**Table 6-31. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 pullup/pulldown enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 pullup/pulldown enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

**Table 6-32. Port P9 Register (Base Address: 0280h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 pullup/pulldown enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |

**Table 6-33. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

**Table 6-34. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| Capture/compare control 3 | TA0CCTL3 | 08h |
| Capture/compare control 4 | TA0CCTL4 | 0Ah |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| Capture/compare 3 | TA0CCR3 | 18h |
| Capture/compare 4 | TA0CCR4 | 1Ah |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

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**Table 6-35. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 6-36. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| Capture/compare control 3 | TB0CCTL3 | 08h |
| Capture/compare control 4 | TB0CCTL4 | 0Ah |
| Capture/compare control 5 | TB0CCTL5 | 0Ch |
| Capture/compare control 6 | TB0CCTL6 | 0Eh |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| Capture/compare 3 | TB0CCR3 | 18h |
| Capture/compare 4 | TB0CCR4 | 1Ah |
| Capture/compare 5 | TB0CCR5 | 1Ch |
| Capture/compare 6 | TB0CCR6 | 1Eh |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

**Table 6-37. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| Capture/compare control 2 | TA2CCTL2 | 06h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| Capture/compare 2 | TA2CCR2 | 16h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |


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**Table 6-38. Battery Backup Registers (Base Address: 0480h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Battery backup memory 0 | BAKMEM0 | 00h |
| Battery backup memory 1 | BAKMEM1 | 02h |
| Battery backup memory 2 | BAKMEM2 | 04h |
| Battery backup memory 3 | BAKMEM3 | 06h |
| Battery backup control | BAKCTL | 1Ch |
| Battery charger control | BAKCHCTL | 1Eh |

**Table 6-39. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-binary conversion | BCD2BIN | 1Eh |

**Table 6-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |

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**Table 6-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**Table 6-41. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA general control: DMA module control 0 | DMACTL0 | 00h |
| DMA general control: DMA module control 1 | DMACTL1 | 02h |
| DMA general control: DMA module control 2 | DMACTL2 | 04h |
| DMA general control: DMA module control 3 | DMACTL3 | 06h |
| DMA general control: DMA module control 4 | DMACTL4 | 08h |
| DMA general control: DMA interrupt vector | DMAIV | 0Ah |
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA channel 3 control | DMA3CTL | 00h |
| DMA channel 3 source address low | DMA3SAL | 02h |
| DMA channel 3 source address high | DMA3SAH | 04h |
| DMA channel 3 destination address low | DMA3DAL | 06h |
| DMA channel 3 destination address high | DMA3DAH | 08h |
| DMA channel 3 transfer size | DMA3SZ | 0Ah |
| DMA channel 4 control | DMA4CTL | 00h |


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**Table 6-41. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 4 source address low | DMA4SAL | 02h |
| DMA channel 4 source address high | DMA4SAH | 04h |
| DMA channel 4 destination address low | DMA4DAL | 06h |
| DMA channel 4 destination address high | DMA4DAH | 08h |
| DMA channel 4 transfer size | DMA4SZ | 0Ah |
| DMA channel 5 control | DMA5CTL | 00h |
| DMA channel 5 source address low | DMA5SAL | 02h |
| DMA channel 5 source address high | DMA5SAH | 04h |
| DMA channel 5 destination address low | DMA5DAL | 06h |
| DMA channel 5 destination address high | DMA5DAH | 08h |
| DMA channel 5 transfer size | DMA5SZ | 0Ah |

**Table 6-42. USCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI control 0 | UCA0CTL0 | 00h |
| USCI control 1 | UCA0CTL1 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

**Table 6-43. USCI_B0 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI synchronous control 0 | UCB0CTL0 | 00h |
| USCI synchronous control 1 | UCB0CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

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**Table 6-44. USCI_A1 Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI control 0 | UCA1CTL0 | 00h |
| USCI control 1 | UCA1CTL1 | 01h |
| USCI baud rate 0 | UCA1BR0 | 06h |
| USCI baud rate 1 | UCA1BR1 | 07h |
| USCI modulation control | UCA1MCTL | 08h |
| USCI status | UCA1STAT | 0Ah |
| USCI receive buffer | UCA1RXBUF | 0Ch |
| USCI transmit buffer | UCA1TXBUF | 0Eh |
| USCI LIN control | UCA1ABCTL | 10h |
| USCI IrDA transmit control | UCA1IRTCTL | 12h |
| USCI IrDA receive control | UCA1IRRCTL | 13h |
| USCI interrupt enable | UCA1IE | 1Ch |
| USCI interrupt flags | UCA1IFG | 1Dh |
| USCI interrupt vector word | UCA1IV | 1Eh |

**Table 6-45. USCI_B1 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI synchronous control 0 | UCB1CTL0 | 00h |
| USCI synchronous control 1 | UCB1CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB1BR0 | 06h |
| USCI synchronous bit rate 1 | UCB1BR1 | 07h |
| USCI synchronous status | UCB1STAT | 0Ah |
| USCI synchronous receive buffer | UCB1RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh |
| USCI I2C own address | UCB1I2COA | 10h |
| USCI I2C slave address | UCB1I2CSA | 12h |
| USCI interrupt enable | UCB1IE | 1Ch |
| USCI interrupt flags | UCB1IFG | 1Dh |
| USCI interrupt vector word | UCB1IV | 1Eh |

**Table 6-46. USCI_A2 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI control 0 | UCA2CTL0 | 00h |
| USCI control 1 | UCA2CTL1 | 01h |
| USCI baud rate 0 | UCA2BR0 | 06h |
| USCI baud rate 1 | UCA2BR1 | 07h |
| USCI modulation control | UCA2MCTL | 08h |
| USCI status | UCA2STAT | 0Ah |
| USCI receive buffer | UCA2RXBUF | 0Ch |
| USCI transmit buffer | UCA2TXBUF | 0Eh |
| USCI LIN control | UCA2ABCTL | 10h |
| USCI IrDA transmit control | UCA2IRTCTL | 12h |
| USCI IrDA receive control | UCA2IRRCTL | 13h |
| USCI interrupt enable | UCA2IE | 1Ch |
| USCI interrupt flags | UCA2IFG | 1Dh |
| USCI interrupt vector word | UCA2IV | 1Eh |


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**Table 6-47. USCI_B2 Registers (Base Address: 0660h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI synchronous control 0 | UCB2CTL0 | 00h |
| USCI synchronous control 1 | UCB2CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB2BR0 | 06h |
| USCI synchronous bit rate 1 | UCB2BR1 | 07h |
| USCI synchronous status | UCB2STAT | 0Ah |
| USCI synchronous receive buffer | UCB2RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB2TXBUF | 0Eh |
| USCI I2C own address | UCB2I2COA | 10h |
| USCI I2C slave address | UCB2I2CSA | 12h |
| USCI interrupt enable | UCB2IE | 1Ch |
| USCI interrupt flags | UCB2IFG | 1Dh |
| USCI interrupt vector word | UCB2IV | 1Eh |

**Table 6-48. ADC12_A Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC12 control 0 | ADC12CTL0 | 00h |
| ADC12 control 1 | ADC12CTL1 | 02h |
| ADC12 control 2 | ADC12CTL2 | 04h |
| Interrupt flag | ADC12IFG | 0Ah |
| Interrupt enable | ADC12IE | 0Ch |
| Interrupt vector word | ADC12IV | 0Eh |
| ADC memory control 0 | ADC12MCTL0 | 10h |
| ADC memory control 1 | ADC12MCTL1 | 11h |
| ADC memory control 2 | ADC12MCTL2 | 12h |
| ADC memory control 3 | ADC12MCTL3 | 13h |
| ADC memory control 4 | ADC12MCTL4 | 14h |
| ADC memory control 5 | ADC12MCTL5 | 15h |
| ADC memory control 6 | ADC12MCTL6 | 16h |
| ADC memory control 7 | ADC12MCTL7 | 17h |
| ADC memory control 8 | ADC12MCTL8 | 18h |
| ADC memory control 9 | ADC12MCTL9 | 19h |
| ADC memory control 10 | ADC12MCTL10 | 1Ah |
| ADC memory control 11 | ADC12MCTL11 | 1Bh |
| ADC memory control 12 | ADC12MCTL12 | 1Ch |
| ADC memory control 13 | ADC12MCTL13 | 1Dh |
| ADC memory control 14 | ADC12MCTL14 | 1Eh |
| ADC memory control 15 | ADC12MCTL15 | 1Fh |
| Conversion memory 0 | ADC12MEM0 | 20h |
| Conversion memory 1 | ADC12MEM1 | 22h |
| Conversion memory 2 | ADC12MEM2 | 24h |
| Conversion memory 3 | ADC12MEM3 | 26h |
| Conversion memory 4 | ADC12MEM4 | 28h |
| Conversion memory 5 | ADC12MEM5 | 2Ah |
| Conversion memory 6 | ADC12MEM6 | 2Ch |
| Conversion memory 7 | ADC12MEM7 | 2Eh |
| Conversion memory 8 | ADC12MEM8 | 30h |
| Conversion memory 9 | ADC12MEM9 | 32h |

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**Table 6-48. ADC12_A Registers (Base Address: 0700h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Conversion memory 10 | ADC12MEM10 | 34h |
| Conversion memory 11 | ADC12MEM11 | 36h |
| Conversion memory 12 | ADC12MEM12 | 38h |
| Conversion memory 13 | ADC12MEM13 | 3Ah |
| Conversion memory 14 | ADC12MEM14 | 3Ch |
| Conversion memory 15 | ADC12MEM15 | 3Eh |

**Table 6-49. DAC12_A Registers (Base Address: 0780h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DAC12_A channel 0 control 0 | DAC12_0CTL0 | 00h |
| DAC12_A channel 0 control 1 | DAC12_0CTL1 | 02h |
| DAC12_A channel 0 data | DAC12_0DAT | 04h |
| DAC12_A channel 0 calibration control | DAC12_0CALCTL | 06h |
| DAC12_A channel 0 calibration data | DAC12_0CALDAT | 08h |
| DAC12_A channel 1 control 0 | DAC12_1CTL0 | 10h |
| DAC12_A channel 1 control 1 | DAC12_1CTL1 | 12h |
| DAC12_A channel 1 data | DAC12_1DAT | 14h |
| DAC12_A channel 1 calibration control | DAC12_1CALCTL | 16h |
| DAC12_A channel 1 calibration data | DAC12_1CALDAT | 18h |
| DAC12_A interrupt vector word | DAC12IV | 1Eh |

**Table 6-50. Comparator_B Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comp_B control 0 | CBCTL0 | 00h |
| Comp_B control 1 | CBCTL1 | 02h |
| Comp_B control 2 | CBCTL2 | 04h |
| Comp_B control 3 | CBCTL3 | 06h |
| Comp_B interrupt | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

**Table 6-51. LDO and Port U Configuration Registers (Base Address: 0900h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LDO key/ID | LDOKEYID | 00h |
| PU port control | PUCTL | 04h |
| LDO power control | LDOPWRCTL | 08h |

**Table 6-52. LCD_B Registers (Base Address: 0A00h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_B control 0 | LCDBCTL0 | 000h |
| LCD_B control 1 | LCDBCTL1 | 002h |
| LCD_B blinking control | LCDBBLKCTL | 004h |
| LCD_B memory control | LCDBMEMCTL | 006h |
| LCD_B voltage control | LCDBVCTL | 008h |
| LCD_B port control 0 | LCDBPCTL0 | 00Ah |
| LCD_B port control 1 | LCDBPCTL1 | 00Ch |
| LCD_B port control 2 | LCDBPCTL2 | 00Eh |


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**Table 6-52. LCD_B Registers (Base Address: 0A00h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_B charge pump control | LCDBCTL0 | 012h |
| LCD_B interrupt vector word | LCDBIV | 01Eh |
| LCD_B memory 1 | LCDM1 | 020h |
| LCD_B memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_B memory 22 | LCDM22 | 035h |
| LCD_B blinking memory 1 | LCDBM1 | 040h |
| LCD_B blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_B blinking memory 22 | LCDBM22 | 055h |

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## 6.14 Input/Output Schematics

### 6.14.1 Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

Figure 6-2 shows the port schematic. summarizes selection of the pin function.

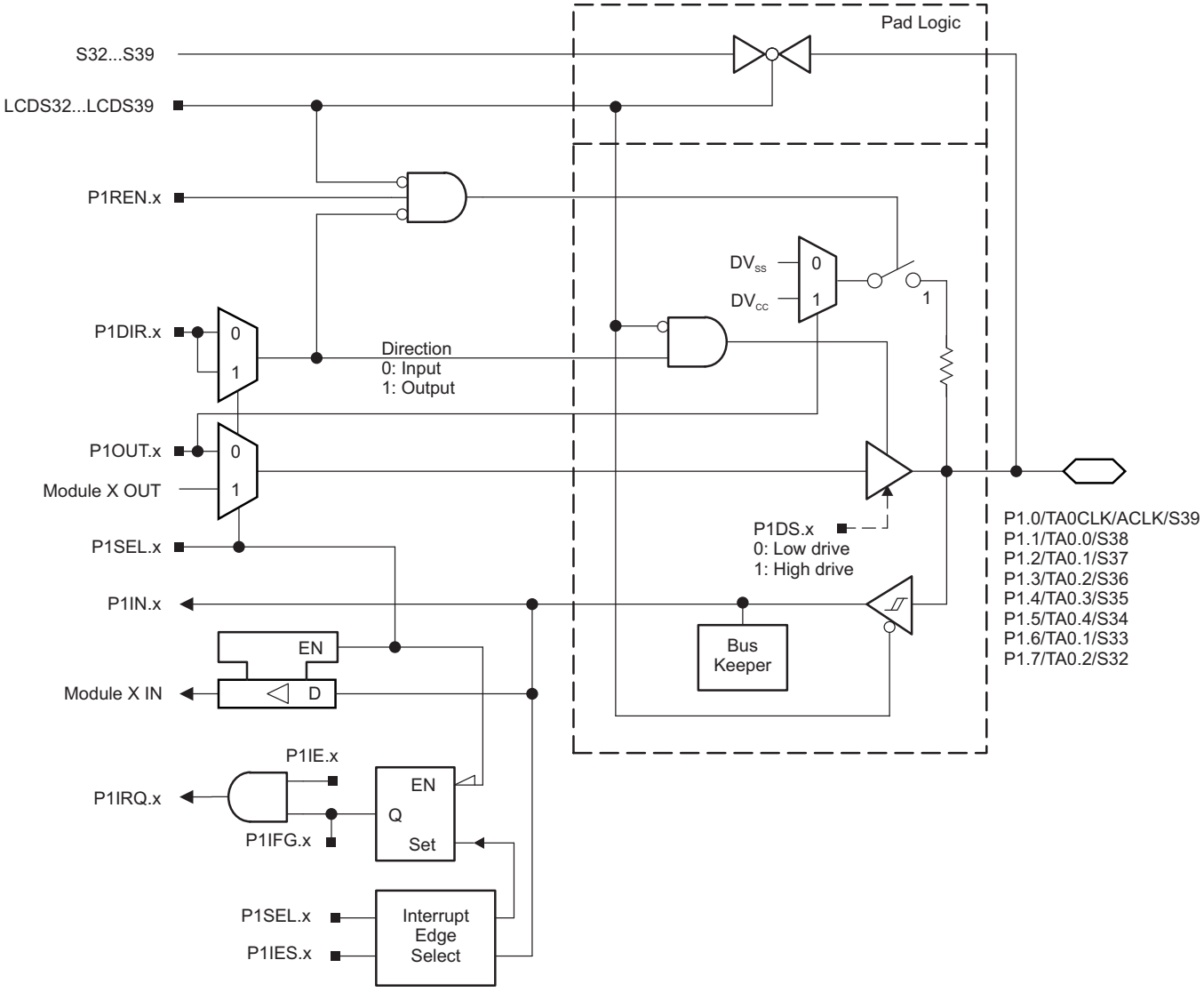


**Figure 6-2. Port P1 (P1.0 to P1.7) Schematic**


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**Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | LCDS32...39 |
| P1.0/TA0CLK/ACLK/ S39 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.TA0CLK | 0 | 1 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | S39 | X | X | 1 |
| P1.1/TA0.0/S38 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA0.0 output | 1 | 1 | 0 |
| | | S38 | X | X | 1 |
| P1.2/TA0.1/S37 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA0.1 output | 1 | 1 | 0 |
| | | S37 | X | X | 1 |
| P1.3/TA0.2/S36 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA0.2 output | 1 | 1 | 0 |
| | | S36 | X | X | 1 |
| P1.4/TA0.3/S35 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI3A capture input | 0 | 1 | 0 |
| | | Timer TA0.3 output | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P1.5/TA0.4/S34 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI4A capture input | 0 | 1 | 0 |
| | | Timer TA0.4 output | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P1.6/TA0.1/S33 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI1B capture input | 0 | 1 | 0 |
| | | Timer TA0.1 output | 1 | 1 | 0 |
| | | S33 | X | X | 1 |
| P1.7/TA0.2/S32 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI2B capture input | 0 | 1 | 0 |
| | | Timer TA0.2 output | 1 | 1 | 0 |
| | | S32 | X | X | 1 |

(1) X = Don't care

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### 6.14.2 Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

Figure 6-3 shows the port schematic. summarizes selection of the pin function.

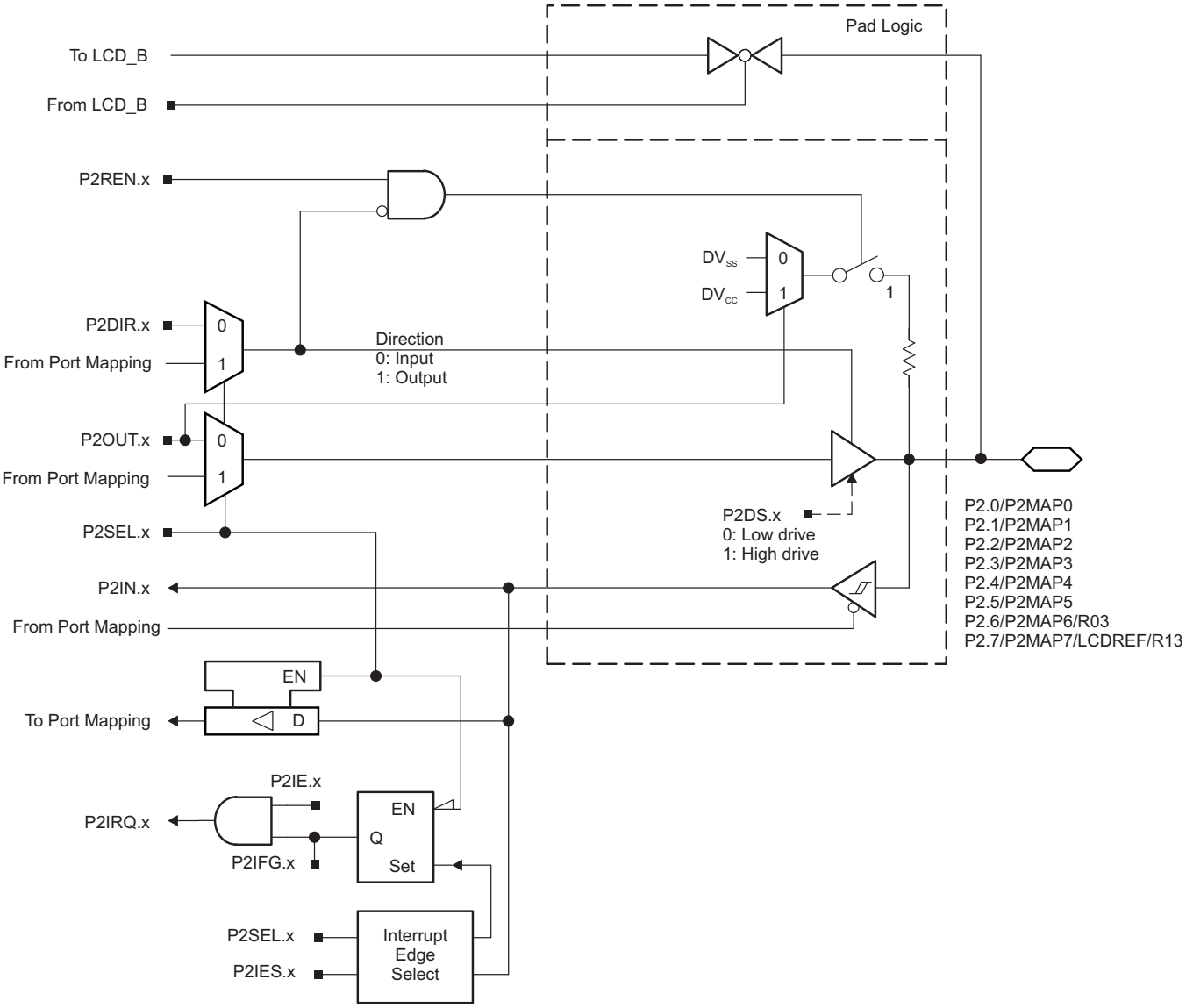


**Figure 6-3. Port P2 (P2.0 to P2.7) Schematic**


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**Port P2 (P2.0 to P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx |
| P2.0/P2MAP0 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.1/P2MAP1 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.2/P2MAP2 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.3/P2MAP3 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.4/P2MAP4 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.5/P2MAP5 | 5 | P2.5 (I/O | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.6/P2MAP6/R03 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| | | R03 | X | 1 | = 31 |
| P2.7/P2MAP7/ LCDREF/R13 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| | | LCDREF/R13 | X | 1 | = 31 |

(1) X = Don't care

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### 6.14.3 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

Figure 6-4 shows the port schematic. summarizes selection of the pin function.

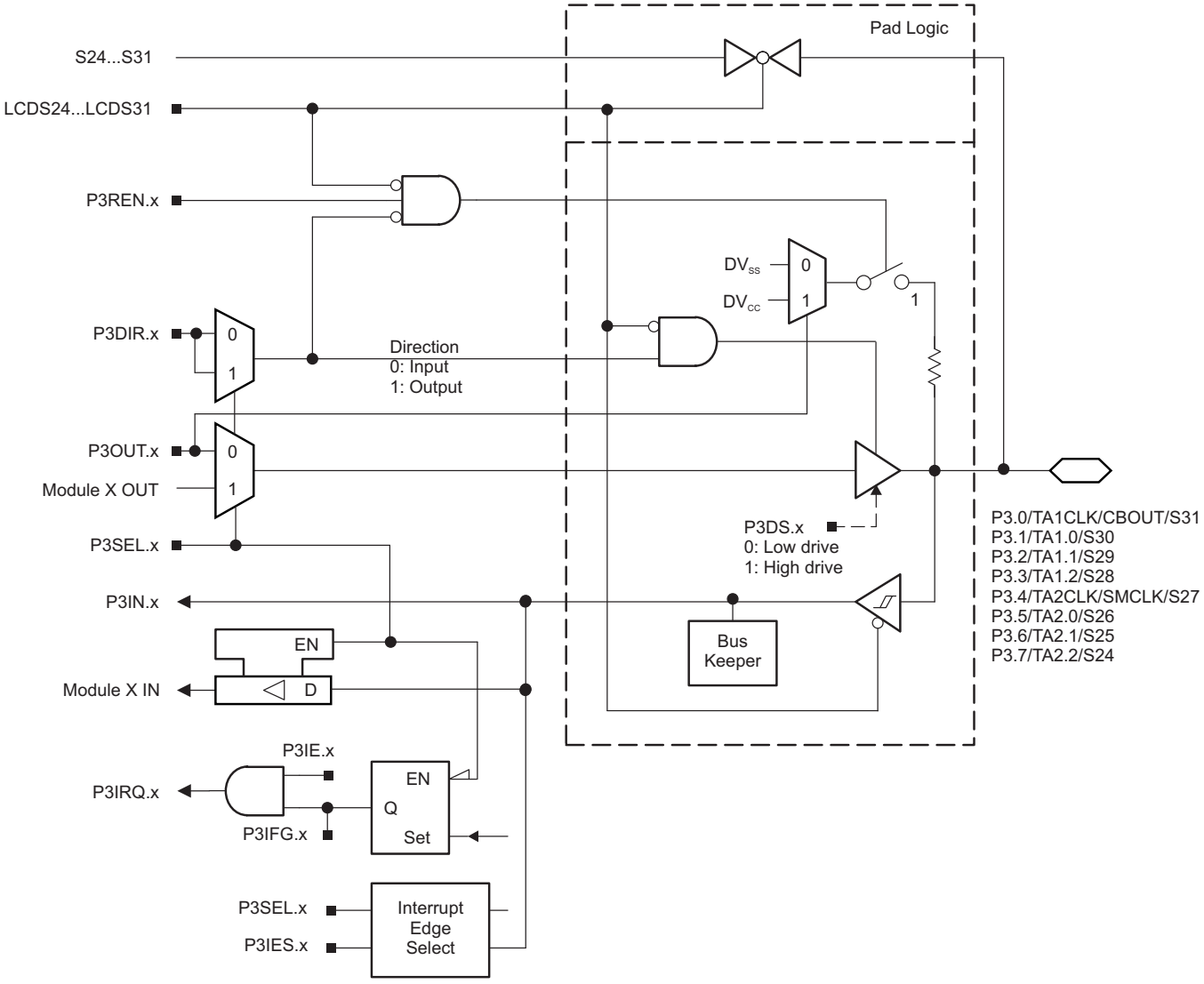


**Figure 6-4. Port P3 (P3.0 to P3.7) Schematic**


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**Port P3 (P3.0 to P3.7) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | LCDS24...31 |
| P3.0/TA1CLK/CBOUT/S31 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.TA1CLK | 0 | 1 | 0 |
| | | CBOUT | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P3.1/TA1.0/S30 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA1.0 output | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P3.2/TA1.1/S29 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA1.1 output | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P3.3/TA1.2/S28 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA1.2 output | 1 | 1 | 0 |
| | | S28 | X | X | 1 |
| P3.4/TA2CLK/SMCLK/S27 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.TA2CLK | 0 | 1 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P3.5/TA2.0/S26 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA2.0 output | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P3.6/TA2.1/S25 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA2.1 output | 1 | 1 | 1 |
| | | S25 | X | X | 1 |
| P3.7/TA2.2/S24 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA2.2 output | 1 | 1 | 0 |
| | | S24 | X | X | 1 |

(1) X = Don't care

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### 6.14.4 Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

Figure 6-5 shows the port schematic. summarizes selection of the pin function.

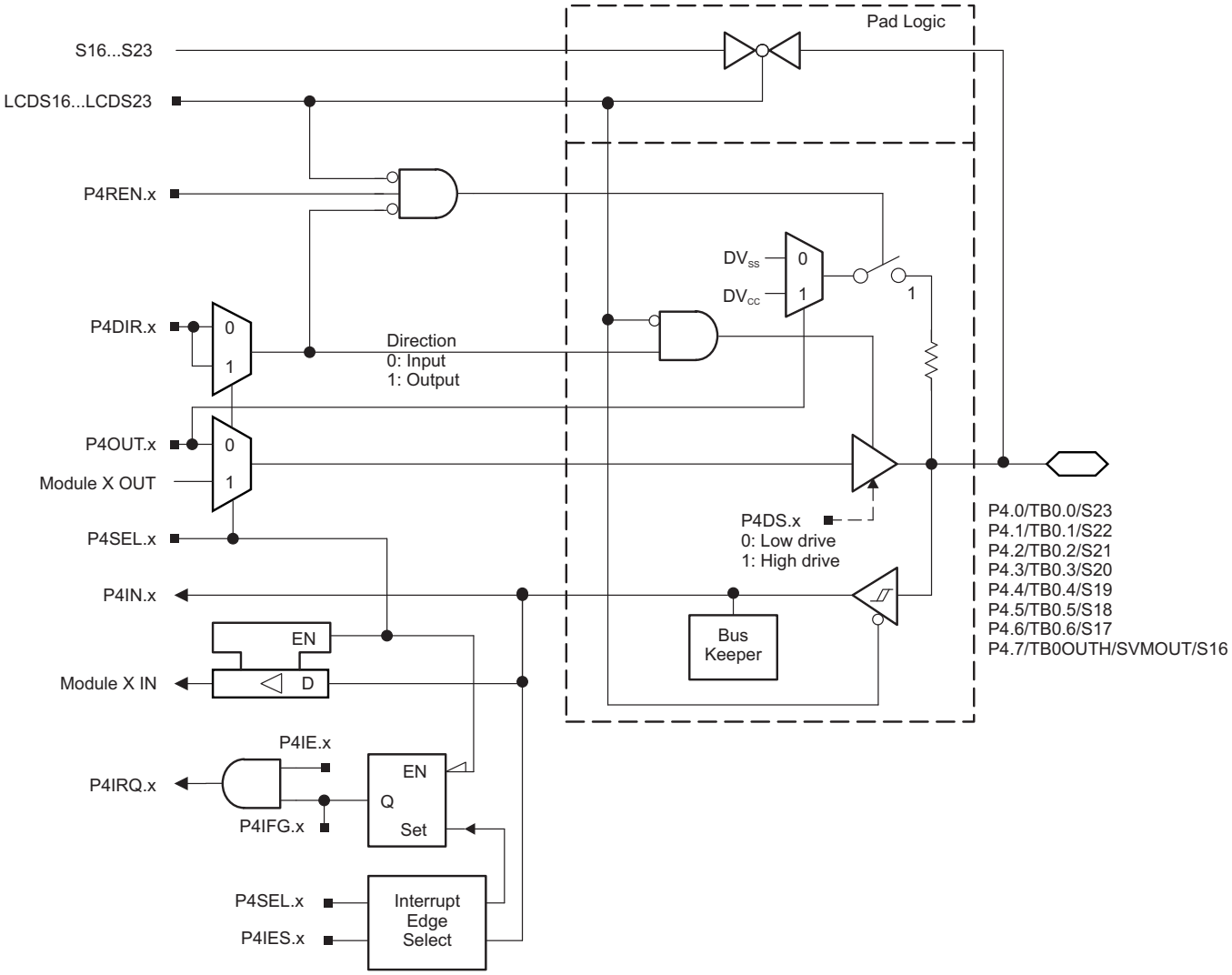


**Figure 6-5. Port P4 (P4.0 to P4.7) Schematic**


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**Port P4 (P4.0 to P4.7) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS16...23 |
| P4.0/TB0.0/S23 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TB0.0 output(2) | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P4.1/TB0.1/S22 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TB0.1 output(2) | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P4.2/TB0.2/S21 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TB0.2 output(2) | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P4.3/TB0.3/S20 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI3A capture input | 0 | 1 | 0 |
| | | Timer TB0.3 output(2) | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P4.4/TB0.4/S19 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI4A capture input | 0 | 1 | 0 |
| | | Timer TB0.4 output(2) | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P4.5/TB0.5/S18 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI5A capture input | 0 | 1 | 0 |
| | | Timer TB0.5 output(2) | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P4.6/TB0.6/S17 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI6A capture input | 0 | 1 | 0 |
| | | Timer TB0.6 output(2) | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P4.7/TB0OUTH/ SVMOUT/S16 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.TB0OUTH | 0 | 1 | 0 |
| | | SVMOUT | 1 | 1 | 0 |
| | | S16 | X | X | 1 |

(1) X = Don't care
(2) Setting TB0OUTH causes all Timer_B configured outputs to be set to high impedance.

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### 6.14.5 Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

Figure 6-6 shows the port schematic. summarizes selection of the pin function.

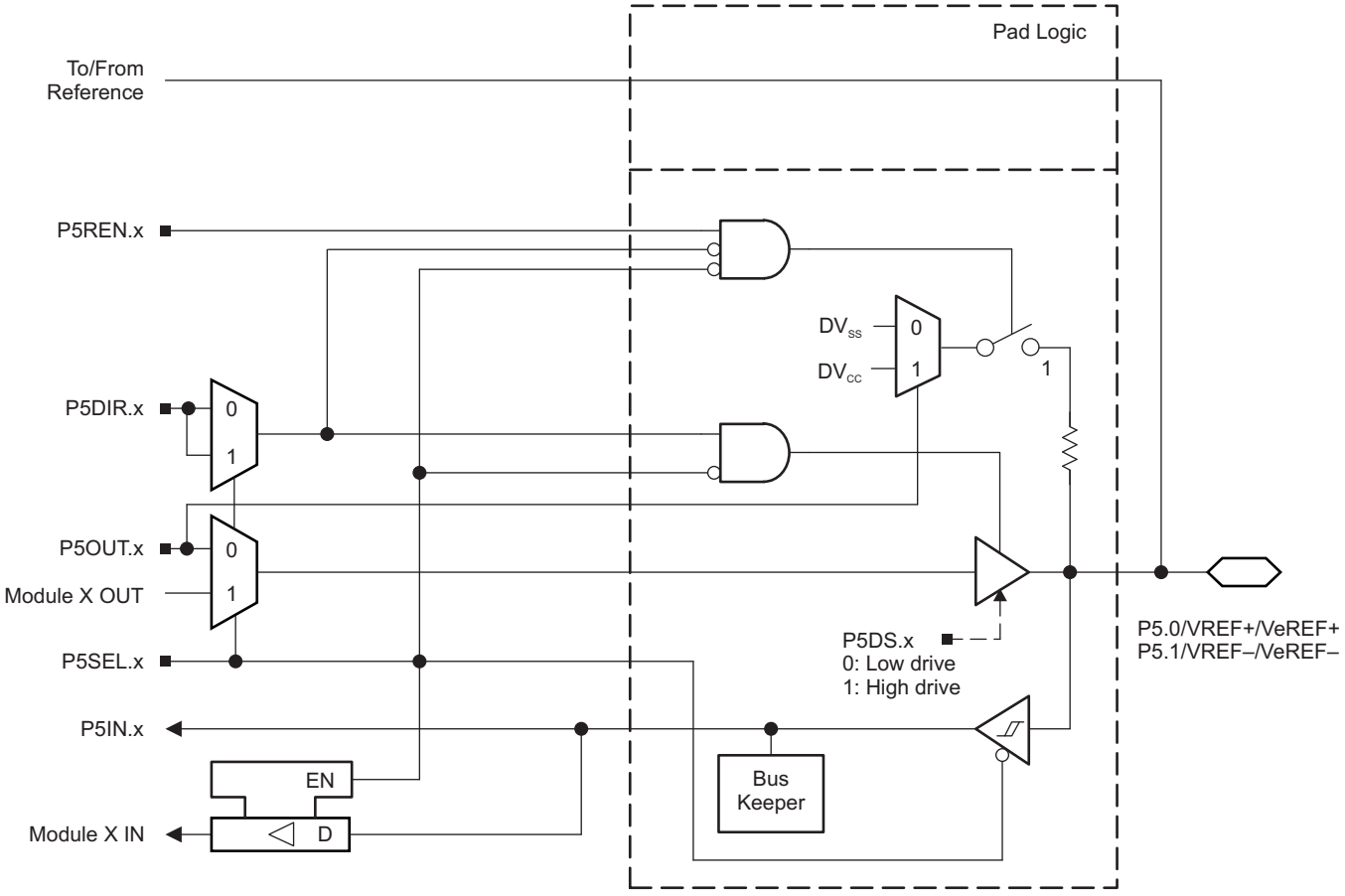


**Figure 6-6. Port P5 (P5.0 and P5.1) Schematic**

**Port P5 (P5.0 and P5.1) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x | REFOUT |
| P5.0/VREF+/VeREF+ | 0 | P5.0 (I/O)(2) | I: 0; O: 1 | 0 | X |
| | | VeREF+(3) | X | 1 | 0 |
| | | VREF+(4) | X | 1 | 1 |
| P5.1/VREF–/VeREF– | 1 | P5.1 (I/O)(2) | I: 0; O: 1 | 0 | X |
| | | VeREF–(5) | X | 1 | 0 |
| | | VREF–(6) | X | 1 | 1 |

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin.
(5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF– reference is available at the pin.


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### 6.14.6 Port P5, P5.2 to P5.7, Input/Output With Schmitt Trigger

Figure 6-7 shows the port schematic. summarizes selection of the pin function.

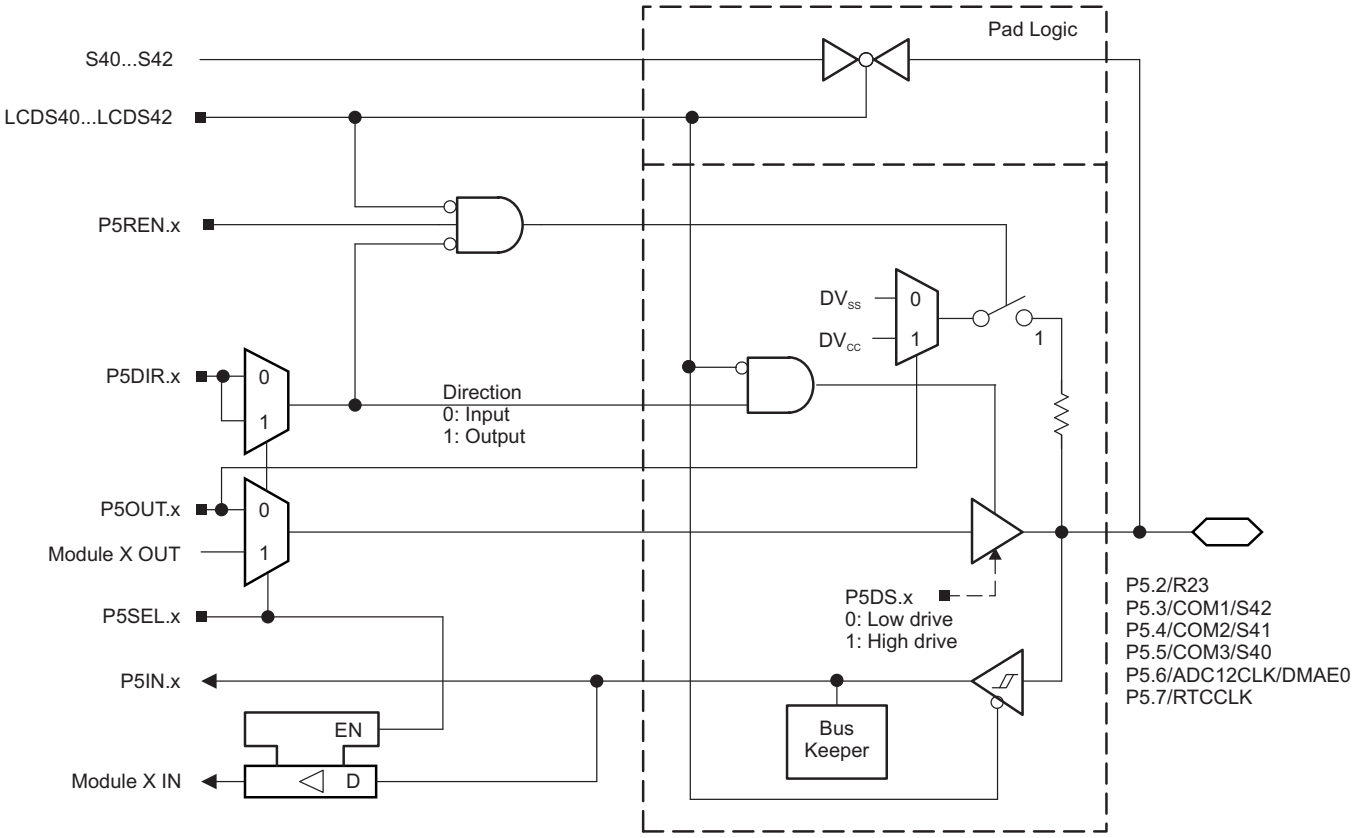


**Figure 6-7. Port P5 (P5.2 to P5.7) Schematic**

**Port P5 (P5.2 to P5.7) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x | LCDS40...42 |
| P5.2/R23 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | N/A |
| | | R23 | X | 1 | N/A |
| P5.3/COM1/S42 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM1 | X | 1 | X |
| | | S42 | X | 0 | 1 |
| P5.4/COM2/S41 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM2 | X | 1 | X |
| | | S41 | X | 0 | 1 |
| P5.5/COM3/S40 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM3 | X | 1 | X |
| | | S40 | X | 0 | 1 |
| P5.6/ADC12CLK/DMAE0 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | N/A |
| | | ADC12CLK | 1 | 1 | N/A |
| | | DMAE0 | 0 | 1 | N/A |
| P5.7/RTCCLK | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | N/A |
| | | RTCCLK | 1 | 1 | N/A |

(1) X = Don't care

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### 6.14.7 Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

Figure 6-8 shows the port schematic. summarizes selection of the pin function.

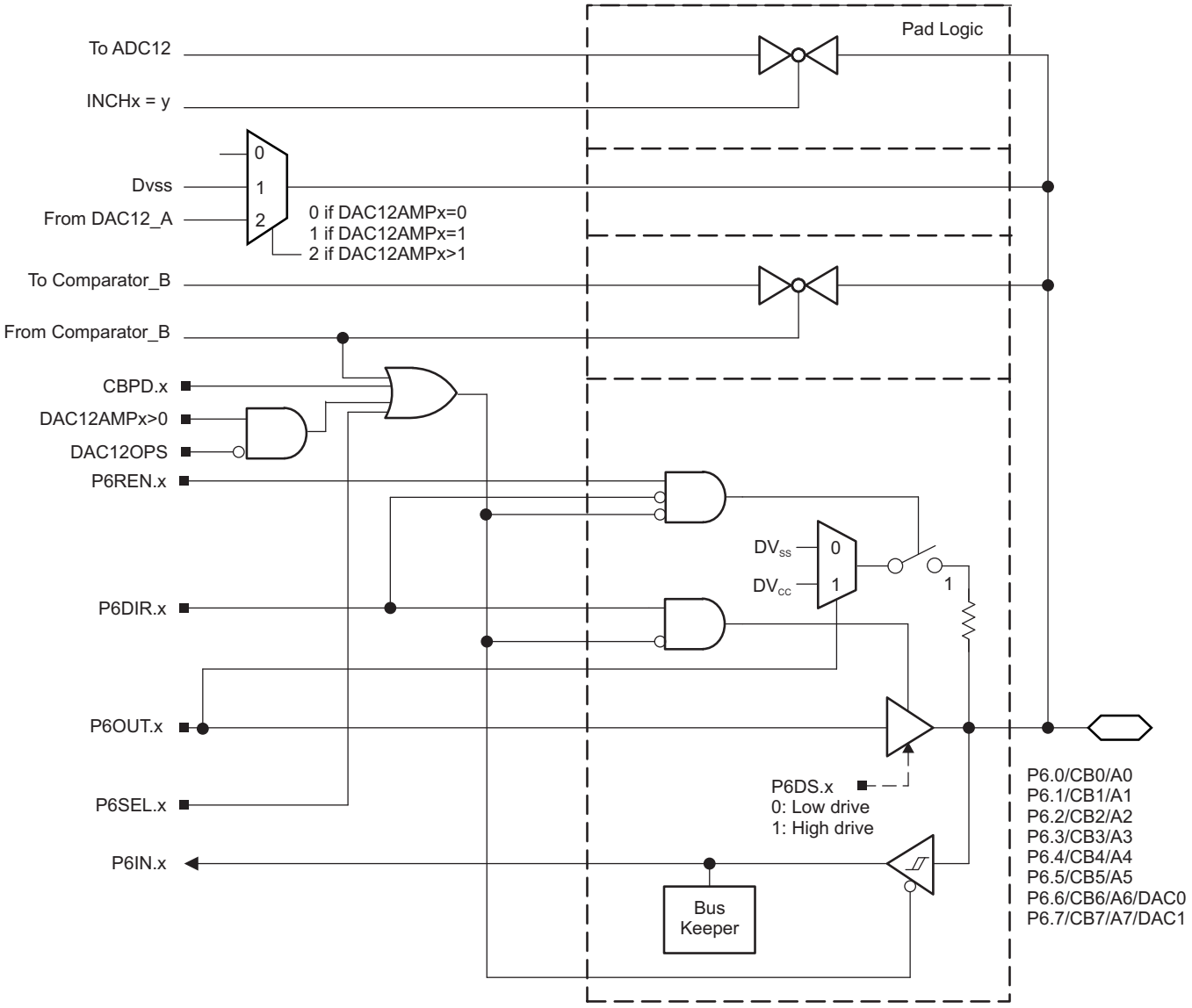


**Figure 6-8. Port P6 (P6.0 to P6.7) Schematic**


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**Port P6 (P6.0 to P6.7) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | | |
|---|---|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL.x | CBPD.x | DAC12OPS | DAC12AMPx |
| P6.0/CB0/A0 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB0 | X | X | 1 | N/A | N/A |
| | | A0(2)(3) | X | 1 | X | N/A | N/A |
| P6.1/CB1/A1 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB1 | X | X | 1 | N/A | N/A |
| | | A1(2)(3) | X | 1 | X | N/A | N/A |
| P6.2/CB2/A2 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB2 | X | X | 1 | N/A | N/A |
| | | A2(2)(3) | X | 1 | X | N/A | N/A |
| P6.3/CB3/A3 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB3 | X | X | 1 | N/A | N/A |
| | | A3(2)(3) | X | 1 | X | N/A | N/A |
| P6.4/CB4/A4 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB4 | X | X | 1 | N/A | N/A |
| | | A4(2)(3) | X | 1 | X | N/A | N/A |
| P6.5/CB5/A5 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | CB5 | X | X | 1 | N/A | N/A |
| | | A5(2)(3) | X | 1 | X | N/A | N/A |
| P6.6/CB6/A6/DAC0 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | CB6 | X | X | 1 | X | 0 |
| | | A6(2)(3) | X | 1 | X | X | 0 |
| | | DAC0 | X | X | X | 0 | >1 |
| P6.7/CB7/A7/DAC1 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | CB7 | X | X | 1 | X | 0 |
| | | A7(2)(3) | X | 1 | X | X | 0 |
| | | DAC1 | X | X | X | 0 | >1 |

(1) X = Don't care
(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to $AV_{SS}$ if not selected by the respective INCHx bits.

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### 6.14.8 Port P7, P7.2, Input/Output With Schmitt Trigger

Figure 6-9 shows the port schematic. summarizes selection of the pin function.

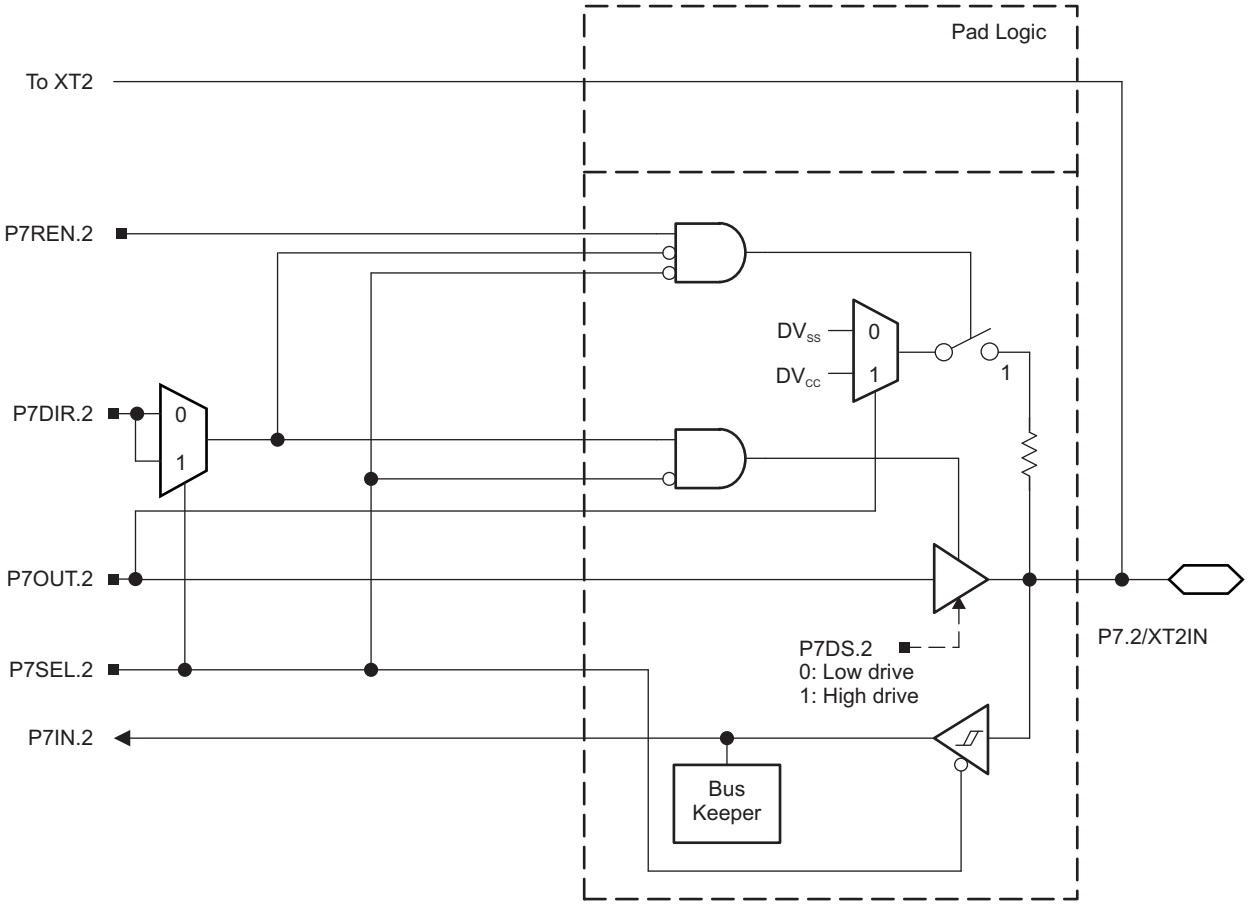


**Figure 6-9. Port P7 (P7.2) Schematic**


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### 6.14.9 Port P7, P7.3, Input/Output With Schmitt Trigger

Figure 6-10 shows the port schematic. summarizes selection of the pin function.

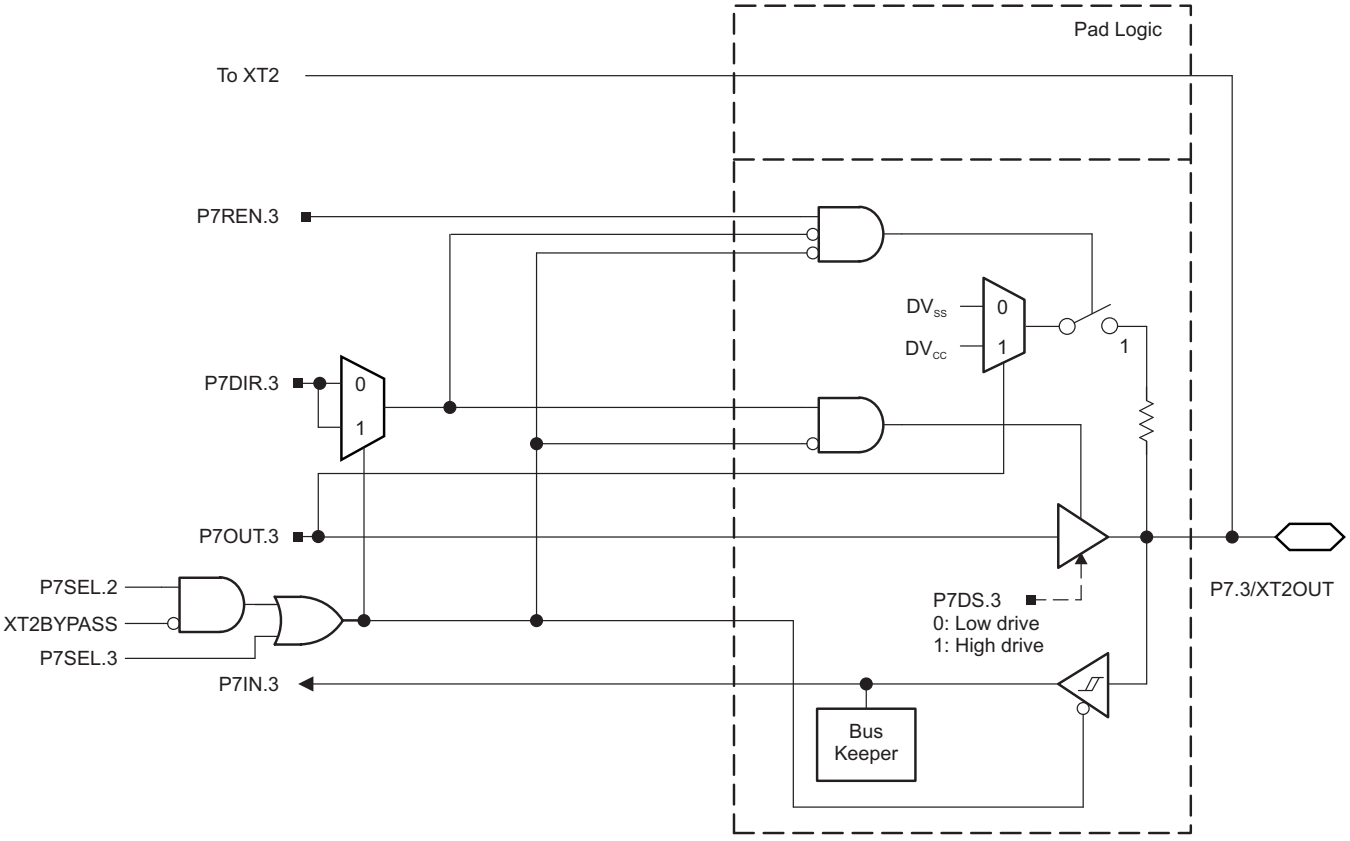


**Figure 6-10. Port P7 (P7.3) Schematic**

**Port P7 (P7.2 and P7.3) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.2 | P7SEL.3 | XT2BYPASS |
| P7.2/XT2IN | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2IN crystal mode(2) | X | 1 | X | 0 |
| | | XT2IN bypass mode(2) | X | 1 | X | 1 |
| P7.3/XT2OUT | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | XT2OUT crystal mode(3) | X | 1 | X | 0 |
| | | P7.3 (I/O)(3) | X | 1 | 0 | 1 |

(1) X = Don't care
(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.

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### 6.14.10 Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger

Figure 6-11 shows the port schematic. summarizes selection of the pin function.

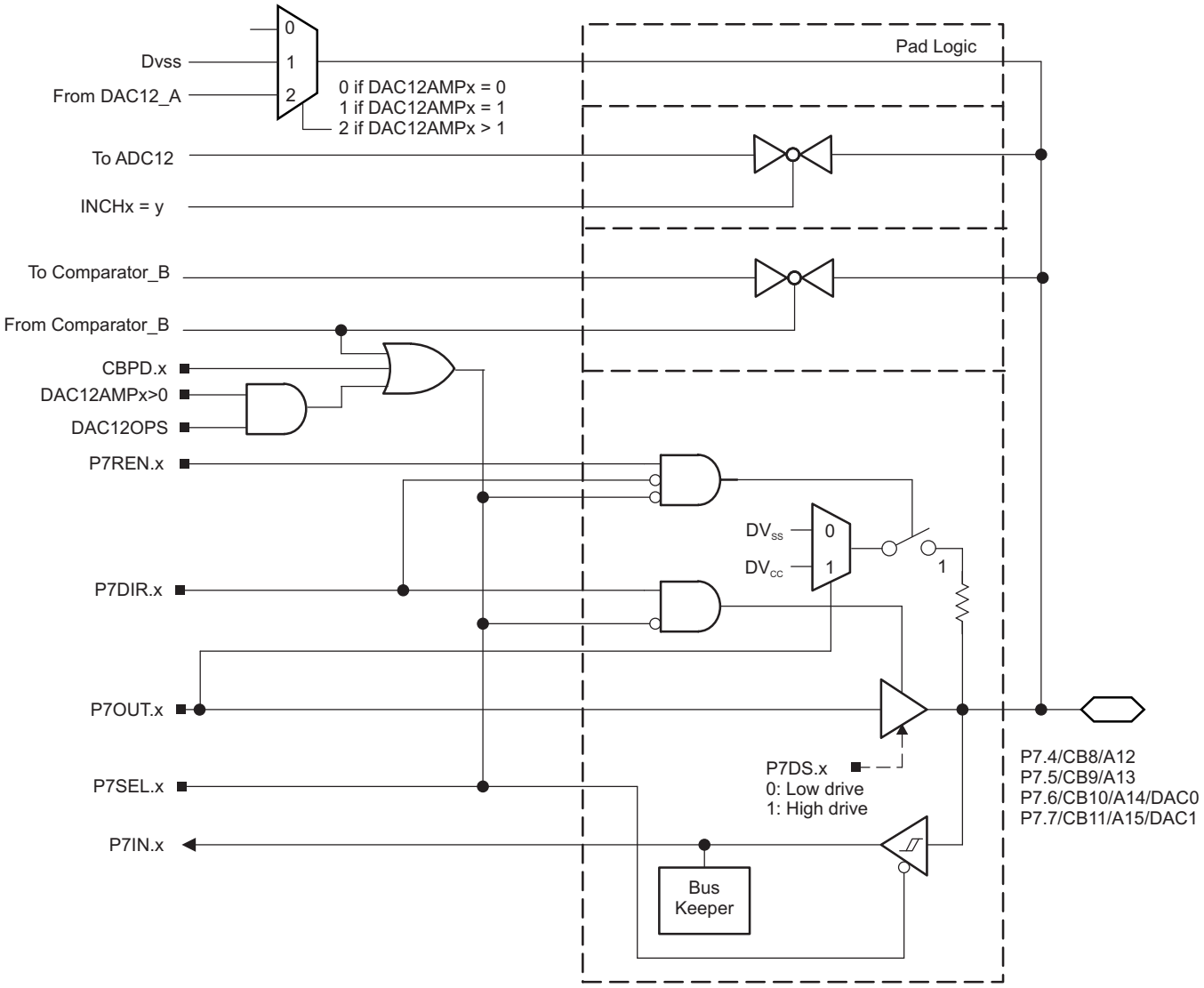


**Figure 6-11. Port P7 (P7.4 to P7.7) Schematic**


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**Port P7 (P7.4 to P7.7) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | | |
|---|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.x | CBPD.x | DAC12OPS | DAC12AMPx |
| P7.4/CB8/A12 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | Comparator_B input CB8 | X | X | 1 | N/A | N/A |
| | | A12(2)(3) | X | 1 | X | N/A | N/A |
| P7.5/CB9/A13 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 | N/A | N/A |
| | | Comparator_B input CB9 | X | X | 1 | N/A | N/A |
| | | A13(2)(3) | X | 1 | X | N/A | N/A |
| P7.6/CB10/A14/DAC0 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | Comparator_B input CB10 | X | X | 1 | X | 0 |
| | | A14(2)(3) | X | 1 | X | X | 0 |
| | | DAC12_A output DAC0 | X | X | X | 1 | >1 |
| P7.7/CB11/A15/DAC1 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | A15(2)(3) | X | 1 | X | X | 0 |
| | | DAC12_A output DAC1 | X | X | X | 1 | >1 |

(1) X = Don't care
(2) Setting the P7SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to $AV_{SS}$ if not selected by the respective INCHx bits.

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### 6.14.11 Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

Figure 6-12 shows the port schematic. summarizes selection of the pin function.

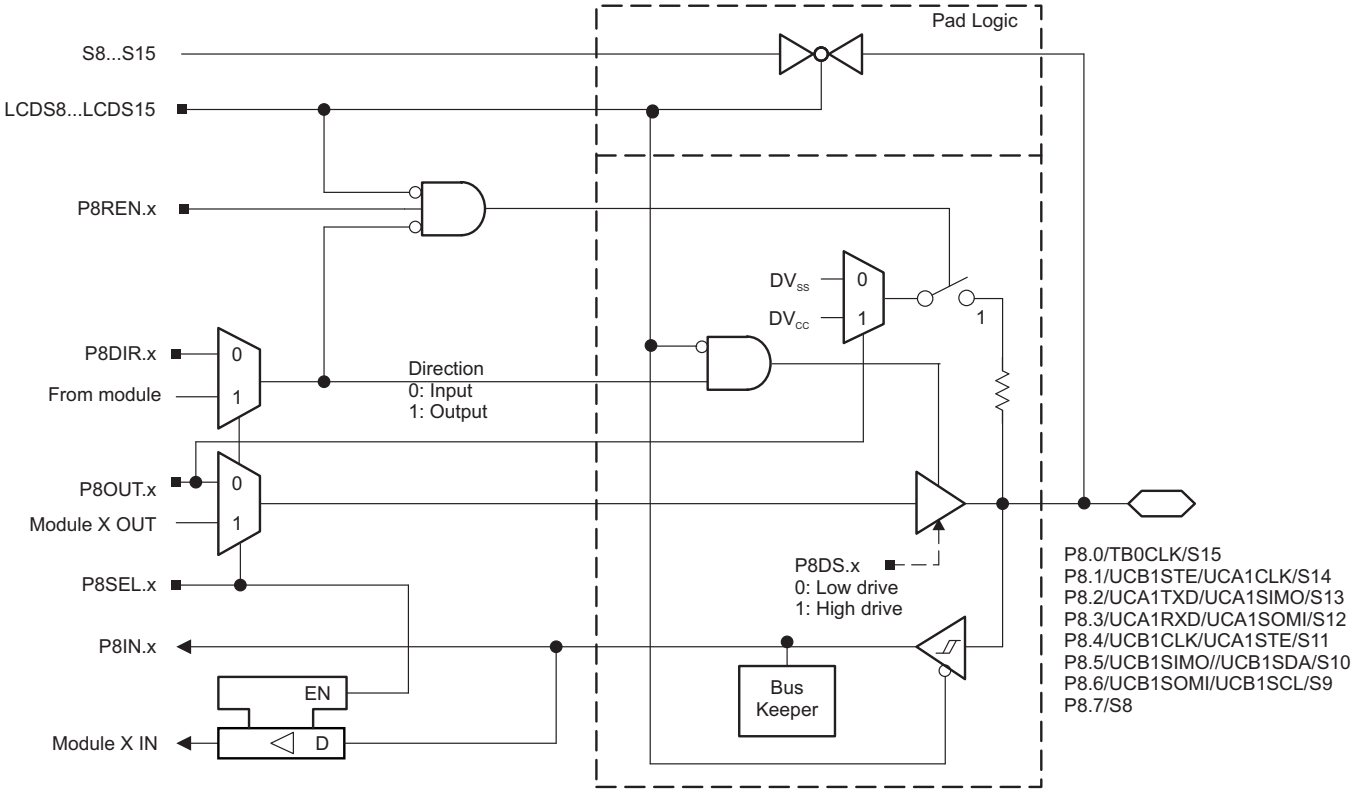


**Figure 6-12. Port P8 (P8.0 to P8.7) Schematic**


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**Port P8 (P8.0 to P8.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x | LCDS8...15 |
| P8.0/TB0CLK/S15 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.TB0CLK clock input | 0 | 1 | 0 |
| | | S15 | X | X | 1 |
| P8.1/UCB1STE/UCA1CLK/S14 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1STE/UCA1CLK | X | 1 | 0 |
| | | S14 | X | X | 1 |
| P8.2/UCA1TXD/UCA1SIMO/S13 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA1TXD/UCA1SIMO | X | 1 | 0 |
| | | S13 | X | X | 1 |
| P8.3/UCA1RXD/UCA1SOMI/S12 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA1RXD/UCA1SOMI | X | 1 | 0 |
| | | S12 | X | X | 1 |
| P8.4/UCB1CLK/UCA1STE/S11 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1CLK/UCA1STE | X | 1 | 0 |
| | | S11 | X | X | 1 |
| P8.5/UCB1SIMO/UCB1SDA/S10 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SIMO/UCB1SDA | X | 1 | 0 |
| | | S10 | X | X | 1 |
| P8.6/UCB1SOMI/UCB1SCL/S9 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SOMI/UCB1SCL | X | 1 | 0 |
| | | S9 | X | X | 1 |
| P8.7/S8 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S8 | X | X | 1 |

(1) X = Don't care

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### 6.14.12 Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger

Figure 6-13 shows the port schematic. summarizes selection of the pin function.

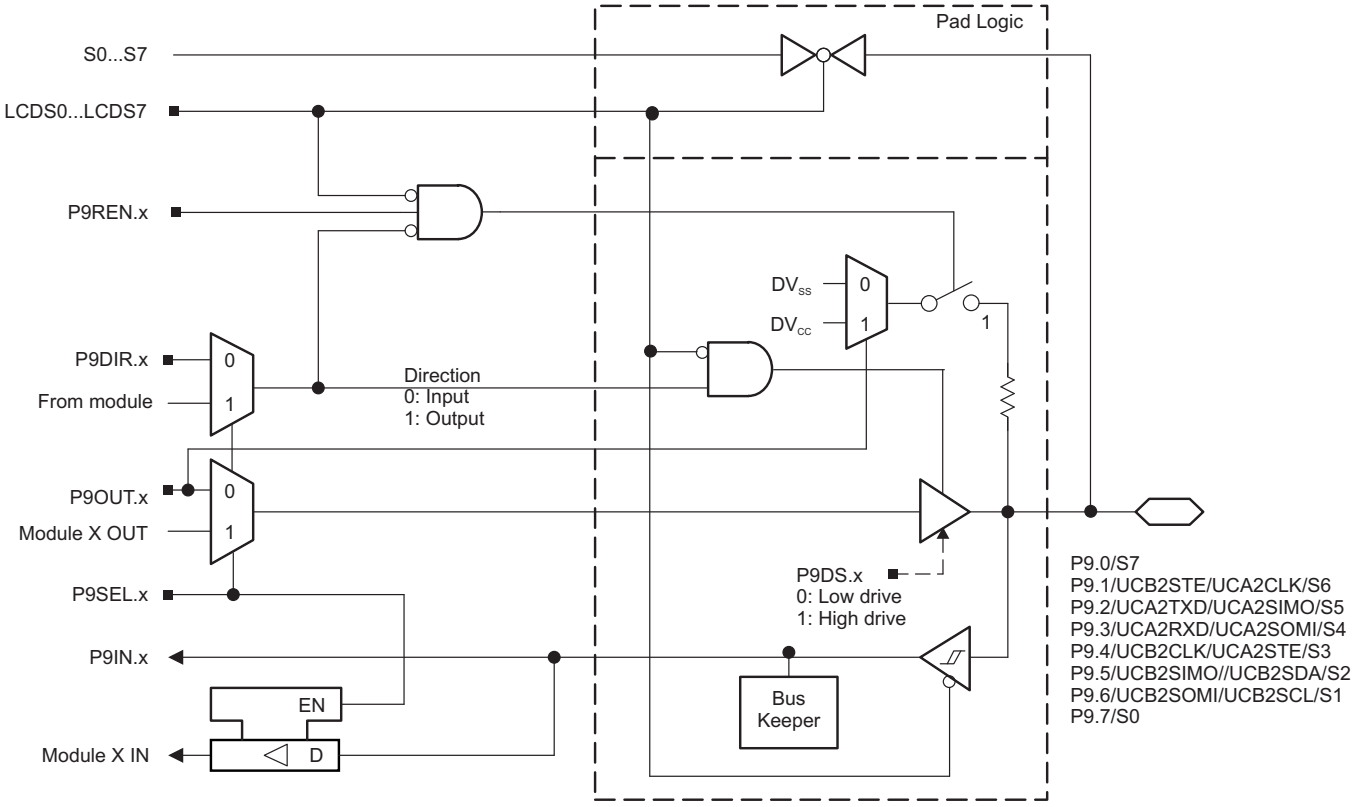


**Figure 6-13. Port P9 (P9.0 to P9.7) Schematic**


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**Port P9 (P9.0 to P9.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x | LCDS0...7 |
| P9.0/S7 | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S7 | X | X | 1 |
| P9.1/UCB2STE/UCA2CLK/S6 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB2STE/UCA2CLK | X | 1 | 0 |
| | | S6 | X | X | 1 |
| P9.2/UCA2TXD/UCA2SIMO/S5 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA2TXD/UCA2SIMO | X | 1 | 0 |
| | | S5 | X | X | 1 |
| P9.3/UCA2RXD/UCA2SOMI/S4 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA2RXD/UCA2SOMI | X | 1 | 0 |
| | | S4 | X | X | 1 |
| P9.4/UCB2CLK/UCA2STE/S3 | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB2CLK/UCA2STE | X | 1 | 0 |
| | | S3 | X | X | 1 |
| P9.5/UCB2SIMO/UCB2SDA/S2 | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB2SIMO/UCB2SDA | X | 1 | 0 |
| | | S2 | X | X | 1 |
| P9.6/UCB2SOMI/UCB2SCLK/S1 | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB2SOMI/UCB2SCLK | X | 1 | 0 |
| | | S1 | X | X | 1 |
| P9.7/S0 | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care

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### 6.14.13 Port PU.0, PU.1 Ports

Figure 6-14 shows the port schematic. Table 6-53 summarizes selection of the pin function.

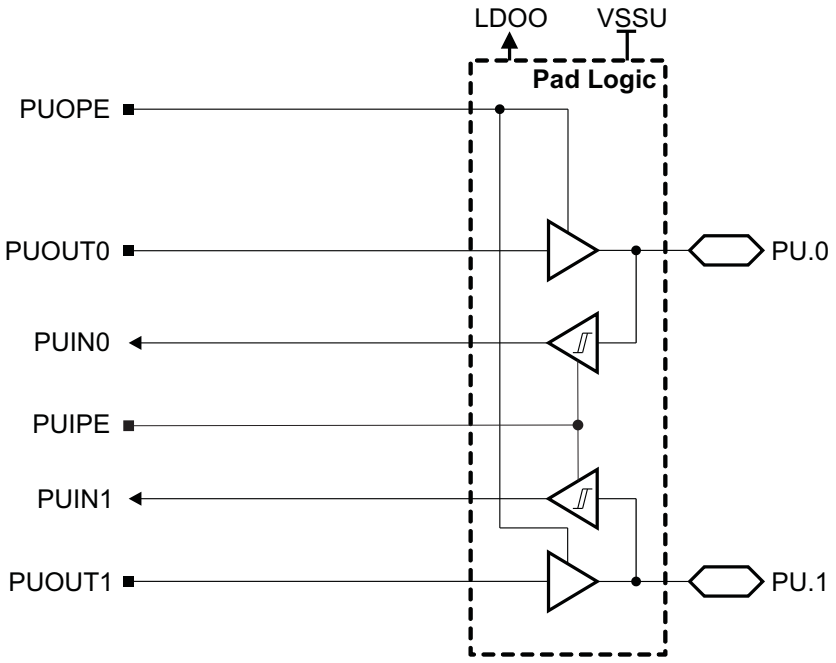


**Figure 6-14. Port U (PU.0 and PU.1) Schematic**

**Table 6-53. Port PU.0, PU.1 Functions(1)**

| PUIPE | PUOPE | PUOUT1 | PUOUT0 | PU.1 | PU.0 | PORT U FUNCTION |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Output low | Output low | Outputs enabled |
| 0 | 1 | 0 | 1 | Output low | Output high | Outputs enabled |
| 0 | 1 | 1 | 0 | Output high | Output low | Outputs enabled |
| 0 | 1 | 1 | 1 | Output high | Output high | Outputs enabled |
| 1 | 0 | X | X | Input enabled | Input enabled | Inputs enabled |
| 0 | 0 | X | X | Hi-Z | Hi-Z | Outputs and inputs disabled |

(1) PU.1 and PU.0 inputs and outputs are supplied from LDOO. LDOO can be generated by the device using the integrated 3.3-V LDO when enabled. LDOO can also be supplied externally when the 3.3-V LDO is not being used and is disabled.


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### 6.14.14 Port J, PJ.0 JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-15 shows the port schematic. summarizes selection of the pin function.

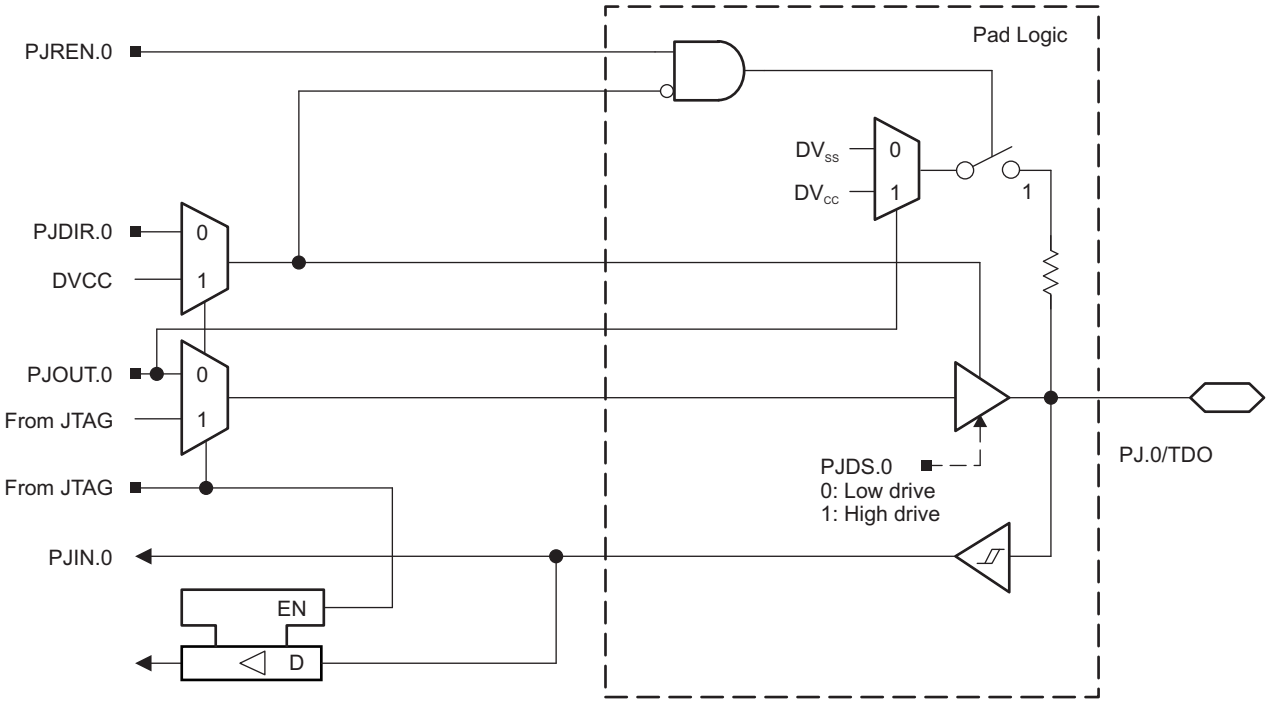


**Figure 6-15. Port PJ (PJ.0) Schematic**

### 6.14.15 Port J, PJ.1 to PJ.3 JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-16 shows the port schematic. summarizes selection of the pin function.

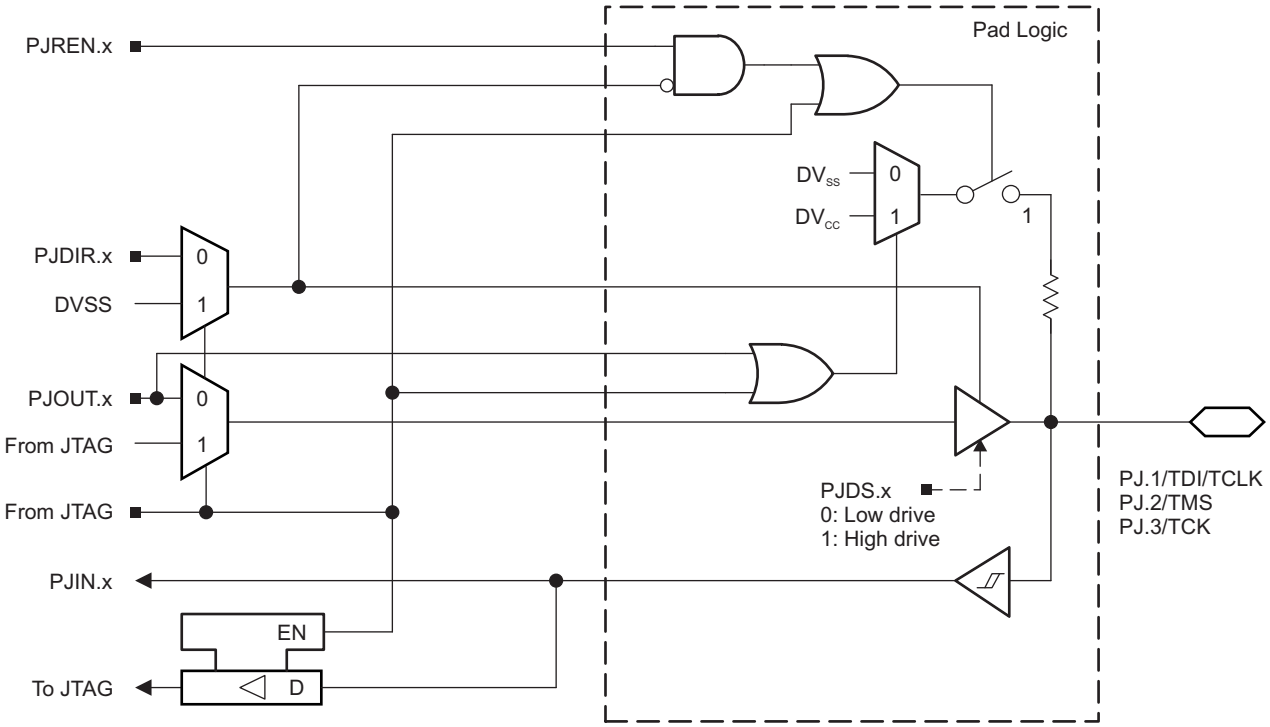


**Figure 6-16. Port PJ (PJ.1 to PJ.3) Schematic**

**Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) |
|---|---|---|---|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O)(2) | I: 0; O: 1 |
| | | TDO(3) | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O)(2) | I: 0; O: 1 |
| | | TDI/TCLK(3) (4) | X |
| PJ.2/TMS | 2 | PJ.2 (I/O)(2) | I: 0; O: 1 |
| | | TMS(3) (4) | X |
| PJ.3/TCK | 3 | PJ.3 (I/O)(2) | I: 0; O: 1 |
| | | TCK(3) (4) | X |

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.


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## 6.15 Device Descriptors

Table 6-54 lists the contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 6-54. Device Descriptor Table(1)**

| DESCRIPTION | | ADDRESS | SIZE (bytes) | VALUE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | F6659 | F6658 | F6459 | F6458 | F5659 | F5658 | F5359 | F5358 |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 2 | 812Bh | 812Ch | 812Dh | 812Eh | 8130h | 8131h | 8132h | 8133h |
| | Hardware revision | 01A06h | 1 | 10h | 10h | 10h | 10h | 10h | 10h | 10h | 10h |
| | Firmware revision | 01A07h | 1 | 10h | 10h | 10h | 10h | 10h | 10h | 10h | 10h |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| ADC12 Calibration | ADC12 calibration tag | 01A14h | 1 | 11h | 11h | 11h | 11h | 11h | 11h | 11h | 11h |
| | ADC12 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC offset | 01A18h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V reference temperature sensor 30°C | 01A1Ah | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V reference temperature sensor 105°C | 01A1Ch | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V reference temperature sensor 30°C | 01A1Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V reference temperature sensor 105°C | 01A20h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5-V reference temperature sensor 30°C | 01A22h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5-V reference temperature sensor 105°C | 01A24h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| REF Calibration | REF calibration tag | 01A26h | 1 | 12h | 12h | 12h | 12h | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 1 | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V reference factor | 01A28h | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V reference factor | 01A2Ah | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V reference factor | 01A2Ch | 2 | per unit | per unit | per unit | per unit | per unit | per unit | per unit | per unit |

(1) N/A = Not applicable

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# 7 Applications, Implementation, and Layout

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

### *7.1.1 Power Supply Decoupling and Bulk Capacitors*

TI recommends connecting a combination of a 1-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommend for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

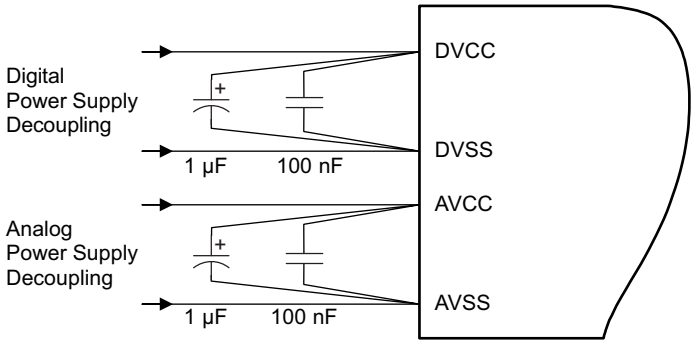


**Figure 7-1. Power Supply Decoupling**

### *7.1.2 External Oscillator*

Depending on the device variant (see Table 3-1), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

Figure 7-2 shows a typical connection diagram.


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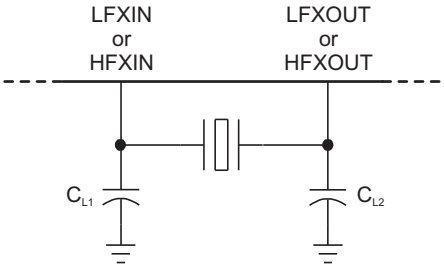


**Figure 7-2. Typical Crystal Connection**

See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide* (SLAU278).

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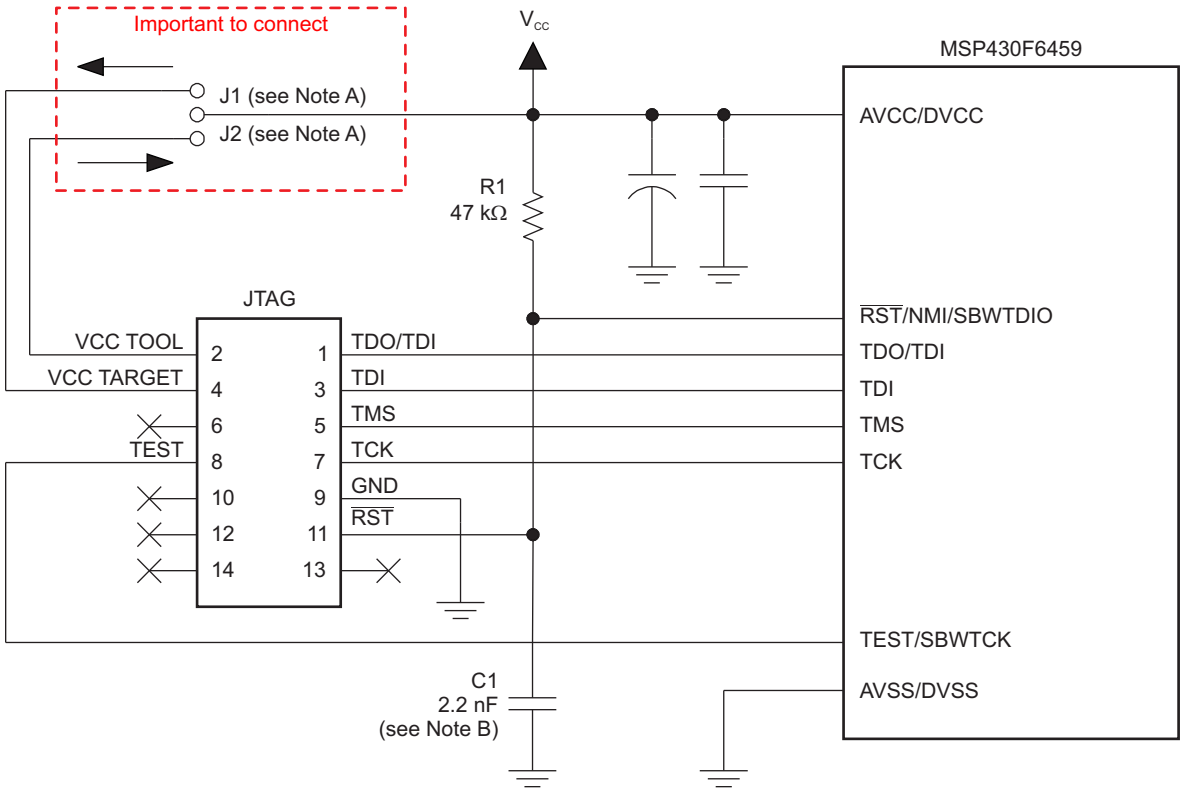


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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 2.2 nF when using current TI tools.

**Figure 7-3. Signal Connections for 4-Wire JTAG Communication**


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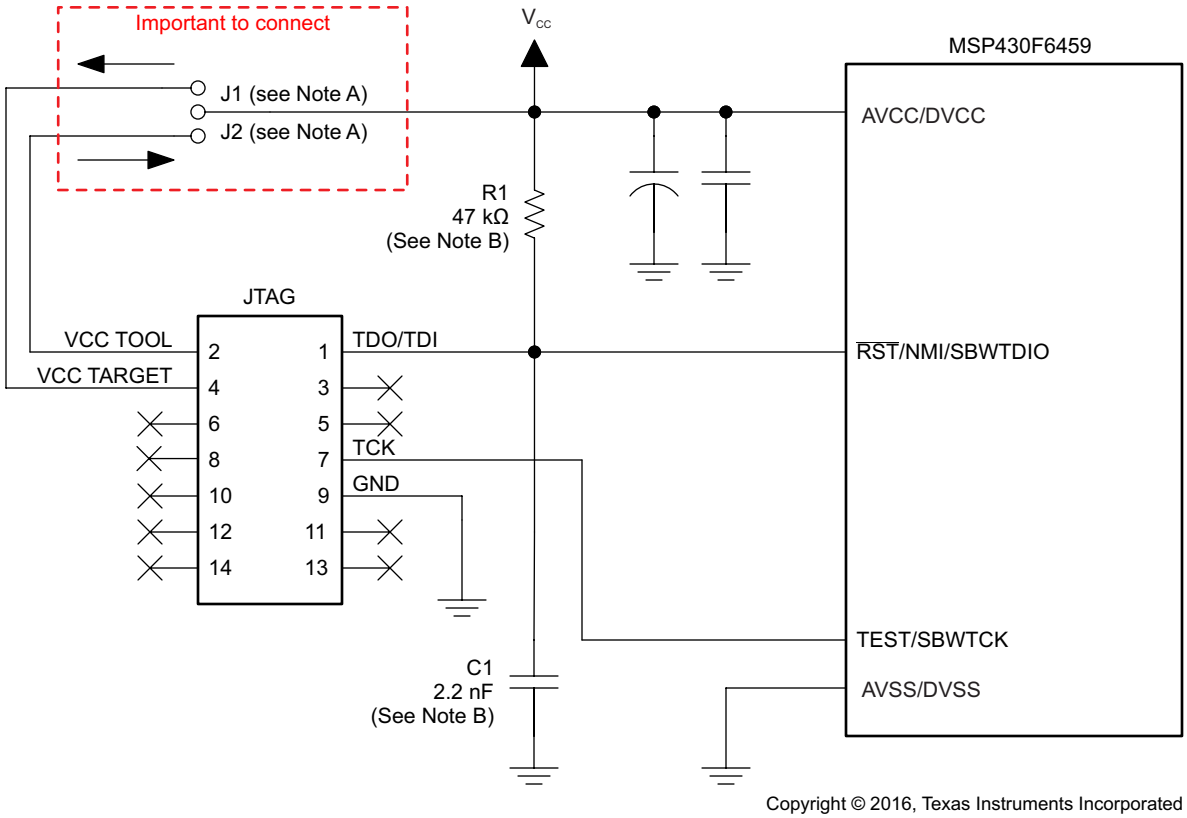


A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

**Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) for more information on the referenced control registers and bits.

### 7.1.5 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Refer to the *Circuit Board Layout Techniques* design guide (SLOA089) for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* (SLAA530) for guidelines.

### 7.1.6 Do's and Don'ts

TI recommends powering the AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC12_B Peripheral

#### 7.2.1.1 Partial Schematic

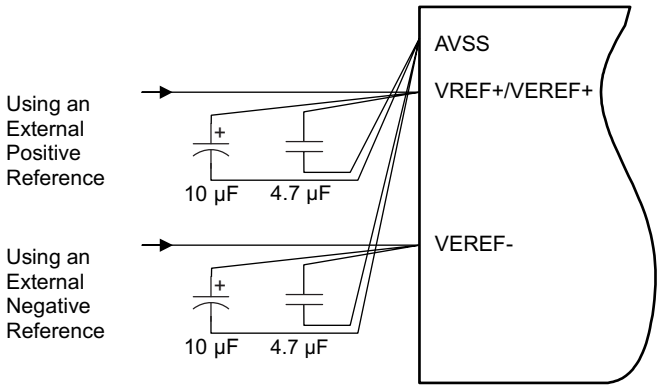


**Figure 7-5. ADC12_B Grounding and Noise Considerations**

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Section 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.


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Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the Reference module's $I_{O(VREF+)}$ specification.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A bypass capacitor of 4.7 µF is used to filter out any high frequency noise.

#### 7.2.1.3 Detailed Design Procedure

For additional design information, see the *ADC12_A* section in the application report *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

#### 7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

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# 8 デバイスおよびドキュメントのサポート

## 8.1 使い始めと次の手順

この MSP430™ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「Getting Started」ページを参照してください。

## 8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5438A). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

**XMS** – Experimental device that is not necessarily representative of the electrical specifications for the final device

**PMS** – Final silicon die that conforms to the electrical specifications for the device but has not completed quality and reliability verification

**MSP** – Fully qualified production device

Support tool development evolutionary flow:

**MSPX** – Development-support product that has not yet completed TI's internal qualification testing.

**MSP** – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). 図 8-1 provides a legend for reading the complete device name for any family member.


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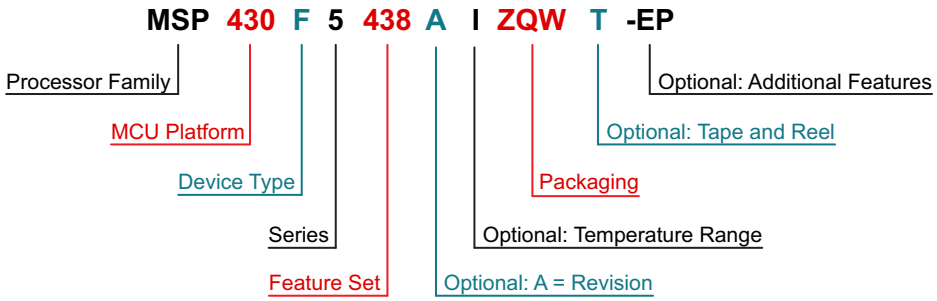


| | | |
|---|---|---|
| **Processor Family** | CC = Embedded RF Radio<br>MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device | |
| **MCU Platform** | 430 = MSP430 low-power microcontroller platform | |
| **Device Type** | **Memory Type**<br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash or FRAM (Value Line)<br>L = No Nonvolatile Memory | **Specialized Application**<br>AFE = Analog Front End<br>BT = Preprogrammed with *Bluetooth*<br>BQ = Contactless Power<br>CG = ROM Medical<br>FE = Flash Energy Meter<br>FG = Flash Medical<br>FW = Flash Electronic Flow Meter |
| **Series** | 1 Series = Up to 8 MHz<br>2 Series = Up to 16 MHz<br>3 Series = Legacy<br>4 Series = Up to 16 MHz with LCD | 5 Series = Up to 25 MHz<br>6 Series = Up to 25 MHz with LCD<br>0 = Low-Voltage Series |
| **Feature Set** | Various Levels of Integration Within a Series | |
| **Optional: A = Revision** | N/A | |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = –40°C to 85°C<br>T = –40°C to 105°C | |
| **Packaging** | http://www.ti.com/packaging | |
| **Optional: Tape and Reel** | T = Small Reel<br>R = Large Reel<br>No Markings = Tube or Tray | |
| **Optional: Additional Features** | -EP = Enhanced Product (–40°C to 105°C)<br>-HT = Extreme Temperature Parts (–55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified | |

**図 8-1. Device Nomenclature**

## 8.3 ツールとソフトウェア

すべての MSP430™マイクロコントローラは、広範なソフトウェアおよびハードウェア開発ツールによりサポートされています。ツールはTIおよびさまざまなサードパーティーから入手できます。www.ti.com/msp430toolsで、すべてのツールを参照できます。

### *8.3.1 ハードウェアの特長*

利用可能な特長の詳細については、*『MSP430用Code Composer Studio ユーザー・ガイド』*(SLAU157)を参照してください。

| MSP430アーキテクチャ | 4線式JTAG | 2線式JTAG | ブレーク・ポイント (N) | 範囲ブレーク・ポイント | クロック制御 | 状態シーケンサ | トレース・バッファ | LPMx.5デバッグ・サポート |
|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | ○ | ○ | 8 | ○ | ○ | ○ | ○ | ○ |

### 8.3.2 推奨ハードウェア・オプション

#### 8.3.2.1 ターゲット・ソケット基板

ターゲット・ソケット基板により、JTAGを使用してデバイスを簡単にプログラムおよびデバッグできます。これらの基板には、プロトタイプ作成用のヘッダー・ピン出力も用意されています。ターゲット・ソケット基板は個別にも、JTAGプログラマおよびデバッガが含まれているキットとしても注文できます。互換性のあるターゲット基板と、対応しているパッケージを、次の表に示します。

| パッケージ | ターゲット基板とプログラマのバンドル | ターゲット基板のみ |
|---|---|---|
| 100ピンLQFP (PZ) | MSP-FET430U100USB | MSP-TS430PZ100USB |

#### 8.3.2.2 検証用基板

一部のMSP430デバイス用に、検証用基板と評価キットが利用可能です。これらのキットには、完全なシステムの評価とプロトタイプ作成を行うため、追加のハードウェア・コンポーネントと接続が用意されています。詳細については、www.ti.com/msp430toolsを参照してください。

#### 8.3.2.3 デバッグおよびプログラミングのツール

ハードウェアのプログラミングおよびデバッグ用のツールは、TIおよびサードパーティーの供給元から入手できます。利用可能なツールすべてのリストは、www.ti.com/msp430toolsで参照できます。

#### 8.3.2.4 量産プログラマ

量産プログラマは、複数のデバイスを同時にプログラムし、ファームウェアをデバイスへ短時間でロードできます。

| 型番 | PCポート | 特長 | プロバイダ |
|---|---|---|---|
| MSP-GANG | シリアルおよびUSB | 8つまでのデバイスを同時にプログラムできます。PCからも使用でき、スタンドアロンのパッケージとしても使用できます。 | テキサス・インスツルメンツ |

### 8.3.3 推奨ソフトウェア・オプション

#### 8.3.3.1 統合開発環境

ソフトウェア開発ツールは、TIまたはサードパーティーから入手できます。オープン・ソースのソリューションも利用可能です。

このデバイスは、Code Composer Studio™ IDE (CCS)によりサポートされています。

#### 8.3.3.2 MSP430Ware

MSP430Wareは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430用設計リソースの完全なコレクションに加えて、MSP430WareにはMSP430ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430WareはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

#### 8.3.3.3 TI-RTOS

TI-RTOSは、MSP430マイクロコントローラ用の最先端のリアルタイム・オペレーティング・システムです。プリエンプティブな決定論的マルチタスク、ハードウェア抽象化、メモリ管理、およびリアルタイム分析機能があります。TI-RTOSは無償で利用でき、完全なソースコードが付属しています。

#### 8.3.3.4 コマンドライン・プログラマ

MSP430 Flasherは、MSP430マイクロコントローラをFETプログラマまたは eZ430™ 開発ツール経由で、JTAGまたはSpy-Bi-Wire (SBW)通信を使用してプログラムするための、オープン・ソースのシェル・ベース・インターフェイスです。MSP430 Flasherは、IDEを使用せずにバイナリ・ファイル(.txtまたは.hex)をMSP430 Flashへ直接ダウンロードするために使用できます。


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## 8.4 ドキュメントのサポート

ドキュメントの更新についての通知を受け取るには、ti.com (**GPN1**、**GPN2**、...)のデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

以下のドキュメントでは、MSP430F665x、MSP430F645x、MSP430F565x、MSP430F535xデバイスについて記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

**SLAZ491** *『MSP430F6459-Hirelデバイス正誤表』*このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

**SLAU278** *『MSP430ハードウェア・ツール・ユーザー・ガイド』* このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。FETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

**SLAU319** *『MSP430ブートローダ(BSL)によるプログラミング』* MSP430ブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430マイクロコントローラの組み込みメモリと通信を行うことができます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。このブートローダは、一部のデジタル・シグナル・プロセッサ(DSP)に見られる、外部メモリからDSPの内部メモリへプログラム・コード(およびデータ)を自動的にロードする、ブートストラップ・ローダ・プログラムとは異なることに注意してください。

**SLAU320** *『JTAGインターフェイスによるMSP430のプログラミング』*このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430 MCUで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してMCUにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

**SLAA322** *『MSP430 32kHz水晶発振器』* 適切な水晶、正しい負荷電流、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

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**SLOA089** *『基板のレイアウト技法』* オペアンプの回路はアナログ回路で、デジタル回路とは大きく異なります。特別なレイアウト技法を使用して、基板上で専用のセクションに分離する必要があります。プリント基板の影響は高速なアナログ回路でより明白になりますが、この章に示す一般的な誤りは、オーディオ回路の性能にも影響を及ぼします。この章の目的は、設計者が犯す最も一般的な過ちのいくつかについて解説し、それらがどのように性能の劣化を引き起こすかについて説明し、問題を回避するための簡単な修正方法を提示することです。

**SLAA530** *『MSP430 システム・レベルESDの考慮事項』* シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

## 8.5 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
*TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.7 商標

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## 8.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 8.9 Export Control Notice

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## 8.10 用語集

**TI** 用語集　この用語集には、用語や略語の一覧および定義が記載されています。


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# 9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430F6459TPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | F6459TPZ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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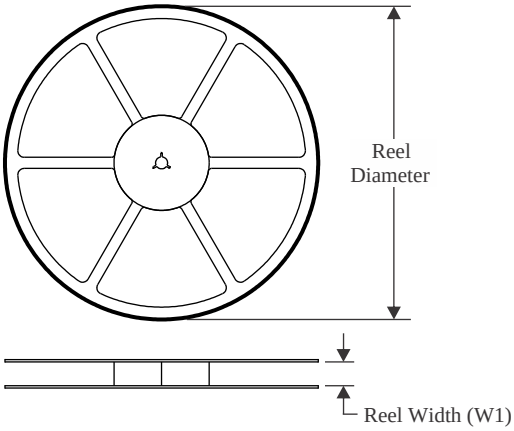
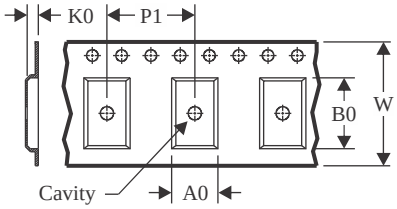
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

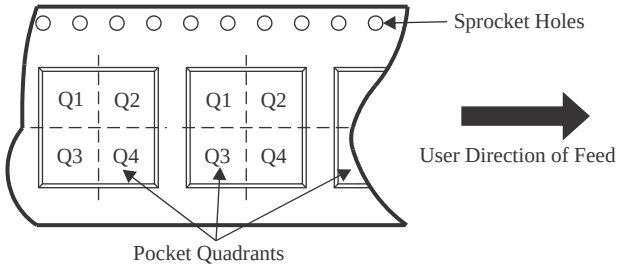



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

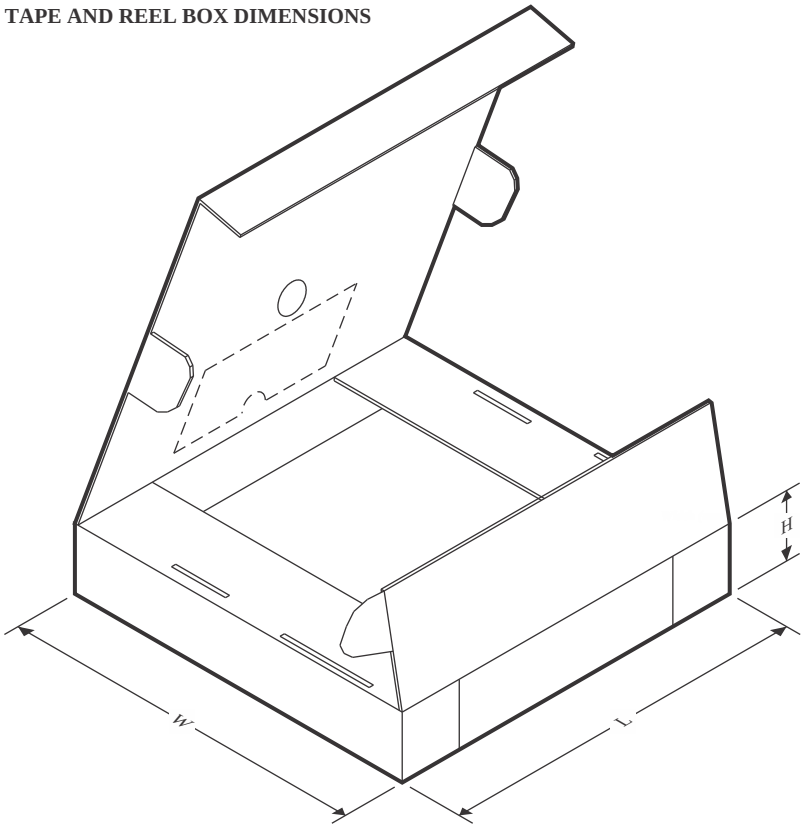
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6459TPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

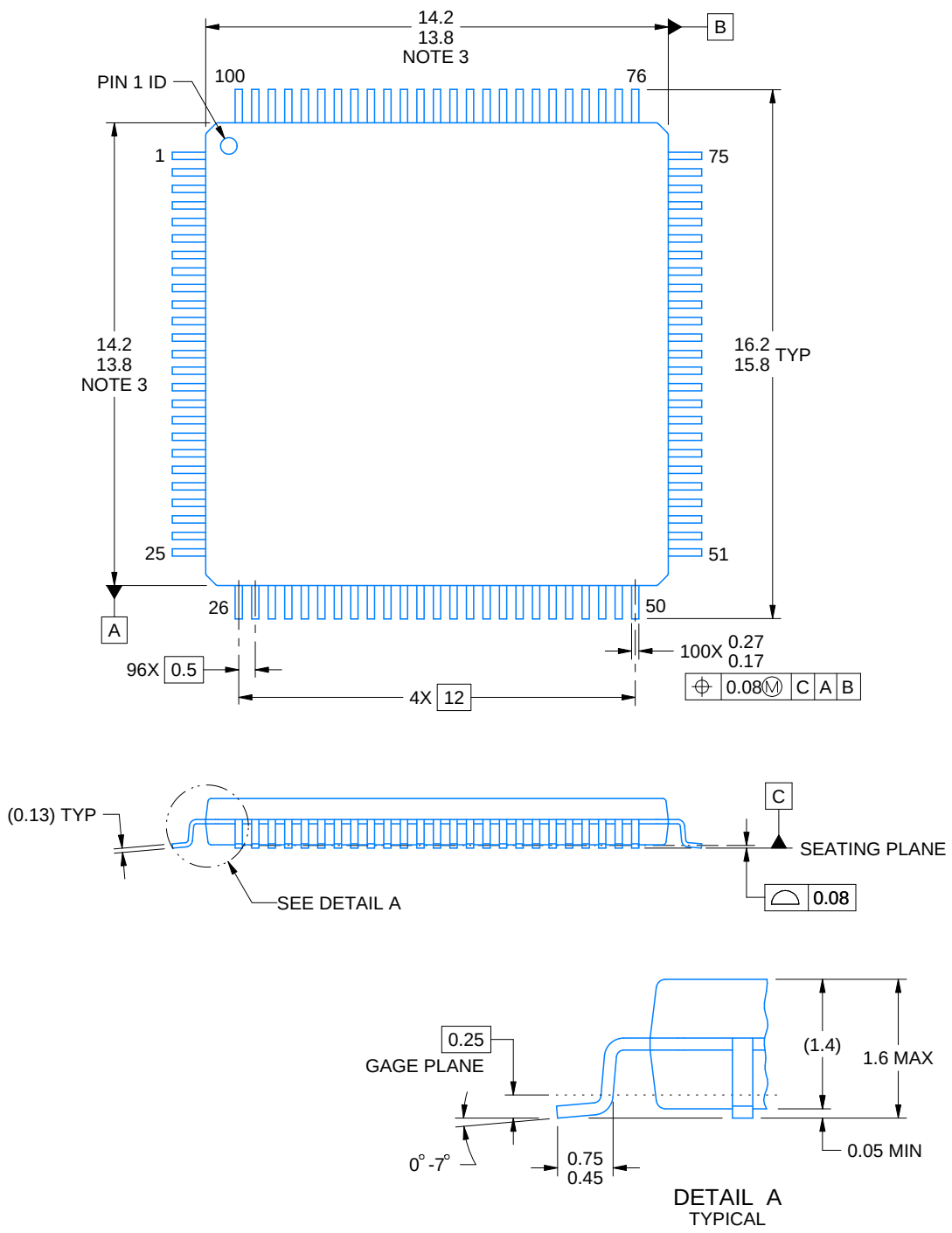
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430F6459TPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

# PACKAGE OUTLINE

## PZ0100A

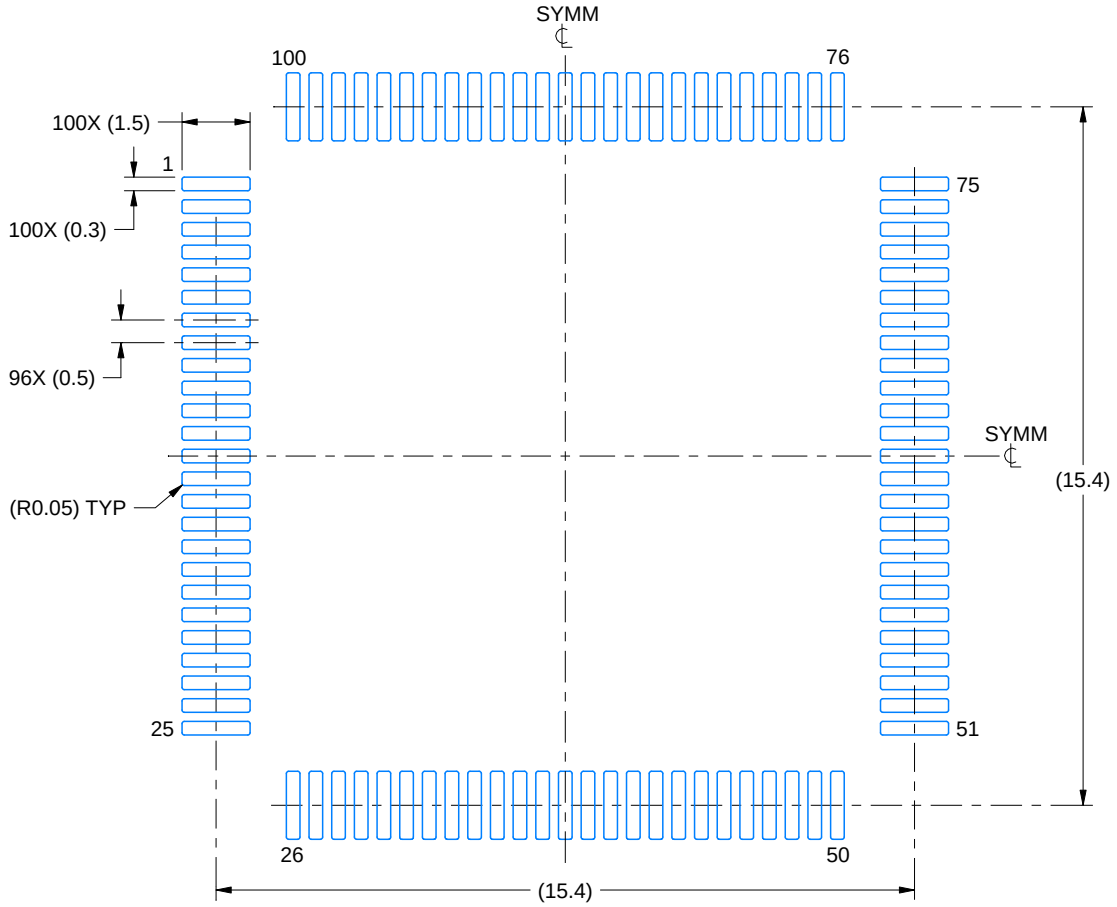
## LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

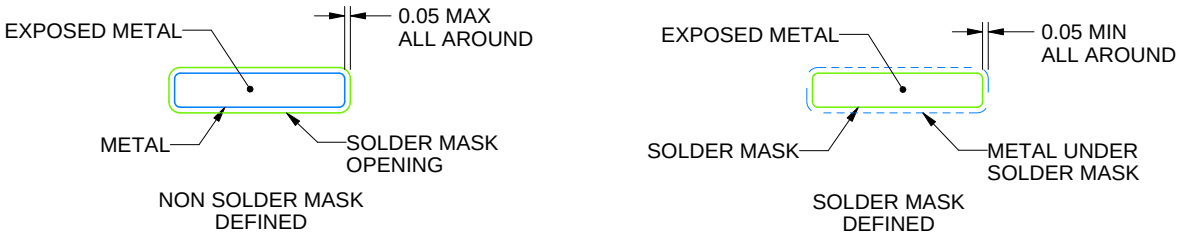



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

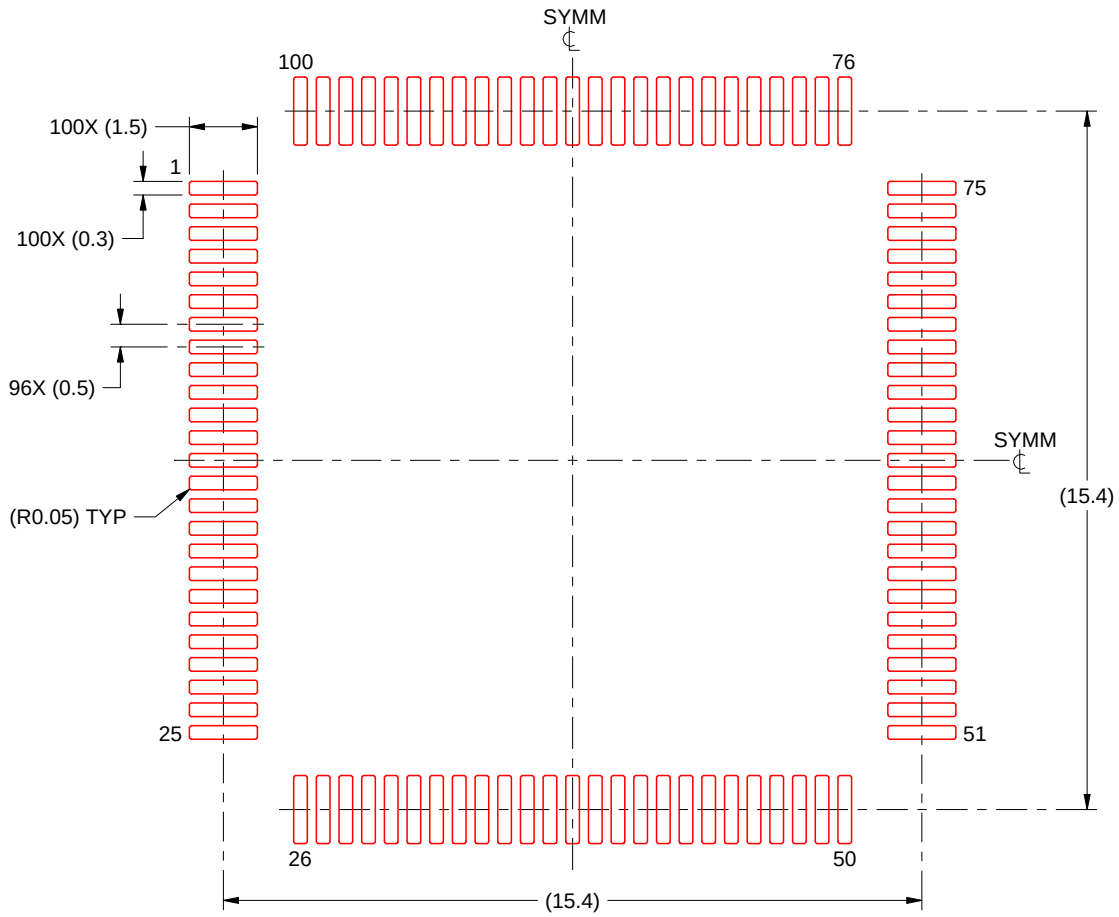



SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

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最終更新日：2025 年 10 月