TEXAS INSTRUMENTS

MSP430F427, MSP430F425, MSP430F423
JAJS274B –APRIL 2004–REVISED NOVEMBER 2016

MSP430F42x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 低い電源電圧範囲: 1.8V～3.6V
- 超低消費電力
  - アクティブ・モード: 400µA (1MHz、3V)
  - スタンバイ・モード: 1.6µA
  - オフ・モード(RAMデータ保持): 0.1µA
- 5つの省電力モード
- スタンバイ・モードからのウェークアップは6µs以下
- 周波数ロック・ループ、FLL+
- 16ビットRISCアーキテクチャ、125nsインストラクション・サイクル・タイム
- 3つの独立した16ビット・シグマ・デルタA/Dコンバータ(差動PGA入力付き)
- 16ビット・タイマ_A (3つのキャプチャ/コンペア・レジスタ付き)
- 128セグメント用のLCDドライバを搭載
- シリアル・コミュニケーション・インターフェイス(USART)、非同期UART、同期SPIインターフェイスの中からソフトウェアで選択
- ブラウン・アウト検出
- プログラム可能なレベル検出による電源電圧監視/モニタ
- シリアル・オンボード・プログラミング、外部プログラミング電圧不要、セキュリティ・ヒューズによるプログラム可能なコード保護
- ブートストラップ・ローダ(BSL)
- 製品ファミリ:
  - MSP430F423
    8KB + 256B フラッシュ・メモリ、256B RAM
  - MSP430F425
    16KB + 256B フラッシュ・メモリ、512B RAM
  - MSP430F427
    32KB + 256B フラッシュ・メモリ、1KB RAM
- 64ピン・クワッド・フラットパック(LQFP)で供給
- モジュールの詳細は、*『MSP430x4xxファミリ ユーザーズ・ガイド』*を参照してください。

1.2 アプリケーション

- ハンドヘルド計量器
- 重量計
- エネルギー・メーター

1.3 概要

TI MSP430™ファミリの超低消費電力マイクロコントローラは、各種アプリケーションを対象とした、異なるペリフェラルを組み合わせた複数デバイスで構成されています。このアーキテクチャは5つの低消費電力モードを持ち、携帯用測定器用途でバッテリ駆動時間を延長するよう最適化されています。このデバイスには、強力な16ビットRISC CPU、16ビット・レジスタ、およびコンスタント・ジェネレータが搭載されており、コード効率が最大限に発揮されます。デジタル制御発振器(DCO)により、デバイスは低消費電力モードからアクティブ・モードへ、6µs以内にウェークアップできます。

MSP430F42xシリーズは、3つの独立した16ビット・シグマ・デルタA/Dコンバータを搭載したマイクロコントローラで、それぞれのA/Dコンバータはプログラム可能な差動ゲイン増幅入力機能を備えます。内蔵の16ビット・タイマ、128セグメントのLCDドライバ機能、ハードウェア・マルチプライヤ、14本のI/O端子も備えています。

標準的なアプリケーションには、ハンドヘルド計量器、重量計、電力量計などの高分解能アプリケーションがあります。

English Data Sheet: SLAS421

製品情報[(1)]

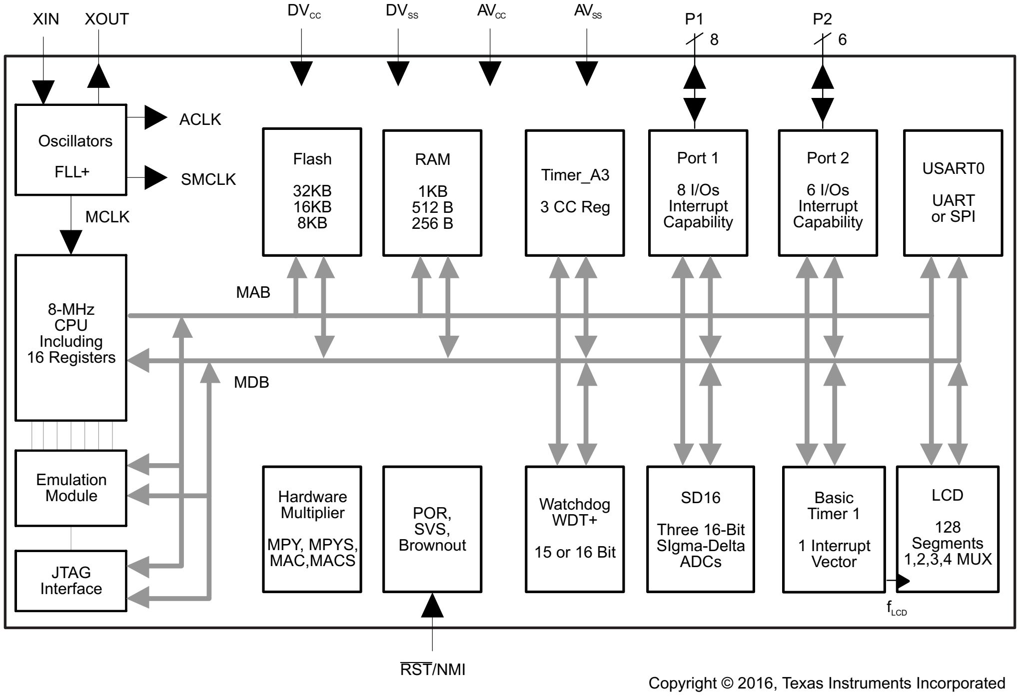
型番	パッケージ	本体サイズ[(2)]
MSP430F427IPM	LQFP (64)	10mm × 10mm
MSP430F425IPM	LQFP (64)	10mm × 10mm
MSP430F423IPM	LQFP (64)	10mm × 10mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については 8の「付録：パッケージ・オプション」またはwww.ti.comのTI Webサイトを参照してください。

(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、8の「メカニカル・データ」を参照してください。

1.4 機能ブロック図

機能ブロック図を、図 1-1に示します。



Copyright © 2016, Texas Instruments Incorporated

図 1-1. MSP430F42xのブロック図

Table of Contents

1 デバイスの概要 1
- 1.1 特長 1
- 1.2 アプリケーション 1
- 1.3 概要 1
- 1.4 機能ブロック図 2

2 改訂履歴 4

3 **Device Comparison** 5
- 3.1 Related Products 5

4 **Terminal Configuration and Functions** 6
- 4.1 Pin Diagram 6
- 4.2 Signal Descriptions 7

5 **Specifications** 10
- 5.1 Absolute Maximum Ratings 10
- 5.2 ESD Ratings 10
- 5.3 Recommended Operating Conditions 10
- 5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current 11
- 5.5 Thermal Resistance Characteristics, PM Package (LQFP64) 12
- 5.6 Schmitt-Trigger Inputs − Ports (P1 and P2), RST/NMI, JTAG (TCK, TMS, TDI/TCLK,TDO/TDI) 12
- 5.7 Inputs P1.x, P2.x, TAx 12
- 5.8 Leakage Current − Ports (P1 and P2) 12
- 5.9 Outputs − Ports (P1 and P2) 13
- 5.10 Output Frequency 13
- 5.11 Typical Characteristics – Ports P1 and P2 14
- 5.12 Wake-up Time From LPM3 15
- 5.13 RAM 15
- 5.14 LCD 15
- 5.15 USART0 15
- 5.16 POR, BOR 16
- 5.17 SVS (Supply Voltage Supervisor and Monitor) 17
- 5.18 DCO 19
- 5.19 Crystal Oscillator, LFXT1 Oscillator 21
- 5.20 SD16 Power Supply and Operating Characteristics 22
- 5.21 SD16 Analog Input Range 22
- 5.22 SD16 Analog Performance 23
- 5.23 SD16 Built-in Temperature Sensor 23
- 5.24 SD16 Built-in Voltage Reference 24
- 5.25 SD16 Built-in Reference Output Buffer 24
- 5.26 SD16 External Reference Input 24
- 5.27 Flash Memory 25
- 5.28 JTAG Interface 25
- 5.29 JTAG Fuse 25

6 **Detailed Description** 26
- 6.1 CPU 26
- 6.2 Instruction Set 27
- 6.3 Operating Modes 28
- 6.4 Interrupt Vector Addresses 29
- 6.5 Special Function Registers 30
- 6.6 Memory Organization 32
- 6.7 Bootloader (BSL) 32
- 6.8 Flash Memory 32
- 6.9 Peripherals 33
- 6.10 Input/Output Diagrams 39

7 デバイスおよびドキュメントのサポート 46
- 7.1 使い始めと次の手順 46
- 7.2 デバイスの項目表記 46
- 7.3 ツールとソフトウェア 48
- 7.4 ドキュメントのサポート 49
- 7.5 関連リンク 51
- 7.6 Community Resources 51
- 7.7 商標 51
- 7.8 静電気放電に関する注意事項 51
- 7.9 Export Control Notice 51
- 7.10 用語集 51

8 メカニカル、パッケージ、および注文情報 52

2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2007年6月2日発行分から2016年11月14日発行分への変更	Page

- ドキュメント全体を通してフォーマットと編成を変更、セクション番号の追加も含む 1
- Added Section 3 5
- Added Section 5 and moved all electrical and timing specifications to it 10
- Added Section 5.2, *ESD Ratings* 10
- Changed the MAX value of the $I_{(LPM3)}$ parameter at 85°C from 2.6 to 3.5 µA in Section 5.4, *Supply Current Into* AV_{CC} *and* DV_{CC} *Excluding External Current* 11
- Added Section 5.5, *Thermal Resistance Characteristics, PM Package (LQFP-64)* 12
- Changed all cases of "bootstrap loader" to "bootloader" 32
- Changed all instances of Port/LCD to $\overline{\text{Port}}$/LCD (added overline) 40
- Changed the value of the $\overline{\text{Port}}$/LCD column in Table 6-14, *Port P1 (P1.2 to P1.7) Pin Functions* 40
- Changed the value of the $\overline{\text{Port}}$/LCD column in Table 6-15, *Port P2 (P2.0 and P2.1) Pin Functions* 41
- 7「デバイスおよびドキュメントのサポート」を追加 46
- 8「メカニカル、パッケージ、および注文情報」を追加 52

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	FLASH (KB)	RAM (B)	FREQUENCY (MHz)	BSL	SD16 (CHANNELS)	I/Os	PACKAGE
MSP430F427	32	1K	8	UART	3	14	PM 64
MSP430F425	16	512	8	UART	3	14	PM 64
MSP430F423	8	256	8	UART	3	14	PM 64

(1) For the most current package and ordering information, see the *Package Option Addendum* in 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI Microcontrollers Product Selection TI's low-power and-high performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Products for MSP430F2x/4x Ultra-Low-Power Microcontrollers MSP430F2x/4x microcontrollers (MCUs) from the MSP ultra-low-power MCU series are general-purpose 16-bit microcontrollers used for a wide range of applications including consumer electronics, data logging applications, portable medical instruments, and low-power metering. MSP430F4x MCUs feature an integrated LCD controller, while select MSP430F2x devices feature extended temperature ranges.

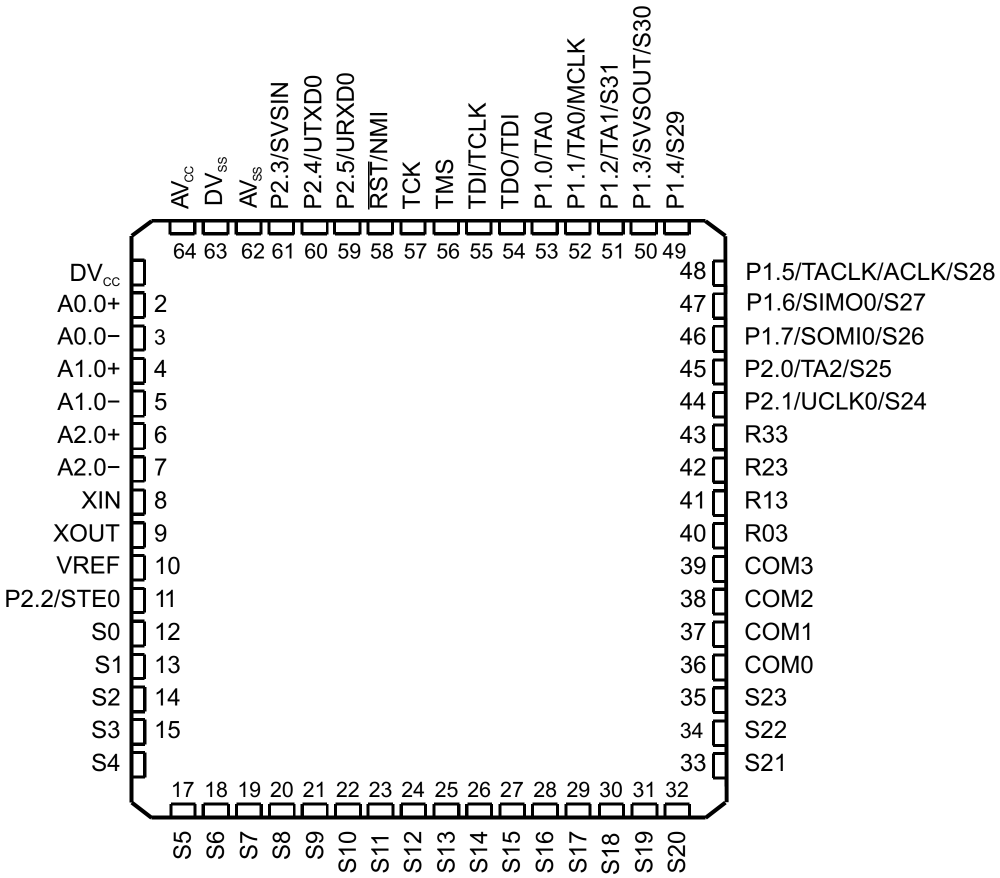
Companion Products for MSP430F427 Review products that are frequently purchased or used with this product.

Reference Designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout for the 64-pin PM package.



NOTE: TI recommends leaving all unused analog inputs open.

Figure 4-1. 64-Pin PM Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants

Table 4-1. Terminal Functions

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
DVCC	1		Digital supply voltage, positive terminal
A0.0+	2	I	Internal connection to SD16 channel 0, input 0 +[1]
A0.0−	3	I	Internal connection to SD16 channel 0, input 0 −[1]
A1.0+	4	I	Internal connection to SD16 channel 1, input 0 +[1]
A1.0−	5	I	Internal connection to SD16 channel 1, input 0 −[1]
A2.0+	6	I	Internal connection to SD16 channel 2, input 0 +[1]
A2.0−	7	I	Internal connection to SD16 channel 2, input 0 −[1]
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
V_{REF}	10	I/O	Input for an external reference voltage, internal reference voltage output (can be used as mid-voltage)
P2.2/STE0	11	I/O	General-purpose digital I/O Slave transmit enable for USART0 in SPI mode
S0	12	O	LCD segment output 0
S1	13	O	LCD segment output 1
S2	14	O	LCD segment output 2
S3	15	O	LCD segment output 3
S4	16	O	LCD segment output 4
S5	17	O	LCD segment output 5
S6	18	O	LCD segment output 6
S7	19	O	LCD segment output 7
S8	20	O	LCD segment output 8
S9	21	O	LCD segment output 9
S10	22	O	LCD segment output 10
S11	23	O	LCD segment output 11
S12	24	O	LCD segment output 12
S13	25	O	LCD segment output 13
S14	26	O	LCD segment output 14
S15	27	O	LCD segment output 15
S16	28	O	LCD segment output 16
S17	29	O	LCD segment output 17
S18	30	O	LCD segment output 18
S19	31	O	LCD segment output 19
S20	32	O	LCD segment output 20
S21	33	O	LCD segment output 21
S22	34	O	LCD segment output 22
S23	35	O	LCD segment output 23
COM0	36	O	Common output, COM0−COM3 are used for LCD backplanes.
COM1	37	O	Common output, COM0−COM3 are used for LCD backplanes.
COM2	38	O	Common output, COM0−COM3 are used for LCD backplanes.
COM3	39	O	Common output, COM0−COM3 are used for LCD backplanes.
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
R13	41	I	Input port of third most positive analog LCD level (V4 or V3)
R23	42	I	Input port of second most positive analog LCD level (V2)

(1) TI recommends open connection for all unused analog inputs.

Table 4-1. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
R33	43	O	Output port of most positive analog LCD level (V1)
P2.1/UCLK0/S24	44	I/O	General-purpose digital I/O External clock input for USART0 in UART or SPI mode or clock output for USART0 in SPI mode LCD segment output 24 (2)
P2.0/TA2/S25	45	I/O	General-purpose digital I/O Timer_A Capture: CCI2A input, Compare: Out2 output LCD segment output 25 (2)
P1.7/SOMI0/S26	46	I/O	General-purpose digital I/O Slave out/master in for USART0 in SPI mode LCD segment output 26 (2)
P1.6/SIMO0/S27	47	I/O	General-purpose digital I/O Slave in/master out for USART0 in SPI mode LCD segment output 27 (2)
P1.5/TACLK/ACLK/S28	48	I/O	General-purpose digital I/O Timer_A and SD16 clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8) LCD segment output 28 (2)
P1.4/S29	49	I/O	General-purpose digital I/O LCD segment output 29 (2)
P1.3/SVSOUT/S30	50	I/O	General-purpose digital I/O SVS: output of SVS comparator LCD segment output 30 (2)
P1.2/TA1/S31	51	I/O	General-purpose digital I/O Timer_A, Capture: CCI1A, CCI1B input, Compare: Out1 output LCD segment output 31 (2)
P1.1/TA0/MCLK	52	I/O	General-purpose digital I/O Timer_A, Capture: CCI0B input. Note: TA0 is only an input on this pin. MCLK output BSL receive
P1.0/TA0	53	I/O	General-purpose digital I/O Timer_A, Capture: CCI0A input, Compare: Out0 output BSL transmit
TDO/TDI	54	I/O	Test data output port, TDO/TDI data output or programming data input terminal
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	58	I	Reset input Nonmaskable interrupt input port
P2.5/URXD0	59	I/O	General-purpose digital I/O Receive data in for USART0 in UART mode
P2.4/UTXD0	60	I/O	General-purpose digital I/O Transmit data out for USART0 in UART mode

(2) The LCD function is selected automatically when the applicable LCD module control bits are set, not with PxSEL bits.

Table 4-1. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
P2.3/SVSIN	61	I/O	General-purpose digital I/O Analog input to brownout, supply voltage supervisor
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry.
DV_{SS}	63		Digital supply voltage, negative terminal
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry. Do not power up before DVCC.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		–0.3	4.1	V
Voltage applied to any pin(2)		–0.3	V_{CC} + 0.3	V
Diode current at any device terminal			±2	mA
Storage temperature range, T_{stg}	Unprogrammed device	–55	150	°C
	Programmed device	–40	85	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}.The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution(1) ($AV_{CC} = DV_{CC} = V_{CC}$)	SD16 disabled		1.8		3.6	V
		SVS enabled, PORON = 1(2), SD16 disabled		2.0		3.6	
		SD16 enabled or during programming of flash memory		2.7		3.6	
V_{SS}	Supply voltage ($AV_{SS} = DV_{SS} = V_{SS}$)			0		0	V
T_A	Operating free-air temperature range			–40		85	°C
$f_{(LFXT1)}$	LFXT1 crystal frequency(3)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
		XT1 selected, XTS_FLL = 1	Ceramic resonator	450		8000	
		XT1 selected, XTS_FLL = 1	Crystal	1000		8000	
$f_{(System)}$	Processor frequency (signal MCLK) (also see Figure 5-1)	V_{CC} = 1.8 V		DC		4.15	MHz
		V_{CC} = 3.6 V		DC		8	

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.

(2) The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.

(3) In LF mode, the LFXT1 oscillator requires a watch crystal.

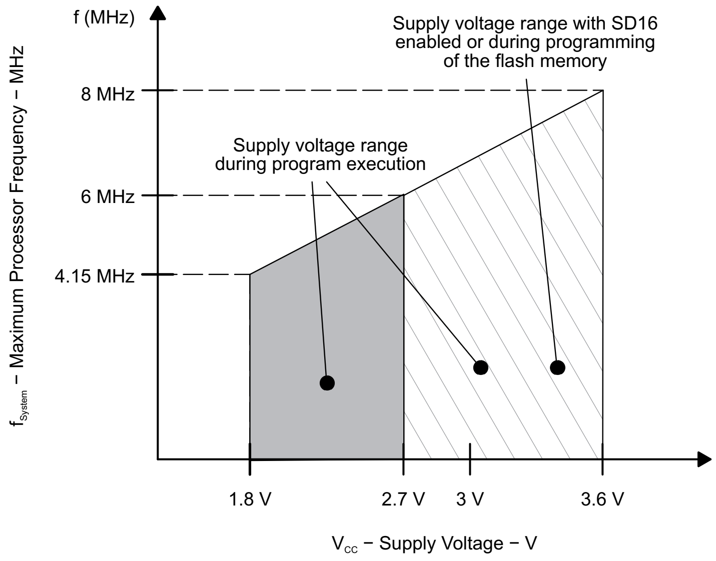


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode (AM) $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)} = 1$ MHz, $f_{(ACLK)} = 32768$ Hz, XTS_FLL = 0, program executes in flash	–40°C to 85°C	3 V		400	500	µA
$I_{(LPM0)}$	Low-power mode 0 or 1 (LPM0 or LPM1)[2] $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)} = 1$ MHz, $f_{(ACLK)} = 32768$ Hz, XTS_FLL = 0, FN_8 = FN_4 = FN_3 = FN_2 = 0	–40°C to 85°C	3 V		130	150	µA
$I_{(LPM2)}$	Low-power mode 2 (LPM2)[2]	–40°C to 85°C	3 V		10	22	µA
$I_{(LPM3)}$	Low-power mode 3 (LPM3) [2]	–40°C	3 V		1.5	2.0	µA
		25°C			1.6	2.1	
		60°C			1.7	2.2	
		85°C			2.0	3.5	
$I_{(LPM4)}$	Low-power mode 4 (LPM4)[2]	–40°C	3 V		0.1	0.5	µA
		25°C			0.1	0.5	
		85°C			0.8	2.5	

[1] All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2, LPM3, and LPM4 are measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the SD16 and the SVS module are specified in their respective sections. LPMx currents measured with WDT+ disabled. The currents are characterized with a KDS Daishinku DT-38 (6 pF) crystal.

[2] Current consumption for brownout is included.

Current consumption of active mode versus system frequency:

$$I_{(AM)} = I_{(AM)}\,[\text{at 1 MHz}] \times f_{(System)}\,[\text{MHz}]$$

Current consumption of active mode versus supply voltage:

$$I_{(AM)} = I_{(AM)}\,[\text{at 3 V}] + 170\ \mu\text{A/V} \times (V_{CC} - 3\ \text{V})$$

5.5 Thermal Resistance Characteristics, PM Package (LQFP64)

PARAMETER		VALUE	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(1)	55.7	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)	16.7	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(3)	27.1	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter	26.8	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter	0.8	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.6 Schmitt-Trigger Inputs − Ports (P1 and P2), $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK,TDO/TDI)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	3 V	1.5	1.98	V
V_{IT-}	Negative-going input threshold voltage	3 V	0.9	1.3	V
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})	3 V	0.45	1	V

5.7 Inputs P1.x, P2.x, TAx

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag(1)	3 V	1.5		cycle
				50		ns
$t_{(cap)}$	Timer_A capture timing	TAx	3 V	50		ns
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TAxCLK, INCLK $t_{(H)} = t_{(L)}$	3 V		10	MHz
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	3 V		10	MHz

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

5.8 Leakage Current − Ports (P1 and P2)(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current, Port P1.x	Port 1: $V_{(P1.x)}$ (2)	3 V		±50	nA
$I_{lkg(P2.x)}$	Leakage current, Port P2.x	Port 2: $V_{(P2.x)}$ (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The port pin must be selected as input.

5.9 Outputs − Ports (P1 and P2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA[1]	3 V	V_{CC} – 0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA[2]	3 V	V_{CC} – 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA[1]	3 V	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA[2]	3 V	V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.

(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

5.10 Output Frequency

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	Output frequency (1 ≤ × ≤ 2, 0 ≤ y ≤ 7)	C_L = 20 F, I_L = ±1.5 mA, V_{CC} = 3 V		DC		12	MHz
$f_{(ACLK)}$, $f_{(MCLK)}$, $f_{(SMCLK)}$	P1.1/TA0/MCLK, P1.5/TACLK/ACLK/S28	C_L = 20 pF, V_{CC} = 3 V				12	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK/S28, C_L = 20 pF, V_{CC} = 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 3 V, $f_{MCLK} = f_{DCOCLK}$		50% – 15 ns	50%	50% + 15 ns	

5.11 Typical Characteristics – Ports P1 and P2

Figure 5-2 through Figure 5-5 show the typical output currents of Ports P1 and P2. One output loaded at a time.

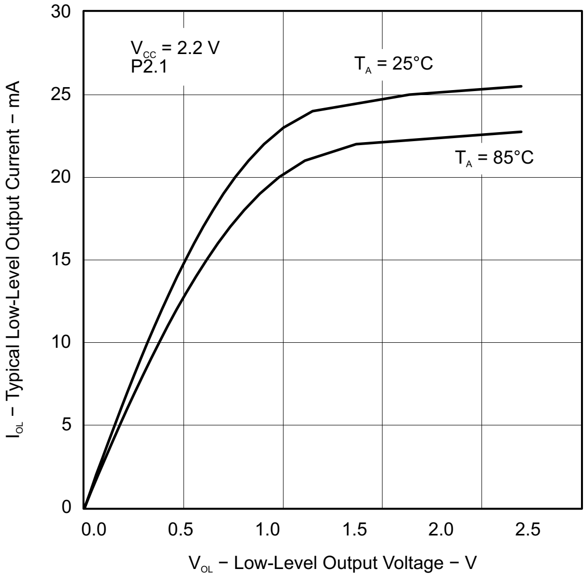


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

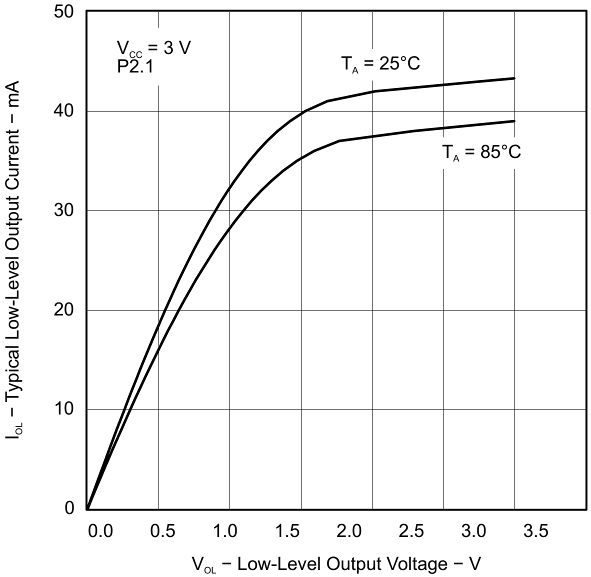


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

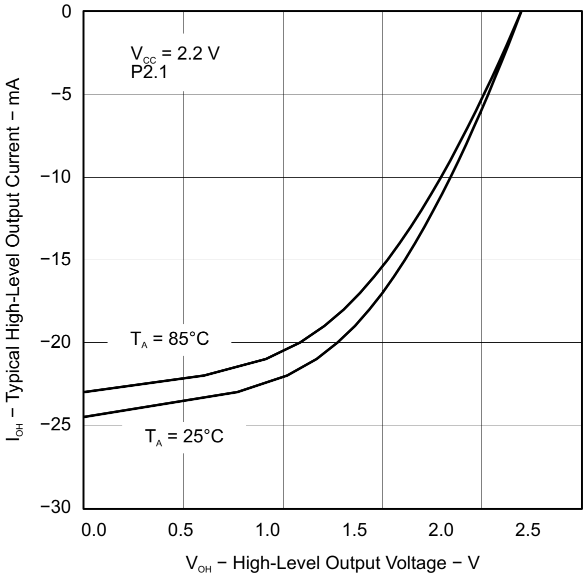


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

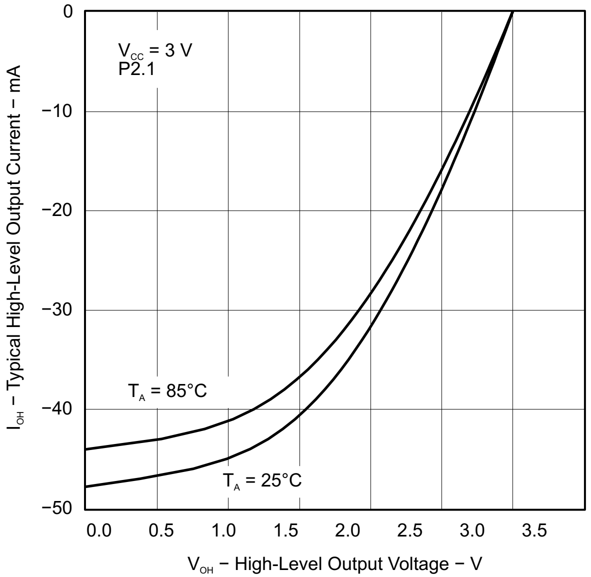


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.12 Wake-up Time From LPM3

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.13 RAM

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{RAMh}	CPU halted[1]	1.6		V

[1] This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.14 LCD

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at R23			$[V_{(33)} – V_{(03)}]$ × 2/3 + $V_{(03)}$		
$V_{(13)}$		Voltage at R13			$[V_{(33)} – V_{(03)}]$ × 1/3 + $V_{(03)}$		
$V_{(33)} – V_{(03)}$		Voltage at R33 to R03		2.5		V_{CC} + 0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		R13 = V_{CC} / 3				±20	
$I_{(R23)}$		R23 = 2 × V_{CC} / 3				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = –3 µA, V_{CC} = 3 V		$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

5.15 USART0[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART0 deglitch time	V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	ns

[1] The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of t(τ) to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of t(τ). The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

5.16 POR, BOR(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout(2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 5-6)		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 5-6 through Figure 5-8)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 5-6)	70	130	180	mV
$t_{(reset)}$		Pulse duration needed at $\overline{RST}$/NMI pin to accept reset internally, V_{CC} = 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)} \leq 1.8$ V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* for more information on the brownout and SVS circuit.

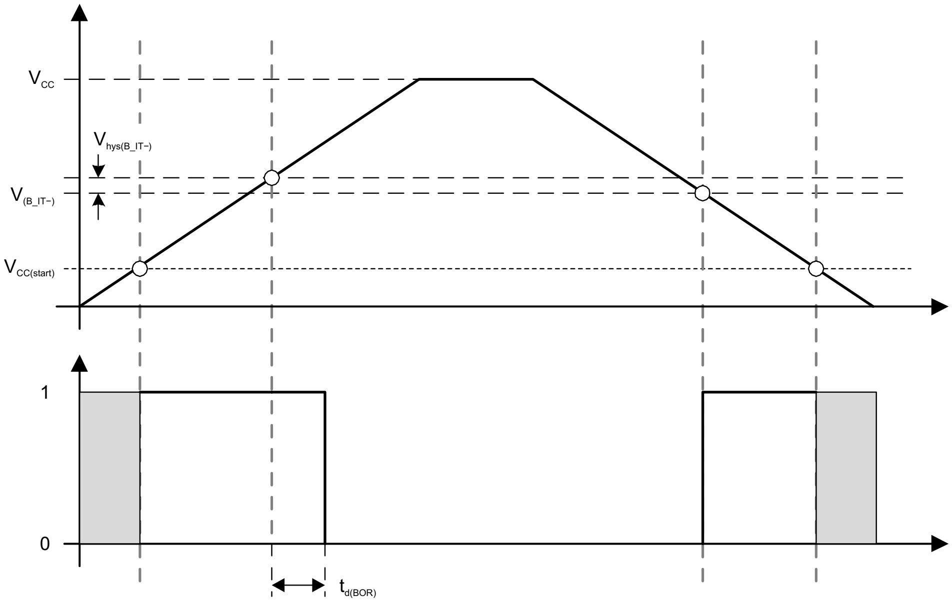


Figure 5-6. POR and BOR vs Supply Voltage

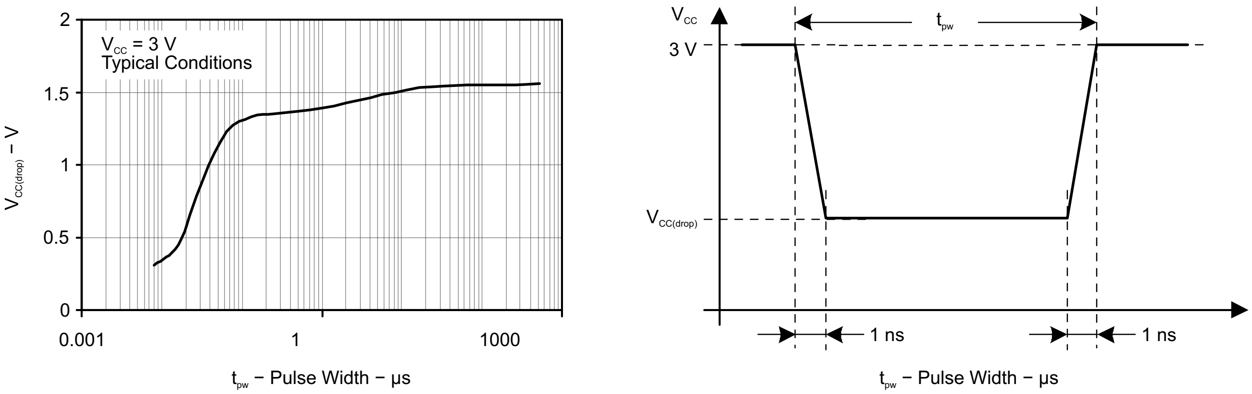


Figure 5-7. $V_{CC(drop)}$ Level With a Rectangular Voltage Drop to Generate a POR or BOR Signal

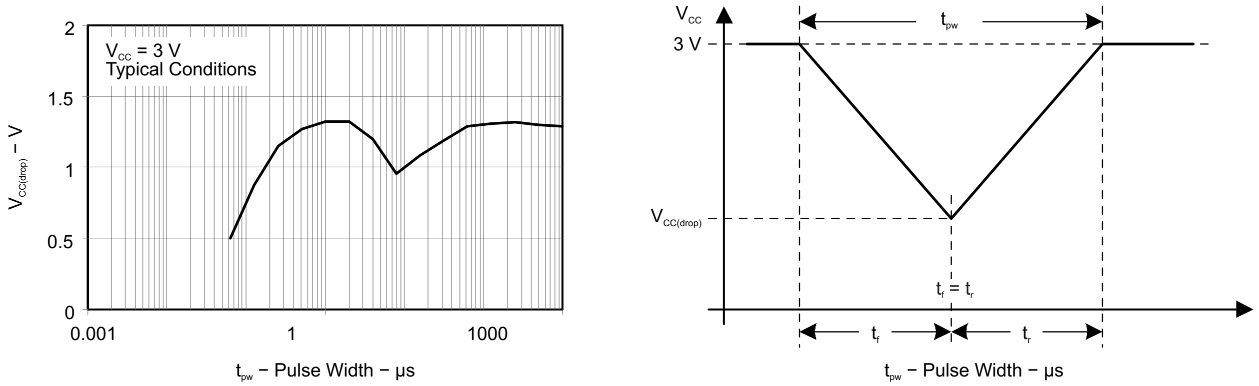


Figure 5-8. $V_{CC(drop)}$ Level With a Triangular Voltage Drop to Generate a POR or BOR Signal

5.17 SVS (Supply Voltage Supervisor and Monitor)(1)

over recommended operating free-air temperature range (unless otherwise noted) (also see Figure 5-10)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 5-9)		5		150	μs
	dV_{CC}/dt ≤ 30 V/ms				2000	
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	μs
t_{settle}	VLD ≠ 0(2)				12	μs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 5-9)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-9)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ × 0.004		$V_{(SVS\_IT-)}$ × 0.008	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-9), external voltage applied on P2.3	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-9)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61(3)	
		VLD = 13	3.24	3.5	3.76(3)	
		VLD = 14	3.43	3.7(3)	3.99(3)	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-9), external voltage applied on P2.3	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$(1)	VLD ≠ 0, V_{CC} = 2.2 V or 3 V			10	15	μA

(1) The current consumption of the SVS module is not included in the I_{CC} current consumption data.
(2) t_{settle} is the settling time that the comparator o/p must have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value between 2 and 15. The overdrive is assumed to be greater than 50 mV.
(3) The recommended operating voltage range is limited to 3.6 V.

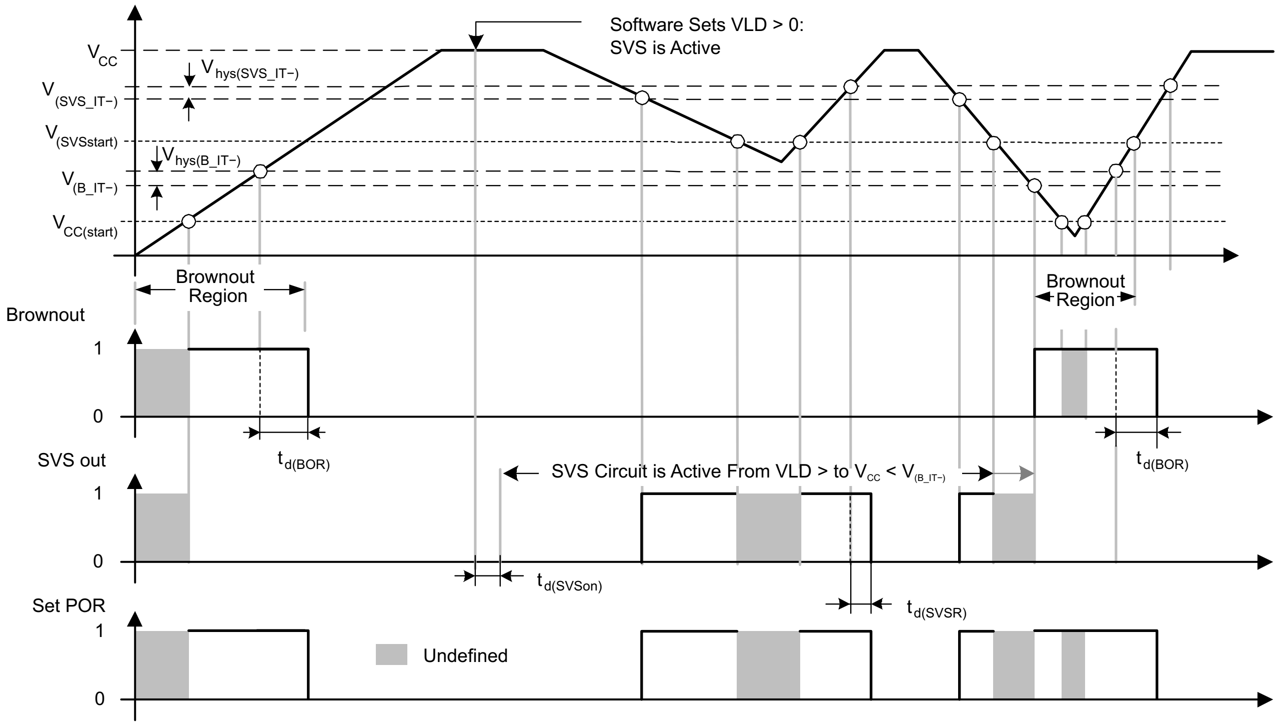


Figure 5-9. SVS Reset (SVSR) vs Supply Voltage

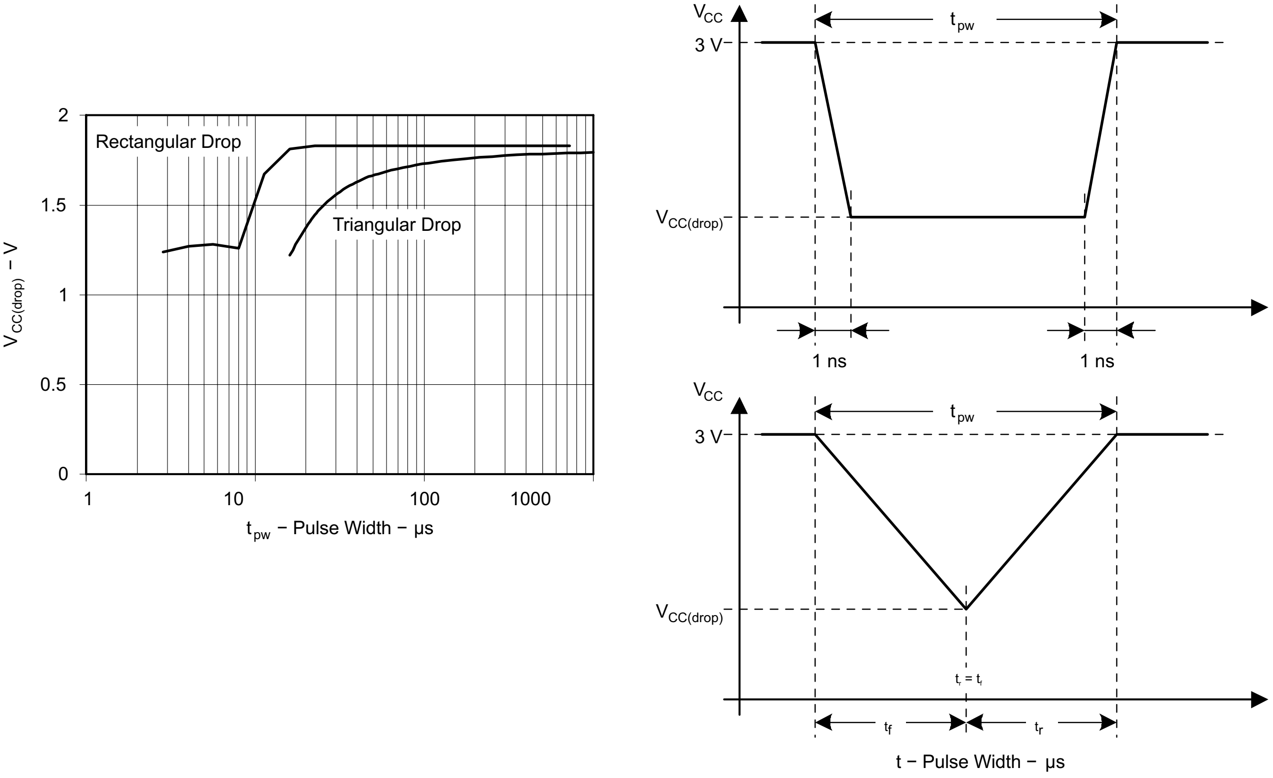


Figure 5-10. $V_{CC(drop)}$ With a Rectangular Voltage Drop and a Triangular Voltage Drop to Generate an SVS Signal

5.18 DCO

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5-11 through Figure 5-13)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0, $f_{Crystal}$ = 32.768 kHz	3 V		1		MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	3 V	0.3	0.7	1.3	MHz
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	3 V	2.7	6.1	11.3	MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	3 V	0.8	1.5	2.5	MHz
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	3 V	6.5	12.1	20	MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	3 V	1.3	2.2	3.5	MHz
$f_{(DCO = 27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	3 V	10.3	17.9	28.5	MHz
$f_{(DCO = 2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	3 V	2.1	3.4	5.2	MHz
$f_{(DCO = 27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	3 V	16	26.6	41	MHz
$f_{(DCO = 2)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1	3 V	4.2	6.3	9.2	MHz
$f_{(DCO = 27)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1	3 V	30	46	70	MHz
S_n	Step size (ratio) between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)}/f_{DCO(Tap\ n)}$ (see Figure 5-12 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	3 V	–0.2	–0.3	–0.4	%/°C
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		0	5	15	%/V

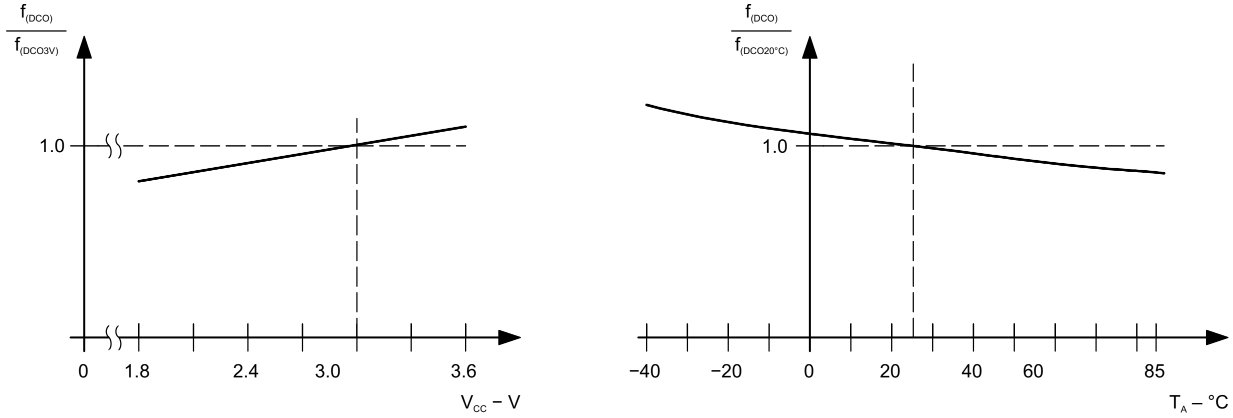


Figure 5-11. DCO Frequency vs Supply Voltage (V_{CC}) and vs Ambient Temperature

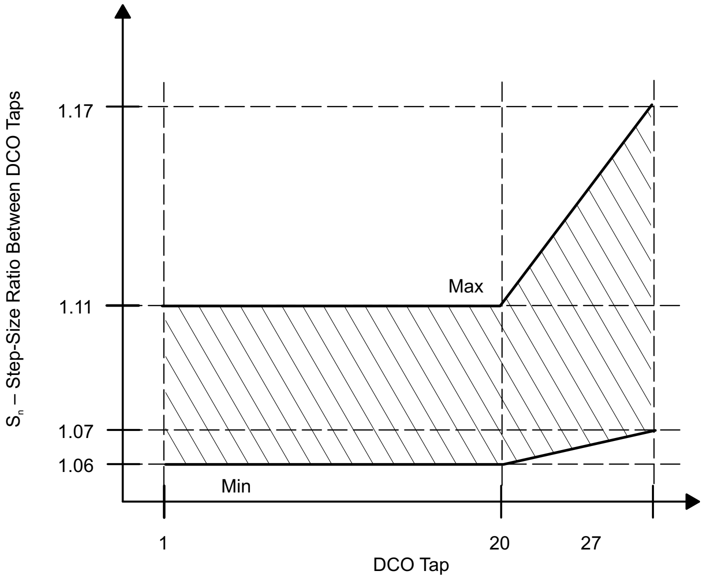


Figure 5-12. DCO Tap Step Size

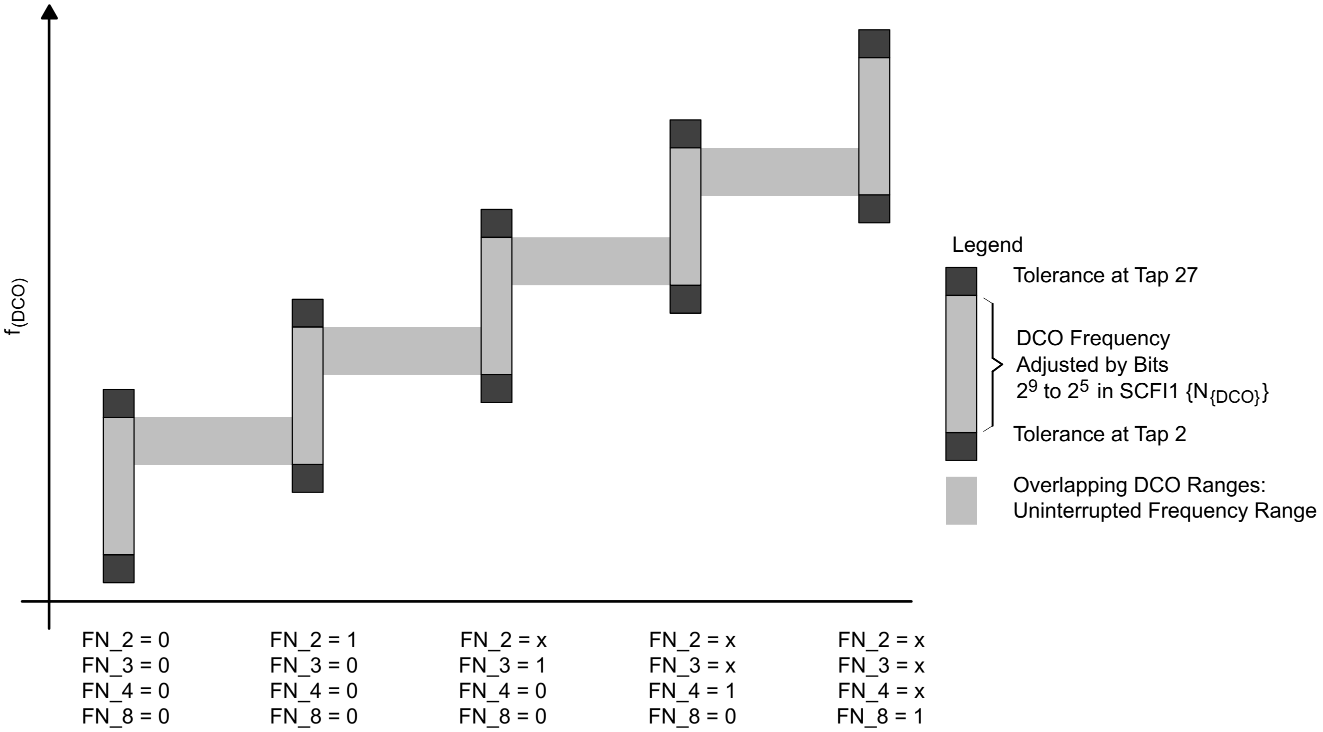


Figure 5-13. Five Overlapping DCO Ranges Controlled by FN_x Bits

5.19 Crystal Oscillator, LFXT1 Oscillator(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance(3)	OSCCAPx = 0h	3 V		0		pF
		OSCCAPx = 1h			10		
		OSCCAPx = 2h			14		
		OSCCAPx = 3h			18		
C_{XOUT}	Integrated output capacitance(3)	OSCCAPx = 0h	3 V		0		pF
		OSCCAPx = 1h			10		
		OSCCAPx = 2h			14		
		OSCCAPx = 3h			18		
V_{IL}	Input levels at XIN(4)		3 V	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}				$0.8 \times V_{CC}$		V_{CC}	

(1) The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. This is independent of XTS_FLL.

(2) To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(3) TI recommends external capacitance for precision real-time clock applications; OSCCAPx = 0h.

(4) Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.

5.20 SD16 Power Supply and Operating Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ = 0 V			2.7		3.6	V
I_{SD16}	Analog supply current: 1 active SD16 channel including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	GAIN: 1, 2	3 V		650	950	µA
			GAIN: 4, 8, 16			730	1100	
			GAIN: 32			1050	1550	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	GAIN: 1			620	930	
			GAIN: 32			700	1060	
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (low-power mode disabled)				1		MHz
		SD16LP = 1 (low-power mode enabled)				0.5		

5.21 SD16 Analog Input Range(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage range for specified performance(2)	SD16GAINx = 1, SD16REFON = 1			±500		mV
		SD16GAINx = 2, SD16REFON = 1			±250		
		SD16GAINx = 4, SD16REFON = 1			±125		
		SD16GAINx = 8, SD16REFON = 1			±62		
		SD16GAINx = 16, SD16REFON = 1			±31		
		SD16GAINx = 32, SD16REFON = 1			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1 MHz, SD16GAINx = 1	3 V		200		kΩ
		f_{SD16} = 1 MHz, SD16GAINx = 32			75		
Z_{ID}	Differential input impedance (IN+ to IN−)	f_{SD16} = 1 MHz, SD16GAINx = 1	3 V	300	400		kΩ
		f_{SD16} = 1 MHz, SD16GAINx = 32		100	150		
V_I	Absolute input voltage range			AV_{SS} – 1		AV_{CC}	V
V_{IC}	Common-mode input voltage range			AV_{SS} – 1		AV_{CC}	V

(1) All parameters pertain to each SD16 channel.
(2) The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF} / 2) / GAIN$ and $V_{FSR-} = -(V_{REF} / 2) / GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

5.22 SD16 Analog Performance

f_{SD16} = 1 MHz, SD16OSRx = 256, SD16REFON = 1, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1, signal amplitude = 500 mV	f_{IN} = 50 Hz or 100 Hz	3 V	83.5	85		dB
		SD16GAINx = 2, signal amplitude = 250 mV			81.5	84		
		SD16GAINx = 4, signal amplitude = 125 mV			76	79.5		
		SD16GAINx = 8, signal amplitude = 62 mV			73	76.5		
		SD16GAINx = 16, signal amplitude = 31 mV			69	73		
		SD16GAINx = 32, signal amplitude = 15 mV			62	69		
G	Nominal gain	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2			1.90	1.96	2.02	
		SD16GAINx = 4			3.76	3.86	3.96	
		SD16GAINx = 8			7.36	7.62	7.84	
		SD16GAINx = 16			14.56	15.04	15.52	
		SD16GAINx = 32			27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1		3 V			±0.2	%FSR
		SD16GAINx = 32					±1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1		3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32				±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz or 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz or 100 Hz				>75		
AC PSRR	AC power-supply rejection ratio	SD16GAINx = 1, V_{CC} = 3 V ±100 mV, f_{VCC} = 50 Hz		3 V		>80		dB
XT	Crosstalk			3 V		<–100		dB

5.23 SD16 Built-in Temperature Sensor(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/K
$V_{Offset,sensor}$	Sensor offset voltage			–100		100	mV
V_{Sensor}	Sensor output voltage(2)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C		355	395	435	
		Temperature sensor voltage at T_A = 0°C		320	360	400	

(1) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV]

(2) Results based on characterization or production test, no TC_{Sensor} or $V_{Offset,sensor}$.

5.24 SD16 Built-in Voltage Reference

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0	3 V		20	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1 SD16VMIDON = 0 (1)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 0, SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turnon time	SD16REFON = 0 → 1, SD16VMIDON = 0, C_{REF} = 100 nF	3 V		5		ms
DC PSR	DC power supply rejection, $\Delta V_{REF}/\Delta V_{CC}$	SD16REFON = 1, SD16VMIDON = 0, V_{CC} = 2.5 V to 3.6 V			200		µV/V

(1) No capacitance is required on V_{REF}. However, TI recommends a capacitance of at least 100 nF to reduce any reference voltage noise.

5.25 SD16 Built-in Reference Output Buffer

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference supply and reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	A
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation versus load current	$\lvert I_{LOAD} \rvert$ = 0 to 1 mA	3 V	–15		+15	mV
t_{ON}	Turnon time	SD16REFON = 0 → 1, SD16VMIDON = 0, C_{REF} = 100 nF	3 V		100		µs

5.26 SD16 External Reference Input

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

5.27 Flash Memory

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.7		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V, 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V, 3.6 V		3	7	mA
t_{CPT}	Cumulative program time (1)		2.7 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time (2)		2.7 V, 3.6 V	200			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time (3)				35		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word (3)				30		
$t_{Block, 1–63}$	Block program time for each additional byte or word (3)				21		
$t_{Block, End}$	Block program end-sequence wait time (3)				6		
$t_{Mass Erase}$	Mass erase time (3)				5297		
$t_{Seg Erase}$	Segment erase time (3)				4819		

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.
(2) The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 × (1 / f_{FTG},max) = 5297 × (1 / 476 kHz)). To achieve the required cumulative mass erase time, the mass erase operation of the flash controller can be repeated until this time is met (a worst case minimum of 19 cycles is required).
(3) These values are hardwired into the state machine of the flash controller (t_{FTG} = 1 / f_{FTG}).

5.28 JTAG Interface

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See (1)	2.2 V	0		5	MHz
			3V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	See (2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

5.29 JTAG Fuse (1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be manged with all instructions.

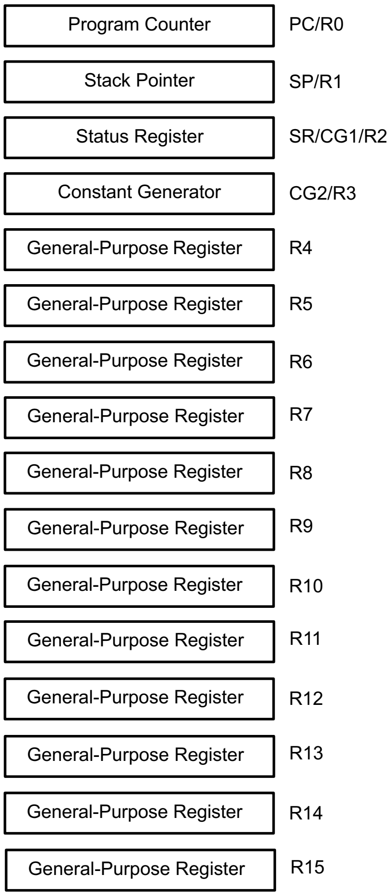


Figure 6-1. CPU Registers

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats, and Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE		OPERATION
Dual operands, source and destination	ADD	R4,R5	R4 + R5 → R5
Single operand, destination only	CALL	R8	PC→(TOS), R8 →PC
Relative jump, unconditional or conditional	JNE		Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S[1]	D[1]	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	●	●	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	●		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) → R11 R10 + 2→ R10
Immediate	●		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

(1) S = source, D = destination

6.3 Operating Modes

The MSP430F42x has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active, MCLK available to modules.
  - FLL+ loop control remains active.
- Low-power mode 1 (LPM1)
  - CPU is disabled.
  - ACLK and SMCLK remain active, MCLK available to modules.
  - FLL+ loop control is disabled.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DC generator of the DCO remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DC generator of the DCO is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DC generator of the DCO is disabled.
  - Crystal oscillator is stopped.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. Table 6-3 lists the interrupt sources, flags, and vectors.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash memory PC out of range(1)	WDTIFG KEYV(2)	Reset	0FFFEh	15, highest
NMI oscillator fault Flash memory access violation	NMIIFG(2) OFIFG(2) ACCVIFG(2)	(Non)maskable(3) (Non)maskable (Non)maskable	0FFFCh	14
			0FFFAh	13
SD16	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG(2)(4)	Maskable	0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
			0FFEEh	7
Timer_A3	TACCR0 CCIFG(4)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, and TACTL TAIFG(2)(4)	Maskable	0FFEAh	5
I/O port P1 (8 flags)	P1IFG.0 to P1IFG.7(2)(4)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (8 flags)	P2IFG.0 to P2IFG.7(2)(4)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h−01FFh) or from within unused address ranges (0600h–0BFFh).
(2) Multiple source flags
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are in the module.

6.5 Special Function Registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is reset or set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is reset or set by POR.
▨	SFR bit is not present in device.

Figure 6-2 shows the Interrupt Enable Register 1, and Table 6-4 describes the bit fields.

Figure 6-2. Interrupt Enable Register 1 (Address = 00h)

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE	▨	▨	OFIE	WDTIE
rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

Table 6-4. Interrupt Enable Register 1 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXIE0	RW	0h	USART0: UART and SPI transmit interrupt enable
6	URXIE0	RW	0h	USART0: UART and SPI receive interrupt enable
5	ACCVIE	RW	0h	Flash access violation interrupt enable
4	NMIIE	RW	0h	(Non)maskable interrupt enable
1	OFIE	RW	0h	Oscillator fault interrupt enable
0	WDTIE	RW	0h	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

Figure 6-3 shows the Interrupt Enable Register 2, and Table 6-5 describes the bit fields.

Figure 6-3. Interrupt Enable Register 2 (Address = 01h)

7	6	5	4	3	2	1	0
BTIE	▨	▨	▨	▨			
rw-0							

Table 6-5. Interrupt Enable Register 2 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BTIE	RW	0h	Basic Timer1 interrupt enable

Figure 6-4 shows the Interrupt Flag Register 1, and Table 6-6 describes the bit fields.

Figure 6-4. Interrupt Flag Register 1 (Address = 02h)

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
rw-1	rw-0		rw-0			rw-1	rw-(0)

Table 6-6. Interrupt Flag Register 1 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXIFG0	RW	1h	USART0: UART and SPI transmit flag
6	URXIFG0	RW	0h	USART0: UART and SPI receive flag
4	NMIIFG	RW	0h	Set by the $\overline{RST}$/NMI pin
1	OFIFG	RW	1h	Flag set on oscillator fault.
0	WDTIFG	RW	0h	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

Figure 6-5 shows the Interrupt Flag Register 2, and Table 6-7 describes the bit fields.

Figure 6-5. Interrupt Flag Register 2 (Address = 03h)

7	6	5	4	3	2	1	0
BTIFG							
rw-0							

Table 6-7. Interrupt Flag Register 2 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BTIFG	RW	0h	Basic Timer1 interrupt flag

Figure 6-6 shows the Module Enable Register 1, and Table 6-8 describes the bit fields.

Figure 6-6. Module Enable Register 1 (Address = 04h)

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0						
rw-0	rw-0						

Table 6-8. Module Enable Register 1 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXE0	RW	0h	USART0: UART mode transmit enable
6	URXE0 USPIE0	RW	0h	USART0: UART mode receive enable USART0: SPI mode transmit and receive enable

Module Enable Register 2 is not defined for the MSP430F42x MCUs.

6.6 Memory Organization

Table 6-9 summarizes the memory map of the MSP430F42x MCUs.

Table 6-9. Memory Organization

		MSP430F423	MSP430F425	MSP430F427
Memory	Size	8KB	16KB	32KB
Interrupt vector	Flash	0FFFFh–0FFE0h	0FFFFh–0FFE0h	0FFFFh–0FFE0h
Code memory	Flash	0FFFFh–0E000h	0FFFFh–0C000h	0FFFFh–08000h
Information memory	Size	256 Byte 010FFh–01000h	256 Byte 010FFh–01000h	256 Byte 010FFh–01000h
Boot memory	Size	1KB 0FFFh–0C00h	1KB 0FFFh–0C00h	1KB 0FFFh–0C00h
RAM	Size	256 Byte 02FFh–0200h	512 Byte 03FFh–0200h	1KB 05FFh–0200h
Peripherals	16-bit	01FFh–0100h	01FFh–0100h	01FFh–0100h
	8-bit	0FFh–010h	0FFh–010h	0FFh–010h
	8-bit SFR	0Fh–00h	0Fh–00h	0Fh–00h

6.7 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the MCU memory through the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see *MSP430 Programming WIth the Bootloader (BSL)*.

BSL FUNCTION	PM PACKAGE PINS
Data transmit	53 - P1.0
Data receiver	52 - P1.1

6.8 Flash Memory

The flash memory (see Figure 6-7) can be programmed using the JTAG port, the bootloader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory before the first use.

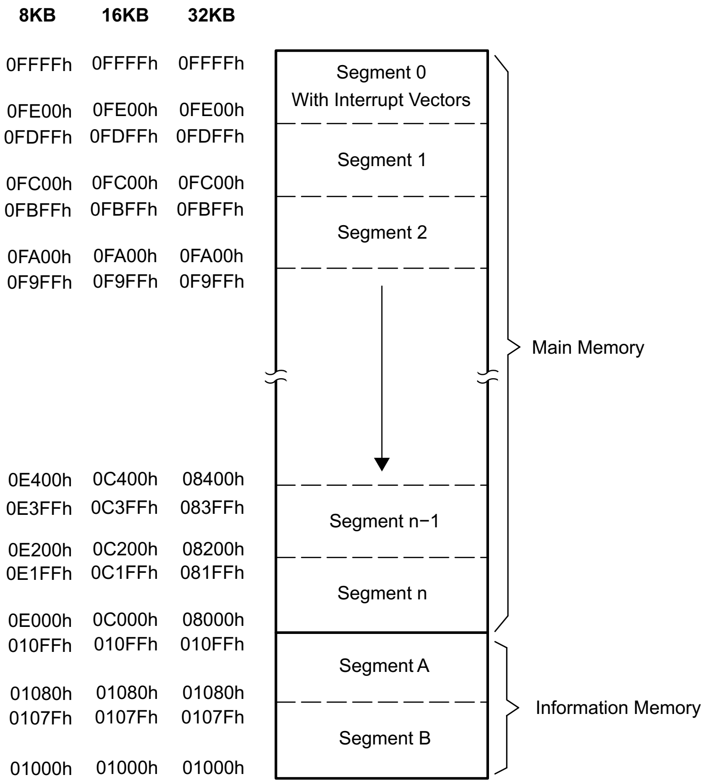


Figure 6-7. Flash Memory Map

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*.

6.9.1 Oscillator and System Clock

The clock system is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 6 µs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

6.9.2 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.3 Digital I/O

Two I/O ports are implemented: ports P1 and P2 (only six P2 I/O signals are available on external pins).

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the 8 bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE

Six bits of port P2 (P2.0 to P2.5) are available on external pins, but all control and data bits for port P2 are implemented.

6.9.4 Basic Timer1

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

6.9.5 LCD Driver

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported by this peripheral.

6.9.6 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.7 *Timer_A3*

Timer_A3 is a 16-bit timer and counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-10). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
48 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
48 - P1.5	$\overline{\text{TACLK}}$	INCLK			
53 - P1.0	TA0	CCI0A	CCR0	TA0	53 - P1.0
52 - P1.1	TA0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
51 - P1.2	TA1	CCI1A	CCR1	TA1	51 - P1.2
51 - P1.2	TA1	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
45 - P2.0	TA2	CCI2A	CCR2	TA2	45 - P2.0
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

6.9.8 *USART0*

The MSP430F42x devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. USART0 supports synchronous SPI (3- or 4-pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.9.9 *Hardware Multiplier*

The multiplication operation is supported by a dedicated peripheral module. The module performs 16- × 16-bit, 16- × 8-bit, 8- × 16-bit, and 8- × 8-bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.9.10 *SD16*

The SD16 module integrates three independent 16-bit sigma-delta ADCs, an internal temperature sensor, and a built-in voltage reference. Each channel is designed with a fully differential analog input pair and programmable gain amplifier input stage.

6.9.11 Peripheral File Map

Table 6-11 and Table 6-12 list the peripheral registers with their addresses.

Table 6-11. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_A3	Timer0_A interrupt vector	TA0IV	012Eh
	Timer0_A control	TACTL0	0160h
	Capture/compare control 0	TACCTL0	0162h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A counter	TA0R	0170h
	Capture/compare 0	TACCR0	0172h
	Capture/compare 1	TACCR1	0174h
	Capture/compare 2	TACCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Hardware Multiplier	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand 1	MACS	0136h
	Multiply + accumulate/operand 1	MAC	0134h
	Multiply signed/operand 1	MPYS	0132h
	Multiply unsigned/operand 1	MPY	0130h
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

Table 6-11. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
SD16 (also see Table 6-12)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Channel 1 control	SD16CCTL1	0104h
	Channel 2 control	SD16CCTL2	0106h
	Reserved		0108h
	Reserved		010Ah
	Reserved		010Ch
	Reserved		010Eh
	Interrupt vector word	SD16IV	0110h
	Channel 0 conversion memory	SD16MEM0	0112h
	Channel 1 conversion memory	SD16MEM1	0114h
	Channel 2 conversion memory	SD16MEM2	0116h
	Reserved		0118h
	Reserved		011Ah
	Reserved		011Ch
	Reserved		011Eh

Table 6-12. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
SD16 (also see Table 6-11)	Channel 0 input control	SD16INCTL0	0B0h
	Channel 1 input control	SD16INCTL1	0B1h
	Channel 2 input control	SD16INCTL2	0B2h
	Reserved		0B3h
	Reserved		0B4h
	Reserved		0B5h
	Reserved		0B6h
	Reserved		0B7h
	Channel 0 preload	SD16PRE0	0B8h
	Channel 1 preload	SD16PRE1	0B9h
	Channel 2 preload	SD16PRE2	0BAh
	Reserved		0BBh
	Reserved		0BCh
	Reserved		0BDh
	Reserved		0BEh
	Reserved		0BFh
LCD	LCD memory 20	LCDM20	0A4h
	⋮	⋮	⋮
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	⋮	⋮	⋮
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h

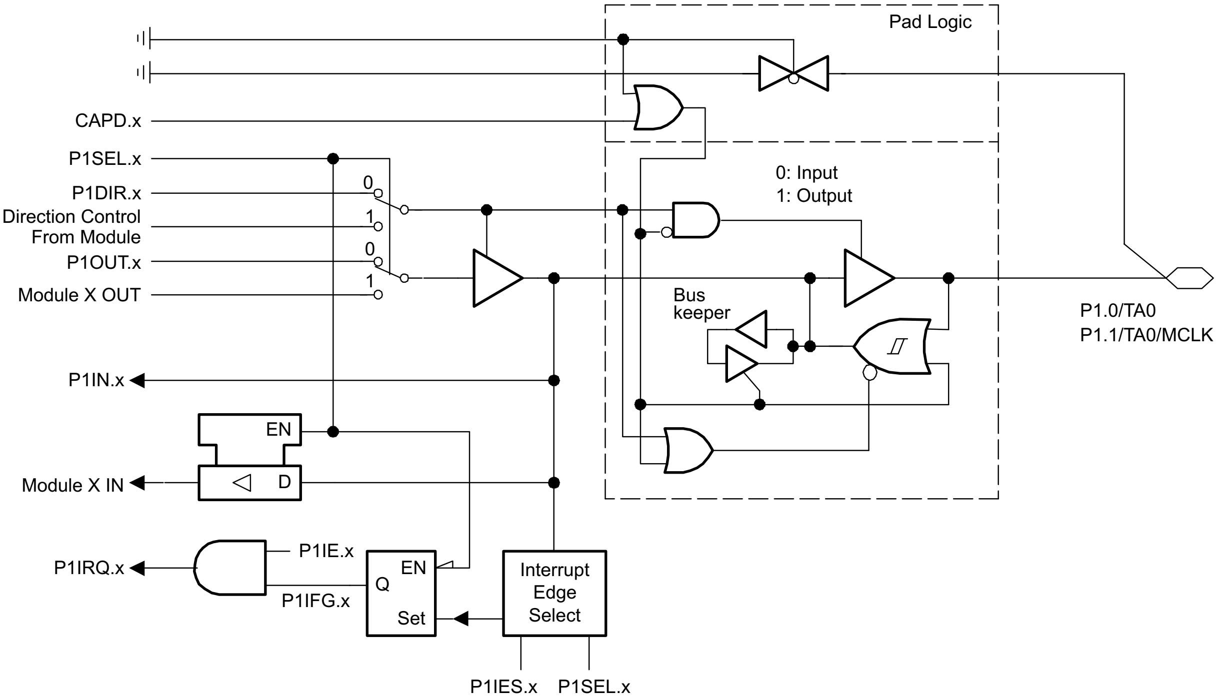
Table 6-12. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate 1	U0BR1	075h
	Baud rate 0	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Brownout, SVS	SVS control register	SVSCTL	056h
FLL+ Clock	FLL+ control 1	FLL_CTL1	054h
	FLL+ control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-13 summarizes the selection of the port function.



NOTE: 0 ≤ x ≤ 1. Port function is active if CAPD.x = 0.

Figure 6-8. Port P1 (P1.0 and P1.1) Diagram

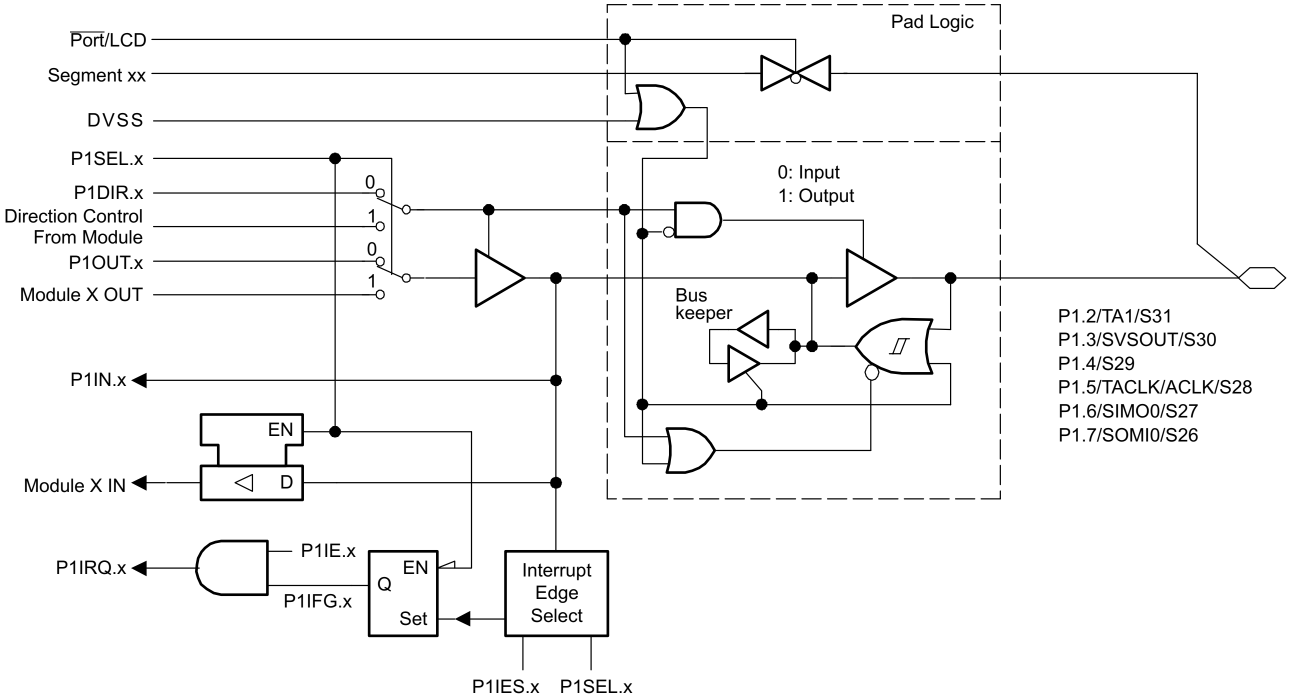
Table 6-13. Port P1 (P1.0 and P1.1) Pin Function

P1SEL.x	P1DIR.x	DIRECTION CONTROL FROM MODULE	P1OUT.x	MODULE X OUT	P1IN.x	MODULE X IN	P1IE.x	P1IFG.x	P1IES.x	CAPD.x
P1SEL.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 Sig.(1)	P1IN.0	CCI0A(1)	P1IE.0	P1IFG.0	P1IES.0	DVSS
P1SEL.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B(1)	P1IE.1	P1IFG.1	P1IES.1	DVSS

(1) Timer_A3

6.10.2 Port P1 (P1.2 to P1.7) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-14 summarizes the selection of the port function.



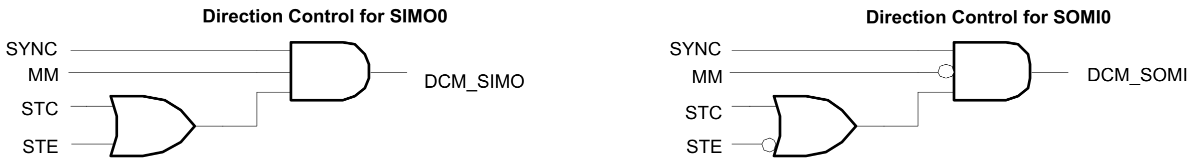
NOTE: 2 ≤ x ≤ 7. Port function is active if $\overline{\text{Port}}$/LCD = 0.

Figure 6-9. Port P1 (P1.2 to P1.7) Diagram

Table 6-14. Port P1 (P1.2 to P1.7) Pin Functions

P1SEL.x	P1DIR.x	DIRECTION CONTROL FROM MODULE	P1OUT.x	MODULE X OUT	P1IN.x	MODULE X IN	P1IE.x	P1IFG.x	P1IES.x	$\overline{\text{Port}}$/LCD	SEGMENT
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 Sig. (1)	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2	0: LCDPx < 05h, 1: LCDPx ≥ 05h	S31
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	unused	P1IE.3	P1IFG.3	P1IES.3		S30
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	DVSS	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4		S29
P1SEL.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK (1)	P1IE.5	P1IFG.5	P1IES.5		S28
P1SEL.6	P1DIR.6	DCM_SIMO	P1OUT.6	SIMO0(o) (2)	P1IN.6	SIMO0(i) (2)	P1IE.6	P1IFG.6	P1IES.6	0: LCDPx < 04h, 1: LCDPx ≥ 04h	S27
P1SEL.7	P1DIR.7	DCM_SOMI	P1OUT.7	SOMI0(o) (2)	P1IN.7	SOMI0(i) (2)	P1IE.7	P1IFG.7	P1IES.7		S26

(1) Timer_A3
(2) USART0 (also see Figure 6-10)

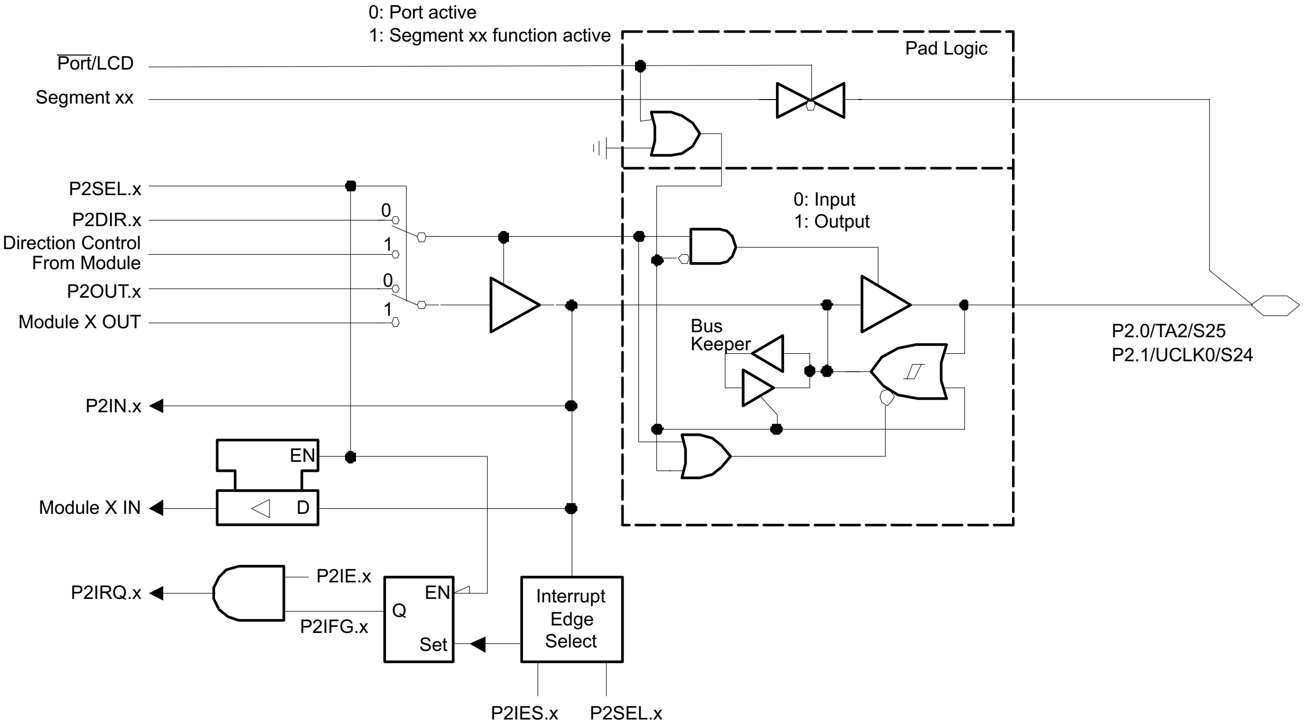

Direction Control for SIMO0

Direction Control for SOMI0

Figure 6-10. Direction Control for SIMO0 and SOMI0

6.10.3 Port P2 (P2.0 and P2.1) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-15 summarizes the selection of the port function.



NOTE: 0 ≤ x ≤ 1. Port function is active if Port/LCD = 0.

Figure 6-11. Port P2 (P2.0 and P2.1) Diagram

Table 6-15. Port P2 (P2.0 and P2.1) Pin Functions

P2Sel.x	P2DIR.x	DIRECTION CONTROL FROM MODULE	P2OUT.x	MODULE X OUT	P2IN.x	MODULE X IN	P2IE.x	P2IFG.x	P2IES.x	Port/LCD	SEGMENT
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 Sig.(1)	P2IN.0	CCI2A(1)	P2IE.0	P2IFG.0	P2IES.0	0: LCDPx < 04h, 1: LCDPx ≥ 04h	S25
P2Sel.1	P2DIR.1	DCM_UCLK	P2OUT.1	UCLK0(o)(2)	P2IN.1	UCLK0(i)(2)	P2IE.1	P2IFG.1	P2IES.1		S24

(1) Timer_A3
(2) USART0 (also see Figure 6-12)

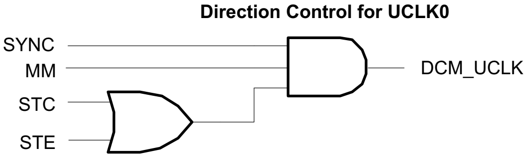
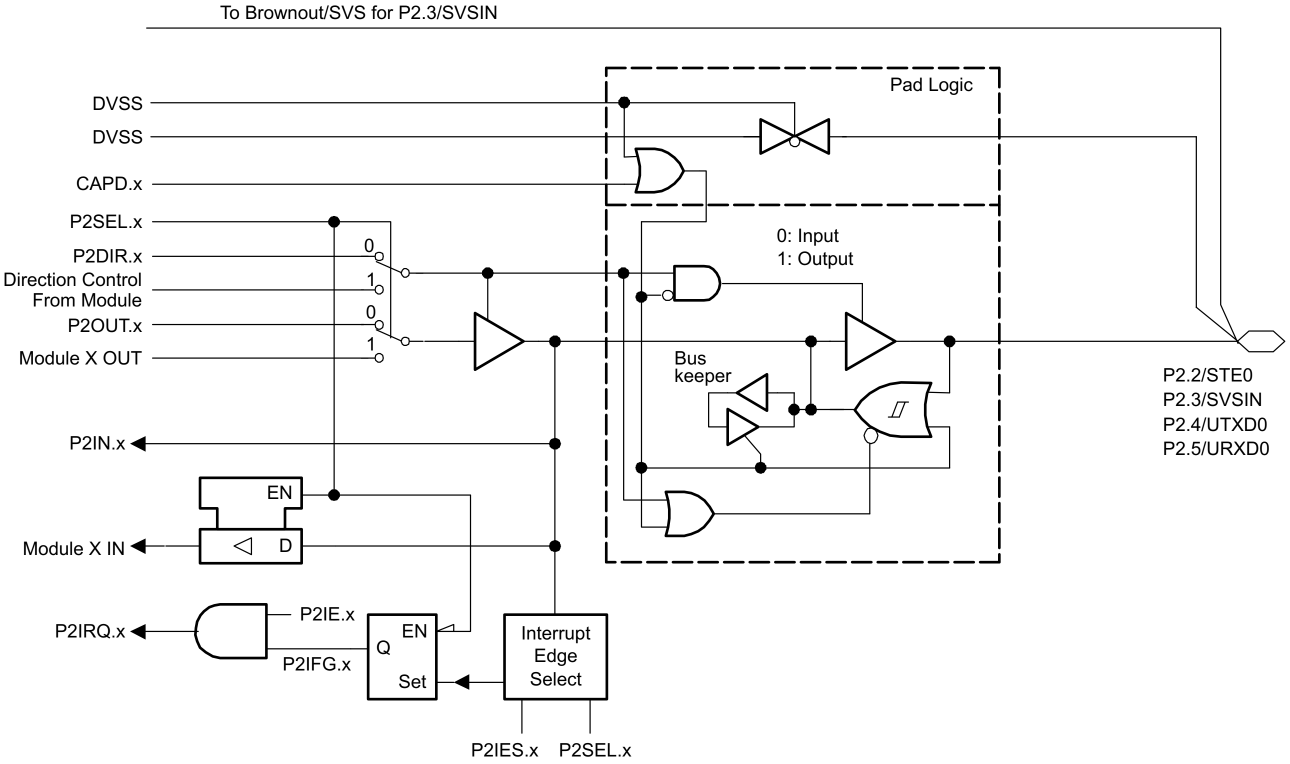


Figure 6-12. Direction Control for UCLK0

6.10.4 Port P2 (P2.2 to P2.5) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-16 summarizes the selection of the port function.



NOTE: 2 ≤ x ≤ 5. Port function is active if CAPD.x = 0

Figure 6-13. Port P2 (P2.2 to P2.5) Diagram

Table 6-16. Port P2 (P2.2 to P2.5) Pin Functions

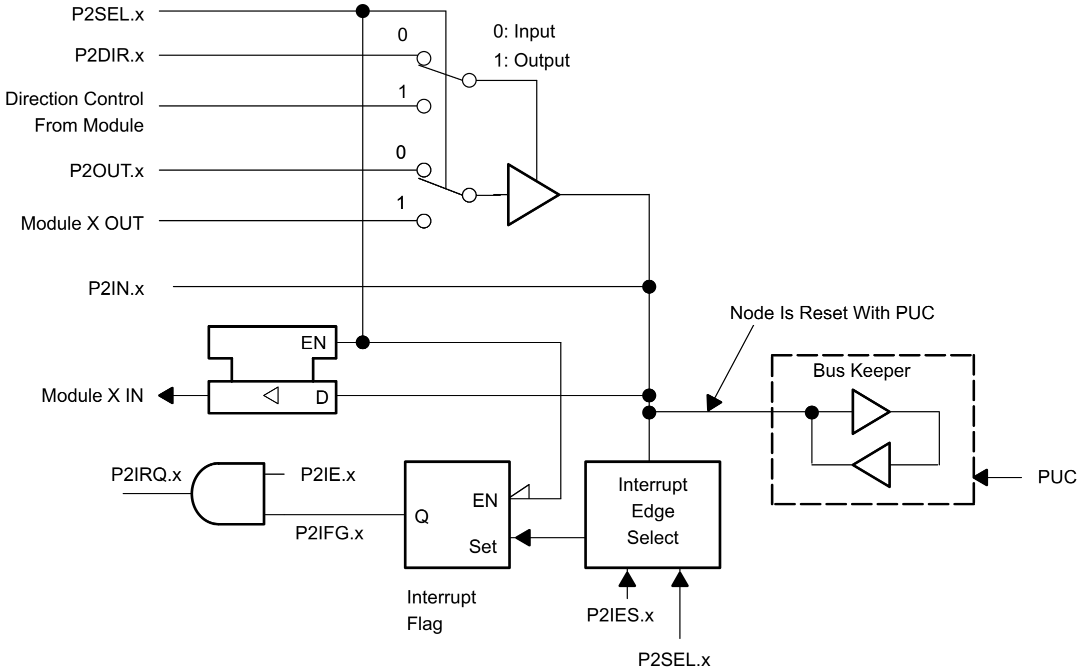
P2SEL.x	P2DIR.x	DIRECTION CONTROL FROM MODULE	P2OUT.x	MODULE X OUT	P2IN.x	MODULE X IN	P2IE.x	P2IFG.x	P2IES.x	CAPD.x
P2SEL.2	P2DIR.2	DVSS	P2OUT.2	DVSS	P2IN.2	STE0(1)	P2IE.2	P2IFG.2	P2IES.2	DVSS
P2SEL.3	P2DIR.3	P2DIR.3	P2OUT.3	DVSS	P2IN.3	Unused	P2IE.3	P2IFG.3	P2IES.3	SVSCTL VLD = 1111b
P2SEL.4	P2DIR.4	DVCC	P2OUT.4	UTXD0(1)	P2IN.4	Unused	P2IE.4	P2IFG.4	P2IES.4	DVSS
P2SEL.5	P2DIR.5	DVSS	P2OUT.5	DVSS	P2IN.5	URXD0(1)	P2IE.5	P2IFG.5	P2IES.5	DVSS

(1) USART0

6.10.5 Port P2 (P2.6 and P2.7) Unbonded GPIOs

Unbonded GPIOs P2.6 and P2.7 can be used as interrupt flags. Only software can affect the interrupt flags. They work as software interrupts.

Figure 6-14 shows the port diagram. Table 6-17 summarizes the selection of the port function.



NOTE: x = Bit identifier 6 or 7 for Port P2 without external pins

Figure 6-14. Port P2 (P2.6 and P2.7) Diagram

Table 6-17. Port P2 (P2.6 and P2.7) Pin Functions

P2SEL.x	P2DIR.x	DIRECTION CONTROL FROM MODULE	P2OUT.x	MODULE X OUT	P2IN.x	MODULE X IN	P2IE.x	P2IFG.x	P2IES.x
P2SEL.6	P2DIR.6	P2DIR.6	P2OUT.6	DVSS	P2IN.6	Unused	P2IE.6	P2IFG.6	P2IES.6
P2SEL.7	P2DIR.7	P2DIR.7	P2OUT.7	DVSS	P2IN.7	Unused	P2IE.7	P2IFG.7	P2IES.7

6.10.6 JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt-Trigger or Output

Figure 6-15 shows the port diagram.

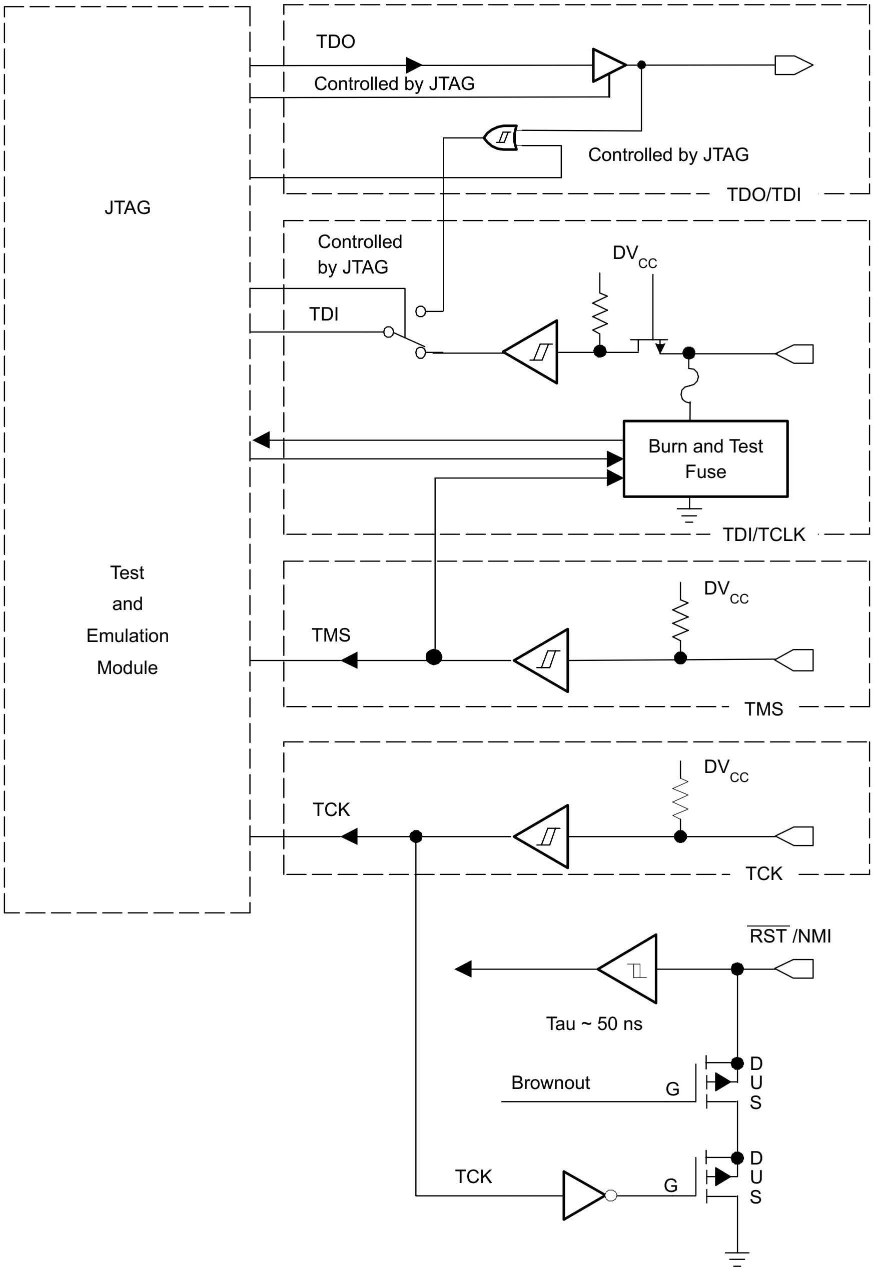


Figure 6-15. JTAG Pins Diagram

6.10.7 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Take care to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-16). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

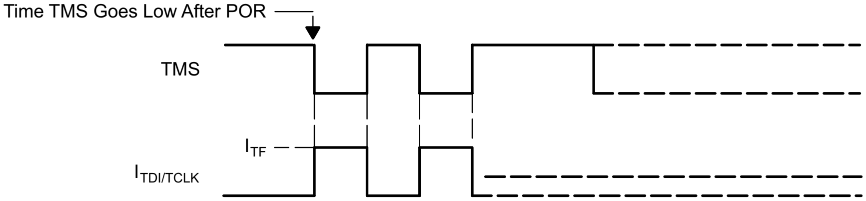


Figure 6-16. Fuse Check Mode Current

7 デバイスおよびドキュメントのサポート

7.1 使い始めと次の手順

MSP430ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「使い始め」ページを参照してください。

7.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP430 MCUデバイスとサポート・ツールのすべての型番に接頭辞が割り当てられています。MSP430 MCU商用ファミリの各番号には、MSP、PMS、XMSのいずれかの接頭辞があります。TIでは、サポート・ツールに使用可能な3つの接頭辞指定子のうち、MSPおよびMSPXの2つを推奨しています。これらの接頭辞は、エンジニアリング・プロトタイプ(デバイスではXMS、ツールではMSPX)から、完全に認定済みの量産版デバイスとツール(デバイスではMSP、ツールではMSP)まで、製品開発の段階を表しています。

デバイス開発の段階は次のとおりです。

XMS - 実験段階のデバイスで、デバイスの最終的な電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

サポート・ツール開発の段階は次のとおりです。

MSPX - TIの社内認定テストが完了していない開発サポート製品です。

MSP - 完全に認定済みの開発サポート製品です。

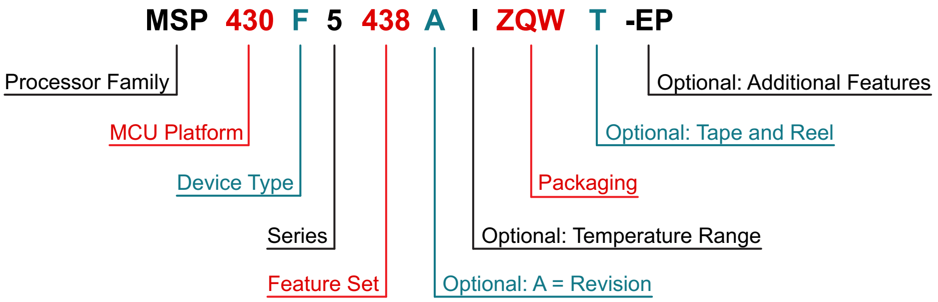
XMSデバイスとMSPX開発サポート・ツールは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスとMSP開発サポート・ツールの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは予測される最終使用時の故障率が未定義であるため、TIではそれらのデバイスを量産システムで使用しないよう推奨しています。認定された製品デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、パッケージの種類(例: PZP)と温度範囲(例: T)を示しています。図 7-1に、任意のファミリ・メンバについて、完全なデバイス名を読み取るための凡例を示します。



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BT = Preprogrammed with *Bluetooth* BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz with LCD	5 Series = Up to 25 MHz 6 Series = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various Levels of Integration Within a Series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small Reel R = Large Reel No Markings = Tube or Tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

NOTE: この図は利用可能な機能とオプションのすべてをリストアップしたものではありません。上記の機能とオプションのすべてが、特定のデバイスまたはファミリで利用可能なことを示すものでもありません。

図 7-1. デバイスの項目表記 - 型番の読み方

7.3 ツールとソフトウェア

表 7-1 に、MSP430F42xマイクロコントローラで対応しているデバッグ機能一覧を示します。利用可能な機能の詳細については、『*MSP430用Code Composer Studio ユーザー・ガイド*』を参照してください。

表 7-1. ハードウェアの特長

MSP430アーキテクチャ	4線式JTAG	2線式JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ
MSP430	○	×	3	なし	グローバル	×	×

設計キットと評価モジュール

64ピン・ターゲット開発ボードとMSP-FETプログラマ・バンドル - MSP430F1x、MSP430F2x、MSP430F4x MCU MSP-FET430U64 は、強力なフラッシュ・エミュレーション・ツールで、MSP430 MCU 向けのアプリケーション開発をすぐに開始するために必要なすべてのハードウェアとソフトウェアが含まれています。この中には、ZIFソケット・ターゲット・ボード（MSP-TS430PM64）とUSBデバッグ・インターフェイス(MSP-FET)が含まれており、JTAGインターフェイス、またはピンを削減できるSpy-Bi-Wire (2線式のJTAG)プロトコルによる、イン・システムでのMSP430のプログラムとデバッグに使用できます。フラッシュ・メモリは、数回のキー操作により、数秒でプログラムまたは消去できます。また、MSP430の超低消費電力フラッシュが搭載されているので、外部電源は不要です。

MSP-TS430PM64 - MSP430F1x MCUとMSP430F2x MCUとMSP430F4xMCUの64ピン・ターゲット開発ボード MSP-TS430PW64はスタンドアロンのZIFソケット・ターゲット・ボードで、JTAGインターフェイスまたはSpy Bi-Wire (2線式JTAG)プロトコルによるMSP430 MCUイン・システムのプログラムとデバッグに使用できます。

ソフトウェア

MSP430x41x、MSP430F42xのサンプル・コード C サンプル・コードは、各種のアプリケーションで使用するそれぞれのペリフェラルを設定します。またすべての MSP デバイスで使用できます。

静電容量式タッチパッド・ソフトウェア・ライブラリ MSP430 MCU上で静電容量式タッチパッド機能を有効にする、無償のCライブラリです。MSP430 MCUバージョンのライブラリには、ROおよびRC方式を含む、いくつかの静電容量式タッチ機能の実装が含まれています。

MSPWareソフトウェア MSPWareソフトウェアは、すべてのMSPデバイス向けのサンプル・コード、データシート、その他の設計リソースを1つの便利なパッケージにまとめたものです。既存のMSP用設計リソースの完全なコレクションに加えて、MSPWareソフトウェアにはMSPドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSPハードウェアを簡単にプログラムできます。MSPWareソフトウェアはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSPドライバ・ライブラリ MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTraceテクノロジ MSP430マイクロコントローラ用のEnergyTraceテクノロジは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するのに役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSPの低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

MSP-GANG量産プログラマ MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8 つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホストPC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

7.4 ドキュメントのサポート

以下のドキュメントには、MSP430F42x MCU についての解説が記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いのデバイスの製品フォルダへ移動します(製品フォルダへのリンクについては、7.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430F427デバイス正誤表』 このデバイスにおける各シリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

『MSP430F425デバイス正誤表』 このデバイスにおける各シリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

『MSP430F423デバイス正誤表』 このデバイスにおける各シリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

ユーザー・ガイド

『MSP430x4xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なモジュールとペリフェラルについての詳細な説明です。

『MSP430用Code Composer Studio v6.1 ユーザー・ガイド』 このマニュアルは、TI Code Composer Studio IDE v6.1 (CCS v6.1)をMSP430超低消費電力マイクロコントローラで使用する方法について解説しています。このマニュアルはCode Composer Studio IDEの Windows®バージョンのみを対象とします。Linux®バージョンの内容はほぼ同じであるため、別の記載はありません。

『MSP430用IAR Embedded Workbenchバージョン3+ ユーザー・ガイド』 このマニュアルは、IAR Embedded Workbench (EW430)をMSP430超低消費電力マイクロコントローラで使用する方法について解説しています。

『ブートローダ(BSL)によるMSP430のプログラミング』 MSP430ブートローダ(BSL、従来の名前はブートストラップ・ローダ)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430マイクロコントローラの組み込みメモリと通信を行うことができます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『MSP430 32kHz水晶発振器』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のため重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

『MSP430とセグメントLCDを用いた設計』 セグメント液晶ディスプレイ(LCD)は、スマート・メーターから電子棚札(ESL)、医療機器に至る広範なアプリケーションで、ユーザーに情報を提供するために必要です。MSP430™マイクロコントローラ・ファミリの中には、低電力のLCDドライバ回路を内蔵し、MSP430 MCUでセグメントLCDガラスを直接制御できるものもあります。このアプリケーション・ノートは以下の項目の補助的な説明を記載しています。セグメントLCDの動作、MSP430 MCUファミリにおける各種LCDモジュールの様々な機能、LCDハードウェアをレイアウトするコツ、効率的で使いやすいLCDドライバ・ソフトウェアの書き方のガイド、デバイス選択に役立つ、様々なLCD機能を含んだMSP430デバイスの製品ラインの概要。

『MSP430フラッシュ・データ保持の理解』 幅広い製品ラインの一部であるMSP430マイクロコントローラ・ファミリには、読み取り専用メモリ(ROM)ベースおよびフラッシュ・ベース両方のデバイスがあります。MSP430フラッシュを理解することは、効率的で堅牢、かつ信頼できるシステムを設計するのに極めて重要です。データ保持は、フラッシュの信頼性という主要な性質の1つです。このアプリケーション・レポートでは、MSP430フラッシュのデータ保持について詳細に検討され、温度の影響が最重要とされています。

『3V MSP430と5V回路とのインターフェイス』 3V MSP430x1xxおよびMSP430x4xxマイクロコントローラ・ファミリと5V以上の電源電圧とのインターフェイスを提示します。入力、出力、およびI/Oインターフェイスを示し、説明します。必要に応じて、ワーストケースの設計式を示しています。両方の電圧を生成するシンプルな電源もいくつか示します。

『MSP430を使用した効率的な乗除』 ハードウェア・マルチプライヤがない場合、乗除演算で多数の命令サイクルが必要になります(特にC言語の場合)。このレポートでは、ハードウェア・マルチプライヤを必要とせず、シフトと加算命令のみで乗除演算を可能とする手法について検討します。このアプリケーション・レポートで説明される手法は、ホーナー法に基づきます。

7.5 関連リンク

表 7-2に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7-2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430F427	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F425	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F423	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 商標

MSP430, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.
Linux is a registered trademark of Linus Torvalds.
Windows is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

7.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 用語集

TI 用語集	この用語集には、用語や略語の一覧および定義が記載されています。

8 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F423IPM	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F423
MSP430F423IPM.B	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F423
MSP430F423IPMR	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F423
MSP430F423IPMR.B	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F423
MSP430F425IPM	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F425
MSP430F425IPM.B	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F425
MSP430F425IPMR	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F425
MSP430F425IPMR.B	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F425
MSP430F427IPM	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F427
MSP430F427IPM.B	NRND	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F427
MSP430F427IPMR	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F427
MSP430F427IPMR.B	NRND	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F427

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

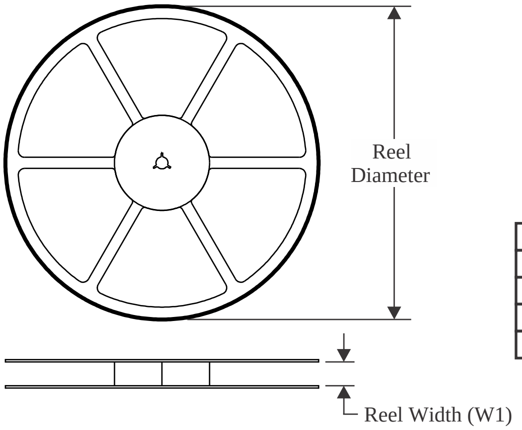
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

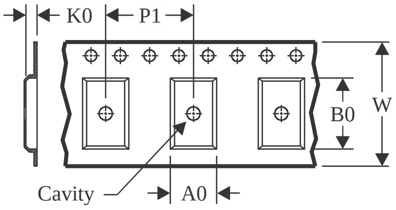
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

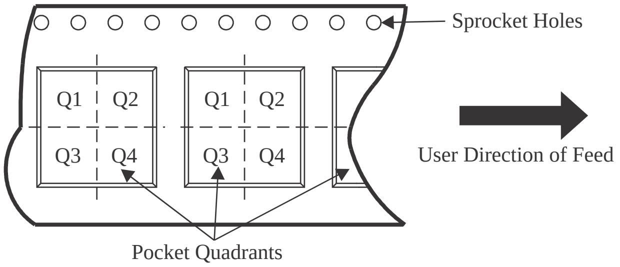


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

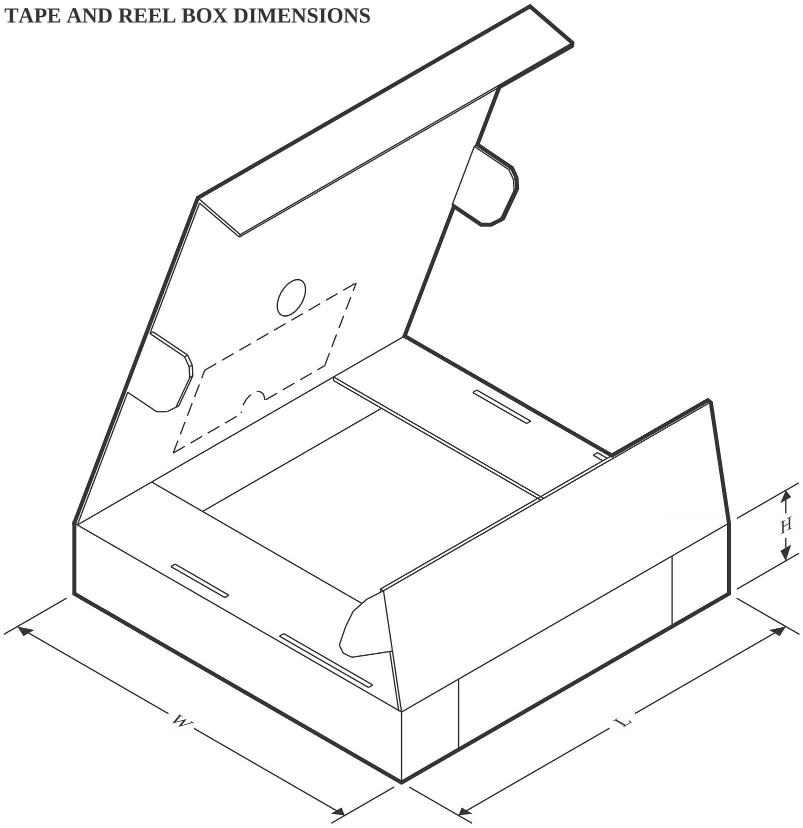
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F423IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F425IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F427IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

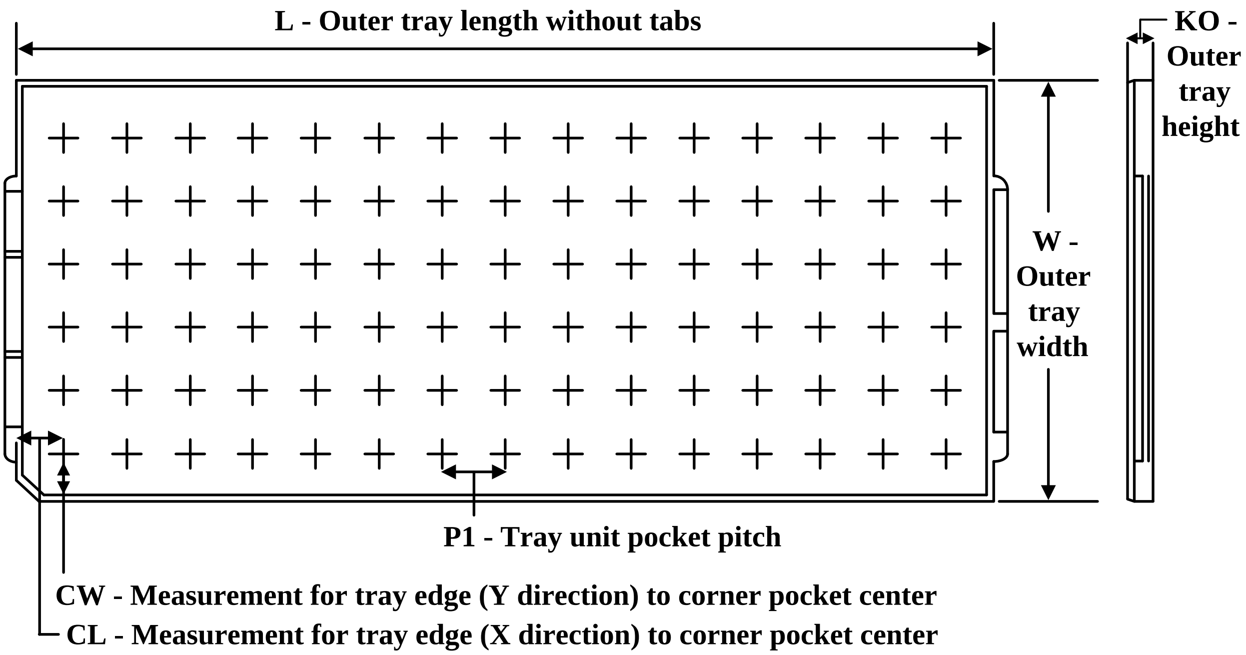
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F423IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F425IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F427IPMR	LQFP	PM	64	1000	336.6	336.6	41.3

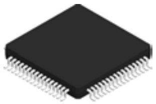
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F423IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F423IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F423IPM.B	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F423IPM.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F425IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F425IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F425IPM.B	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F425IPM.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F427IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F427IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F427IPM.B	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F427IPM.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

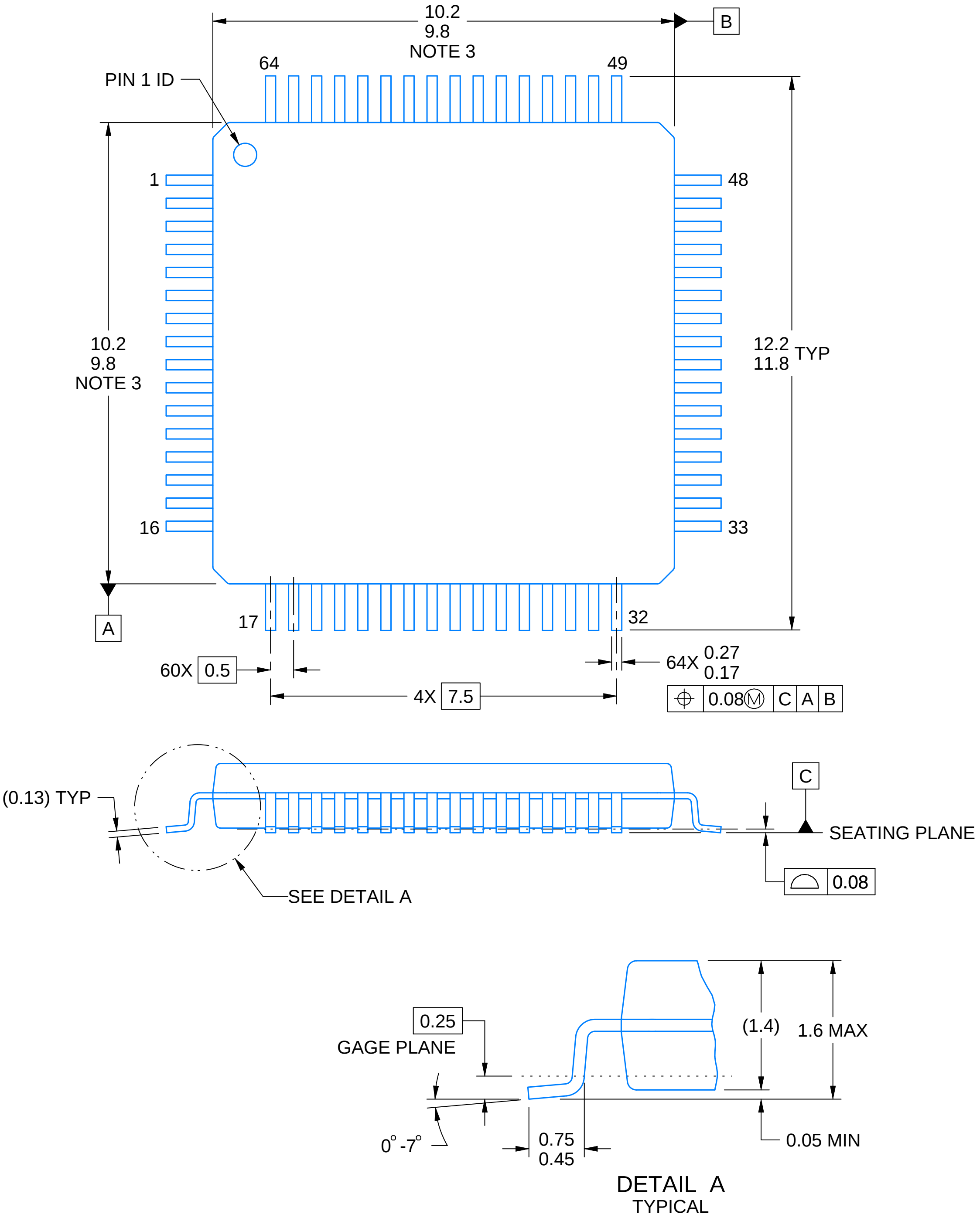


PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

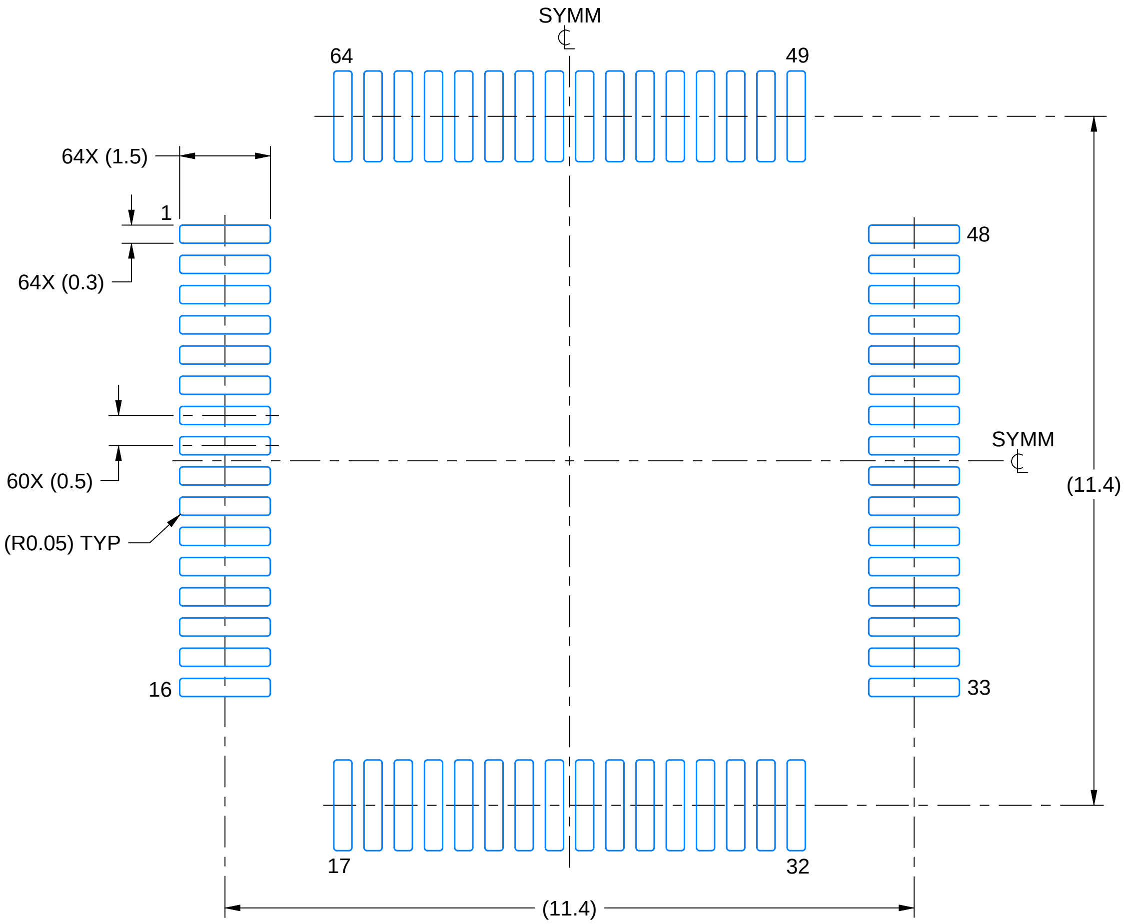
PLASTIC QUAD FLATPACK



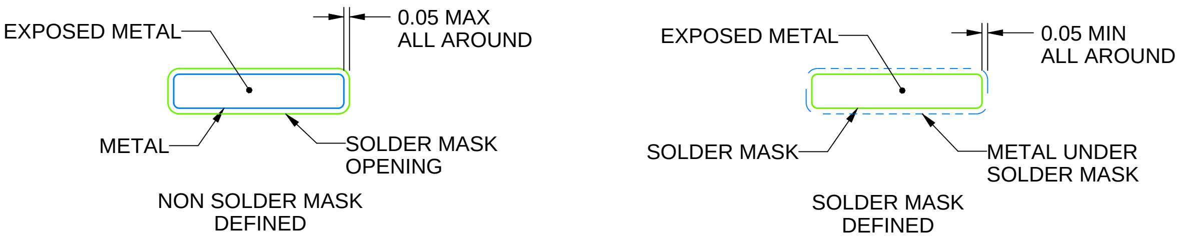
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

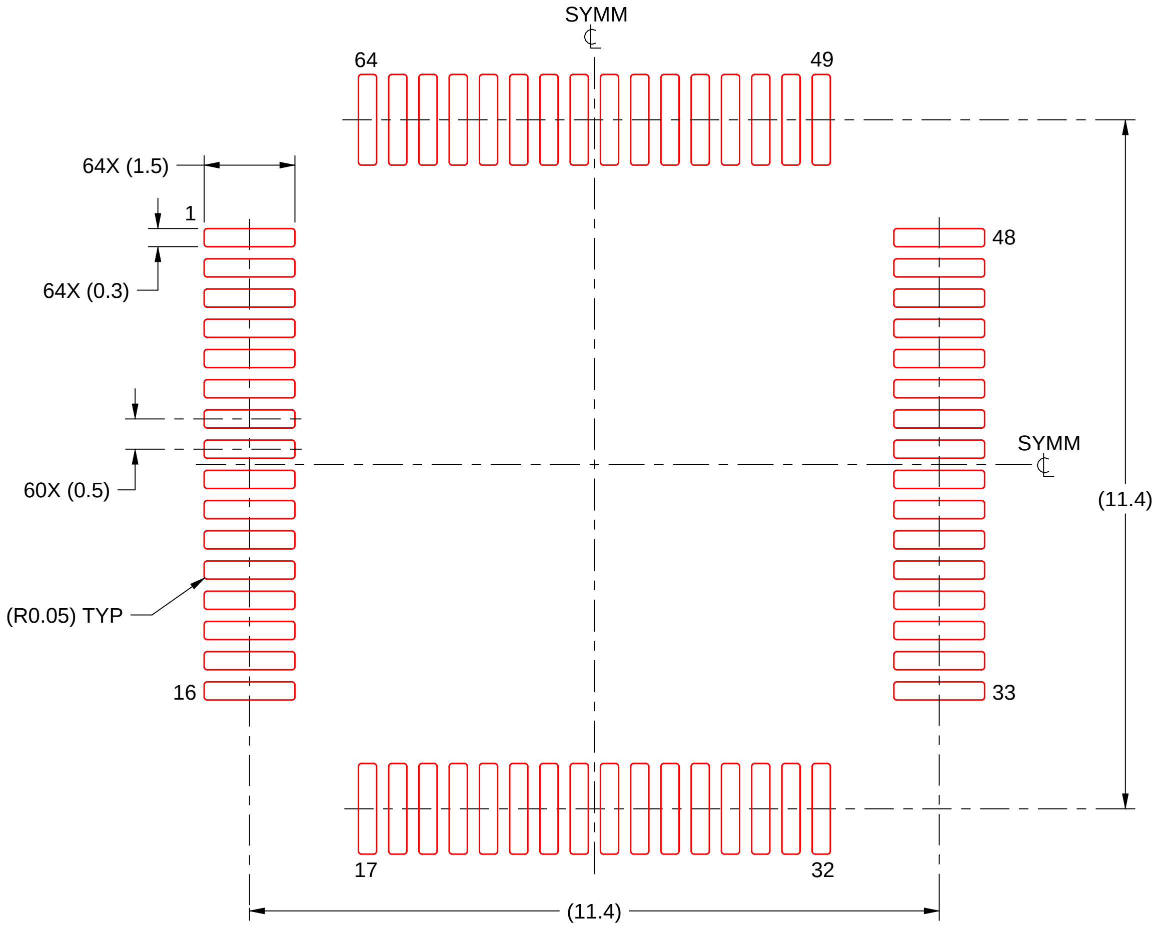


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス･インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス･インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス･インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス･インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス･インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス･インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス･インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス･インスツルメンツは一切の責任を拒否します。

テキサス･インスツルメンツの製品は、 テキサス･インスツルメンツの販売条件、または ti.com やかかる テキサス･インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス･インスツルメンツがこれらのリソースを提供することは、適用される テキサス･インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス･インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265