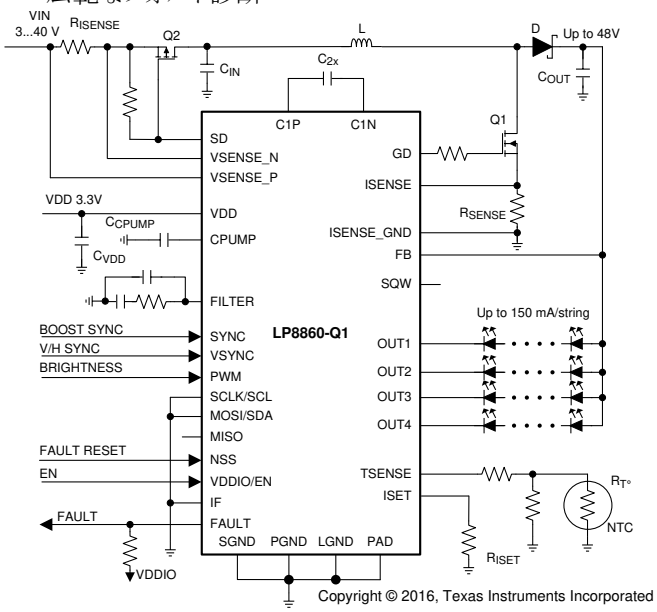
LP8860-Q1 低 EMI 車載 LED ドライバ、150mA チャネル

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40°C ～ +125°C の動作時周囲温度
- 入力電圧動作範囲:3V～48V
- 4 つの高精度電流シンク
  - 電流マッチング 0.5% (標準値)
  - チャネルごとに最大 150mA の LED ストリング電流
  - 外部の PWM 輝度制御機能を使用し、13 000:1 を上回る調光比
  - SPI または I²C による 16 ビット調光制御
  - ディスプレイ モード (グローバル調光) とクラスタ モード (独立調光) をサポート
- LED 駆動の光効率の向上に役立つハイブリッド PWM 調光と電流調光機能
- LED PWM 周波数の同期
- スイッチング周波数を 100kHz ～ 2.2MHz にプログラム可能な昇圧コントローラと、拡散スペクトラム オプションにより EMI を低減
- 昇圧同期入力
- パワー ライン FET 制御により、突入電流に対する保護とスタンバイ電力の削減
- 外部温度センサにより、自動的に LED 電流を低減
- 広範なフォルト診断



概略回路図

2 アプリケーション

- 次の応用でのバックライト:
  - 車載インフォテインメント
  - 車載用計器盤
  - スマート ミラー
  - ヘッドアップ ディスプレイ (HUD)
  - 集中情報ディスプレイ (CID)
  - オーディオ ビデオ ナビゲーション (AVN)

3 説明

LP8860-Q1 は、昇圧コントローラを搭載した車載用高効率 LED ドライバです。4 つの高精度電流シンクが内蔵されており、PWM 入力信号、SPI または I²C マスタ、または両方で制御可能です。

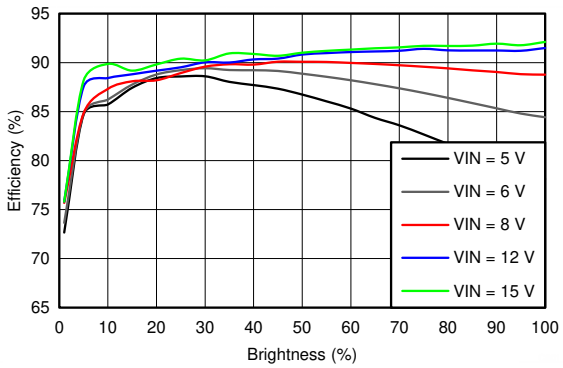
この昇圧コンバータは、LED 電流シンクのヘッドルーム電圧に基づいた適応型出力電圧制御機能を備えています。この機能により、すべての条件で、必要最低限のレベルに電圧昇圧を調整することで消費電力を最小化できます。周波数を広範囲に調整可能なため、LP8860-Q1 は AM ラジオ周波数帯の妨害を回避できます。

LP8860-Q1 は組み込みのハイブリッド PWM と電流調光をサポートしているため、EMI の削減、LED の寿命の延長、総合的な光学効率の向上を実現できます。フェーズシフト PWM により、可聴範囲のノイズと出力リップルが減少します。

デバイス情報 (1)

部品番号	パッケージ	本体サイズ (公称)
LP8860-Q1	HLQFP (32)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



システム効率

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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Device Comparison Table

	LP8860-Q1	LP8862-Q1	LP8861-Q1	TPS61193-Q1	TPS61194-Q1	TPS61196-Q1
VIN range	3V to 48V	4.5V to 45V	4.5V to 45V	4.5V to 45V	4.5V to 45V	8V to 30V
Number of LED channels	4	2	4	3	4	6
LED current / channel	150mA	160mA	100mA	100mA	100mA	200mA
I2C/SPI support	Yes	No	No	No	No	No
SEPIC support	No	Yes	Yes	Yes	Yes	No

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4 Pin Configuration and Functions

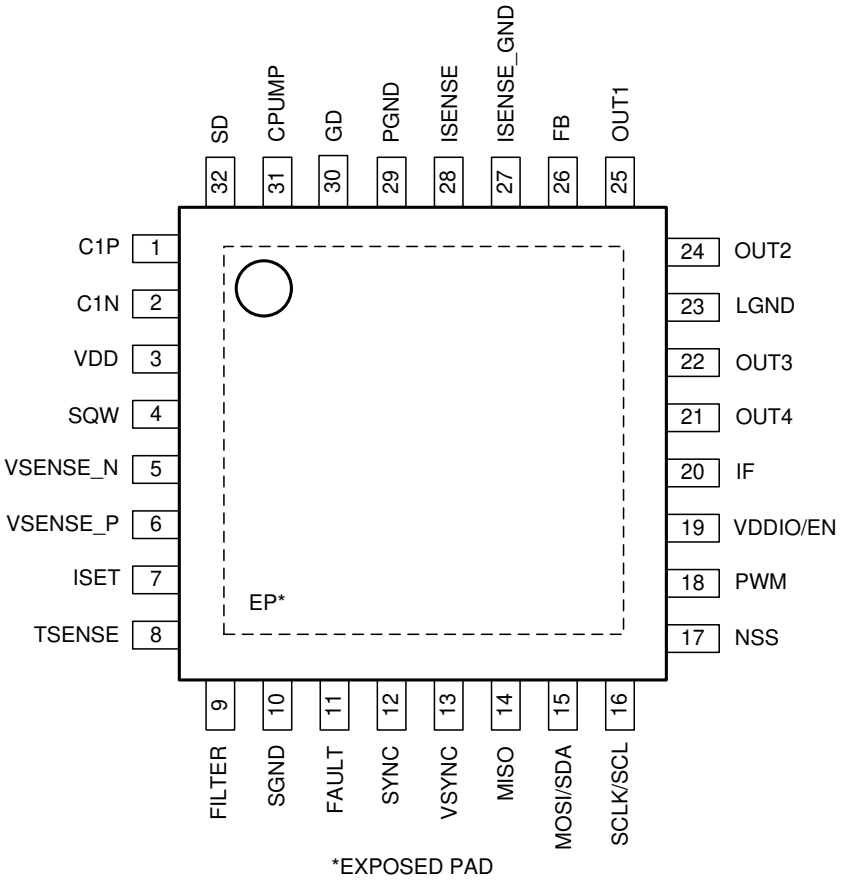

図 4-1. VFP Package 32-Lead PowerPAD™ Quad Flatpack S-PQFP-G32 Top View

Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NUM	NAME		
1	C1P	A	Positive pin for charge pump flying capacitor. If feature is disabled, the pin may be left floating.
2	C1N	A	Negative pin for charge pump flying capacitor. If feature is disabled, the pin may be left floating.
3	VDD	P	Input voltage pin for internal circuit.
4	SQW	A	Square wave output. Can be used for generating extra voltage rail. If unused, the pin may be left floating.
5	VSENSE_N	A	Pin for input current sense.
6	VSENSE_P	A	Pin for OVP/UVLO protection and input current sense.
7	ISET	A	Optional resistor for setting LED maximum current. If feature is disabled, the pin may be left floating.
8	TSENSE	A	External temperature sensor for LED current control. If feature is disabled, the pin may be left floating.
9	FILTER	A	Low pass filter for PLL. If feature is disabled, the pin may be left floating.
10	SGND	G	Signal ground.
11	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
12	SYNC	I	Input for synchronizing boost. This pin must be connected to GND if not used.
13	VSYNC	I	Input for synchronizing PWM generation to display refresh. This pin must be connected to GND if feature is disabled.
14	MISO	O	Slave data output (SPI). If unused, the pin may be left floating.
15	MOSI/SDA	I/O	Slave data input (SPI) or serial data (I^2C). This pin must be connected to GND if not used.
16	SCLK/SCL	I	Serial clock for SPI or I^2C. This pin must be connected to GND if not used.
17	NSS	I	Slave select (SPI mode) or fault reset (I^2C or standalone mode). This pin must be connected to GND if not used.
18	PWM	I	PWM dimming input. This pin must be connected to GND if feature is disabled.
19	VDDIO/EN	I	Enable input pin and reference voltage for digital pins.
20	IF	I	Interface selection: low – I^2C or standalone mode; high – SPI.
21	OUT4	A	LED current sink output. If unused, the pin may be left floating.
22	OUT3	A	LED current sink output. If unused, the pin may be left floating.
23	LGND	G	LED current ground.
24	OUT2	A	LED current sink output. If unused, the pin may be left floating.
25	OUT1	A	LED current sink output. If unused, the pin may be left floating.
26	FB	A	Boost feedback input.
27	ISENSE_GND	A	Boost controller's current sense resistor GND.
28	ISENSE	A	Boost current sense pin.
29	PGND	G	Power ground.
30	GD	A	Gate driver output for boost FET.
31	CPUMP	P	Charge pump output pin.
32	SD	A	Power line FET control. If unused, the pin may be left floating.

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1] [2]

	MIN	MAX	UNIT
Voltage on pins VSENSE_N, VSENSE_P, OUT1 to OUT4, FB, SD	–0.3	52	V
Voltage on pins VDD, FILTER, SYNC, VSYNC, PWM, SCLK/SCL, MOSI/SDA, MISO, NSS, VDDIO/EN, IF, ISENSE, ISENSE_GND, FAULT, ISET, TSENSE, C1N	–0.3	6	V
Voltage on pins C1P, CPUMP, GD, SQW	–0.3	12	V
Continuous power dissipation[3]	Internally Limited		
Ambient temperature, T_A [4]	–40	125	°C
Junction temperature, T_J [4]	–40	150	°C
Maximum lead temperature (soldering)		See[5]	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 135°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 150°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.
(5) For detailed soldering specifications and information, refer to *PowerPAD™ Thermally Enhanced Package Application Note* .

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±500	
		Corner pins (1,8,9,16,17,24,25,32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Voltage on pins VSENSE_N, VSENSE_P	3	48	V
VDD input voltage	3	5.5	V
VDDIO/EN input voltage	1.65	VDD	V
Voltage on pins FILTER, ISENSE, ISENSE_GND, ISET, TSENSE, C1N	0	5.5	V
FAULT, PWM, SCLK/SCL, MOSI/SDA, NSS, IF, SYNC, MISO, VSYNC	0	VDDIO	V
Voltage on pins C1P, CPUMP, GD, SQW	0	11	V
Voltage on pins OUT1 to OUT4, FB, SD	0	48	V

(1) All voltages are with respect to the potential at the GND pins.

5.4 Thermal Information

THERMAL METRIC[1]		LP8860 HLQFP PowerPAD (VLP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	36.0	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

5.5 Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).[1] [2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_Q	Shutdown supply current for VDD	Device disabled, VDDIO/EN = 0V		1	5	µA
	Active supply current for VDD, VDD = 5V	Backlight enabled (no load), boost enabled, PLL and CP disabled, DRV_LED_BIAS_CTRL[1:0] = 10 , boost f_{SW} = 300kHz		2.5	6	mA
		Backlight enabled (no load), boost enabled, CP disabled, f_{PLL} = 10MHz, DRV_LED_BIAS_CTRL[1:0] = 11, boost f_{SW} = 400kHz		4.5	15	
$V_{VDD_POR_R}$	Power-on reset rising threshold				2.2	V
$V_{VDD_POR_F}$	Power-on reset falling threshold		1.1			
T_{TSD}	Thermal shutdown threshold		150	165	180	°C
T_{TSD_THR}	Thermal shutdown hysteresis			30		
INTERNAL OSCILLATOR						
f_{OSC}	Frequency			10		MHz
	Frequency accuracy		–7%		7%	

(1) All voltages are with respect to the potential at the GND pins.
(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis.

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5.6 Current Sinks Electrical Characteristics

Limits apply over the full ambient temperature range –40°C ≤ T_A ≤ +125°C. Unless otherwise specified: V_{DD} = 3.3V, V_{IN} = 12V, EN/VDDIO = 3.3V, L = 22µH, C_{IN} = 2 × 10µF ceramic and 33µF electrolytic, C_{OUT} = 2 × 10µF ceramic and 33µF electrolytic, C_{VDD} = 1µF, C_{CPUMP} = 10µF, Q = IPD25N06S4L-30-ND, D = SS5P10-M3/86A.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT4, V_{OUT} = 48V		0.1	1	µA
I_{MAX}	Maximum source current	OUT1 to OUT4		150		mA
I_{OUT}	Output current accuracy	I_{OUT} = 150mA	−3%		3%	
I_{MATCH}	Output current matching(1)	I_{OUT} = 150mA, 100% brightness		0.5%	2%	
f_{LED_PWM}	LED PWM output frequency for display mode	PWM_FREQ[3:0] = 0000b PWM_FREQ[3:0] = 1111b		4883 39 063		Hz
f_{PWM}	PWM input frequency	BRT_MODE[1:0] = 00, 01 and 10	100		500	Hz
$t_{PWM\ MIN}$	Minimum on and off time for PWM input			400		ns
I_{DIM}	Dimming ratio (input resolution)	External 100 Hz PWM	13 000:1			
		SPI or I^2C control		16		bit
PWM_{RES}	PWM output resolution, PWM control for BRT_MODE[1:0] = 00, 01, and 10 (without dithering)	f_{LED_PWM} = 5kHz, f_{OSC} = 5MHz		10		bits
		f_{LED_PWM}= 10kHz, f_{OSC} = 5MHz		9		
		f_{LED_PWM} = 20kHz, f_{OSC} = 5MHz		8		
		f_{LED_PWM} = 40kHz, f_{OSC} = 5MHz		7		
		f_{LED_PWM} = 5kHz, f_{OSC} = 40MHz		13		
		f_{LED_PWM} = 10kHz, f_{OSC} = 40MHz		12		
		f_{LED_PWM} = 20kHz, f_{OSC} = 40MHz		11		
		f_{LED_PWM} = 40kHz, f_{OSC} = 40MHz		10		
ΔI_{OUT}	Individual output current adjustment range	DRV_OUTx_CORR[3:0] = 1111		–7.4%		
		DRV_OUTx_CORR[3:0] = 0000		6.5%		
V_{SAT}	Saturation voltage(2)	I_{OUT} = 150mA		0.5	0.75	V
$V_{SHORT_FAULT_THR}$	LED short detection threshold	DRV_LED_FAULT_THR[1:0] = 00		3.6		V
		DRV_LED_FAULT_THR[1:0] = 01		3.6		
		DRV_LED_FAULT_THR[1:0] = 10		6.9		
		DRV_LED_FAULT_THR[1:0] = 11		10.6		

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT4), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.

(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1V.

5.7 Boost Converter Characteristics

Limits apply over the full ambient temperature range – 40°C ≤ T_A ≤ +125°C. Unless otherwise specified: V_{DD} = 3.3V, V_{IN} = 12V, EN/VDDIO = 3.3V, L = 22µH, C_{IN} = 2 × 10µF ceramic and 33µF electrolytic, C_{OUT} = 2 × 10µF ceramic and 33µF electrolytic, C_{VDD} = 1µF, C_{CPUMP} = 10µF, Q = IPD25N06S4L-30-ND, D = SS5P10-M3/86A.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LOAD}	Maximum continuous load current	V_{IN} = 6V, V_{BOOST} = 48V (f_{SW} = 303kHz)	600			mA
		V_{IN} = 3V, V_{BOOST} = 30V (f_{SW} = 1.1MHz)	150			
		V_{IN} = 3V, V_{BOOST} = 30V (f_{SW} = 2.2MHz)	100			
V_{OUT}/V_{IN}	Conversion ratio				10	
f_{SW}	Switching frequency (central frequency if spread spectrum is enabled)	BOOST_FREQ = 000 BOOST_FREQ = 001 BOOST_FREQ = 010 BOOST_FREQ = 011 BOOST_FREQ = 100 BOOST_FREQ = 101 BOOST_FREQ = 110 BOOST_FREQ = 111	–7%	100 200 303 400 629 800 1100 2200	7%	kHz
$t_{BOOST\ START\text{-}UP}$	Start-up time (1)			50		ms
I_{MAX}	SW current limit	R_{SENSE} = 25mΩ				A
		BOOST_IMAX_SEL=000 BOOST_IMAX_SEL=001 BOOST_IMAX_SEL=010 BOOST_IMAX_SEL=011 BOOST_IMAX_SEL=100 BOOST_IMAX_SEL=101 BOOST_IMAX_SEL=110 BOOST_IMAX_SEL=111		2 3 4 5 6 7 8 9		
V_{GD}	Gate driver output voltage		0		11	V
$I_{GD_SOURCE_PEAK}$	Gate driver peak current, sourcing	BOOST_DRIVER_SIZE[1:0] = 11 BOOST_GD_VOLT = 1 V_{DD}= 5V, V_{CPUMP} = 10V FET SQ4850EY		1.7		A
$I_{GD_SINK_PEAK}$	Gate driver peak current, sinking			1.5		

(1) Start-up time is measured from the moment the boost is activated until the V_{OUT} crosses 90% of its initial voltage value.

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5.8 Logic Interface Characteristics

VDDIO/EN = 1.65V to V_{DD}, V_{DD} = 3.3V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
I_I	Input current		−1		1	µA
LOGIC INPUT SYNC, VSYNC, PWM, SCLK/SCL, MOSI/SDA, NSS, IF						
V_{IL}	Input low level				0.2 × VDDIO/EN	V
V_{IH}	Input high level		0.8 × VDDIO/EN			
I_I	Input current		−1		1	µA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	I = 3mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5V			1	µA
LOGIC OUTPUT MISO						
V_{OL}	Output low level	I_{OUT} = 3mA		0.3	0.5	V
V_{OH}	Output high level	I_{OUT} = –2mA	0.7 × VDDIO/EN	0.9 × VDDIO/EN		
I_L	Output leakage current				1	µA
LOGIC OUTPUTS SDA						
V_{OL}	Output low level	I = 3mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5V			1	µA

5.9 V_{IN} Undervoltage Protection (VIN_UVLO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	V_{IN} UVLO threshold voltage	UVLO[1:0] = 00		Disabled		V
		UVLO[1:0] = 01	2.64	3	3.36	
		UVLO[1:0] = 10	4.4	5	5.6	
		UVLO[1:0] = 11	7.04	8	8.96	

5.10 V_{DD} Undervoltage Protection (VDD_UVLO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDD_UVLO}	V_{DD} UVLO threshold voltage	VDD_UVLO_LEVEL = 0		2.5		V
		VDD_UVLO_LEVEL = 1		3		
V_{HYST}	V_{DD} UVLO hysteresis			50		mV

5.11 V_{IN} Overvoltage Protection (VIN_OVP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	V_{IN} OVP threshold voltage	OVP[1:0] = 00		Disabled		V
		OVP[1:0] = 01	6.16	7	7.84	
		OVP[1:0] = 10	9.68	11	12.32	
		OVP[1:0] = 11	19.8	22.5	25.2	

5.12 V_{IN} Overcurrent Protection (VIN_OCP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCP}	V_{IN} current protection limit with R_{ISENSE} = 20 mΩ, V_{IN} = 12 V See[(1)]	PL_SD_LEVEL[1:0] = 10		6		A
		PL_SD_LEVEL[1:0] = 11		8		

(1) Refer to *Selecting Current Sensing Resistor for LP8860-Q1 Power Input* application note.

5.13 Power-Line FET Control Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L,VSENSE_P}$	VSENSE_P pin leakage current	V_{SENSE_P} = 48 V		0.1	3	µA
$I_{L,VSENSE_N}$	VSENSE_N pin leakage current	V_{SENSE_N} = 48 V				
$I_{L,SD}$	SD pin leakage current	V_{SD} = 48 V				
$I_{SD\ PFET}$	Pulldown current for power-line p-FET, NMOS_PLFET_EN=0	PL_SD_SINK_LEVEL = 00 PL_SD_SINK_LEVEL = 01 PL_SD_SINK_LEVEL = 10 PL_SD_SINK_LEVEL = 11		55 110 220 440		µA

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5.14 External Temp Sensor Control Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TEMP_HIGH}	T_{SENSE} high level resistance value	EXT_TEMP_LEVEL_HIGH[3:0] = 0000		79.67		kΩ
		EXT_TEMP_LEVEL_HIGH[3:0] = 0001		43.35		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0010		29.77		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0011		22.67		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0100		18.30		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0101		15.34		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0110		13.21		
		EXT_TEMP_LEVEL_HIGH[3:0] = 0111		11.60		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1000		10.34		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1001		9.32		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1010		8.49		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1011		7.79		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1100		7.20		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1101		6.69		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1110		6.25		
		EXT_TEMP_LEVEL_HIGH[3:0] = 1111		5.87		
R_{TEMP_LOW}	TSENSE low-level resistance value	EXT_TEMP_LEVEL_LOW[3:0] = 0000		79.67		kΩ
		EXT_TEMP_LEVEL_LOW[3:0] = 0001		43.35		
		EXT_TEMP_LEVEL_LOW[3:0] = 0010		29.77		
		EXT_TEMP_LEVEL_LOW[3:0] = 0011		22.67		
		EXT_TEMP_LEVEL_LOW[3:0] = 0100		18.30		
		EXT_TEMP_LEVEL_LOW[3:0] = 0101		15.34		
		EXT_TEMP_LEVEL_LOW[3:0] = 0110		13.21		
		EXT_TEMP_LEVEL_LOW[3:0] = 0111		11.60		
		EXT_TEMP_LEVEL_LOW[3:0] = 1000		10.34		
		EXT_TEMP_LEVEL_LOW[3:0] = 1001		9.32		
		EXT_TEMP_LEVEL_LOW[3:0] = 1010		8.49		
		EXT_TEMP_LEVEL_LOW[3:0] = 1011		7.79		
		EXT_TEMP_LEVEL_LOW[3:0] = 1100		7.20		
		EXT_TEMP_LEVEL_LOW[3:0] = 1101		6.69		
		EXT_TEMP_LEVEL_LOW[3:0] = 1110		6.25		
		EXT_TEMP_LEVEL_LOW[3:0] = 1111		5.87		
R_{TS_FLOAT}	T_{SENSE} maximum resistance (missing resistor fault value)			2		MΩ

5.15 I²C Serial Bus Timing Parameters (SDA, SCLK)

See 図 5-1.

		MIN	NOM	MAX	UNIT
f_{SCLK}	Clock frequency			400	kHz
1	Hold time (repeated) START Condition	0.6			µs
2	Clock low time	1.3		25000	µs
3	Clock high time	600			ns
4	Set-up time for a repeated START condition	600			ns
5	Data hold time	50			ns
6	Data setup time	100			ns
7	Rise Time of SDA and SCL	$20+0.1xC_b$		300	ns
8	Fall Time of SDA and SCL	$15+0.1xC_b$		300	ns
9	Set-up time for STOP condition	600			ns
10	Bus free time between a STOP and a START Condition	1.3			µs
C_b	Capacitive load parameter for each bus line load of 1pF corresponds to 1ns.	10		200	ns

5.16 SPI Timing Requirements

See 図 5-2.

		MIN	NOM	MAX	UNIT
1	Cycle time	70			ns
2	Enable lead time	35			ns
3	Enable lag time	35			ns
4	Clock low time	35			ns
5	Clock high time	35			ns
6	Data setup time	20			ns
7	Data hold time	20			ns
8	Disable time			10	ns
9	Data valid			29	ns
10	NSS inactive time	700			ns
C_b	Bus capacitance	5		40	pF

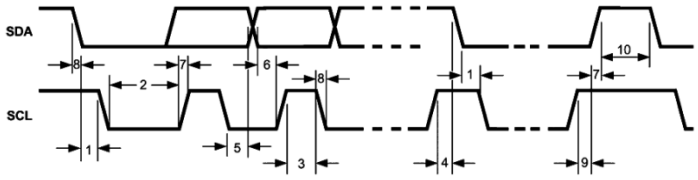

図 5-1. I²C Timing

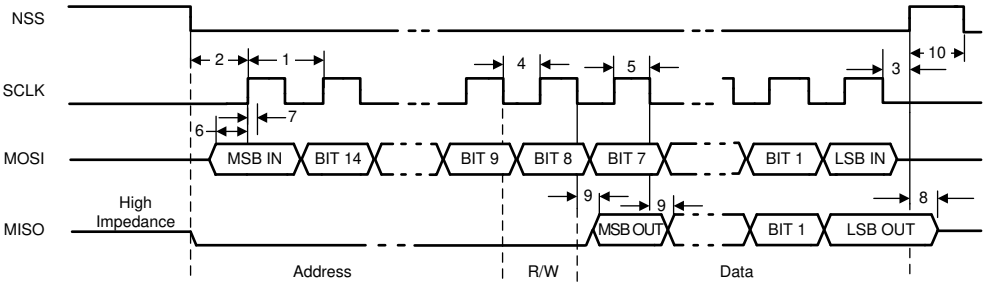

図 5-2. SPI Timing Diagram

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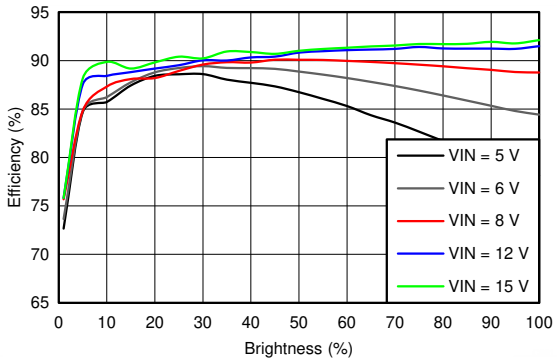
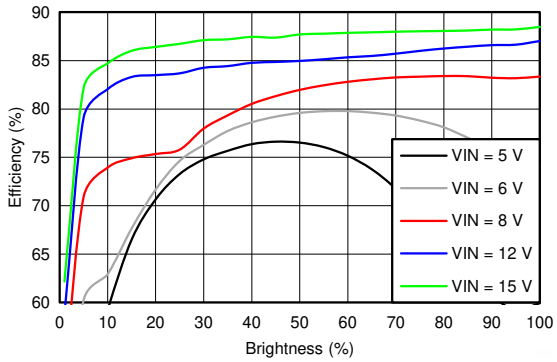
5.17 Typical Characteristics

Unless otherwise specified: L= 22µH (IHLP-5050FDER220M5A), C_{IN} = 2 × 10µF ceramic and 33µF electrolytic, C_{OUT} = 2 × 10µF ceramic and 33µF electrolytic, Q = IPD25N06S4L-30-ND, D = SS5P10-M3/86A, V_{DD} = 5V, charge pump disabled, T = 25°C



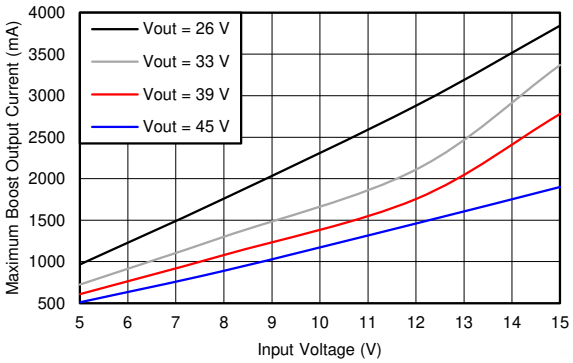
f_{SW} = 303kHz 8 LEDs/string 150mA/string
4 strings

図 5-3. System Efficiency



f_{SW} = 2.2MHz 8 LEDs/string 100mA/string
4 strings

図 5-4. System Efficiency



f_{SW} = 303kHz Adaptive voltage control off

図 5-5. Boost Maximum Output Current

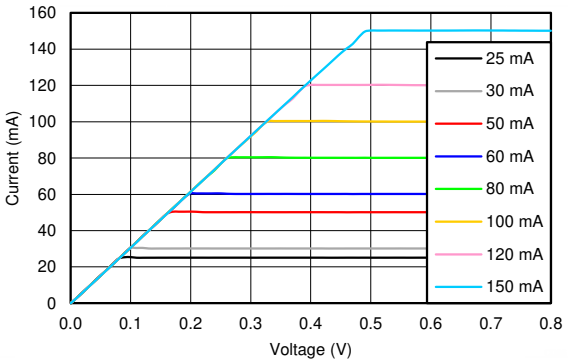
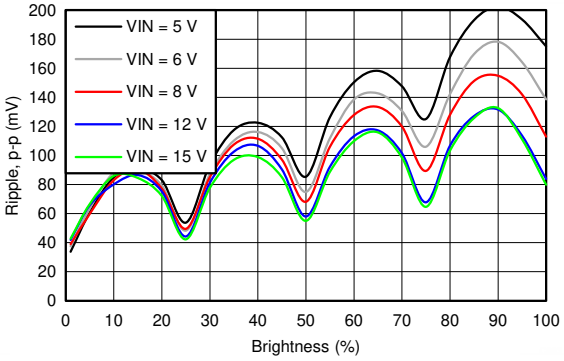
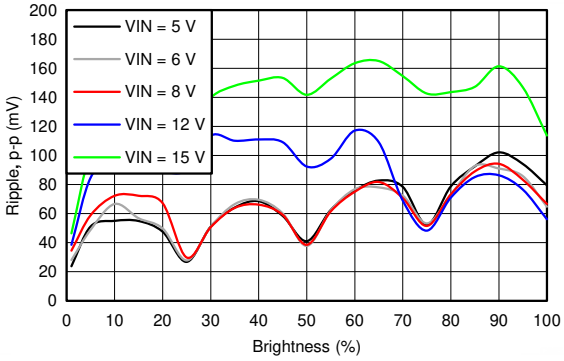


図 5-6. LED Current vs Headroom Voltage



f_{SW} = 303kHz 8 LEDs/string 150mA/string
4 strings Phase shift 90° f_{LED_PWM} = 4.9kHz

図 5-7. Boost Ripple



f_{SW} = 2.2MHz 8 LEDs/string 100mA/string
4 strings Phase shift 90° f_{LED_PWM}= 4.9kHz

図 5-8. Boost Ripple

6 Detailed Description

6.1 Overview

The LP8860-Q1 is a high-voltage LED driver for automotive infotainment, LED clusters, and medium-sized LCD backlight applications with a boost controller. The device can be used as a stand-alone device, with a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- FAULT output to indicate fault condition
- NSS input for fault reset

Alternatively, the LP8860-Q1 can be controlled through I^2C or SPI serial interface which allows wide range of user-specific configurable features.

6.1.1 Boost Controller

The boost controller generates a 16-V to 48-V supply for LED strings. To optimize LED drive efficiency the boost controller includes adaptive output voltage control which gets feedback from monitoring the internal LED current sinks voltage circuit. This feature minimizes power consumption by adjusting the boost voltage to lowest sufficient level in all conditions.

Boost switching frequency can be set in a wide range from 100 kHz to 2.2 MHz. This enables system optimization for both high power applications, where efficiency is critical, and for lower power applications where small solution size can be achieved with high boost switching frequency.

The LP8860-Q1 has several features for system EMI optimization:

- Boost switching frequency can be selected either below or above AM band.
- Spread spectrum can be enabled to reduce energy around the switching frequency and its harmonics.
- Boost switching can be synchronized to an external clock with a dedicated SYNC input.
- Gate drive strength for the external FET is controllable with EEPROM.

6.1.2 LED Output Configurations

The LP8860-Q1 has four high-precision current sinks with up to 150 mA per output capability. LED outputs can be connected parallel to reach higher current levels.

LED outputs are highly configurable; for example, there are features such as brightness slope control, external clock synchronization, phase shifting, adaptive headroom control, etc.

In general there are 2 main user modes:

- Display Mode (with full feature set) and/or
- Cluster Mode (with limited feature set)

These modes and features are detailed in later sections.

6.1.3 Display Mode

In Display Mode LED outputs are configured to power an LCD backlight. Maximum current per string is set by R_{ISET}; alternatively, through a user-programmable EEPROM value.

Brightness is controlled with PWM input or I^2C/SPI register writes. An optional sloper feature enables automatic smooth transition between brightness levels. Sloper time can be programmed to EEPROM registers, and an advanced slope feature allows smoother response to eye compared to traditional linear slope.

Outputs are controlled with a Phase Shift PWM (PSPWM) Scheme. Due to the phase shift between the outputs they are not activated simultaneously which brings several benefits:

- Peak load current from the boost output is decreased, which reduces the voltage ripple seen at the boost output and allows smaller output capacitors.
- Smaller ripple reduces the possible audible noise from the ceramic boost output capacitors.

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- PSPWM scheme multiplies the effective load frequency seen at the boost output by number of active channels. This further reduces the audible noise by transferring the output ripple frequency above human hearing.
- Optical ripple through LCD panel is reduced, helping to reduce the “waterfall” effect which is caused by asynchronous backlight ripple and LCD refresh.

PWM output frequency is set with EEPROM registers from 4.9 kHz to 39 kHz. Selecting output frequency depends on the number of strings used, system requirements for the frequency, and desired dimming ratio. Dimming resolution is a function of PWM output frequency — the higher the frequency, the lower the resolution.

User can choose to increase resolution by:

- enabling dithering function (optional through EEPROM), or
- increasing internal clock frequency.

Increasing internal clock frequency increases device current consumption.

In high-quality display systems an "anti-waterfall" feature may be required. The LP8860-Q1 supports this by offering output synchronization to the LCD refresh signal through VSYNC input. VSYNC input is synchronized to outputs through internal PLL; EEPROM and filtering are described in later sections.

6.1.4 Cluster Mode

In Cluster mode LED strings have independent control but fewer features enabled than in Display Mode.

Brightness (PWM and current) are independently controlled for all 4 outputs. When there is an unequal number of LEDs per channel, the LP8860-Q1 adaptive voltage control is not used in Cluster mode; therefore, boost output voltage is fixed (or externally controlled or powered).

In Cluster mode PWM frequency can be set through EEPROM, and Phase Shift PWM mode is enabled.

Cluster mode does not support the PWM input pin, hybrid dimming, slope control or dither mode.

6.1.5 Hybrid Dimming

Hybrid dimming combines both PWM and current-dimming benefits offering the best optical efficiency to drive LEDs. At higher brightness levels only the LED constant current is controlled; at lower brightness levels LED brightness is controlled by adding PWM on top of low constant current value.

Because LED optical efficacy declines with high forward current, reducing the current yields better system optical efficiency compared with conventional PWM dimming. An additional benefit of current dimming is reduced EMI compared to PWM switching. PWM dimming is used with lower brightness values to achieve a higher dimming ratio. The optimum switch point between PWM and current dimming is programmable and depends on the LED type.

6.1.6 Charge Pump and Square Waveform (SQW) Output

The gate driver for the external boost FET can be powered directly from the VDD input or from the charge pump integrated into the LP8860-Q1. When a 5-V rail is available in the system for VDD supply, it is typically a high enough voltage to drive the external FET, and the internal charge pump can be disabled. In this case, the VDD and CPUMP pins must be shorted together, and the fly cap can be removed. When the system VDD is not high enough to drive the gate of the boost FET (typical case is 3.3 V), the charge pump can be used to multiply the gate drive voltage to 2× VDD.

The SQW output provides a 100-kHz square wave signal (1 mA maximum) with amplitude equal to the charge-pump output voltage. When the charge pump is disabled, the amplitude of the SQW signal is equal to VDD. See *セクション 6.3.7* and *セクション 7.2.3* sections for usage examples.

6.1.7 Power-Line FET

Some automotive systems require a safety switch to disconnect the driver device from the battery. The LP8860-Q1 offers a power-line FET control circuit, which limits inrush current from the power line during start-up and reduces standby power consumption by disconnecting device from the power-line during an off state. This FET

disconnects the boost and LED strings from the input during fault conditions. For example, when the input voltage is above the overvoltage protection (OVP) level, the power-line FET disconnects the LED strings from the power-line to protect LED outputs against overheating.

Depending on which fault has shut down the power-line FET, the device can enter automatic fault recovery state where the power-line FET is turned on in 100-ms time periods to see if the fault condition has been removed. If the fault was only short-term, and normal operation condition returns, the device turns back on automatically.

6.1.8 Protection Features

Extensive fault-detection and protection features of the LP8860-Q1 include:

- Open-string and shorted LED detections
  - LED fault detection prevents system overheating in case of open in some of the LED strings
- Boost overcurrent
- Boost overvoltage
- VIN input overvoltage protection
  - Threshold sensing from VSENSE_P pin
- VIN input undervoltage protection
  - Threshold sensing from VSENSE_P pin
- VIN input overcurrent protection
  - Threshold sensing across R_{ISENSE} resistor
- VDD input undervoltage lockout
- Thermal shutdown in case of die overtemperature (165°C nominal)

Fault protection thresholds are EEPROM programmable and some protection features can be disabled, or masked, if necessary.

A fault condition is indicated through the FAULT pin. If an I^2C/SPI interface is used, the fault reason can be read from the register, and flags can be cleared with register write.

6.1.9 Advanced Thermal Protection Features

The LP8860-Q1 has a unique features for protecting against overheating:

1. Die temperature based Thermal de-rating function. Average LED current is automatically lowered when die temperature increases above a predefined (90°C, 100°C, or 110°C) level. Decreasing LED current reduces thermal loading on the device and prevents overheating.
2. An external NTC sensor-based protection, where a sensor can be placed close to LEDs to protect them from overheating. The sensor is connected to the TSENSE pin of the device. Two methods are available:
   - Current de-rating, where the LED current is lowered proportionally to the temperature measured with the external NTC sensor. This method is available only if LED max current is set with R_{ISET} resistor.
   - Brightness limitation above a predefined temperature

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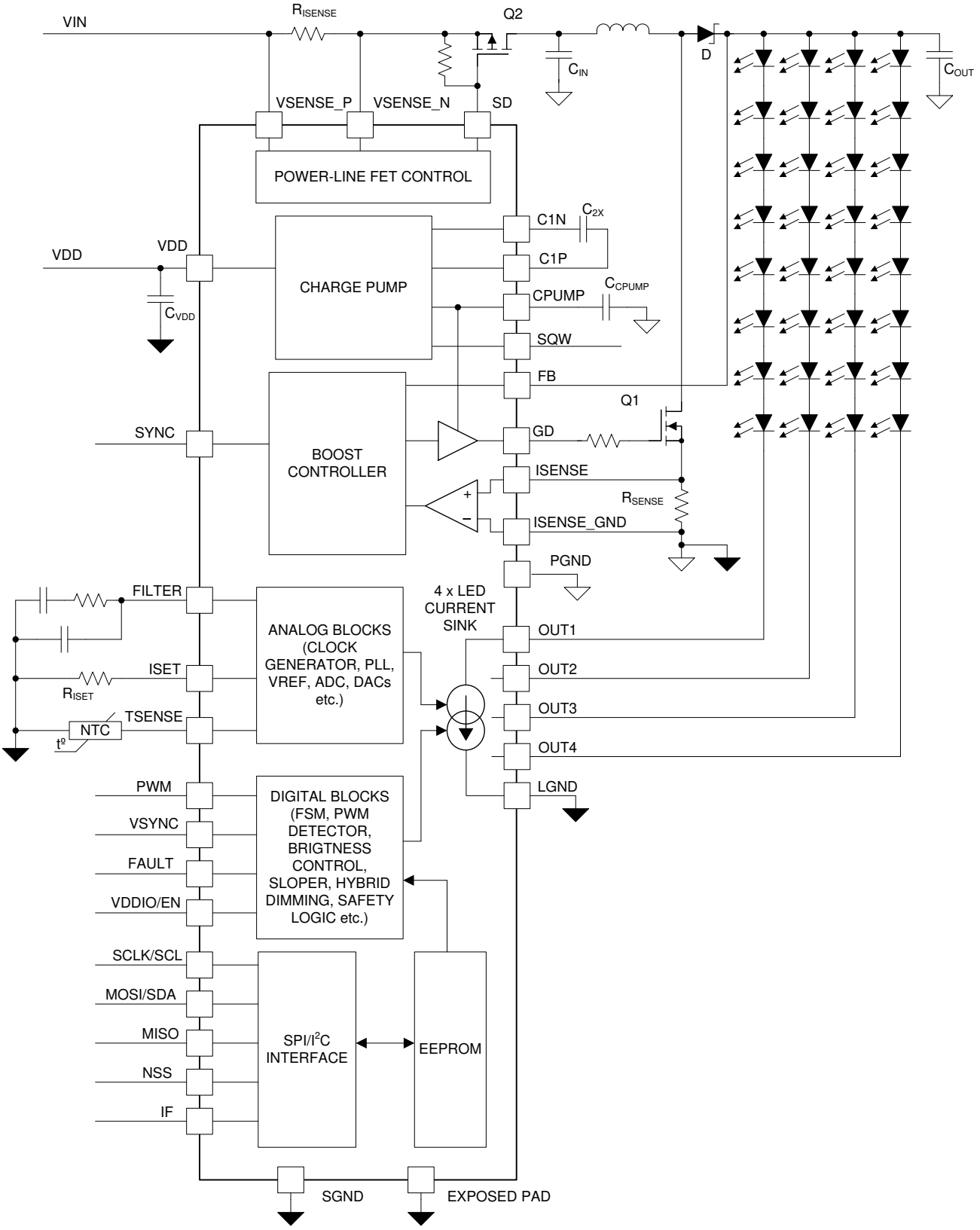
6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Clock Generation

The LP8860-Q1 has an internal 10-MHz oscillator which is used for clocking the PWM input duty cycle measurement. The 10-MHz clock is divided by two, and the 5-MHz clock is used for clocking the state machine and internal timings.

The internal 5-MHz clock can be used for generating the LED PWM output frequency directly or it can be multiplied with an internal PLL to achieve higher resolution. The higher clock frequency for the PWM generation block allows the higher resolution; however, the tradeoff is higher power consumption of the part. Clock multiplication is set with <PWM_RESOLUTION[1:0]> EEPROM bits.

6.3.1.1 LED PWM Clock Generation With VSYNC

Unsynchronized LCD line scanning and LED backlight ripple may cause a “waterfall” effect. Synchronizating LED output PWM frequency with video processor or timing controller VSYNC/HSYNC signal can reduce this effect.

The PLL can be used for generating required PWM generation clock from the VSYNC signal. This ensures that the LED output PWM remains synchronized to the VSYNC signal, and there is no clock variation between the LCD display video update and the LED backlight output frequency. If PWM_COUNTER_RESET = 1, the VSYNC signal rising edge restartsthe PWM generation, ensuring there is no clock drifting. The slow divider is intended for LED PWM frequency synchronization with an external VSYNC. An external filter connected to the FILTER pin must be used only if a slow divider is enabled — otherwise the LP8860-Q1 uses internal compensation.

The f_{OUT} of the PLL must be chosen in the 5-MHz to 40-MHz range. If VSYNC is enabled, the signal must be active before VDDIO/EN is set high and present whenever VDDIO/EN is high.

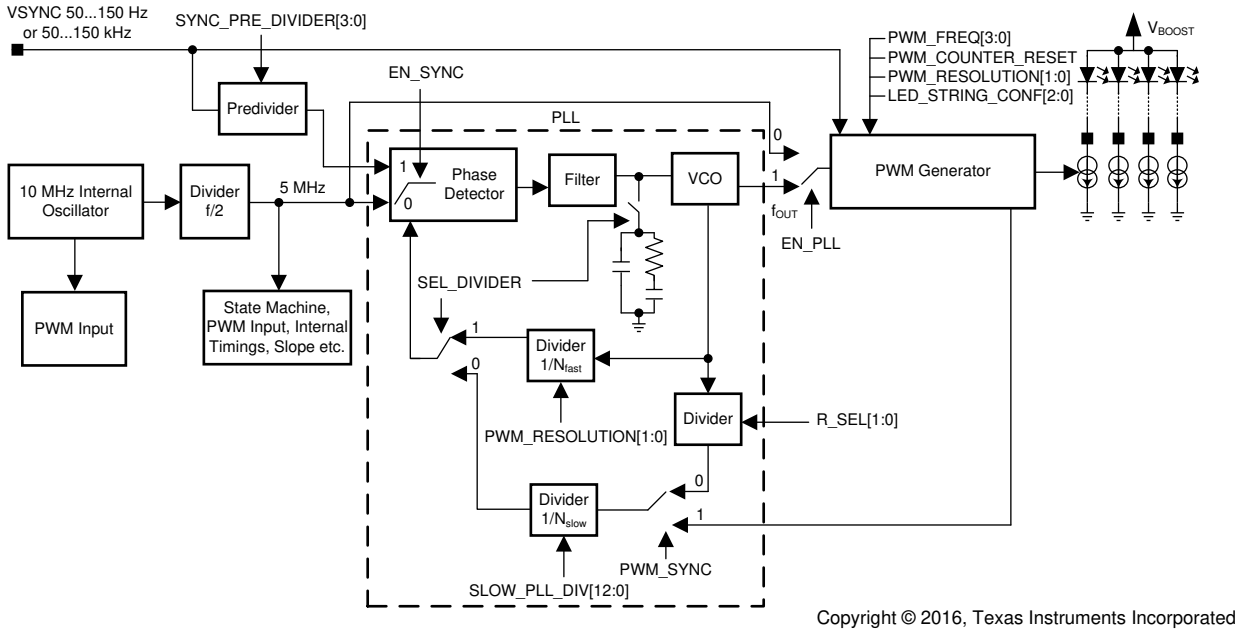

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図 6-1. PLL Clock Generation

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6.3.1.2 LED PWM Frequency and Resolution

LED output PWM frequency is selected with <PWM_FREQ[3:0]> EEPROM register when using a 5MHz internal oscillator for generating PWM output. <LED_STRING_CONF[2:0]> bits define phase shift between LED outputs as described later. <PWM_RESOLUTION[1:0]> EEPROM bits select the PLL output frequency and hence the LED PWM resolution. PWM frequencies with <EN_SYNC> = 0 are listed in 表 6-1.

注

If the VSYNC signal is used for generating PWM output frequency, it affects all clock frequencies, as well as the LED PWM output frequency. The *セクション 6.6.2* section explains how all the dividers affect the output clocks.

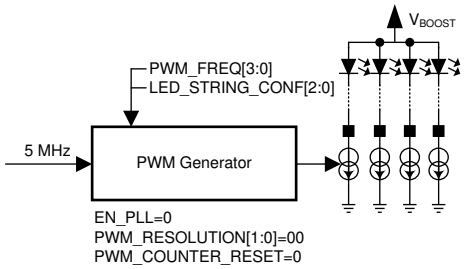

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図 6-2. PWM Clocking With Internal Oscillator

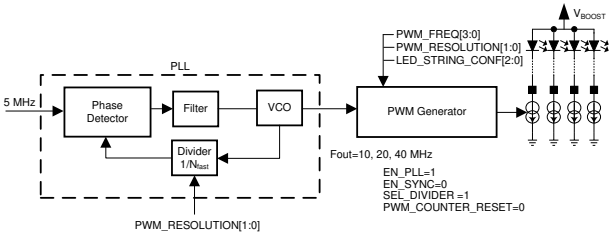

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図 6-3. PWM Clocking With PLL, Internal Oscillator as Reference

表 6-1. Output PWM Frequency and Resolution With Internal Oscillator

		00 OSC = 5MHz	01 OSC = 10MHz	10 OSC = 20MHz	11 OSC = 40MHz
PWM_FREQ[3:0]	**PWM_RESOLUTION[1:0] PWM FREQUENCY (Hz)**	**RESOLUTION (bit)**			
1111	39063	7	8	9	10
1110	34180	7	8	9	10
1101	30518	7	8	9	10
1100	29297	7	8	9	10
1011	28076	7	8	9	10
1010	26855	7	8	9	10
1001	25635	7	8	9	10
1000	24412	7	8	9	10
0111	23192	7	8	9	10
0110	21973	7	8	9	10
0101	20752	7	8	9	10
0100	19531	8	9	10	11
0011	17090	8	9	10	11
0010	13428	8	9	10	11
0001	9766	9	10	11	12
0000	4883	10	11	12	13

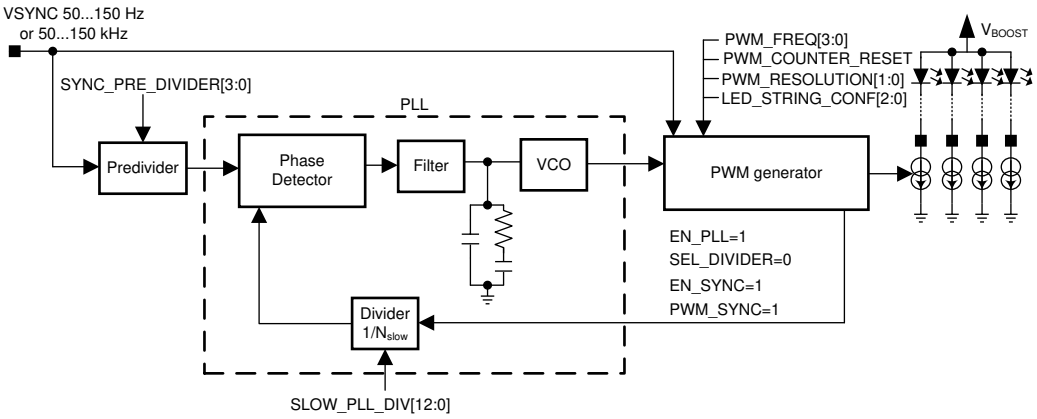

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図 6-4. PWM Synchronization With External VSYNC Input

PWM clock frequencies with different <SEL_DIVIDER>, <EN_PLL>, and <EN_SYNC> combinations are listed in 表 6-2.

表 6-2. PLL Clock and LED PWM Frequency

PWM_SYNC	SEL_DIVIDER	EN_PLL	EN_SYNC	PLL CLOCK	PWM FREQUENCY
0	X	0	0	5MHz	See 表 6-1
0	1	1	0	5, 10, 20, 40MHz	See 表 6-1
0	0	1	1	SYNC × R_SEL[1:0] × SLOW_PLL_DIV[12:0]/ SYNC_PRE_DIV[3:0]	PLL clock / GEN_DIV
1	0	1	1	SYNC × GEN_DIV × SLOW_PLL_DIV[12:0]/ SYNC_PRE_DIV[3:0]	PLL clock / GEN_DIV

GEN_DIV coefficients and resolution (bit) are listed on 表 6-3.

表 6-3. GEN_DIV Coefficients and Resolution

	PWM_RESOLUTION[1:0]											
	00			01			10			11		
PWM_ FREQ[3:0]	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)
0000	64	1024.00	10	32	2048.00	11	16	4096.00	12	8	8192.00	13
0001	128	512.00	9	64	1024.00	10	32	2048.00	11	16	4096.00	12
0010	176	372.36	8	88	744.73	9	44	1489.45	10	22	2978.91	11
0011	224	292.57	8	112	585.14	9	56	1170.29	10	28	2340.57	11
0100	256	256.00	8	128	512.00	9	64	1024.00	10	32	2048.00	11
0101	272	240.94	7	136	481.88	8	68	963.76	9	34	1927.53	10
0110	288	227.56	7	144	455.11	8	72	910.22	9	36	1820.44	10
0111	304	215.58	7	152	431.16	8	76	862.32	9	38	1724.63	10
1000	320	204.80	7	160	409.60	8	80	819.20	9	40	1638.40	10
1001	336	195.05	7	168	390.10	8	84	780.19	9	42	1560.38	10
1010	352	186.18	7	176	372.36	8	88	744.73	9	44	1489.45	10
1011	368	178.09	7	184	356.17	8	92	712.35	9	46	1424.70	10
1100	384	170.67	7	192	341.33	8	96	682.67	9	48	1365.33	10
1101	400	163.84	7	200	327.68	8	100	655.36	9	50	1310.72	10
1110	448	146.29	7	224	292.57	8	112	585.14	9	56	1170.29	10

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表 6-3. GEN_DIV Coefficients and Resolution (続き)

	PWM_RESOLUTION[1:0]											
	00			01			10			11		
PWM_ FREQ[3:0]	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)	STEP	GEN_DIV	RES (bits)
1111	512	128.00	7	256	256.00	8	128	512.00	9	64	1024.00	10

Dithering allows increased resolution and smaller average steps size. Dithering can be programmed with EEPROM bits <DITHER[2:0]> 0 to 4 bits. 図 6-5 shows 1-bit dithering. For 3-bit dithering, every 8th pulse is made 1 LSB longer to increase the average value by 1/8th. Dither is available in steady state condition when <EN_STEADY_DITHER> is high, otherwise during slope only.

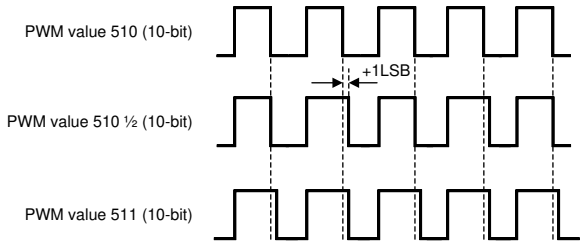

図 6-5. Example of the Dithering, 1-Bit Dither, 10-Bit Resolution

6.3.2 Brightness Control (Display Mode)

The LP8860-Q1 LED outputs can be configured to display or cluster mode. The following sections describe display mode options. Cluster mode is a special mode with individually controlled LED outputs. See *セクション 6.3.5* section for details.

The LP8860-Q1 controls the brightness of the display with conventional PWM or with Hybrid PWM and Current dimming. Brightness control is received either from PWM input pin or from I^{2}C/SPI register bits. The brightness source is selected with <BRT_MODE[1:0]> bits as follows:

表 6-4. Brightness Control Selection

BRT_MODE[1:0]	BRIGHTNESS CONTROL
00	PWM input duty cycle
01	PWM input duty cycle x Brightness register
10	Brightness register
11	PWM direct control (PWM in = PWM out)

6.3.2.1 PWM Input Duty Cycle Based Control

In this mode the LED brightness is controlled by the input PWM duty cycle. The PWM detector block measures the duty cycle in the PWM pin and uses this 16-bit value to control the duty cycle of the LED output PWM. Input PWM period is measured from rising edge to the next rising edge.

The ratio of input PWM frequency and 10-MHz sampling clock defines resolution reachable with external PWM.

PWM input block timeout is 24 ms after the last rising edge; it must be taken into account for 0% and 100% brightness setting. For setting 100% brightness, a high-level PWM input signal must last at least 24 ms. The minimum on and off time for the PWM input signal is 400 ns.

6.3.2.2 Brightness Register Control

With brightness register control the LED output PWM is controlled with 16-bit resolution <DISP_CL1_BRT[15:0]> register bits.

6.3.2.3 PWM Input Duty × Brightness Register

In this mode the PWM input duty cycle value is multiplied with the 16-bit <DISP_CL1_BRT[15:0]> register value to achieve the LED output PWM.

6.3.2.4 PWM-Input Direct Control

With PWM-input direct control the output PWM directly follows the input PWM frequency and duty cycle. Due to the internal logic structure the input is clocked with the 5-MHz clock or the PLL clock (if it is enabled). The output PWM delay can be 5 to 6 clock cycles from input PWM.

In the direct control mode several of the advanced features are not available: Phase Shift PWM (PSPWM), brightness slope, dither, Hybrid PWM and Current dimming, and LED current limitation with external NTC.

Dimming ratio can be calculated as the ratio between the brightness PWM input signal and sampling clock (5-MHz or PLL clock) frequencies. In direct mode PWM duty cycle must be less than 100%. Boost adaptive mode turns off at 100% duty cycle.

6.3.2.5 Brightness Slope

Sloper makes the smooth transition from one brightness value to another. Slope time can be programmed with EEPROM bits <PWM_SLOPE[2:0]> from 0 to 511 ms. Slope time is used for sloping up and down. Advanced slope makes brightness changes smooth for eye.

表 6-5. Slope Time

PWM_SLOPE[2:0]	SLOPE TIME
000	disabled
001	1 ms
010	2 ms
011	52 ms
100	105 ms
101	210 ms
110	315 ms
111	511 ms

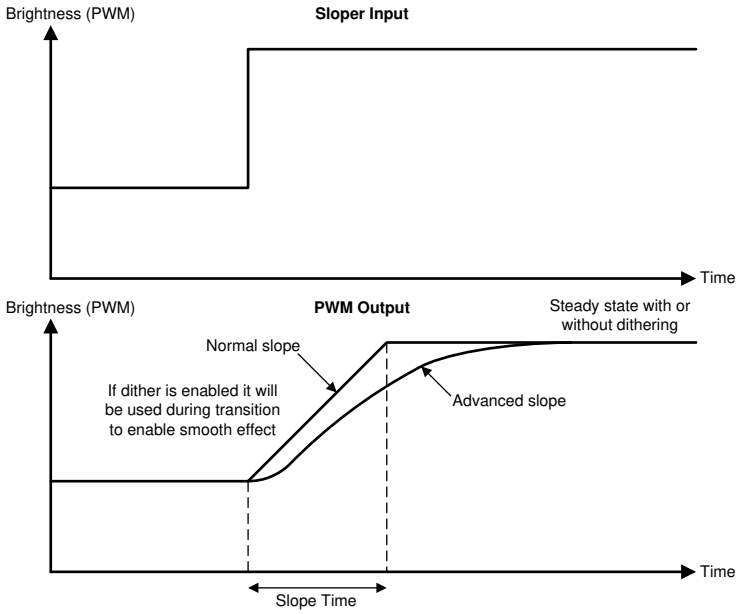

図 6-6. Sloper Operation

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6.3.2.6 LED Dimming Methods

In additional to conventional PWM dimming control the LP8860-Q1 supports Hybrid PWM and Current dimming. Hybrid dimming combines the PWM and current dimming methods. PWM dimming operates with a lower range of light, and linear current dimming is used with higher brightness values. If the <EN_PWM_I EEPROM> bit is set to 1, the system enables hybrid dimming. Principles of PWM dimming and Hybrid PWM and Current dimming are illustrated by 図 6-7. Only 25% switch points and slope gain = 1 are shown for simplicity.

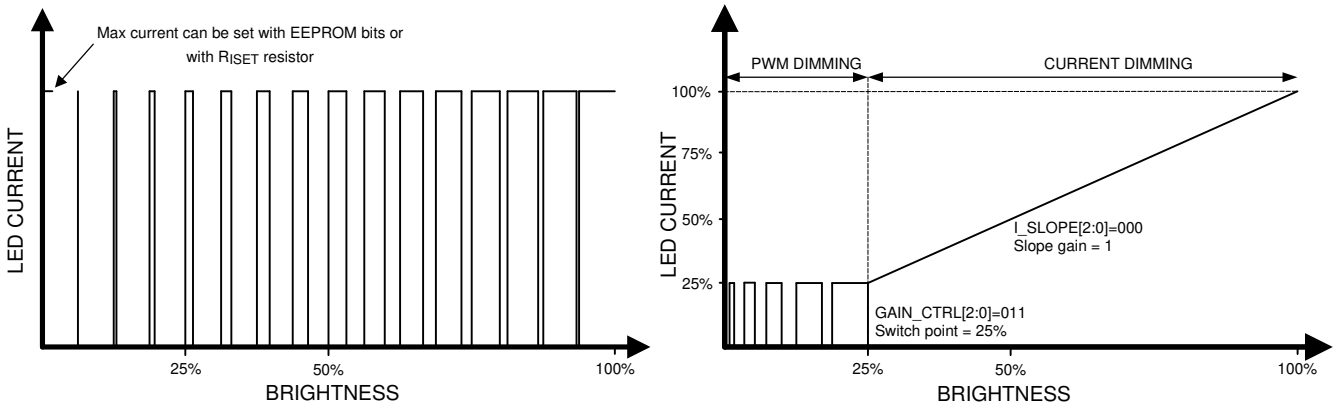

図 6-7. Principles of PWM Dimming and Hybrid PWM and Current Dimming

LED forward voltage increases and efficiency declines when forward current is increased. Use of constant current with PWM dimming at lower brightness and current dimming at greater brightness (instead of PWM dimming at full brightness range), yields better optical efficiency and resolution especially at lower brightness values. The optimum switch point between PWM and current dimming modes and current slope depend on the LED type.

PWM control ranges from 12.5% to 50% and the current slope can be selected using <GAIN_CTRL[2:0]> and <I_SLOPE[2:0]> EEPROM bits, respectively (see 表 6-6 and 表 6-7).

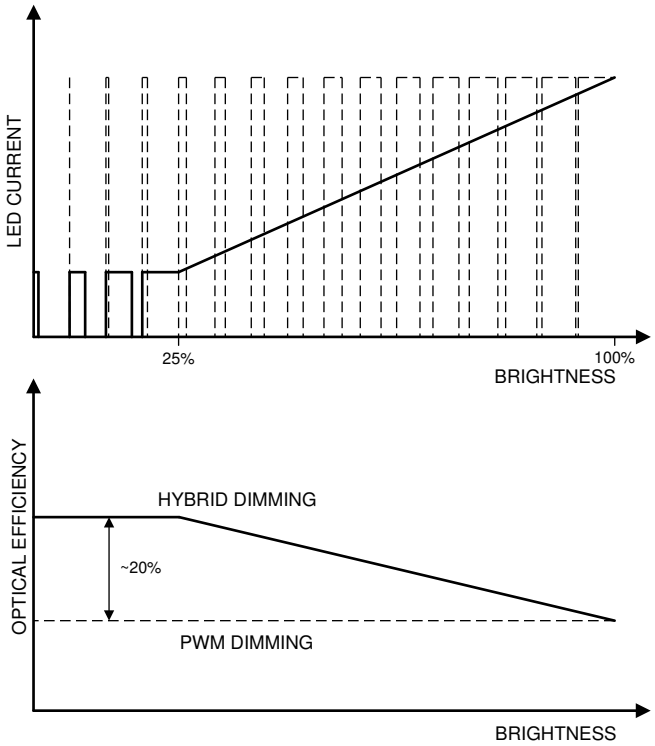

図 6-8. Optical Efficiency Improvement With PWM and Current Dimming

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表 6-6. Gain Control Selections

GAIN_CTRL[2:0]	SWITCH POINT FROM PWM TO CURRENT DIMMING
000	50.0%
001	40.6%
010	31.3%
011	25.0%
100	21.9%
101	18.8%
110	15.6%
111	12.5%

表 6-7. Current Slope Control Selections

I_SLOPE[2:0]	SLOPE GAIN
000	1.000
001	1.023
010	1.047
011	1.070
100	1.094
101	1.117
110	1.141
111	1.164

The current setting for DISP_CL1_CURRENT[11:0] in Hybrid PWM and Current dimming mode can be defined by the following formula (assuming individual LED sink current correction DRV_OUTx_CORR[3:0] is 0%):

$$I_{DISP_CL1_CURRENT[11:0]} = I_{MAX} - DRV_LED_CURRENT_SCALE[2:0] \times I_SLOPE[2:0] \times \frac{(100\% - GAIN_CTRL[2:0])}{100\%} \quad (1)$$

Example of calculation for Hybrid PWM and Current dimming mode, 100-mA maximum output current:

Target maximum current 100 mA	$I_{DISP_CL1_CURRENT}$ = 100 – 100 × 1 × ((100 – 25) / 100) = 25 mA
Maximum scale 100 mA (DRV_LED_CURRENT_SCALE[2:0]=101)	
Slope = 1.000 (I_SLOPE[2:0]=000)	
Switch point = 25% (GAIN_CTRL[2:0]=011)	

Example of calculation for Hybrid PWM and Current dimming mode, 23-mA maximum output current:

Target maximum current 23 mA	$I_{DISP_CL1_CURRENT}$ = 23 – 25 × 1.094 × ((100 – 25) / 100) = 2.49 mA
Maximum scale 25 mA (DRV_LED_CURRENT_SCALE[2:0]=000)	
Slope = 1.094 (I_SLOPE[2:0]=100)	
Switch point = 25% (GAIN_CTRL[2:0]=011)	

注

1. Formula is only approximation for the actual value.
2. DISP_CL1_CURRENT[11:0] value must be chosen to avoid current saturation before 100% brightness is achieved.

6.3.2.7 PWM Calculation Data Flow for Display Mode

図 6-9 shows the PWM calculation data flow for display mode. In PWM direct control mode most of the blocks are bypassed, and this flow chart does not apply.

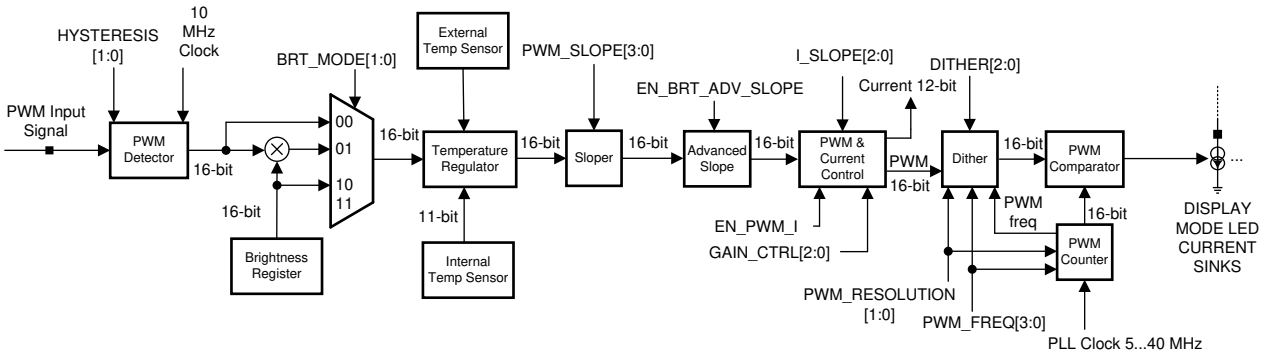

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図 6-9. PWM Data Flow Calculation

表 6-8. PWM Calculation Blocks

BLOCK NAME	DESCRIPTION
PWM detector	PWM detector block measures the duty cycle of the input PWM signal. Resolution depends on the input signal frequency. Hysteresis selection sets the minimum allowable change to the input. Smaller changes are ignored.
Brightness register	16-bit register for brightness setting <DISP_CL1_BRT[15:0]>
Brightness mode control	Brightness control block gets 16-bit value from the PWM detector, and also 16-bit value from the brightness register <DISP_CL1_BRT[15:0]>. <BRT_MODE[1:0]> selects whether to use PWM input duty cycle value, the brightness register value or multiplication.
Temperature regulator	Temperature regulator reduces LED PWM duty cycle depending on internal and external temperature sensor. See *セクション 6.3.9.2* and *セクション 6.3.9.3* for details
External temperature sensor	External NTC temperature sensor
Internal temperature sensor	Internal die temperature sensor
Sloper	Sloper makes the smooth transition from one brightness value to another. Slope time can be adjusted from 0 ms to 511 ms with <PWM_SLOPE[2:0]> EEPROM bits.
Advanced sloper	Advanced slope makes brightness changes smoother for eye; see *セクション 6.3.2.5* for details
PWM and Current Control	Hybrid PWM and Current dimming improves the optical efficiency of the LEDs by using PWM control with lower brightness values and current control with greater values. <EN_PWM_I> EEPROM bit enables Hybrid PWM and Current control. PWM dimming range can be set 12.5 to 50% of the brightness range with <GAIN_CTRL[2:0]> EEPROM bits. Current slope can be adjusted by using the <I_SLOPE[2:0]> EEPROM bits. See *セクション 6.3.2.6* for details
Dither	With dithering the output resolution can be further increased. This way the brightness change steps are not visible to eye. The amount of dithering is 0 to 4 bits, and is selected with <DITHER[2:0]> EEPROM bits.
PWM comparator	PWM comparator compares the PWM counter output to the value received from the dither block. Output of the PWM comparator directly controls the LED current sinks. If Phase Shift PWM (PSPWM) mode is used, the PWM counter values for each LED output are modified by summing an offset value to create different phases.

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表 6-8. PWM Calculation Blocks (続き)

BLOCK NAME	DESCRIPTION
PWM counter	Overflowing 16-bit PWM counter creates new PWM cycle. Step for incrementation is defined by <PWM_FREQ[3:0]> and <PWM_RESOLUTION[1:0]> bits, see 表 6-3.

6.3.3 LED Output Modes and Phase Shift PWM (PSPWM) Scheme

The PSPWM scheme allows delaying the time when each LED output is active. When the LED outputs are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. The PSPWM scheme also increases the load frequency seen on boost output up to 4 times, therefore transferring possible audible noise to a frequency above human hearing range. In addition, “optical ripple” through the LCD panel is reduced helping in waterfall noise reduction.

図 6-10 shows the available LED output modes. The number of LED outputs used can be one to four; outputs can be tied together to increase current for one string or all four strings can be independently controlled in the cluster mode.

In <LED_STRING_CONF[2:0]> = 000 the phase difference between channels is 90 degrees. This mode is intended for application in 図 7-1. When <LED_STRING_CONF[2:0] > = 001 the phase difference between 3 channels in display mode is 120 degrees. This mode is intended for application shown in 図 7-11. When <LED_STRING_CONF[2:0]> = 010 the phase difference between 2 channels in display mode is 180 degrees, channels 3 and 4 in cluster mode, intended for application illustrated by 図 7-8. LED strings not used in Display mode can be used for Cluster mode, or not used. When <LED_STRING_CONF[2:0]> = 111 all strings are in cluster mode.

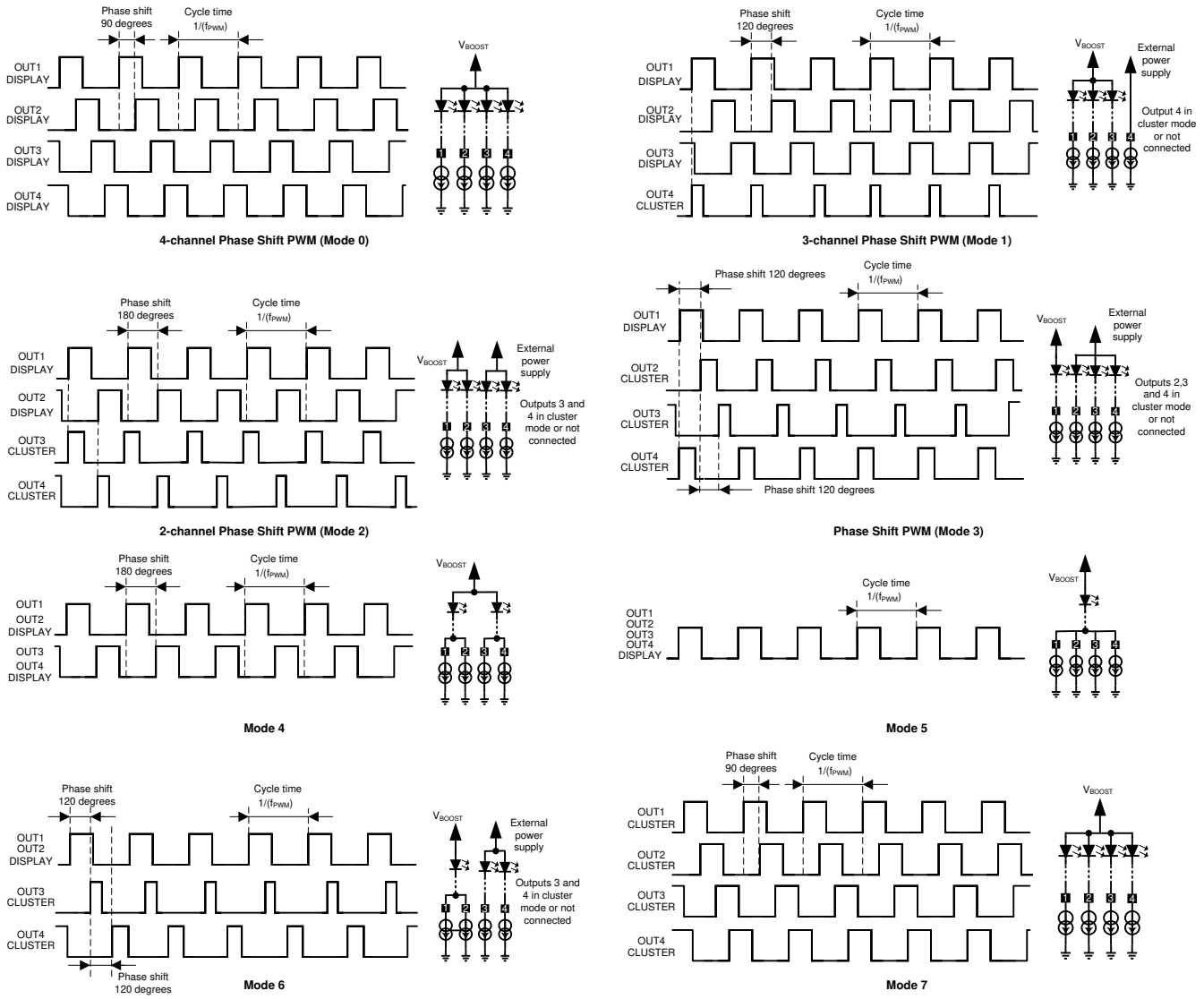

図 6-10. Phase Shift Modes

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表 6-9. Description of the LED Output Modes

MODE	LED_STRING_CONF[2:0]	DESCRIPTION
0	000	4 separate LED strings with 90° phase shift
1	001	3 separate LED strings with 120° phase shift (String 4 in cluster mode or not used)
2	010	2 separate LED strings with 180° phase shift (Strings 3 and 4 in cluster mode or not used)
3	011	1 LED string. (Strings 2,3 and 4 in cluster mode or not used)
4	100	2 LED strings (1+2, 3+4) with 180° phase shift. Strings with same phase can be connected together.
5	101	1 LED string (1+2+3+4). All strings with same phase (can be tied together).
6	110	1 LED string (1+2). 1st and 2nd strings tied with same phase, strings 3 and 4 are in cluster mode or not used
7	111	All strings are used in cluster mode with 90° phase shift

表 6-10. Output Mode Configuration

LED_STRING_CONF[2:0]	000		001		010		011		100		101		110		111	
SETUP	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**	**No. of Displ. Strings**	**No. of Cluster Strings**
	4	**0**	**3**	**1**	**2**	**1+1**	**1**	**1+1+1**	**2+2**	**0**	**same phase/ 4 tied**	**0**	**same phase/ 2 tied**	**1+1**	**0**	**1+1+1+1**
Adaptive voltage control	Y		Y	N	Y	N	Y	N	Y		Y		Y	N		N
FAULT DETECTION																
Open LED string	Y		Y	Y	Y	Y	Y	Y	Y		Y		Y	Y		Y
Short LED string	Y		Y	Y	Y	Y	N	Y	Y		Y/N		Y/N	Y		Y
OPTIONS																
Sloper	Y		Y	N	Y	N	Y	N	Y		Y		Y	N		N
Dithering																
Int. temp. current dimming																
Ext. temp. current limit																
Ext. temp. current dimming				Y		Y		Y						Y		Y
Brightness modes	All		All	Reg. only	All	Reg. only	All	Reg. only	All		All		All	Reg. only		Reg. only
PMW dimming	Y		Y	Y	Y	Y	Y	Y	Y		Y		Y	Y		Y
Hybrid PWM and Current Dimming				N		N		N						N		N
LED OUTPUT PARAMETERS (PLL Frequency 40 MHz)																
$f_{LED\ PWM}$ min	4.9 kHz		4.9 kHz								4.9 kHz		4.9 kHz			4.9 kHz
Resolution at min $f_{LED\ PWM}$	13		13								13		13			13
$f_{LED\ PWM}$ max	39 kHz		39 kHz								39 kHz		39 kHz			4.9 kHz
Resolution at max $f_{LED\ PWM}$	10		10								10		10			13
Additional Dither for Display	4		4	N	4	N	4	N	4		4		4	N		N
LED OUTPUT PARAMETERS (PLL Frequency 5 MHz/off																
$f_{LED\ PWM}$ min	4.9 kHz		4.9 kHz								4.9 kHz		4.9 kHz			610 Hz
Resolution at min $f_{LED\ PWM}$	10		10								10		10			13
$f_{LED\ PWM}$ Max	39 kHz		39 kHz								39 kHz		39 kHz			610 Hz
Resolution at max $f_{LED\ PWM}$	7		7										7			13
Additional bits with dither	4		4	N	4	N	4	N	4		4		4	N		N

6.3.4 LED Current Setting

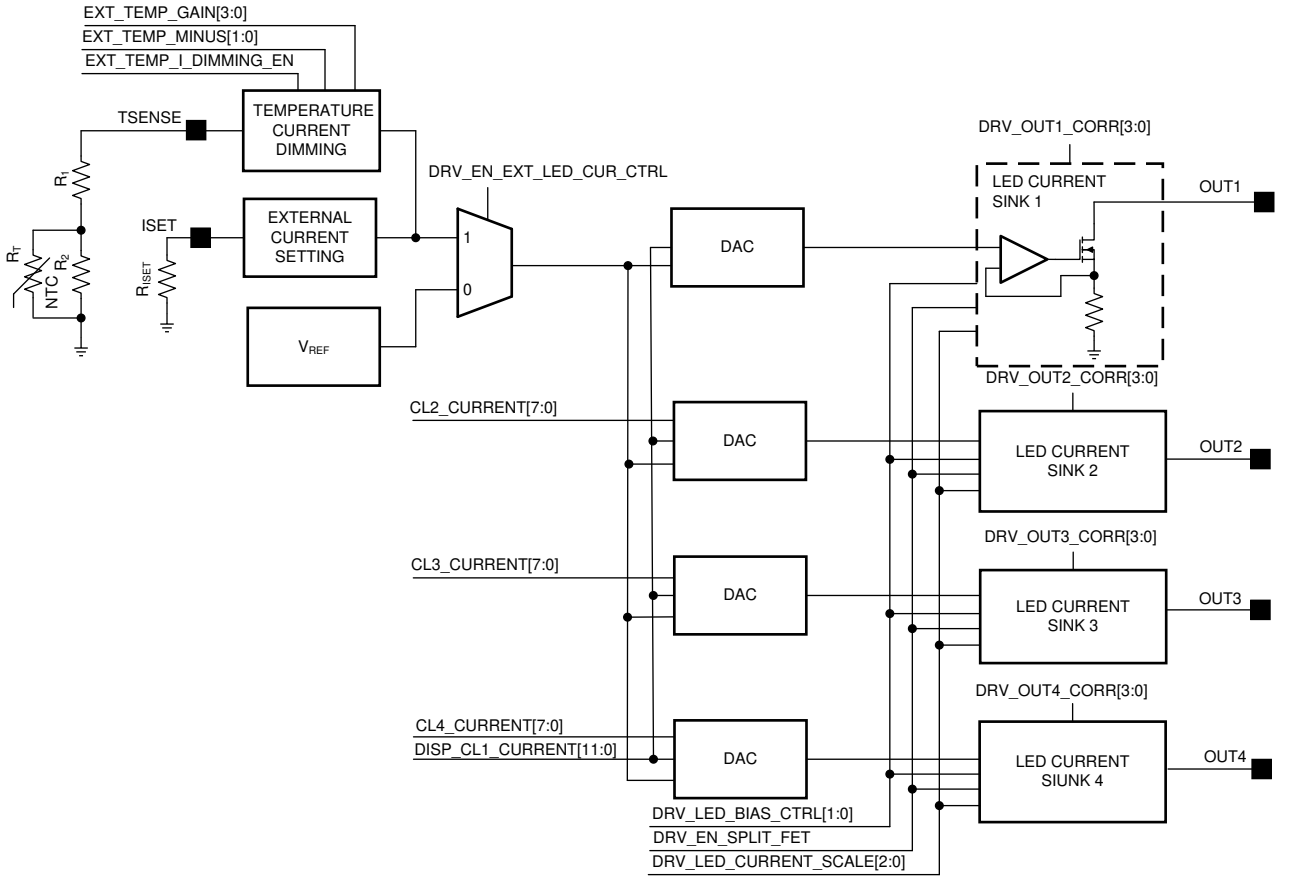

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図 6-11. LED Current Setting

The output LED current can be set by a register. Maximum output LED current can be set by an external resistor when that option is enabled. For strings in cluster mode current for every LED output can be set independently. For more details regarding electrical overstress analysis options, see TI Application Note LP8860-Q1 Electrical Overstress Analysis and Recommendation (SNVA843).

The maximum current for the LED outputs in display mode are controlled with <DISP_CL1_CURRENT [11:0]> bits. Current for the outputs in the cluster mode are controlled separately by the register bits <DISP_CL1_CURRENT[11:0]>, <CL2_CURRENT[7:0]>, <CL3_CURRENT[7:0]>, and <CL4_CURRENT[7:0]> respectively. In the display mode resolution for current control is 12 bits. In the cluster mode resolution is 8 bits for all outputs except OUT1. For OUT1 maximum current resolution is always 12 bits.

Additionally, current for every output current can be scaled with <DRV_LED_CURRENT_SCALE[2:0]> bits (see 表 6-11) and can be corrected by <DRV_OUTx_CORR[3:0]> EEPROM bits. The adjustment range is shown in 表 6-12 Maximum current settings are effective for display and cluster modes.

表 6-11. LED Current Scaling

DRV_LED_CURRENT_SCALE[2:0]	MAXIMUM CURRENT
000	25 mA
001	30 mA
010	50 mA
011	60 mA

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表 6-11. LED Current Scaling (続き)

DRV_LED_CURRENT_SCALE[2:0]	MAXIMUM CURRENT
100	80 mA
101	100 mA
110	120 mA
111	150 mA

When maximum current is controlled by anexternal resistor R_{ISET} (<DRV_EN_EXT_LED_CUR_CTRL>=1), current for outputs in display mode or for OUT1 in cluster mode can be calculated as follows:

$$I_{LED} = \frac{3000 \times V_{BG}}{R_{ISET}} \times \frac{DISP_CL1_CURRENT[11:0]}{4095} \times \frac{DRV_LED_CURRENT_SCALE[2:0]}{150} \times \frac{(DRV_OUTx_CORR[3:0]+100)}{100} \quad (2)$$

Where V_{BG} = 1.2 V.

For example, if <DISP_CL1_CURRENT[11:0]> is 0xFFF, <DRV_LED_CURRENT_SCALE[0:2]> is 111, and a 24-kΩ R_{ISET} resistor is used, then the LED maximum current is 150 mA.

When current control with external resistor is disabled (<DRV_EN_EXT_LED_CUR_CTRL>=0) LED current for outputs in display mode or for OUT1 in cluster mode can be calculated as follow:

$$I_{LED} = \frac{DISP_CL1_CURRENT[11:0]}{4095} \times DRV_LED_CURRENT_SCALE[2:0] \times \frac{(DRV_OUTx_CORR[3:0]+100)}{100} \quad (3)$$

When maximum current control with external resistor is enabled, LED current for OUT2…OUT4 outputs in cluster mode is defined as:

$$I_{LED} = \frac{3000 \times V_{BG}}{R_{ISET}} \times \frac{CLx_CURRENT[7:0]}{255} \times \frac{DRV_LED_CURRENT_SCALE[2:0]}{150} \times \frac{(DRV_OUTx_CORR[3:0]+100)}{100} \quad (4)$$

Otherwise, when current control with external resistor is disabled:

$$I_{LED} = \frac{CLx_CURRENT[7:0]}{255} \times DRV_LED_CURRENT_SCALE[2:0] \times \frac{(DRV_OUTx_CORR[3:0]+100)}{100} \quad (5)$$

Correction value is defined by <DRV_OUTx_CORR[3:0]> shown in 表 6-12:

表 6-12. Individual Current Correction

DRV_OUTx_CORR[3:0]	CORRECTION
0000	6.50%
0001	5.60%
0010	4.70%
0011	3.70%
0100	2.80%
0101	1.90%
0110	0.90%
0111	0.00%
1000	–0.9%
1001	–1.90%
1010	–2.80%
1011	–3.70%

表 6-12. Individual Current Correction (続き)

DRV_OUTx_CORR[3:0]	CORRECTION
1100	–4.70%
1101	–5.60%
1110	–6.50%
1111	–7.40%

注

Formulas are only approximation for the actual current.

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The <DISP_CL1_CURRENT[11:0]> register is initialized during start-up by the <LED_CURRENT_CTRL[11:0]> EEPROM bits. <DRV_LED_CURRENT_SCALE[2:0]> are initialized by the <DRV_LED_CURRENT_SCALE[2:0]> EEPROM bits. Cluster mode current registers for outputs OUT2 and OUT3 are initialized by 0 during power on reset.

Current register value must be not written to 0 if brightness is not zero – it may cause LED faults and adaptive voltage control instability.

6.3.5 Cluster Mode

Cluster is a simplified mode which allows independent current and PWM control for every string in cluster mode. In this mode brightness control is limited to conventional PWM through the SPI/I^{2}C brightness registers. The PWM input pin, Hybrid PWM and Current dimming mode, slope control, or dither are not available. Brightness for different LED strings depends on <DISP_CL1_BRT[15:0]>, <CL2_BRT[12:0]>, <CL3_BRT[12:0]> and <CL4_BRT[12:0]> registers. If OUT1 is in cluster mode, only 13 MSB are used. If all LED outputs are in the cluster mode, LED output PWM resolution is always 13 bits, and frequency depends on <PWM_RESOLUTION[1:0]> bits (see 表 6-13). If one or more of the LED outputs is in display mode, frequency, and resolution for strings in the cluster mode is the same as for strings in the display mode (see 表 6-1).

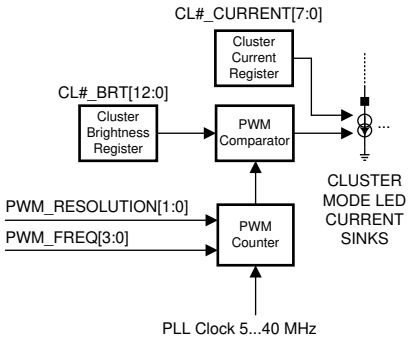

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図 6-12. Cluster Mode Block Diagram

表 6-13. Output PWM Frequency for Mode 7 (All Strings in Cluster Mode)

PWM_RESOLUTION[1:0]	00	01	10	11
OSC frequency (MHz)	5	10	20	40
$f_{LED\ PWM}$ (Hz)	610	1221	2442	4883

When the LP8860-Q1 is set in cluster mode, fault protection functionality is limited. Headroom for LED strings must be between the high-voltage comparator level <DRV_LED_FAULT_THR[1:0]> and low-voltage comparator level <DRV_HEADR[2:0]> (which depend upon saturation voltage); otherwise a fault is generated.

Adaptive boost control does not follow strings in cluster mode. Display mode strings and cluster mode strings must not be connected to the same boost. When LED strings in display and cluster modes are connected to the same boost, LED open or short faults may be generated if the LED forward-voltage mismatch is too high.

If all LED outputs are in cluster mode, boost output voltage is fixed and must be set by EEPROM <BOOST_INITIAL_VOLTAGE[5:0]> bits to a value high enough to ensure correct LED string operation in all conditions.

<EN_CL_LED_FAULT>=0 disables cluster LED fault detection, even if all LED strings are in the cluster mode. The current de-rating (based on the internal temperature sensor) and LED current limitation (based on external temperature sensor) are not functional in this mode, and analog current dimming based on the external sensor functionality is limited (LED shutdown for high temperature is not operational).

6.3.6 Boost Controller

The LP8860-Q1 boost controller generates a 16-V to 48-V supply voltage for the LEDs. Output voltage can be increased by an external resistive voltage divider connected to the FB pin, but voltage lower than 16 V is not supported.

The output voltage can be controlled either with EEPROM register bits <BOOST_INITIAL_VOLTAGE[5:0]>, or automatic adaptive boost control can be used. During start-up the output voltage is ramped to default start-up voltage <BOOST_INITIAL_VOLTAGE[5:0]> where it then adapts to the required voltage based on LED output headroom voltage (if adaptive mode has been enabled in EEPROM). Initial voltage for adaptive voltage control mode must be higher than LED string voltage — otherwise the system may generate a boost overvoltage fault during VDDIO/EN pin toggling if the output boost capacitor is not discharged below the initial voltage before the next boost start-up. A different option is to set <MASK_BOOST_OVP_STATUS> bit high to prevent a boost overvoltage fault.

The converter is a magnetic switching PWM mode DC-DC converter with a current limit. The topology of the magnetic boost converter is called Current Programmed Mode (CPM) control, where the inductor current is measured and controlled with the feedback. Switching frequency is selectable from 100 kHz and 2.2 MHz with EEPROM bits <BOOST_FREQ_SEL[2:0]>. In most cases lower frequency has the highest system efficiency. For more details regarding boost compensation register options, see TI Application Note LP8860-Q1 Boost Compensation Registers (SNVA789A).

In adaptive mode the boost output voltage is adjusted automatically based on LED current sink headroom voltage. Boost output voltage control step size is, in this case, 125 mV to ensure as small as possible current sink headroom and high efficiency. The adaptive mode is enabled with the <EN_ADAP EEPROM> bit. If boost is started with adaptive mode enabled, then the initial boost output voltage value is defined with the <BOOST_INITIAL_VOLTAGE[5:0]> EEPROM register bits in order to eliminate long output voltage iteration time when boost is started after VDDIO/EN toggling or power-on reset.

Boost can be clocked by an external SYNC signal (100 kHz to 2.2 MHz); minimum pulse length for the signal is 200 ns. If an external SYNC disappears, boost uses internal frequency defined by <BOOST_FREQ_SEL[2:0]> EEPROM bits. The boost frequency with external SYNC and EEPROM bits-defined frequency need to be close to each other; maximum frequency mismatch is ±25%. The boost controller has optional spread-spectrum switching operation (±3% from central frequency, 1.875-kHz modulation frequency) which reduces spectrum spikes around the switching frequency and its harmonic frequencies.

Further EMI reduction can be achieved by limiting the rise and fall times of the FET with an additional external resistor on the GD pin.

The boost gate driver is powered directly from VDD voltage or from the charge pump which multiplies V_{DD} voltage by 2. If the charge pump is disabled, the VDD and CPUMP pins must be tied together.

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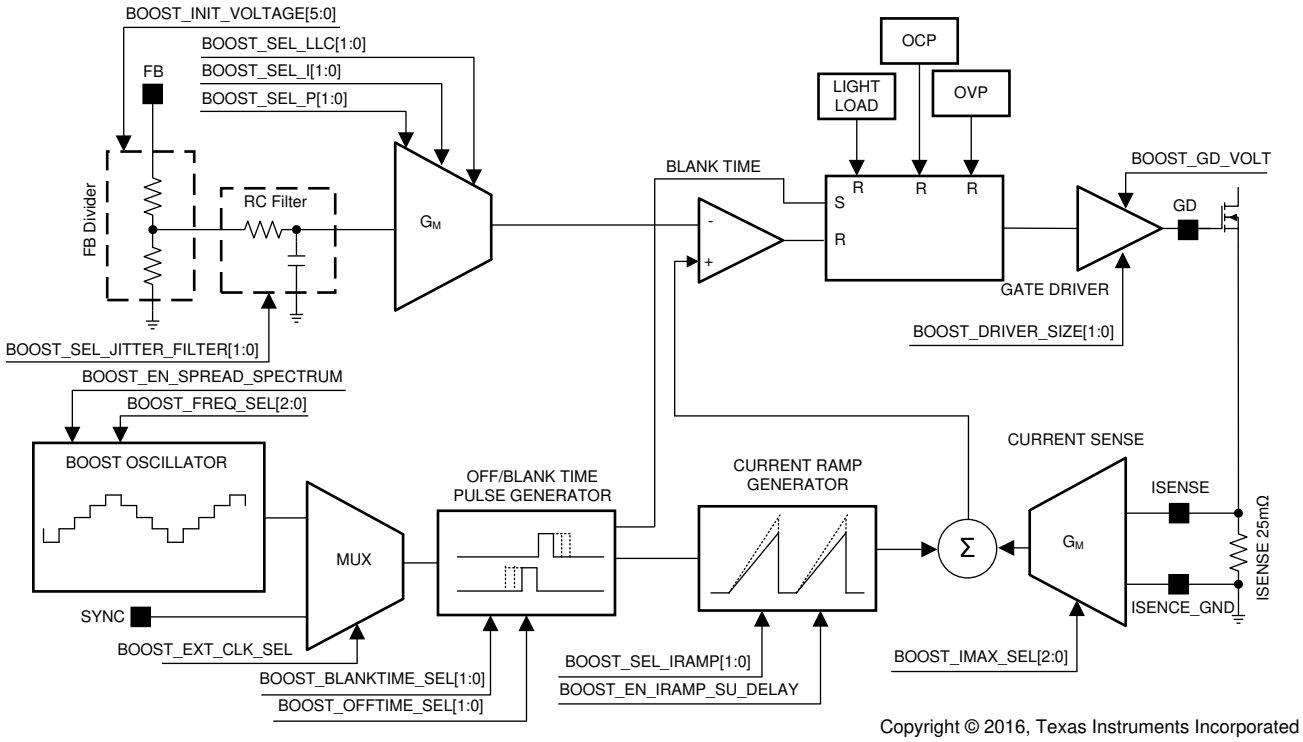

図 6-13. Boost Converter Topology

6.3.7 Charge Pump

The boost switch FET gate driver is powered typically from VDD voltage. When the VDD voltage is not high enough to drive the boost FET gate, the charge pump can be used to increase gate-driver voltage.

The charge pump effectively doubles the VDD voltage for gate driver. Maximum DC output current is 50 mA. Boost driver voltage selection bit BOOST_GD_VOLT must be set to 1 before enabling the charge pump. If VDD voltage is 5 V, the charge pump is not typically needed. In this case, a flying capacitor is not necessary, and the charge pump output CPUMP pin must be connected to the VDD input pin.

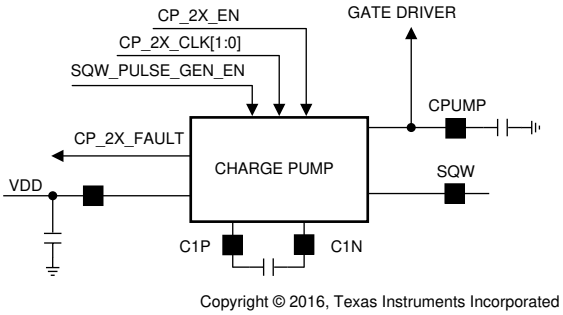

図 6-14. Charge Pump

表 6-14. Charge Pump Clock Frequency

CP_2X_CLK	FREQUENCY (kHz)
00	104
01	208
10	417
11	833

Square-waveform (SQW) output provides a 100-kHz square wave signal (1 mA max) with amplitude equal to the charge pump output voltage. When the charge pump is disabled, amplitude of this voltage is equal to VDD. This signal can be used to generate low-current voltage rails; for example, a gate-reference voltage for output protective FET (図 7-9) or for using nMOSFET as power-line FET (図 6-17). 図 6-15 and 図 6-16 show examples of possible connections.

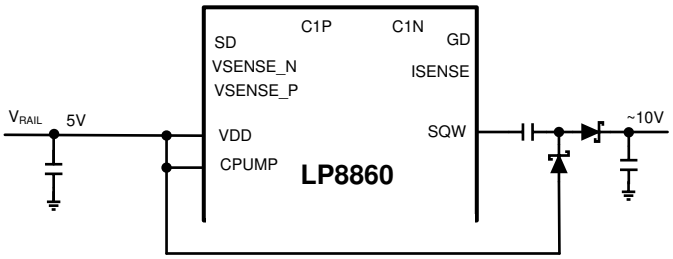

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図 6-15. V_{RAIL} Multiplied by 2

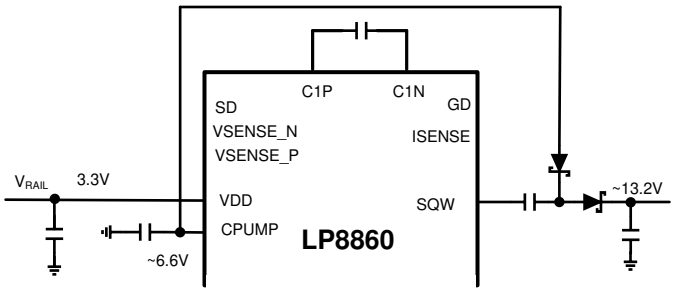

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図 6-16. V_{RAIL} Multiplied by 4

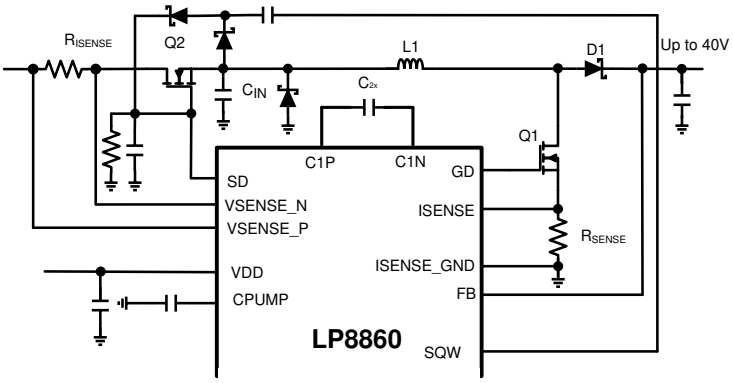

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図 6-17. Using nFET for Power-Line Control

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6.3.8 Powerline Control FET

The power-line FET limits peak current from the power line during start-up and allows the boost and LED strings to be disconnected during a fault condition, when device is in fault recovery state.

The power-line control block has VSENSE_P and VSENSE_N pins for sensing input current and a shutdown SD pin for driving the gate of the power-line FET. The power-line FET is opened when the LP8860-Q1 is enabled by VDDIO/EN signal and V_{IN} is greater than V_{GS} in steady state (when pFET is used as a power-line FET). A power-line pFET must be chosen with minimal V_{GS} in steady state. Gate current is defined by the <PL_SD_SINK_LEVEL[1:0]> EEPROM bits.

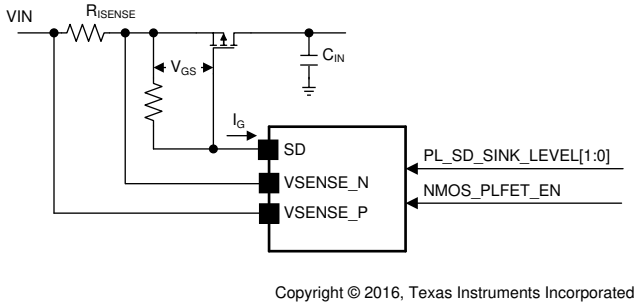

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図 6-18. Power-line FET Control

During a shutdown state the LP8860-Q1 closes the power-line FET and prevents possible boost and LED leakage. Sense pins are used to detect overcurrent. Power-line FET is closed when an OCP fault occurs. A VIN OCP is indicated with PL_FET_FAULT bit. The power-line FET closes with all faults, followed by entering to a recovery state.

When it is not possible to choose a pFET with the necessary characteristics, a schematic with nFET can be used (see *セクション 6.3.7* section, 図 6-17); the <NMOS_PLFET_EN EEPROM> bit must be set accordingly. In this case the SD pin provides current to shut down the power-line nFET during fault condition.

6.3.9 Protection and Fault Detection Modes

The LP8860-Q1 has fault detection for LED outputs, low and high input voltage, power line overcurrent, boost overcurrent, boost overvoltage, and charge pump overload. In addition, the device has thermal shutdown and LED overtemperature protection with an external NTC thermistor.

Faults have dedicated fault flags in registers <FAULT> and <LED_FAULT>. Mask bits can be used to disable certain faults (see 表 6-17 for details). In addition the open-drain output pin FAULT can be used to indicate occurred fault. Writing CLEAR_FAULTS or setting the NSS pin (I^2C interface mode only) high resets the fault. Setting the VDDIO/EN pin low, then high again, resets the faults as well.

6.3.9.1 LED Fault Comparators and Adaptive Boost Control

Every LED current sink has 3 comparators for adaptive boost control and fault detection. Each comparator outputs is filtered. Filter control bits <BL_COMP_FILTER_SEL [3:0]> select how many PWM generator clock cycles (5 MHz if PLL disabled or PLL clock) high/mid comparator is filtered before it is used to detect shorted LEDs and boost voltage down-scaling. Usually 1 µs is sufficient; for 5-MHz frequency it means <BL_COMP_FILTER_SEL [3:0]> = 0000b, 10 MHz = 0001b, 20 MHz = 0010b, and 40 MHz = 0011b.

Adaptive boost-control function adjusts the boost output voltage to the minimum sufficient voltage for proper LED current sink operation. The output with the highest V_F LED string is detected and the boost output voltage adjusted accordingly. Current sink headroom can be adjusted with EEPROM bits <DRV_HEADR[2:0]>. Boost adaptive control voltage step size is 125 mV. Boost adaptive control operates similarly with and without PSPWM. Additionally, when faster boost response is needed in larger brightness steps, the "jump" command can be used. Jump allows increase of the boost voltage with greater steps. Jump is enabled with the <EN_JUMP> EEPROM bit. The threshold for the magnitude of brightness increase that requires use of jump can be set with the

<JUMP_STEP_SIZE[1:0]> EEPROM bits. <BRIGHTNESS_JUMP_THRES[1:0]> EEPROM bits define when the jump command is activated.

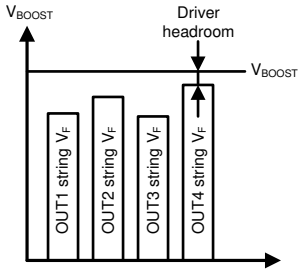

図 6-19. Boost Voltage Adaptation

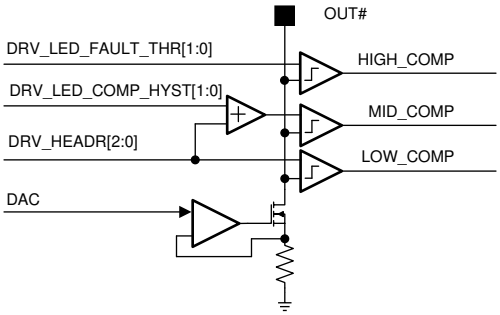

図 6-20. Output Voltage Comparators

図 6-21 shows different cases which cause boost voltage increase, decrease, or generate faults.

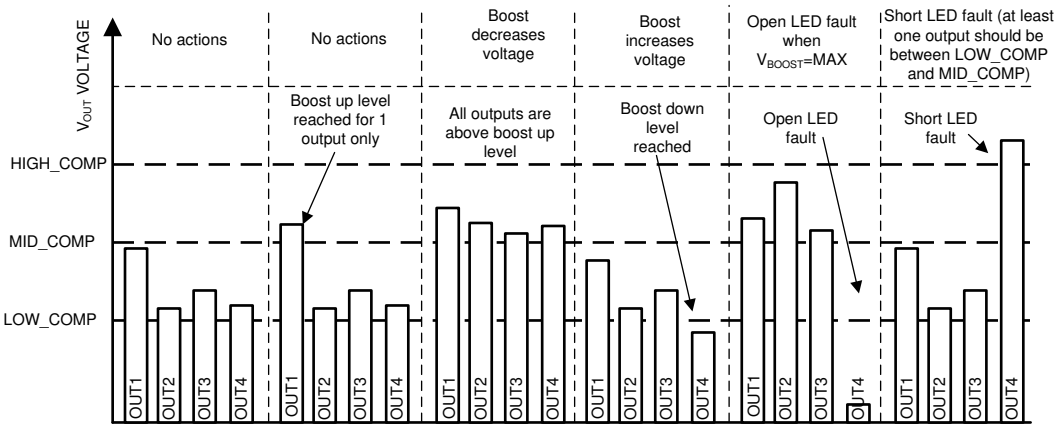

図 6-21. Protection and Boost Adaptation Algorithms

注

In the Cluster mode, if voltage of one or more outputs is below LOW_COMP, it causes open LED fault detection.

6.3.9.2 LED Current Dimming With Internal Temperature Sensor

The LP8860-Q1 can prevent thermal shutdown (TSD) by reducing the average LED strings current based on die temperature.

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When die temperature reaches <INT_TEMP_LIM[1:0]> EEPROM bits-defined threshold, the device automatically lowers the brightness (2.25% / °C typical). Depending on brightness control mode either PWM duty cycle or current is used for average current reduction.

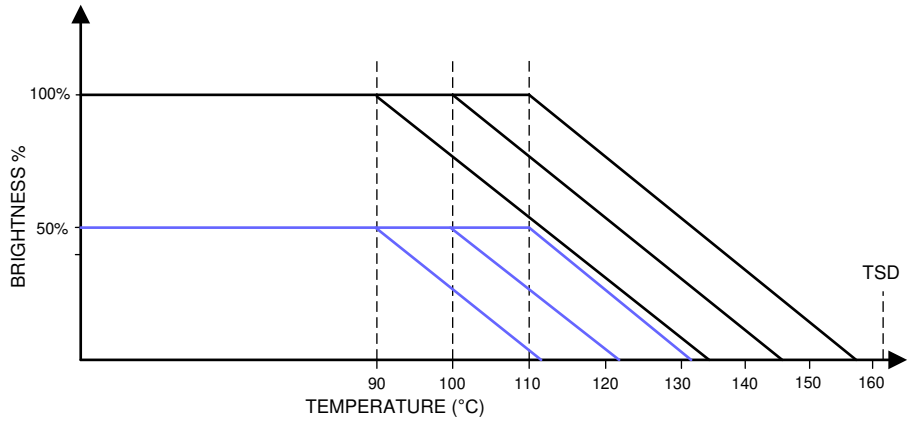

図 6-22. Thermal De-Rating Function Example With 100% and 50% Brightness

表 6-15. Thermal De-rating Function Temperature Thresholds

INT_TEMP_LIM[1:0]	TEMPERATURE
00	disabled
01	90°C
10	100°C
11	110°C

表 6-16. Temperature ADC Output for Different Temperatures

TEMPERATURE (°C)	DECIMAL OUTPUT VALUE OF TEMP[10:0] REGISTER	
	VDD 3.6 (V)	VDD 5 (V)
–40	885	891
–35	901	907
–30	916	923
–25	932	939
–20	948	954
–15	964	970
-10	980	986
-5	994	1002
0	1010	1018
5	1026	1034
10	1041	1050
15	1057	1066
20	1073	1082
25	1089	1098
30	1105	1115
35	1121	1131
40	1137	1147
45	1154	1163
50	1170	1180

表 6-16. Temperature ADC Output for Different Temperatures (続き)

TEMPERATURE (°C)	DECIMAL OUTPUT VALUE OF TEMP[10:0] REGISTER	
	VDD 3.6 (V)	VDD 5 (V)
55	1186	1196
60	1202	1212
65	1219	1229
70	1235	1245
75	1252	1262
80	1268	1278
85	1285	1293
90	1301	1310
95	1318	1328
100	1332	1343
105	1349	1359
110	1365	1375

6.3.9.3 LED Current Limitation With External NTC Sensor

The <EXT_TEMP_COMP_EN> EEPROM bit enables the LED current limitation mode. The principle of current limitation is shown in 図 6-23.

When LED temperature reaches <EXT_TEMP_LEVEL_LOW[3:0]> level, the device automatically tries to reduce LED average current step-by-step by 3.125% from maximum brightness value. Step time is defined by <EXT_TEMP_PERIOD[4:0]> EEPROM bits. If temperature continues to increase and reaches <EXT_TEMP_LEVEL_HIGH[3:0]> level, the device shuts down the LEDs and generates a fault condition. The LEDs are turned on automatically when the temperature is below the <EXT_TEMP_LEVEL_LOW[3:0]> level. Otherwise, if after one or more steps the temperature drops down below <EXT_TEMP_LEVEL_LOW[3:0]>, brightness increases with the same step time until it reaches the original level. The LP8860-Q1 uses PWM duty reduction to reduce LED current. The device detects external NTC resistor availability, and the <TEMP_RES_MISSING> flag is set, if the NTC sensor is missing (resistance is 2 MΩ or more).

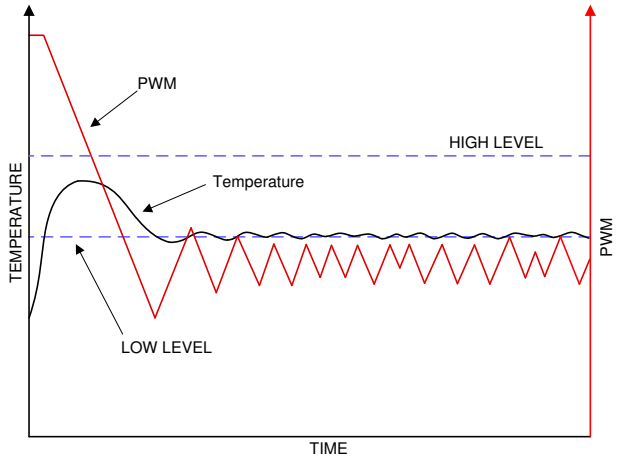

図 6-23. LED Current Limitation With NTC

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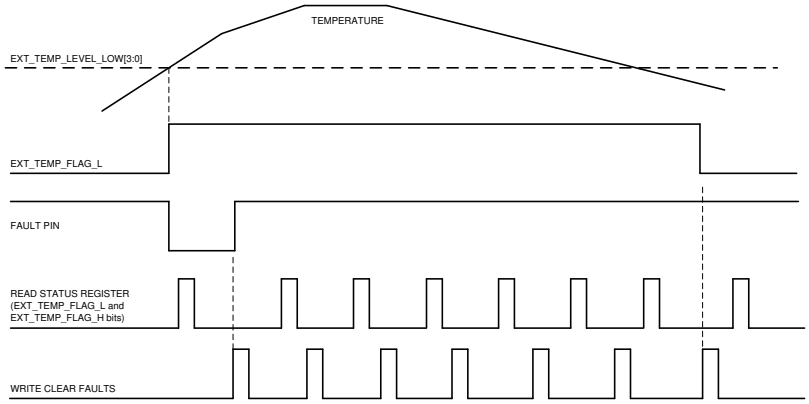

図 6-24. Timing Diagram for LED Current Limitation With NTC

6.3.9.4 LED Current Dimming With External NTC Sensor

When an external resistor for maximum current control is used, current dimming for LED current can be used also. In this case LED current can be de-rated when ambient temperature is high. This option must be enabled by <EXT_TEMP_I_DIMMING_EN> and <EXT_TEMP_COMP_EN> EEPROM bits.

Knee point and slope are defined by <EXT_TEMP_MINUS[1:0]> and <EXT_TEMP_GAIN[3:0]> EEPROM bits respectively. LED shutdown temperature is defined by <EXT_TEMP_LEVEL_HIGH[3:0]> bits. Serial and parallel resistors R1 and R2 affect the slope and knee point and can be used for the thermal curve adjustment and NTC linearization.

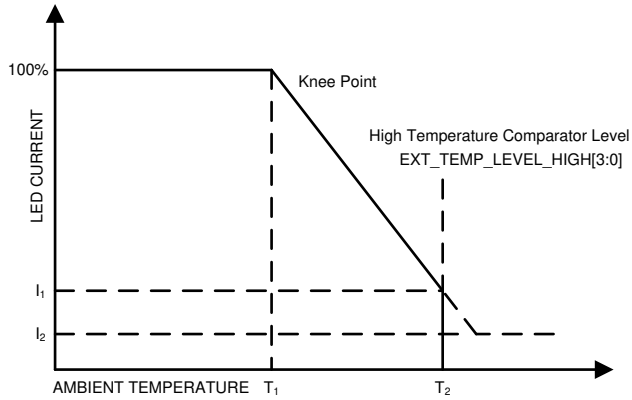

図 6-25. Current Dimming for High Ambient Temperature

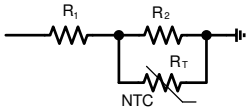

図 6-26. NTC Linearization

図 6-27 and 図 6-28 show the block diagrams for current dimming.

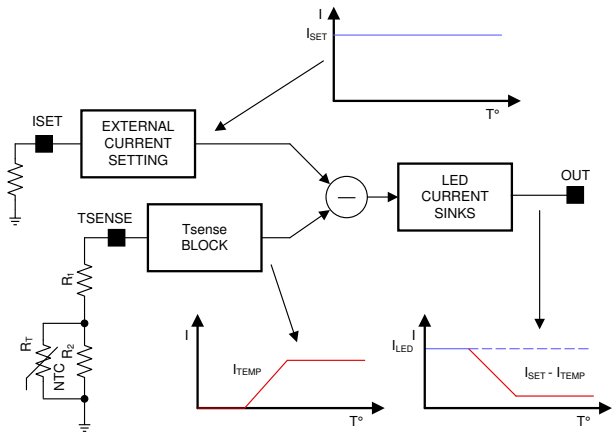

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図 6-27. Temperature-Dependent NTC Current (Subtracted from ISET Current)

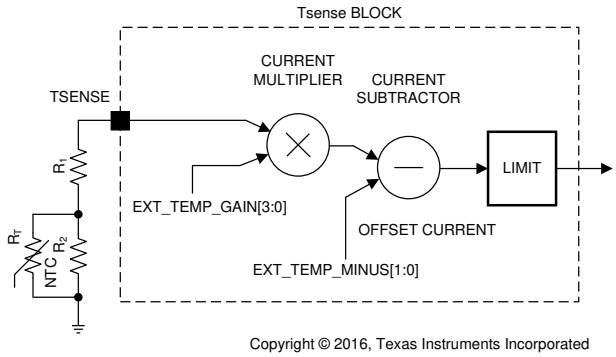

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図 6-28. NTC Current Processing — Scaling, Shift, and Limitation

Current dimming by external NTC sensor for 150-mA scale can be defined by formulas:

$$I_{SET} = \frac{V_{BG}}{50 \times R_{ISET}} \times 1000 \tag{6}$$

$$I_{TEMP} = \left[\frac{\left(\frac{V_{BG}}{R1 + \frac{R2 \times R_{NTC}}{R2 + R_{NTC}}} \times 1000 + 3.57\mu A \right)}{EXT_TEMP_GAIN[3:0]} \right] - EXT_TEMP_MINUS[1:0] \tag{7}$$

I_{TEMP} cannot be negative; if $I_{TEMP} < 0$, then I_{TEMP} must be 0.

$$I_{LED} = (I_{SET} - I_{TEMP}) \times 150\ mA \tag{8}$$

I_{LED} cannot go below a 5-mA level; if calculated $I_{LED} < 5$ mA, then $I_{LED} = 5$ mA.

where

- I_{SET}: Maximum current setting with external resistor R_{ISET}, µA
- I_{TEMP}: Temperature compensation, µA
- R_{ISET}: External resistor, kΩ
- R1, R2: Resistors for adjustment, kΩ
- I_{LED}: Output current per channel, mA
- EXT_TEMP_MINUS[1:0]: 1, 5, 9, 13 µA
- EXT_TEMP_GAIN[[3:0]: 50/n, n = 16 to 1
- V_{BG}: 1.2 V

6.3.9.5 Protection Feature and Fault Summary

表 6-17 summarizes protection features and related faults.

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表 6-17. Overview of the Fault/Protection Schemes

FAULT/ PROTECTION	FAULT NAME	THRESHOLD		ACTION[1] [2]	MASK[4]	FAULT CLEARING[3] [5]
Input overvoltage protection	VIN_OVP	OVP_LEVEL[1:0] (V)		VIN overvoltage monitored from soft start. Fault causes entry to FAULT_RECOVERY state. If device is restarted successfully with recovery timer, the fault register bit is not automatically cleared. FAULT pin is pulled low.	MASK_OVP_FSM Masks fault recovery, but not status and fault pin operations	Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
		00	OFF			
		01	7			
		10	11			
		11	22.5			
Input undervoltage protection	VIN_UVLO	UVLO_LEVEL[1:0] (V)		VIN undervoltage monitored from soft start. Fault causes entry to FAULT_RECOVERY state. If device is restarted successfully with recovery timer, the fault register bit is not automatically cleared. FAULT pin is pulled low.	MASK_VIN_UVLO Masks fault recovery, status and fault pin operations	Fault bit and FAULT pin: 1.POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
		00	OFF			
		01	3			
		10	5			
		11	8			
VDD undervoltage protection	VDD_UVLO	VDD_UVLO_LEVEL Threshold (V)		Device enters STANDBY state. Recovers when fault disappears. All registers are cleared or reloaded from EEPROM (if defined) with exception registers 0x00, 0x01, 0x04…0x0C. After recovery LP8860-Q1 provides the same brightness as before fault detection, if DISP_CL1_CURRENT[11:0] context stays same as LED_CURRENT_CTRL[11:0] EEPROM setting. If VDD voltage goes below POR level, registers 0x00, 0x01, 0x04…0x0C are cleared. This fault does not have any flags and doesn't generate FAULT. Voltage hysteresis is 50 mV (typical).		
		0	2.5			
		1	3			
Boost overcurrent protection	BOOST_OCP	V_{BOOST} longer than 110 ms 5 V (typical) below set value. Set value is voltage value defined by logic during adaptation in adaptive mode or initial boost voltage setting in manual mode.		Fault monitoring started from boost start. Fault causes entry to FAULT_RECOVERY state. If device is restarted successfully with recovery timer, the fault register bit is not automatically cleared. FAULT pin is pulled low.	MASK_BOOST_OCP_ FSM Masks fault recovery, but not status and fault pin operations	Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
Boost overvoltage protection	BOOST_OVP	V_{BOOST} voltage 1.6 V (typical) above set value Set value is voltage value defined by logic during adaptation in adaptive mode or initial boost voltage setting in manual mode.		Boost OVP fault monitored during normal operation FAULT pin is pulled low.	MASK_BOOST_OVP_ STATUS	Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin

表 6-17. Overview of the Fault/Protection Schemes (続き)

FAULT/ PROTECTION	FAULT NAME	THRESHOLD		ACTION[1] [2]	MASK[4]	FAULT CLEARING[3] [5]
Input voltage overcurrent protection	PL_FET_FAULT	PL_SD_LEVEL[1:0] (A)		Fault is detected with 2 methods: 1. Detects overcurrent from soft start by measuring R_{ISENSE} voltage. 2. Detects FB voltage at the end of soft start. If voltage is below 1.2 V, fault is detected. Fault causes entry to FAULT_RECOVERY state. If device is restarted successfully with recovery timer, the fault register bit is not automatically cleared. FAULT pin is pulled low.		Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
		10	6			
		11	8			
Short LED fault	SHORT_LED	DRV_LED_FAULT_THR[1:0] (V)		LED output in display mode: Triggered if one or more outputs voltage is above DRV_LED_FAULT_THR and at least one LED output voltage is between DRV_HEADR and DRV_HEADR + DRV_LED_COMP_HYST. Is set only if LED faults are enabled in EEPROM. Shorted string is removed from voltage control loop and LED current sink n is disabled. LED output in cluster mode: If one or more outputs voltage above DRV_LED_FAULT_THR fault is detected. Is pulled low only if LED faults are enabled in EEPROM. Shorted string PWM output is disabled. FAULT pin is pulled low.	EN_DISPLAY_LED_ FAULT for LEDs in display mode EN_CL_LED_FAULT for LEDs in cluster mode	Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin When fault is cleared it can be set again only during next POR or if there is another LED short fault in different output.
		00	3.6			
		01	3.6			
		10	6.9			
		11	10.6			
		DRV_LED_COMP_HYST[1:0] (mV)				
		00	1000			
		01	750			
		10	500			
		11	250			
Open LED fault	OPEN_LED	DRV_HEADR[2:0] (mV)		LED output in display mode: Triggered if one or more outputs voltage is below DRV_HEADR, and boost adaptive control has reach the maximum voltage. Is set only if led faults enabled in EEPROM. Open string is removed from voltage control loop and PWM generation is disabled. LED output in cluster mode: Triggered if one or more outputs voltage is below DRV_HEADR. Is set only if LED faults enabled in EEPROM. Open string PWM generation is disabled. FAULT pin is pulled low.	EN_DISPLAY_LED_FAULT for LEDs in display mode EN_CL_LED_FAULT for LEDs in cluster mode	Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin When open fault is cleared it can set again only during next power-up or if there is another LED open fault.
		111	V_{SAT}+50			
		110	V_{SAT}+175			
		101	V_{SAT}+300			
		100	V_{SAT}+450			
		011	V_{SAT}+575			
		010	V_{SAT}+700			
		001	V_{SAT}+875			
		000	V_{SAT}+1000			
LED faults	LED_FAULT[4:1]			Defines which string has either open or short fault. Cleared only during power down.		POR or VDDIO/EN
Charge pump fault	CP_2X_FAULT	V_{CPUMD} < 0.85 × (2 × V_{DD}) (typical)		Charge pump voltage not high enough condition. Fault causes entry to FAULT_RECOVERY state. CP voltage monitored from the boost soft start. If device is restarted successfully with recovery timer, the fault register bit is not automatically cleared. FAULT pin is pulled low.		Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin

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表 6-17. Overview of the Fault/Protection Schemes (続き)

FAULT/ PROTECTION	FAULT NAME	THRESHOLD	ACTION(1) (2)	MASK(4)	FAULT CLEARING(3) (5)
Thermal Current Limit (LED Outputs)	No faults	INT_TEMP_LIM[1:0] 00 disabled 01 90°C 10 100°C 11 110°C	When die temperature increases temperature defined by INT_TEMP_LIM[1:0] the device automatically lowers the PWM duty for outputs 2.25%/°C (typical). For Hybrid PWM and Current dimming mode current is used for brightness reduction as well.		
Thermal LED Current Limit with external NTC sensor.	EXT_TEMP_ FLAG_L	EXT_TEMP_LEVEL_LOW[3:0] Setting / Level (kΩ) 0000 79.67 0001 43.35 0010 29.77 0011 22.67 0100 18.30 0101 15.34 0110 13.21 0111 11.60 1000 10.34 1001 9.32 1010 8.49 1011 7.79 1100 7.20 1101 6.69 1110 6.25 1111 5.87	Fault is monitored during normal operation. If EXT_TEMP_LEVEL_LOW[3:0] is exceeded, LED current is reduced. FAULT pin is pulled low when EXT_TEMP_FLAG_L goes high.	EXT_TEMP_COMP _EN=0 disables fault	Fault bit: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin when fault deasserted. Fault pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
	EXT_TEMP_ FLAG_H	EXT_TEMP_LEVEL_HIGH[3:0] Setting / Level (kΩ) 0000 79.67 0001 43.35 0010 29.77 0011 22.67 0100 18.30 0101 15.34 0110 13.21 0111 11.60 1000 10.34 1001 9.32 1010 8.49 1011 7.79 1100 7.20 1101 6.69 1110 6.25 1111 5.87	Fault is monitored during normal operation. If EXT_TEMP_LEVEL_HIGH[3:0] limit is exceeded, the LED outputs are turned off. FAULT pin is pulled low.	EXT_TEMP_COMP _EN=0 disables fault	Fault bit: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin when fault deasserted. Fault pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
NTC missing	TEMP_RES _ MISSING	Resistance > 2 MΩ	NTC is missing. Fault is monitored during normal operation. Not connected to FAULT output pin. TEMP_RES_FAULT is monitored if EXT_TEMP_COMP_EN EEPROM bit has been enabled	EXT_TEMP_COMP _EN=0 disables fault	1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin
Thermal shutdown	TSD	Rising temperature =165°C Falling temperature = 135°C	Thermal shutdown is monitored from soft start. Fault causes entry to the FAULT_RECOVERY state. FAULT pin is pulled low.		Fault bit and FAULT pin: 1. POR or VDDIO/EN 2. Writing CLEAR_FAULTS bit or toggling NSS pin

(1) Recovery time is 100 ms.

(2) During fault recovery state the LED outputs and boost is shut down and power-line FET is turned off.
(3) If fault is cleared during fault recovery state, FAULT pin is pulled low again after recovery state, if this fault still exists.
(4) If fault recovery is masked, fault bit sets again after cleaning.
(5) The NSS pin can be used for fault reset only for I^{2}C interface mode. NSS is level sensitive; be aware NSS is set to low after fault reset.

Fault detection is digitally filtered — filtering time for different faults is shown in 表 6-18.

表 6-18. Fault Filters

FAULT/PROTECTON	FAULT NAME	TIME	ENABLED
Boost Overcurrent Protection	BOOST_OCP	110 ms	From boost start
Boost Overvoltage Protection	BOOST_OVP	100 µs	In normal mode
Input Overvoltage Protection	VIN_OVP	100 µs	From soft start
Input Undervoltage Protection	VIN_UVLO	100 µs	From soft start
Input Overcurrent Protection	PL_FET_FAULT	100 µs	From soft start
VDD Undervoltage Protection	VDD_UVLO	5 µs	Always
Thermal Shutdown	TSD	100 µs	From soft start
Charge Pump fault	CP_2X_FAULT	10 µs	From boost start
Thermal LED Current Limit with external NTC sensor.	EXT_TEMP_FLAG_H	10 µs	In normal mode
	EXT_TEMP_FLAG_L	10 µs	In normal mode
NTC missing	TEMP_RES_FAULT	100 µs	In normal mode

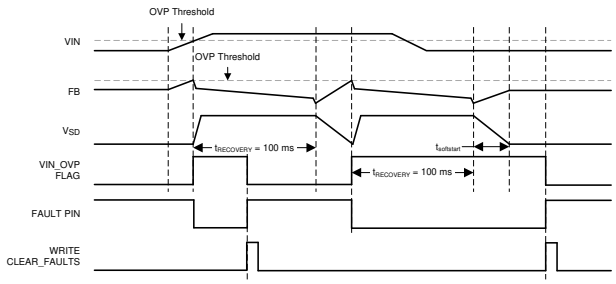

図 6-29. Input OVP Triggering and Recovery

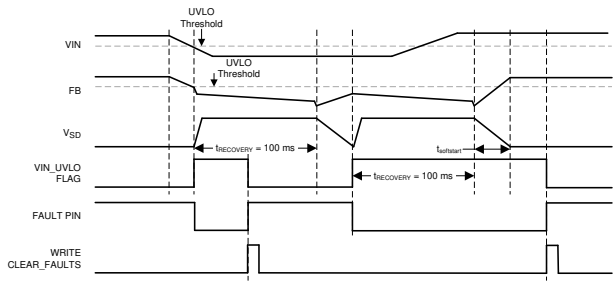

図 6-30. Input UVLO Triggering and Recovery

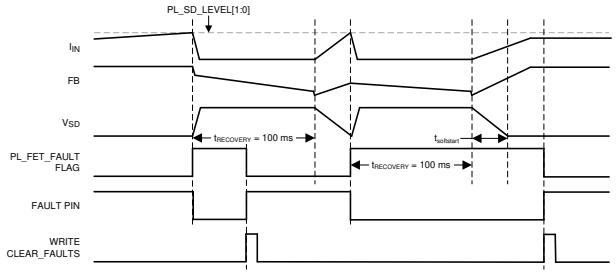

図 6-31. Input OVP Triggering and Recovery

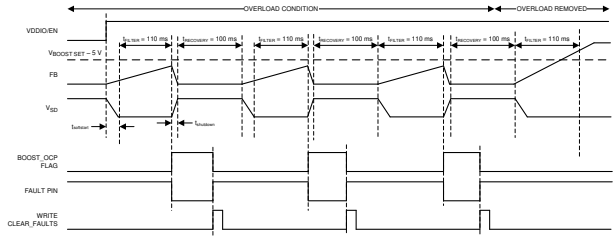

図 6-32. Boost OCP Triggering and Recovery

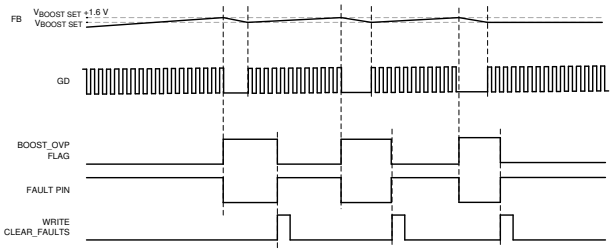

図 6-33. Boost OVP Triggering and Recovery

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6.4 Device Functional Modes

6.4.1 Standby Mode

The device is in standby mode when the EN/VDDIO pin is low. Current consumption from the VDD pin in this mode is typically 1 µA.

6.4.2 Active Mode

The EN/VDDIO pin enables the logic and analog blocks. The device goes through the start-up sequence where EEPROM context is loaded to the registers, the power-line FET is enabled during soft start, and boost starts during boost start-time. In this mode I^{2}C and SPI communication are available after soft start, and register settings can be changed.

6.4.3 Fault Recovery State

Fault recovery state is special state which can be caused by faults. In this state power line FET is switched off, boost and LED current sinks are disabled. I^{2}C or SPI interfaces are available in this state — for example, fault flags can be read.

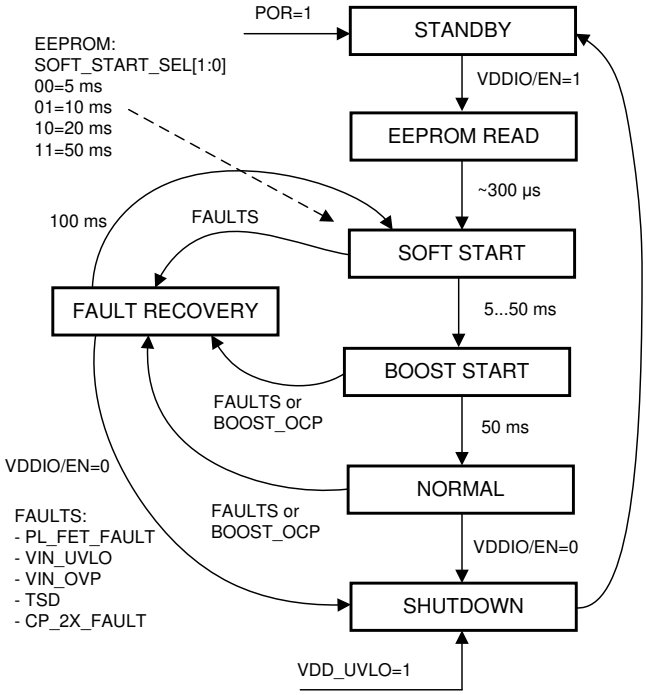

図 6-34. State Diagram

6.4.4 Start-Up and Shutdown Sequences

Depending on EEPROM settings the LP8860-Q1 can be started up or shut down differently. Typical start-up/shutdown sequence is shown in 図 6-35.

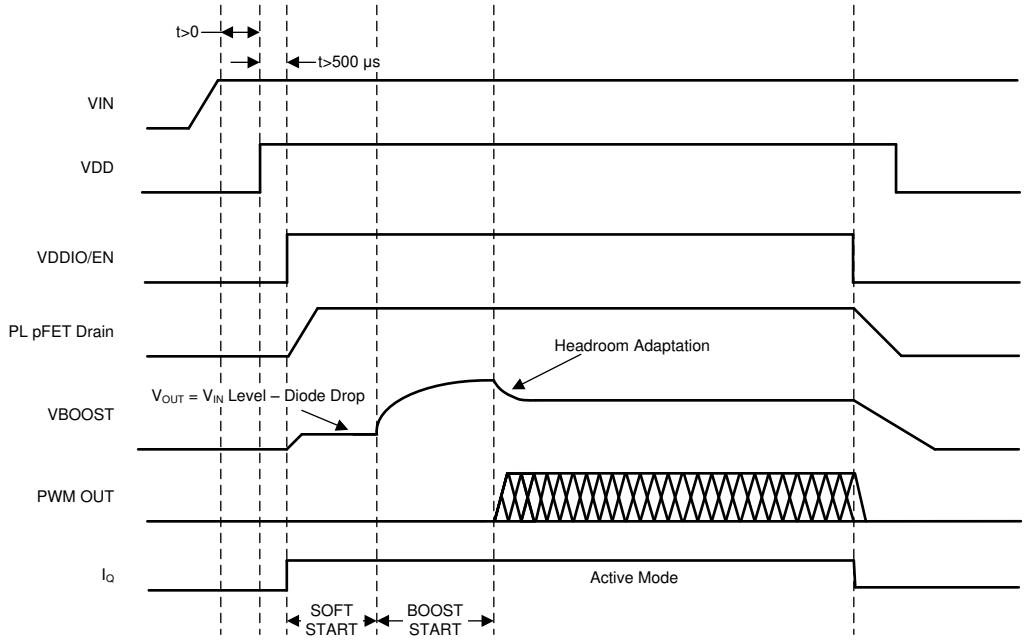

図 6-35. Timing Diagram for the Typical Start-Up and Shutdown

6.5 Programming

6.5.1 EEPROM

EEPROM memory stores various parameters for chip control. The 200-bit EEPROM memory is organized as 25 × 8 bits. The EEPROM structure consists of a register front-end and the non-volatile memory (NVM). Register data can be read and written through the I^{2}C/SPI serial interface. EEPROM must be burned with the new data; otherwise, data disappears after power-on reset or VDDIO/EN cycling. PWM outputs and PLL must be disabled when writing to EEPROM registers or burning EEPROM (<DISP_CL1_BRT[15:0]> = 0, <CL2_BRT[12:0]> = 0, <CL3_BRT[12:0]> = 0, <CL2_BRT[12:0]> = 0, <EN_PLL> = 0). To read and program EEPROM NVM separate commands need to be sent. Erase and program voltages are generated internally; no other voltages other than the normal VDD voltage is required. A complete EEPROM memory map is shown in the 表 6-23.

The user must make sure that VDD power is on, and the VDDIO/EN pin is kept high, during the whole programming/burn sequence to avoid memory corruption.

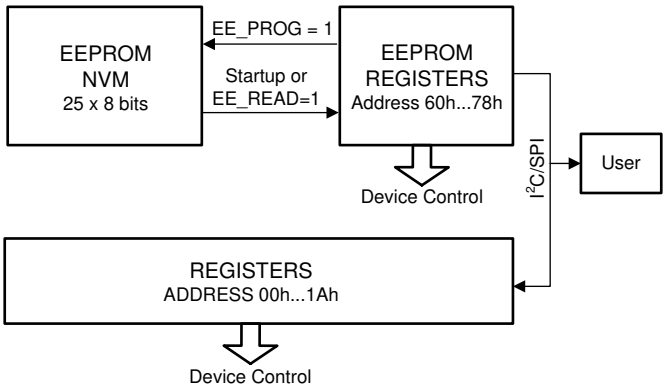

図 6-36. EEPROM and Register Configuration

EEPROM has protection against accidental writes. EEPROM access can be unlocked by writing a pass code to the EEPROM_UNLOCK register. It unlocks the EEPROM Control register EEPROM_CNTRL and all EEPROM

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registers. Lock is enabled again by writing any other code to the EEPROM_UNLOCK register (for example, 0x00 enables the lock any time).

表 6-19. EEPROM Pass Code Protection

PASS CODE TO EEPROM_UNLOCK REGISTER
0x08, 0xBA, 0xEF

EEPROM is used as fixed product-configuration storage, to be set or programmed during production before normal operation. EEPROM can be reprogrammed for evaluation purposes up to 1000 cycles. Data-retention lifetime for factory-programmed content is 10 years, minimum. For more details regarding EEPROM options, see TI Application Note *Selecting the Correct LP8860-Q1 EEPROM Version* (SNVA757).

6.5.2 Serial Interface

The LP8860-Q1 supports 2 different interface modes:

- SPI interface (4-wire serial)
- I²C-compatible (2-wire serial)

The user can define the interface mode by IF pin as shown in 表 6-20. The LP8860-Q1 detects interface mode selection during start-up. When the device is in normal mode, the IF signal does not affect the interface selection.

表 6-20. Interface Modes

IF PIN	INTERFACE
GND	I²C
VDDIO	SPI

6.5.2.1 SPI Interface

The LP8860-Q1 is compatible with SPI serial-bus specification, and it operates as a slave. The transmission consists of 16-bit write and read cycles. One cycle consists of 7 address bits, 1 read/write (R/W) bit, and 8 data bits. The R/W bit high state defines a write cycle and low defines a read cycle. MISO output is normally in a high-impedance state. When the slave select NSS for LP8680 is active (that is, low), MISO output is pulled low for both read and write operations, except for the period when Data is sent out during a read cycle. The Address and Data are transmitted MSB first. The Slave Select signal NSS must be low during the Cycle transmission. NSS resets the interface when high, and it has to be taken high between successive cycles. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

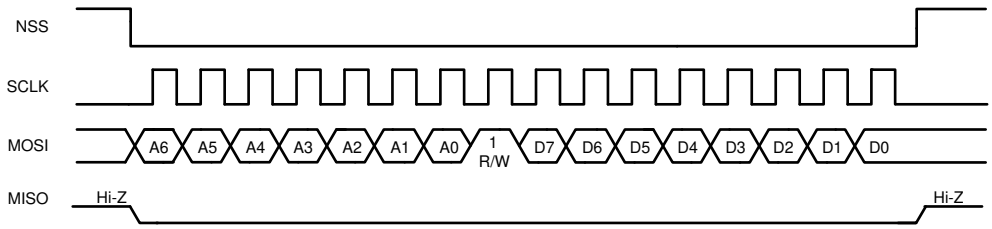

図 6-37. SPI Write Cycle

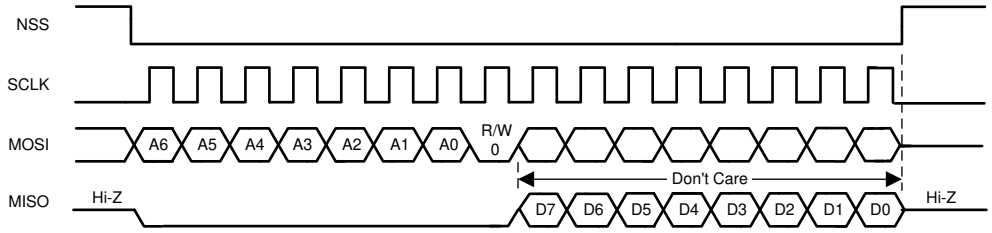

図 6-38. SPI Read Cycle

6.5.2.2 I²C Serial Bus Interface

6.5.2.2.1 Interface Bus Overview

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol is using a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines must be connected to a positive supply through a pullup resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCL. The LP8860-Q1 is always a slave device.

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6.5.2.2.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the SCL. Consequently, throughout the clock high period, the data must remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data must be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

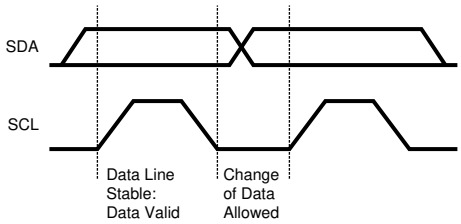

図 6-39. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

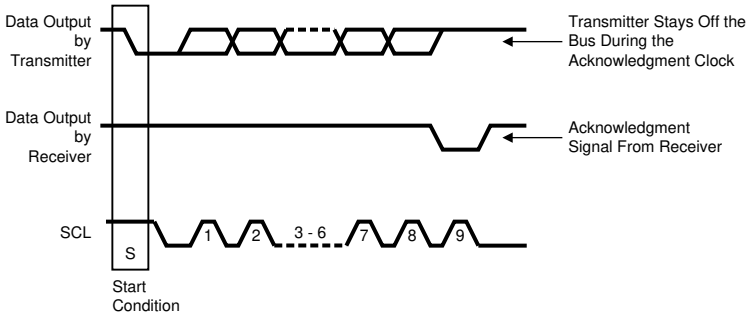

図 6-40. Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

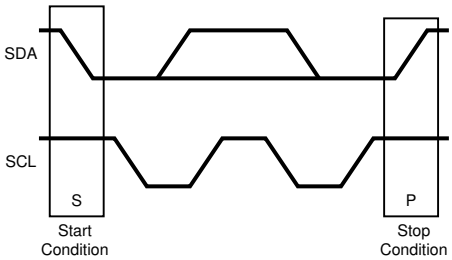

図 6-41. Stop and Start Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

6.5.2.2.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

6.5.2.2.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*") the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

6.5.2.2.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8860-Q1 operates as a slave device with 7-bit address combined with data direction bit. Default slave address is 2Dh as 7-bit or 5Ah for write and 5Bh for read in 8-bit format.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device sends an acknowledge signal on the SDA line, once it recognizes its address. The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit. When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

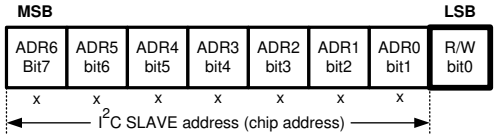

図 6-42. Address and Read/Write Bit

6.5.2.2.6 Control Register Write Cycle

1. Master device generates start condition.
2. Master device sends slave address (7 bits) and the data direction bit (r/w = "0").
3. Slave device sends acknowledge signal if the slave address is correct.
4. Master sends control register address (8 bits).
5. Slave sends acknowledge signal.
6. Master sends data byte to be written to the address register.
7. Slave sends acknowledgement.
8. Write cycle ends when the master creates stop condition.

6.5.2.2.7 Control Register Read Cycle

1. Master device generates start condition.
2. Master device sends slave address (7 bits) and the data direction bit (r/w = "0").
3. Slave device sends acknowledge signal if the slave address is correct.
4. Master sends control register address (8 bits).
5. Slave sends acknowledge signal if slave address is correct.
6. Master generates repeated start condition

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7. Master sends the slave address (7 bits) and the data direction bit (r/w = “1”)
8. Slave sends acknowledgment if the slave address is correct.
9. Read cycle ends when master does not generate acknowledge signal after data byte and generates stop condition.

表 6-21. Data Read and Write Cycles

MODE	ACTION[(1)]
Data Read	<Start Condition>
	<Slave Address><r/w = ‘0’>[Ack]
	<Register Addr.>[Ack]
	<Repeated Start Condition>
	<Slave Address><r/w = ‘1’>[Ack]
	[Register Data]<Ack or Nack>
	register address possible
	<Stop Condition>
Data Write	<Start Condition>
	<Slave Address><r/w=’0’>[Ack]
	<Register Addr.>[Ack]
	<Register Data>[Ack]
	register address possible
	<Stop Condition>

(1) <> Data from master; [] Data from slave

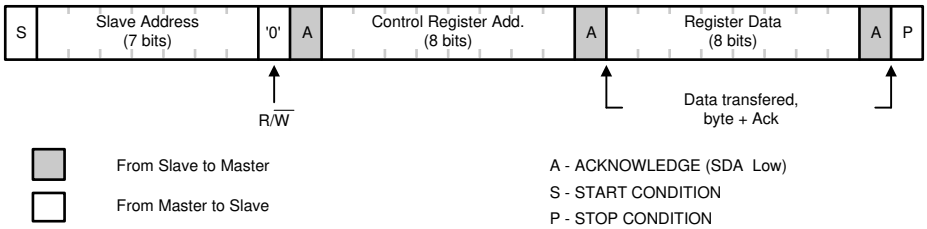

図 6-43. Register Write Format

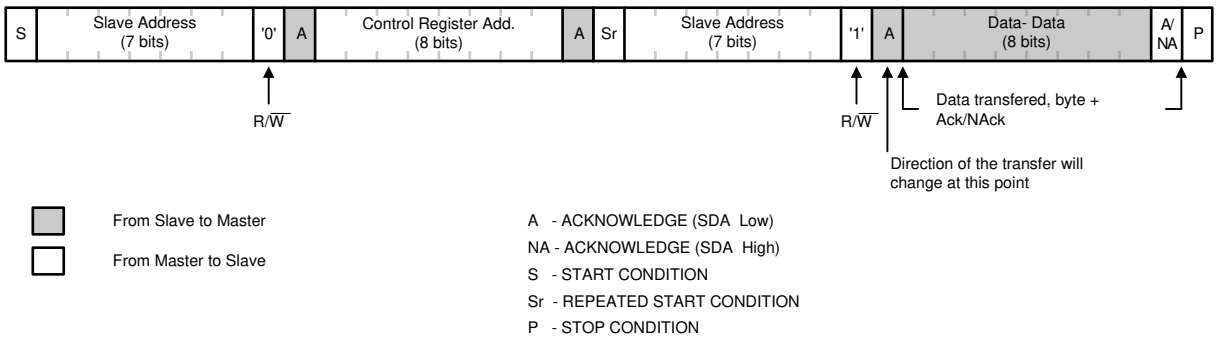

図 6-44. Register Read Format

6.6 Register Maps

表 6-22. Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0x00	DISP_CL1_BRT	DISP_CL1_BRT[15:8]							
0x01		DISP_CL1_BRT[7:0]							
0x02	DISP_CL1_CURRENT	RESERVED				DISP_CL1_CURRENT[11:8]			
0x03		DISP_CL1_CURRENT[7:0]							
0x04	CL2_BRT	RESERVED			CL2_BRT[12:8]				
0x05		CL2_BRT[7:0]							
0x06	CL2_CURRENT	CL2_CURRENT[7:0]							
0x07	CL3_BRT	RESERVED			CL3_BRT[12:8]				
0x08		CL3_BRT[7:0]							
0x09	CL3_CURRENT	CL3_CURRENT[7:0]							
0x0A	CL4_BRT	RESERVED			CL4_BRT[12:8]				
0x0B		CL4_BRT[7:0]							
0x0C	CL4_CURRENT	CL4_CURRENT[7:0]							
0x0D	CONFIGURATION	RESERVED	DRV_LED_CURENT_SCALE[2:0]			EN_ADVANCED_ SLOPE	PWM_SLOPE[2:0]		
0x0E	STATUS	RESERVED				BRT_SLOPE_ DONE	TEMP_RES_ MISSING	EXT_TEMP_ FLAG_L	EXT_TEMP_ FLAG_H
0x0F	FAULT	RESERVED	VIN_OVP	VIN_UVLO	TSD	BOOST_OCP	BOOST_OVP	PL_FET_ FAULT	CP_2X_ FAULT
0x10	LED FAULT	RESERVED		OPEN_LED	SHORT_LED	LED_FAULT[4:1]			
0x11	FAULT CLEAR	RESERVED							CLEAR_FAULTS
0x12	ID	FULL_LAYER_REVISION				METAL_REVISION			
0x13	TEMP MSB	RESERVED					TEMP[10:8]		
0x14	TEMP LSB	TEMP[7:0]							
0x15	DISP LED CURRENT	RESERVED				LED_CURRENT[11:8]			
0x16		LED_CURRENT[7:0]							
0x17	DISP LED PWM	PWM[15:8]							
0x18		PWM[7:0]							
0x19	EEPROM_CNTRL	EE_READY	RESERVED					EE_PROG	EE_READ
0x1A	EEPROM_UNLOCK	EEPROM_UNLOCK_CODE[7:0]							

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表 6-23. EEPROM Register Map (1)

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0x60	EEPROM REG 0	EXT_TEMP_MINUS[1:0]		DRV_LED_BIAS_CTRL[1:0]		LED_CURRENT_CTRL[11:8]			
0x61	EEPROM REG 1	LED_CURRENT_CTRL[7:0]							
0x62	EEPROM REG 2	RESERVED	EN_STEADY_ DITHER	PWM_INPUT_HYSTERESIS[1:0]		EN_ADVANCED_SLOPE	PWM_SLOPE[2:0]		
0x63	EEPROM REG 3	EN_DISPAY_LED_ FAULT	DRV_LED_CURRENT_SCALE[2:0]			LED_STRING_CONF[2:0]			EN-PWM_I
0x64	EEPROM REG 4	EN_CL_LED_ FAULT	DRV_LED_COMP_HYST[1:0]		DRV_LED_FAULT_THR[1:0]		DRV_HEADR[2:0]		
0x65	EEPROM REG 5	I_SLOPE[2:0]			PWM_RESOLUTION[1:0]		DITHER[2:0]		
0x66	EEPROM REG 6	RESERVED	GAIN_CTRL[2:0]			DRV_EN_EXT_ LED_CUR_CTR	DRV_EN_SPLIT_FET	BRT_MODE[1:0]	
0x67	EEPROM REG 7	DRV_OUT2_CORR[3:0]				DRV_OUT1_CORR[3:0]			
0x68	EEPROM REG 8	DRV_OUT4_CORR[3:0]				DRV_OUT3_CORR[3:0]			
0x69	EEPROM REG 9	EXT_TEMP_GAIN[3:0]				BL_COMP_FILTER_SEL[3:0]			
0x6A	EEPROM REG 10	EXT_TEMP_I_ DIMMING_EN	NMOS_PLFET_ EN	SOFT_START_SEL[1:0]		PL_SD_LEVEL[1:0]		PL_SD_SINK_LEVEL[1:0]	
0x6B	EEPROM REG 11	SLOW_PLL_DIV[12:5]							
0x6C	EEPROM REG 12	EN_SYNC	PWM_SYNC	PWM_ COUNTER_ RESET	SLOW_PLL_DIV[4:0]				
0x6D	EEPROM REG 13	R_SELL[1:0]		SEL_DIVIDER	EN_PLL	SYNC_PRE_DIVIDER[3:0]			
0x6E	EEPROM REG 14	RESERVED			SYNC_TYPE	PWM_FREQ[3:0]			
0x6F	EEPROM REG 15	MASK_BOOST_ OVP_FSM	MASK_BOOST_ OCP_FSM	MASK_OVP_ FSM	MASK_VIN_ UVLO	UVLO_LEVEL[1:0]		OVP_LEVEL[1:0]	
0x70	EEPROM REG 16	RESERVED		BOOST_EN_ IRAMP _SU_ DELAY	BOOST_EXT_ CLK_SEL	BOOST_IMAX_SEL[2:0]			BOOST_GD_ VOLT
0x71	EEPROM REG 17	BOOST_EN_ SPREAD_ SPECTRUM	BOOST_SEL_IND[1:0]		BOOST_SEL_IRAMP[1:0]		BOOST_FREQ_SEL[2:0]		
0x72	EEPROM REG 18	BOOST_DRIVER_SIZE[1:0]		EN_ADAP	EN_JUMP	BRIGHTNESS_JUMP_THRES[1:0]		JUMP_STEP_SIZE[1:0]	
0x73	EEPROM REG 19	RESERVED		BOOST_INITIAL_VOLTAGE[5:0]					
0x74	EEPROM REG 20	BOOST_SEL_LLC[1:0]		BOOST_SEL_JITTER_FILTER[1:0]		BOOST_SEL_I[1:0]		BOOST_SEL_P[1:0]	
0x75	EEPROM REG 21	BOOST_OFFTIME_SEL[1:0]		BOOST_BLANKTIME_SEL[1:0]		RESERVED	BOOST_VO_SLOPE_CTRL[2:0]		
0x76	EEPROM REG 22	VDD_UVLO_LEVEL	RESERVED			CP_2X_CLK[1:0]		CP_2X_EN	SQW_PULSE_ GEN_EN
0x77	EEPROM REG 23	EXT_TEMP_LEVEL_HIGH[3:0]				EXT_TEMP_LEVEL_LOW[3:0]			
0x78	EEPROM REG 24	INT_TEMP_LIM[1:0]		EXT_TEMP_PERIOD[4:0]					EXT_TEMP_ COMP_EN

(1) Unused bits data must not be changed.

6.6.1 Register Bit Explanations

6.6.1.1 Display/Cluster1 Brightness Control MSB

Address 0x00

Reset value 0000 0000b

DISP_CL1_BRT MSB							
7	6	5	4	3	2	1	0
DISP_CL1_BRT[15:8]							

Name	Bit	Access	Description
DISP_CL1_BRT[15:8]	7:0	R/W	Backlight brightness control MSB

6.6.1.2 Display/Cluster1 Brightness Control LSB

Address 0x01

Reset value 0000 0000b

DISP_CL1_BRT LSB							
7	6	5	4	3	2	1	0
DISP_CL1_BRT[7:0]							

Name	Bit	Access	Description
DISP_CL1_BRT LSB	7:0	R/W	Backlight brightness control LSB

The DISP_CL1_BRT MSB register must be written first. New value is valid after writing DISP_CL1_BRT LSB. If output 1 is used in display mode, the Brightness/Cluster Output 1 Brightness Control register is used for all outputs in display mode (16-bits register). Otherwise it is the Brightness Control register for cluster output 1. For cluster bit control is 13 bit, most significant bit are used.

6.6.1.3 Display/Cluster1 Output Current MSB

Address 0x02

Reset value loaded during start-up from EEPROM REG0

DISP_CL1_CURRENT MSB							
7	6	5	4	3	2	1	0
RESERVED				DISP_CL1_CURRENT[11:8]			

Name	Bit	Access	Description
DISP_CL1_CURRENT[11:8]	3:0	R/W	Display/Cluster current control MSB

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6.6.1.4 Display/Cluster1 Output Current LSB

Address 0x03

Reset value loaded during start-up from EEPROM REG1

DISP_CL1_CURRENT LSB							
7	6	5	4	3	2	1	0
DISP_CL1_CURRENT[7:0]							

Name	Bit	Access	Description
DISP_CL1_CURRENT[7:0]	7:0	R/W	Display/Cluster current control LSB

The DISP_CL1_CURRENT MSB register must be written first. New value is valid after writing DISP_CL1_CURRENT LSB. If one of few outputs is used in display mode, the DISP_CL1_CURRENT register is used for all outputs in display mode (12-bit), otherwise it is Cluster1 Output Current register.

Maximum current is defined by DRV_LED_CURRENT_SCALE[2:0] bits.

6.6.1.5 Cluster2 Brightness Control MSB

Address 0x04

Reset value 0000 0000b

CL2_BRT MSB							
7	6	5	4	3	2	1	0
RESERVED			CL2_BRT[12:8]				

Name	Bit	Access	Description
CL2_BRT[12:8]	4:0	R/W	Cluster output 2 brightness control MSB

6.6.1.6 Cluster2 Brightness Control LSB

Address 0x05

Reset value 0000 0000b

CL2_BRT LSB							
7	6	5	4	3	2	1	0
CL2_BRT[7:0]							

Name	Bit	Access	Description
CL2_BRT[7:0]	7:0	R/W	Cluster output 2 brightness control LSB

The CL2_BRT MSB register must be written first. New value is valid after writing CL2_BRT LSB.

6.6.1.7 Cluster2 Output Current

Address 0x06

Reset value 0000 0000b

CL2_CURRENT							
7	6	5	4	3	2	1	0
CL2_CURRENT[7:0]							

Name	Bit	Access	Description
CL2_CURRENT[7:0]	7:0	R/W	Cluster output 2 current control

Maximum current is defined by DRV_LED_CURRENT_SCALE[2:0] bits.

6.6.1.8 Cluster3 Brightness Control MSB

Address 0x07

Reset value 0000 0000b

CL3_BRT MSB							
7	6	5	4	3	2	1	0
RESERVED			CL3_BRT[12:8]				

Name	Bit	Access	Description
CL3_BRT[12:8]	4:0	R/W	Cluster output 3 brightness control MSB

6.6.1.9 Cluster3 Brightness Control LSB

Address 0x08

Reset value 0000 0000b

CL3_BRT LSB							
7	6	5	4	3	2	1	0
CL3_BRT[7:0]							

Name	Bit	Access	Description
CL3_BRT[7:0]	7:0	R/W	Cluster output 3 brightness control LSB

The CL3_BRT MSB register must be written first. New value is valid after writing CL3_BRT LSB.

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6.6.1.10 Cluster3 Output Current

Address 0x09

Reset value 0000 0000b

CL3_CURRENT							
7	6	5	4	3	2	1	0
CL3_CURRENT[7:0]							

Name	Bit	Access	Description
CL3_CURRENT[7:0]	7:0	R/W	Cluster output 3 current control

Maximum current is defined by DRV_LED_CURRENT_SCALE[2:0] bits.

6.6.1.11 Cluster4 Brightness Control MSB

Address 0x0A

Reset value 0000 0000b

CL4_BRT MSB							
7	6	5	4	3	2	1	0
RESERVED			CL4_BRT[12:8]				

Name	Bit	Access	Description
CL4_BRT[12:8]	4:0	R/W	Cluster output 4 brightness control MSB

6.6.1.12 Cluster4 Brightness Control LSB

Address 0x0B

Reset value 0000 0000b

CL4_BRT LSB							
7	6	5	4	3	2	1	0
CL4_BRT[7:0]							

Name	Bit	Access	Description
CL4_BRT[7:0]	7:0	R/W	Cluster output 4 brightness control LSB

The CL4_BRT MSB register must be written first. New value is valid after writing CL4_BRT LSB.

6.6.1.13 Cluster4 Output Current

Address 0x0C

Reset value 0000 0000b

CL4_CURRENT							
7	6	5	4	3	2	1	0
CL4_CURRENT[7:0]							

Name	Bit	Access	Description
CL4_CURRENT[7:0]	7:0	R/W	Cluster output 4 current control

Maximum current is defined by DRV_LED_CURRENT_SCALE[2:0] bits.

6.6.1.14 Configuration

Address 0x0D

Reset value loaded during start-up from EEPROM

CONFIGURATION							
7	6	5	4	3	2	1	0
RESERVED	DRV_LED_CURRENT_SCALE[2:0]			EN_ADVANCED _SLOPE	PWM_SLOPE[2:0]		

Name	Bit	Access	Description
DRV_LED_CURRENT_SCALE[2:0]	6:4	R/W	Scales the maximum LED current when EN_EXT_LED_CUR_CTRL = 0 Effective for display and cluster mode. 000 = 25 mA 001 = 30 mA 010 = 50 mA 011 = 60 mA 100 = 80 mA 101 = 100 mA 110 = 120 mA 111 = 150 mA
EN_ADVANCED_SLOPE	3	R/W	Enable for advanced slope (smooth brightness change) 0 = Linear slope used only 1 = Advanced slope used
PWM_SLOPE[2:0]	2:0	R/W	Linear brightness sloping time (typical) 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 52 ms 100 = 105 ms 101 = 210 ms 110 = 315 ms 111 = 511 ms

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6.6.1.15 Status

Address 0x0E

Reset value 0000 0000b

STATUS							
7	6	5	4	3	2	1	0
RESERVED				BRT_SLOPE_DONE	TEMP_RES_MISSING	EXT_TEMP_FLAG_L	EXT_TEMP_FLAG_H

Name	Bit	Access	Description
BRT_SLOPE_DONE	3	R	Status bit for the brightness sloping 0 = Sloping ongoing 1 = Sloping done
TEMP_RES_MISSING	2	R	NTC sensor missing flag 0 = sensor OK 1 = NTC sensor missing
EXT_TEMP_FLAG_L	1	R	External temperature sensor low limit exceeded flag 0 = limit not detected 1 = low temperature limit detected
EXT_TEMP_FLAG_H	0	R	External temperature sensor high limit exceeded flaf 0 = limit not detected 1 = high temperature limit detected

6.6.1.16 Fault

Address 0x0F

Reset value 0000 0000b

STATUS							
7	6	5	4	3	2	1	0
RESERVED	VIN_OVP	VIN_UVLO	TSD	BOOST_OCP	BOOST_OVP	PL_FET_FAULT	CP_2X_FAULT

Name	Bit	Access	Description
VIN_OVP	6	R	VIN overvoltage protection flag 0 = No fault 1 = Fault detected
VIN_UVLO	5	R	VIN undervoltage lockout flag 0 = No fault 1 = Fault detected
TSD	4	R	Thermal shutdown 0 = No flag 1 = Fault detected
BOOST_OCP	3	R	Boost overcurrent protection flag 0 = No flag 1 = Fault detected
BOOST_OVP	2	R	Boost output overvoltage protection flag 0 = No flag 1 = Fault detected
PL_FET_FAULT	1	R	VIN overcurrent protection flag 0 = No fault 1 = Fault detected
CP_2X_FAULT	0	R	Charge pump output voltage too low 0 = No fault 1 = Fault detected

6.6.1.17 LED Fault

Address 0x10

Reset value 0000 0000b

LED FAULT							
7	6	5	4	3	2	1	0
RESERVED		OPEN_LED	SHORT_LED	LED_FAULT[4:1]			

Name	Bit	Access	Description
OPEN_LED	5	R	Open LED fault. 0 = No fault 1 = Fault detected
SHORT_LED	4	R	Short LED fault. 0 = No fault 1 = Fault detected
LED_FAULT[4:1]	3:0	R	Defines which string has either open or short fault. 0001 = LED OUT1 0010 = LED OUT2 0100 = LED OUT3 1000 = LED OUT4

6.6.1.18 Fault Clear

Address 0x11

Reset value 0000 0000b

FAULT CLEAR							
7	6	5	4	3	2	1	0
RESERVED							CLEAR_FAULTS

Name	Bit	Access	Description
CLEAR_FAULTS	0	W	Write only bit, writing CLEAR_FAULTS high clears faults.

6.6.1.19 Identification

Address 0x12

ID							
7	6	5	4	3	2	1	0
FULL_LAYER_REVISION[3:0]				METAL REVISIONS[3:0]			

Name	Bit	Access	Description
FULL_LAYER_REVISION	7:4	R	Manufacturer ID code – full layer revision
METAL REVISIONS	3:0	R	Manufacturer ID code – metal mask revision

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6.6.1.20 Temp MSB

Address 0x13

TEMP MSB							
7	6	5	4	3	2	1	0
RESERVED					TEMP[10:8]		

Name	Bit	Access	Description
TEMP[10:8]	2:0	R	Device internal temperature sensor reading, first 3 MSB. MSB must be read before LSB, because reading of MSB register latches the data.

6.6.1.21 Temp LSB

Address 0x14

TEMP LSB							
7	6	5	4	3	2	1	0
TEMP[7:0]							

Name	Bit	Access	Description
TEMP[7:0]	7:0	R	Device internal temperature sensor reading, last 8 LSB. MSB must be read before LSB, because reading of MSB register latches the data.

6.6.1.22 Display LED Current MSB

Address 0x15

DISP LED CURRENT MSB							
7	6	5	4	3	2	1	0
RESERVED				LED_CURRENT[11:8]			

Name	Bit	Access	Description
LED_CURRENT[11:8]	3:0	R	Display LED current value reading, first 3 MSB. DISP LED CURRENT MSB must be read before DISP LED CURRENT LSB, DISP LED PWM MSB, and DISP LED PWM LSB because reading of the MSB register latches the data for current and PWM.

6.6.1.23 Display LED Current LSB

Address 0x16

DISP LED CURRENT LSB							
7	6	5	4	3	2	1	0
LED_CURRENT[7:0]							

Name	Bit	Access	Description
LED_CURRENT[7:0]	7:0	R	Display LED current value reading, last 8 LSB. Note: DISP LED CURRENT MSB latches the data for current and PWM.

6.6.1.24 Display LED PWM MSB

Address 0x17

Reset value 0000 0000b

DISP LED PWM MSB							
7	6	5	4	3	2	1	0
PWM[15:8]							

Name	Bit	Access	Description
PWM[7:0]	7:0	R	Display LED current value reading, first 8 MSB. Note: DISP LED CURRENT MSB latches the data for current and PWM.

6.6.1.25 Display LED PWM LSB

Address 0x18

Reset value 0000 0000b

DISP LED PWM LSB							
7	6	5	4	3	2	1	0
PWM[7:0]							

Name	Bit	Access	Description
PWM[7:0]	7:0	R	Display LED PWM reading, last 8 LSB. Note: DISP LED CURRENT MSB latches the data for current and PWM.

6.6.1.26 EEPROM Control

Address 0x19

Reset value 1000 0000b

EEPROM CTRL							
7	6	5	4	3	2	1	0
EE_READY	RESERVED					EE_PROG	EE_READ

Name	Bit	Access	Description
EE_READY	7	R	EEPROM ready 0 = EEPROM programming or read in progress 1 = EEPROM ready, not busy
EE_PROG	1	R/W	EEPROM programming 0 = Normal operation 1 = Start the EEPROM programming sequence. Programs data currently in the EEPROM registers to non-volatile memory (NVM).
EE_READ	0	R/W	EEPROM read 0 = Normal operation 1 = Reads the data from NVM to the EEPROM registers. Can be used to restore default values if EEPROM registers are changed during testing.

Programming sequence (program data permanently from registers to NVM):

1. Turn on the chip by setting VDDIO/EN pin high.
2. Unlock EEPROM by writing the unlock codes to register 0x1A.
   - Write 0x08 to address 0x1A
   - Write 0xBA to address 0x1A
   - Write 0xEF to address 0x1A
3. Write data to EEPROM registers (address 0x60…0x78).

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4. Write EE_PROG to high in address 0x19. (0x02 to address 0x19).
5. Wait 200 ms.
6. Write EE_PROG to low in address 0x19. (0x00 to address 0x19).

Read sequence (load data from NVM to registers):

1. Turn on the chip by writing setting VDDIO/EN pin high.
2. Unlock EEPROM by writing the unlock codes to register 0x1A.
   - Write 0x08 to address 0x1A
   - Write 0xBA to address 0x1A
   - Write 0xEF to address 0x1A
3. Write EE_READ to high in address 0x19. (0x01 to address 0x19).
4. Wait 1 ms.
5. Write EE_READ to low in address 0x19. (0x00 to address 0x19).

注

EEPROM bits are intended to be set/programmed before normal operation only once during silicon production, but can be reprogrammed for evaluation purposes up to 1000 cycles.

6.6.1.27 EEPROM Unlock Code

Address 0x1A

Reset value 0000 0000b

EEPROM UNLOCK							
7	6	5	4	3	2	1	0
EEPROM UNLOCK_CODE[7:0]							

Name	Bit	Access	Description
EEPROM_UNLOCK_CODE[7:0]	7:0	W	Unlock EEPROM control register (0x19) and EEPROM registers. Writing 0x08, 0xBA, 0xEF sequence unlocks EEPROM registers. Lock is enabled again by writing any other code to the register.

6.6.2 EEPROM Bit Explanations

6.6.2.1 EEPROM Register 0

Address 0x60

EEPROM REGISTER 0							
7	6	5	4	3	2	1	0
EXT_TEMP_MINUS[1:0]		DRV_LED_BIAS_CTRL[1:0]		LED_CURRENT_CTRL[11:8]			

Name	Bit	Access	Description
EXT_TEMP_MINUS[1:0]	7:6	R/W	External temperature sensor current dimming knee point, see *セクション 6.3.9.2* for details. 00 = 1 µA 01 = 5 µA 10 = 9 µA 11 = 13 µA
DRV_LED_BIAS_CTRL[1:0]	5:4	R/W	Controls the LED current sink bias current. Effects LED current sink rise time and current consumption. 150-mA LED current is suggested. 00 = slowest LED current sink setting and low Iq (typical 800-ns rise time / 200 µA per sink) 01 = slow (typical 400-ns rise time / 400 µA per sink) 10 = fast (typical 200-ns rise time / 800 µA per sink) 11 = fastest LED current sink and higher current consumption (typical100-ns rise time / 1.6 mA per sink)
LED_CURRENT_CTRL[11:8]	3:0	R/W	MSB bits for 12-bit LED current control. Step size is 150 mA / 4095 = 36.63 µA (typical) when max current is set to 150 mA. Max current can be scaled with R_{ISET} resistor or with DRV_LED_CURRENT_SCALE EEPROM bits. 000h = 0 mA 001h = 0.037 mA 002h = 0.073 mA 003h = 0.110 mA … FFEh = 149.963 mA FFFh = 150.000 mA

6.6.2.2 EEPROM Register 1

Address 0x61

EEPROM REGISTER 1							
7	6	5	4	3	2	1	0
LED_CURRENT_CTRL[7:0]							

Name	Bit	Access	Description
LED_CURRENT_CTRL[7:0]	7:0	R/W	LSB bits for 12-bit LED current control. Step size is 150 mA / 4095 = 36.63 µA when max current is set to 150 mA. Max current can be scaled with R_{ISET} resistor or with DRV_LED_CURRENT_SCALE EEPROM bits. 000h = 0 mA 001h = 0.037 mA 002h = 0.073 mA 003h = 0.110 mA … FFEh = 149.963 mA FFFh = 150.000 mA

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6.6.2.3 EEPROM Register 2

Address 0x62

EEPROM REGISTER 2							
7	6	5	4	3	2	1	0
RESERVED	EN_STEADY_DITHER	PWM_INPUT_HYSTERESIS[1:0]		EN_ADVANCED_SLOPE	PWM_SLOPE[2:0]		

Name	Bit	Access	Description
EN_STEADY_DITHER	6	R/W	Enable dithering in steady state condition 0 = Disabled, dithering used in sloping (brightness changes) only 1 = Enabled, dithering used in sloping as well as steady-state condition. Dithering defined with DITHER[2:0] bits.
PWM_INPUT_HYSTERESIS[1:0]	5:4	R/W	PWM input hysteresis function. Defines how small changes in the PWM input are ignored. Hysteresis used to remove constant switching between two values. 00 = ±1-step hysteresis with 16-bit resolution 01 = ±8-step hysteresis with 16-bit resolution 10 = ±16-step hysteresis with 16-bit resolution 11 = ±256-step hysteresis with 16-bit resolution
EN_ADVANCED_SLOPE	3	R/W	Advanced smooth slope for brightness changes 0 = Advanced slope is disabled 1 = Use advanced slope for brightness change to make brightness changes smooth for eye
PWM_SLOPE[2:0]	2:0	R/W	Linear brightness sloping time (typical) 000 = Slope function disabled, immediate brightness change 001 = 1 ms 010 = 2 ms 011 = 52 ms 100 = 105 ms 101 = 210 ms 110 = 315 ms 111 = 511 ms

6.6.2.4 EEPROM Register 3

Address 0x63

EEPROM REGISTER 3							
7	6	5	4	3	2	1	0
EN_DISPLAY_LED_FAULT	DRV_LED_CURRENT_SCALE[2:0]			LED_STRING_CONF[2:0]			EN_PWM_I

Name	Bit	Access	Description
EN_DISPLAY_LED_FAULT	7	R/W	0 = LED open/short faults disabled 1 = LED open/short faults enabled
DRV_LED_CURRENT_SCALE[2:0]	6:4	R/W	Scales the maximum LED current when EN_EXT_LED_CUR_CTRL = 0 Effective for both modes – display and cluster. 000 = 25 mA 001 = 30 mA 010 = 50 mA 011 = 60 mA 100 = 80 mA 101 = 100 mA 110 = 120 mA 111 = 150 mA
LED_STRING_CONF[2:0]	3:1	R/W	LED current sink configuration 000 = 4 separate LED strings with 90° phase shift 001 = 3 separate LED strings with 120° phase shift (String 4 in cluster mode or not used) 010 = 2 separate LED strings with 180° phase shift (Strings 3 and 4 in cluster mode or not used) 011 = 1 LED string. (Strings 2,3 and 4 in cluster mode or not used) 100 = 2 LED strings (1+2, 3+4) with 180° phase shift. Tied strings with same phase. 101 = 1 LED string (1+2+3+4). Tied strings with same phase 110 = 1 LED string (1+2). 1st and 2nd strings tied with same phase, strings 3 and 4 are in cluster mode or not used 111 = All strings are used in cluster mode
EN_PWM_I	0	R/W	Enable Hybrid PWM and Current dimming mode 0 = Disabled, dimming only with PWM 1 = Enabled

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6.6.2.5 EEPROM Register 4

Address 0x64

EEPROM REGISTER 4							
7	6	5	4	3	2	1	0
EN_CL_LED_FAULT	DRV_LED_COMP_HYST[1:0]		DRV_LED_FAULT_THR[1:0]		DRV_HEADER[2:0]		

Name	Bit	Access	Description
EN_CL_LED_FAULT	7	R/W	Enable open/short LED fault for cluster strings 0 = LED fault in cluster mode disabled 1 = LED fault in cluster mode enabled
DRV_LED_COMP_HYST[1:0]	6:5	R/W	LED comparator hysteresis – difference between mid and low comparator, used for boost adaptive voltage control (boost high level) 00 = 1000 mV 01 = 750 mV 10 = 500 mV 11 = 250 mV
DRV_LED_FAULT_THR[1:0]	4:3	R/W	LED Fault thresholds, used for short LED detection. 00 = 3.6 V 01 = 3.6 V 10 = 6.9 V 11 = 10.6 V
DRV_HEADER[2:0]	2:0	R/W	LED current sink headroom control, used for boost adaptive voltage control (boost low level) and open LED detection. V_{SAT} is the saturation voltage of the sink, typically 500 mV with 150-mA current. 111 = V_{SAT} + 50 mV 110 = V_{SAT} + 175 mV 101 = V_{SAT} + 300 mV 100 = V_{SAT} + 450 mV 011 = V_{SAT} + 575 mV 010 = V_{SAT} + 700 mV 001 = V_{SAT} + 875 mV 000 = V_{SAT} + 1000 mV

6.6.2.6 EEPROM Register 5

Address 0x65

EEPROM REGISTER 5							
7	6	5	4	3	2	1	0
I_SLOPE[2:0]			PWM_RESOLUTION[1:0]		DITHER[2:0]		

Name	Bit	Access	Description
I_SLOPE[2:0]	7:5	R/W	Slope gain adjusts the current slope for Hybrid PWM and Current dimming mode 000 = 1.000 001 = 1.023 010 = 1.047 011 = 1.070 100 = 1.094 101 = 1.117 110 = 1.141 111 = 1.164
PWM_RESOLUTION[1:0]	4:3	R/W	For PWM clocking with internal oscillator (VSYNC is not used) these bits control the PLL multiplier and hence the PWM output resolution 00 = 5-MHz clock used for generating PWM 01 = 10-MHz clock used for generating PWM 10 = 20-MHz clock used for generating PWM 11 = 40-MHz clock used for generating PWM
DITHER[2:0]	2:0	R/W	Dither function controls 000 = Dither function disabled 001 = 1-bit dither 010 = 2-bit dither 011 = 3-bit dither 1XX = 4-bit dither

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6.6.2.7 EEPROM Register 6

Address 0x66

EEPROM Register 6							
7	6	5	4	3	2	1	0
RESERVED	GAIN_CTRL[2:0]			EN_EXT_LED_CUR_CTRL	DRV_EN_SPLIT_FET	BRT_MODE[1:0]	

Name	Bit	Access	Description
GAIN_CTRL[2:0]	6:4	R/W	Switch point from PWM to current control for Hybrid PWM and Current dimming mode 000 = 50.0% 001 = 40.6% 010 = 31.3% 011 = 25.0% 100 = 21.9% 101 = 18.8% 110 = 15.6% 111 = 12.5%
EN_EXT_LED_CUR_CTRL	3	R/W	Enable LED current set resistor 0 = Resistor is disabled and current is scaled with SCALE[2:0] EEPROM register bits 1 = Enable LED current set resistor. LED current is scaled by the R_{ISET} resistor
DRV_EN_SPLIT_FET	2	R/W	LED current sink FET control 0 = big size FET is driving LED current 1 = enable use of smaller FET for driving low LED output currents. Smaller FET is selected automatically when current setting is below 1/16 of the scale. Automatic scaling improves accuracy for output currents below 1/16 of the full current scale.
BRT_MODE[1:0]	1:0	R/W	Brightness control mode 00 = PWM input pin duty cycle control 01 = PWM input duty x Brightness register 10 = Brightness register 11 = Direct PWM control from PWM input pin

6.6.2.8 EEPROM Register 7

Address 0x67

EEPROM Register 7							
7	6	5	4	3	2	1	0
DRV_OUT2_CORR[3:0]				DRV_OUT1_CORR[3:0]			

Name	Bit	Access	Description
DRV_OUT2_CORR[3:0]	7:4	R/W	Current correction for OUT2 LED current sink 0000 = 6.5% 0001 = 5.6% 0010 = 4.7% 0011 = 3.7% 0100 = 2.8% 0101 = 1.9% 0110 = 0.9% 0111 = 0.0% 1000 = –0.9% 1001 = –1.9% 1010 = –2.8% 1011 = –3.7% 1100 = –4.7% 1101 = –5.6% 1110 = –6.5% 1111 = –7.4%

Name	Bit	Access	Description
DRV_OUT1_CORR[3:0]	3:0	R/W	Current correction for OUT1 LED current sink 0000 = 6.5% 0001 = 5.6% 0010 = 4.7% 0011 = 3.7% 0100 = 2.8% 0101 = 1.9% 0110 = 0.9% 0111 = 0.0% 1000 = –0.9% 1001 = –1.9% 1010 = –2.8% 1011 = –3.7% 1100 = –4.7% 1101 = –5.6% 1110 = –6.5% 1111 = –7.4%

6.6.2.9 EEPROM Register 8

Address 0x68

EEPROM Register 8							
7	6	5	4	3	2	1	0
DRV_OUT4_CORR[3:0]				DRV_OUT3_CORR[3:0]			

Name	Bit	Access	Description
DRV_OUT4_CORR[3:0]	7:4	R/W	Current correction for OUT4 LED current sink 0000 = 6.5% 0001 = 5.6% 0010 = 4.7% 0011 = 3.7% 0100 = 2.8% 0101 = 1.9% 0110 = 0.9% 0111 = 0.0% 1000 = –0.9% 1001 = –1.9% 1010 = –2.8% 1011 = –3.7% 1100 = –4.7% 1101 = –5.6% 1110 = –6.5% 1111 = –7.4%
DRV_OUT3_CORR[3:0]	3:0	R/W	Current correction for OUT3 LED current sink 0000 = 6.5% 0001 = 5.6% 0010 = 4.7% 0011 = 3.7% 0100 = 2.8% 0101 = 1.9% 0110 = 0.9% 0111 = 0.0% 1000 = –0.9% 1001 = –1.9% 1010 = –2.8% 1011 = –3.7% 1100 = –4.7% 1101 = –5.6% 1110 = –6.5% 1111 = –7.4%

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6.6.2.10 EEPROM Register 9

Address 0x69

EEPROM Register 8							
7	6	5	4	3	2	1	0
EXT_TEMP_GAIN[3:0]				BL_COMP_FILTER_SEL[3:0]			

Name	Bit	Access	Description
EXT_TEMP_GAIN[3:0]	7:4	R/W	External temperature sensor current dimming gain control, see *セクション 6.3.9.2* for details.
BL_COMP_FILTER_SEL[3:0]	3:0	R/W	Filter selects how many PWM generator clock cycles high/mid comparator is filtered before it is used to detect shorted LEDs and boost voltage down scaling. 0000 = 5 0001 = 10 0010 = 20 0011 = 40 0100 = 60 0101 = 80 0110 = 100 0111 = 140 1000 = 180 1001 = 220 1010 = 260 1011 = 300 1100 = 340 1101 = 380 1110 = 420 1111 = 460

6.6.2.11 EEPROM Register 10

Address 0x6A

EEPROM Register 9							
7	6	5	4	3	2	1	0
EXT_TEMP_I_DIMMING_EN	NMOS_PLFET_EN	SOFT_START_SEL[1:0]		PL_SD_LEVEL[1:0]		PL_SD_SINK_LEVEL[1:0]	

Name	Bit	Access	Description
EXT_TEMP_I_DIMMING_EN	7	R/W	External temperature sensor current dimming enabled 0 = disabled 1 = enabled
NMOS_PLFET_EN	6	R/W	Powerline FET selection: 0 = pFET 1 = nFET
SOFT_START_SEL[1:0]	5:4	R/W	Soft-start time selection 00 = 5 ms 01 = 10 ms 10 = 20 ms 11 = 50 ms
PL_SD_LEVEL[1:0]	3:2	R/W	Power-line FET current limit selection VIN OCP (assumed R_{ISENSE} = 20 mΩ). 10 = 6 A 11 = 8 A
PL_SD_SINK_LEVEL[1:0]	1:0	R/W	Power-line FET gate current

	NMOS_PLFET_EN = 0 (current for normal mode)	NMOS_PLFET_EN = 1 (current for fault recovery mode, otherwise 0mA)
00	55 µA	0.3 mA
01	110 µA	0.5 mA
10	220 µA	1.0 mA
11	440 µA	2.2 mA

6.6.2.12 EEPROM Register 11

Address 0x6B

EEPROM Register 11							
7	6	5	4	3	2	1	0
SLOW_PLL_DIV[12:5]							

Name	Bit	Access	Description
SLOW_PLL_DIV[12:5]	7:0	R/W	Divider for VSYNC operation. 8 MSB bits

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6.6.2.13 EEPROM Register 12

Address 0x6C

EEPROM Register 12							
7	6	5	4	3	2	1	0
EN_SYNC	PWM_SYNC	PWM_COUNTER_RESET	SLOW_PLL_DIV[4:0]				

Name	Bit	Access	Description
EN_SYNC	7	R/W	VSYNC input enable 0 = VSYNC input disabled 1 = VSYNC input enabled
PWM_SYNC	6	R/W	Enable PWM generation synchronization to VSYNC signal 0 = Disabled 1 = Enabled. PWM output used for phase detector input after dividing with SLOW_PLL_DIV divider
PWM_COUNTER_RESET	5	R/W	Enable PWM generator resetting on VSYNC signal rising edge 0 = Disabled 1 = Enabled
SLOW_PLL_DIV[4:0]	4:0	R/W	Divider for VSYNC operation. 5 LSB bits

6.6.2.14 EEPROM Register 13

Address 0x6D

EEPROM Register 13							
7	6	5	4	3	2	1	0
R_SEL[1:0]		SEL_DIVIDER	EN_PLL	SYNC_PRE_DIVIDER[3:0]			

Name	Bit	Access	Description
R_SEL[1:0]	7:6	R/W	Coefficient for the slow PLL divider 00 = 16 01 = 32 10 = 64 11 = 128
SEL_DIVIDER	5	R/W	PLL divider selection 0 = Slow PLL divider with external compensation (when using VSYNC) 1 = Fast PLL divider with internal compensation (when using 5-MHz internal clock)
EN_PLL	4	R/W	PLL enable 0 = PLL disabled and internal 5-MHz oscillator used for PWM generation 1 = PLL is used for generating the PWM generation clock from the internal oscillator or VSYNC signal
SYNC_PRE_DIVIDER[3:0]	3:0	R/W	VSYNC signal pre-divider from 1 to 16. Used when VSYNC frequency is higher than PWM output frequency.

6.6.2.15 EEPROM Register 14

Address 0x6E

EEPROM Register 14							
7	6	5	4	3	2	1	0
RESERVED			SYNC_TYPE	PWM_FREQ[3:0]			

Name	Bit	Access	Description
SYNC_TYPE	4	R/W	Type of the VSYNC input. Affects the PLL functionality. 0 = HSYNC (50 to 150 kHz) 1 = VSYNC (50 to 150 Hz)
PWM_FREQ[3:0]	3:0	R/W	PWM output frequency setting when internal oscillator is used. See *セクション 6.3.2*

6.6.2.16 EEPROM Register 15

Address 0x6F

EEPROM Register 13							
7	6	5	4	3	2	1	0
MASK_BOOST_OVP_STATUS	MASK_BOOST_OCP_FSM	MASK_OVP_FSM	MASK_VIN_UVLO	UVLO_LEVEL[1:0]		OVP_LEVEL[1:0]	

Name	Bit	Access	Description
MASK_BOOST_OVP_STATUS	7	R/W	Boost overvoltage protection enable 0 = Enabled 1 = Fault bit and FAULT pin disabled.
MASK_BOOST_OCP_FSM	6	R/W	Boost overcurrent protection fault recovery state enable 0 = Enabled 1 = Entering fault recovery state disabled. Fault bit and FAULT pin operate normally.
MASK_OVP_FSM	5	R/W	VIN overvoltage fault recovery state enable 0 = Enabled 1 = Entering fault recovery state disabled. Fault bit and FAULT pin operate normally.
MASK_VIN_UVLO	4	R/W	VIN undervoltage lockout fault recovery state enable 0 = Enabled 1 = Entering fault recovery state disabled. Fault bit and FAULT pin operate normally.
UVLO_LEVEL[1:0]	3:2	R/W	VIN Undervoltage protection thresholds (UVLO) 00 = disabled 01 = 3 V 10 = 5 V 11 = 8 V
OVP_LEVEL[1:0]	1:0	R/W	VIN Overvoltage protection thresholds (OVP) 00 = disabled 01 = 7 V 10 = 11 V 11 = 22.5 V

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6.6.2.17 EEPROM Register 16

Address 0x70

EEPROM Register 16							
7	6	5	4	3	2	1	0
RESERVED		BOOST_EN_IRAMP_DELAY	BOOST_EXT_CLK_SEL	BOOST_IMAX_SEL[2:0]			BOOST_GD_VOLT

Name	Bit	Access	Description
BOOST_EN_IRAMP_DELAY	5	R/W	Boost current ramp delay enable (for adjusting conversion ratio/ stability, 35% of period) 1 = Delay enabled 0 = Delay disabled
BOOST_EXT_CLK_SEL	4	R/W	Boost clock selection 0 = Internal clock 1 = External clock (SYNC pin) If external clock selected and sync disappears for 1.5…2 periods, boost automatically switches to using internal oscillator with frequency defined by BOOST_FREQ_SEL[2:0]
BOOST_IMAX_SEL[2:0]	3:1	R/W	Maximum current limit for boost SW mode. Values below based on 25-mΩ sense resistor value. 000 = 2 A 001 = 3 A 010 = 4 A 011 = 5 A 100 = 6 A 101 = 7 A 110 = 8 A 111 = 9 A
BOOST_GD_VOLT	0	R/W	Boost gate driver voltage selection 1 = Charge pump output ($V_{GATE\ DRIVER}$ > 6 V) 0 = VDD

6.6.2.18 EEPROM Register 17

Address 0x71

EEPROM Register 17							
7	6	5	4	3	2	1	0
BOOST_EN_SPREAD_SPECTRUM	BOOST_SEL_IND[1:0]		BOOST_SEL_IRAMP[1:0]		BOOST_FREQ_SEL[2:0]		

Name	Bit	Access	Description
BOOST_EN_SPREAD_SPECTRUM	7	R/W	Boost spread spectrum (±3% from central frequency, 1.875 kHz modulation frequency) enable 0 = Spread spectrum disabled 1 = Spread spectrum enabled
BOOST_SEL_IND[1:0]	6:5	R/W	See BOOST_SEL_IRAMP for selecting BOOST_SEL_IND setting
BOOST_SEL_IRAMP[1:0]	4:3	R/W	Boost artificial current ramp peak value, A/s. Select value higher than I_{RAMP_GAIN}: I_{RAMP_GAIN} =1.2 x 0.5 x ($VOUT_{max}$ - VIN_{min})/(0.7 x L x 60000), where VIN, VOUT are boost input and output voltage, L - inductance, H. 25-mΩ R_{SENSE} is suggested.

	BOOST_SEL_IND[1:0]			
BOOST_SEL_IRAMP [1:0]	00	01	10	11
00	130	65	34	29
01	88	43	23	20
10	56	28	15	13
11	37	18	10	8.5

BOOST_FREQ_SEL[2:0]	2:0	R/W	BOOST_EXT_CLK_SEL=0 Boost output frequency selection (internal oscillator) 000= 100 kHz 001 = 200 kHz 010 = 303 kHz 011 = 400 kHz 100 = 629 kHz 101 = 800 kHz 110 = 1100 kHz 111 = 2200 kHz BOOST_EXT_CLK_SEL=1 Boost output frequency selection (for external sync mode if external sync disappears) 000= 100 kHz 001 = 200 kHz 010 = 303 kHz 011 = 400 kHz 100 = 625 kHz 101 = 833 kHz 110 = 1111 kHz 111 = 2500 kHz

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6.6.2.19 EEPROM Register 18

Address 0x72

EEPROM Register 16							
7	6	5	4	3	2	1	0
BOOST_DRIVER_SIZE[1:0]		EN_ADAP	EN_JUMP	BRIGHTNESS_JUMP_THRES[1:0]		JUMP_STEP_SIZE[1:0]	

Name	Bit	Access	Description
BOOST_DRIVER_SIZE[1:0]	7:6	R/W	Boost gate driver scaling. Affects gate driver peak current and SW node voltage rise/fall times 00 = 0.4/0.45 A (typical) peak sink/source current 01 = 0.75/0.87 A (typical) peak sink/source current 10 = 1.2/1.3 A (typical) peak sink/source current 11 = 1.5/1.7 A (typical) peak sink/source current
EN_ADAP	5	R/W	Enable boost converter adaptive mode 0 = adaptive mode disabled, boost converter output voltage is set with BOOST_INITIAL_VOLTAGE EEPROM register bits. 1 = adaptive mode enabled. Boost converter start-up voltage is set with BOOST_INITIAL_VOLTAGE EEPROM register bits. Further boost voltage is adapted to the highest LED string V_F. If all LED outputs are in cluster mode, adaptive mode is disabled automatically.
EN_JUMP	4	R/W	Enable large boost voltage jump command for the fast brightness increase. 0 = Normal steps used for boost voltage control 1 = Jump command allowed in boost voltage control
BRIGHTNESS_JUMP_THRES[1:0]	3:2	R/W	Defines the magnitude of the input brightness change after which jump command is given. 00 = Jump command after 10% brightness change 01 = Jump command after 30% brightness change 10 = Jump command after 50% brightness change 11 = Jump command after 70% brightness change
JUMP_STEP_SIZE[1:0]	1:0	R/W	Boost control step size that jump command increases backlight boost output voltage 00: 8 steps (1.0 V typ) 01: 16 steps (2.0 V typ) 10: 32 steps (4.0 V typ) 11: 64 steps (8.0 V typ)

6.6.2.20 EEPROM Register 19

Address 0x73

EEPROM Register 19							
7	6	5	4	3	2	1	0
RESERVED		BOOST_INITIAL_VOLTAGE[5:0]					

Name	Bit	Access	Description
BOOST_INITIAL_VOLTAGE[5:0]	5:0	R/W	Boost voltage control from 16 V to 47.5 V with 0.5 V step (without FB resistive divider). When resistive divider is used on the FB pin, the voltages are scaled accordingly. If adaptive boost control is enabled, this sets the initial start voltage for the boost converter. If adaptive mode is disabled, this sets the output voltage of the boost converter. 000000 = 16.0 V (typical) 000001 = 16.5 V (typical) 000010 = 17.0 V (typical) 000011 = 17.5 V (typical) 000100 = 18.0 V (typical) ... 111100 = 46.0 V (typical) 111101 = 46.5 V (typical) 111110 = 47.0 V (typical) 111111 = 47.5 V (typical)

6.6.2.21 EEPROM Register 20

Address 0x74

EEPROM Register 20							
7	6	5	4	3	2	1	0
BOOST_SEL_LLC[1:0]		BOOST_SEL_JITTER_FILTER[1:0]		BOOST_SEL_I[1:0]		BOOST_SEL_P[1:0]	

Name	Bit	Access	Description
BOOST_SEL_LLC[1:0]	7:6	R/W	Light load comparator control. Selects boost PFM entry threshold (compensator current) 00 = 5 µA (boost switches from PFM to PWM early at light loads) 01 = 10 µA 10 = 15 µA 11 = 20 µA (boost operates in PFM mode to higher loads)
BOOST_SEL_JITTER_FILTER[1:0]	5:4	R/W	Boost jitter filter selection 00 = bypass 01 = 300 kHz 10 = 60 kHz 11 = 30 kHz
BOOST_SEL_I[1:0]	3:2	R/W	Boost PI compensator control: integral part 00 = 1 01 = 2 10 = 3 11 = 4
BOOST_SEL_P[1:0]	1:0	R/W	Boost PI compensator control: proportional part 00 = 1 01 = 2 10 = 3 11 = 4

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6.6.2.22 EEPROM Register 21

Address 0x75

EEPROM Register 21							
7	6	5	4	3	2	1	0
BOOST_OFFTIME_SEL[1:0]		BOOST_BLANKTIME_SEL[1:0]		RESERVED	BOOST_VO_SLOPE_CTRL[2:0]		

Name	Bit	Access	Description
BOOST_OFFTIME_SEL[1:0]	7:6	R/W	Boost time off selection 00 = 131 ns 01 = 68 ns 10 = 38 ns 11 = 24 ns
BOOST_BLANKTIME_SEL[1:0]	5:4	R/W	Boost blank time selection 00 = 162 ns 01 = 88 ns 10 = 63 ns 11 = 40 ns
BOOST_VO_SLOPE_CTRL[2:0]	2:0	R/W	Sets the speed for boost output voltage scaling up or down 000 = 1 (every PWM cycle) 001 = 2 (every other PWM cycle) 010 = 3 (every third PWM cycle) 011 = 4 (every 4th PWM cycle) 100 = 5 (every 5th PWM cycle) 101 = 6 (every 6th PWM cycle) 110 = 8 (every 8th PWM cycle) 111 = 16 (every 16th PWM cycle)

6.6.2.23 EEPROM Register 22

Address 0x76

EEPROM Register 20							
7	6	5	4	3	2	1	0
VDD_UVLO_LEVEL	RESERVED			CP_2X_CLK[1:0]		CP_2X_EN	SQW_PULSE_GEN_EN

Name	Bit	Access	Description
VDD_UVLO_LEVEL	7	R/W	VDD UVLO protection level 0 = 2.5 V 1 = 3.0 V Voltage hysteresis typically 50 mV. 2.5V level can be used if PLL frequency up to 20 MHz. With higher PLL frequency logic is not specified to work down to 2.5 V VDD
CP_2X_CLK[1:0]	3:2	R/W	Charge pump clock frequency 00 = 104 kHz 01 = 208 kHz 10 = 417 kHz 11 = 833 kHz
CP_2X_EN	1	R/W	Charge pump enable. CP is enabled at soft start if CP_2X_EN EEPROM bit asserted. 0 = disabled 1 = enabled
SQW_PULSE_GEN_EN	0	R/W	External charge pump clock enable (50% duty cycle 100 kHz). Clock connected to SQW pin. SQW clock enabled at soft start. 0 = disabled 1 = enabled

6.6.2.24 EEPROM Register 23

Address 0x77

EEPROM Register 23							
7	6	5	4	3	2	1	0
EXT_TEMP_LEVEL_HIGH[3:0]				EXT_TEMP_LEVEL_LOW[3:0]			

Name	Bit	Access	Description
EXT_TEMP_LEVEL_HIGH[3:0]	7:4	R/W	High external temperature sensor limit, kΩ 0000 = 79.67 0001 = 43.35 0010 = 29.77 0011 = 22.67 0100 = 18.30 0101 = 15.34 0110 = 13.21 0111 = 11.60 1000 = 10.34 1001 = 9.32 1010 = 8.49 1011 = 7.79 1100 = 7.20 1101 = 6.69 1110 = 6.25 1111 = 5.87
EXT_TEMP_LEVEL_LOW[3:0]	3:0	R/W	Low external temperature sensor limit, kΩ 0000 = 79.67 0001 = 43.35 0010 = 29.77 0011 = 22.67 0100 = 18.30 0101 = 15.34 0110 = 13.21 0111 = 11.60 1000 = 10.34 1001 = 9.32 1010 = 8.49 1011 = 7.79 1100 = 7.20 1101 = 6.69 1110 = 6.25 1111 = 5.87

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6.6.2.25 EEPROM Register 24

Address 0x78

EEPROM Register 24							
7	6	5	4	3	2	1	0
INT_TEMP_LIM[1:0]		EXT_TEMP_PERIOD[4:0]					EXT_TEMP_COMP_EN

Name	Bit	Access	Description
INT_TEMP_LIM[1:0]	7:6	R/W	Internal temperature sensor brightness thermal de-rating starting level. Thermal de-rating function temperature threshold: 00 = thermal de-rating function disabled 01 = 90°C 10 = 100°C 11 = 110°C
EXT_TEMP_PERIOD[4:0]	5:1	R/W	Step time for temperature limitation with external sensor 00000 = 2 s 00001 = 4 s 00010 = 6 s 00011 = 8 s 00100 = 10 s 00101 = 12 s 00110 = 14 s 00111 = 16 s 01000 = 18 s 01001 = 20 s 01010 = 22 s 01011 = 24 s 01100 = 26 s 01101 = 28 s 01110 = 30 s 01111 = 32 s … 11110 = 62 s 11111 = 64 s
EXT_TEMP_COMP_EN	0	R/W	External temperature sensor (NTC) enable 0 = disabled 1 = enabled

7 Application and Implementation

注

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7.1 Application Information

The LP8860-Q1 is designed for automotive applications, and an input voltage V_{IN} is intended to be connected to the car battery. The device is internally powered from the VDD pin, and voltage must be in 3-V to 5.5-V range. The device has flexible configurability; outputs configuration are defined by EEPROM settings. If the VDD voltage is not high enough to drive an external nMOSFET gate, an internal charge pump must be used to power the gate driver. The charge pump is configured by EEPROM.

The LP8860-Q1 can be used as a stand-alone device, using only the VDDIO/EN pin and the PWM signal. Alternatively, the device can be a part of system, connected to a microprocessor by an SPI or I^2C interface.

注

Maximum operating voltage for V_{IN} is 48 V; the boost converter can achieve output voltage up to 48 V (typical) without external feedback divider in adaptive voltage control mode. However, V_{IN} must be below output voltage, and the conversion ratio (max 10) must be taken into account. If necessary, boost can provide higher output voltage with an external resistive feedback voltage divider. For high output-voltage applications, outputs must be protected by external components to prevent overvoltage.

7.2 Typical Applications

7.2.1 Typical Application for Display Backlight

図 7-1 shows the typical application for the LP8860-Q1 with factory-programmed settings. It supports 4 LED strings in display mode with a 90° phase shift. Brightness control register is used for LED dimming by using conventional PWM dimming method. VDD voltage is 5 V, charge pump is disabled, and boost switching frequency is 303 kHz.

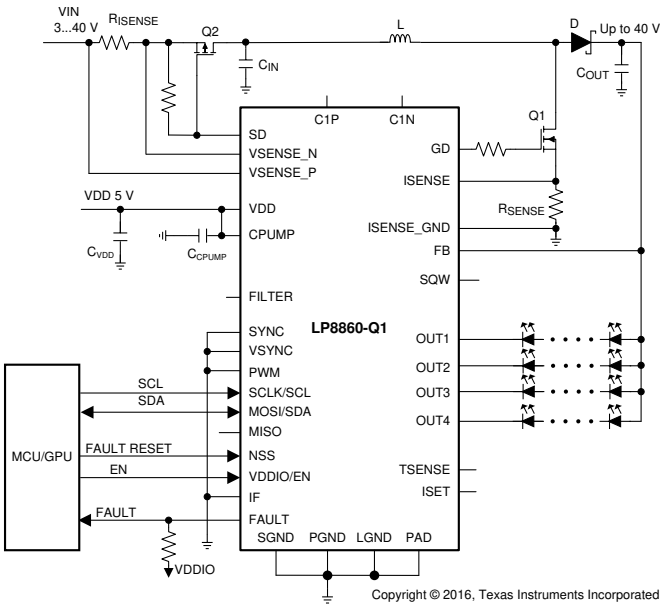

図 7-1. VDD = 5 V, I^2C, 4 LED Outputs in Display Mode

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7.2.1.1 Design Requirements

表 7-1. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	ED
61	DF
62	DC
63	F0
64	DF
65	E5
66	F2
67	77
68	77
69	71
6A	3F
6B	B7
6C	17
6D	EF
6E	B0
6F	87
70	CE
71	72
72	E5
73	DF
74	35
75	06
76	DC
77	FF
78	3E

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 40 V
VDD voltage	5 V
Charge pump	Disabled
Brightness Control	I^2C
Output configuration	Mode 1, OUT1 to OUT4 are in display mode (phase shift 90°)
LED string current	130 mA
External current set resistor	Disabled
Boost frequency	303 kHz
Inductor	22 µH to 33 µH, at least 9-A saturation current
Input/Output capacitors	10 µF ceramic and 33 µF electrolytic
R_{ISENSE}	20 mΩ
R_{SENSE}	25 mΩ
Current dimming with external NTC	Disabled

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferable. The saturation current must be greater than the sum of the maximum load current and the worst case average-to-peak inductor current. The equation below shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D) \tag{9}$$

- I_{RIPPLE}: peak inductor current
- I_{OUTMAX}: maximum load current
- V_{IN}: minimum input voltage in application
- L: min inductor value including worst case tolerances
- f: minimum switching frequency
- V_{OUT}: output voltage
- D: Duty Cycle for CCM Operation
- V_{OUT}: Output Voltage

As a result the inductor must be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum switch current limit defined by <BOOST_IMAX_SEL[2:1]> EEPROM bits. A 22-µH to 33-µH inductor with a saturation current rating of at least 9 A is recommended for most applications. The inductor resistance must be less than 300 mΩ for good efficiency. See detailed information in Texas Instruments Application Note *Understanding Boost Power Stages in Switch Mode Power Supplies* (SLVA061). “Power Stage Designer™ Tools” can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

7.2.1.2.2 Output Capacitor Selection

A ceramic capacitor with a 100-V voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, a consideration for capacitance value selection. Effectively the capacitance must be 33 µF for 600-mA loads. A different option is to use an aluminum electrolytic capacitor with low ESR and ceramic capacitor in parallel. Typically a 33-µF (ESR < 500 mΩ) with 10-µF (effective) ceramic capacitor in parallel is sufficient. If ESR is lower, capacitance for ceramic capacitor can be decreased.

For higher switching frequency (2.2 MHz) and boost output current below 400 mA, two 10-µF ceramic capacitors in parallel are sufficient.

7.2.1.2.3 Input Capacitor Selection

A ceramic capacitor with 50-V voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, a consideration for capacitance value selection. Effectively the capacitance must be 33 µF for 600-mA loads. A different option is to use an aluminum electrolytic capacitor with low ESR and ceramic capacitor in parallel. Typically a 33-µF (ESR < 500 mΩ) with 10-µF (effective) ceramic capacitor in parallel is sufficient. If ESR is lower, capacitance for ceramic capacitor can be decreased.

For higher switching frequency (2.2 MHz) and boost output current below 400 mA two 10-µF ceramic capacitors in parallel are sufficient.

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7.2.1.2.4 Charge Pump Output Capacitor

A ceramic capacitor with at least 16-V voltage rating is recommended for the output capacitor of the charge pump. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 10-µF capacitor is sufficient.

7.2.1.2.5 Charge Pump Flying Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the flying capacitor of the charge pump. Typically 1-µF capacitor is sufficient.

7.2.1.2.6 Diode

A Schottky diode must be used for the boost output diode. Peak repetitive current must be greater than inductor peak current (up to 9 A) to ensure reliable operation. Average current rating must be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage. Do not use ordinary rectifier diodes because slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

7.2.1.2.7 Boost Converter Transistor

An nFET transistor with high enough voltage rating (V_{DS} at least 5 V higher than maximum output voltage) must be used. Current rating for the FET must be the same as the inductor peak current. Gate-drive voltage for the FET is VDD or about 2 x VDD, if the charge pump is enabled (EEPROM selection).

7.2.1.2.8 Boost Sense Resistor

A high-power 25-mΩ resistor must be used for sensing the boost SW current. Power rating can be calculated from the inductor current and sense resistor resistance value.

7.2.1.2.9 Power Line Transistor

A pFET transistor with necessary voltage rating (V_{DS} at least 5 V higher than max input voltage) must be used. Current rating for the FET must be the same as input peak current or greater. Transfer characteristic is very important for pFET. V_{GS} for open transistor must be less then V_{IN}. A 20-kΩ resistor between the pFET gate and source is sufficient.

If a pFET with high enough V_{DS} and low V_{GS} is not available, it is possible to use an nFET with extra external components with the EEPROM bit NMOS_PLFET_EN set high. See *セクション 6.3.7* section (図 6-17) for using the nFET as a power-line FET.

7.2.1.2.10 Input Current Sense Resistor

A high-power 20-mΩ resistor must be used for sensing the boost input current. Power rating can be calculated from the input current and sense resistor resistance value.

7.2.1.2.11 Filter Component Values

表 7-2 shows recommended filter component values for the VSYNC PLL filter (phase margin 60°). An external filter must be used only when external VSYNC is used; otherwise, the LP8860-Q1 uses internal compensation.

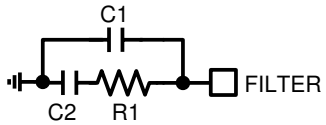

図 7-2. Filter Components

表 7-2. Filter Components Selection

V/H SYNC	PLL FREQUENCY (MHz)	C1	C2	R1
50 Hz (BW3dB = 1 Hz)	5	100 nF	1.4 µF	85 kΩ
	10	54 nF	0.7 µF	170 kΩ
	20	27 nF	0.35 µF	338 kΩ
	40	13.6 nF	0.175 µF	677 kΩ
20 kHz (BW3dB = 330 Hz)	5	10 nF	129 nF	14 kΩ
	10	5 nF	65 nF	28 kΩ
	20	2.5 nF	32 nF	56 kΩ
	40	1.2 nF	16 nF	112 kΩ
50 kHz (BW3dB = 330 Hz)	5	22 nF	322 nF	5.6 kΩ
	10	12 nF	161 nF	11.2 kΩ
	20	6.2 nF	80 nF	22.3 kΩ
	40	3.1 nF	40 nF	44,7 kΩ

7.2.1.2.11.1 Critical Components for Design

Schematic on 図 7-3 shows the critical part of circuitry: boost components, the LP8860-Q1 internal charge pump for gate driver powering and powering/grounding of LP8860-Q1 boost components. Layout example for this is shown in 図 7-15.

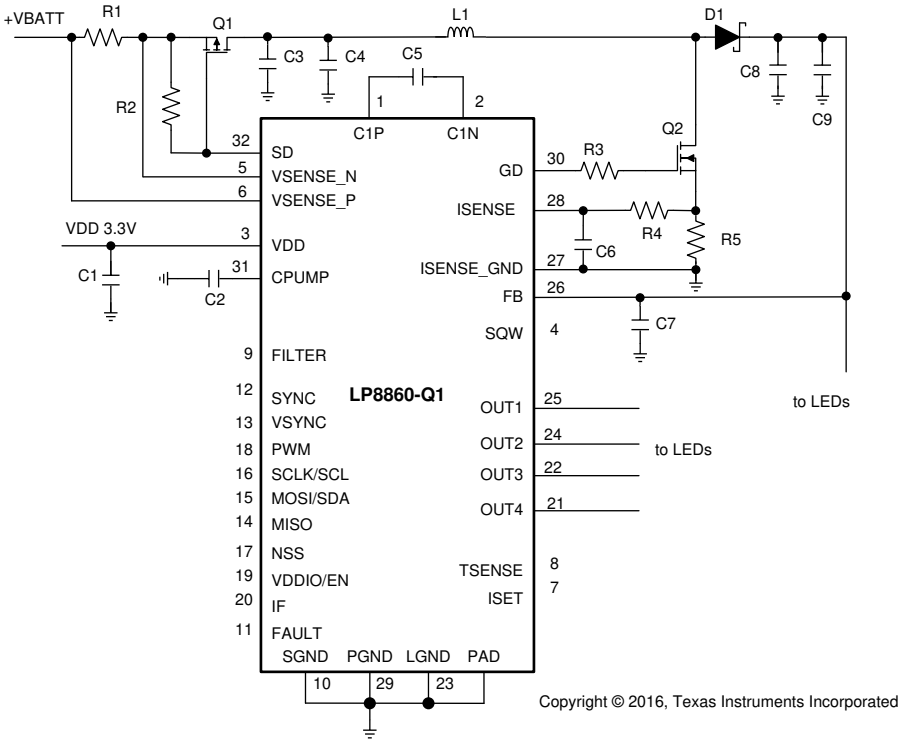

図 7-3. Critical Components for Design

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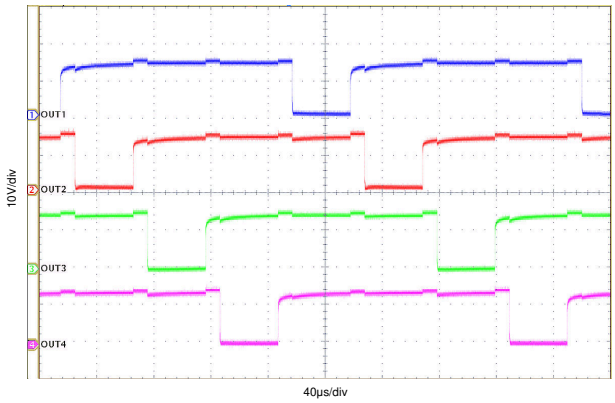
表 7-3. Bill of Materials for Design Example

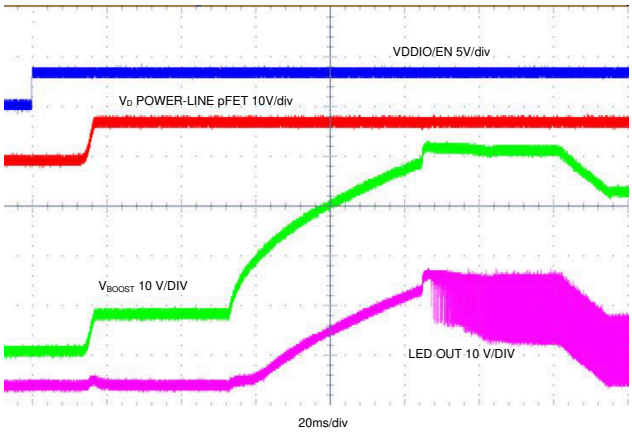
REFERENCE DESIGNATOR	DESCRIPTION	NOTE
R1	20 mΩ 3 W	Input current sensing resistor
R2	20 kΩ 0.1 W	Power-line FET gate pullup resistor
R3	10 Ω 0.1 W	Gate resistor for boost FET
R4	10 Ω 0.1 W	Current sensing filter resistor
R5	25 mΩ 3 W	Boost current sensing resistor
C1	1 µF 10 V ceramic capacitor	VDD bypass capacitor
C2	10 µF 16 V ceramic capacitor	Charge pump output capacitor
C3	33 µF 50 V electrolytic capacitor	Boost input capacitor
C4	10 µF 50 V ceramic capacitor	Boost input capacitor
C5	1 µF 10 V ceramic capacitor	Flying capacitor
C6	1000 pF 10 V ceramic capacitor	Current sensing filter capacitor
C7	39 pF 50 V ceramic capacitor	High frequency bypass capacitor
C8	33 µF 50 V electrolytic capacitor	Boost output capacitor
C9	10 µF 100 V ceramic capacitor	Boost output capacitor
L1	22 µH saturation current 9 A	Boost inductor
D1	60 V 15 A Schottky diode	Boost Schottky diode
Q1	60 V 10 A pMOSFET	Power-line FET
Q2	60 V 15 A nMOSFET	Boost nMOSFET

7.2.1.3 Application Performance Plots



f_{LED_PWM} = 4.9 kHz　　Phase shift 90°　　4 strings

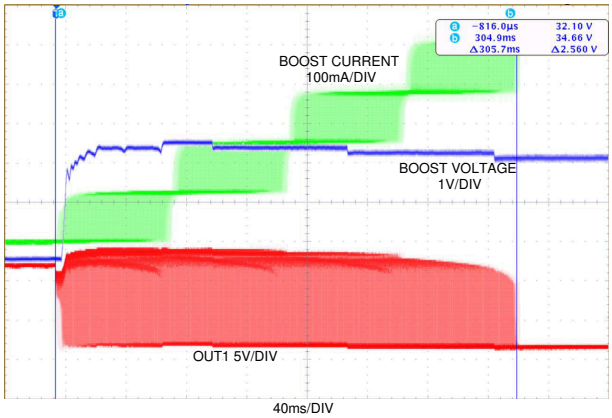
図 7-4. Voltage of LED Outputs Showing Phase-Shift PWM Operation



f_{SW} = 303 kHz　　130 mA/string

C_{IN} = C_{OUT}= 33 µF(el) + 10 µF(cer)

図 7-5. Typical Start-up

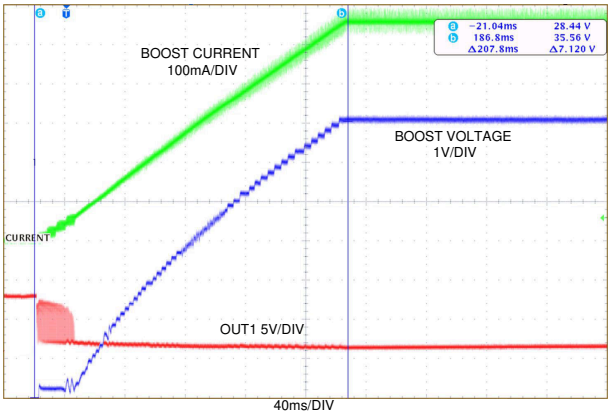


PWM_SLOPE = 110　　130 mA/string　　Phase Shift = 90°

4 strings　　10 LED/string

EN_ADVANCED_SLOPE = 0

図 7-6. Slope with Phase-Shift Mode



EN_PWM_I = 1　　I_SLOPE =000　　130 mA/string

PWM_SLOPE = 101　　GAIN_CTRL = 111　　4 strings

EN_ADVANCED_SLOPE = 0　　Phase Shift = 90°

図 7-7. Slope With Hybrid Dimming and Phase Shift

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7.2.2 Low VDD Voltage and Combined Output Mode Application

図 7-8 shows the application for LED strings in Display mode (OUT1 and OUT2) and Cluster mode (OUT3 and OUT4). External powering must be used for Cluster-mode LED strings. VDD voltage is 3.3 V, and the charge pump for gate driver powering is enabled.

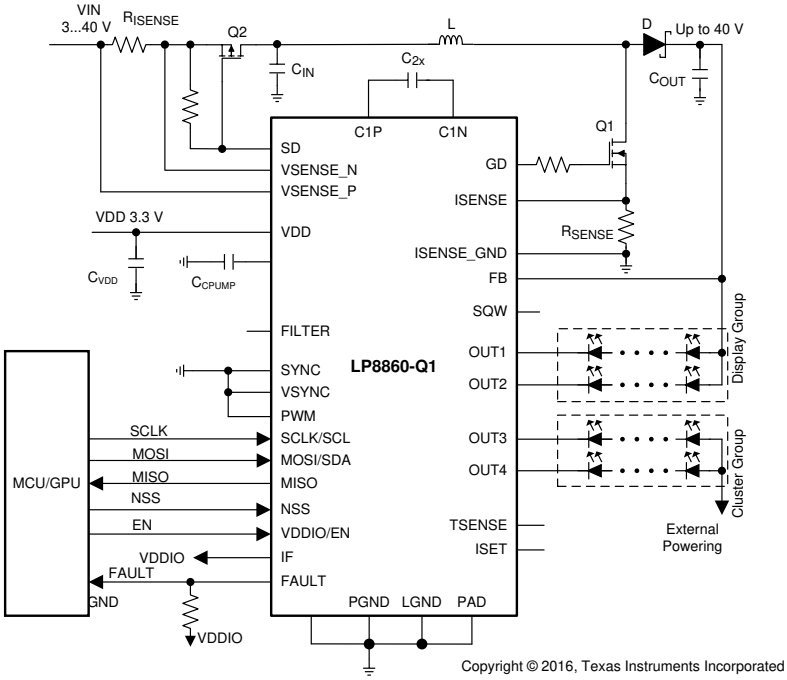

図 7-8. VDD = 3.3V, SPI, 2 Outputs in Display Mode, 2 in Cluster Mode Schematic

7.2.2.1 Design Requirements

表 7-4. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	ED
61	DF
62	DC
63	F4
64	DF
65	E5
66	F2
67	77
68	77
69	71
6A	3F
6B	B7
6C	17
6D	EF
6E	B0
6F	87
70	CF
71	72
72	E5
73	DF
74	35
75	06
76	DE
77	FF
78	3E

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 40 V
VDD voltage	3.3 V
Charge pump	Enabled
Brightness Control	SPI
Output configuration	Mode 2, OUT1 and OUT2 - display mode (phase shift 180°), OUT3 and OUT4 - cluster mode
LED string current	OUT1 and OUT2 - 130 mA; OUT3 - 30 mA; OUT4 - 33 mA
External current set resistor	Disabled
Boost frequency	303 kHz
Inductor	22 µH to 33 µH, at least 5-A saturation current
Input/Output capacitors	10 µF ceramic and 33 µF electrolytic
Current dimming with external NTC	Disabled

7.2.2.2 Detailed Design Procedure

See *セクション 7.2.1.2*.

7.2.2.3 Application Performance Plots

See *セクション 7.2.1.3*.

7.2.3 High Output Voltage Application

The LP8860-Q1 has ability to control up to 16 or 17 LEDs per string with additional external components for output overvoltage protection. nFET transistors can protect outputs, and SQW output can be used to produce extra rail voltage for the transistor gates, if necessary voltage is not available in the system.

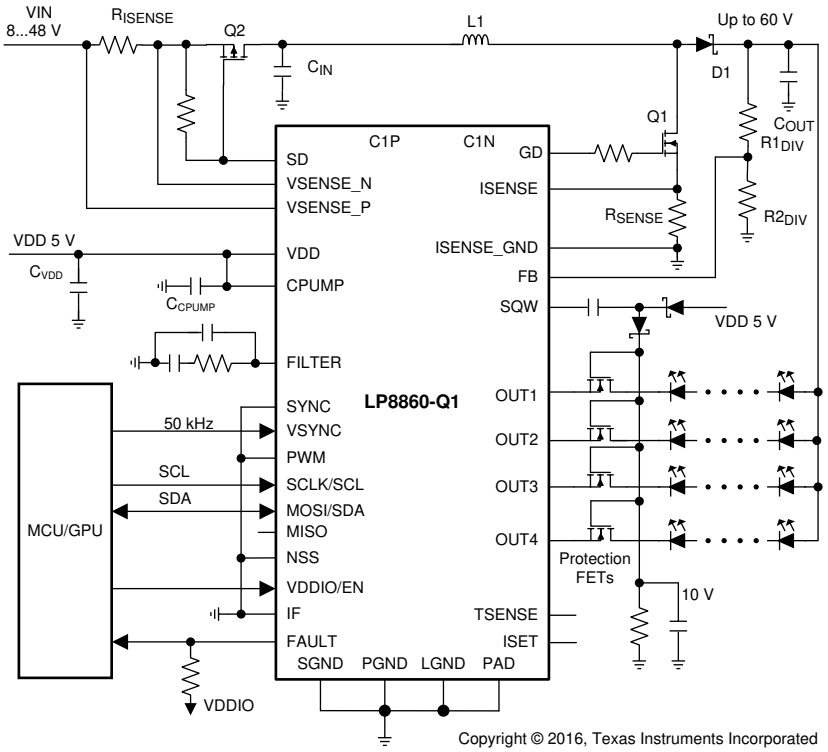

図 7-9. VDD = 5 V, I²C, High-Voltage Output with Output Protection FETs Circuits

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7.2.3.1 Design Requirements

表 7-5. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	ED
61	DF
62	DC
63	F4
64	DF
65	E5
66	F2
67	77
68	77
69	71
6A	3F
6B	B7
6C	17
6D	EF
6E	B0
6F	87
70	CF
71	72
72	E5
73	DF
74	35
75	06
76	DE
77	FF
78	3E

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 48 V
VDD voltage	5 V
Charge pump	Disabled
Brightness Control	I^2C
Output configuration	Mode 0, all outputs are in display mode, phase shift 90°, synchronized with VSYNC 50kHz, 10 LEDs per string, f_{LED_PWM}= 10 kHz
LED string current	OUT1 to OUT4 - 120 mA
External current set resistor	Disabled
Boost frequency	303 kHz
Inductor	22 µH to 33 µH, at least 9-A saturation current
Input/Output capacitors	10 µF ceramic and 33 µF electrolytic
Current dimming with external NTC	Disabled
VSYNC	Enabled, 50 kHz
Feedback voltage divider	$R1_{DIV}$ = 30 kΩ, $R2_{DIV}$ = 150 kΩ

7.2.3.2 Detailed Design Procedure

See *セクション 7.2.1.2*.

7.2.3.3 Application Performance Plots

See *セクション 7.2.1.3*.

7.2.4 High Output Current Application

The LP8860-Q1 outputs can be tied together to drive LED with higher current. To drive a 300 mA/string, connect 2 outputs together. All 4 outputs connected together can drive up to a 600-mA LED string.

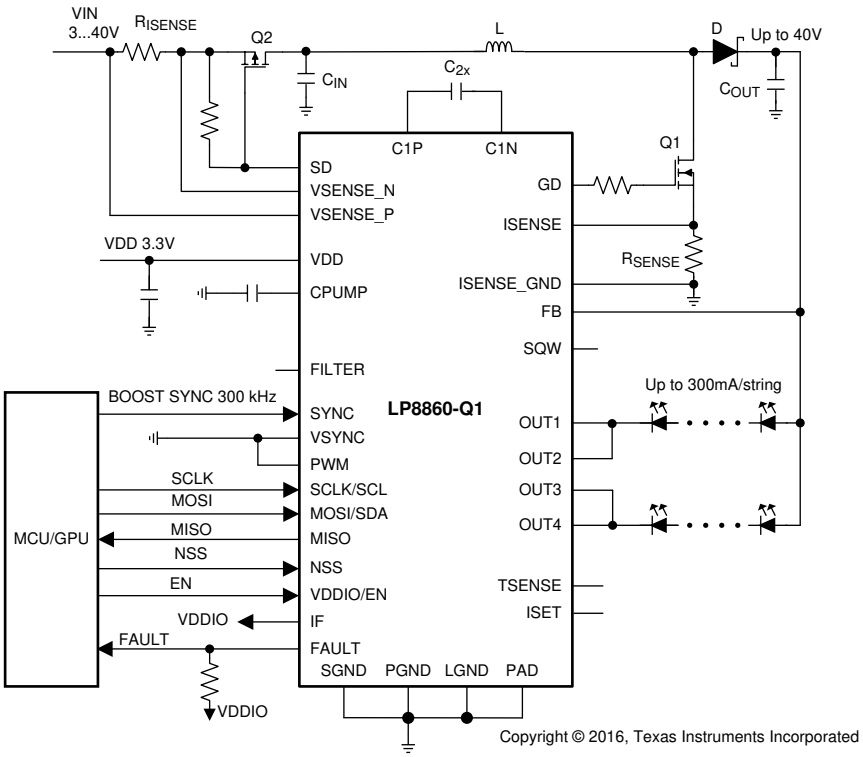

図 7-10. Two Channels at 300 mA/String, VDD = 3.3 V, SPI

7.2.4.1 Design Requirements

表 7-6. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	EF
61	FF
62	DC
63	F8
64	DF
65	E5
66	F2
67	77
68	77
69	71
6A	3F
6B	B7
6C	17
6D	EF
6E	B1
6F	87
70	DF
71	72
72	E5
73	DF
74	35
75	06
76	DE
77	FF
78	3E

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 40 V
VDD voltage	3.3 V

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DESIGN PARAMETER	VALUE
Charge pump	Enabled
Brightness Control	SPI
Output configuration	Mode 4, OUT1 to OUT4 in display mode, phase shift between tied groups 180°
LED string current	OUT1 and OUT2 - 300 mA; OUT3 and OUT4 - 300 mA
External current set resistor	Disabled
Boost frequency	300 kHz externally synchronized
Inductor	22 µH to 33 µH, at least 9-A saturation current
Input/Output capacitors	10-µF ceramic and 33-µF electrolytic
Current dimming with external NTC	Disabled

7.2.4.2 Detailed Design Procedure

See *セクション 7.2.1.2*.

7.2.4.3 Application Performance Plots

See *セクション 7.2.1.3*.

7.2.5 Three-Channel Configuration Without Serial Interface

Outputs which are not used can be left floating. In this example 3 outputs are in use. PSPWM mode for 3 outputs is set to mode 1 <LED_STRING_CONF[2:0]> = 001b, and the serial interface is not used. The device is enabled with the EN/VDDIO pin, and brightness control is set with the PWM input. EEPROM settings must be pre-programmed for brightness dimming with external PWM.

LED current dimming with external NTC sensor is used in this application to protect LEDs against over-heating.

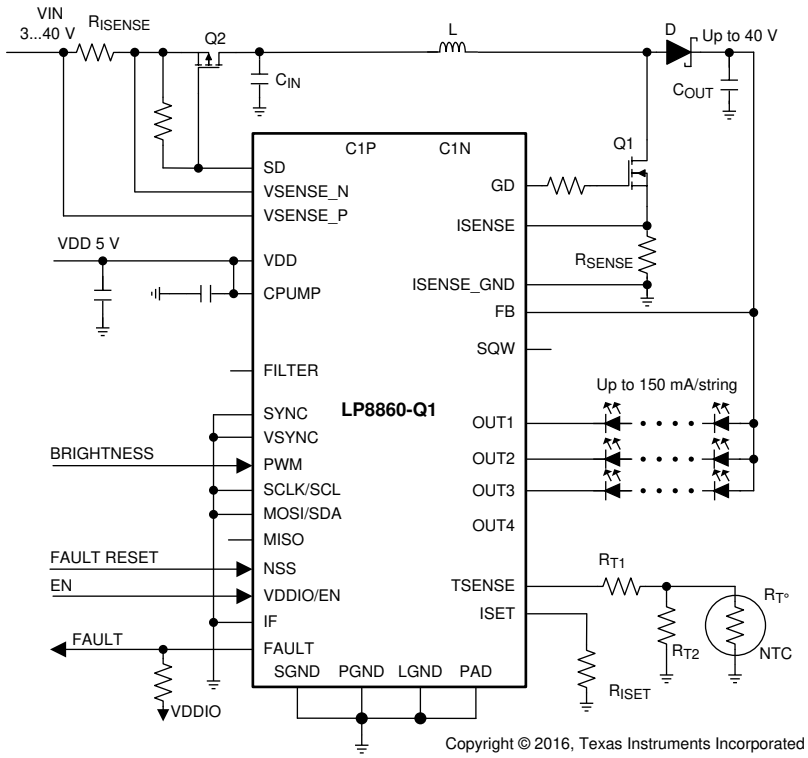

図 7-11. Three-Channel Configuration without Serial Interface

7.2.5.1 Design Requirements

表 7-7. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	6F
61	FF
62	DC
63	F2
64	DF
65	E5
66	F8
67	77
68	77
69	E1
6A	BF
6B	B7
6C	17
6D	EF
6E	B1
6F	87
70	CE
71	72
72	E5
73	DF
74	35
75	06
76	DC
77	CF
78	3F

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 40 V
VDD voltage	5 V
Charge pump	Disabled
Brightness Control	PWM
Output configuration	Mode 1, OUT1 to OUT3 - display mode; OUT4 - not used
LED string current	OUT1 to OUT3 - 150 mA
External current set resistor	Enabled, R_{ISET} = 24 kΩ
Boost frequency	303 kHz
Inductor	22 µH to 33 µH, at least 6-A saturation current
Input/Output capacitors	10-µF ceramic and 33 µF electrolytic
Current dimming with external NTC	Enabled,$R_{T°}$= NCP15XH103F03RC (Murata), see 図 7-12, R_{T1} = 6.6 kΩ, R_{T2} not assembled

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7.2.5.2 Detailed Design Procedure

LED current dimming with external NTC sensor is used in this application — see section *セクション 6.3.9.4* for details. 図 7-13 shows LED current de-rating versus temperature measured by NTC sensor with characteristic shown in 図 7-12.

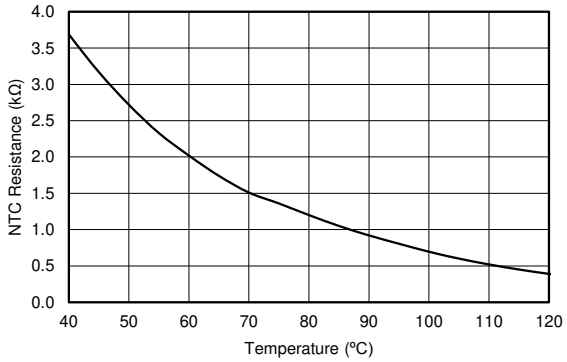

図 7-12. NTC Sensor Resistance vs Temperature

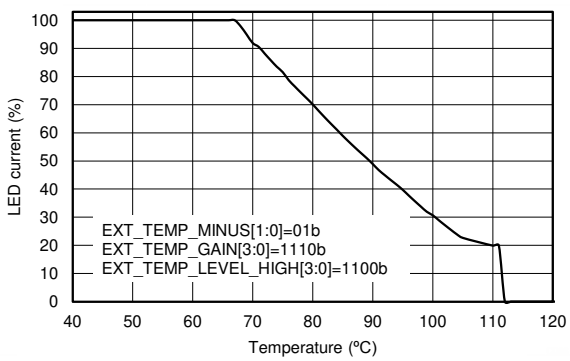

図 7-13. LED Current De-rating vs Temperature

7.2.5.3 Application Performance Plots

See *セクション 7.2.1.3*.

7.2.6 Solution With Minimum External Components

The LP8880-Q1 needs only a few external components for basic functionality if material cost and PCB area for a LP8860-Q1-based solution need to be minimized. In this example the power-line FET is removed, as is input current sensing. External synchronization functions are disabled.

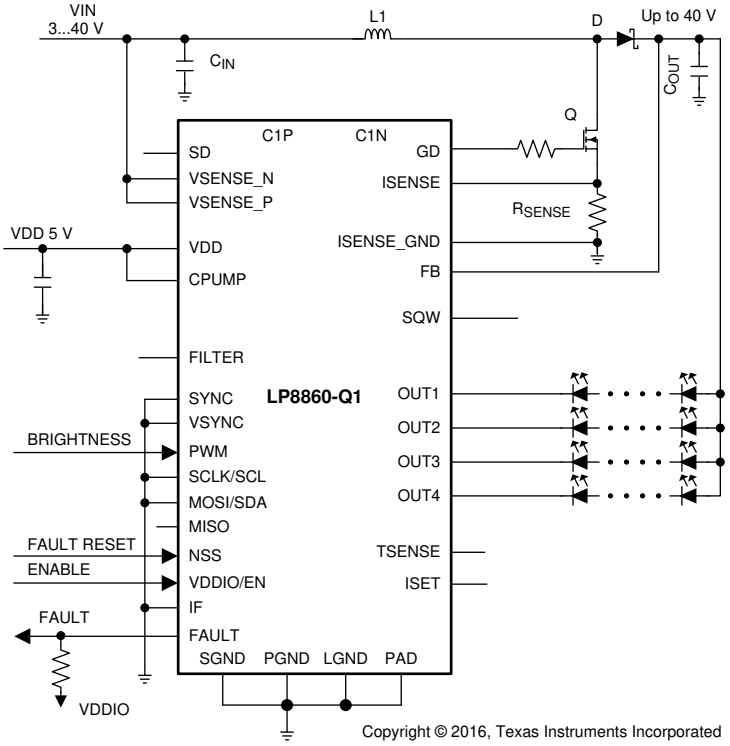

図 7-14. Solution With Minimum External Components

7.2.6.1 Design Requirements

表 7-8. EEPROM Setting Example

ADDRESS (HEX)	DATA (HEX)
60	EF
61	FF
62	DC
63	D0
64	DF
65	E5
66	F0
67	77
68	77
69	71
6A	3F
6B	B7
6C	17
6D	EF
6E	B0
6F	87
70	CE
71	07
72	E5
73	DF
74	75
75	86
76	DC
77	FF
78	3E

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 40 V
VDD voltage	5 V
Charge pump	Disabled
Brightness Control	PWM
Output configuration	Mode0, OUT1 to OUT4 in display mode, phase shift 90°
LED string current	OUT1 to OUT4 - 100 mA
External current set resistor	Disabled
Boost frequency	2.2 MHz
Inductor	4.7 µH to 22 µH, at least 6-A saturation current
Input/Output capacitors	2 × 10-µF ceramic
Current dimming with external NTC	Disabled

7.3 Power Supply Recommendations

The LP8860-Q1 is designed to operate from a car battery. V_{IN} input must be protected from reversal voltage and voltage dump over 48 Volts. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor .

The voltage range for VDD is 3 V to 5.5 V. A ceramic capacitor must be placed as close as possible to the VDD pin. The boost gate driver is powered from the VDD pin; this must be taken into account. For high boost frequency and high internal PLL frequency (can be up to 40 MHz), power consumption from VDD pin can be around 20 mA to 40 mA.

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7.4 Layout

7.4.1 Layout Guidelines

図 7-15 shows a layout recommendation for the LP8860-Q1. 図 7-15 is used to show the principles of good layout. This layout can be adapted to the actual application layout if and where possible. It is important that all boost components are close to each other and to the device; the high-current traces must be wide enough. VDD must be as noise-free as possible. Place a VDD bypass capacitor near the pin and ground it to a noise-free ground. A charge-pump capacitor and boost input and output capacitors must be connected to PGND. Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close to each other as possible. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents try to find route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
  - For high frequency the copper area capacitance must be taken into account. For example, the copper area for the drain of boost nMOSFET is a tradeoff between capacitance and components cooling capacity.
- GND plane must be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting must be in the same direction in optimal case.
- Inductors must be placed so that the current flows in the same direction as in the current loops. Rotating the inductor 180° changes current direction.
- Use separate power and noise-free grounds. The power ground is used for boost converter return current and noise-free ground for more sensitive signals, like VDD bypass capacitor grounding as well as grounding the GND pins of the LP8860-Q1 itself.
- Boost output feedback voltage to LEDs need to be taken out *after* the output capacitors, not straight from the diode cathode.
- A small (for example, 39-pF) bypass capacitor must be placed close to the FB pin to suppress high frequency noise
- VDD line must be separated from the high current supply path to the boost converter to prevent high frequency ripple affecting the chip behavior. A separate 1-µF bypass capacitor is used for the VDD pin, and it is grounded to noise-free ground.
- Capacitor connected to charge pump output CPUMP must have 10-µF capacitance, grounded by shortest way to boost switch current sensing resistor. This capacitor must be as close as possible to CPUMP pin. This capacitor provides a greater peak current for gate driver and must be used even if the charge pump is disabled. If the charge pump is disabled, the VDD and CPUMP pins must be tied together.
- Input and output capacitors need strong grounding (wide traces, many vias to PGND plane).
- If two or more output capacitors are used, symmetrical layout must be used to get all capacitors working ideally.
- Input/output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads. DC bias characteristics need to be obtained from the component manufacturer; it is not taken into account on component tolerance. TI recommends X5R/X7R capacitors.

7.4.2 Layout Example

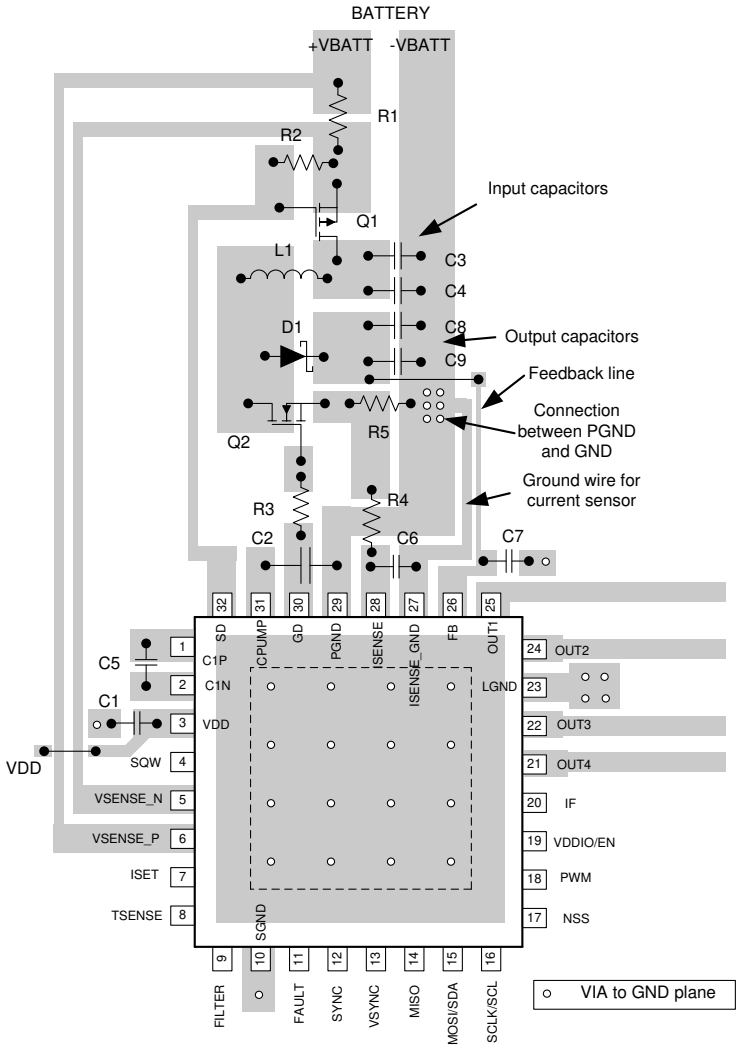

図 7-15. LP8860-Q1 Layout

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8 Device and Documentation Support

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package Application Note*
- *Understanding Boost Power Stages in Switch Mode Power Supplies*
- Power Stage Designer™ Tools

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Community Resources

8.5 Trademarks

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9 Revision History

Changes from Revision G (October 2017) to Revision H (April 2025)	Page
• Add Application Note link to *"LP8860-Q1 Electrical Overstress Analysis and Recommendation (SNVA843)"*	30
• Add Application Note link to *"LP8860-Q1 Boost Compensation Registers (SNVA789A)"*	34

Changes from Revision F (July 2017) to Revision G (October 2017)	Page
• Updated with more detailed package drawings	102

Changes from Revision E (November 2016) to Revision F (July 2017)	Page
• Changed placement of "7" data hold time in 図 5-2	12
• Deleted "The LP8860-Q1 doesn't support incremental addressing." after 表 6-20	50
• Changed "short" to "open" in DRV_HEADER[2:0] row, *セクション 6.6.2.5*	69

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8860AQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860AQ1
LP8860AQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860AQ1
LP8860AQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860AQ1
LP8860BQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860BQ1
LP8860BQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860BQ1
LP8860BQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860BQ1
LP8860CQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860CQ1
LP8860CQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860CQ1
LP8860CQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860CQ1
LP8860DQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860DQ1
LP8860DQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860DQ1
LP8860DQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860DQ1
LP8860HQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860HQ1
LP8860HQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860HQ1
LP8860HQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860HQ1
LP8860JQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860JQ1
LP8860JQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860JQ1
LP8860JQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860JQ1
LP8860LQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860LQ1
LP8860LQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860LQ1
LP8860LQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860LQ1
LP8860NQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860NQ1
LP8860NQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860NQ1
LP8860NQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860NQ1
LP8860RQVFPRQ1	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860RQ1
LP8860RQVFPRQ1.A	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860RQ1
LP8860RQVFPRQ1.B	Active	Production	HLQFP (VFP) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8860RQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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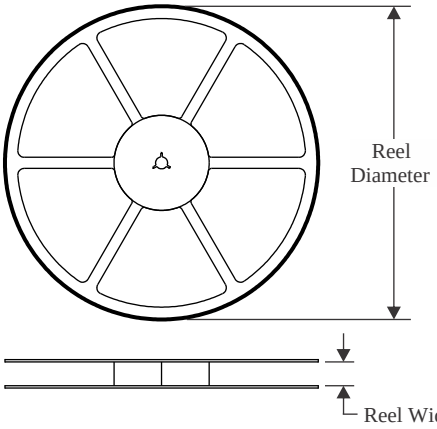
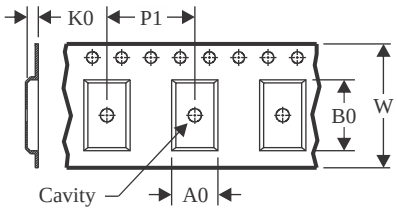
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

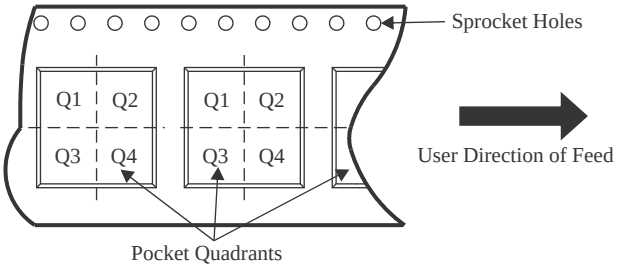


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

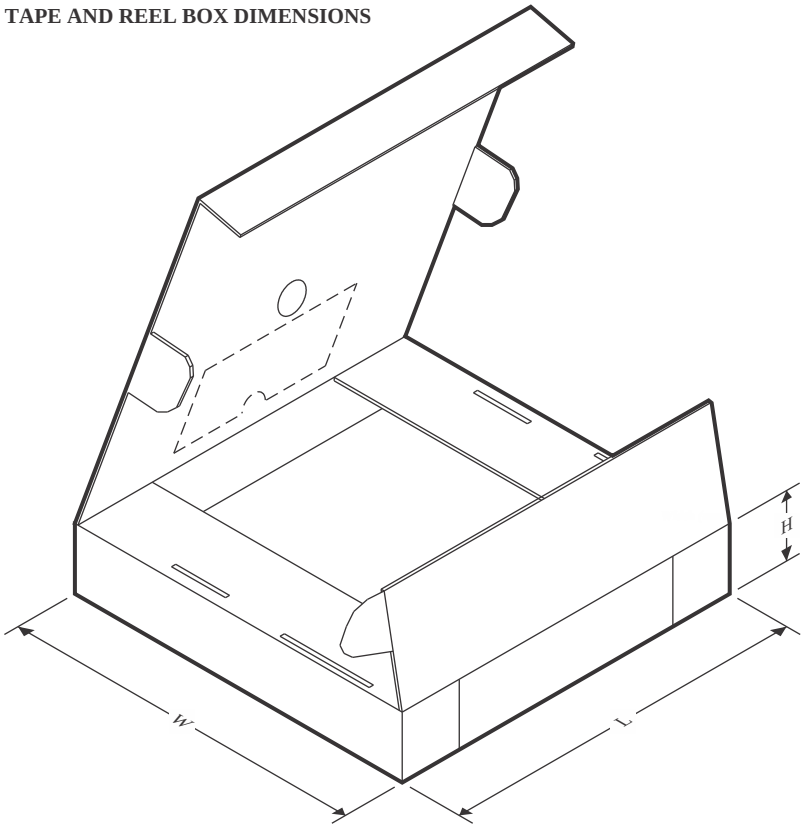
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8860AQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860BQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860CQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860DQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860HQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860JQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860LQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860NQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
LP8860RQVFPRQ1	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

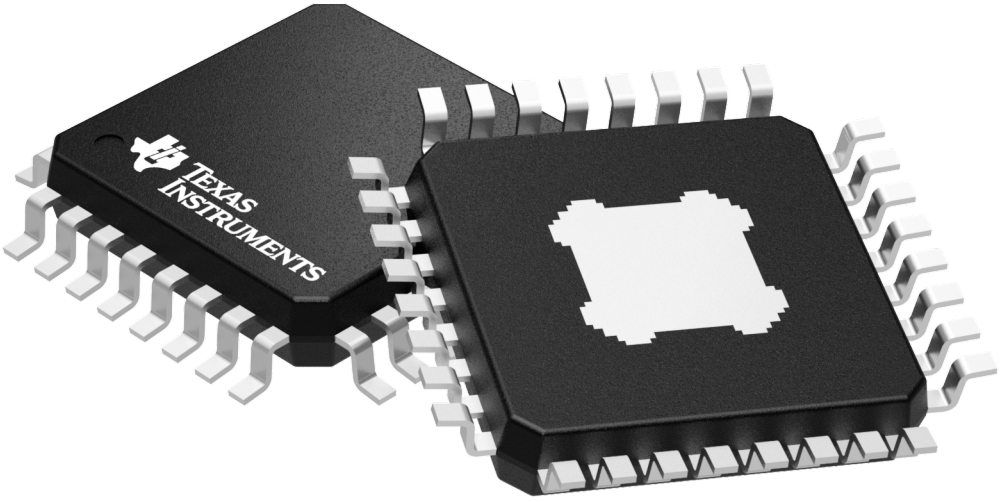


*All dimensions are nominal

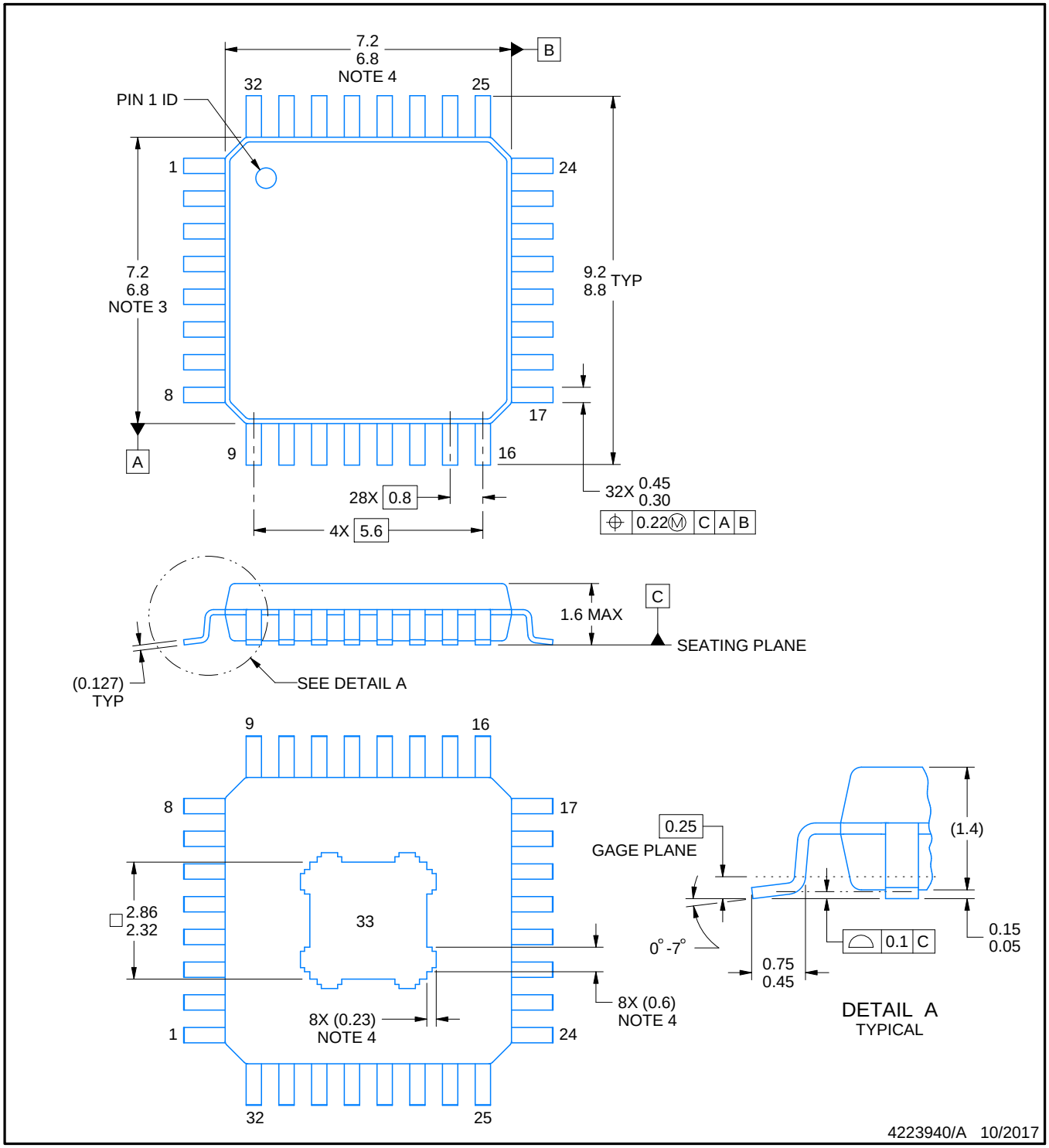
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8860AQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860BQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860CQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860DQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860HQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860JQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860LQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860NQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0
LP8860RQVFPRQ1	HLQFP	VFP	32	1000	350.0	350.0	43.0

VFP 32 PowerPAD™ LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



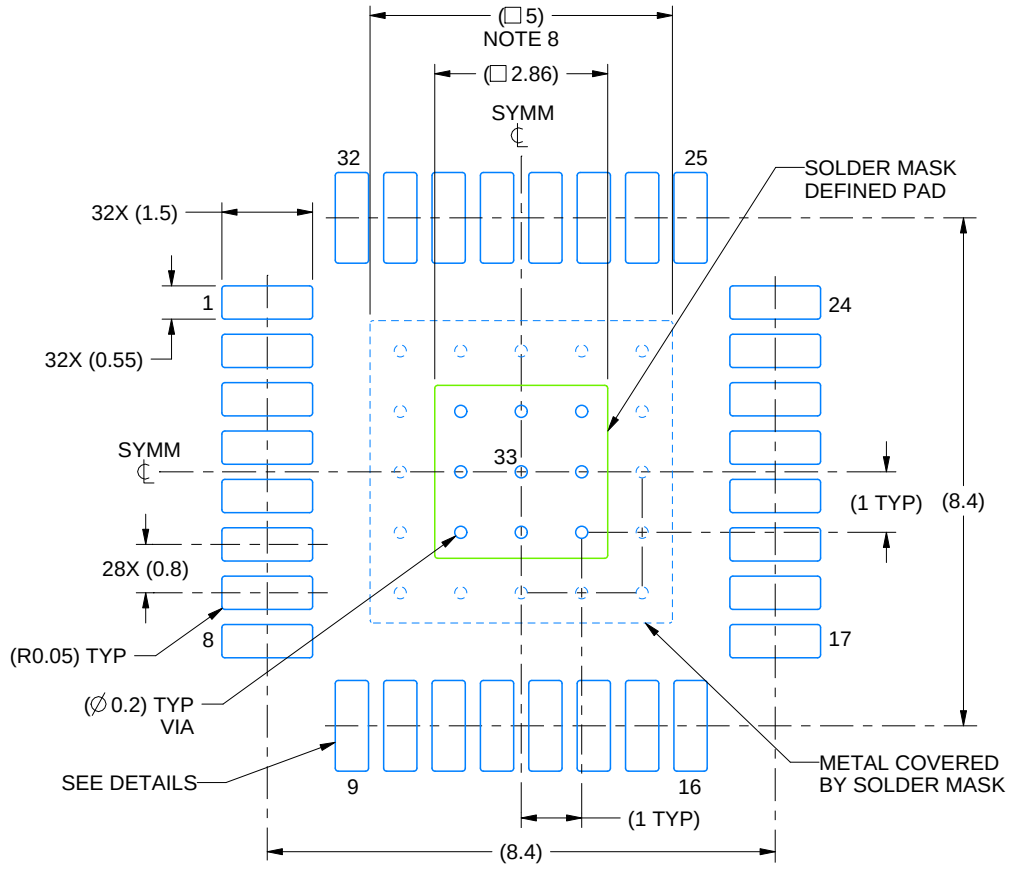
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



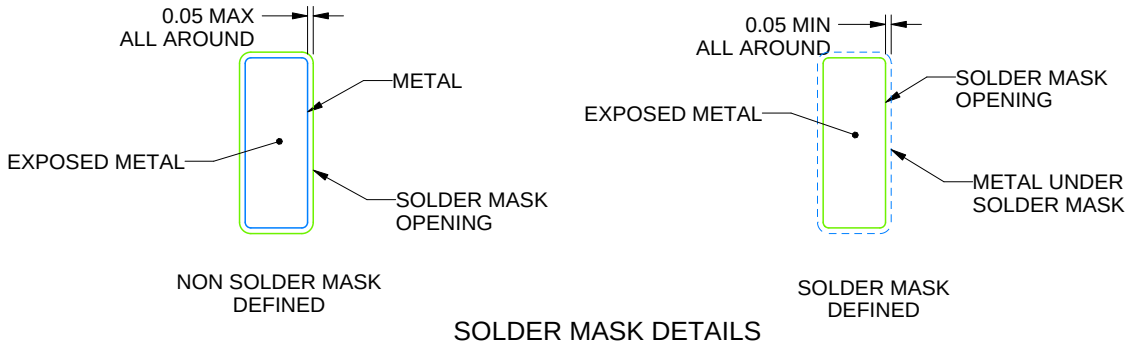
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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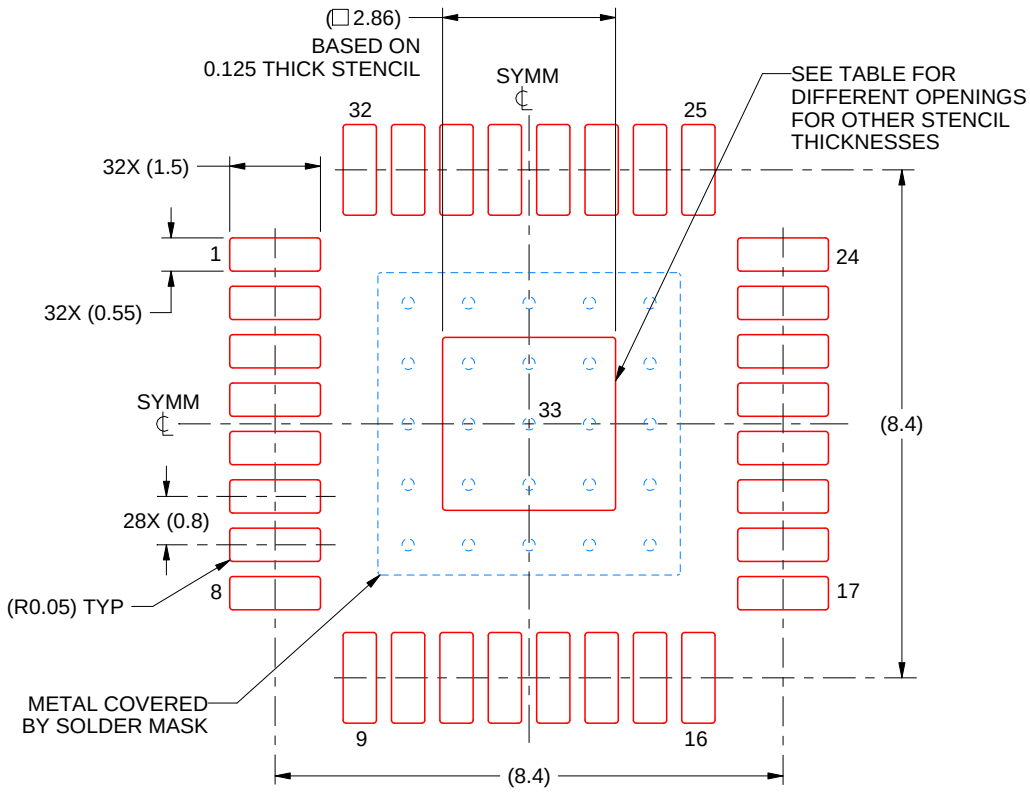
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.20 X 3.20
0.125	2.86 X 2.86 (SHOWN)
0.15	2.61 X 2.61
0.175	2.42 X 2.42

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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