

LP8762-Q1 4 相、12A 降圧コンバータ、内蔵スイッチ付き

1 特長

- 以下の結果で AEC-Q100 認定済み:
 - 入力電圧: 2.8V~5.5V
 - デバイス温度グレード 1: 動作時周囲温度範囲 -40°C~+125°C
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- 機能安全準拠
 - 機能安全アプリケーション向けに開発
 - ASIL-D までの ISO 26262 システムの設計に役立つ資料を提供
 - SIL-3 までの IEC 61508 システムの設計に役立つ資料を提供
 - ASIL-D までの決定論的対応能力
 - ASIL-D までのハードウェア安全度
 - 電圧および過電流のウィンドウ モニタ
 - トリガ / Q&A モードを選択可能なウォッチドッグ
 - レベルまたは PWM エラー信号モニタ (ESM)
 - 温度監視と高温警告およびサーマル シャットダウン
 - 構成レジスタと不揮発性メモリ (NVM) のビット整合性 (CRC) エラー検出
- 4 つの高効率降圧 DC/DC コンバータ:
 - 出力電圧: 0.3V~3.34V (多相出力で 0.3V~1.9V)
 - 最大出力電流: 1 相あたり 3A、4 相構成で最大 12A
 - 出力電圧のスルーレートをプログラム可能: 0.5mV/μs~33mV/μs
 - スイッチング周波数: 2.2MHz または 4.4MHz
- 設定が可能な 10 個の汎用 I/O (GPIO)
- マルチ PMIC 同期用 SPMI インターフェイス
- 入力過電圧保護 (OVP) および低電圧誤動作防止 (UVLO)

2 アプリケーション

- 先進運転支援システム (ADAS)
- フロント カメラ
- サラウンド ビュー システムの ECU
- 長距離レーダー
- センサ フュージョン
- ドメイン コントローラ

3 概要

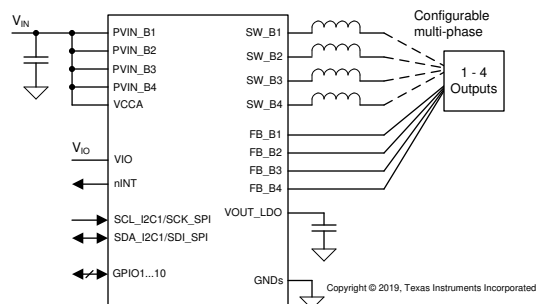
LP8762-Q1 デバイスは、さまざまな車載用および産業用の安全関連アプリケーションで、最新のプロセッサおよびプラットフォームの電力管理要件を満たすよう設計されています。このデバイスには 4 つの降圧 DC/DC コンバータコアがあり、この出力は、5 種類の相構成が可能で、1 つの 4 相出力から 4 つの単相出力までを選択できます。デバイス設定は、I²C 互換のシリアル インターフェイス、または SPI シリアル インターフェイスにより変更可能です。

自動 PFM/PWM (AUTO モード) 動作と、自動相加算および相減算により、広い範囲の出力電流について最大の効率が得られます。LP8762-Q1 デバイスは、多相出力のリモート差動電圧センシングに対応しており、レギュレータ出力とポイント オブ ロード (POL) との間の IR 降下を補償することで出力電圧の精度を高めることができます。スイッチング クロックを強制的に PWM モードに設定することができ、位相をインターリーブします。スイッチングを外部クロックと同期させることができ、拡散スペクトラム モードを有効にすることにより、外乱による変動を最小限に抑えられます。

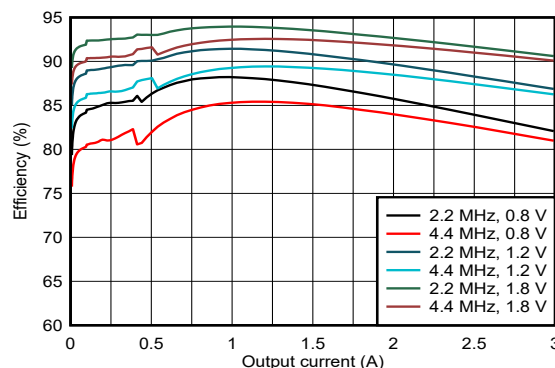
製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
LP8762-Q1	VQFN-HR (32)	5.50mm × 5.00mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図



効率と出力電流との関係 (1 相)



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4 Device Comparison Table

The LP8762-Q1 device family has several sub-family variants as outlined below:

表 4-1. Device Sub-Family Variants

Sub-Family Variant	Orderable Part Number	DC/DC Configuration
LP87621-Q1	LP87621xyyRQKRQ1	One 4-phase output
LP87622-Q1	LP87622xyyRQKRQ1	One 3-phase and One 1-phase outputs
LP87623-Q1	LP87623xyyRQKRQ1	One 2-phase and two 1-phase outputs
LP87624-Q1	LP87624xyyRQKRQ1	Four 1-phase outputs
LP87625-Q1	LP87625xyyRQKRQ1	Two 2-phase outputs

Each of these sub-families have non-volatile memory (NVM) and other configuration options. The NVM option is configured by Texas Instruments, generating unique device configurations with specific orderable part numbers represented by the YY in the part numbers. Please see the Technical Reference Manual of the specific LP8762-Q1 device for the NVM configuration implemented.

The orderable part numbering of these sub-families is summarized by:

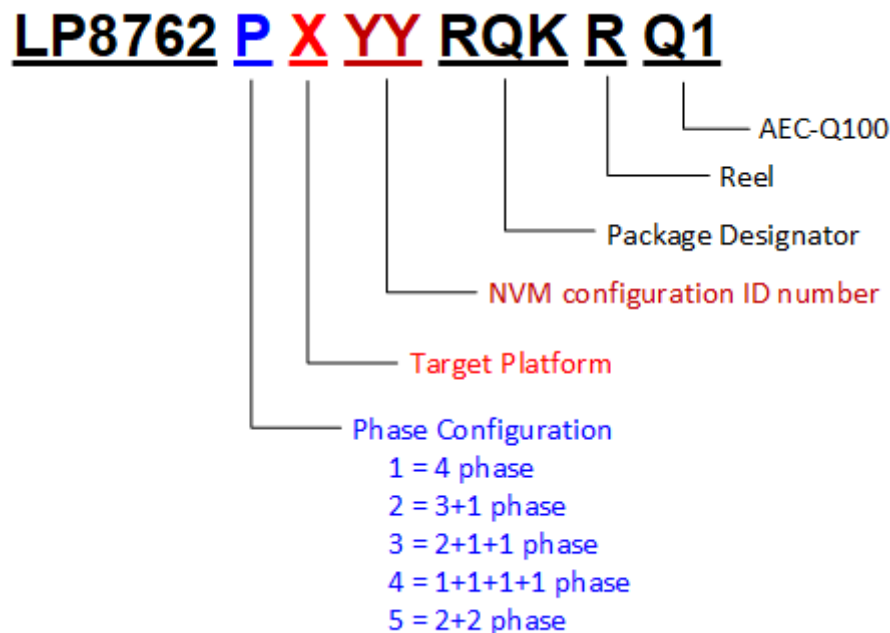


図 4-1. Orderable Part Numbering

5 Pin Configuration and Functions

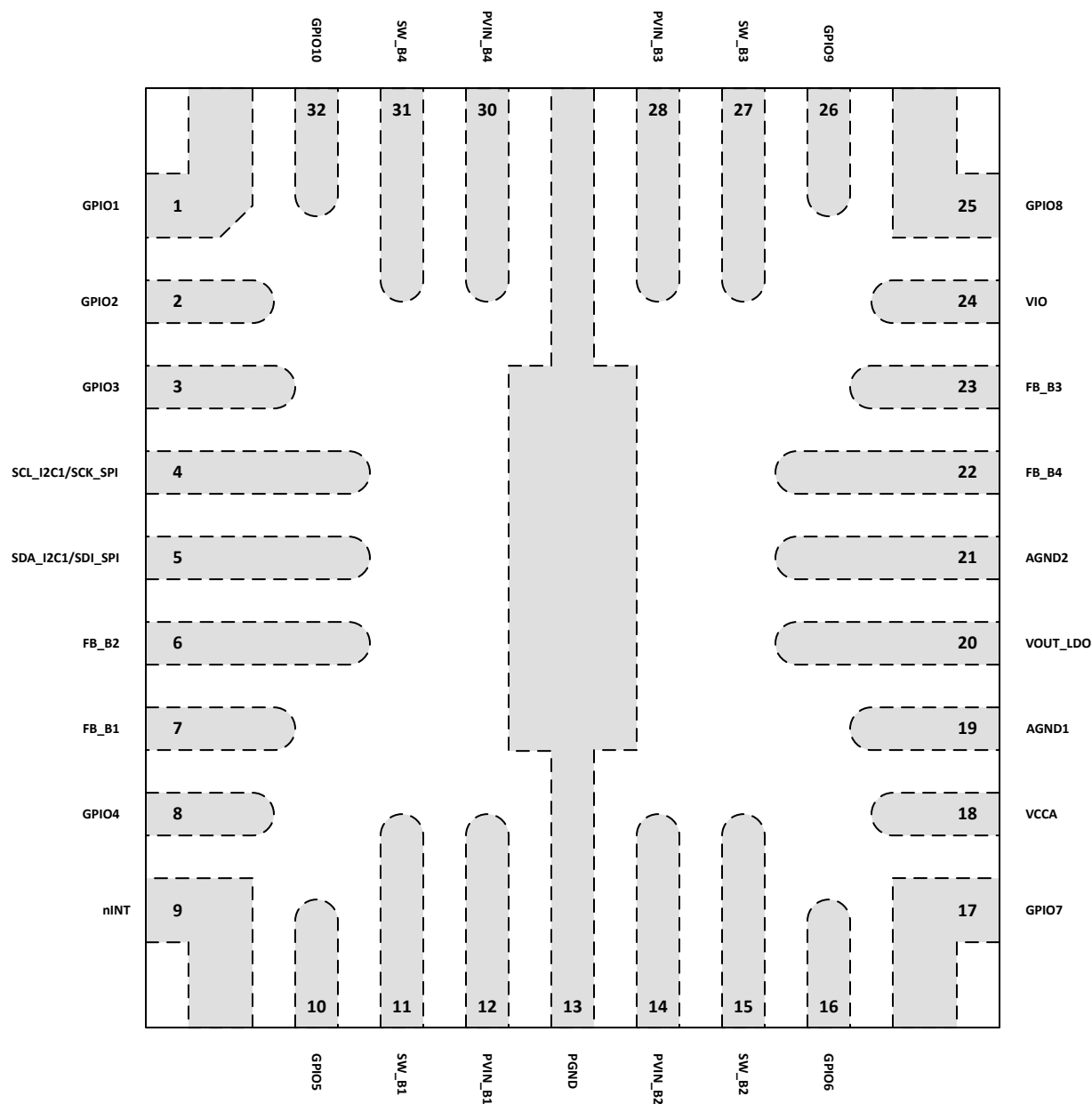


图 5-1. RQK Package 32-Pin VQFN-HR Top View

表 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	GPIO1	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: EN_DRV - Enable Drive output pin to indicate the device entering safe state (set low when ENABLE_DRV bit is '0').	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
2	GPIO2	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SCL_I2C2 - Serial interface clock input for I2C access.	Ground
		I	Digital	Alternative programmable function: CS_SPI - Serial interface Chip Select signal for SPI access.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
3	GPIO3	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDA_I2C2 - Serial interface data input and output for I2C access.	Ground
		O	Digital	Alternative programmable function: SDO_SPI - Serial interface data output signal for SPI access.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
4	SCL_I2C1/ SCK_SPI	I	Digital	If SPI is not used: SCL_I2C1 - Serial interface clock input for I2C access.	Ground
		I	Digital	If SPI is used: SCK_SPI - Serial interface clock input for SPI access.	Ground
5	SDA_I2C1/ SDI_SPI	I/O	Digital	If SPI is not used: SDA_I2C1 - Serial interface data input and output for I2C access.	Ground
		I	Digital	If SPI is used: SDI_SPI - Serial interface data input signal for SPI access.	Ground
6	FB_B2	—	Analog	Output voltage feedback (positive) for BUCK2. Alternatively ground feedback for BUCK1 in multiphase configuration.	Ground
7	FB_B1	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground

表 5-1. Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
8	GPIO4	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: ENABLE - External power-on control.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		—	Analog	Alternative programmable function: BUCK1_VMON - Voltage monitoring input for BUCK1 regulator.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
9	nINT	O	Digital	Open-drain interrupt output, active LOW.	Floating
10	GPIO5	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
11	SW_B1	—	Analog	BUCK1 switch node.	Floating
12	PVIN_B1	—	Power	Power input for BUCK1. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
13	PGND	—	Ground	Power ground for Buck regulators.	Ground
14	PVIN_B2	—	Power	Power input for BUCK2. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
15	SW_B2	—	Analog	BUCK2 switch node.	Floating
16	GPIO6	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

表 5-1. Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
17	GPIO7	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Analog	Alternative programmable function: REFOUT - Buffered bandgap output.	Floating
		I	Analog	Alternative programmable function: VMON1 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
18	VCCA	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bx pins must be connected together in the application and be locally bypassed.	System supply
19	AGND1	—	Ground	Ground	Ground
20	VOUT_LDO	—	Power	LDO regulator filter node. LDO is used for internal purposes.	—
21	AGND2	—	Ground	Ground	Ground
22	FB_B4	—	Analog	Output voltage feedback (positive) for BUCK4. Alternatively ground feedback for BUCK3 in dual phase configuration.	Ground
23	FB_B3	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
24	VIO	—	Power	Supply voltage for selected digital outputs.	Ground
25	GPIO8	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SCLK_SPMI - Multi-PMIC SPMI serial interface clock signal. This pin is an output pin for the master SPMI device, and an input pin for the slave SPMI device.	Ground
		I	Analog	Alternative programmable function: VMON2 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
26	GPIO9	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDATA_SPMI - Multi-PMIC SPMI serial interface bidirectional data signal	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
27	SW_B3	—	Analog	BUCK3 switch node.	Floating
28	PVIN_B3	—	Power	Power input for BUCK3. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply

表 5-1. Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
30	PVIN_B4	—	Power	Power input for BUCK4. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
31	SW_B4	—	Analog	BUCK4 switch node.	Floating
32	GPIO10	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: nRSTOUT - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGNDx ground of the device.
(1)

POS			MIN	MAX	UNIT
M1.1	Voltage on supply input pin	VCCA	−0.3	6	V
M1.2	Voltage on all buck supply voltage input pins	PVIN_Bx	−0.3	6	V
M1.3	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	−0.5	0.5	V
M1.4a	Voltage on all buck switch nodes	SW_Bx pins	−0.3	$V_{PVIN_Bx} + 0.3\text{ V}$, up to 6 V	V
M1.4b	Voltage on all buck switch nodes	SW_Bx pins, 10-ns transient	−2	10	V
M1.5	Voltage on all buck voltage sense nodes	FB_Bx	−0.3	4	V
M1.6	Voltage on all buck power ground pins	PGND	−0.3	0.3	V
M1.7	Voltage on internal LDO output pin	VOUT_LDO	−0.3	2	V
M1.8	Voltage on I/O supply pin	VIO	−0.3	The lower of two: VCCA or 6V	V
M1.9	Voltage on logic pins (input or output)	I ² C and SPI pins, nINT pin, and all GPIO pins	−0.3	6	V
M1.13a	Voltage rise slew-rate on input supply pins	VCCA, PVIN_Bx (voltage below 2.7 V)		60	mV/μs
M1.13b		VIO (only when VCCA < 2 V)		60	
M1.10a	Peak output current	All pins other than power resources		20	mA
M1.10b		Buck regulators: PVIN_Bx, SW_Bx, and PGNDx per phase		5	
M1.10c	Average output current, 100 k hour, T _J = 125°C	GPIOx pins, source current		3	mA
M1.10d		GPIO1/3/5/8/9/10, SDA_I2C1/SDI_SPI and nINT pins, sink current		8	
M1.10e		GPIO2/4/6/7 pins, sink current		3	
M1.10f		Buck regulators		3.5	A
M1.11	Junction temperature, T _J		−45	160	°C
M1.12	Storage temperature, T _{stg}		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

POS				VALUE	UNIT
M1.13	V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
M1.14	V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	V

- (1) AEC Q100-002 indicates that HBM stressing is in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGNDx ground of the device.

POS			MIN	NOM	MAX	UNIT
R1.1	Voltage on supply input pin	VCCA	2.8	3.3	5.5	V
R1.2	Voltage on all buck supply input pins	PVIN_Bx	2.8	3.3	5.5	V
R1.3	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	−0.2		0.2	V
R1.4	Voltage on all buck switch nodes	SW_Bx pins	0		5.5	V
R1.5	Voltage on all buck voltage sense nodes	FB_Bx	0	$V_{OUT(BUCKx)max}$		V
R1.6	Voltage on all buck power ground pins	Between PGND and AGNDx		0		V
R1.7	Voltage on internal LDO output pin	VOUT_LDO	1.65		1.95	V
R1.8a	Voltage on I/O supply pin	$V_{VIO} = 1.8\text{ V}$	1.7	1.8	1.9	V
R1.8b		$V_{VIO} = 3.3\text{ V}$	3.135	3.3	V_{VCCA} , up to 3.465V	
R1.9	Voltage on logic pins (input) ⁽²⁾		0		5.5	
R1.10a	Voltage on logic pins (output, push-pull) in VIO domain ⁽²⁾		0		V_{VIO}	V
R1.10b	Voltage on logic pins (output, push-pull) in LDOVINT domain ⁽²⁾		0		V_{VOUT_LDO}	V
R1.10c	Voltage on logic pins (output, open-drain) ⁽²⁾		0		5.5	
R1.11	Voltage on logic pins (output) in VCCA domain	EN_DRV	0		V_{VCCA}	V
R1.12	Voltage on AGND ground pins	AGND1 and AGND2		0		V
R1.13	Operating free-air temperature ⁽¹⁾		−40	25	125	°C
R1.14	Junction temperature, T_J	Operational	−40	25	150	°C

(1) Additional cooling strategies may be necessary to keep junction temperature at recommended limits.

(2) Internal pull-up resistor is disabled if pin voltage is above V_{VOUT_LDO} (LDOVINT domain pins) or V_{VIO} (VIO domain pins)

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device is a multi-phase step-down converter with four switcher cores, that can be configured to:

- Single output four-phase regulator
- Three-phase and one-phase regulators
- Two-phase and two one-phase regulators
- Four one-phase regulators or
- Two 2-phase regulators

7.1.1 Typical Applications

The five possible configurations are shown in the following figures.

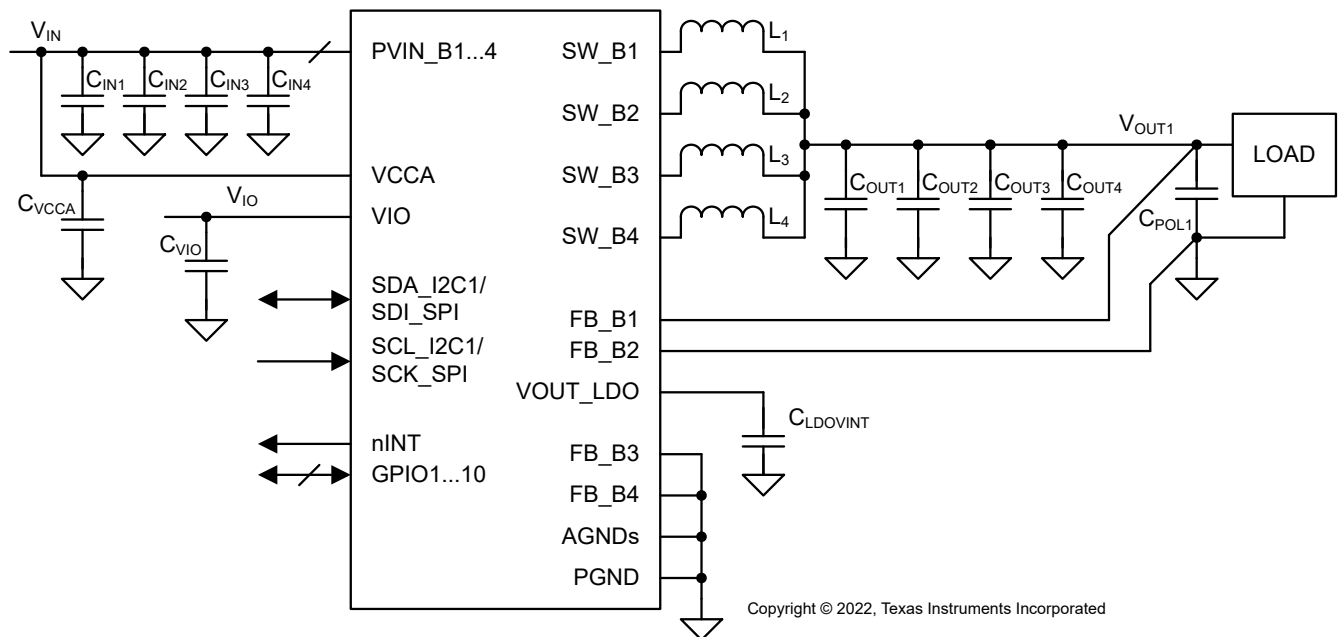


図 7-1. 4-Phase Configuration

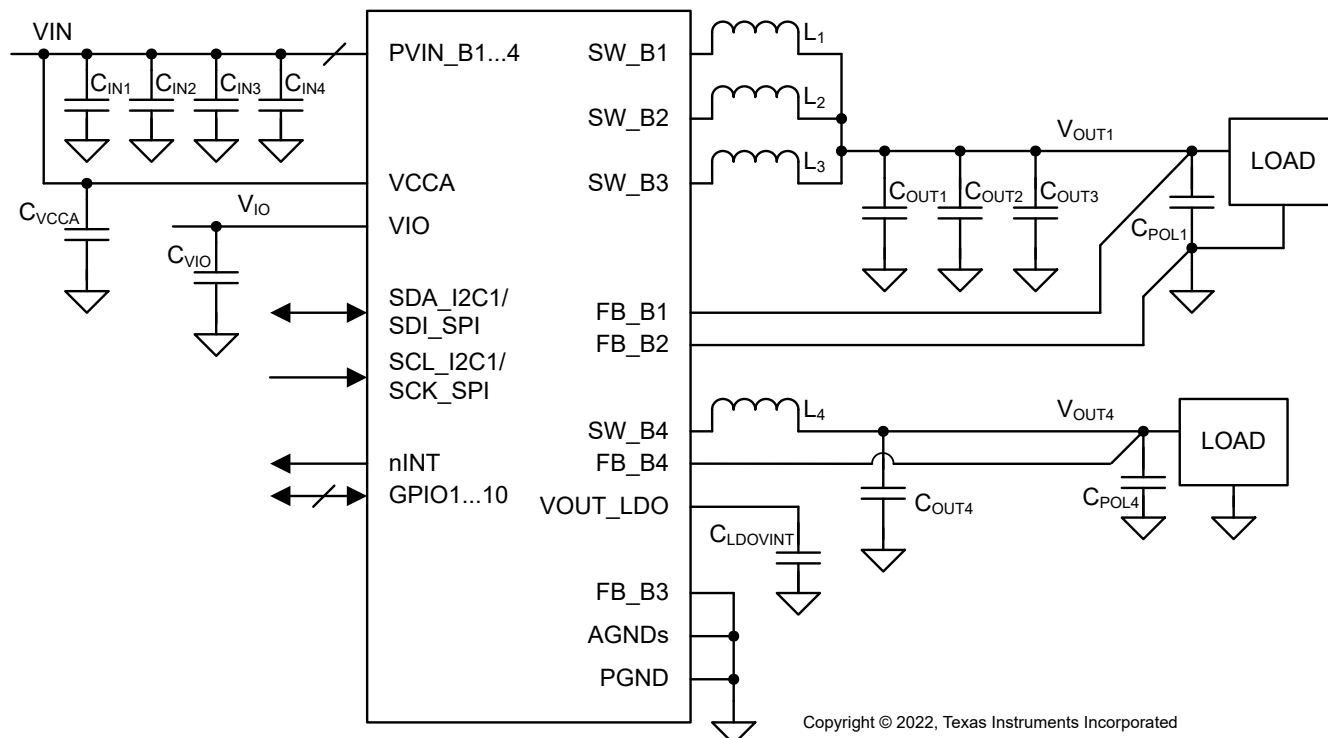


図 7-2. 3-Phase and 1-Phase Configuration

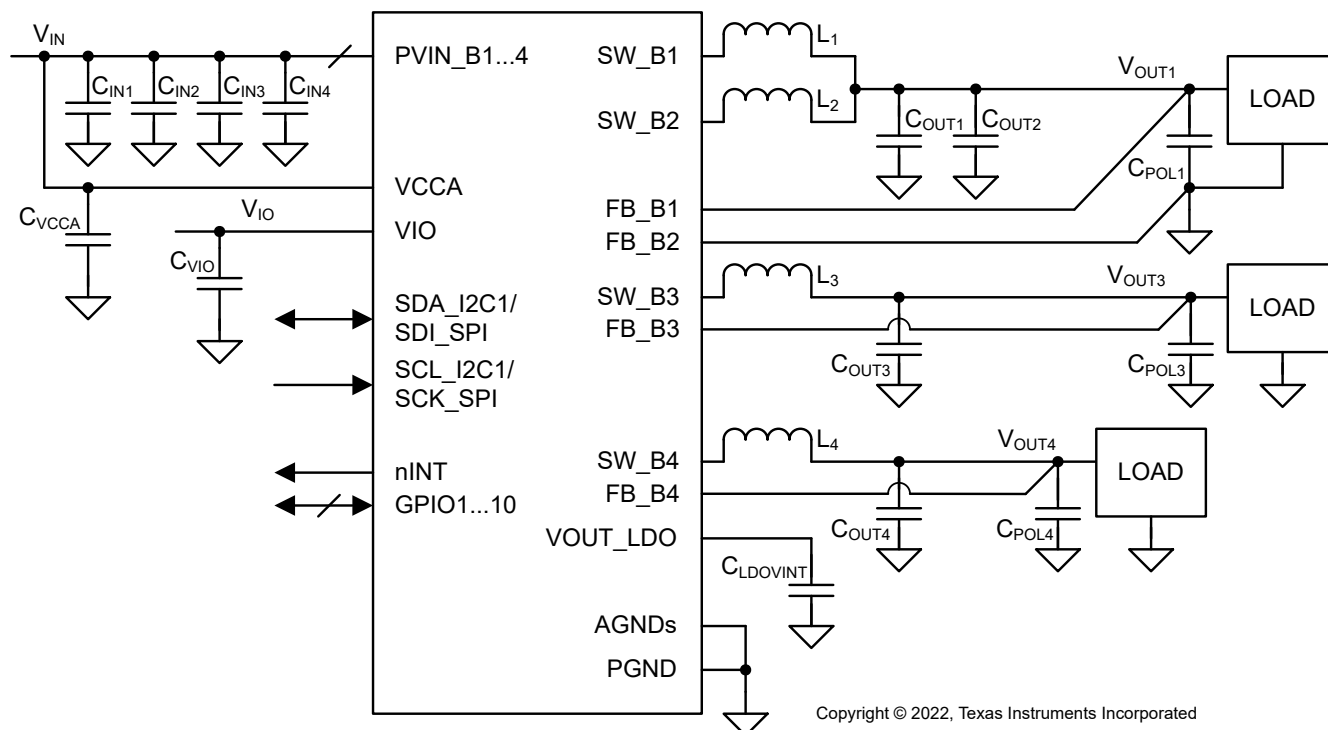


図 7-3. 2-Phase and Dual 1-Phase Configuration

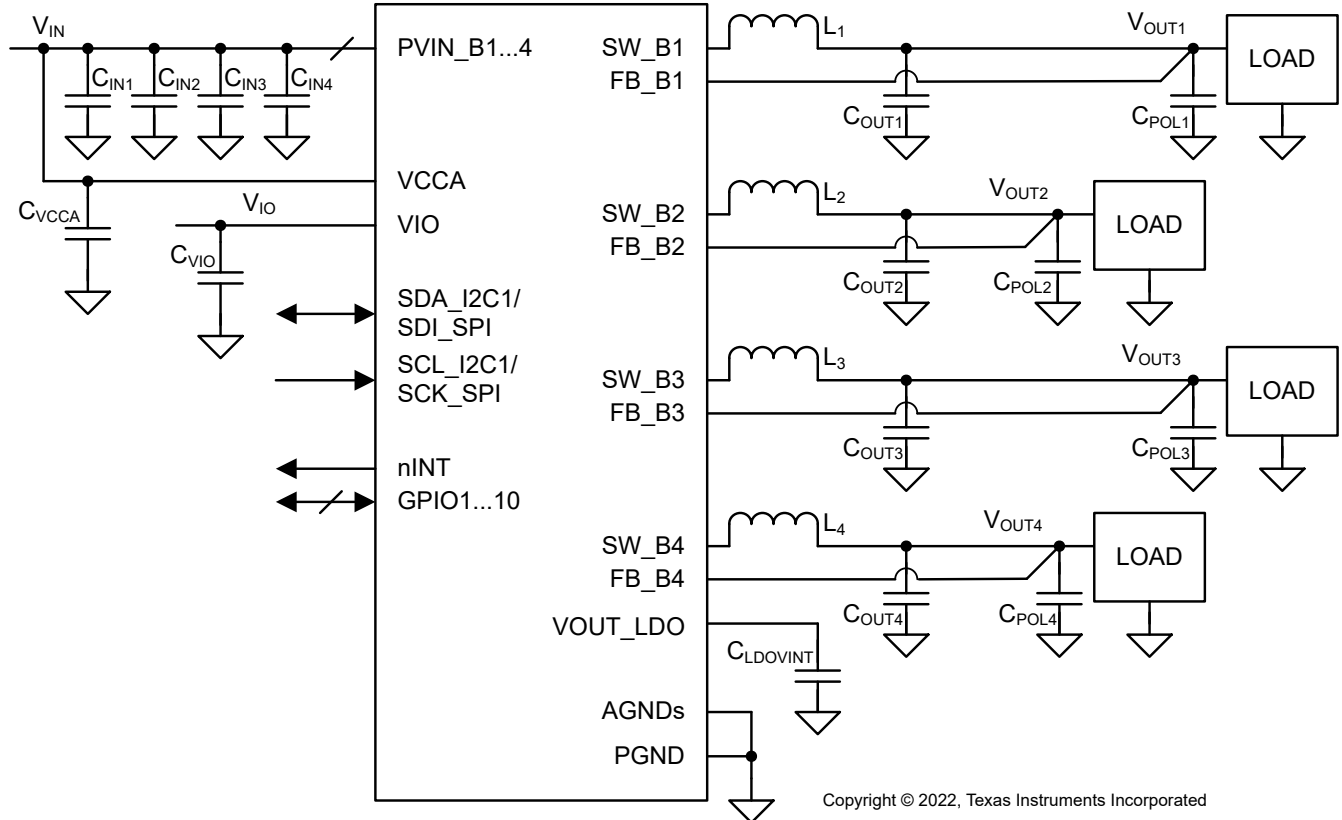


図 7-4. Four 1-Phase configuration

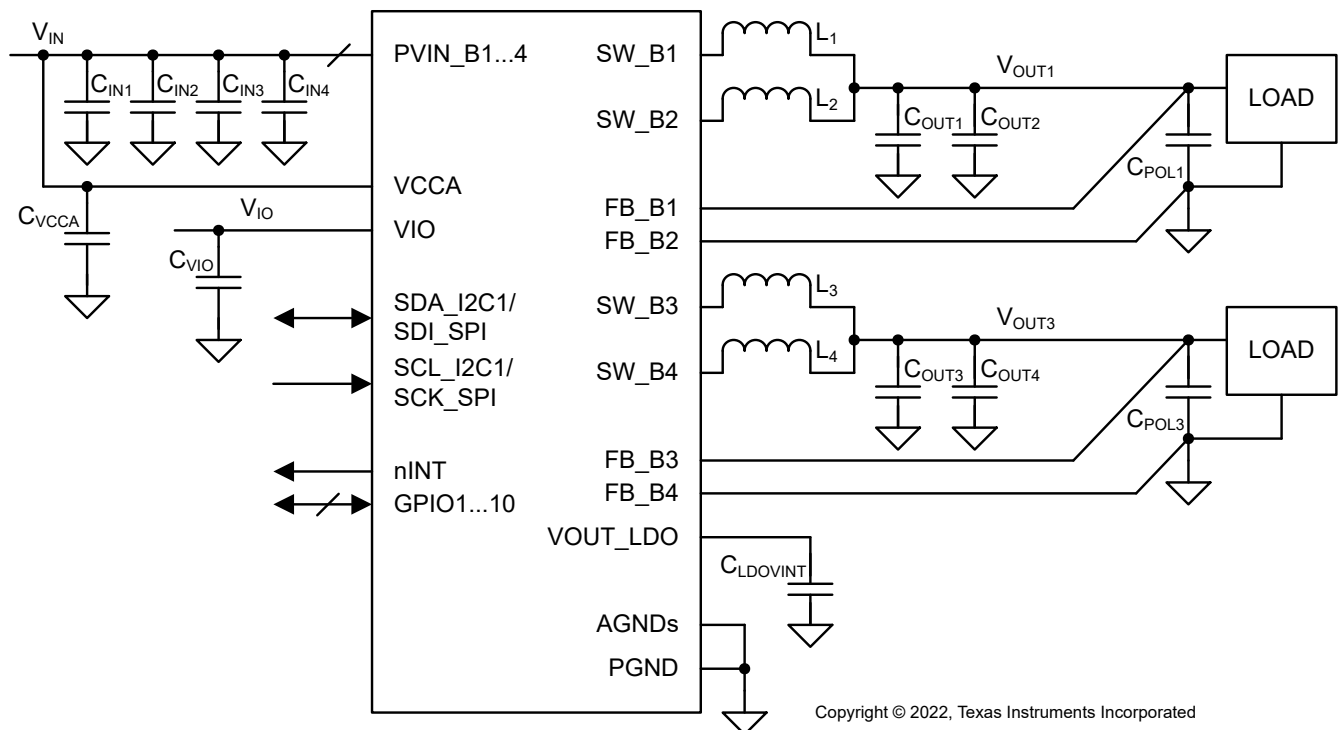


図 7-5. Dual 2-Phase configuration

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2024	*	Initial release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

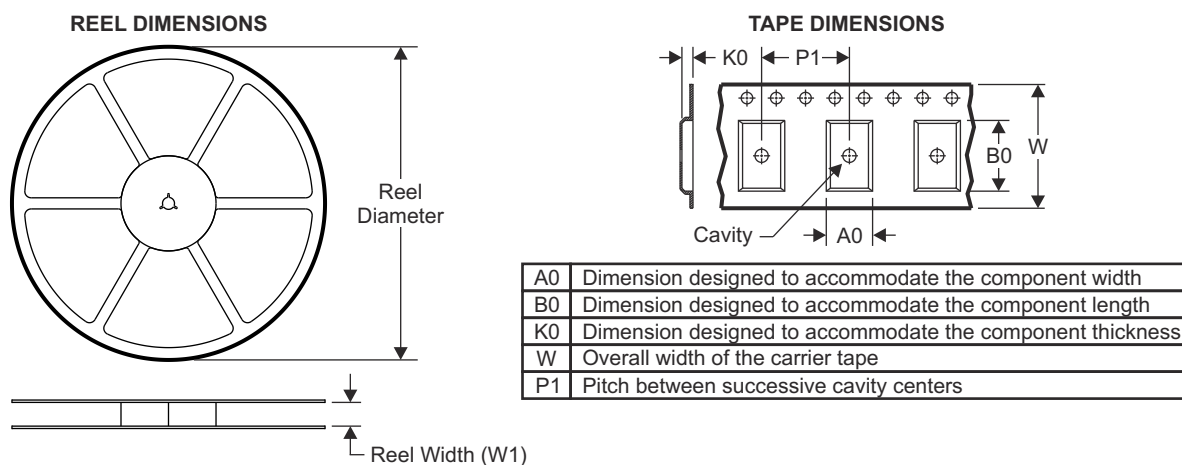
10.1 Packaging Option Addendum

Packaging Information

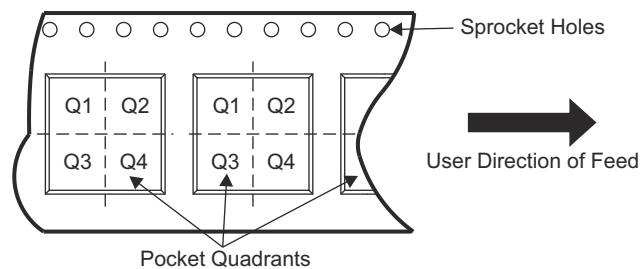
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁴⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(5) (6)}
LP8762PXYYRQKRQ1	ACTIVE	VQFN-HR	RQK	32	3000	RoHS & グリー ン	SN	Level-2-260C-1 YEAR	-40~125	LP8762 PXYY-Q1

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
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10.2 Tape and Reel Information

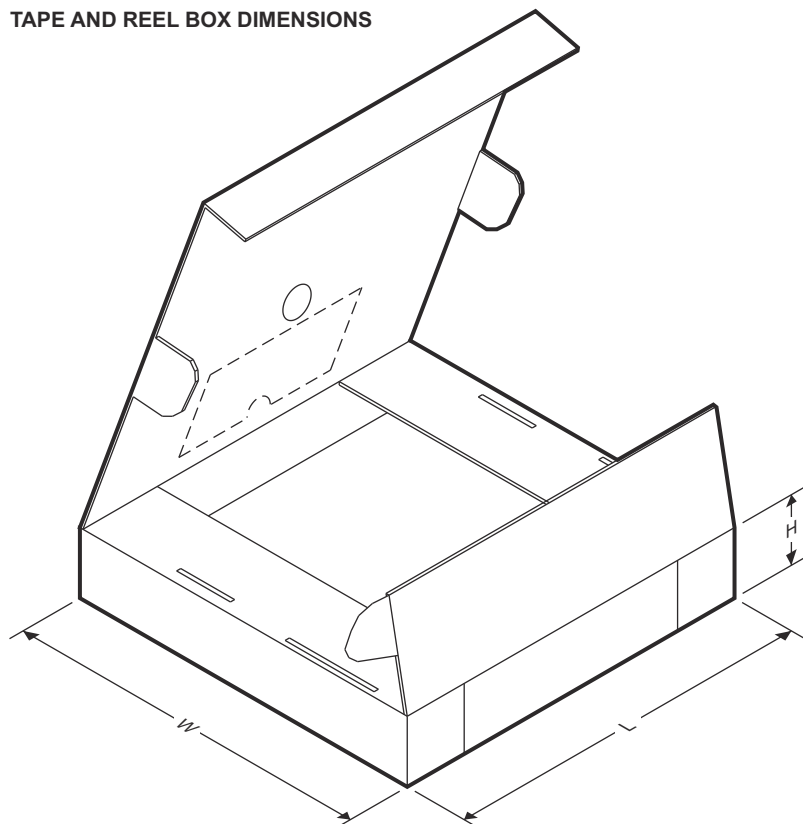


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8762PXYRQKRQ1	VQFN-HR	RQK	32	3000	330.0	12.4	5.25	5.75	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



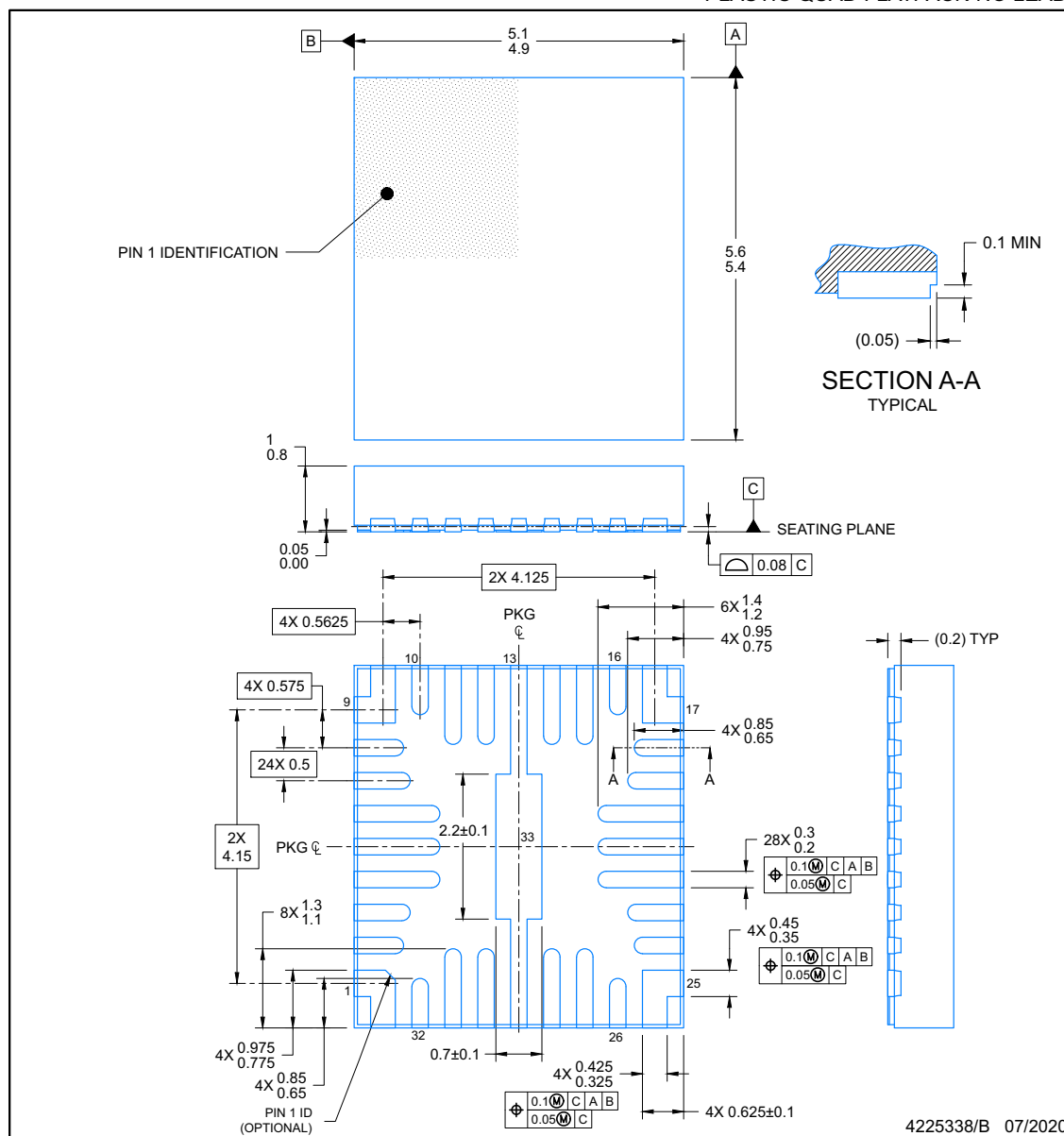
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8762PXYRQKRQ1	VQFN-HR	RQK	32	3000	346.0	346.0	35.0

RQK0032A

PACKAGE OUTLINE

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

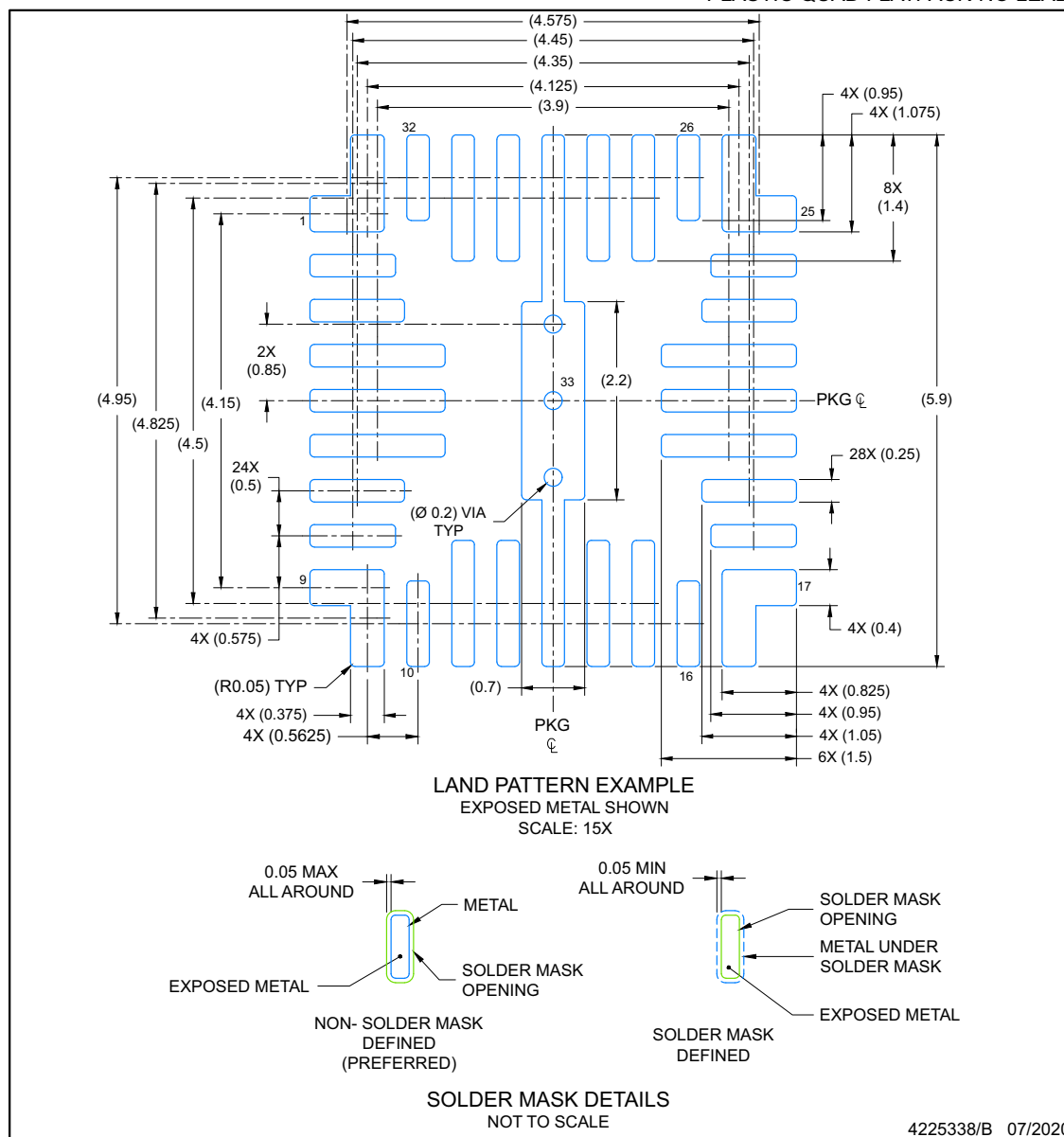
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

VQFN-HR - 1 mm max height

RQK0032A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

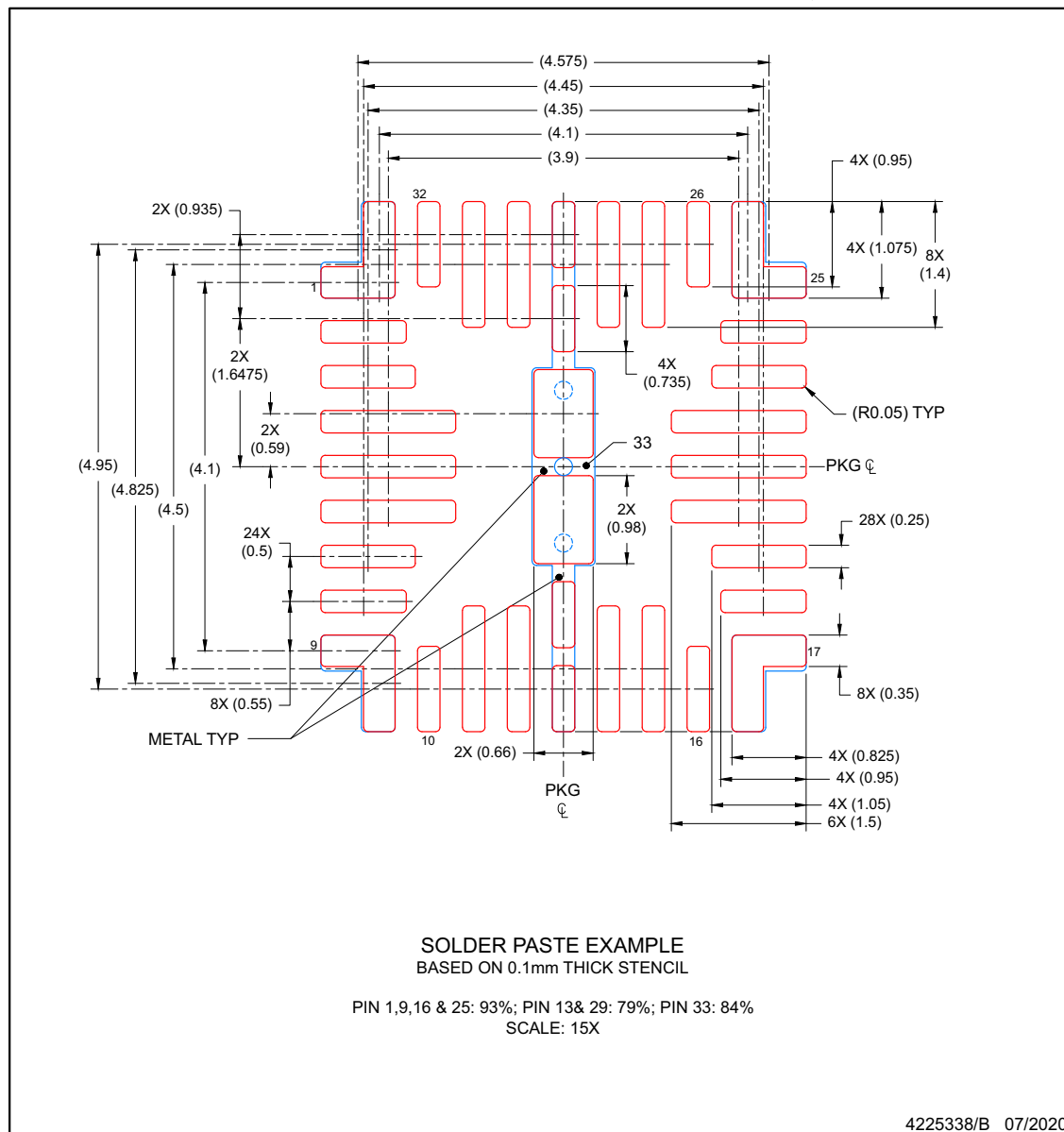
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RQK0032A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

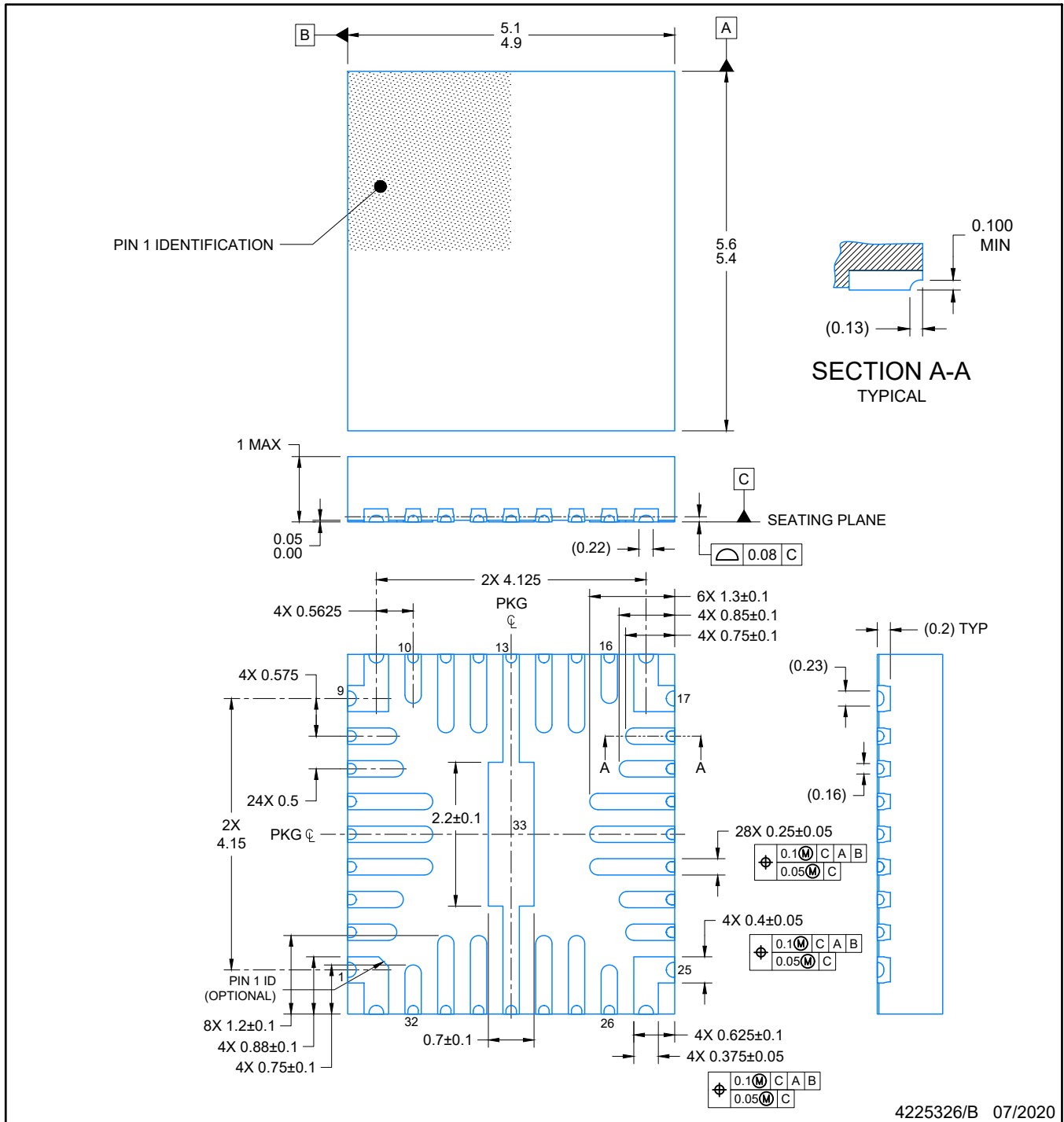
Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP876244C6RQKRQ1	Active	Production	VQFN-HR (RQK) 32	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8762 44C6-Q1
LP876244C6RQKRQ1.A	Active	Production	VQFN-HR (RQK) 32	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8762 44C6-Q1

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

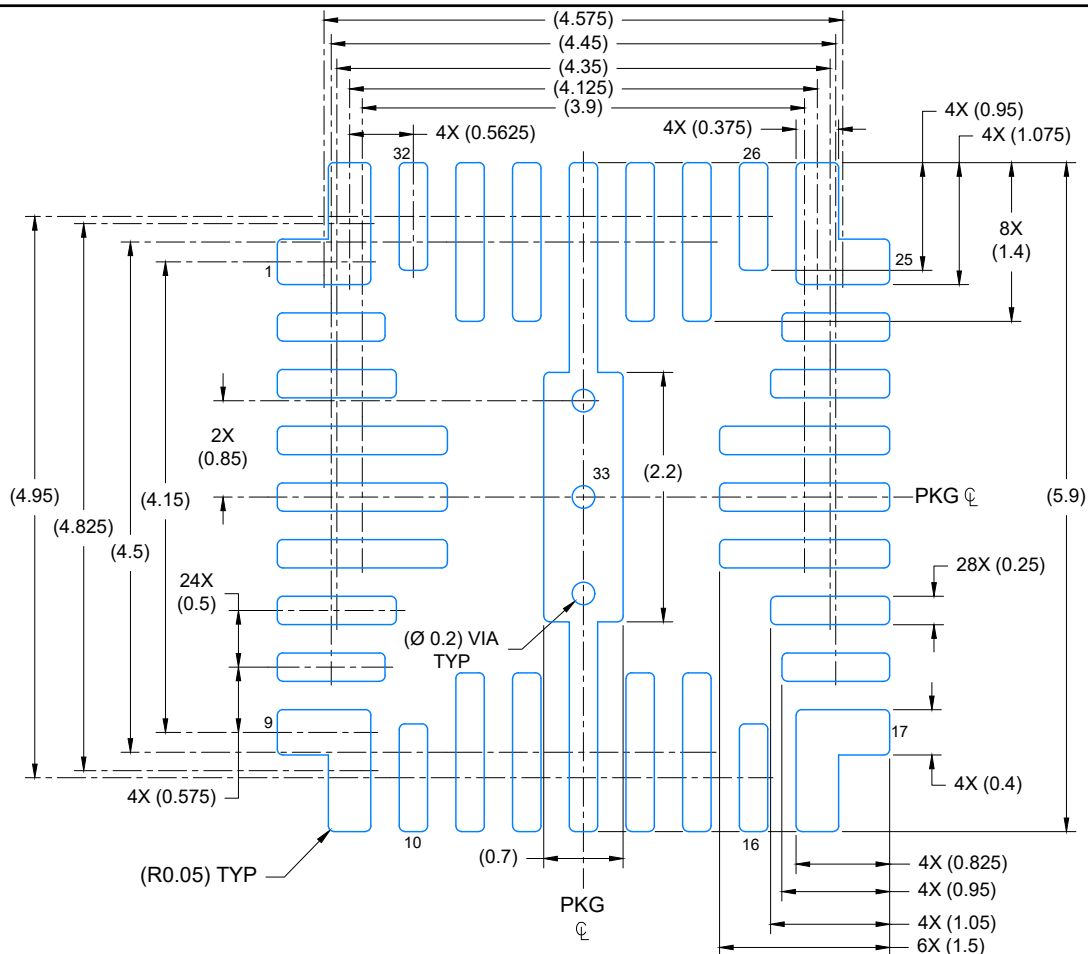
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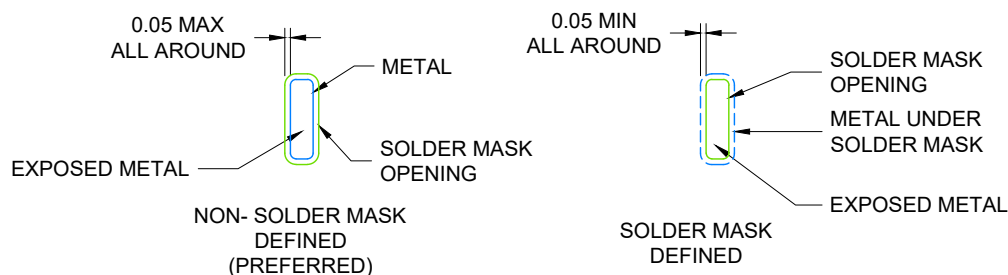


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN
SCALE: 15X

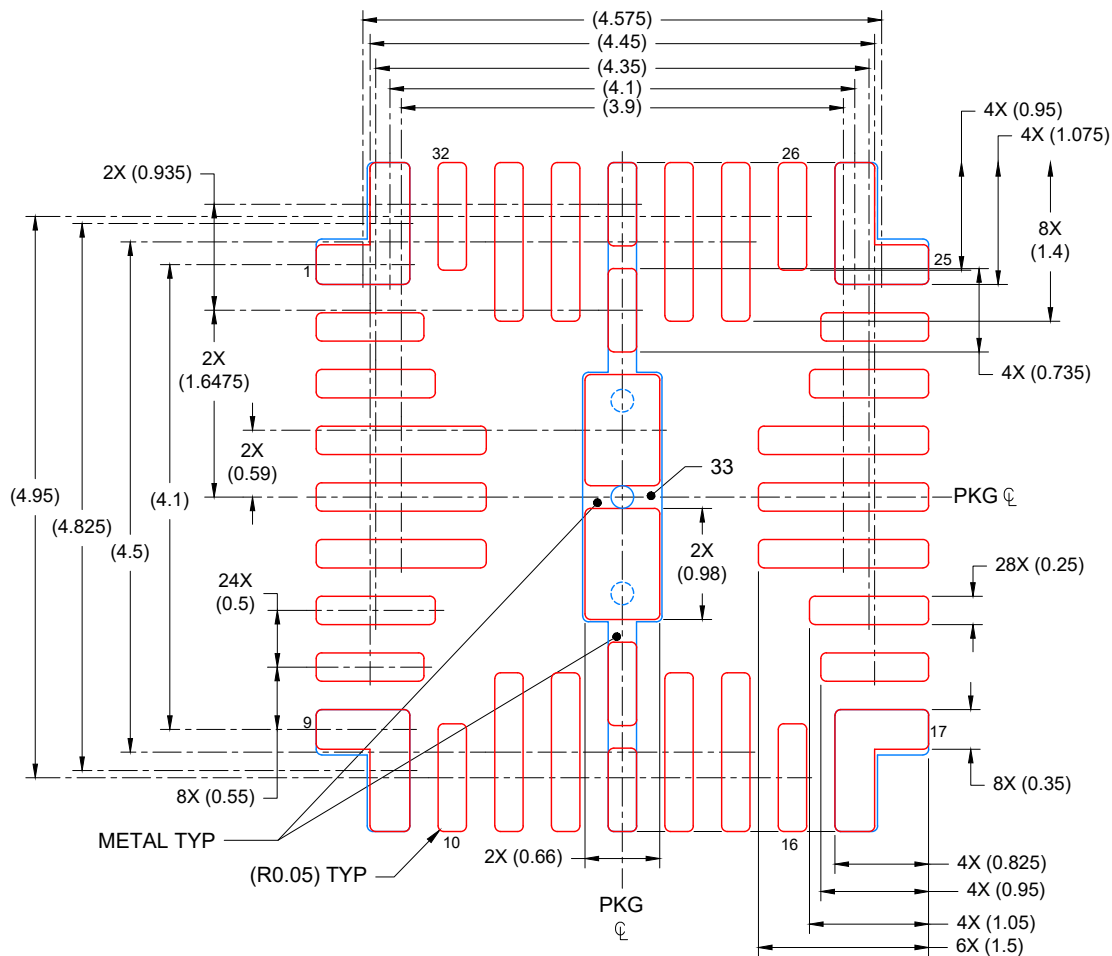
SOLDER MASK DETAILS

NOT TO SCALE

4225326/B 07/2020

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.1mm THICK STENCIL

PIN 1,9,16 & 25: 93%; PIN 13& 29: 79%; PIN 33: 84%
 SCALE: 15X

4225326/B 07/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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