LP5922 2A、低ノイズ可変LDO、低入力/出力電圧機能付き

1 特長

- 広い入力電圧範囲: 1.3V～6V
- 低いV_{IN}電圧、追加バイアス電圧なし
- 出力電圧を0.5V～5Vの範囲で変更可能
- 低ドロップアウト: 2A負荷で200mV
- 低い出力電圧ノイズ: 25µV_{RMS}
- 出力電流: 2A
- 動作時接合部温度: -40℃～+125℃
- プログラム可能なソフトスタートにより突入電流を制限
- 3mm×3mm×0.75mmの10ピンWSONパッケージ
- 熱過負荷および短絡保護
- 出力電圧許容範囲: ±1.5%
- シャットダウン時消費電流: 0.1µA
- PSRR: 1kHz時70dB
- パワー・グッド出力

2 アプリケーション

- 実装面積に制限のあるアプリケーション
- ノイズおよびリップルへの感受性が高い大電流アナログまたはRFシステム
- 対象分野
  - 医療、テスト、計測機器
  - 携帯および消費者電子機器
  - テレコムおよびネットワーク・カード
  - ワイヤレス・インフラストラクチャ
  - 産業用アプリケーション
- 一般的なシステム
  - 無線トランシーバ、電力アンプ、PLL/シンセサイザ、クロック、VCO、GPRS、3Gモジュール、FPGA、DSP、GPU、その他

3 概要

LP5922は2Aの低ドロップアウト(LDO)リニア・レギュレータで、最大電流レベルにおいて標準的なドロップアウト電圧が200mVです。LP5922デバイスは、追加のバイアス電源なしで、電圧レールから最低1.3Vまでの電圧で動作できます。低いドロップアウトと低いV_{IN}能力により、システム効率が最大化、消費電力が最小化されます。低い静止電流と、非常に低いシャットダウン時電流も、このデバイスの特長です。

LP5922デバイスは、高いPSRRと低い出力ノイズを実現し、追加のフィルタリングなしに感受性の高いアナログ・アプリケーションをサポートするよう設計されています。SS/NRピンに小容量のコンデンサを実装すると、出力ノイズをさらに減らすことができます。

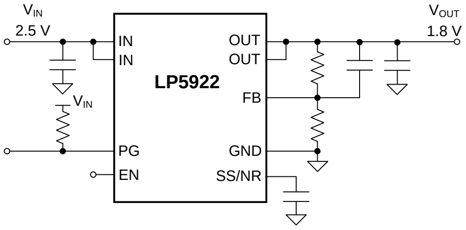
出力電圧は、外付けの分割抵抗によって0.5V～5Vの範囲で調整可能です。イネーブル・ピン、可変ソフトスタート、オプションのパワー・グッド機能は、システムのパワー・シーケンシングに役立ちます。突入電流はソフトスタートによりコントロールされ、デバイスには短絡および熱保護が組み込まれています。

製品情報(1)

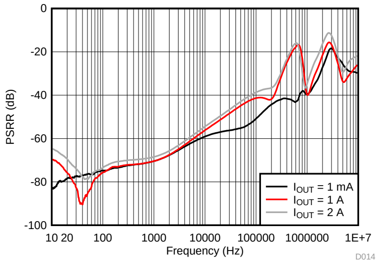
型番	パッケージ	本体サイズ(公称)
LP5922	WSON (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



PSRR



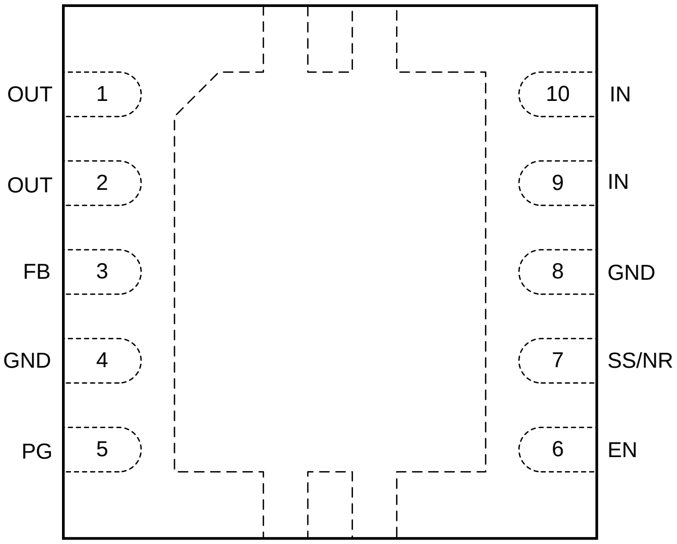
目次

4 改訂履歴

日付	改訂内容	注
2016年11月	*	初版

5 Pin Configuration and Functions

DSC Package
10-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Regulated output voltage, connect directly to pin 2
2	OUT	O	Regulated output voltage, connect directly to pin 1
3	FB	I	Voltage feedback input to the internal error amplifier
4	GND	Ground	Ground; connect to device pin 8.
5	PG	O	Power Good to indicate the status of output voltage. Requires an external pull-up resistor. When PG pin voltage is high the output voltage is considered good.
6	EN	I	Enable
7	SS/NR	I/O	Soft-start and noise reduction pin
8	GND	Ground	Ground —connect to device pin 4.
9	IN	I	Supply voltage input — connect directly to pin 10.
10	IN	I	Supply voltage input —connect directly to pin 9.
Exposed pad	Thermal Pad	—	The exposed thermal pad on the bottom of the package must be connected to a copper area under the package on the PCB. Connect to ground potential. Do not connect to any potential other than the same ground potential seen at device pins 4 and 8 (GND). See *Power Dissipation* for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
IN pin voltage, V_{IN}	–0.3	7	V
OUT pin voltage, V_{OUT}		See(3)	
EN pin voltage, V_{EN}	–0.3	7	V
PG pin voltage, V_{PG}	–0.3	7	V
SS/NR pin voltage, $V_{SS/NR}$	–0.3	3.6	V
FB pin voltage, V_{FB}	–0.3	3.6	V
Junction temperature, T_J		150	°C
Continuous power dissipation(4)	Internally limited		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Absolute maximum V_{OUT} is the lesser of V_{IN} + 0.3 V, or 7 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	1.3		6	V
Output voltage, V_{OUT}	0.5		5	V
FB voltage, V_{FB}		0.5		V
EN input voltage, V_{EN}	0		V_{IN}	V
Recommended load current, I_L	0		2	A
Operating junction temperature, $T_{J\text{-}MAX\text{-}OP}$	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP5922 DSC (WSON) 10 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High K	49.5(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
(3) The PCB for the WSON/DSC package $R_{\theta JA}$ includes four (4) thermal vias, in a 2 × 2 array, under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.3 V, whichever is greater; V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor (unless otherwise noted).(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		1.3		6	V
UVLO	Undervoltage lock-out threshold	V_{IN} Rising (↑) until output is ON		1.2	1.25	V
ΔUVLO	UVLO hysteresis	V_{IN} Falling (↓) from UVLO threshold until output is OFF		160		mV
OUTPUT VOLTAGE AND REGULATION						
V_{OUT}	Output voltage range		0.5		5	V
ΔV_{OUT}	Line regulation	I_{OUT} = 5 mA, 1.3 V ≤ V_{IN} ≤ 6 V		0.02		%/V
	Load regulation	5 mA ≤ I_{OUT} ≤ 2 A		0.1		%/A
V_{DO}	Dropout voltage (4)	V_{IN} = 1.4 V, I_{OUT} = 2 A		220	400	mV
		V_{IN} = 2.5 V, I_{OUT} = 2 A		100	180	
		V_{IN} = 5.3 V, I_{OUT} = 2 A		90	160	
FB						
V_{FB}	FB voltage	I_{OUT} = 5 mA to 2 A	492.5	500	507.5	mV
I_{FB}	FB pin input current	V_{FB} = 0.5 V	–100		100	nA
CURRENT LEVELS						
I_L	Maximum load current	V_{IN} ≥ 1.3 V	2			A
I_{SC}	Short-circuit current limit (5)		2.2	3	3.8	A
I_{GND}	Ground-current minimum load (6)	V_{IN} = 6 V, I_{OUT} = 0 mA		0.7		mA
	Ground-current maximum load (6)	V_{IN} = 1.3 V, I_{OUT} = 2 A		1	4	
$I_{GND(SD)}$	Shutdown current (7)	V_{IN} = 6 V, V_{EN} = 0 V, V_{PG} = 0 V		0.1	15	µA
V_{IN} to V_{OUT} RIPPLE REJECTION (8)						
PSRR	Power-supply rejection ratio	V_{IN} ≥ 1.4 V, ƒ = 1 kHz, I_{OUT} = 2 A		70		dB
		V_{IN} ≥ 1.4 V, ƒ = 10 kHz, I_{OUT} = 2 A		55		
		V_{IN} ≥ 1.4 V, ƒ = 100 kHz, I_{OUT} = 2 A		40		
		V_{IN} ≥ 1.4 V, ƒ = 1 MHz, I_{OUT} = 2 A		30		
OUTPUT NOISE VOLTAGE						
e_N	Noise voltage (8)	V_{IN}= 2.5 V, V_{OUT}= 1.8 V BW = 10 Hz to 100 kHz		25		μV_{RMS}

(1) All voltages are with respect to the GND pin.
(2) Minimum and maximum limits are design targeted limits over the junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(3) C_{IN}, C_{OUT}: Low-ESR surface-mount-ceramic capacitors (MLCCs) used in setting electrical characteristics.
(4) Dropout voltage is the voltage difference between the input and the output at which the FB voltage drops to 97% of its nominal value.
(5) Short-circuit current (I_{SC}) is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(6) Ground current is defined here as the total current flowing to ground as a result of all voltages applied to the device $I_{GND} = ((I_{IN} - I_{OUT}) + I_{EN} + I_{LKG(PG)})$
(7) Ground current in shutdown mode, $I_{GND(SD)}$, does NOT include current from PG pin.
(8) This specification is verified by design.

Electrical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)}$ + 0.5 V or 1.3 V, whichever is greater; V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor (unless otherwise noted).(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT THRESHOLDS						
$V_{IL(EN)}$	EN pin low threshold	V_{EN} falling (↓) until output is OFF			0.35	V
$V_{IH(EN)}$	EN pin high threshold	V_{EN} rising (↑) until output is ON	1.2			V
I_{EN}	Input current at EN pin [9]	V_{IN} = 6 V, V_{EN} = 6 V		3		µA
PG_{HTH}	PG high threshold (% of nominal V_{OUT})	V_{OUT} rising (↑) until PG goes high		94%		
PG_{LTH}	PG low threshold (% of nominal V_{OUT})	V_{OUT} falling (↓) until PG goes low		90%		
$V_{OL(PG)}$	PG pin low-level output voltage	$V_{OUT} < PG_{LTH}$, sink current = 1 mA			400	mV
$I_{LKG(PG)}$	PG pin leakage current	$V_{OUT} > PG_{HTH}$, V_{PG} = 6 V			1	µA
SOFT START						
I_{SS}	SS/NR pin charging current			6.2		µA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
ΔT_{SD}	Thermal shutdown hysteresis			15		°C
TRANSITION CHARACTERISTICS						
ΔV_{OUT}	Line transients	ΔV_{IN} = 0.5 V, V_{OUT} = 2.8 V, $t_{RISE} = t_{FALL}$ = 5 µs		3		mV
	Load transients	V_{OUT} = 3.3 V, I_{OUT} = 10 mA to 2 A to 10 mA $t_{RISE} = t_{FALL}$ = 1 V/µs		25		
R_{AD}	Output discharge pull-down resistance	V_{EN} = 0 V, V_{IN} = 2.3 V		400		Ω

(9) There is a 2-MΩ resistor between EN and ground (pulldown) on the device.

6.6 Input and Output Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance [1]			22		µF
C_{OUT}	Output capacitance	V_{OUT} ≤ 0.8 V	34	47		µF
		V_{OUT} > 0.8 V	15	22		

(1) Typically input capacitance placed close to the device is in the same order as output capacitance. See also *Input Capacitor, C_{IN}*.

6.7 Typical Characteristics

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and T_J = 25°C, unless otherwise stated.

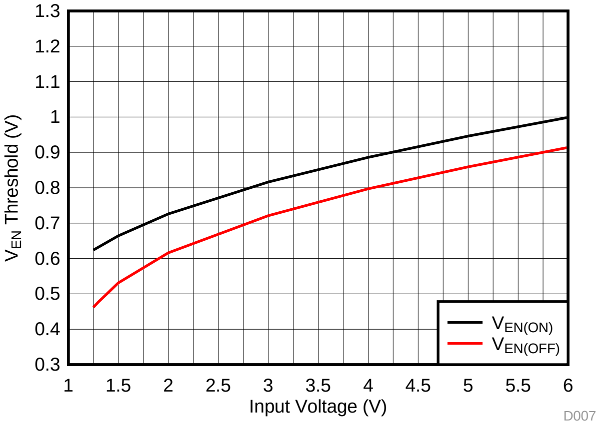


Figure 1. V_{EN} Thresholds vs Input Voltage

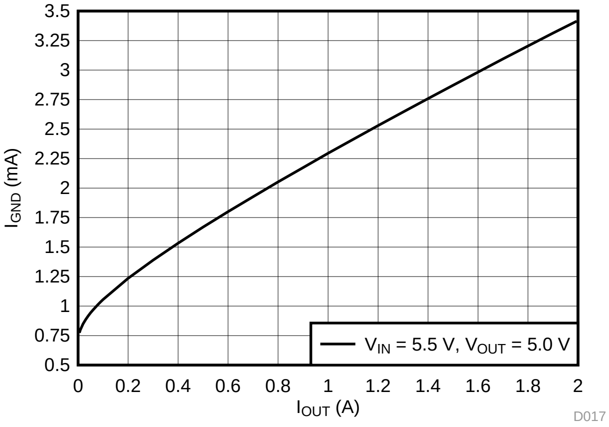
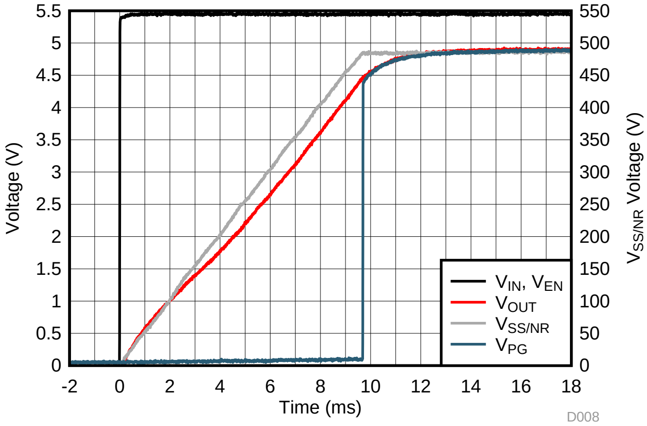
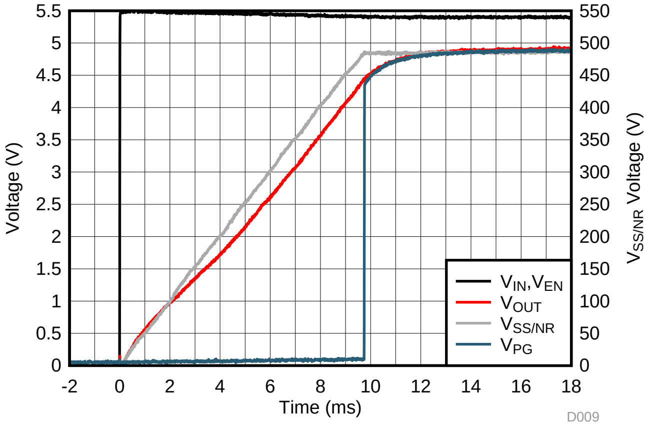


Figure 2. Ground Current vs Output Current



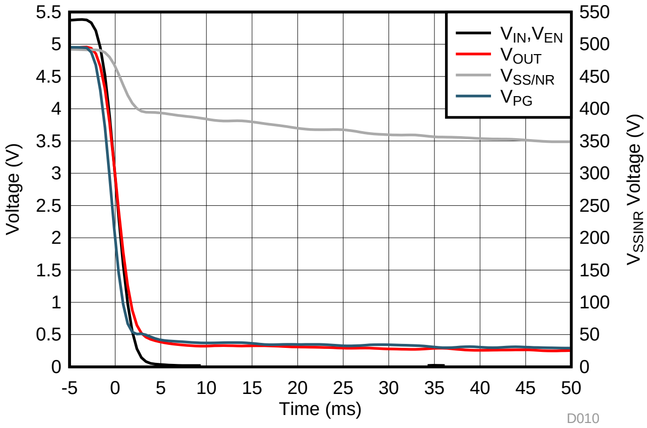
V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 1 mA

Figure 3. Power Up



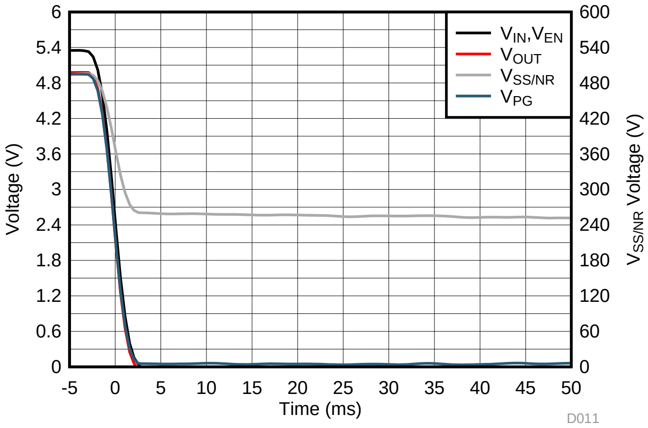
V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 2 A

Figure 4. Power Up



V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 1 mA

Figure 5. Power Down

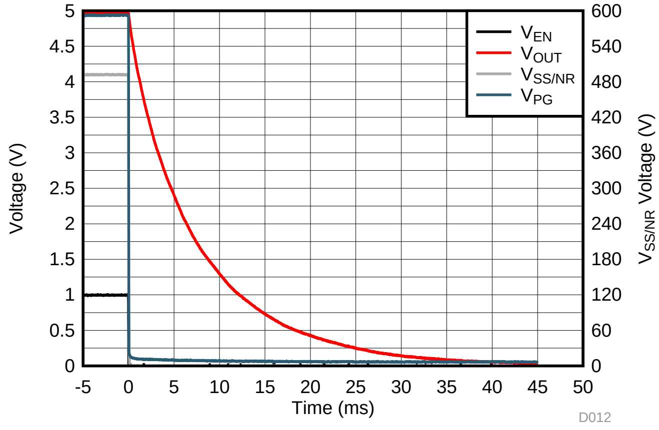


V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 2 A

Figure 6. Power Down

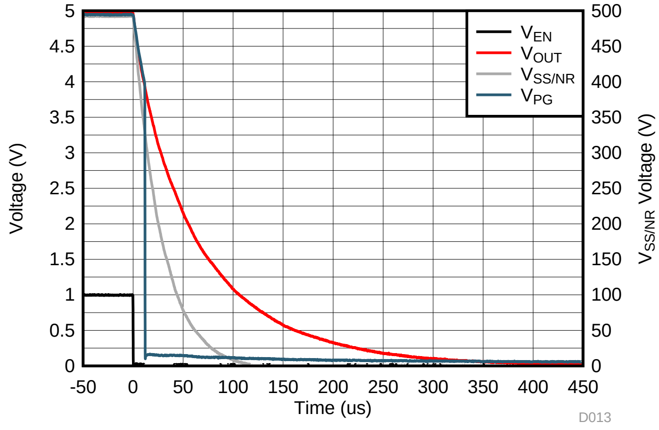
Typical Characteristics (continued)

$V_{IN} = V_{OUT} + 0.5$ V, $V_{EN} = 1.2$ V, $C_{IN} = 22$ µF, $C_{OUT} = 22$ µF, OUT connected to 50 Ω to GND, $V_{FB} = 0.5$ V, $C_{SS/NR} = 0.12$ µF, $C_{FF} = 0.01$ µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and $T_J = 25$°C, unless otherwise stated.



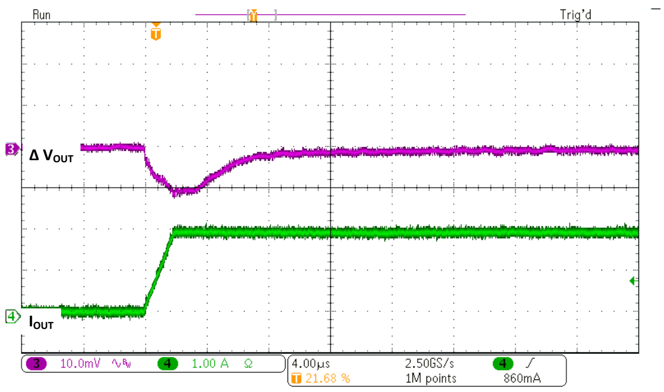
$V_{OUT} = 5$ V $I_{OUT} = 1$ mA

Figure 7. Power Down



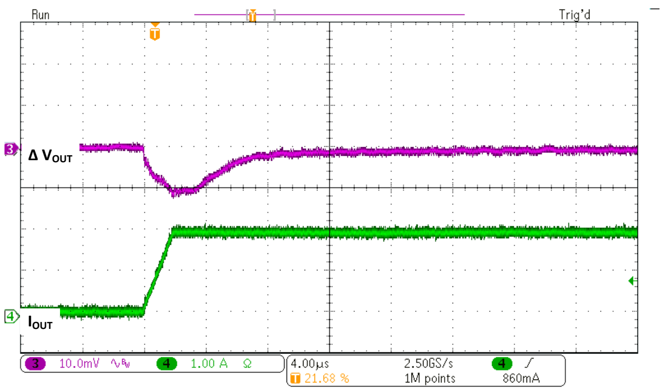
$V_{OUT} = 5$ V $I_{OUT} = 2$ A

Figure 8. Power Down



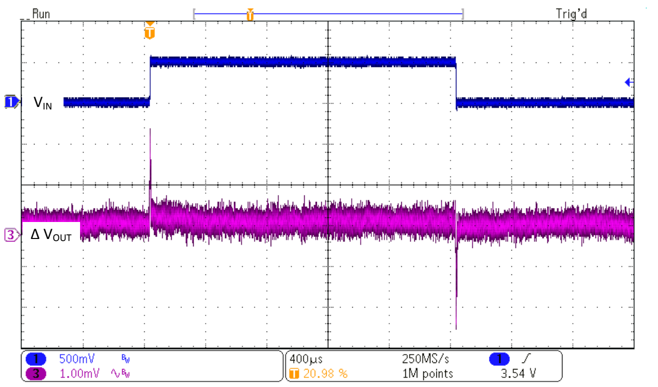
$V_{OUT} = 2.8$ V $I_{OUT} = 10$ mA to 2 A $t_{rise} = 1$ V/µs

Figure 9. Load Transient Response



$V_{OUT} = 2.8$ V $I_{OUT} = 2$ A to 10 mA $t_{fall} = 1$ V/µs

Figure 10. Load Transient Response



$V_{OUT} = 2.8$ V V_{IN} 3.3 V to 3.8V to 3.3 V $t_{fall} = 1$ V/µs

Figure 11. Line Transient Response

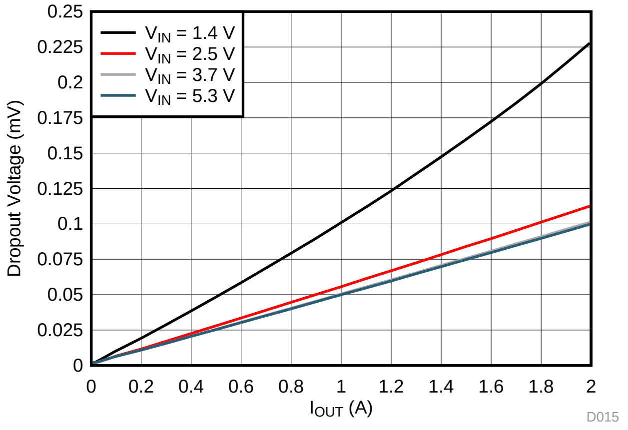
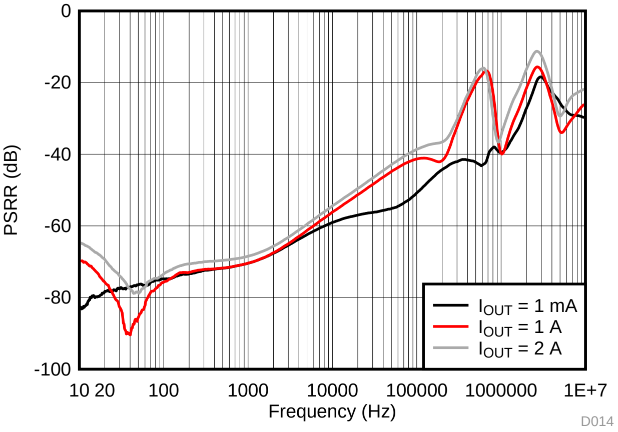


Figure 12. Dropout Voltage (V_{DO}) vs Load Current

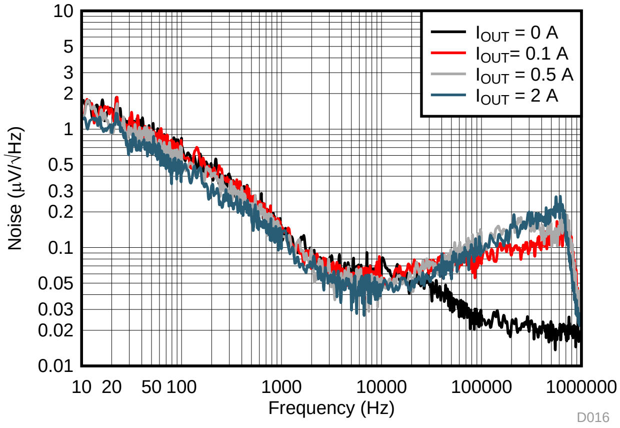
Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and T_J = 25°C, unless otherwise stated.



V_{IN} = 5.5 V V_{OUT} = 5 V

Figure 13. PSRR vs Frequency



V_{IN} = 2.5 V V_{OUT} = 1.8 V

Figure 14. Noise Density vs Frequency

7 Detailed Description

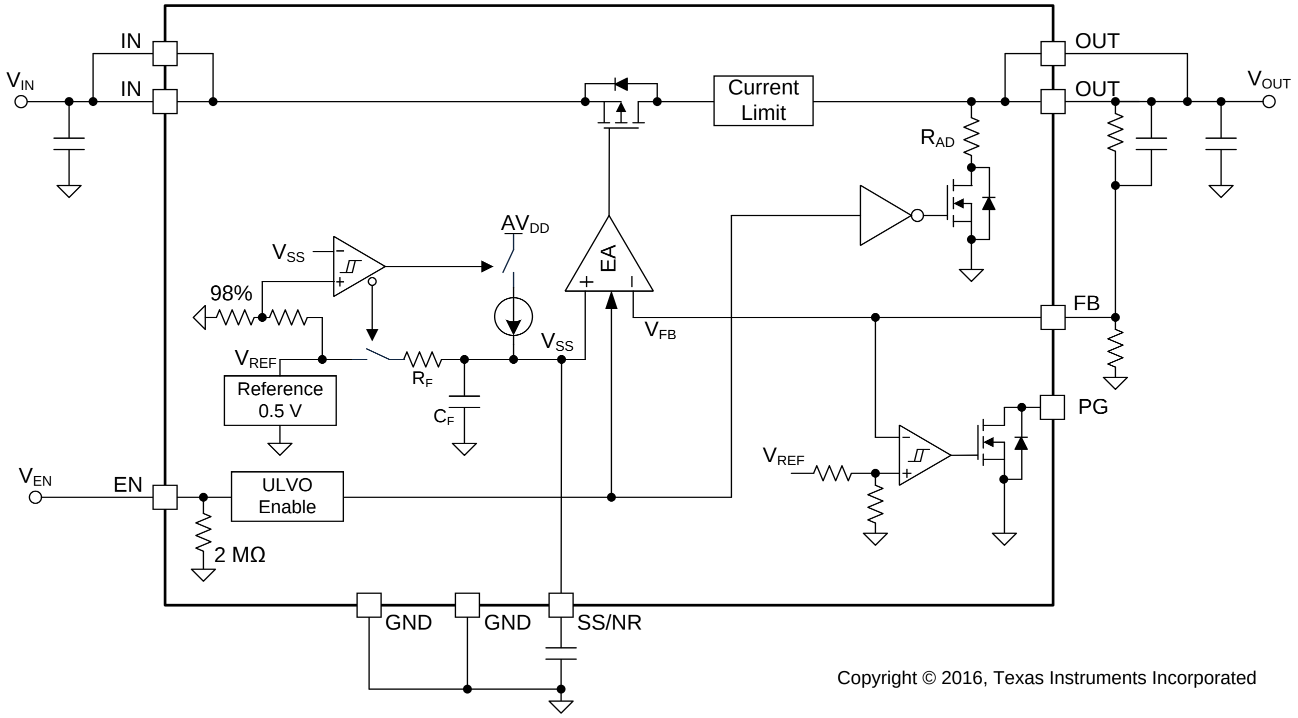
7.1 Overview

The LP5922 is a low-noise, high PSRR, low-dropout regulator capable of sourcing a 2-A load. The LP5922 can operate down to 1.3-V input voltage and 0.5-V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout (LDO) regulator to power a multitude of loads from noise-sensitive communication components to battery-powered system.

The LP5922 block diagram contains several features, including:

- Low-noise, 0.5-V reference
- Internal protection circuit, such as current limit and thermal shutdown
- Programmable soft-start circuit
- Power Good output

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage

The LP5922 output voltage can be set to any value from 0.5 V to 5 V using two external resistors shown as R_{UPPER} and R_{LOWER} in Figure 15. The value for the R_{LOWER} should be less than or equal to 100 kΩ for good loop compensation. R_{UPPER} can be selected for a given V_{OUT} using Equation 1:

$$R_{UPPER} = \frac{(V_{OUT} - V_{FB}) \times R_{LOWER}}{V_{FB}}$$

where

- $V_{FB} = 0.5$ V (1)

Feature Description (continued)

7.3.2 Enable

The LP5922 EN pin is internally held low by a 2-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the VIL threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.3 Output Automatic Discharge

The LP5922 output employs an internal 400-Ω (typical) pulldown resistance to discharge the output capacitor when the EN pin is low, and the device is disabled.

7.3.4 Programmable Soft Start and Noise Reduction

The output voltage of LP5922 ramps up linearly in a constant slew rate until reaching the target regulating voltage after a stable V_{IN} (greater than V_{OUT} + V_{DO}) is supplied and EN pin is pulled high. The slew rate of V_{OUT} ramping is programmable by an external capacitor on the SS/NR pin; therefore, the duration for soft-start period is programmable as well. Once the LP5922 is enabled, the SS/NR pin sources a constant 6-µA current to charge the external $C_{SS/NR}$ capacitor until the voltage at the SS/NR pin reaches 98% of the internal reference voltage (V_{REF}) of 500 mV typical. The final 2% of $C_{SS/NR}$ charge is determined by a RC time constant. During the soft-start period, the current flowing into the IN pin primarily consists of the sum of the load current at the LDO output and the charging current into the output capacitor. The soft-start period can be calculated by Equation 2:

$$t_{SS} = \frac{C_{SS/NR} \times V_{FB}}{I_{SS}}$$

where

- V_{FB} = 0.5 V - this is the voltage that $C_{SS/NR}$ charges to;
- $C_{SS/NR}$ is the value of the capacitor connected between the SS/NR pin and ground; and
- I_{SS} = 6.2 µA is the typical charging current to the SS/NR pin during start-up period. (2)

The recommended value for $C_{SS/NR}$ is 100 nF or larger. Equation 2 is most accurate for these values. The $C_{SS/NR}$ capacitor is also the filter capacitor for internal reference for noise reduction purpose. An integrated resistor and the $C_{SS/NR}$ capacitor structure a RC low-pass filter to remove the noise on the internal reference voltage.

7.3.5 Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

7.3.6 Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to T_{SD} level, which allows the device to cool. When the junction temperature cools by ΔT_{SD}, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the LP5922 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the LP5922 into thermal shutdown degrades device reliability.

Feature Description (continued)

7.3.7 Power Good Output

The LP5922 has a Power-Good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages (low impedance to GND). When the output voltage rises above the PG threshold voltage (PG_{HTH}), the PG pin becomes high-impedance. By connecting a pullup resistor to an external supply, any downstream device can receive PG as a logic signal. User must make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices; use a pullup resistor from 10 kΩ to 100 kΩ for best results.

In Power-Good function, the PG output pin pulled high immediatelly after output voltage rises above the PG threshold voltage.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5922 enable (EN) pin is internally held low by a 2-MΩ resistor to GND. If the EN pin is open the output is OFF. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuit is activated. Any charge on the OUT pin is discharged to GND through the internal pulldown resistance.

7.4.2 Undervoltage Lockout (UVLO)

The LP5922 incorporates UVLO. The UVLO circuit monitors the input voltage and keeps the LP5922 disabled while a rising V_{IN} is less than 1.2 V (typical). The rising UVLO threshold is approximately 100 mV below the recommended minimum operating V_{IN} of 1.3 V.

7.4.3 Minimum Operating Input Voltage

The LP5922 internal circuit is not fully functional until V_{IN} is at least 1.3 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.3 V or (V_{OUT} + V_{DO}).

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5922 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 22 µF. The LP5922 delivers this performance in an industry-standard WSON package which, for this device, is specified with an operating junction temperature (T_J) of –40°C to +125°C.

8.2 Typical Application

Figure 15 shows the typical application circuit for the LP5922. Input and output capacitances may need to be increased above 22 µF minimum for some applications.

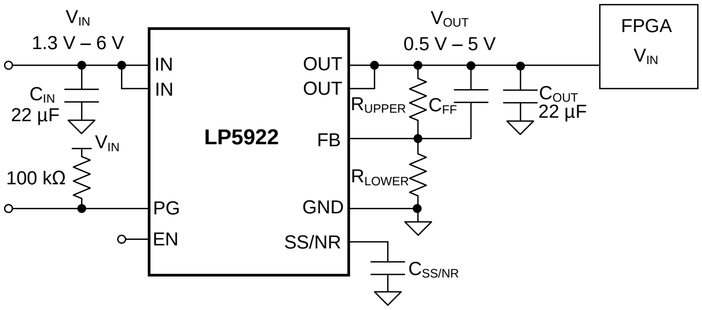


Figure 15. LP5922 Typical Application

8.2.1 Design Requirements

For typical LP5922 applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25 V to 2.75 V
Output voltage	1.8 V
Output current	2000 mA
Output capacitor range	22 µF to 47 µF
Output capacitor ESR range	2 mΩ to 500 mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The LP5922 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and the noise-reduction pin (SS/NR). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance. Additionally, the case size has a direct impact on the capacitance versus applied voltage derating.

Regardless of the ceramic capacitor type selected, the actual capacitance varies with the applied operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a effective capacitance derating of approximately 50%, but at high applied voltage conditions the capacitance derating can be greater than 50% and must be taken into consideration. The minimum capacitance values declared in *Input and Output Capacitors* must be met across the entire expected operating voltage range and temperature range.

8.2.2.2 Input Capacitor, C_{IN}

An input capacitor is required for stability. A capacitor with a value of at least 22 μF must be connected between the LP5922 IN pin and ground for stable operation over full load current range. It is acceptable to have more output capacitance than input, as long as the input is at least 22 μF.

The input capacitor must be located as close as possible to, but at a distance not more than 1 cm from, the IN pin and returned to the device GND pin with a clean analog ground. This will minimize the trace inductance between the capacitor and the device. Any good quality ceramic or tantalum capacitor may be used at the input.

8.2.2.3 Output Capacitor, C_{OUT}

The LP5922 is designed to work specifically with a low ESR ceramic (MLCC) output capacitor, typically 22 μF. A ceramic capacitor (dielectric types X5R or X7R) in the 22-μF to 100-μF range, with an ESR not exceeding 500 mΩ, is suitable in the LP5922 application circuit having an output voltage greater than 0.8 V. For output voltages of 0.8 V or less, the output capacitance must be increased to typically 47 μF. The output capacitor must be connected between the device OUT and GND pins. The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that does not exceed 500 mΩ to ensure stability.

It is possible to use tantalum capacitors at the device output, but these are not as attractive for reasons of size, cost, and performance.

A combination of multiple output capacitors in parallel boosts the high-frequency PSRR. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating optimizes PSRR response in the frequency range of 400 kHz to 700 kHz (which is a typical range for dc-dc supply switching frequency). This 47-µF || 10-µF || 10-µF combination also ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 75% at 5 V, so the addition of the two 10-µF capacitors ensures that the capacitance is at or above 22 µF.

8.2.2.4 Soft-Start and Noise-Reduction Capacitor, $C_{SS/NR}$

Recommended value for $C_{SS/NR}$ is 100 nF or larger. The soft-start period can be calculated by Equation 2. The $C_{SS/NR}$ capacitor is also the filter capacitor for internal reference for noise reduction purpose.

8.2.2.5 Feed-Forward Capacitor, C_{FF}

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external C_{FF} optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} value can be used; however, the start-up time may be longer and the Power-Good signal may incorrectly indicate that the output voltage is settled. The maximum recommended value is 100 nF

To ensure proper PGx functionality, the time constant defined by CNR/SSx must be greater than or equal to the time constant from CFFx. For a detailed description, see the application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* (SBVA042).

8.2.2.6 No-Load Stability

The LP5922 remains stable, and in regulation, with no external load.

8.2.2.7 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the exposed thermal pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 3.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \tag{3}$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DSC) package, the primary conduction path for heat is through the exposed thermal pad into the PCB. To ensure the device does not overheat, connect the exposed thermal pad, through multiple thermal vias, to an internal ground plane with an appropriate amount of PCB copper area.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 4 or Equation 5:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \tag{4}$$

$$P_D = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \tag{5}$$

If the V_{IN}-V_{OUT} voltage is known, the maximum allowable output current can be calculated with Equation 6

$$I_{OUT(MAX)} = (((125°C - T_A) / R_{\theta JA}) / (V_{IN} - V_{OUT})) \tag{6}$$

Unfortunately, the $R_{\theta JA}$ value is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the PCB size, total copper area, copper weight, any thermal vias, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper spreading area, and is to be used only as a relative measure of package thermal performance. For a well designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.8 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 7 and Equation 8.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- T_{TOP} is the temperature measured at the center-top of the device package.
- $P_{D(MAX)}$ is described at Equation 3 (7)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.
- $P_{D(MAX)}$ is described at Equation 3 (8)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* ; for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* ; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the *TI Application Report Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.

8.2.2.9 Recommended Continuous Operating Area

The continuous operational area of an LDO is limited by the input voltage (V_{IN}), the output voltage (V_{OUT}), the dropout voltage (V_{DO}), the output current (I_{OUT}), and the junction temperature (T_J). The recommended area for continuous operation for a linear regulator can be separated into the following steps, and is shown in Figure 16.

- Limited by dropout: Dropout voltage limits the minimum differential voltage between the input and the output (V_{IN} – V_{OUT}) at a given output current level.
- Limited by the rated output current: The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- Limited by thermals: This portion of the boundary is defined by Equation 6. The slope is nonlinear because the junction temperature of the LDO is controlled by the power dissipation (P_D) across the LDO; therefore, when V_{IN} – V_{OUT} increases, the output current must decrease in order to ensure that the rated maximum operating junction temperature of the device is not exceeded. Exceeding the maximum operating junction temperature rating can cause the device to fall out of specifications, reduces long-term reliability, and may activate the thermal shutdown protection circuitry.
- Limited by V_{IN} range: The rated operating input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

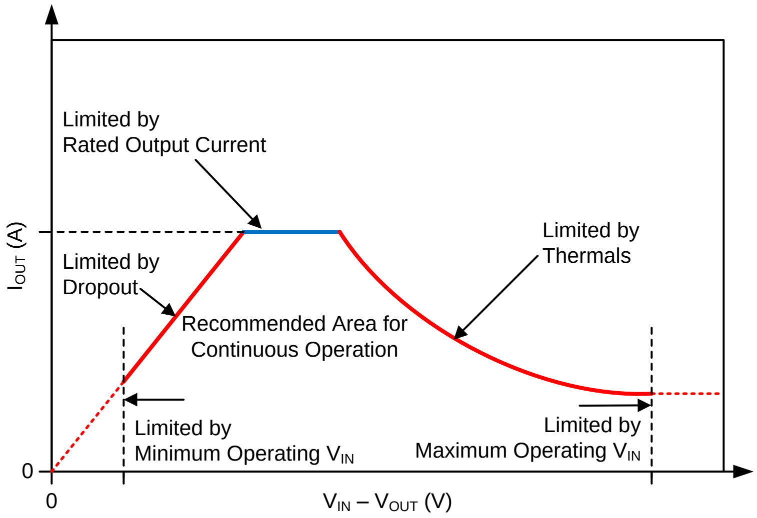


Figure 16. Recommended Continuous Operating Area

Figure 17 to Figure 22 show the recommended continuous operating area boundaries for this device in the WSON (DSC) package mounted to a EIA/JEDEC High-K printed circuit board, as defined by JESD51-7, with an $R_{\theta JA}$ rating of 49.5°C/W.

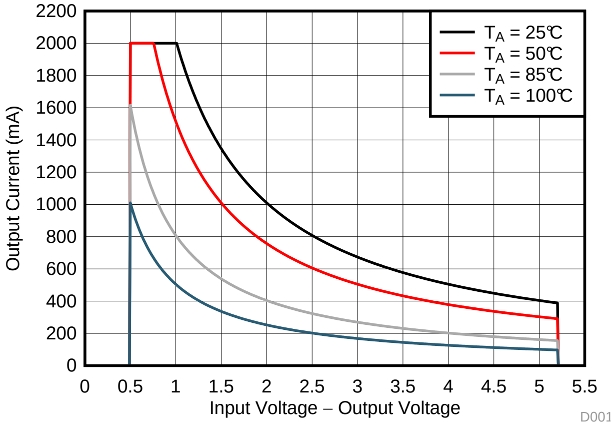


Figure 17. Recommended Continuous Operating Area for V_{OUT} = 0.8 V

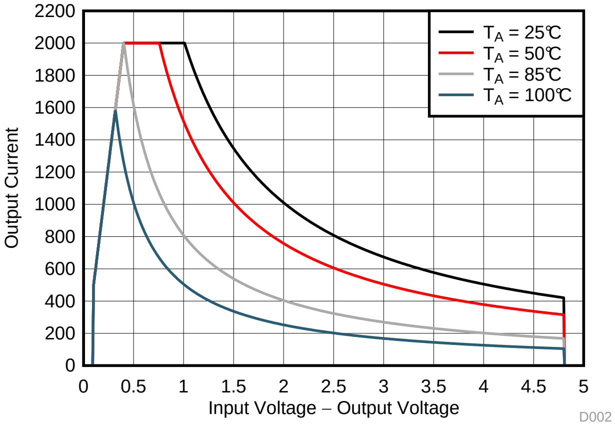


Figure 18. Recommended Continuous Operating Area for V_{OUT} = 1.2 V

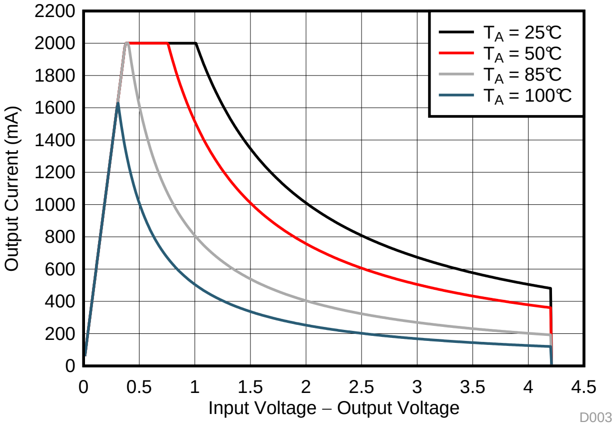


Figure 19. Recommended Continuous Operating Area for V_{OUT} = 1.8 V

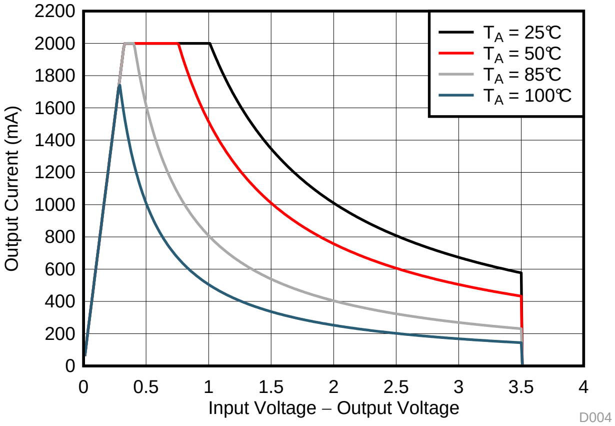


Figure 20. Recommended Continuous Operating Area for V_{OUT} = 2.5 V

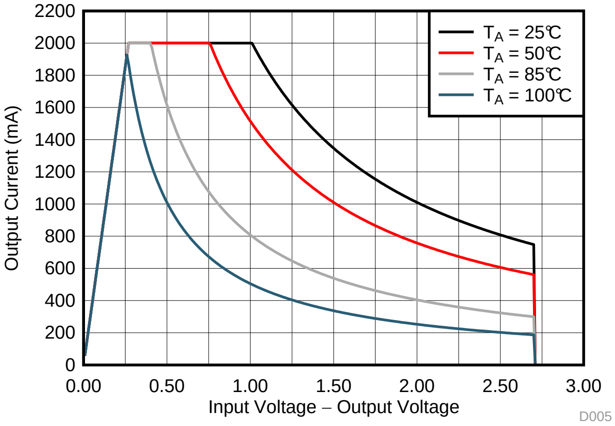


Figure 21. Recommended Continuous Operating Area for V_{OUT} = 3.3 V

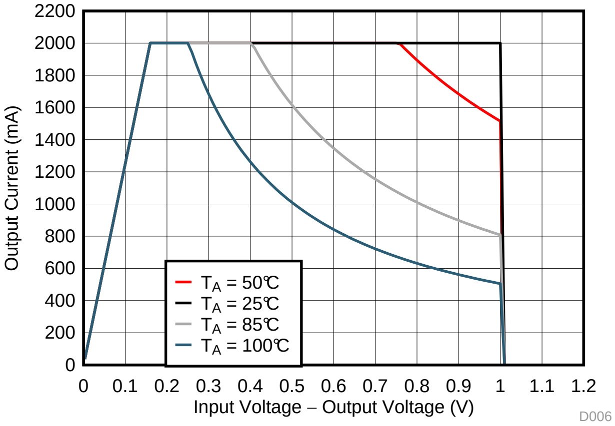


Figure 22. Recommended Continuous Operating Area for V_{OUT} = 5 V

8.2.3 Application Curves

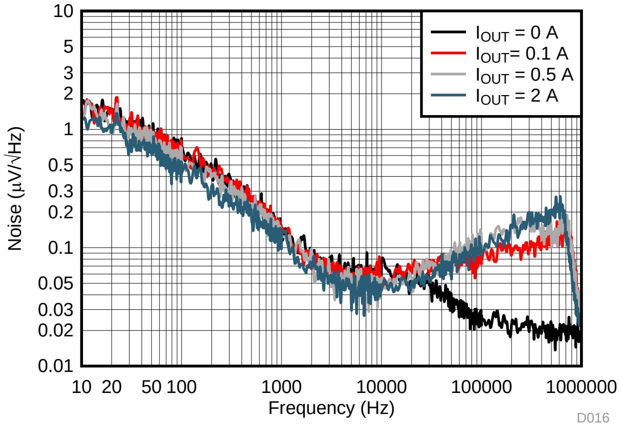


Figure 23. Noise Density vs Frequency

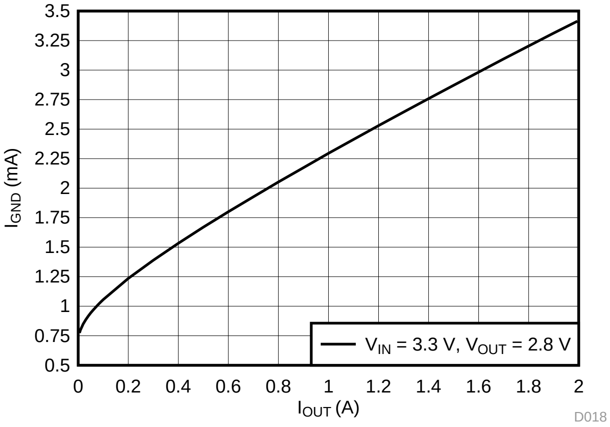


Figure 24. Ground Current vs Output Current

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.3 V to 6 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5922 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 1 V. A minimum capacitor value of 22 µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5922 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5922.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5922 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5922 GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths, narrow trace widths, or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Example

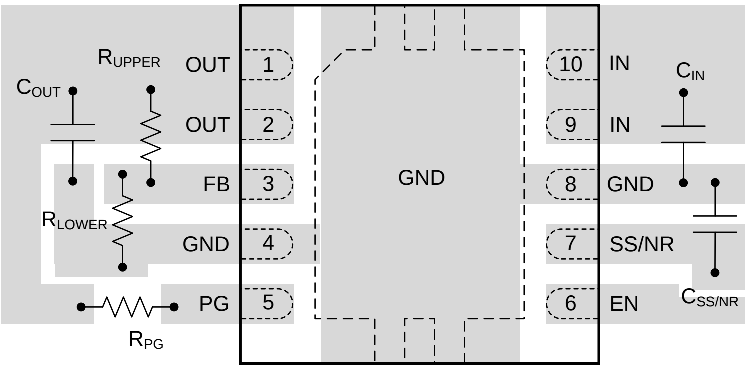


Figure 25. LP5922 Typical Layout

11 デバイスおよびドキュメントのサポート

11.1 関連資料

詳細情報については、以下を参照してください。

- *『新しい温度指標の使用』*
- *『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）*コミュニティ。**エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP592201DSCR	NRND	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201
LP592201DSCR.A	NRND	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201
LP592201DSCT	NRND	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201
LP592201DSCT.A	NRND	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

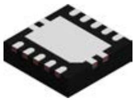
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

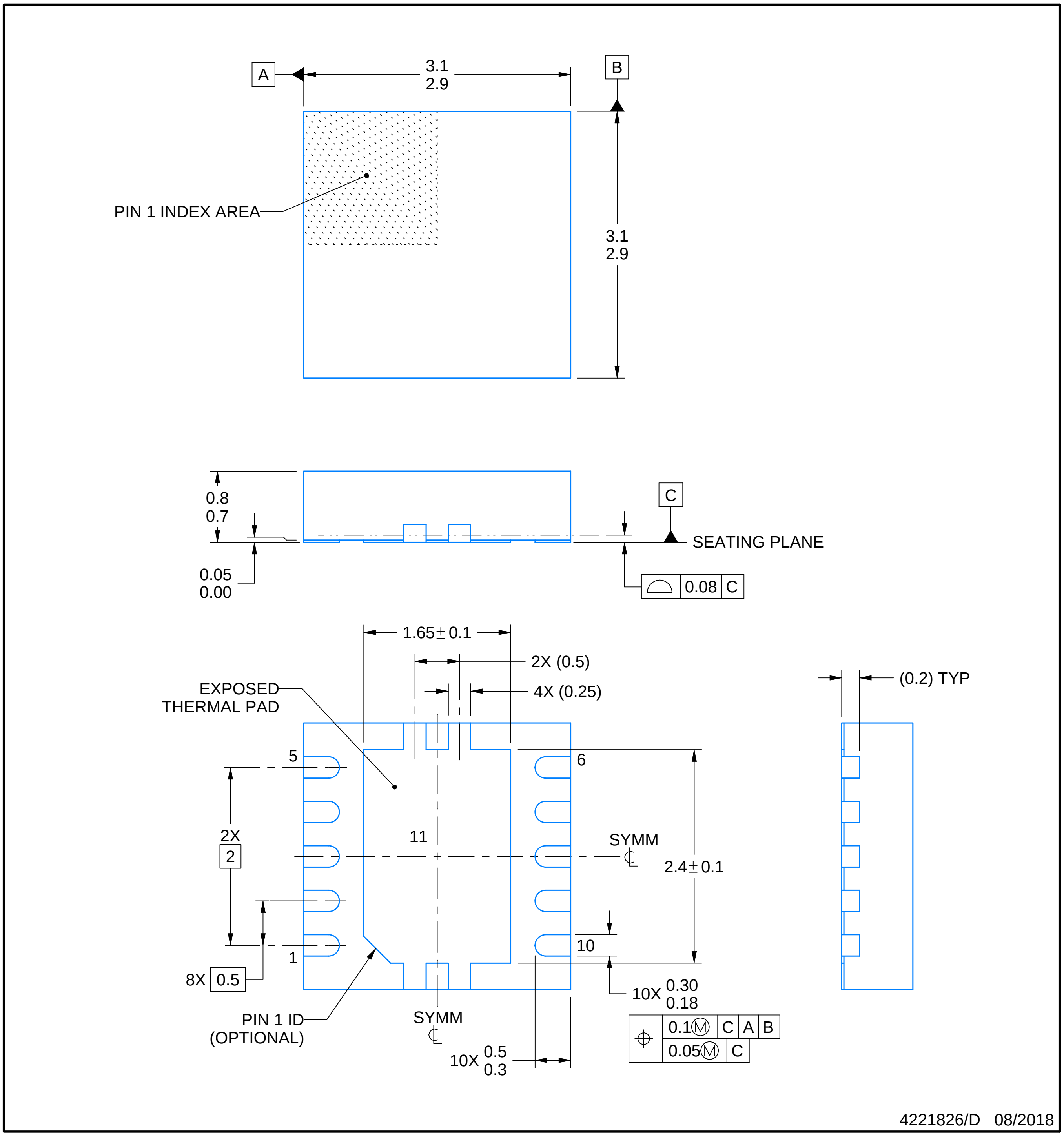


DSC0010J

PACKAGE OUTLINE

WSON - 0.8 mm max height

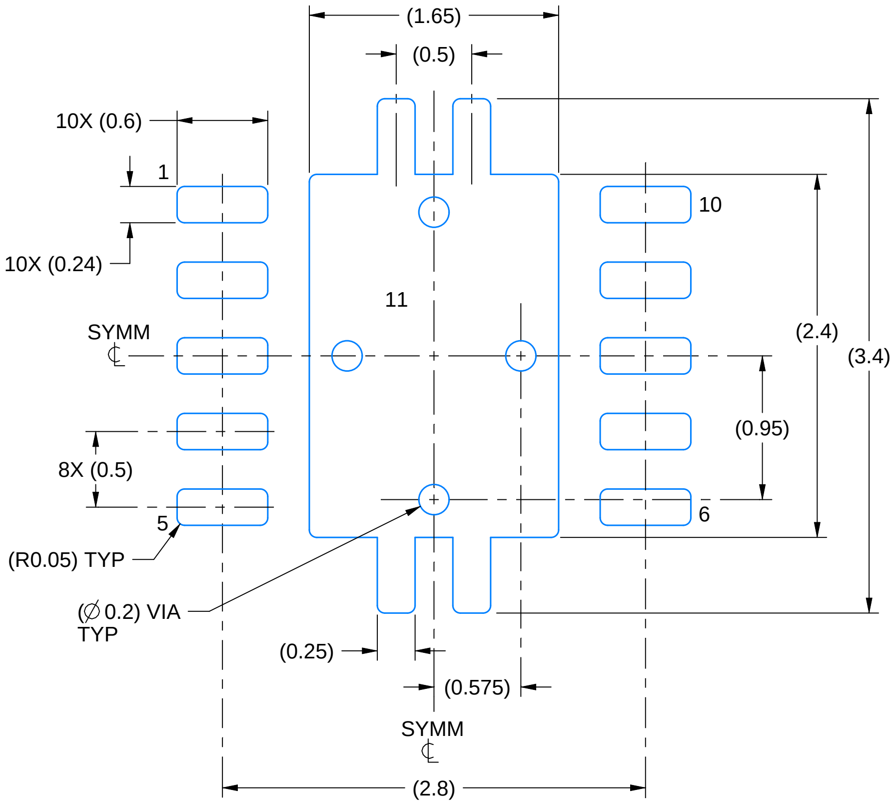
PLASTIC SMALL OUTLINE - NO LEAD



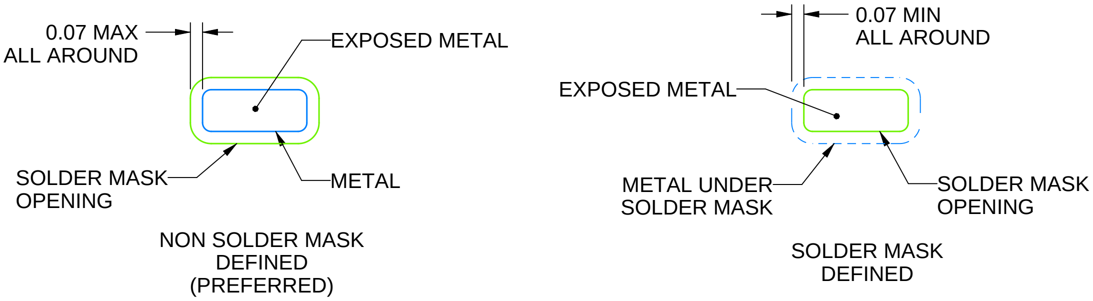
4221826/D 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

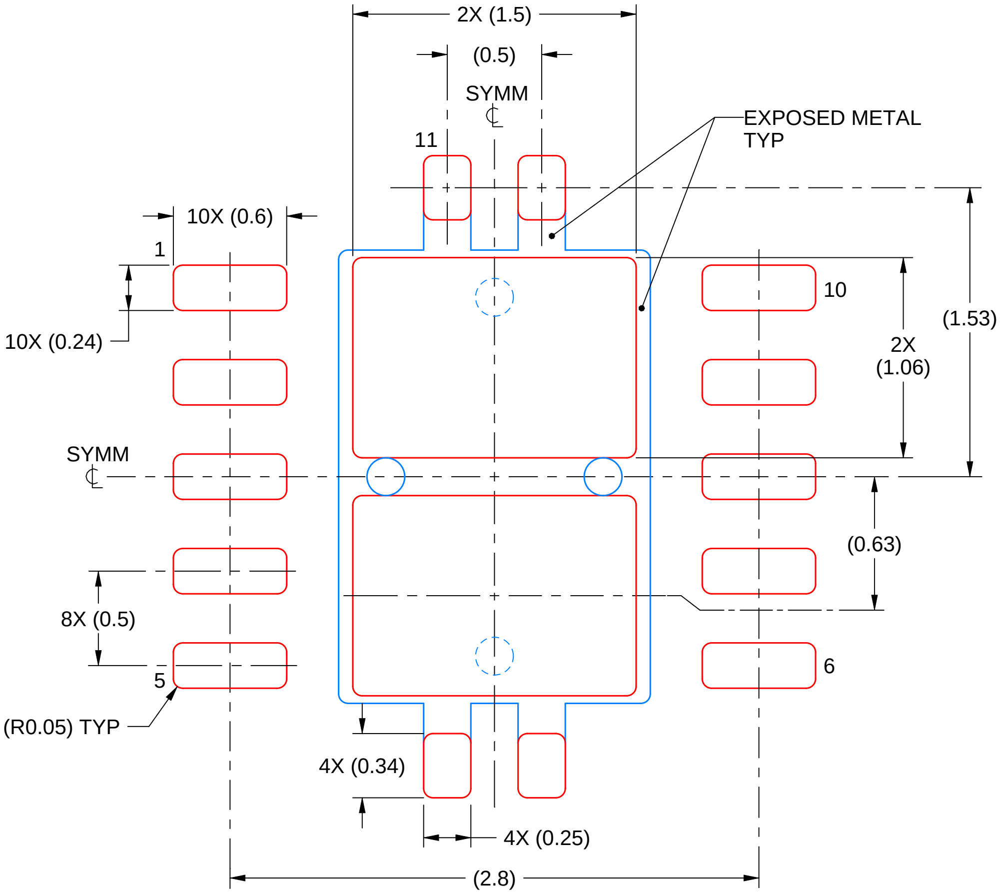


SOLDER MASK DETAILS

4221826/D 08/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス· インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス· インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス· インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス· インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス· インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス· インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス· インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス· インスツルメンツは一切の責任を拒否します。

テキサス· インスツルメンツの製品は、 テキサス· インスツルメンツの販売条件、または ti.com やかかる テキサス· インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス· インスツルメンツがこれらのリソースを提供することは、適用される テキサス· インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス· インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265