









LP5018, LP5024 JAJSF10C - OCTOBER 2018 - REVISED JULY 2024

# LP50xx 18/24 チャネル、12 ビット、PWM 超低静止電流、I<sup>2</sup>C RGB LED ドライ バ

# 1 特長

- 動作電圧範囲:
  - V<sub>CC</sub> 範囲:2.7V~5.5V
  - EN、SDA、SCLピンは 1.8V、3.3V、5V の電源レールに対応
  - 最大出力電圧:6V
- 24 個の高精度定電流シンク
  - V<sub>CC</sub>の全範囲で、チャネルごとに最大 25.5mA
  - V<sub>CC</sub> ≥ 3.3V のとき、チャネルごとに最大 35mA
  - デバイス間誤差:±7%、チャネル間誤差:±7%
- 非常に低い静止電流
  - シャットダウン モード: EN Low で最大値 1μA
  - パワー セーブ モード: EN High、すべての LED が 30ms を超えてオフのとき標準値 10µA
- 各チャネルに 12 ビット、29kHz の PWM ジェネレータ を内蔵:
  - チャネルごとに独立の色混合レジスタ
  - RGB LED モジュールごとに独立の輝度制御レジ
  - 対数的または線形的スケールの輝度制御を選択可
  - 3 相 PWM シフト方式を搭載
- 3 つのプログラム可能バンク (R、G、B) により、各色を ソフトウェアで簡単に制御
- 2 つの外部ハードウェア アドレス ピンにより、最大 4 つのデバイスに接続可能
- ブロードキャストスレーブアドレスにより、複数のデバ イスを同時に構成可能
- 自動インクリメント機能により、1回の伝送で連続する 複数のレジスタを書き込み / 読み取り可能
- 最大 400kHz のファスト モード I<sup>2</sup>C 速度

# 2 アプリケーション

次のような機器の LED ライティング、インジケータ ライト、 および装飾用ライト

- スマート スピーカ (音声アシスタント付き)
- スマートホーム家電
- ビデオドアベル
- 電子スマートロック
- 煙感知器と熱感知器
- STB および DVR
- スマートルータ
- ハンドヘルド デバイス

# 3 概要

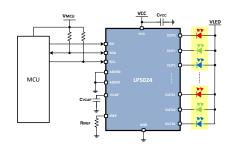
スマート ホームや、ヒューマン マシン インターフェイスを 活用する他のアプリケーションでは、高性能の RGB LED ドライバが必要となります。フラッシュ、ブリージング、追跡 などの LED アニメーション効果により、ユーザー向けの環 境を大幅に改良できます。またシステムノイズが最小限で あることは不可欠です。

LP50xx デバイスは、18 または 24 チャネルの定電流シン ク LED ドライバです。LP50xx デバイスにはカラー ミキシ ングおよび輝度制御機能が内蔵されており、事前設定に よりソフトウェアのコーディング処理を簡素化できます。12 ビット、29kHzの PWM ジェネレータが各チャネルに内蔵 されているため、LED で円滑に、鮮明な色を再現でき、可 聴ノイズが除去されます。

#### 製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LP5024	VQFN (32)	4.00mm × 4.00mm
LP5018	VQFN (32)	4.00mm × 4.00mm
LF3010	VSSOP (28)	7.30mm × 3.00mm

利用可能なすべてのパッケージについては、データシートの末尾 にある注文情報を参照してください。



概略回路図



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# 4 概要 (続き)

LP50xx デバイスは、29kHz のスイッチング周波数、12 ビットの PWM 分解能で各 LED の出力を制御するので、スムーズな調光効果を達成でき、可聴周波数のノイズが排除されます。カラーミキシングと輝度の制御レジスタを別々に制御できるため、ソフトウェアのコーディングが明快になります。フェードイン、フェードアウト型のブリージング効果を行う際、グローバルな R、G、B バンクの制御により、マイクロコントローラの負荷が大幅に減少します。また、LP50xx デバイスにはPWM 位相シフト機能も実装されており、LED が同時にオンになるときの入力電力バジェットを低減するために役立ちます。

LP50xx デバイスには、自動パワーセービング モードが実装されており、非常に低い静止電流を実現しています。 すべて のチャネルが 30ms の間オフのとき、デバイスの合計消費電力は 10μA まで低下するため、LP50xx デバイスはバッテリ 駆動の最終製品に適しています。

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Product Folder Links: LP5018 LP5024



# 5 Pin Configuration and Functions

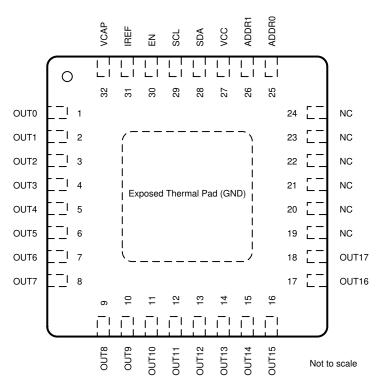


図 5-1. LP5018 RSM Package 32-Pin VQFN With Exposed Thermal Pad Top View

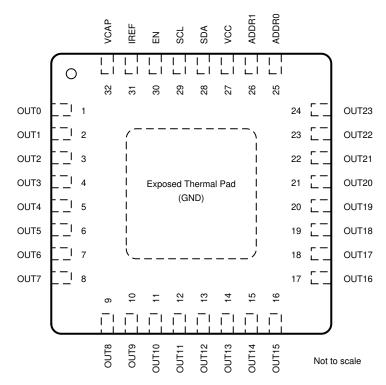


図 5-2. LP5024 RSM Package 32-Pin VQFN With Exposed Thermal Pad Top View

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English Data Sheet: SLVSEB8

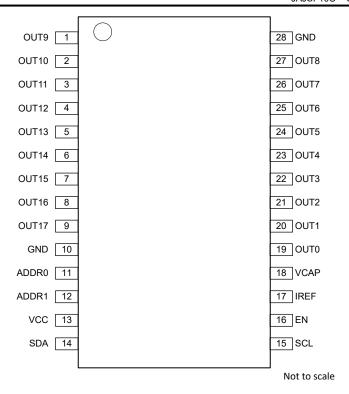


図 5-3. LP5018 DGS Package 28-pin VSSOP Top View

表 5-1. Pin Functions

	LP5018RSM         LP5024RSM         LP5018           DR0         25         25         11           DR1         26         26         12           30         30         16           F         31         31         17           19, 20, 21, 22, 23, 24						
NAME	NO.		I/O	DESCRIPTION			
NAME	LP5018RSM	LP5024RSM	LP5018DGS				
ADDR0	25	25	11	_	I <sup>2</sup> C slave-address selection pin. This pin must not be left floating.		
ADDR1	26	26	12	_	I <sup>2</sup> C slave-address selection pin. This pin must not be left floating.		
EN	30	30	16	I	Chip enable input pin		
IREF	31	31	17	_	Output current-reference global-setting pin		
NC		_	_	_	No internal connection		
OUT0	1	1	19	0	Current sink output 0. If not used, this pin can be left floating.		
OUT1	2	2	20	0	Current sink output 1. If not used, this pin can be left floating.		
OUT2	3	3	21	0	Current sink output 2. If not used, this pin can be left floating.		
OUT3	4	4	22	0	Current sink output 3. If not used, this pin can be left floating.		
OUT4	5	5	23	0	Current sink output 4. If not used, this pin can be left floating.		
OUT5	6	6	24	0	Current sink output 5. If not used, this pin can be left floating.		
OUT6	7	7	25	0	Current sink output 6. If not used, this pin can be left floating.		
OUT7	8	8	26	0	Current sink output 7. If not used, this pin can be left floating.		
OUT8	9	9	27	0	Current sink output 8. If not used, this pin can be left floating.		
OUT9	10	10	1	0	Current sink output 9. If not used, this pin can be left floating.		
OUT10	11	11	2	0	Current sink output 10. If not used, this pin can be left floating.		
OUT11	12	12	3	0	Current sink output 11. If not used, this pin can be left floating.		
OUT12	13	13	4	0	Current sink output 12. If not used, this pin can be left floating.		
OUT13	14	14	5	0	Current sink output 13. If not used, this pin can be left floating.		
OUT14	15	15	6	0	Current sink output 14. If not used, this pin can be left floating.		

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資料に関するフィードバック(ご意見やお問い合わせ)を送信



# 表 5-1. Pin Functions (続き)

		PIN			
NAME		NO.		I/O	DESCRIPTION
NAIVIE	LP5018RSM	LP5024RSM	RSM LP5018DGS		
OUT15	16	16	7	0	Current sink output 15. If not used, this pin can be left floating.
OUT16	17	17	8	0	Current sink output 16. If not used, this pin can be left floating.
OUT17	18	18	9	0	Current sink output 17. If not used, this pin can be left floating.
OUT18	_	19	_	0	Current sink output 18. If not used, this pin can be left floating.
OUT19	_	20	_	0	Current sink output 19. If not used, this pin can be left floating.
OUT20	_	21	_	0	Current sink output 20. If not used, this pin can be left floating.
OUT21	_	22	_	0	Current sink output 21. If not used, this pin can be left floating.
OUT22	_	23	_	0	Current sink output 22. If not used, this pin can be left floating.
OUT23	_	24	_	0	Current sink output 23. If not used, this pin can be left floating.
SCL	29	29	15	I	I <sup>2</sup> C bus clock line. If not used, this pin must be connected to GND or VCC.
SDA	28	28	14	I/O	I <sup>2</sup> C bus data line. If not used, this pin must be connected to GND or VCC.
VCAP	32	32	18	_	Internal LDO output pin, this pin must be connected to a 1µF capacitor to GND. Place the capacitor as close to the device as possible.
VCC	27	27	13	I	Input power.
GND	GND	GND	10, 28	_	Exposed thermal pad also serves the ground pin for the device.

English Data Sheet: SLVSEB8



# 6 Specifications

# **6.1 Absolute Maximum Ratings**

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage on EN, IREF, OUTx, SCL, SDA, VCC	-0.3	6	V
Voltage on ADDRx	-0.3	VCC+0.3	V
Voltage on VCAP	-0.3	2	V
Continuous power dissipation	Inter	nally limited	
Junction temperature, T <sub>J-MAX</sub>	-40	125	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	V

<sup>1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1500 V may actually have higher performance.

## **6.3 Recommended Operating Conditions**

over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage on VCC	2.7	5.5	V
Voltage on OUTx	0	5.5	V
Voltage on ADDRx, EN, SDA, SCL	0	5.5	V
Operating ambient temperature, T <sub>A</sub>	-40	85	°C

#### **6.4 Thermal Information**

		LP5018 d	or LP5024	
	THERMAL METRIC <sup>(1)</sup>	RSM (VQFN)	DGS (VSSOP)	UNIT
		32 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.4	80.2	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	34.8	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	41.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.9	3.8	°C/W
ΨЈВ	Junction-to-board characterization parameter	16	40.7	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	6.3	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see Semiconductor and ICPackage Thermal Metrics .

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.



#### **6.5 Electrical Characteristics**

over operating ambient temperature range ( $-40^{\circ}$ C <  $T_A$ <85°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER	SUPPLIES (VCC)						
V <sub>VCC</sub>	Supply voltage		2.7		5.5	V	
	Shutdown supply current	V <sub>EN</sub> = 0 V		0.2	1		
	Standby supply current	V <sub>EN</sub> = 3.3 V, Chip_EN = 0 (bit)		6	10	μA	
I <sub>vcc</sub>	Normal-mode supply current	With 10-mA LED current per OUTx		5	8	mA	
VCC	Power-save mode supply current	V <sub>EN</sub> = 3.3 V, Chip_EN = 1 (bit), Power_Save_EN = 1 (bit), all the LEDs off duration > t <sub>PSM</sub>		6	10	μА	
V <sub>UVR</sub>	Undervoltage restart	V <sub>VCC</sub> rising	,		2.5	V	
V <sub>UVF</sub>	Undervoltage shutdown	V <sub>VCC</sub> falling	2			V	
V <sub>UV_HYS</sub>	Undervoltage shutdown hysteresis			0.2		V	
OUTPUT	STAGE (OUTx)				I.		
I <sub>MAX</sub>	Maximum sink current (OUT0– OUTx) (For LP5024, x = 23. For LP5018, x = 17.)	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), PWM = 100%			25.5	mA	
'MAX	Maximum sink current (OUT0– OUTx) (For LP5024, x = 23. For LP5018, x = 17.)	V <sub>VCC</sub> ≥ 3.3 V, Max_Current_Option = 1 (bit), PWM = 100%			35		
I <sub>LIM</sub>	Internal sink current limit (OUT0– OUTx) (For LP5024, x = 23. For LP5018, x = 17.)	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), V <sub>IREF</sub> = 0 V	35	55	80	mA	
	Internal sink current limit (OUT0– OUTx) (For LP5024, x = 23. For LP5018, x = 17.)	V <sub>VCC</sub> ≥ 3.3V, Max_Current_Option=1 (bit), V <sub>IREF</sub> = 0 V	40	75	120		
I <sub>lkg</sub>	Leakage current (OUT0-OUTx) (For LP5024, x = 23. For LP5018, x = 17.)	PWM = 0%		0.1	1	μΑ	
I <sub>ERR_DD</sub>	Device to device current error, I <sub>ERR_DD</sub> =(I <sub>AVE</sub> -I <sub>SET</sub> )/I <sub>SET</sub> ×100%	All channels' current set to 10 mA.  PWM = 100%. Already includes the  V <sub>IREF</sub> and K <sub>IREF</sub> tolerance	<b>-7</b> %		7%		
I <sub>ERR_CC</sub>	Channel to channel current error, I <sub>ERR_CC</sub> =(I <sub>OUTX</sub> -I <sub>AVE</sub> )/I <sub>AVE</sub> ×100%	All channels' current set to 10 mA.  PWM = 100%. Already includes the  V <sub>IREF</sub> and K <sub>IREF</sub> tolerance	-7%		7%		
V <sub>IREF</sub>	IREF voltage			0.7		V	
K <sub>IREF</sub>	IREF ratio			105			
$f_{\sf PWM}$	PWM switching frequency		21	29		kHz	
$V_{SAT}$	Output saturation voltage	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.25	0.35	V	
		V <sub>VCC</sub> ≥ 3.3 V, Max_Current_Option = 1 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.3	0.4	•	
LOGIC IN	IPUTS (EN, SCL, SDA, ADDRx)						
V <sub>IL</sub>	Low level input voltage				0.4	V	
V <sub>IH</sub>	High level input voltage		1.4			V	
I <sub>LOGIC</sub>	Input current		-1		1	μΑ	
V <sub>SDA</sub>	SDA output low level	I <sub>PULLUP</sub> = 5 mA			0.4	V	

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Product Folder Links: LP5018 LP5024



# 6.5 Electrical Characteristics (続き)

over operating ambient temperature range ( $-40^{\circ}$ C <  $T_A$ <85°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MA	X UNIT
PROTECTI	ON CIRCUITS				
T <sub>(TSD)</sub>	Thermal-shutdown junction temperature			160	°C
T <sub>(HYS)</sub>	Thermal shutdown temperature hysteresis			15	°C

# **6.6 Timing Requirements**

over operating ambient temperature range (-40°C < T<sub>A</sub><85°C) (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT
fosc	Internal oscillator frequency		15		MHz
t <sub>PSM</sub>	Power save mode deglitch time	20	30	40	ms
t <sub>EN_H</sub>	EN first rising edge until first I <sup>2</sup> C access			500	μs
t <sub>EN_L</sub>	EN first falling edge until first I <sup>2</sup> C reset			3	μs
$f_{\sf SCL}$	I <sup>2</sup> C clock frequency			400	kHz
1	Hold time (repeated) START condition	0.6			μs
2	Clock low time	1.3			μs
3	Clock high time	600			ns
4	Setup time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data setup time	100			ns
7	Rise time of SDA and SCL	20 + 0.1 C <sub>b</sub>		300	ns
8	Fall time of SDA and SCL	15 + 0.1 C <sub>b</sub>		300	ns
9	Setup time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			μs
C <sub>b</sub>	Capacitive load parameter for each bus line Load of 1 pF corresponds to one nanosecond.	10		200	pF

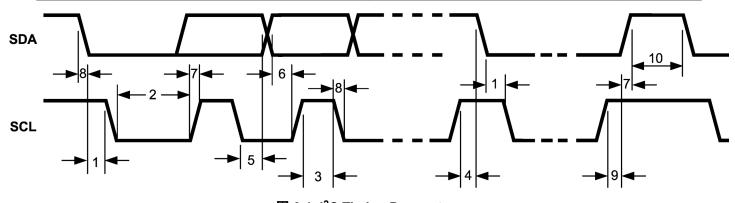


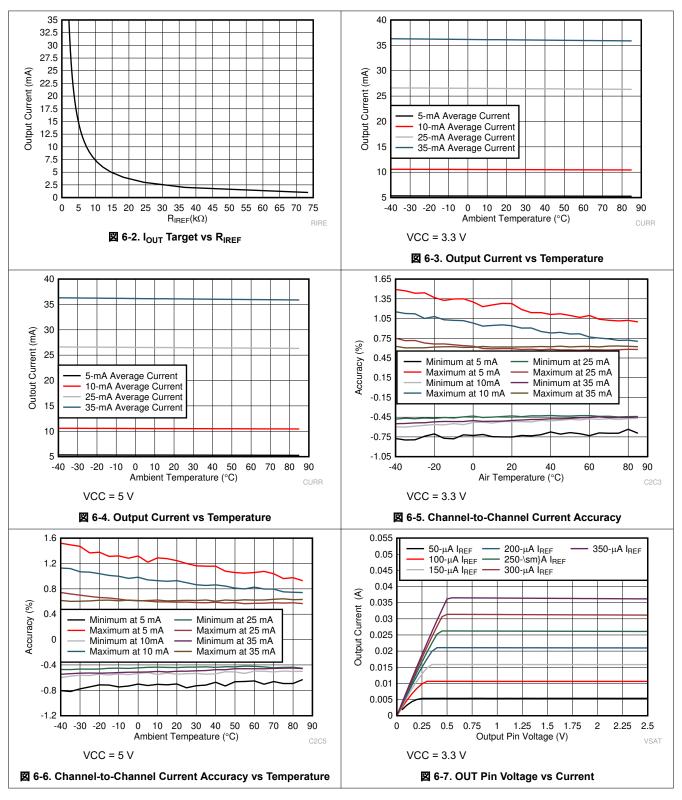
図 6-1. I<sup>2</sup>C Timing Parameters

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Product Folder Links: LP5018 LP5024



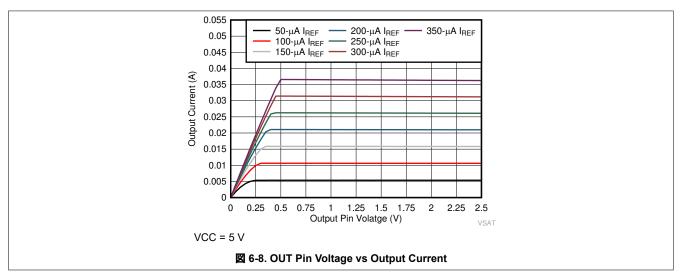
#### 6.7 Typical Characteristics



English Data Sheet: SLVSEB8



# **6.7 Typical Characteristics (continued)**



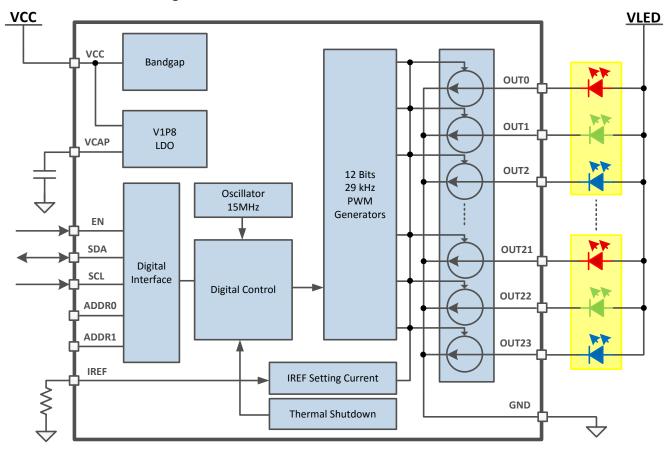
# 7 Detailed Description

#### 7.1 Overview

The LP50xx device is an 18- or 24-channel constant-current-sink LED driver. The LP50xx device includes all necessary power rails, an on-chip oscillator, and a two-wire serial  $I^2C$  interface. The maximum constant-current value of all channels is set by a single external resistor. Two hardware address pins allow up to four devices on the same bus. An automatic power-saving mode is implemented to keep the total current consumption under  $10\mu A$ , which makes the LP50xx device a potential choice for battery-powered end-equipment.

The LP50xx device is optimized for RGB LEDs regarding to both live effects and software efforts. The LP50xx device controls each LED output with 12-bit PWM resolution at 29kHz switching frequency, which helps achieve a smooth dimming effect and eliminates audible noise. The independent color-mixing and intensity-control registers make the software coding straightforward. When targeting a fade-in, fade-out type breathing effect, the global RGB bank control reduces the microcontroller loading significantly. The LP50xx device also implements a PWM phase-shifting function to help reduce the input power budget when LEDs turn on simultaneously.

#### 7.2 Functional Block Diagram



#### 7.3 Feature Description

#### 7.3.1 PWM Control for Each Channel

Most traditional LED drivers are designed for the single-color LEDs, in which the high-resolution PWM generator is used for intensity control only. However, for RGB LEDs, both the color mixing and intensity control should be addressed to achieve the target effect. With the traditional solution, the users must handle the color mixing and intensity control simultaneously with a single PWM register. Several undesired effects occur: the limited dimming steps, the complex software design, and the color distortion when using a logarithmic scale control.

The LP50xx device is designed with independent color mixing and intensity control, which makes the RGB LED effects fancy and the control experience straightforward. With the inputs of the color-mixing register and the intensity-control register, the final PWM generator output for each channel is 12-bit resolution and 29kHz dimming frequency, which helps achieve a smooth dimming effect and eliminates audible noise. See  $\boxtimes$  7-1.

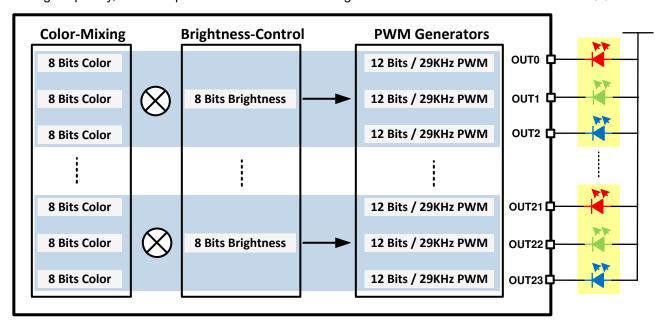


図 7-1. PWM Control Scheme for Each Channel

#### 7.3.1.1 Independent Color Mixing Per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUTx\_COLOR). The device allows every RGB LED module to achieve >16 million (256 × 256 × 256) color-mixing.

#### 7.3.1.2 Independent Intensity Control Per RGB LED Module

When color is fixed, the independent intensity-control is used to achieve accurate and flexible dimming control for every RGB LED module.

#### 7.3.1.2.1 Intensity-Control Register Configuration

Every three consecutive output channels are assigned to their respective intensity-control register (LEDx\_BRIGHTNESS). For example, OUT0, OUT1, and OUT2 are assigned to LED0\_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in LED Bank Control . The LP50xx device allows 256-step intensity control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the LED0\_BRIGHTNESS register results in 100% dimming duty cycle. With this setting, users can just configure the color mixing register by channel to achieve the target dimming effect in a single-color LED application.

#### 7.3.1.2.2 Logarithmic- or Linear-Scale Intensity Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. However, for RGB LEDs, if using a single register to achieve both color mixing and intensity control, color distortion can be observed easily when using a logarithmic scale. The LP50xx device, with independent color-mixing and intensity-control registers, implements the logarithmic scale dimming control inside the intensity control function, which solves the color distortion issue effectively. See  $\boxtimes$  7-2. Also, the LP50xx device allows users to configure the dimming scale either logarithmically or linearly through the global Log\_Scale\_EN register. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach. See  $\boxtimes$  7-3.

# Brightness Control 8 Bits Brightness Linear OR Logarithmic 8 Bits Brightness Linear OR Logarithmic

図 7-2. Logarithmic- or Linear-Scale Intensity Control

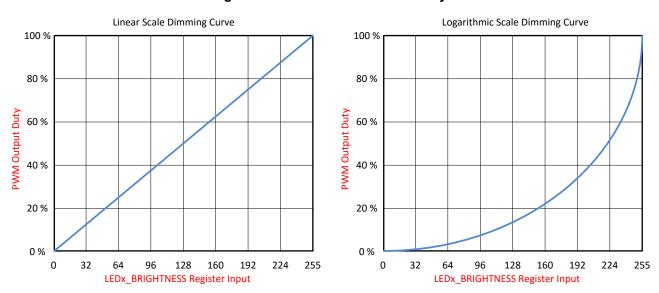


図 7-3. Logarithmic vs Linear Dimming Curve

#### 7.3.1.3 12-Bit, 29-kHz PWM Generator Per Channel

# 7.3.1.3.1 PWM Generator

With the inputs of the color mixing and the intensity control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related intensity-control register value. The

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final output PWM duty cycle has 12 bits of control accuracy, which is achieved by a 9 bits of pure PWM resolution and 3 bits of digital dithering control. For 3-bit dithering, every eighth pulse is made 1 LSB longer to increase the average value by 1 / 8th. The LP50xx device allows users to enable or disable the dithering function through the PWM\_Dithering\_EN register. When enabled (default), the output PWM duty-cycle accuracy is 12 bits. When disabled, the output PWM duty-cycle accuracy is 9 bits.

To eliminate the audible noise due to the PWM switching, the LP50xx device sets the PWM switching frequency at 29-kHz, above the 20-kHz human hearing range.

#### 7.3.1.4 PWM Phase-Shifting

A PWM phase-shifting scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases.

- Phase 1—the rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, ..., LED21.
- Phase 2—the middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, ..., LED22.
- Phase 3—the falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, ..., LED23.

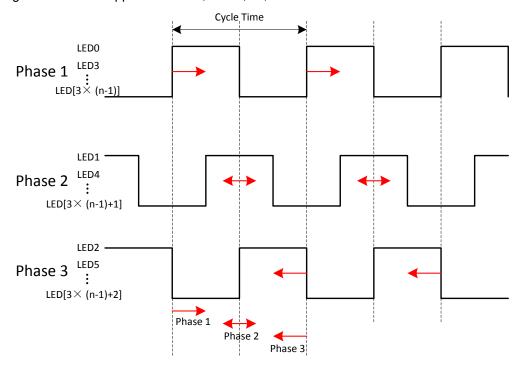


図 7-4. PWM Phase-Shifting

#### 7.3.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily, the LP50xx device provides an easy coding approach, the LED bank control.

Each channel can be configured as either independent control or bank control through the LEDx\_Bank\_EN register. When LEDx\_Bank\_EN = 0 (default), the LED is controlled independently by the related color-mixing and intensity-control registers. When LEDx\_Bank\_EN = 1, the LP50xx device drives the LEDs in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM

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scheme of each channel. For more details, see *PWM Control for Each Channel*. When a channel is configured in LED bank-control mode, the related color mixing and intensity control is governed by the bank control registers (BANK\_A\_COLOR, BANK\_B\_COLOR, BANK\_C\_COLOR, and BANK\_BRIGHTNESS) regardless of the inputs on its own color-mixing and intensity-control registers.

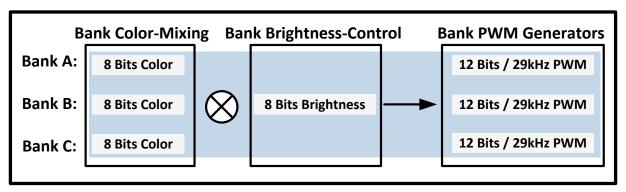


図 7-5. Bank PWM Control Scheme

表 7-1. Bank Number and LED Number Assignment

		. Dank Number a	nd LED Number A	Assignment		
	OUT NUMBER		OUT CORLOR	BANK Number	RGB LED MODULE	
LP5024VQFN	LP5018VQFN	LP5018VSSOP	OUTCORLOR	DANK Number	NUMBER	
OUT0	OUT0	OUT0	OUT0_COLOR	Bank A		
OUT1	OUT1	OUT1	OUT1_COLOR	Bank B	LED0	
OUT2	OUT2	_	OUT2_COLOR	Bank C	1	
OUT3	OUT3	OUT2	OUT3_COLOR	Bank A		
OUT4	OUT4	OUT3	OUT4_COLOR	Bank B	LED1	
OUT5	OUT5	OUT4	OUT5_COLOR	Bank C		
OUT6	OUT6	_	OUT6_COLOR	Bank A		
OUT7	OUT7	OUT5	OUT7_COLOR	Bank B	LED2	
OUT8	OUT8	OUT6	OUT8_COLOR	Bank C		
OUT9	9 OUT9 (		OUT9_COLOR	Bank A		
OUT10	OUT10	OUT8	OUT10_COLOR	Bank B	LED3	
OUT11	OUT11	_	OUT11_COLOR	Bank C		
OUT12	OUT12	OUT9	OUT12_COLOR	Bank A		
OUT13	OUT13	OUT10	OUT13_COLOR	Bank B	LED4	
OUT14	OUT14	OUT11	OUT14_COLOR	Bank C		
OUT15	OUT15	OUT12	OUT15_COLOR	Bank A		
OUT16	OUT16	_	OUT16_COLOR	Bank B	LED5	
OUT17	OUT17	OUT13	OUT17_COLOR	Bank C		
OUT18	_	_	OUT18_COLOR	Bank A		
OUT19	_	OUT14	OUT19_COLOR	Bank B	LED6	
OUT20	— OUT15		OUT20_COLOR	Bank C	1	
OUT21	_	OUT16	OUT21_COLOR	Bank A		
OUT22	_	OUT17	OUT22_COLOR	Bank B	LED7	
OUT23	_	_	OUT23_COLOR	Bank C		



With the bank control configuration, the LP50xx device enables users to achieve smooth and live LED effects globally with an ultrasimple software effort.  $\boxtimes$  7-6 shows an example using LED0 as an independent RGB indicator and others with group breathing effect.

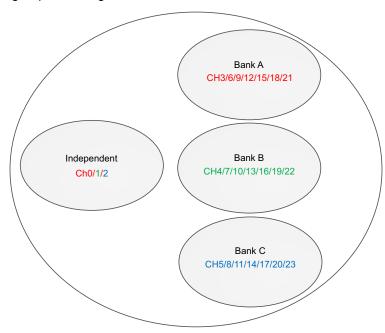


図 7-6. Bank PWM Control Example (Applicable to LP5024 VQFN and LP5018 VQFN only)

#### 7.3.3 Current Range Setting

The constant-current value ( $I_{SET}$ ) of all 24 channels is set by a single external resistor,  $R_{IREF}$ . The value of  $R_{IREF}$  can be calculated by  $\pm 1$ .

$$R_{IREF} = K_{IREF} \times \frac{V_{IREF}}{I_{SET}}$$
 (1)

where:

- K<sub>IREF</sub> = 105
- V<sub>IREE</sub> = 0.7V

With the IREF pin floating, the output current is close to zero. With the IREF pin shorted to GND, the LP50xx device provides internal current-limit protection, and the output-channel maximum current is limited to  $I_{LIM}$ .

The LP50xx device supports two levels of maximum output current, I<sub>MAX</sub>.

- When V<sub>CC</sub> is in the range from 2.7V to 5.5V, and the Max Current Option (bit) = 0, I<sub>MAX</sub> = 25.5mA.
- When  $V_{CC}$  is in the range from 3.3V to 5.5V, and the Max\_Current\_Option (bit) = 1,  $I_{MAX}$  = 35mA.

#### 7.3.4 Automatic Power-Save Mode

When all the LED outputs are inactive, the LP50xx device is able to enter power-save mode automatically, thus lowering idle-current consumption down to  $10\mu A$  (typical). Automatic power-save mode is enabled when register bit Power\_Save\_EN = 1 (default) and all the LEDs are off for a duration of >30ms. Almost all analog blocks are powered down in power-save mode. If any I<sup>2</sup>C command to the device occurs, the LP50xx device returns to NORMAL mode.

#### 7.3.5 Protection Features

#### 7.3.5.1 Thermal Shutdown

The LP50xx device implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical), the device switches into shutdown mode. The LP50xx device releases thermal shutdown when the junction temperature of the device is reduced to 145°C (typical).

#### 7.3.5.2 UVLO

The LP50xx device has an internal comparator that monitors the voltage at  $V_{CC}$ . When  $V_{CC}$  is below  $V_{UVF}$ , reset is active and the LP50xx device is in the INITIALIZATION state.

#### 7.4 Device Functional Modes

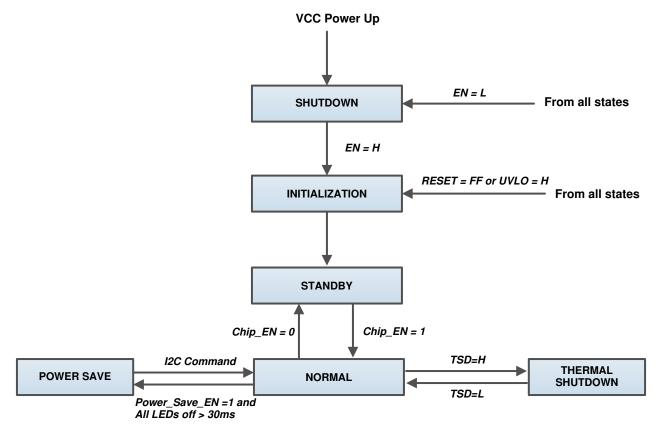


図 7-7. Functional Modes

- **INITIALIZATION**: The device enters into INITIALIZATION mode when EN = H. In this mode, all the registers are reset. Entry can also be from any state, if the RESET (register) = FFh or UVLO is active.
- NORMAL: The device enters the NORMAL mode when Chip\_EN (register) = 1. I<sub>CC</sub> is 10mA (typical).
- POWER SAVE: The device automatically enters the POWER SAVE mode when Power\_Save\_EN (register) =
  1 and all the LEDs are off for a duration of > 30ms. In POWER SAVE mode, analog blocks are disabled to
  minimize power consumption, but the registers retain the data and keep it available via I<sup>2</sup>C. I<sub>CC</sub> is 10μA
  (typical). In case of any I<sup>2</sup>C command to this device, it returns to the NORMAL mode.
- SHUTDOWN: The device enters into SHUTDOWN mode from all states on V<sub>CC</sub> power up or when EN = L.
   I<sub>CC</sub> is < 1μA (maximum).</li>
- **STANDBY**: The device enters the STANDBY mode when Chip\_EN (register) = 0. In this mode, all the OUTx pins are shut down, but the registers retain the data and keep it available via I<sup>2</sup>C. STANDBY is the low-power-consumption mode, when all circuit functions are disabled. I<sub>CC</sub> is 10µA (typical).

• **THERMAL SHUTDOWN**: The device automatically enters the THERMAL SHUTDOWN mode when the junction temperature exceeds 160°C (typical). In this mode, all the OUTx outputs are shut down. If the junction temperature decreases below 145°C (typical), the device returns to the NORMAL mode.

#### 7.5 Programming

#### 7.5.1 I<sup>2</sup>C Interface

The I<sup>2</sup>C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle.

#### 7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

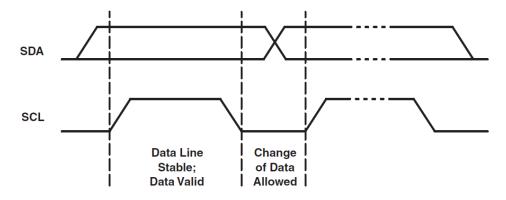


図 7-8. Data Validity

#### 7.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

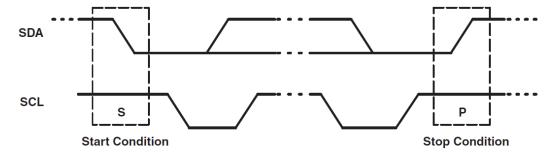


図 7-9. Start and Stop Conditions

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#### 7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most-significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the ninth clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge-after-every-byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

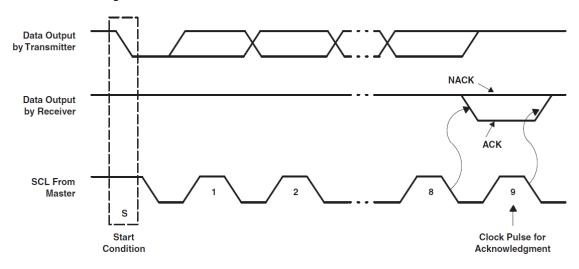


図 7-10. Acknowledge and Not Acknowledge on I<sup>2</sup>C Bus

#### 7.5.1.4 I<sup>2</sup>C Slave Addressing

The device slave address is defined by connecting GND or VCC to the ADDR0 and ADDR1 pins. A total of four independent slave addresses can be realized by combinations when GND or VCC is connected to the ADDR0 and ADDR1 pins (see  $\pm$  7-2 and  $\pm$  7-3).

The device responds to a broadcast slave address regardless of the setting of the ADDR0 and ADDR1 pins. Global writes to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I<sup>2</sup>C bus contain the same value in the addressed register.

ADDR1	ADDR0	SLAVE ADDRESS							
ADDRI	ADDRO	INDEPENDENT	BROADCAST						
GND	GND	010 1000							
GND	VCC	010 1001	011 1100						
VCC	GND	010 1010	011 1100						
VCC	VCC	010 1011							

表 7-2. Slave-Address Combinations

English Data Sheet: SLVSEB8

# 表 7-3. Chip Address

		SLAVE ADDRESS							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Independent	0	1	0	1	0	ADDR1	ADDR0	1 or 0	
Broadcast	0	1	1	1	1	0	0	1 or 0	

#### 7.5.1.5 Control-Register Write Cycle

- · The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/ $\overline{W}$  = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- · The slave device sends an acknowledge signal.
- The master device sends the data byte to be written to the addressed register.
- The slave device sends an acknowledge signal.
- If the master device sends further data bytes, the control register address of the slave is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The write cycle ends when the master device creates a stop condition.



図 7-11. Write Cycle

#### 7.5.1.6 Control-Register Read Cycle

- · The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/ W = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- · The master device generates a repeated-start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/ $\overline{W}$  = 1).
- The slave device sends an acknowledge signal if the slave address is correct.
- The slave device sends the data byte from the addressed register.
- If the master device sends an acknowledge signal, the control-register address is incremented by 1. The slave device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the master device does not generate an acknowledge signal after a data byte and generates a stop condition.

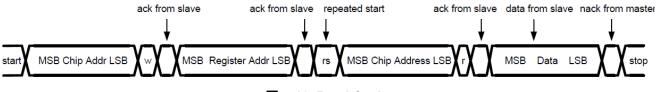


図 7-12. Read Cycle

#### 7.5.1.7 Auto-Increment Feature

The auto-increment feature allows writing or reading several consecutive registers within one transmission. For example, when an 8-bit word is sent to the device, the internal address index counter is incremented by 1, and

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the next register is written. The auto-increment feature is enabled by default and can be disabled by setting the Auto\_Incr\_EN bit = 0 in the DEVICE\_CONFIG1 register. The auto-increment feature is applied for the full register address from 0h to FFh.

Product Folder Links: LP5018 LP5024



# 7.6 Register Maps

表 7-4 lists the memory-mapped registers of the device.

# 表 7-4. Register Maps

			I		32, 7 7. 1	register maps			I		
REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEF- AULT
DEVICE_ CONFIG0	00h	R/W	RESERVED	Chip_EN			RESE	RVED			00h
DEVICE_ CONFIG1	01h	R/W	RESE	RVED	Log_Scale_EN	Power_Save_ EN	Auto_Incr_EN	PWM_ Dithering_EN	Max_Current_ Option	LED_Global Off	3Ch
LED_CONFIG0	02h	R/W	LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN	00h
BANK_ BRIGHTNESS	03h	R/W		Bank_Brightness FF						FFh	
BANK_A_ COLOR	04h	R/W		Bank_A_Color 0					00h		
BANK_B_ COLOR	05h	R/W		Bank_B_Color 0						00h	
BANK_C_ COLOR	06h	R/ ₩		Bank_C_Color 00						00h	
LED0_ BRIGHTNESS	07h	R/ ₩				LED0_B	rightness				FFh
LED1_ BRIGHTNESS	08h	R/W				LED1_B	rightness				FFh
LED2_ BRIGHTNESS	09h	R/W				LED2_B	rightness				FFh
LED3_ BRIGHTNESS	0Ah	R/W				LED3_B	rightness				FFh
LED4_ BRIGHTNESS	0Bh	R/ ₩				LED4_B	rightness				FFh
LED5_ BRIGHTNESS	0Ch	R/₩				LED5_B	rightness				FFh
LED6_ BRIGHTNESS	0Dh	R/W				LED6_B	rightness				FFh
LED7_ BRIGHTNESS	0Eh	R/W		LED7_Brightness F					FFh		
OUT0_COLOR	0Fh	R/W		OUT0_Color 00						00h	
OUT1_COLOR	10h	R/W		OUT1_Color 0					00h		
OUT2_COLOR	11h	R/W				OUT2	_Color				00h

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表 7-4. Register Maps (続き)

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEF- AULT
OUT3_COLOR	12h	R/W		OUT3_Color							
OUT4_COLOR	13h	R/W				OUT4	_Color				00h
OUT5_COLOR	14h	R/W				OUT5	_Color				00h
OUT6_COLOR	15h	R/W				OUT6	_Color				00h
OUT7_COLOR	16h	R/W				OUT7	_Color				00h
OUT8_COLOR	17h	R/W				OUT8	_Color				00h
OUT9_COLOR	18h	R/W				OUT9	_Color				00h
OUT10_COLOR	19h	R/W				OUT10	_Color				00h
OUT11_COLOR	1Ah	R/W				OUT11	_Color				00h
OUT12_COLOR	1Bh	R/W				OUT12	_Color				00h
OUT13_COLOR	1Ch	R/W				OUT13	_Color				00h
OUT14_COLOR	1Dh	R/W				OUT14	_Color				00h
OUT15_COLOR	1Eh	R/W				OUT15	_Color				00h
OUT16_COLOR	1Fh	R/W				OUT16	_Color				00h
OUT17_COLOR	20h	R/W				OUT17	_Color				00h
OUT18_COLOR	21h	R/W				OUT18	_Color				00h
OUT19_COLOR	22h	R/W				OUT19	_Color				00h
OUT20_COLOR	23h	R/W		OUT20_Color						00h	
OUT21_COLOR	24h	R/W	OUT21_Color						00h		
OUT22_COLOR	25h	R/W	OUT22_Color						00h		
OUT23_COLOR	26h	R/W		OUT23_Color							00h
RESET	27h	W				Re	set				00h

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Product Folder Links: LP5018 LP5024



表 7-5. Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION						
Read Type								
R	R	Read						
Write Type								
W	W	Write						
Reset or Default Value	Reset or Default Value							
-n		Value after reset or the default value						

25

Product Folder Links: LP5018 LP5024

## 7.6.1 DEVICE\_CONFIG0 (Address = 0h) [reset = 0h]

DEVICE\_CONFIG0 is shown in 図 7-13 and described in 表 7-6.

Return to 表 7-4.

## 図 7-13. DEVICE\_CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED	Chip_EN			RESE	RVED		
R/ W-0h	R/ W-0h			R/ ₹	∇-0h		

## 表 7-6. DEVICE\_CONFIGO Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	Chip_EN	R/W	0h	1 = LP50xx enabled 0 = LP50xx not enabled
5–0	RESERVED	R/W	0h	Reserved

# 7.6.2 DEVICE\_CONFIG1 (Address = 1h) [reset = 3Ch]

DEVICE\_CONFIG1 is shown in 図 7-14 and described in 表 7-7.

Return to 表 7-4.

## 図 7-14. DEVICE\_CONFIG1 Register

7	6	5	4	3	2	1	0
RESE	RVED	Log_Scale_EN	Power_Save_E	Auto_Incr_EN		Optional_Headr	LED_Global Off
			N		_EN	oom	
R/ ₹	∇-0h	R/ <b>W</b> -1h	R/ ₩-1h	R/ ₩-1h	R/ ₩-1h	R/ W-0h	R/ ₩-0h

#### 表 7-7. DEVICE\_CONFIG1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–6	RESERVED	R/W	0h	Reserved
5	Log_Scale_EN	R/W	1h	1 = Logarithmic scale dimming curve enabled     0 = Linear scale dimming curve enabled
4	Power_Save_EN	R/W	1h	<ul><li>1 = Automatic power-saving mode enabled</li><li>0 = Automatic power-saving mode not enabled</li></ul>
3	Auto_Incr_EN	R/W	1h	<ul><li>1 = Automatic increment mode enabled</li><li>0 = Automatic increment mode not enabled</li></ul>
2	PWM_Dithering_EN	R/W	1h	1 = PWM dithering mode enabled 0 = PWM dithering mode not enabled
1	Max_Current_Option	R/W	0h	1 = Output maximum current I <sub>MAX</sub> = 35 mA. 0 = Output maximum current I <sub>MAX</sub> = 25.5 mA.
0	LED_Global Off	R/W	0h	1 = Shut down all LEDs 0 = Normal operation

## 7.6.3 LED\_CONFIG0 (Address = 2h) [reset = 00h]

LED\_CONFIG0 is shown in 図 7-15 and described in 表 7-8.

Return to 表 7-4.

#### 図 7-15. LED CONFIG0 Register

			_				
7	6	5	4	3	2	1	0
LED7_Bank_E	LED6_Bank_E	LED5_Bank_E	LED4_Bank_E	LED3_Bank_E	LED2_Bank_E	LED1_Bank_E	LED0_Bank_E
N	N	N	N	N	N	N	N

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# 図 7-15. LED\_CONFIG0 Register (続き)

R/ $\overline{W}$ -0h R/ $\overline{W}$ -0h

# 表 7-8. LED\_CONFIG0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	LED7_Bank_EN	R/W	0h	1 = LED7 bank control mode enabled 0 = LED7 independent control mode enabled
6	LED6_Bank_EN	R/W	0h	1 = LED6 bank control mode enabled 0 = LED6 independent control mode enabled
5	LED5_Bank_EN	R/W	0h	1 = LED5 bank control mode enabled 0 = LED5 independent control mode enabled
4	LED4_Bank_EN	R/W	0h	1 = LED4 bank control mode enabled 0 = LED4 independent control mode enabled
3	LED3_Bank_EN	R/W	0h	1 = LED3 bank control mode enabled 0 = LED3 Independent control mode enabled
2	LED2_Bank_EN	R/W	0h	1 = LED2 bank control mode enabled 0 = LED2 independent control mode enabled
1	LED1_Bank_EN	R/W	0h	1 = LED1 bank control mode enabled 0 = LED1 independent control mode enabled
0	LED0_Bank_EN	R/W	0h	1 = LED0 bank control mode enabled 0 = LED0 independent control mode enabled

# 7.6.4 BANK\_BRIGHTNESS (Address = 3h) [reset = FFh]

BANK\_BRIGHTNESS is shown in 図 7-16 and described in 表 7-9.

Return to 表 7-4.

# 図 7-16. BANK\_BRIGHTNESS Register

7 6 5 4				3	2	1	0	
	Bank_Brightness							
			R/W	-FFh				

# 表 7-9. BANK\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	Bank_Brightness	R/W	FFh	FFh = 100% of full brightness
				 80h = 50% of full brightness
				00h = 0% of full brightness

## $7.6.5 \, BANK\_A\_COLOR \, (Address = 4h) \, [reset = 00h]$

BANK\_A\_COLOR is shown in 図 7-17 and described in 表 7-10.

Return to 表 7-4.

# 図 7-17. BANK\_A\_COLOR Register

7	6	5	4	3	2	1	0	
	Bank_A_Color							
	R/ W-0h							

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# 表 7-10. BANK\_A\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	Bank_A_Color	R/W	0h	FFh = The color mixing percentage is 100%.
				 80h = The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## $7.6.6 \; BANK\_B\_COLOR \; (Address = 5h) \; [reset = 00h]$

BANK\_B\_COLOR is shown in 図 7-18 and described in 表 7-11.

Return to 表 7-4.

# 図 7-18. BANK\_B\_COLOR Register

7	6	5 4		3	2	1	0
Bank_B_Color							
			R/ ₹	√-0h			

## 表 7-11. BANK\_B\_COLOR Register Field Descriptions

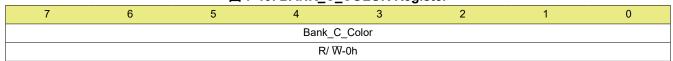
	Bit	Field	Туре	Reset	Description
Γ	7–0	Bank_B_Color	R/W	0h	FFh = The color mixing percentage is 100%.
					 80h = The color mixing percentage is 50%.
					 00h = The color mixing percentage is 0%.

## $7.6.7 \; BANK\_C\_COLOR \; (Address = 6h) \; [reset = 00h]$

BANK\_C\_COLOR is shown in 図 7-19 and described in 表 7-12.

Return to 表 7-4.

# 図 7-19. BANK\_C\_COLOR Register



#### 表 7-12. BANK\_C\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	Bank_C_Color	R/W	0h	FFh = The color mixing percentage is 100%.
				 80h = The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

# 7.6.8 LED0\_BRIGHTNESS (Address = 7h) [reset = FFh]

LED0\_BRIGHTNESS is shown in 図 7-20 and described in 表 7-13.

Return to 表 7-4.

#### 図 7-20. LED0\_BRIGHTNESS Register

7	7 6 5 4				2	1	0	
	LED0_Brightness							
	R/ W-FFh							

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### 表 7-13. LED0\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	LED0_Brightness	R/W	FFh	FFh = 100% of full intensity
				80h = 50% of full intensity
				 00h = 0% of full intensity

#### 7.6.9 LED1\_BRIGHTNESS (Address = 8h) [reset = FFh]

LED1 BRIGHTNESS is shown in 図 7-21 and described in 表 7-14.

Return to 表 7-4.

# 図 7-21. LED1\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED1_Brightness							
			R/ W	7-FFh			

#### 表 7-14. LED1 BRIGHTNESS Register Field Descriptions

			_		9
	Bit	Field	Туре	Reset	Description
ĺ	7–0	LED1_Brightness	R/W	FFh	FFh = 100% of full intensity
					 80h = 50% of full intensity
					 00h = 0% of full intensity

#### 7.6.10 LED2\_BRIGHTNESS (Address = 9h) [reset = FFh]

LED2\_BRIGHTNESS is shown in 図 7-22 and described in 表 7-15.

Return to 表 7-4.

#### 図 7-22. LED2\_BRIGHTNESS Register



#### 表 7-15. LED2\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	LED2_Brightness	R/W	FFh	FFh = 100% of full intensity
				 80h = 50% of full intensity
				00h = 0% of full intensity

# 7.6.11 LED3\_BRIGHTNESS (Address = 0Ah) [reset = FFh]

LED3\_BRIGHTNESS is shown in 図 7-23 and described in 表 7-16.

Return to 表 7-4.

#### 図 7-23. LED3 BRIGHTNESS Register

			· -		J			
7	6	5	4	3	2	1	0	
LED3_Brightness								
	R/ W-FFh							

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## 表 7-16. LED3\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	LED3_Brightness	R/W	FFh	FFh = 100% of full intensity
				 80h = 50% of full intensity
				 00h = 0% of full intensity

## 7.6.12 LED4\_BRIGHTNESS (Address = 0Bh) [reset = FFh]

LED4\_BRIGHTNESS is shown in 図 7-24 and described in 表 7-17.

Return to 表 7-4.

# 図 7-24. LED4\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
	LED4_Brightness						
			R/ W	-FFh			

## 表 7-17. LED4\_BRIGHTNESS Register Field Descriptions

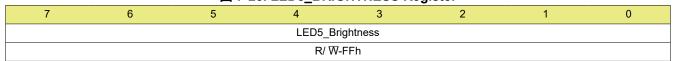
Bit	Field	Туре	Reset	Description
7–0	LED4_Brightness	R/W	FFh	FFh = 100% of full intensity
				 80h = 50% of full intensity
				00h = 0% of full intensity

## 7.6.13 LED5\_BRIGHTNESS (Address = 0Ch) [reset = FFh]

LED5\_BRIGHTNESS is shown in 図 7-25 and described in 表 7-18.

Return to 表 7-4.

# 図 7-25. LED5\_BRIGHTNESS Register



#### 表 7-18. LED5\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	LED5_Brightness	R/W	FFh	FFh = 100% of full intensity
				 80h = 50% of full intensity
				 00h = 0% of full intensity

# 7.6.14 LED6\_BRIGHTNESS (Address = 0Dh) [reset = FFh]

LED6\_BRIGHTNESS is shown in 図 7-26 and described in 表 7-19.

Return to 表 7-4.

#### 図 7-26. LED6\_BRIGHTNESS Register

7	6	5	4	3	2	1	0		
	LED6_Brightness								
	R/ W-FFh								

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# 表 7-19. LED6\_BRIGHTNESS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	LED6_Brightness	R/W	FFh	FFh = 100% of full intensity
				80h = 50% of full intensity 00h = 0% of full intensity

## 7.6.15 LED7\_BRIGHTNESS (Address = 0Eh) [reset = FFh]

LED7\_BRIGHTNESS is shown in 図 7-27 and described in 表 7-20.

Return to 表 7-4.

## 図 7-27. LED7\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
	LED7_Brightness						
			R/ W	-FFh			

#### 表 7-20. LED7 BRIGHTNESS Register Field Descriptions

		_		•
Bit	Field	Туре	Reset	Description
7–0	LED7_Brightness	R/W	FFh	FFh = 100% of full intensity
				 80h = 50% of full intensity
				 00h = 0% of full intensity

#### 7.6.16 OUT0\_COLOR (Address = 0Fh) [reset = 00h]

OUT0\_COLOR is shown in 図 7-28 and described in 表 7-21.

Return to 表 7-4.

#### 図 7-28. OUT0\_COLOR Register



#### 表 7-21. OUT0\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT0_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				00h = The color mixing percentage is 0%.

# 7.6.17 OUT1\_COLOR (Address = 10h) [reset = 00h]

OUT1\_COLOR is shown in 図 7-29 and described in 表 7-22.

Return to 表 7-4.

## 図 7-29. OUT1\_COLOR Register

7	6	5	4	3	2	1	0		
OUT1_Color									
	R/ ₩-00h								

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## 表 7-22. OUT1\_COLOR Register Field Descriptions

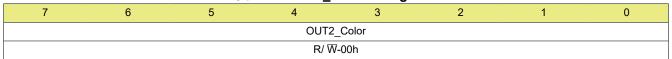
Bit	Field	Туре	Reset	Description
7–0	OUT1_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				80h =The color mixing percentage is 50%.
				00h = The color mixing percentage is 0%.

## 7.6.18 OUT2\_COLOR (Address = 11h) [reset = 00h]

OUT2\_COLOR is shown in 図 7-30 and described in 表 7-23.

Return to 表 7-4.

# 図 7-30. OUT2\_COLOR Register



## 表 7-23. OUT2\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT2_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
			00h = The color mixing percentage is 0%.	

## 7.6.19 OUT3\_COLOR (Address = 12h) [reset = 00h]

OUT3\_COLOR is shown in 図 7-31 and described in 表 7-24.

Return to 表 7-4.

## 図 7-31. OUT3\_COLOR Register



#### 表 7-24. OUT3\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description	
7–0	OUT3_Color	R/W	00h	FFh = The color mixing percentage is 100%.	
				80h =The color mixing percentage is 50%.	
			00h = The color mixing percentage is 0%.		

# 7.6.20 OUT4\_COLOR (Address = 13h) [reset = 00h]

OUT4\_COLOR is shown in 図 7-32 and described in 表 7-25.

Return to 表 7-4.

#### 図 7-32. OUT4\_COLOR Register

7	6	5	4	3	2	1	0				
OUT4_Color											
	R/ W-00h										

English Data Sheet: SLVSEB8



# 表 7-25. OUT4\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description	
7–0	OUT4_Color	R/W	00h	FFh = The color mixing percentage is 100%.	
				80h =The color mixing percentage is 50%.	
				00h = The color mixing percentage is 0%.	

## 7.6.21 OUT5\_COLOR (Address = 14h) [reset = 00h]

OUT5\_COLOR is shown in 図 7-33 and described in 表 7-26.

Return to 表 7-4.

# 図 7-33. OUT5\_COLOR Register

7	6	5 4 3 2		2	1	0					
OUT5_Color											
	R/ W-00h										

# 表 7-26. OUT5\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description		
7–0	OUT5_Color	R/W	00h	FFh = The color mixing percentage is 100%.		
				80h =The color mixing percentage is 50%.		
			00h = The color mixing percentage is 0%.			

## 7.6.22 OUT6\_COLOR (Address = 15h) [reset = 00h]

OUT6\_COLOR is shown in  $\boxtimes$  7-34 and described in  $\not\equiv$  7-27.

Return to 表 7-4.

## 図 7-34. OUT6\_COLOR Register



#### 表 7-27. OUT6\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description	
7–0	OUT6_Color	R/W	00h	FFh = The color mixing percentage is 100%.	
				80h =The color mixing percentage is 50%.	
			00h = The color mixing percentage is 0%.		

# 7.6.23 OUT7\_COLOR (Address = 16h) [reset = 00h]

OUT7\_COLOR is shown in 図 7-35 and described in 表 7-28.

Return to 表 7-4.

#### 図 7-35. OUT7 COLOR Register

		_								
7	6 5 4				2	1	0			
OUT7_Color										
			R/ ₩	7-00h						

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#### 表 7-28. OUT7\_COLOR Register Field Descriptions

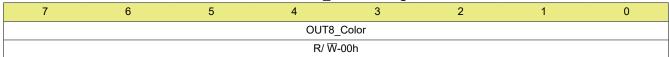
Bit	Field	Туре	Reset	Description
7–0	OUT7_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## 7.6.24 OUT8\_COLOR (Address = 17h) [reset = 00h]

OUT8\_COLOR is shown in 図 7-36 and described in 表 7-29.

Return to 表 7-4.

#### 図 7-36. OUT8\_COLOR Register



# 表 7-29. OUT8\_COLOR Register Field Descriptions

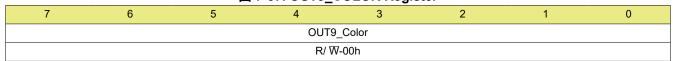
Bit	Field	Туре	Reset	Description	
7–0	OUT8_Color	R/W	00h	FFh = The color mixing percentage is 100%.	
				80h =The color mixing percentage is 50%.	
			00h = The color mixing percentage is 0%.		

## 7.6.25 OUT9\_COLOR (Address = 18h) [reset = 00h]

OUT9\_COLOR is shown in  $\boxtimes$  7-37 and described in  $\not\equiv$  7-30.

Return to 表 7-4.

# 図 7-37. OUT9\_COLOR Register



#### 表 7-30. OUT9\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description	
7–0	OUT9_Color	R/W	00h	FFh = The color mixing percentage is 100%.	
				 80h =The color mixing percentage is 50%.	
			00h = The color mixing percentage is 0%.		

# 7.6.26 OUT10\_COLOR (Address = 19h) [reset = 00h]

OUT10\_COLOR is shown in 図 7-38 and described in 表 7-31.

Return to 表 7-4.

## 図 7-38. OUT10\_COLOR Register

7	6	5	4	3	2	1	0				
OUT10_Color											
	R/ ₩-00h										

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#### 表 7-31. OUT10 COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT10_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

# 7.6.27 OUT11\_COLOR (Address = 1Ah) [reset = 00h]

OUT11\_COLOR is shown in 図 7-39 and described in 表 7-32.

Return to 表 7-4.

# 図 7-39. OUT11\_COLOR Register

7	6	5	4	3	2	1	0		
OUT11_Color									
	R/ ₩-00h								

#### 表 7-32. OUT11\_COLOR Register Field Descriptions

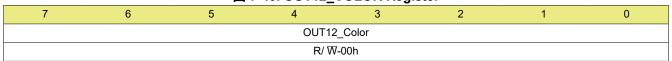
Bit	Field	Туре	Reset	Description
7–0	OUT11_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## 7.6.28 OUT12\_COLOR (Address = 1Bh) [reset = 00h]

OUT12\_COLOR is shown in 図 7-40 and described in 表 7-33.

Return to 表 7-4.

#### 図 7-40. OUT12\_COLOR Register



#### 表 7-33. OUT12\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT12_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

# 7.6.29 OUT13\_COLOR (Address = 1Ch) [reset = 00h]

OUT13\_COLOR is shown in 図 7-41 and described in 表 7-34.

Return to 表 7-4.

## 図 7-41. OUT13\_COLOR Register

7	6	5	4	3	2	1	0		
OUT13_Color									
R/ W-00h									

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# 表 7-34. OUT13\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT13_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				80h =The color mixing percentage is 50%.
				00h = The color mixing percentage is 0%.

## 7.6.30 OUT14\_COLOR (Address = 1Dh) [reset = 00h]

OUT14\_COLOR is shown in 図 7-42 and described in 表 7-35.

Return to 表 7-4.

# 図 7-42. OUT14\_COLOR Register

7	6	5 4		3	2	1	0		
OUT14_Color									
R/ W̄-00h									

# 表 7-35. OUT14\_COLOR Register Field Descriptions

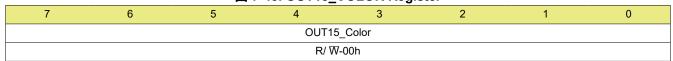
Bit	Field	Туре	Reset	Description
7–0	OUT14_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## 7.6.31 OUT15\_COLOR (Address = 1Eh) [reset = 00h]

OUT15\_COLOR is shown in 図 7-43 and described in 表 7-36.

Return to 表 7-4.

#### 図 7-43. OUT15\_COLOR Register



#### 表 7-36. OUT15\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT15_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## 7.6.32 OUT16\_COLOR (Address = 1Fh) [reset = 00h]

OUT16\_COLOR is shown in 図 7-44 and described in 表 7-37.

Return to 表 7-4.

## 図 7-44. OUT16\_COLOR Register

7	6	5	4	3	2	1	0			
OUT16_Color										
R/ W-00h										

English Data Sheet: SLVSEB8



### 表 7-37. OUT16\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT16_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				00h = The color mixing percentage is 0%.

## 7.6.33 OUT17\_COLOR (Address = 20h) [reset = 00h]

OUT17\_COLOR is shown in 図 7-45 and described in 表 7-38.

Return to 表 7-4.

### 図 7-45. OUT17\_COLOR Register

7	6	5	4	3	2	1	0
			OUT17	_Color			
			R/ W	<i>ī</i> -00h			

### 表 7-38. OUT17\_COLOR Register Field Descriptions

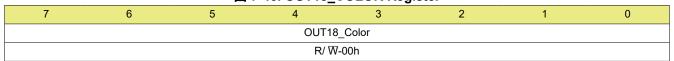
Bit	Field	Туре	Reset	Description
7–0	OUT17_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

### 7.6.34 OUT18\_COLOR (Address = 21h) [reset = 00h]

OUT18\_COLOR is shown in 図 7-46 and described in 表 7-39.

Return to 表 7-4.

### 図 7-46. OUT18\_COLOR Register



### 表 7-39. OUT18\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT18_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

# 7.6.35 OUT19\_COLOR (Address = 22h) [reset = 00h]

OUT19\_COLOR is shown in 図 7-47 and described in 表 7-40.

Return to 表 7-4.

### 図 7-47. OUT19\_COLOR Register

7	6	5	4	3	2	1	0	
	OUT19_Color							
			R/W	-00h				

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# 表 7-40. OUT19\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT19_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

### 7.6.36 OUT20\_COLOR (Address = 23h) [reset = 00h]

OUT20\_COLOR is shown in 図 7-48 and described in 表 7-41.

Return to 表 7-4.

### 図 7-48. OUT20\_COLOR Register

7	6	5	4	3	2	1	0
			OUT20	)_Color			
			R/ W	7-00h			

### 表 7-41. OUT20\_COLOR Register Field Descriptions

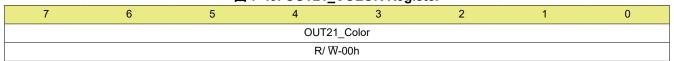
Bit	Field	Туре	Reset	Description
7–0	OUT20_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

### 7.6.37 OUT21\_COLOR (Address = 24h) [reset = 00h]

OUT21\_COLOR is shown in 図 7-49 and described in 表 7-42.

Return to 表 7-4.

### 図 7-49. OUT21\_COLOR Register



### 表 7-42. OUT21\_COLOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7–0	OUT21_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				 80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

# 7.6.38 OUT22\_COLOR (Address = 25h) [reset = 00h]

OUT22\_COLOR is shown in 図 7-50 and described in 表 7-43.

Return to 表 7-4.

# 図 7-50. OUT22\_COLOR Register

7	6	5	4	3	2	1	0	
	OUT22_Color							
			R/ W	7-00h				

English Data Sheet: SLVSEB8

# 表 7-43. OUT22\_COLOR Register Field Descriptions

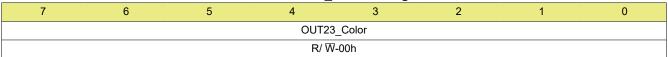
Bit	Field	Туре	Reset	Description
7–0	OUT22_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

## 7.6.39 OUT23\_COLOR (Address = 26h) [reset = 00h]

OUT23\_COLOR is shown in 図 7-51 and described in 表 7-44.

Return to 表 7-4.

### 図 7-51. OUT23\_COLOR Register



### 表 7-44. OUT23\_COLOR Register Field Descriptions

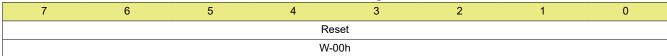
Bit	Field	Туре	Reset	Description
7–0	OUT23_Color	R/W	00h	FFh = The color mixing percentage is 100%.
				80h =The color mixing percentage is 50%.
				 00h = The color mixing percentage is 0%.

### 7.6.40 RESET (Address = 27h) [reset = 00h]

RESET is shown in  $\boxtimes$  7-52 and described in  $\not\equiv$  7-45.

Return to 表 7-4.

### 図 7-52. RESET Register



### 表 7-45. OUT14\_COLOR Register Field Descriptions

Bit Field		Туре	Reset	Description
7–0	Reset	W	00h	FFh = Reset all the registers to default value.

English Data Sheet: SLVSEB8

# 8 Application and Implementation

注

以下のアプリケーション情報は、TIの製品仕様に含まれるものではなく、TIではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The LP50xx device is an 18- or 24-channel constant-current-sink LED driver. The LP50xx device improves the user experience in color mixing and intensity control, for both live effects and coding effort. The optimized performance for RGB LEDs makes it a good choice for human-machine interaction applications.

### 8.2 Typical Application

The LP50xx design supports up to four devices in parallel with different configurations on the ADDR0 and ADDR1 pins.

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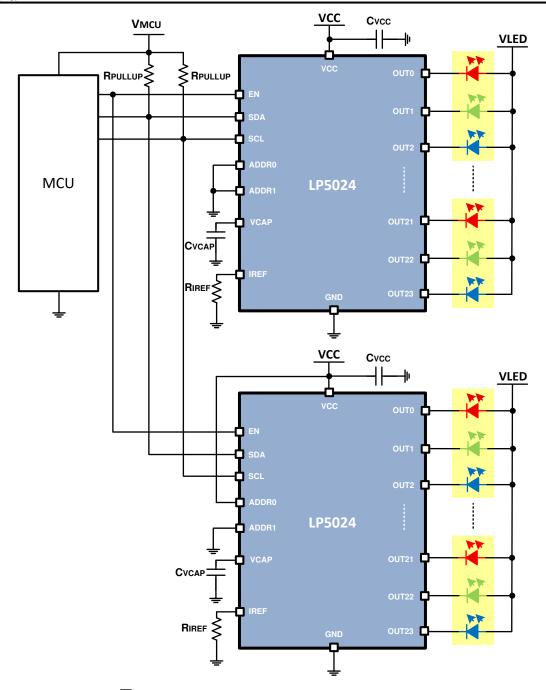


図 8-1. Driving Dual LP5024 Application Example

#### 8.2.1 Design Requirements

Set the LED current to 15mA using the R<sub>IREF</sub> resistor.

### 8.2.2 Detailed Design Procedure

LP50xx scales up the reference current ( $I_{REF}$ ) set by the external resistor ( $R_{IREF}$ ) to sink the output current ( $I_{OUT}$ ) at each output port. The following formula can be used to calculate the external resistor ( $R_{IREF}$ ):

$$R_{IREF} = K_{IREF} \times \frac{V_{IREF}}{I_{SET}}$$
 (2)



The SCL and SDA lines must each have a pullup resistor placed somewhere on the line (the pullup resistors are normally located on the bus master). In typical applications, values of  $1.8k\Omega$  to  $4.7k\Omega$  are used.

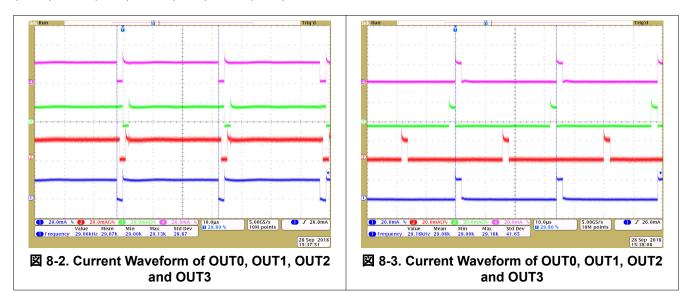
VCAP is internal LDO output pin. This pin must be connected through a 1µF capacitor to GND. Place the capacitor as close to the device as possible.

TI recommends having a 1µF capacitor between VCC and GND to ensure proper operation. Place the capacitor as close to the device as possible.

#### 8.2.3 Application Curves

The test condition for Figure 9-2 is that the testing is under bank control, using the following register values: 0x02 (0xFF), 0x04 (0xA0), 0x05 (0xA0), 0x06 (0xA0).

The test condition for Figure 9-2 is that the testing is under bank control, using the following register values: 0x02 (0xFF), 0x04 (0x10), 0x05 (0x10), 0x06 (0x10).



### 8.3 Power Supply Recommendations

The device is designed to operate from a  $V_{VCC}$  input-voltage supply range between 2.7V and 5.5V. This input supply must be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even in a load-transition condition (start-up or rapid intensity change). The resistance of the input supply rail must be low enough that the input-current transient does not cause a drop below a 2.7V level in the LP50xx  $V_{VCC}$  supply voltage.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

To prevent thermal shutdown, the junction temperature,  $T_J$ , must be less than  $T_{(TSD)}$ . If the voltage drop across the output channels is high, the device power dissipation can be large. The LP50xx device has very good thermal performance because of the thermal pad design; however, the PCB layout is also very important to ensure that the device has good thermal performance. Good PCB design can optimize heat transfer, which is essential for the long-term reliability of the device.

Use the following guidelines when designing the device layout:

• Place the  $C_{VCAP}$ ,  $C_{VCC}$  and  $R_{IREF}$  as close to the device as possible. Also, TI recommends to put the ground plane as  $\boxtimes$  8-4,  $\boxtimes$  8-5 and  $\boxtimes$  8-6.

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- www.ti.com/ja-jp
- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through copper on the PCB. Maximum copper density is extremely important when no heat sinks are attached to the PCB on the other side from the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- Use either plated-shut or plugged and capped vias for all the thermal vias on both sides of the board to prevent solder voids.

### 8.4.2 Layout Examples

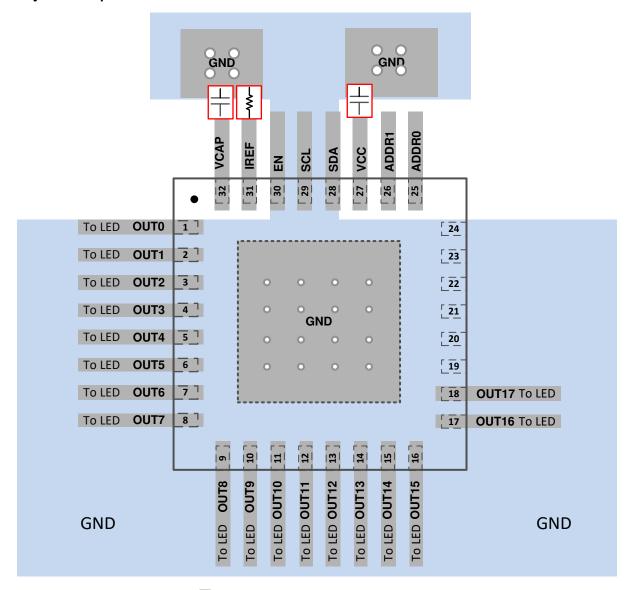


図 8-4. LP5018 VQFN Layout Example



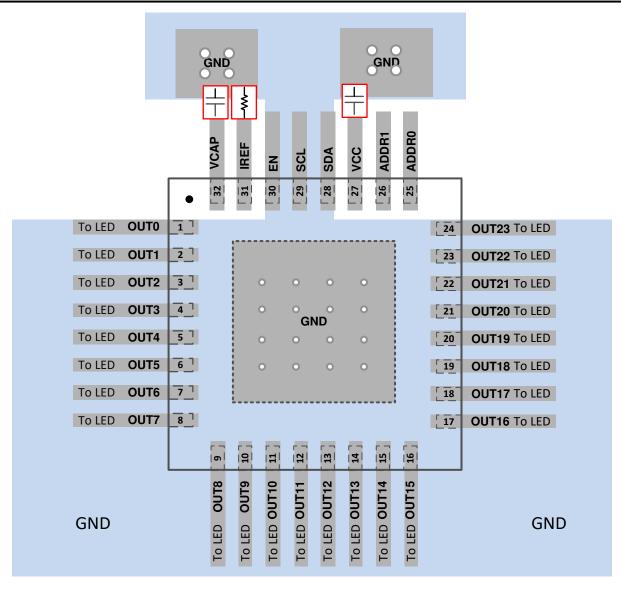


図 8-5. LP5024 VQFN Layout Example



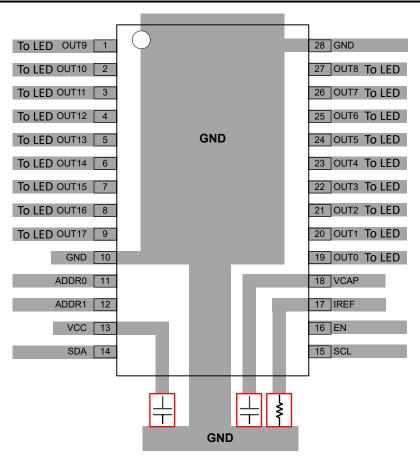


図 8-6. LP5018 VSSOP Layout Example for Single Layer PCB

45

Product Folder Links: LP5018 LP5024

# 9 Device and Documentation Support

#### 9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	ORDER NOW TECHNICAL DOCUMENTS		SUPPORT & COMMUNITY	
LP5018	Click here	Click here	Click here	Click here	Click here	
LP5024	Click here	Click here	Click here	Click here	Click here	

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 9.6 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

English Data Sheet: SLVSEB8



# **10 Revision History**

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (October 2018) to Revision C (July 2024)	Page
<ul><li>ドキュメント全体にわたって表、図、相互参照の採番方法を更新</li></ul>	1
• LP5018 VSSOP (28) パッケージを追加	
Added pin configuration image for LP5018 VSSOP	4
Added LP5018 VSSOP thermal information	<mark>7</mark>
Updated Bank Number and LED Number Assignment	
Updated description of OUTX_COLOR registers throughout	<mark>23</mark>
• Updated the description in 表 7-21 through 表 7-44	31
Removed the last sentence in the Layout Guidelines section	42
Added LP5018 VSSOP layout example	
Changes from Revision A (October 2018) to Revision B (October 2018)	Page
Added % after 100 in Parameter for I <sub>ERR DD</sub> and I <sub>ERR CC</sub> under OUTPUT STAGE	8
Changed value of "K <sub>IREF</sub> = 100" to "K <sub>IREF</sub> = 105"	17
Changes from Revision * (October 2018) to Revision A (October 2018)	Page
<ul><li>初版リリース</li></ul>	



# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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Product Folder Links: LP5018 LP5024

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17-Jun-2025

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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LP5018DGSR	Active	Production	VSSOP (DGS)   28	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP5018
LP5018DGSR.A	Active	Production	VSSOP (DGS)   28	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP5018
LP5018RSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LP 5018
LP5018RSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP 5018
LP5018RSMRG4	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP 5018
LP5018RSMRG4.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP 5018
LP5024RSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	LP 5024
LP5024RSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP 5024
LP5024RSMRG4	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP 5024
LP5024RSMRG4.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP 5024

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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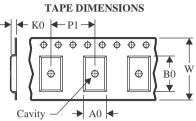
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**PACKAGE MATERIALS INFORMATION** 

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5018DGSR	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
LP5018RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LP5018RSMRG4	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LP5024RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LP5024RSMRG4	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



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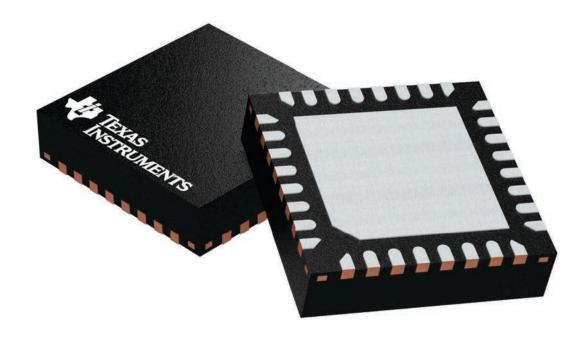
#### \*All dimensions are nominal

7 till dillitoriolorio di o riorimilar							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5018DGSR	VSSOP	DGS	28	5000	353.0	353.0	32.0
LP5018RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
LP5018RSMRG4	VQFN	RSM	32	3000	367.0	367.0	35.0
LP5024RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
LP5024RSMRG4	VQFN	RSM	32	3000	367.0	367.0	35.0

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

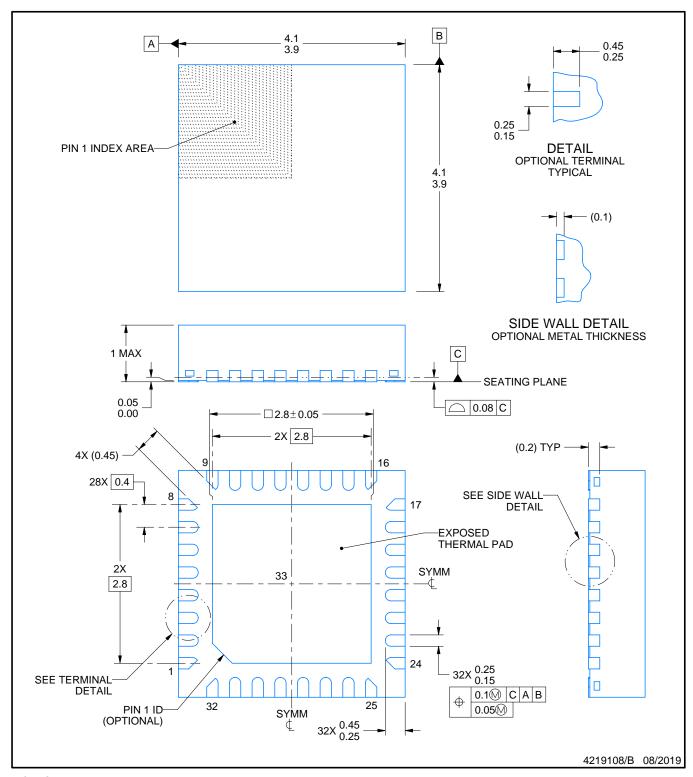
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.







PLASTIC QUAD FLATPACK - NO LEAD



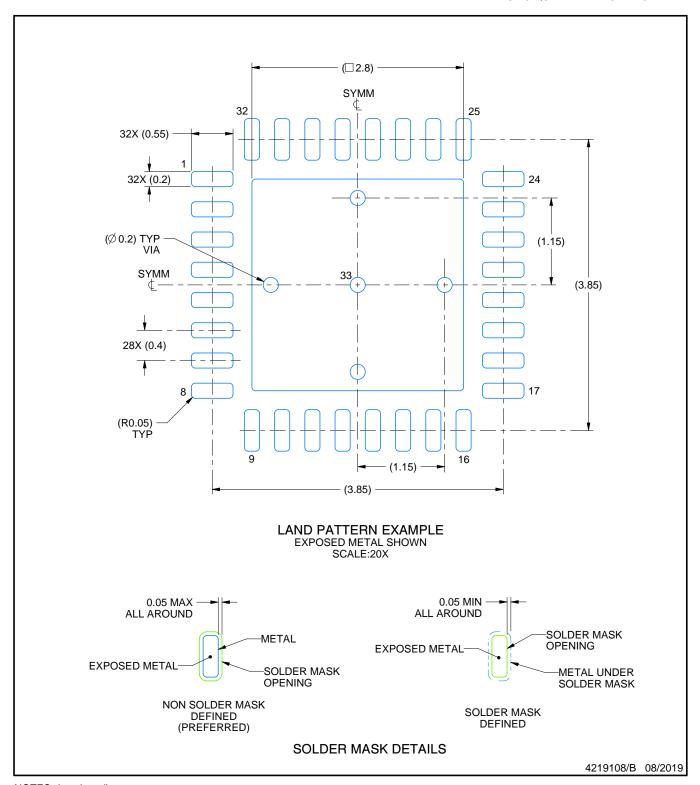
### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

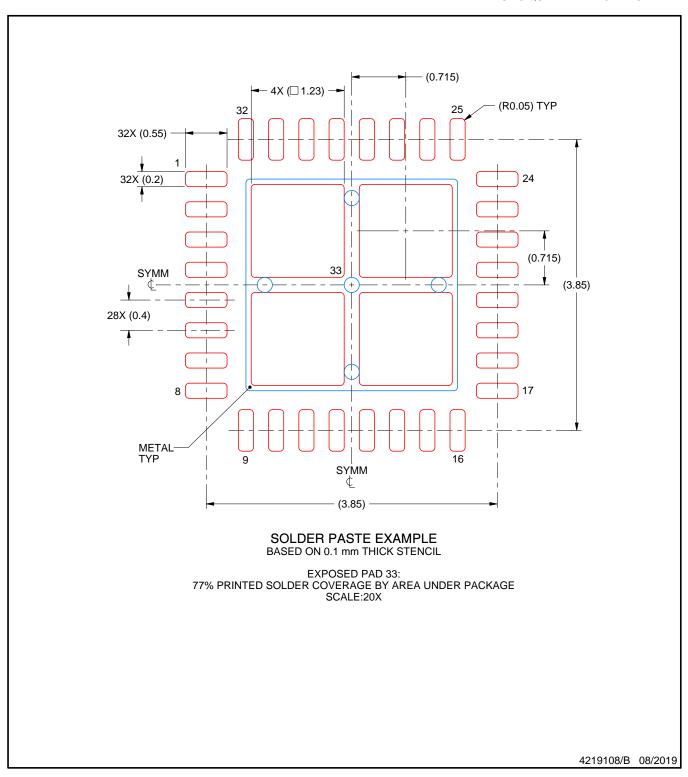


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



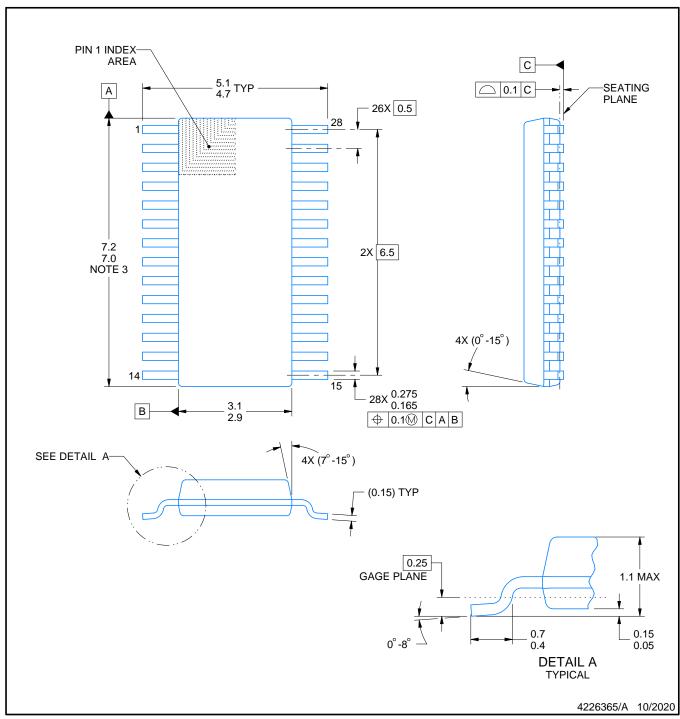
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



#### NOTES:

PowerPAD is a trademark of Texas Instruments.

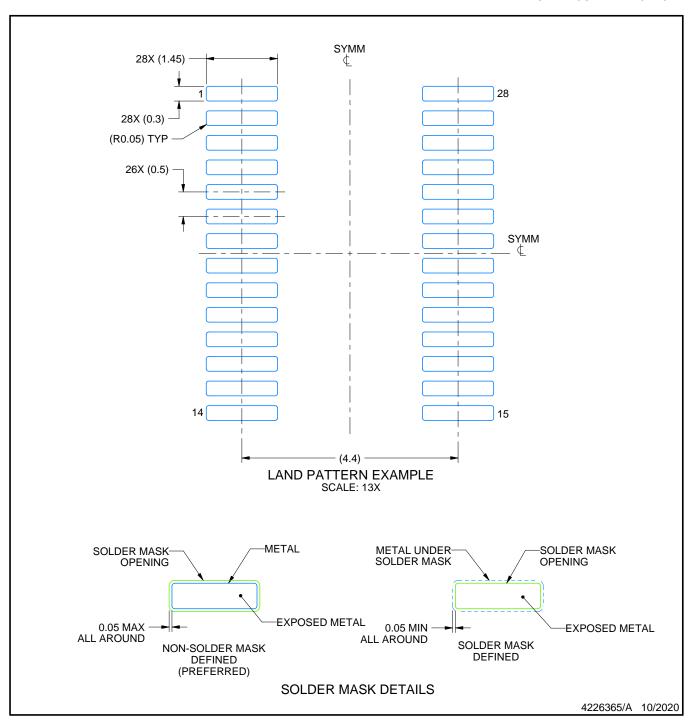
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.



SMALL OUTLINE PACKAGE

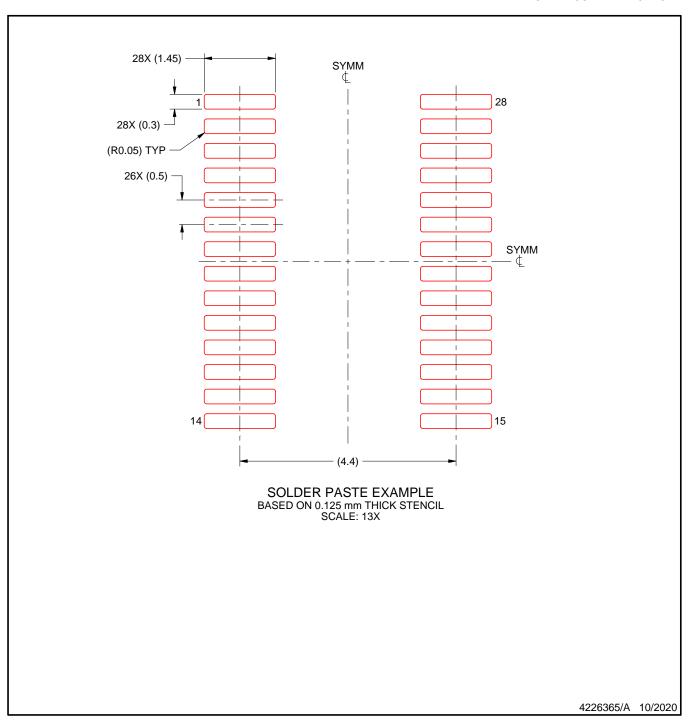


#### NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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