# LP2980-N マイクロパワー、50mA、超低ドロップアウトレギュレータ、SOT-23 パッケージ

## 1 特長

- $V_{IN}$ 範囲 (新チップ):2.5V ～ 16V
- $V_{OUT}$ 範囲 (新チップ):
  - 1.2V ～ 5.0V (固定、100mV 刻み)
- $V_{OUT}$ 精度:
  - ±0.5% (A グレードの従来チップ)
  - ±1% (標準グレードの従来チップ)
  - ±0.5% (A グレードおよび標準グレードの新チップ)
- 負荷および温度範囲にわたる出力精度:±1% (新チップ)
- 出力電流:最大 50mA
- 低い $I_Q$ (新チップ):69µA ($I_{LOAD}$ = 0mA の場合)
- 低い $I_Q$ (新チップ):380µA ($I_{LOAD}$ = 50mA の場合)
- シャットダウン電流と温度との関係:
  - 0.01µA (標準値) (従来チップ)
  - 1.12µA (標準値) (新チップ)
- 出力電流制限および過熱保護
- 2.2µF のセラミック コンデンサで安定 (新しいチップ)
- 高 PSRR (新チップ):
  - 1kHz で 75dB、1MHz で 45dB
- 動作時接合部温度:-40℃ ～ +125℃
- パッケージ:5 ピン SOT-23 (DBV)

## 2 アプリケーション

- 住宅用ブレーカ
- ソリッド・ステート・ドライブ (SSD)
- 電気メーター
- 電化製品
- ビル・オートメーション

## 3 概要

LP2980-N は、固定出力で入力範囲の広い、低ドロップアウト (LDO) の電圧レギュレータで、2.5V～16V の入力電圧範囲、最大 50mA の負荷電流に対応します。LP2980-N は、1.2V～5.0V の出力範囲をサポートしています (新チップ)。

さらに、LP2980-N (新チップ) は、負荷および温度の全範囲にわたって 1% の出力精度を備えており、低電圧マイクロコントローラ (MCU) およびプロセッサのニーズを満たすことができます。

新チップの広帯域の PSRR 特性は、1kHz で 75dB、1MHz で 45dB であり、上流の DC/DC コンバータのスイッチング周波数を減衰して、レギュレータ後のフィルタ処理を最小化できます。

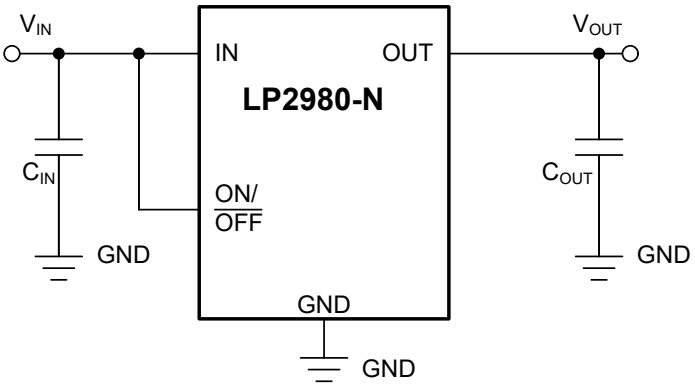
内部ソフトスタート時間および電流制限保護により、スタートアップ時の突入電流が減少し、入力静電容量を最小化しました。過電流および過熱保護などの一般的な保護機能を備えています。

LP2980-N は 5 ピン、2.9mm × 1.6mm の SOT-23 (DBV) パッケージで供給されます。

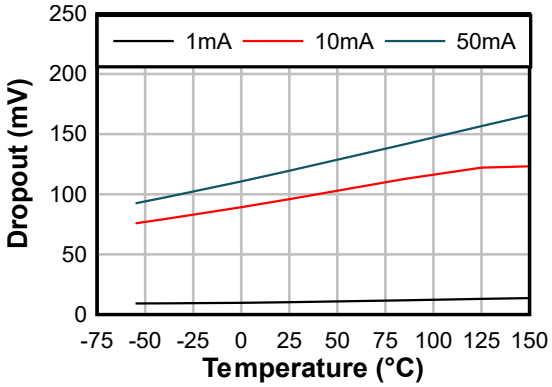
**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| LP2980-N | DBV (SOT-23、5) | 2.9mm × 2.8mm |

(1) 詳細については、*メカニカル、パッケージ、および注文情報*をご覧ください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。




代表的なアプリケーション回路




ドロップアウト電圧と温度との関係 (新チップ)

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## 4 Pin Configuration and Functions

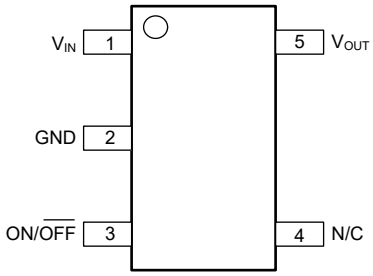



**図 4-1. DBV Package, 5-Pin SOT-23 (Top View)**

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IN | I | Input supply pin. Use a capacitor with a value of 1µF or larger from this pin to ground. See the *Input Capacitor Requirements* section for more information. |
| 2 | GND | — | Common ground (device substrate). |
| 3 | ON/$\overline{\text{OFF}}$ | I | Enable pin for the LDO. Driving the ON/$\overline{\text{OFF}}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. Tie this pin to $V_{IN}$ if unused. |
| 4 | N/C | — | *Do not connect.* Device pin 4 is reserved for post packaging test and calibration of the LP2980-N VOUT accuracy. Leave device pin 4 floating. Do not connect this pin to any potential. Do not connect to ground. Any attempt to perform pin continuity testing on device pin 4 is discouraged. Continuity test results are variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 4 activates the trim circuitry, thus forcing VOUT to move out of tolerance. |
| 5 | OUT | O | Output of the regulator. Use a capacitor with a value of 2.2µF or larger from this pin to ground(2). See the *Input Capacitor Requirements* section for more information. |

(1) I = Input, O = Output.
(2) The nominal output capacitance must be greater than 1µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1µF.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Continuous input voltage range (for legacy chip) | –0.3 | 16 | V |
| | Continuous input voltage range (for new chip) | –0.3 | 18 | |
| $V_{OUT}$ | Output voltage range (for legacy chip) | –0.3 | 9 | V |
| | Output voltage range (for new chip) | –0.3 | $V_{IN}$ + 0.3 or 9 (whichever is smaller) | |
| $V_{ON/\overline{OFF}}$ | ON/$\overline{OFF}$ pin voltage range (for legacy chip) | –0.3 | 16 | V |
| | ON/$\overline{OFF}$ pin voltage range (for new chip) | –0.3 | 18 | |
| Current | Maximum output | Internally limited | | A |
| Temperature | Operating junction, $T_J$ | –55 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.

## 5.2 ESD Ratings

| | | | VALUE (Legacy Chip) | VALUE (New Chip) | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | ±3000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | ±1000 | |

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage (for legacy chip) | 2.2 | | 16 | V |
| | Supply input voltage (for new chip) | 2.5 | | 16 | V |
| $V_{OUT}$ | Output voltage (for legacy chip) | 1.2 | | 10.0 | V |
| | Output voltage (for new chip) | 1.2 | | 5 | V |
| $V_{ON/\overline{OFF}}$ | Enable voltage (for legacy chip) | 0 | | $V_{IN}$ | V |
| | Enable voltage (for new chip) | 0 | | 16 | V |
| $I_{OUT}$ | Output current | 0 | | 50 | mA |
| $C_{IN}$ (1) | Input capacitor | | 1 | | µF |
| $C_{OUT}$ | Output capacitor (for legacy chip)(4) | 2.2 | 4.7 | | |
| | Output capacitance (for new chip) (1) | 1 | 2.2 | 200 | |
| $C_{OUT}$ ESR(2) | Output capacitor ESR (for new chip)(3) | 0 | | 1 | Ω |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.
(2) Maximum supported ESR range for new chip is 1Ω. For output capacitor with higher ESR values, place a low ESR MLCC capacitor with value of 100nF, close to the output pin of the LDO.
(3) Details related to supported ESR range for the legacy chip are available in *Recommended Capacitors for the Legacy Chip*.

(4) For legacy chip a minimum value of 2.2µF is usually needed when using multilayer ceramic capacitors. A minimum value of 1µF is usually needed with surface-mount solid tantalum capacitors.

## 5.4 Thermal Information

| THERMAL METRIC (2) (1) | | Legacy Chip DBV (SOT23-5) 5 PINS | New Chip DBV (SOT23-5) 5 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 205.4 | 178.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 78.8 | 77.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 46.7 | 47.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.3 | 15.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 46.3 | 46.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

## 5.5 Electrical Characteristics

specified at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{ON/OFF}$ = 2 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 2.2 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Output voltage tolerance | $I_L$ = 1mA | Legacy chip (standard grade) | −1.0 | | 1.0 | % |
| | | | Legacy chip (A grade) | −0.5 | | 0.5 | |
| | | | New chip | −0.5 | | 0.5 | |
| | | 1 mA ≤ $I_L$ ≤ 50 mA | Legacy chip (standard grade) | −1.5 | | 1.5 | |
| | | | Legacy chip (A grade) | −0.75 | | 0.75 | |
| | | | New chip | −0.5 | | 0.5 | |
| | | 1 mA ≤ $I_L$ ≤ 50 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip (standard grade) | −3.5 | | 3.5 | |
| | | | Legacy chip (A grade) | −2.5 | | 2.5 | |
| | | | New chip | −1.0 | | 1.0 | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation | $V_{O(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V | Legacy chip | | 0.007 | 0.014 | %/V |
| | | | New chip | | 0.002 | 0.014 | |
| | | $V_{O(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 0.007 | 0.032 | |
| | | | New chip | | 0.002 | 0.032 | |

## 5.5 Electrical Characteristics (続き)

specified at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{ON/OFF}$ = 2 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 2.2 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ - $V_{OUT}$ | Dropout voltage[1] | $I_{OUT}$ = 0 mA | Legacy chip | | 1 | 3 | mV |
| | | | New chip | | 1 | 2.75 | |
| | | $I_{OUT}$ = 0 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 5 | |
| | | | New chip | | | 3 | |
| | | $I_{OUT}$ = 1 mA | Legacy chip | | 7 | 10 | |
| | | | New chip | | 11.5 | 14 | |
| | | $I_{OUT}$ = 1 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 15 | |
| | | | New chip | | | 17 | |
| | | $I_{OUT}$ = 10 mA | Legacy chip | | 40 | 60 | |
| | | | New chip | | 98 | 115 | |
| | | $I_{OUT}$ = 10 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 90 | |
| | | | New chip | | | 148 | |
| | | $I_{OUT}$ = 50 mA | Legacy chip | | 120 | 150 | |
| | | | New chip | | 120 | 145 | |
| | | $I_{OUT}$ = 50 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 225 | |
| | | | New chip | | | 184 | |

## 5.5 Electrical Characteristics (続き)

specified at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{ON/OFF}$ = 2 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 2.2 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GND}$ | GND pin current | $I_{OUT}$ = 0 mA | Legacy chip | | 65 | 95 | uA |
| | | | New chip | | 69 | 95 | |
| | | $I_{OUT}$ = 0 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 65 | 125 | |
| | | | New chip | | | 120 | |
| | | $I_{OUT}$ = 1 mA | Legacy chip | | 75 | 110 | |
| | | | New chip | | 78 | 110 | |
| | | $I_{OUT}$ = 1 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 170 | |
| | | | New chip | | | 140 | |
| | | $I_{OUT}$ = 10 mA | Legacy chip | | 120 | 220 | |
| | | | New chip | | 175 | 210 | |
| | | $I_{OUT}$ = 10 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 400 | |
| | | | New chip | | | 250 | |
| | | $I_{OUT}$ = 50 mA | Legacy chip | | 350 | 600 | |
| | | | New chip | | 380 | 440 | |
| | | $I_{OUT}$ = 50 mA, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | | 900 | |
| | | | New chip | | | 650 | |
| | | $V_{ON/OFF}$ < 0.18 V, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 0 | 1 | |
| | | | New chip | | 1.12 | 2.25 | |
| $V_{UVLO+}$ | Rising bias supply UVLO | $V_{IN}$ rising, –40°C ≤ $T_J$ ≤ 125°C | New chip | | 2.2 | 2.4 | V |
| $V_{UVLO-}$ | Falling bias supply UVLO | $V_{IN}$ falling, –40°C ≤ $T_J$ ≤ 125°C | | 1.9 | 2.07 | | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | –40°C ≤ $T_J$ ≤ 125°C | | | 0.130 | | |
| $I_{O(SC)}$ | Short output current | $R_L$ = 0 Ω (steady state) | Legacy chip | | 150 | | mA |
| | | | New chip | | 150 | | |
| IO(PK) | Peak output current | $V_{OUT}$ ≥ $V_{O(NOM)}$ –5% (steady state) | Legacy chip | 110 | 150 | | |
| | | | New chip | 110 | 150 | | |
| $V_{ON/\overline{OFF}}$ | ON/$\overline{OFF}$ input voltage | Low = Output OFF, $V_{OUT}$ + 1 ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 0.55 | 0.18 | V |
| | | | New chip | | | 0.15 | |
| | | High = Output ON, $V_{OUT}$ + 1 ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | 1.6 | 1.4 | | |
| | | | New chip | 1.6 | | | |
| $I_{ON/\overline{OFF}}$ | ON/OFF input current | $V_{ON/OFF}$ = 0 V, $V_{OUT}$ + 1 ≤ $V_{IN}$ ≤ 16 V,–40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 0 | -1 | uA |
| | | | New chip | | | -0.9 | |
| | | $V_{ON/OFF}$ = 5 V, $V_{OUT}$ + 1 ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | Legacy chip | | 5 | 15 | |
| | | | New chip | | | 2.20 | |
| $\Delta V_O/\Delta V_{IN}$ | Ripple rejection | f = 1 kHz, $C_{OUT}$ = 10 µF | Legacy chip | | 63 | | dB |
| | | f = 1 kHz, $C_{OUT}$ = 10 µF | New chip | | 75 | | |
| | | f = 100 kHz, $I_{LOAD}$ = 50mA | New chip | | 45 | | |
| $V_n$ | Output noise voltage | Bandwidth = 300 Hz to 50 kHz, $C_{OUT}$ = 10uF, $V_{OUT}$ = 3.3V, $I_{LOAD}$ = 50mA | Legacy chip | | 160 | | µVRMS |
| | | Bandwidth = 300 Hz to 50 kHz, $C_{OUT}$ = 2.2uF, $V_{OUT}$ = 3.3V, $I_{LOAD}$ = 50mA | New chip | | 140 | | |
| | | Bandwidth = 10 Hz to 100 kHz, $C_{OUT}$ = 2.2uF, $V_{OUT}$ = 3.3V, $I_{LOAD}$ = 50mA | New chip | | 50 | | |

## 5.5 Electrical Characteristics (続き)

specified at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{ON/OFF}$ = 2 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 2.2 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $T_{sd+}$ | Thermal shutdown threshold | Shutdown, temperature increasing | New chip | | 170 | | °C |
| $T_{sd-}$ | | Reset, temperature decreasing | | | 150 | | |

(1) Dropout voltage ($V_{DO}$) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential. $V_{DO}$ is measured with $V_{IN}$ = $V_{OUT(nom)}$ - 100mV for fixed output devices.

## 5.6 Typical Characteristics

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

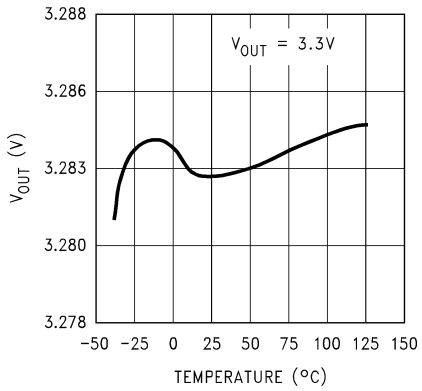
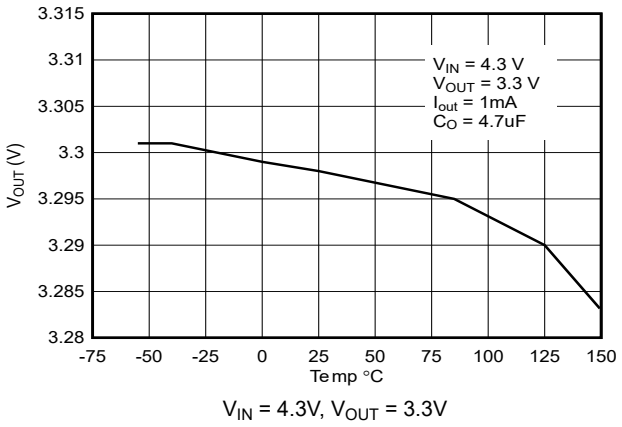



図 5-1. Output Voltage vs Temperature (Legacy Chip)




$V_{IN}$ = 4.3V, $V_{OUT}$ = 3.3V

図 5-2. Output Voltage vs Temperature (New Chip)

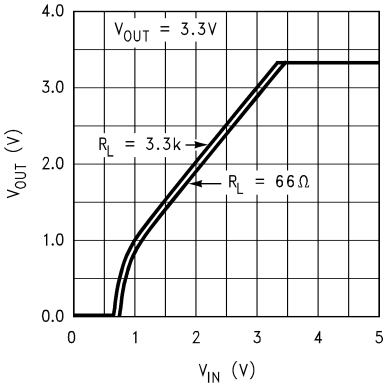



図 5-3. Output Voltage vs $V_{IN}$ (Legacy Chip)

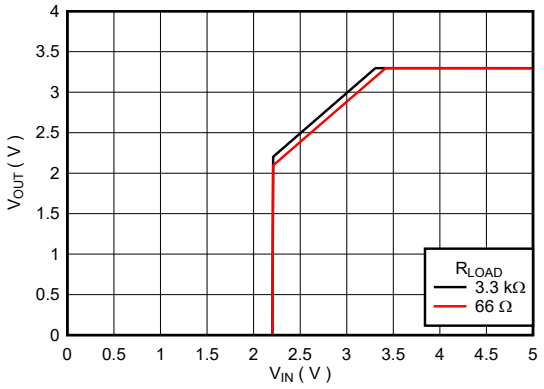



図 5-4. Output Voltage vs $V_{IN}$ (New Chip)

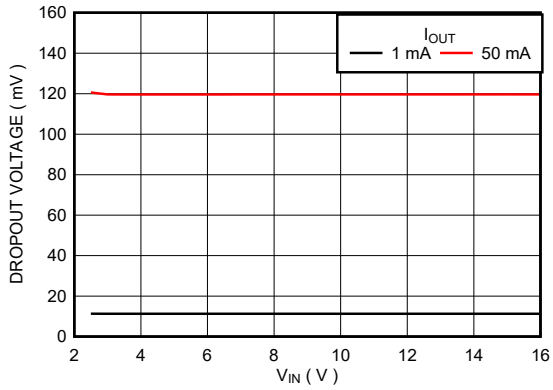



図 5-5. Dropout Voltage vs $V_{IN}$ (New Chip)

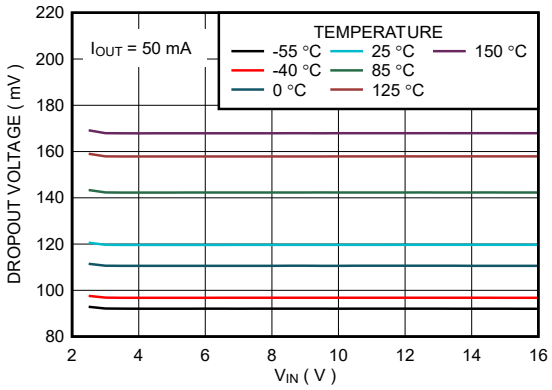



図 5-6. Dropout Voltage vs $V_{IN}$ and Temperature (New Chip)

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

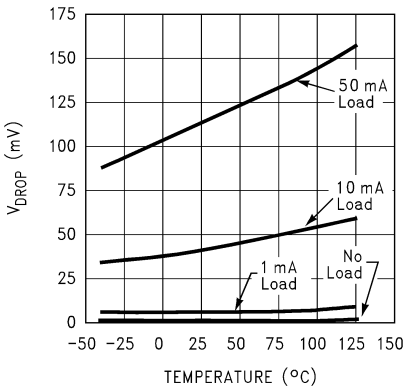



**図 5-7. Dropout Voltage vs Temperature (Legacy Chip)**

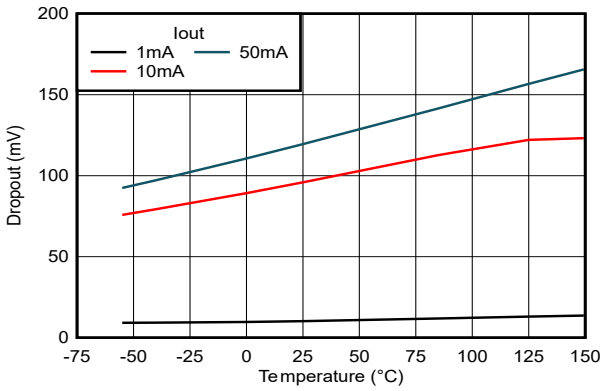



**図 5-8. Dropout Voltage vs Temperature (New Chip)**

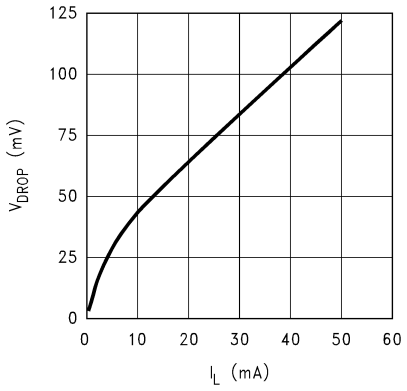



**図 5-9. Dropout Voltage vs Load Current (Legacy Chip)**

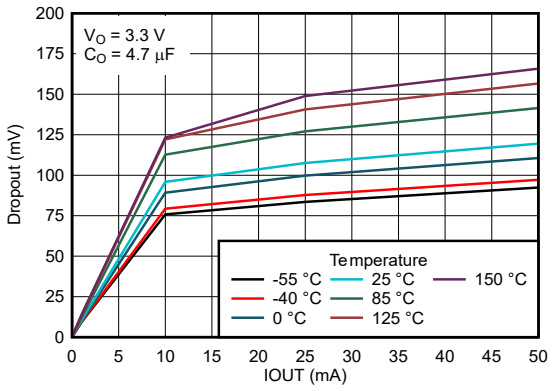



**図 5-10. Dropout Voltage vs Load Current (New Chip)**

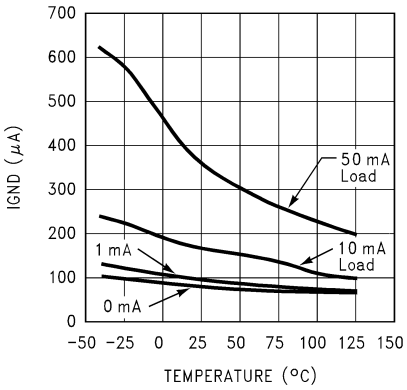



**図 5-11. Ground Pin Current vs Temperature (Legacy Chip)**

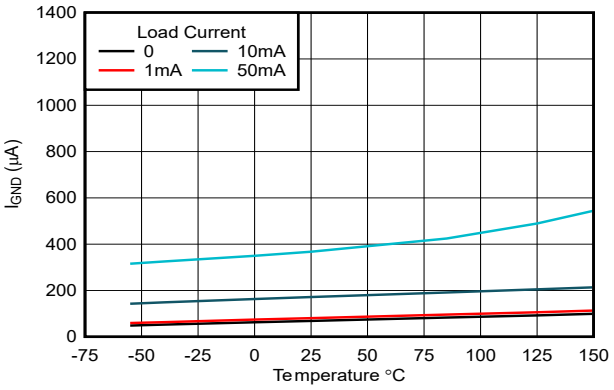



**図 5-12. Ground Pin Current vs Temperature (New Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

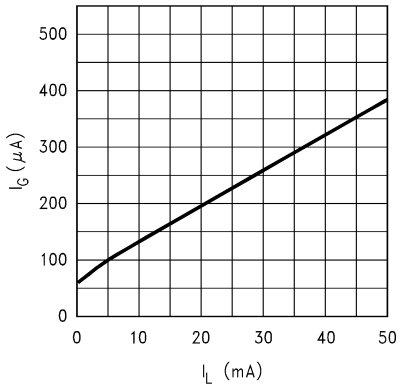



**図 5-13. Ground Pin Current vs Load Current (Legacy Chip)**

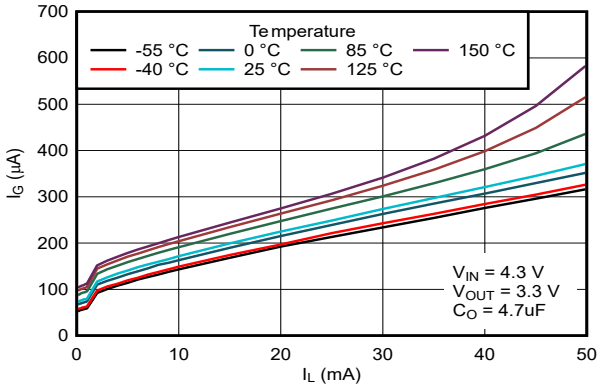



**図 5-14. Ground Pin Current vs Load Current (New Chip)**

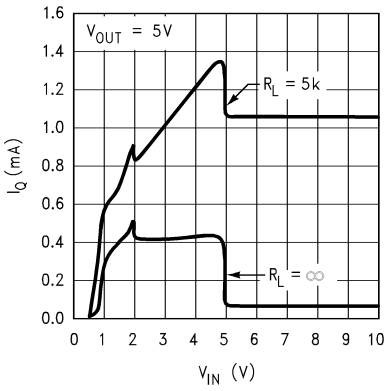



**図 5-15. Input Current vs $V_{IN}$ (Legacy Chip)**

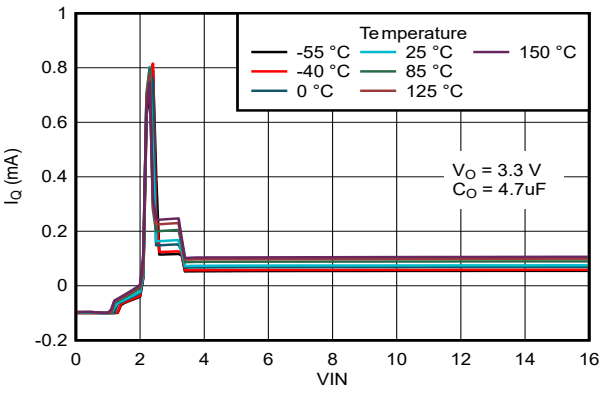



**図 5-16. Input Current vs Input Voltage (New Chip)**

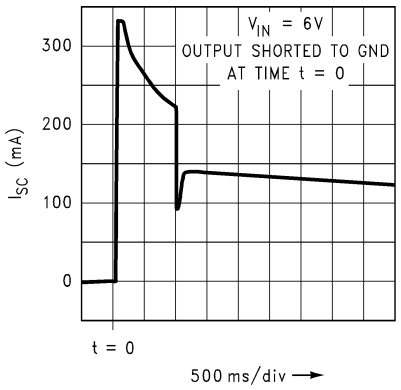



**図 5-17. Short-Circuit Current vs Time (Legacy Chip)**

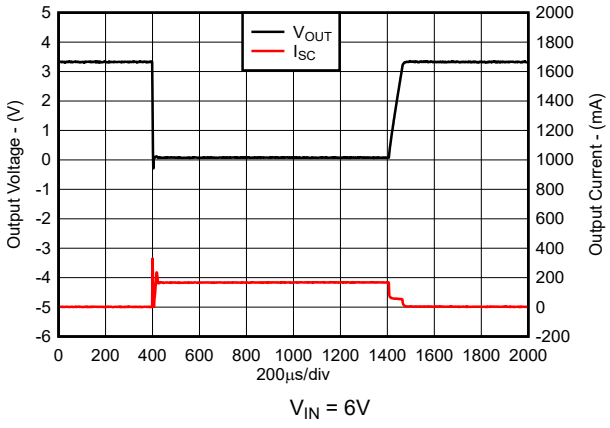



**図 5-18. Short-Circuit Current vs Time (New Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

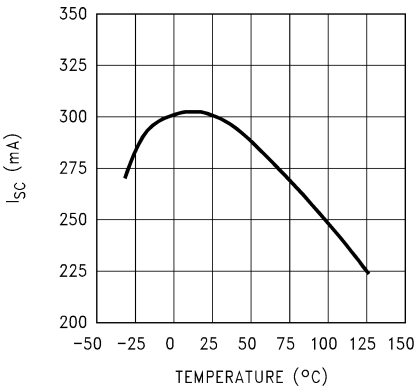



**図 5-19. Short-Circuit Current vs Temperature (Legacy Chip)**

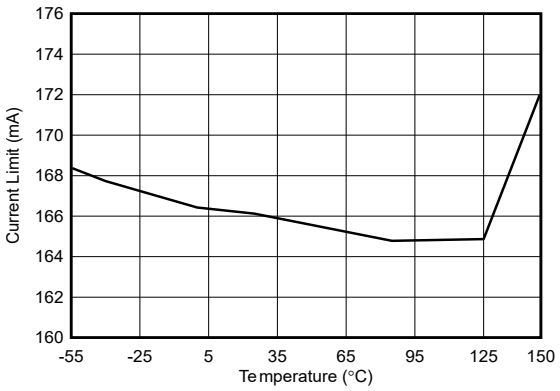



**図 5-20. Short-Circuit Current vs Temperature (New Chip)**

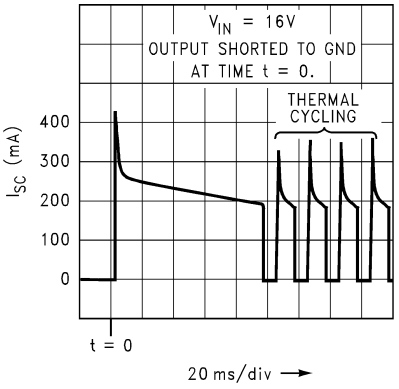



**図 5-21. Short-Circuit Current vs Time (Legacy Chip)**

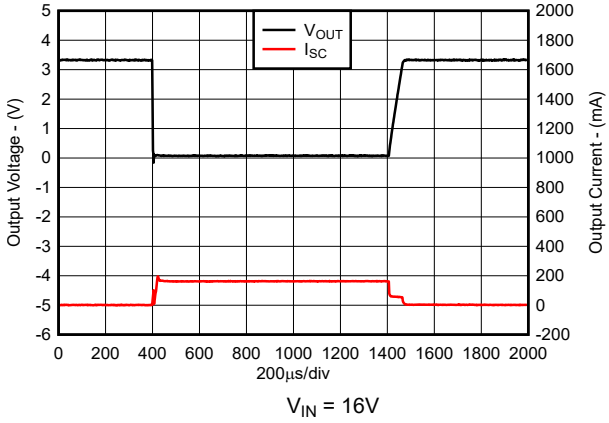



**図 5-22. Short-Circuit Current vs Time (New Chip)**

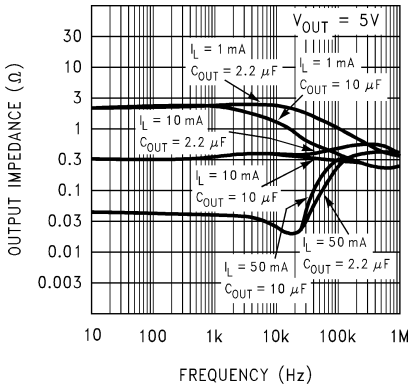



**図 5-23. Output Impedance vs Frequency (Legacy Chip)**

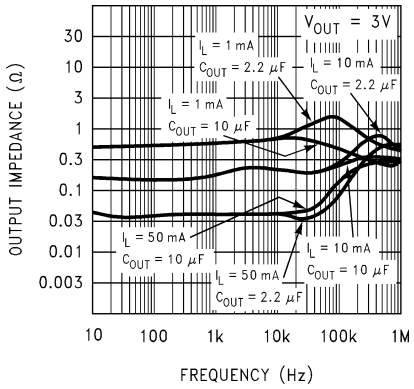



**図 5-24. Output Impedance vs Frequency (Legacy Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

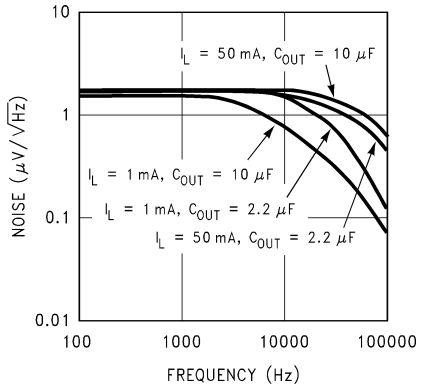
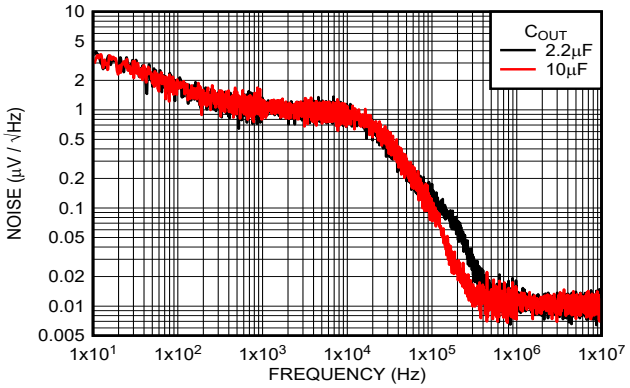
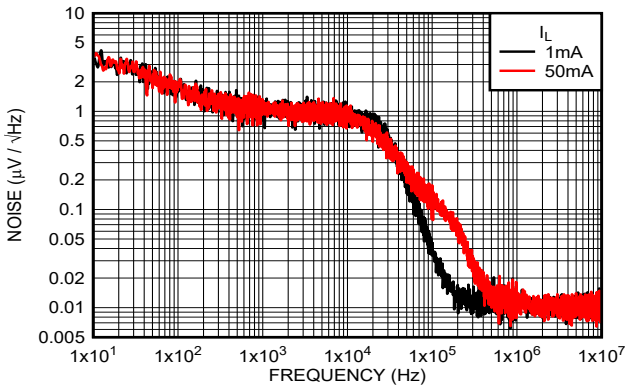



**図 5-25. Output Noise Density (Legacy Chip)**




$V_{OUT}$ = 3.3V, $I_{OUT}$ = 50mA

**図 5-26. Output Noise Density vs $C_{OUT}$ (New Chip)**




$V_{OUT}$ = 3.3V, $C_{OUT}$ = 2.2µF

**図 5-27. Output Noise Density vs $I_{OUT}$ (New Chip)**

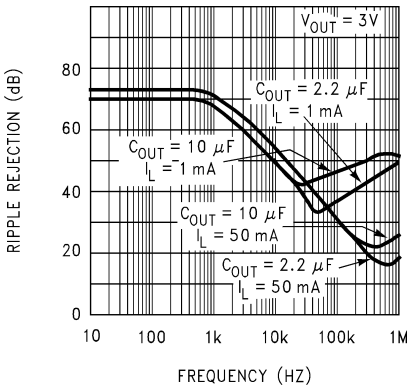
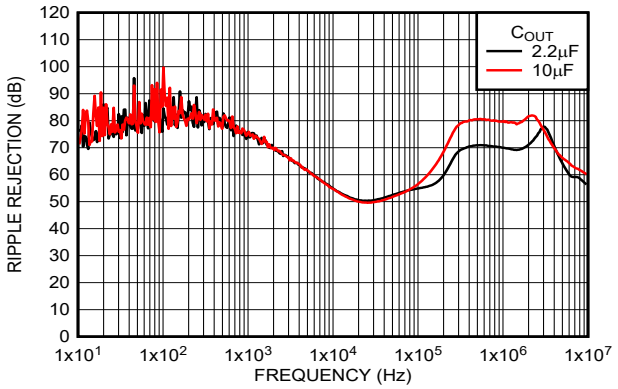
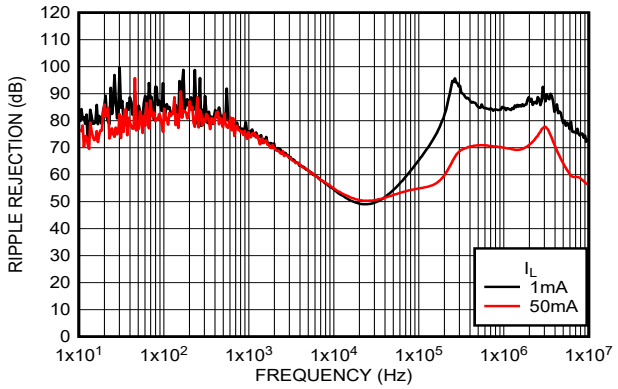



**図 5-28. Ripple Rejection (Legacy Chip)**




$V_{OUT}$ = 3.3V, $I_{OUT}$ = 50mA

**図 5-29. Ripple Rejection vs $C_{OUT}$ (New Chip)**




$V_{OUT}$ = 3.3V, $C_{OUT}$ = 2.2µF

**図 5-30. Ripple Rejection vs $I_{OUT}$ (New Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

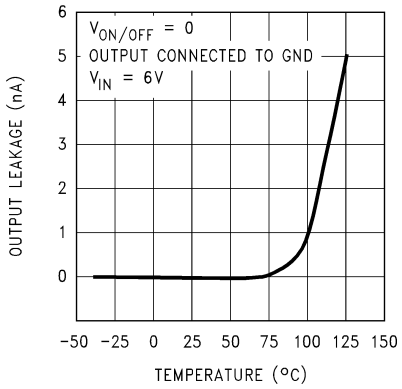



**図 5-31. Input to Output Leakage vs Temperature (Legacy Chip)**

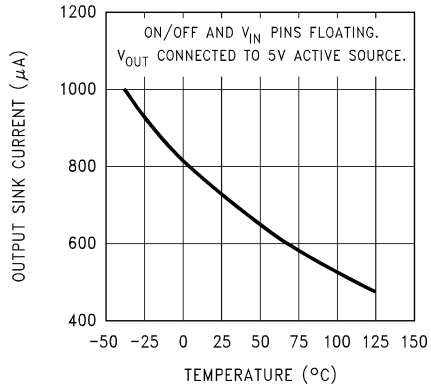



**図 5-32. Output Reverse Leakage vs Temperature (Legacy Chip)**

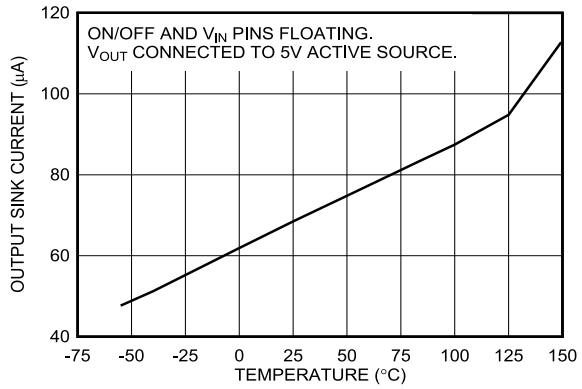



**図 5-33. Output Reverse Leakage vs Temperature (New Chip)**

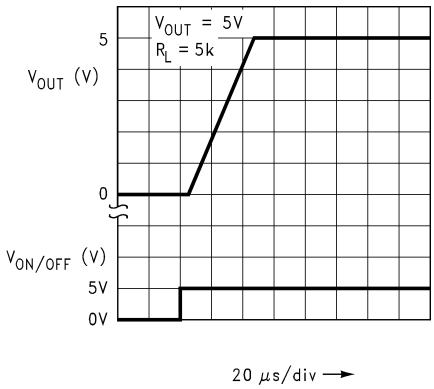
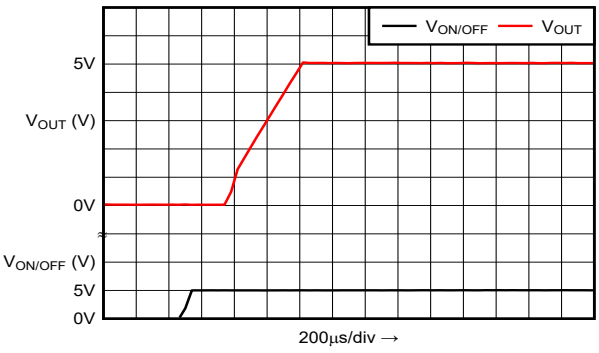



**図 5-34. Turn-On Waveform (Legacy Chip)**




VOUT = 3.3V, IOUT = 50mA

**図 5-35. Turn-On Waveform (New Chip)**

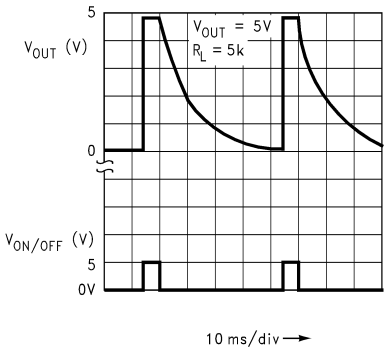
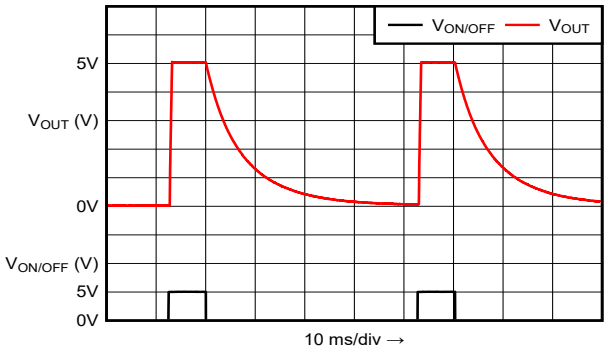



**図 5-36. Turnoff Waveform (Legacy Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)




$V_{OUT}$ = 3.3V, $I_{OUT}$ = 50mA

**図 5-37. Turnoff Waveform (New Chip)**

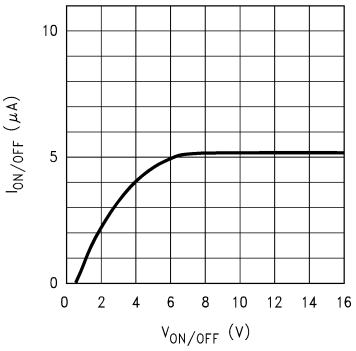
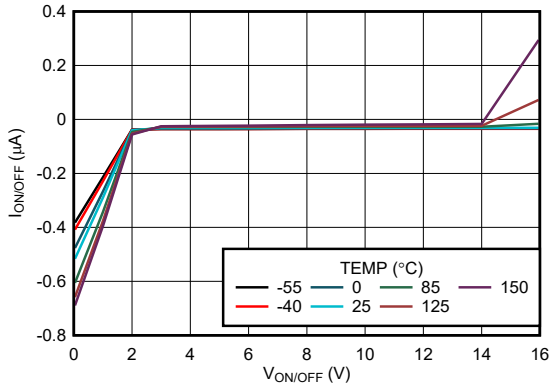
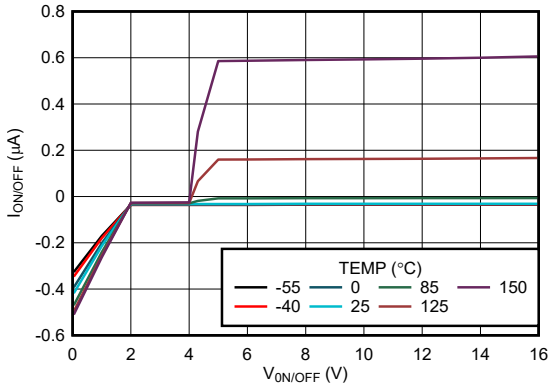



**図 5-38. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$ (Legacy Chip)**




$V_{IN}$ = 16V

**図 5-39. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$ (New Chip)**




$V_{IN}$ = 4.3V

**図 5-40. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$ (New Chip)**

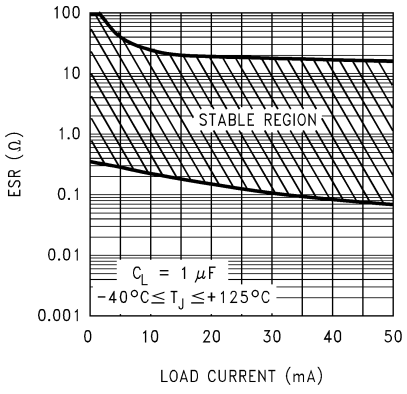



**図 5-41. 1µF ESR Range vs $I_{OUT}$ (Legacy Chip)**

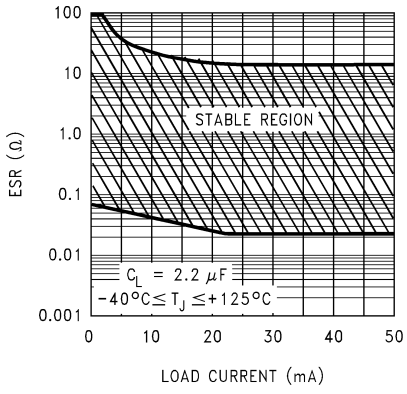



**図 5-42. 2.2µF ESR Range vs $I_{OUT}$ (Legacy Chip)**

## 5.6 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 2.2µF for the legacy chip, and $C_{OUT}$ = 4.7µF for the new chip (unless otherwise noted)

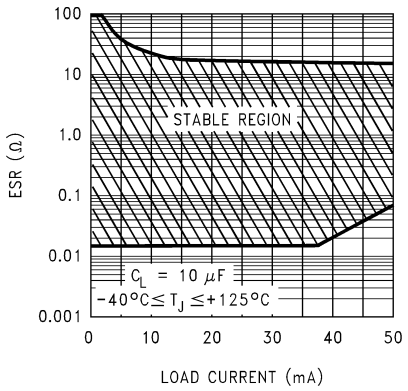



**図 5-43. 10µF ESR Range vs $I_{OUT}$ (Legacy Chip)**

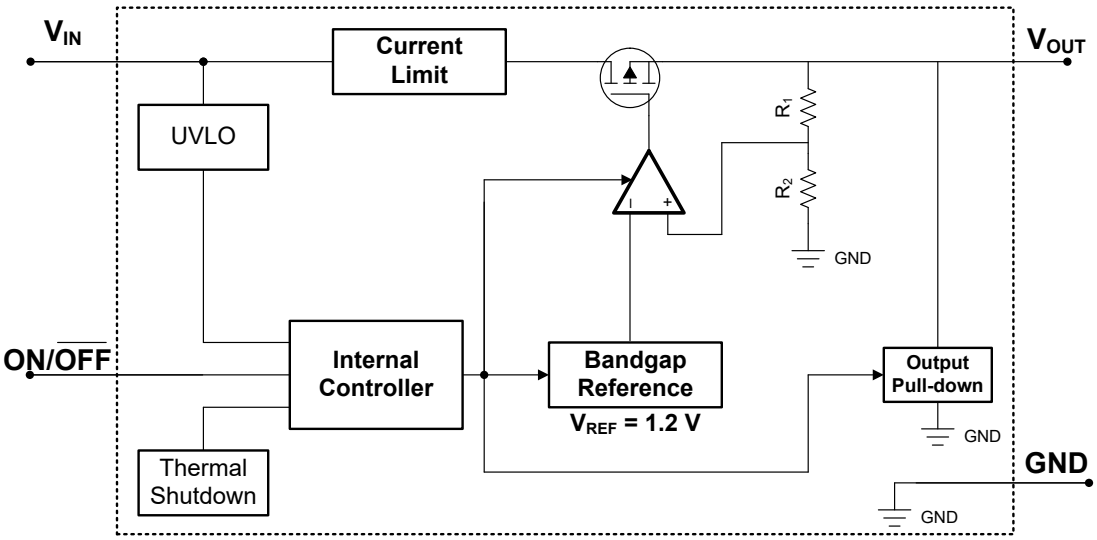
# 6 Detailed Description

## 6.1 Overview

The LP2980-N is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2980-N has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 50 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to +125°C.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled when the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

For the new chip, the device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin to actively discharge the output voltage.

### 6.3.2 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### 6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). $I_{CL}$ is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the current limit.

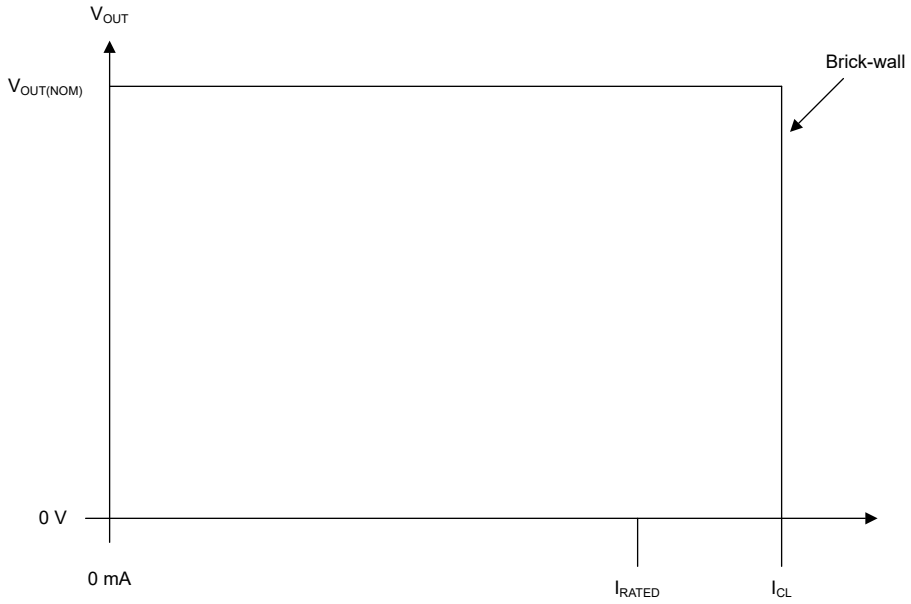



**図 6-1. Current Limit**

### 6.3.4 Undervoltage Lockout (UVLO)

For the new chip, the device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 6.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0V < $V_{IN}$ < $V_{UVLO}$

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

### 6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

## 6.4 Device Functional Modes

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)}$ + $V_{DO}$)
- The output current is less than the current limit ($I_{OUT}$ < $I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J$ < $T_{SD}$)
- The ON/$\overline{\text{OFF}}$ voltage has previously exceeded the ON/$\overline{\text{OFF}}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN}$ < $V_{OUT(NOM)}$ + $V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)}$ + $V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 6.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

# 7 Application and Implementation

注

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## 7.1 Application Information

### *7.1.1 Recommended Capacitor Types*

This section describes the recommended capacitors for both the new chip and the legacy chip.

#### 7.1.1.1 Recommended Output Capacitors (Legacy Chip)

The legacy chip version of the LP2980-N requires an output capacitor to maintain regulator loop stability. Select this capacitor to meet the requirements of minimum capacitance and equivalent series resistance (ESR) range. Because the acceptable capacitance and ESR ranges are wider than for most other LDOs, finding capacitors that meet the stability criteria of the LP2980-N is not difficult. Dynamic device performance also improves by using an output capacitor.

In general, make sure the capacitor value is at least 1µF (over the actual ambient operating temperature), and the ESR is within the range indicated in 図 5-41, 図 5-42, and 図 5-43. Although a maximum ESR is given in these figures, capacitors generally do not support such high ESR values.

##### *7.1.1.1.1 Tantalum Capacitors (Legacy Chip)*

Surface-mount solid tantalum capacitors offer a good combination of small physical size for the capacitance value, and an ESR in the range needed by the legacy chip version of the LP2980-N.

The results of testing the LP2980-N (legacy chip) stability with surface-mount solid tantalum capacitors show good stability with values of at least 1µF. Increase the value to 2.2µF (or more) for even better performance, including transient response and noise.

Small-value tantalum capacitors that are verified as appropriate for use with the LP2980-N (legacy chip) are shown in 表 7-1. Increase capacitance values without limit.

##### *7.1.1.1.2 Aluminum Electrolytic Capacitors (Legacy Chip)*

Although not a good choice for a production design, because of relatively large physical size, an aluminum electrolytic capacitor is able to be used in the design prototype for an LP2980-N regulator. Use a value of at least 1µF, and make sure the ESR meets the conditions of 図 5-41, 図 5-42, and 図 5-43. If the operating temperature drops below 0°C the regulator does not remain stable, because the ESR of the aluminum electrolytic capacitor increases and exceeds the limits indicated in 図 5-41, 図 5-42, and 図 5-43. 表 7-1 lists the available tantalum capacitors.

**表 7-1. Surface-Mount Tantalum Capacitor Selection Guide (Legacy Chip)**

| 1µF SURFACE-MOUNT TANTALUM CAPACITORS | |
|---|---|
| **MANUFACTURER** | **PART NUMBER** |
| Kemet | T491A105M010AS |
| NEC | NRU105M10 |
| Siemens | B45196-E3105-K |
| Nichicon | F931C105MA |
| Sprague | 293D105X0016A2T |
| **2.2µF SURFACE-MOUNT TANTALUM CAPACITORS** | |
| Kemet | T491A225M010AS |
| NEC | NRU225M06 |
| Siemens | B45196/2.2/10/10 |
| Nichicon | F930J225MA |
| Sprague | 293D225X0010A2T |

#### *7.1.1.1.3 Multilayer Ceramic Capacitors (Legacy Chip)*

Surface-mount multilayer ceramic capacitors are an attractive choice because of the relatively small physical size and excellent RF characteristics. However, these capacitors sometimes have ESR values lower than the minimum required by the LP2980-N (legacy chip), and relatively large capacitance change with temperature. Consult the manufacturer data sheet for the capacitor before selecting a value.

Test results of the LP2980-N (legacy chip) stability using multilayer ceramic capacitors show a minimum value of 2.2µF is typically needed for the 5V regulator. For lower output voltages, or better performance, use a higher value (such as 4.7µF).

表 7-2 lists multilayer ceramic capacitors that are verified as appropriate for use with the LP2980-N.

**表 7-2. Surface-Mount Multilayer Ceramic Capacitor Selection Guide (Legacy Chip)**

| 2.2µF SURFACE-MOUNT CERAMIC | |
|---|---|
| **MANUFACTURER** | **PART NUMBER** |
| Tokin | 1E225ZY5U-C203 |
| Murata | GRM42-6Y5V225Z16 |
| **4.7µF SURFACE-MOUNT CERAMIC** | |
| Tokin | 1E475ZY5U-C304 |

### 7.1.1.2 Recommended Output Capacitors (New Chip)

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Maximum supported ESR range across complete temperature (−40°C to +125°C) and load current range (0mA - 50mA) is less than 1Ω. For existing board implementations that use capacitors with higher ESR (for example: tantalum), place a low ESR MLCC capacitor with a value of 100nF as close as possible to the output ($V_{OUT}$) pin of the LP2980-N.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The output capacitors

listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 7.1.2 Input Capacitor Requirements

For the legacy chip, an input capacitor ($C_{IN}$) ≥1µF is required (the amount of capacitance can be increased without limit). Any good-quality tantalum or ceramic capacitor can be used. The capacitor must be located no more than half an inch from the input pin and returned to a clean analog ground.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

The input capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 7.1.3 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($\psi_{JT}$) and junction-to-board characterization parameter ($\psi_{JB}$). These parameters provide two methods for calculating the junction temperature ($T_J$), as described in the following equations. Use the junction-to-top characterization parameter ($\psi_{JT}$) with the temperature at the center-top of device package ($T_T$) to calculate the junction temperature. Use the junction-to-board characterization parameter ($\psi_{JB}$) with the PCB surface temperature 1 mm from the device package ($T_B$) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (2)$$

where:

- $P_D$ is the dissipated power
- $T_T$ is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (3)$$

where:

- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

### 7.1.4 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ($P_D$).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

### 7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

図 7-1 shows one approach for protecting the device.

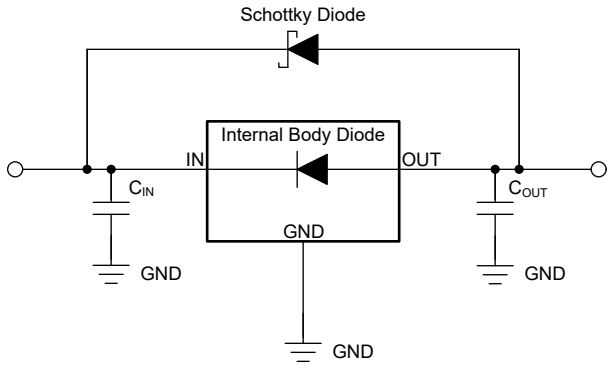
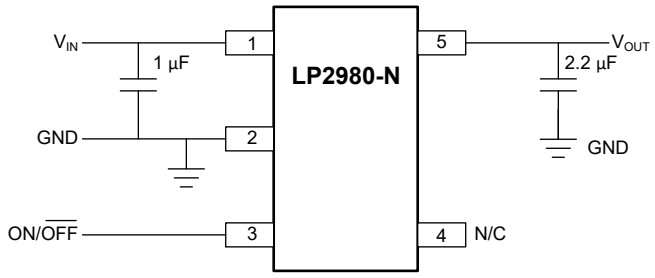



**図 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode**

## 7.2 Typical Application

図 7-2 shows the standard usage of the LP2980-N as a low-dropout regulator.




NOTE: Do not make connections to the NC pin.

**図 7-2. LP2980-N Typical Application**

### *7.2.1 Design Requirements*

For this design, use the minimum $C_{OUT}$ value for stability (which can be increased without limit for improved stability and transient response). The ON/$\overline{\text{OFF}}$ pin must be actively terminated. Connect this pin to $V_{IN}$ if the shutdown feature is not used.

For the new chip, 表 7-3 summarizes the design requirements for 図 7-2.

**表 7-3. Design Parameter**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 12 V |
| Output voltage | 3.3 V |
| Output current | 50 mA |

### *7.2.2 Detailed Design Procedure*

#### 7.2.2.1 ON/$\overline{\text{OFF}}$ Input Operation

The LP2980-N is shut off by driving the ON/OFF input low, and turned on by pulling the ON/OFF input high. If this feature is not used, the ON/OFF input must be tied to $V_{IN}$ to keep the regulator output on at all times (the ON/OFF input must not be left floating).

To provide proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on and turn-off voltage thresholds that specify an ON or OFF state (see the *Electrical Characteristics* table).

For the legacy chip, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate greater than 40mV/µs.

For the new chip, there is no restriction on the slew rate of the voltage signals applied to the ON/OFF input. Both fast and slow ramping voltage signals can be used to drive the ON/OFF pin.

注

For the legacy chip, the ON/OFF function does not operate correctly if a slow-moving signal is used to drive the ON/OFF input.

### 7.2.3 Application Curves

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), $I_{OUT}$ = 1mA, ON/$\overline{OFF}$ pin tied to $V_{IN}$, $C_{IN}$ = 1.0µF, and $C_{OUT}$ = 4.7µF (unless otherwise noted)

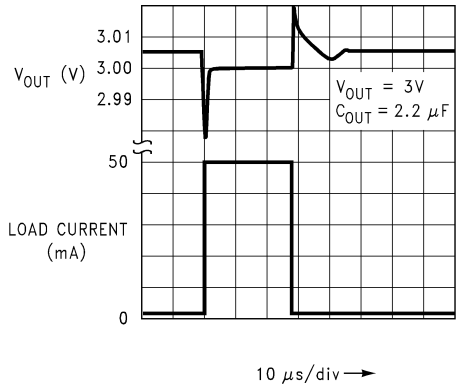
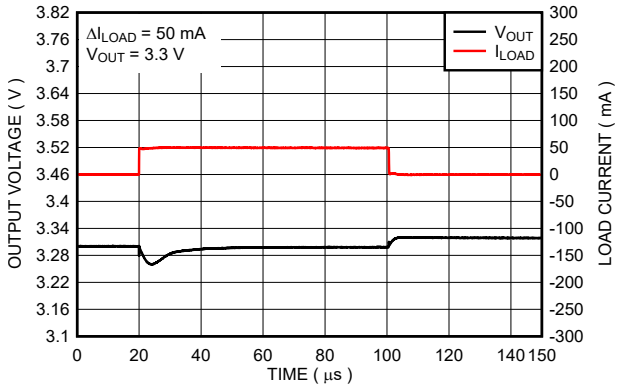
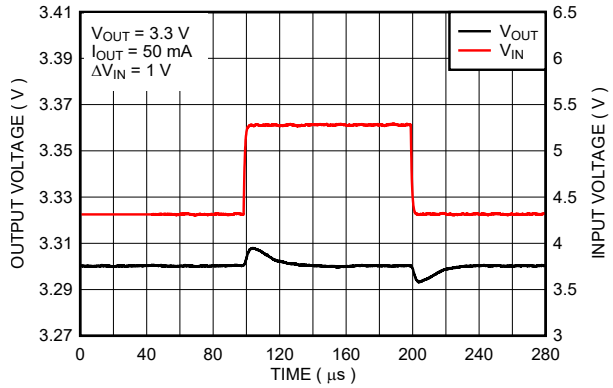



図 7-3. Load Transient Response (Legacy Chip)



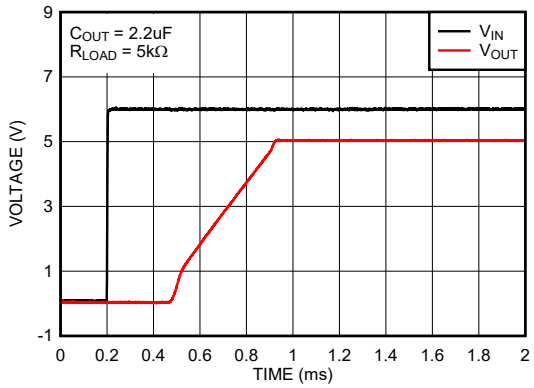

dI/dt = 1A/µs

図 7-4. Load Transient Response (New Chip)




$V_{OUT}$ = 3.3V, $\Delta V_{IN}$ = 1V, $I_{OUT}$ = 50mA, dV/dt = 1V/µs

図 7-5. Line Transient Response (New Chip)




$V_{OUT}$ = 5V, dV/dt = 1V/µs

図 7-6. Start-Up (New Chip)

## 7.3 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. Using vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. Use a ground reference plane that is either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage, shields noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

### *7.4.2 Layout Example*

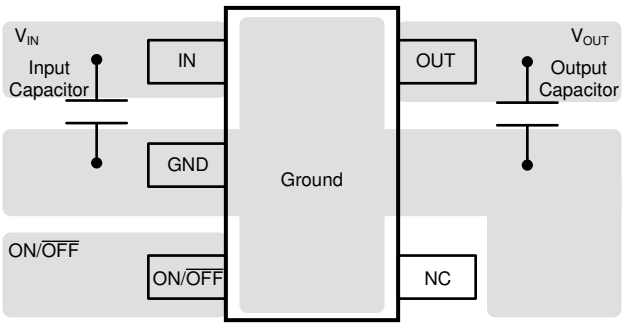



**図 7-7. LP2980-N Layout Example**

# 8 Device and Documentation Support

## 8.1 Device Support

### 8.1.1 サード・パーティ製品に関する免責事項

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### 8.1.2 Device Nomenclature

**表 8-1. Available Options**

| PRODUCT(1) | $V_{OUT}$ |
|---|---|
| LP2980**vwxxy-z.z**/NOPB | **v** is the accuracy specification for the legacy chip (*A* or blank). See the *Electrical Characteristics* for more information. This character is insignificant for the new chip.<br>**w** is the operating temperature range (I = −40°C to 125°C).<br>**xx** is the package designator (M5 = SOT-23).<br>**y** is the reel designator size. See the Package Addendum for more information on package quantity.<br>**z.z** is the nominal output voltage (for example, 3.3 = 3.3V; 5.0 = 5.0V).<br>**/NOPB** indicates material construction that does not use Lead (Pb).<br>This device ships with the legacy chip (CSO: DLN or GF8) or the new chip (CSO: RFB) which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the data sheet. |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## 8.2 ドキュメントの更新通知を受け取る方法

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## 8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision Q (November 2023) to Revision R (February 2025)** **Page**

- Changed description of N/C pin in *Pin Functions* table and added footnote 1 ... 2
- Added ESR range for output capacitor ... 3
- Changed *Short-Circuit Current vs Time (New Chip)*, *Short-Circuit Current vs Temperature (New Chip)*, *Short-Circuit Current vs Time (New Chip)* curves ... 8
- Added *1µF ESR Range vs IOUT (Legacy Chip)*, *2.2µF ESR Range vs IOUT (Legacy Chip)*, and *10µF ESR Range vs IOUT (Legacy Chip)* curves ... 8
- Added *Recommended Output Capacitors (Legacy Chip)* section ... 19
- Added *Tantalum Capacitors (Legacy Chip)* section ... 19
- Added *Aluminum Electrolytic Capacitors (Legacy Chip)* section ... 19
- Added *Multilayer Ceramic Capacitors (Legacy Chip)* section ... 20
- Changed *Recommended Output Capacitors (New Chip)* section ... 20
- Changed title and last paragraph of *Input Capacitor Requirements* section ... 21

**Changes from Revision P (August 2016) to Revision Q (November 2023)** **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 現在のファミリのフォーマットに合わせてドキュメント全体を変更 ... 1
- ドキュメントに M3 デバイスを追加 ... 1
- Updated *Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics* and *Thermal Information* for M3-suffix(new chip) ... 4
- Added *Device Nomenclature* section ... 26

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LP2980AIM5-2.5/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NA |
| LP2980AIM5-2.5/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NA |
| LP2980AIM5-3.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L02A |
| LP2980AIM5-3.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L02A |
| LP2980AIM5-3.3/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L00A |
| LP2980AIM5-3.3/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L00A |
| LP2980AIM5-4.7/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37A |
| LP2980AIM5-4.7/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37A |
| LP2980AIM5-5.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L01A |
| LP2980AIM5-5.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L01A |
| LP2980AIM5X-2.5/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NA |
| LP2980AIM5X-2.5/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NA |
| LP2980AIM5X-3.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L02A |
| LP2980AIM5X-3.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L02A |
| LP2980AIM5X-3.3/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L00A |
| LP2980AIM5X-3.3/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L00A |
| LP2980AIM5X-4.7/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37A |
| LP2980AIM5X-4.7/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37A |
| LP2980AIM5X-5.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L01A |
| LP2980AIM5X-5.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L01A |
| LP2980IM5-2.5/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NB |
| LP2980IM5-2.5/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NB |
| LP2980IM5-2.5/NOPB.B | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NB |
| LP2980IM5-3.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L02B |
| LP2980IM5-3.0/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L02B |
| LP2980IM5-3.3/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L00B |
| LP2980IM5-3.3/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L00B |
| LP2980IM5-3.8/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L21B |
| LP2980IM5-3.8/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L21B |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LP2980IM5-3.8/NOPB.B | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L21B |
| LP2980IM5-4.7/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37B |
| LP2980IM5-4.7/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37B |
| LP2980IM5-4.7/NOPB.B | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L37B |
| LP2980IM5-5.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L01B |
| LP2980IM5-5.0/NOPB.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L01B |
| LP2980IM5X-2.5/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NB |
| LP2980IM5X-2.5/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L0NB |
| LP2980IM5X-3.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L02B |
| LP2980IM5X-3.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L02B |
| LP2980IM5X-3.3/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L00B |
| LP2980IM5X-3.3/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L00B |
| LP2980IM5X-5.0/NO.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L01B |
| LP2980IM5X-5.0/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L01B |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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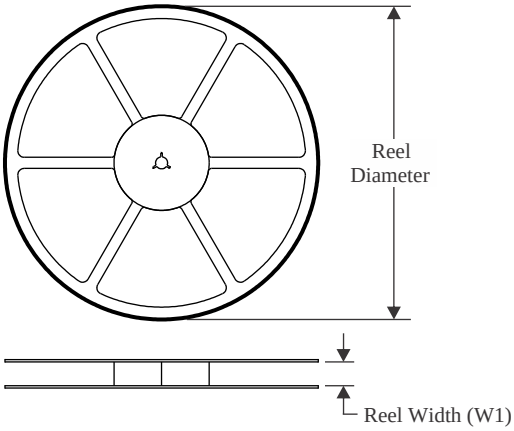
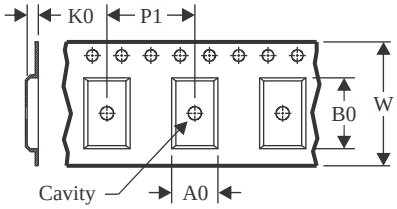
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

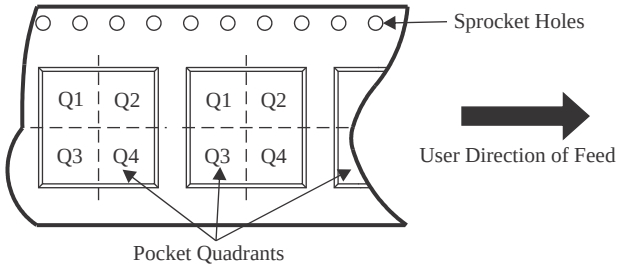



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

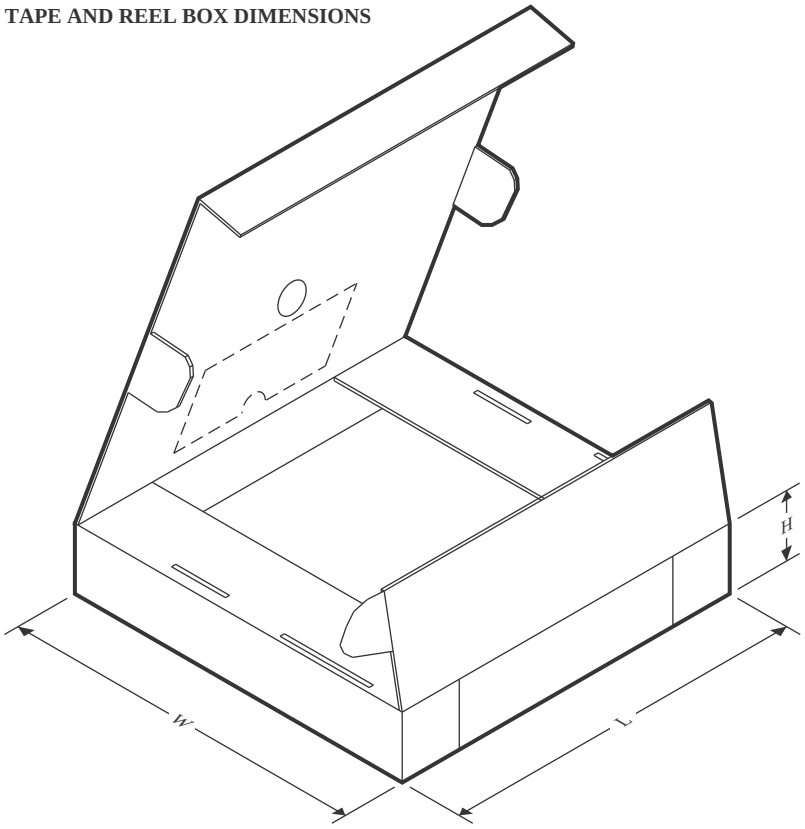



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2980AIM5-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5-4.7/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5X-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5X-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5X-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5X-4.7/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980AIM5X-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-2.5/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-3.8/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-4.7/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2980IM5X-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5X-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5X-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2980IM5X-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2980AIM5-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5-4.7/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5X-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5X-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5X-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5X-4.7/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980AIM5X-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-2.5/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-3.8/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-4.7/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5X-2.5/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2980IM5X-3.0/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

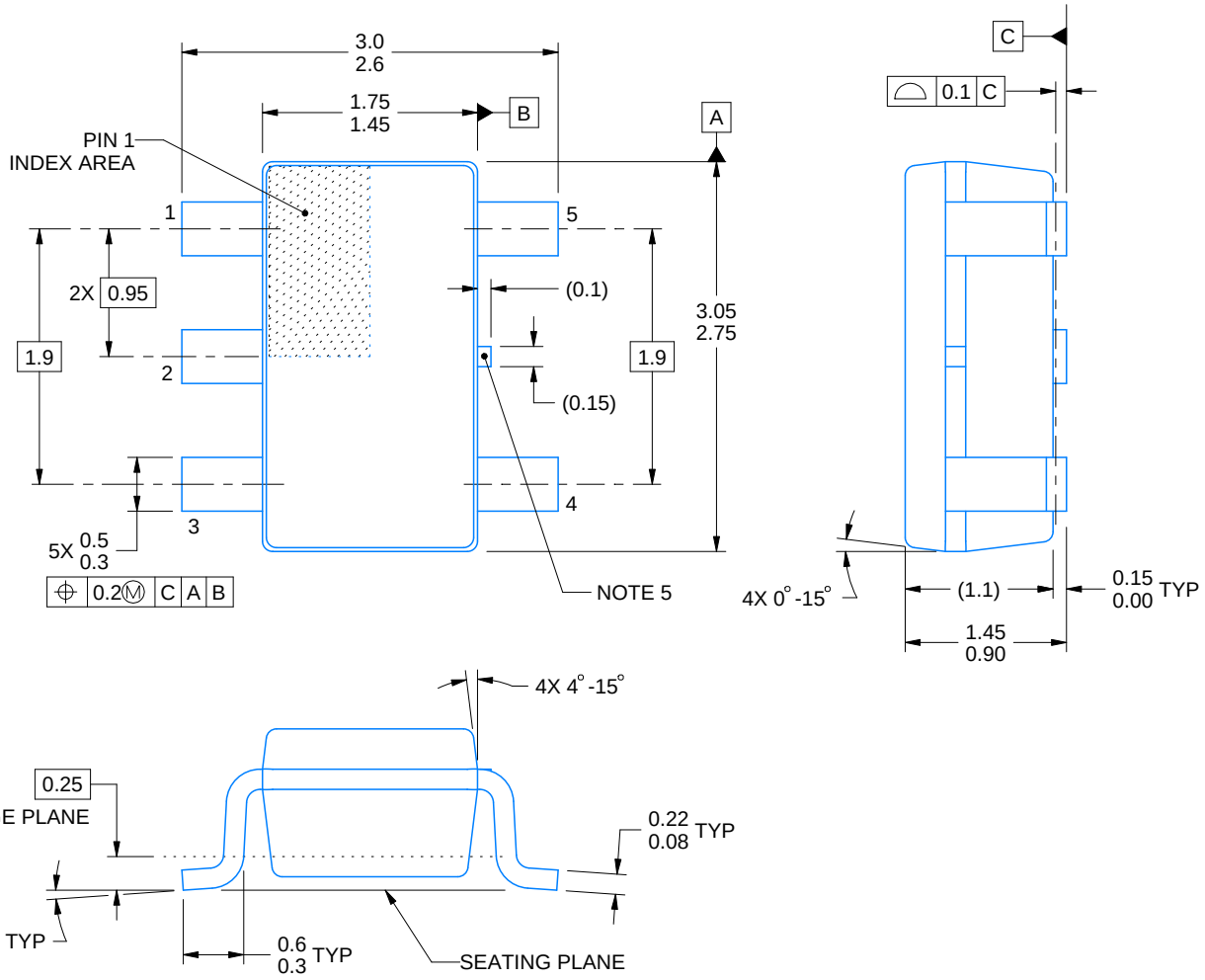
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2980IM5X-3.3/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LP2980IM5X-5.0/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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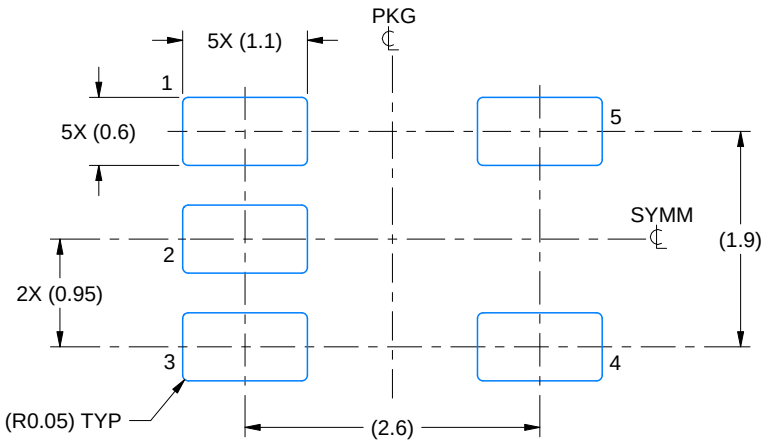
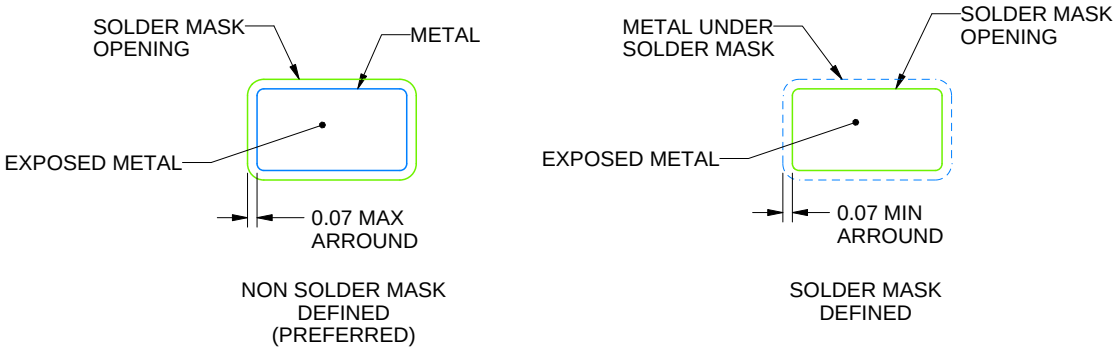
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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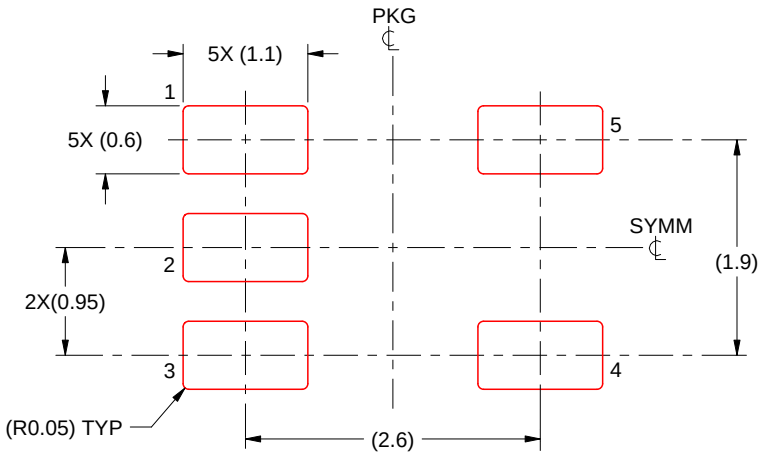
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265