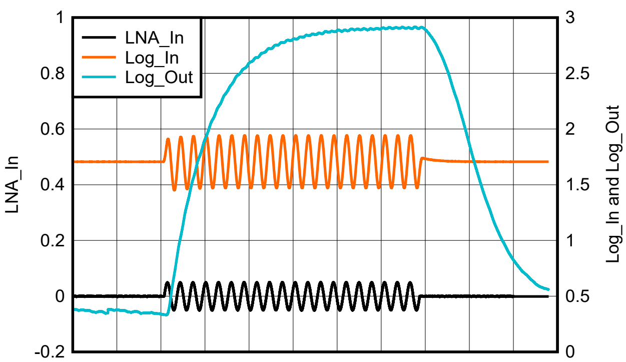
LOG300 低ノイズ アンプ内蔵、40MHz、98dB 対数検出器

1 特長

- 入力範囲：
  - LNA + 対数検出器：7μV$_P$～200mV$_P$
  - 対数検出器：20μV$_P$～1.6V$_P$
- 入力に対する出力の「スロープ」と「応答時間」を調整可能
- ダイナミック レンジ：98dB (対数適合性誤差 (LCE) = ±1dB の場合)
- 最大 40MHz の信号検出 (LCE が小さい場合、さらに高い周波数の信号を検出できます。)
- 入力周波数検出、ゼロクロス検出
- 電源電圧：3V～5.25V

2 アプリケーション

- 距離と材質の超音波検出
- フローサイトメトリー
- ESD および高エネルギー EMI 信号検出
- エネルギー検出
- 気泡、閉塞検出



3 概要

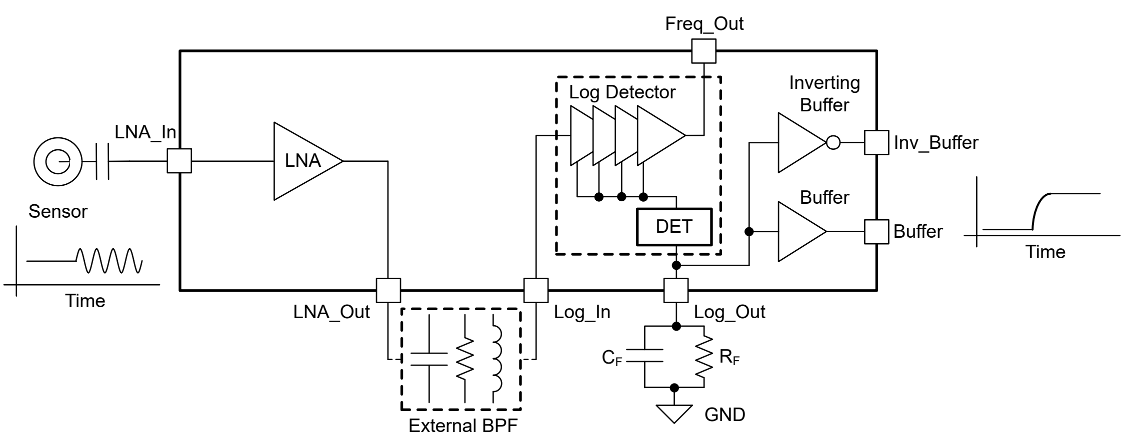
LOG300 は、低ノイズアンプ (LNA) と対数検出器ブロックで構成された統合型アナログ フロント エンド (AFE) です。このデバイスは最大 40MHz の入力周波数範囲と 98dB (標準値) のダイナミック レンジに対応しています。LOG300 は、広いダイナミック レンジの電圧および信号測定が求められるアプリケーションに適しています。LOG300 の対数検出器ブロックは、シングルエンド入力と差動入力の両方をサポートしています。内蔵 LNA は入力ノイズが小さいため、最小 7μV$_P$ の信号を測定できます。Log_Out ピンに接続されたコンデンサを調整することで、過渡出力応答を調整できます。LOG300 の内蔵周波数検出機能を使うと、入力信号の周波数とゼロクロス情報を抽出できます。

LOG300 は、16 ピン SOIC および 16 ピン VQFN パッケージで供給されます。LOG300 は、-40℃～+125℃の周囲温度範囲全体にわたって、3V～5.25V の電源で動作します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LOG300	D (SOIC、16)	9.9mm × 6mm
	RGT (VQFN、16)	3mm × 3mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



対数検出器と包絡線検出器

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4 Pin Configuration and Functions

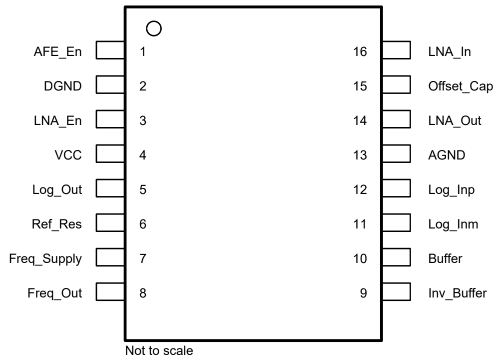


図 4-1. D Package, 16-Pin SOIC (top view)

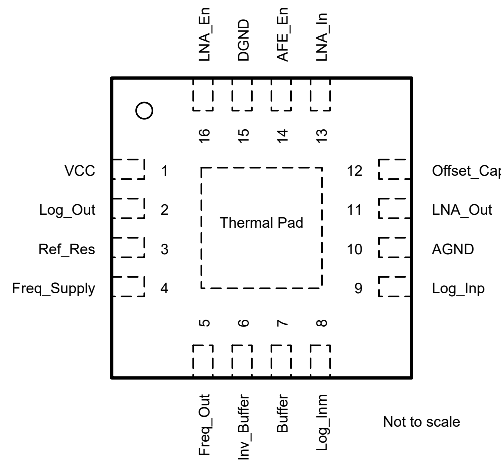


図 4-2. RGT Package, 16-Pin VQFN (top view)

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	D (SOIC)	RGT (VQFN)		
AFE_En	1	14	I	LNA and Log Detector block enable and disable pin. AFE_En = High for AFE enable. Floating this pin keeps both blocks enabled as well.
AGND	13	10	P	Analog ground for LNA and Log detector block
Buffer	10	7	O	Noninverting buffered output. $V_{Buffer} = V_{Log\_Out} \times 2$.
DGND	2	15	P	Digital ground for Freq_Out pin
Freq_Out	8	5	O	This pin toggles at the same signal frequency applied at the Log_In.
Freq_Supply	7	4	P	Power supply for Freq_Out function. Float this pin if the frequency-detection feature is not required.
Inv_Buffer	9	6	O	Inverted buffered output. $V_{Inv\_Buffer} = VCC – V_{Log\_Out} \times 2$.
LNA_En	3	16	I	Low-noise amplifier enable and disable. LNA_En = High for LNA enable. Floating this pin keeps the LNA enabled as well.
LNA_In	16	13	I	Low-noise amplifier input
LNA_Out	14	11	O	Low-noise amplifier output
Log_Inm	11	8	I	Inverting input of Log Detector block. Connect an appropriate capacitor to ground when used in a single-ended input. Refer to セクション 7.3.2.
Log_Inp	12	9	I	Noninverting input of Log Detector block
Log_Out	5	2	O	Unbuffered output of Log Detector block. Connect an appropriate resistor R_F (to set the input to output slope) and capacitor C_F (to set the response time).
Offset_Cap	15	12	I	Connect a recommended capacitor from this pin to ground. This capacitor sets the pole of the internal offset correction loop. Refer to セクション 7.3.1 for the recommended capacitor.
Ref_Res	6	3	I	Connect a 1% 56kΩ resistor to this pin. Float this pin if the default relaxed slope accuracy is acceptable.
VCC	4	1	P	Supply

表 4-1. Pin Functions (続き)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	D (SOIC)	RGT (VQFN)		
Thermal Pad	—	Thermal Pad	P	Thermal pad. Electrically isolated from the device. Connect to a heat spreading plane, typically ground.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	Supply voltage and Freq_Supply		5.5	V
	Supply turn-on and turn-off maximum dV/dT(3)		1	V/µs
	AFE_En and LNA_En	GND–0.5	VCC+0.5	V
LNA_In	LNA input voltage		±1	V_P
Log_In	Single ended input voltage (Log_Inp and Log_Inm)		(VCC × 0.17) + 0.9	V_P
I_I	Continuous input current for all pins(2)		±10	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit the input signals, which can swing more than 0.5V beyond the supply rails to 10mA or less. Can be easily achieved with a RC filter on VCC.
(3) Do not exceed this ± supply turn-on edge rate to prevent the edge-triggered ESD absorption device across the supply pins from turning on.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3		5.25	V
T_A	Ambient temperature	–40	25	125	°C
Ref_Res	Recommended reference resistor to ground		56		kΩ
Log_In	Log detector input at 3.3V VCC(1)			1.2	V_P
	Log detector input at 5V VCC(1)			1.6	

(1) At room temperature, irrespective of the frequency and waveform of the input signal.

5.4 Thermal Information

THERMAL METRIC[1]		LOG300 D (SOIC) 16 PINS	LOG300 VQFN (RGT) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	48.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.3	56.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.7	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	23.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics Low Noise Amplifier (LNA)

at T_A = 25°C, VCC = 3.3V to 5V, LNA_Out = 1kΩ to AGND, R_{SOURCE} = 50Ω, and input ac coupling capacitor (C_{IN}) = 10nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
G_{LNA}	Internal gain			11		V/V
	Internal gain error	T_A = –40°C to +125°C		±0.8	±1	%
AC PERFORMANCE						
SSBW	Small-signal bandwidth	LNA_Out = 20mV_{PP}		39		MHz
LSBW	Large-signal bandwidth			36		MHz
SR	Slew rate	2V step at LNA_Out		200		V/µs
	Total input referred noise	f > 100kHz, includes gain and bias resistors		2.6		nV/√Hz
	Overdrive recovery time	2 × output overdrive		1		µs
	Capacitive drive[1]	< 3dB of peaking		∞		nF
INPUT						
V_{LNA_In}	Linear input voltage	VCC = 5V			200	mV_P
		VCC = 3.3V			140	mV_P
V_{BIAS}	Internal bias voltage	At LNA_In, T_A = –40°C to +125°C		VCC × 0.044		mV
	Input impedance of LNA			1.7 || 1.8		kΩ || pF
OUTPUT						
	Output bias point of LNA	LNA_In = open		V_{BIAS} × 11		V
	Output impedance of LNA		0.850	1	1.150	kΩ
POWER SUPPLY						
	Quiescent operating current	LNA_Out = Open		2	2.7	mA
		T_A = –40°C to +125°C			3	mA
POWER DOWN						
	LNA enable voltage threshold		VCC – 1.2			V
	LNA disable voltage threshold				GND + 0.6	V
	Turn-on time	Time from disable to enable		50		µs
	Turn off time	Time from enable to disable		130		ns

(1) Infinite capacitive drive possible due to presence of 1kΩ of isolation resistor.

5.6 Electrical Characteristics Log Detector

at T_A = 25°C, VCC = 3.3V to 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) for VCC = 5V and R_F = 30kΩ for VCC = 3.3V, Ref_resistor = 1% 56kΩ, 10nF capacitor to AGND or to source on Log_inp and Log_inm (unless otherwise noted)[(1)] [(2)]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
LCE	Log conformance error[(3)]	f = 1MHz			±0.6	±1	dB
			T_A = –40°C to +125°C			±1.1	
		f = 40MHz			±2		
			T_A = –40°C to +125°C		±2.5		
DR	Dynamic range[(3)]	LCE = ±1dB, f = 1MHz, VCC = 5V		96	98		dB
	Log Detector slope[(4)]				R_F value in kΩ[(5)]		mV/dB
	Log Detector slope variation[(3)]	Ref_Res = 56kΩ, f = 1MHz			±1	±6	%
			T_A = –40°C to +125°C			±6.8	
		Ref_Res = open, f = 1MHz			±4.5		
			T_A = –40°C to +125°C		±5.6		
INPUT							
V_{Log_In}	Typical input range	VCC = 3.3V, LCE = ±2dB, f = 20MHz		20µ		1.2	V_P
			T_A = –40°C to +85°C	24µ		1	
			T_A = –40°C to +125°C	26µ		0.8	
		VCC = 5V, LCE = ±2dB, f = 20MHz		20µ		1.6	
			T_A = –40°C to +85°C	22µ		1.6	
			T_A = –40°C to +125°C	32µ		1.6	
	Differential input voltage	(Log_Inp) – (Log_Inm), T_A = –40°C to +125°C				±1.6	V
	Internal bias voltage	Log_Inp and Log_Inm			1.7		V
	Input impedance	for Log_Inp and Log_Inm			1.7 || 10		kΩ || pF
LOG_OUT							
	Log_Out rise time	C_F = 220pF			20		µs
		C_F = 1nF			95		
	Log_Out fall time	C_F = 220pF			27		µs
		C_F = 1nF			100		
	Output overdrive recovery	C_F = 220pF			250		µs
	Minimum output voltage[(3)] [(6)] Log_Inp = 10nF to AGND	QFN Package		82	142	233	mV
			T_A = –40°C to +125°C			301	
		SOIC Package		90	130	162	
			T_A = –40°C to +125°C			250	mV
	Maximum output voltage	T_A = –40°C to +125°C		VCC– 0.3			V

5.6 Electrical Characteristics Log Detector (続き)

at T_A = 25°C, VCC = 3.3V to 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) for VCC = 5V and R_F = 30kΩ for VCC = 3.3V, Ref_resistor = 1% 56kΩ, 10nF capacitor to AGND or to source on Log_inp and Log_inm (unless otherwise noted)(1) (2)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
BUFFER OUTPUT (C_{LOAD} || R_{LOAD} = 100pF || 10kΩ)							
	Gain	V_{Buffer}/V_{Log_Out}			+2		V/V
	Output voltage equation				2 × Log_Out		V
	Output-referred offset					30	mV
	Output voltage	T_A = –40°C to +125°C		GND + 0.1		VCC– 0.1	V
	Rise-and-fall time(5)	C_{LOAD} || R_{LOAD} = 100pF || 10kΩ			1.5		µs
	Short-circuit current	Source-and-sink current		10			mA
Z_{OUT}	Output impedance				5.3		Ω
INV_BUFFER OUTPUT (C_{LOAD} || R_{LOAD} = 100pF || 10kΩ)							
	Gain	$V_{Inv\_Buffer}/V_{Log\_Out}$			–2		V/V
	Output voltage equation				VCC–(2× Log_Out)		V
	Output voltage	T_A = –40°C to +125°C		GND + 0.1		VCC – 0.1	V
	Rise-and-fall time(5)	C_{LOAD} || R_{LOAD} = 100pF || 10kΩ			1.5		µs
	Output-referred offset					32	mV
	Short-circuit current	Source-and-sink current		10			mA
	Output impedance				6.3		Ω
FREQUENCY DETECT OUTPUT							
	Frequency detect block typical input sensitivity	Log_Inp signal of f < 20MHz		250µ		1.6	V_P
	Frequency error	Averaged over 1ms, T_A = –40°C to +125°C			0.15		%
	Freq_Out swing			DGND		Freq_Supply	V
POWER SUPPLY							
	Quiescent current	Current through VCC			3.6	4.6	mA
			T_A = –40°C to +125°C			5.9	
		Current through Freq_Supply				0.37	

(1) See *Offset Correction Loop* to calculate the value of capacitor on Offset_Cap pin based on signal frequency.
(2) The symbol f stands for a short burst of sine wave applied at the Log_Inp pin. This definition applies across the data sheet.
(3) Characterized through 32 units.
(4) Log-Detector slope reduces with increased input signal frequency, see *Typical Characteristics*.
(5) See *Parameter Measurement Information* for definition of R_F.
(6) Minimum output voltage is the lowest voltage that Log_Out settles to when the inputs are shorted to the AGND pin using a high-value capacitor with no signal applied.

5.7 Electrical Characteristics LNA + Log Detector (AFE)

at T_A = 25°C, VCC = 5V, C_F = 1nF and R_F = 43kΩ (slope = 43mV/dB for f = 1MHz), Ref_resistor = 1% 56kΩ, with 2nd-order external band-pass filter (BPF) of gain = –7dB, and R_{SOURCE} = 50Ω, 10nF capacitor to AGND or to source on LNA_In (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AFE AC PERFORMANCE							
LCE	Log conformance error	f = 1MHz			±1		dB
			T_A = –40°C to +125°C		±1		
DR	Dynamic range	For LCE = ±1dB, f = 1MHz			91		dB
	Log Detector slope variation[(1)]	Ref_Res = open			±4.5		%
		Ref_Res = 56kΩ			±1	±7	
		Ref_Res = 56kΩ	T_A = –40°C to +125°C			±7.2	
AFE INPUT							
	Typical input voltage	LCE = ±1dB, f = 1MHz		7μ		200m	V_P
			T_A = –40°C to +125°C	8μ		200m	
		LCE = ±2dB, f = 20MHz		12μ		200m	
			T_A = –40°C to +125°C	14μ		200m	
	Output rise time	BPF = 180kHz, C_F = 350pF			35		μs
		BPF = 1MHz, C_F = 500pF			50		
	Output fall time	BPF = 180kHz, C_F = 350pF			65		μs
		BPF = 1MHz, C_F = 500pF			45		
LOG_OUT							
	Minimum output voltage[(1)]	LNA_In = 10nF to AGND			290	335	mV
			T_A = –40°C to +125°C			450	
POWER SUPPLY							
	VCC quiescent current	Total AFE, LNA_Out = open			6	7.2	mA
			T_A = –40°C to +125°C			8.3	
POWER DOWN							
	VCC disabled current	Total AFE, VCC = 3.3V	T_A = –40°C to +125°C			65	μA
		Total AFE, VCC = 5V				130	
	AFE enable voltage threshold			VCC– 1.2			V
	AFE disable voltage threshold					AGND + 0.6	V

(1) Characterized through 32 devices.

5.8 Typical Characteristics: VCC = 5V

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block

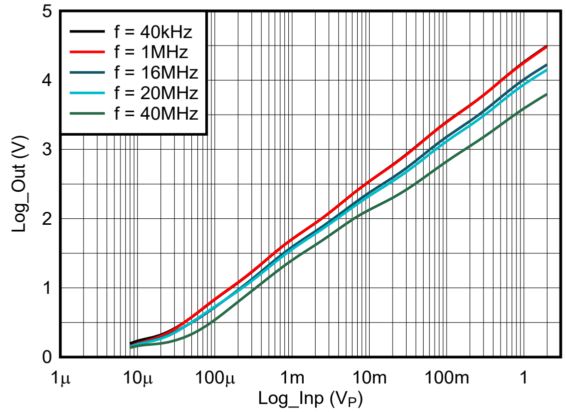


図 5-1. Log-Detector Output at Various Frequencies

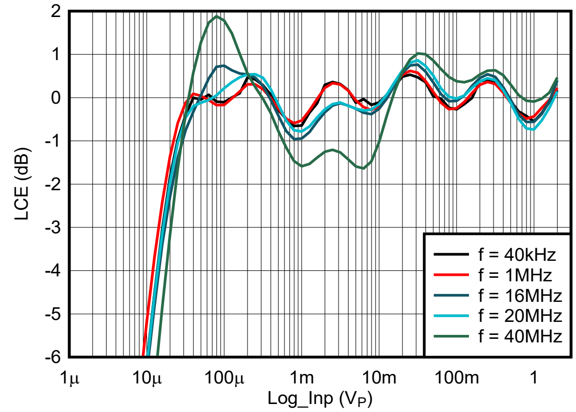


図 5-2. Log-Detector Conformance Error for Different Frequencies

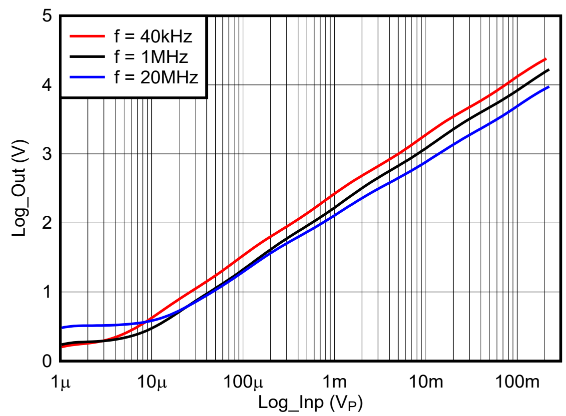


図 5-3. AFE Output at Various Frequencies

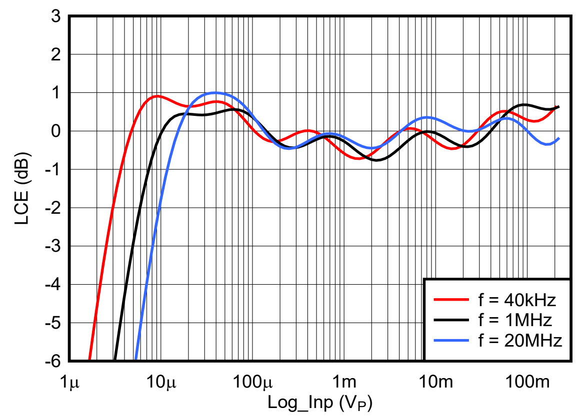
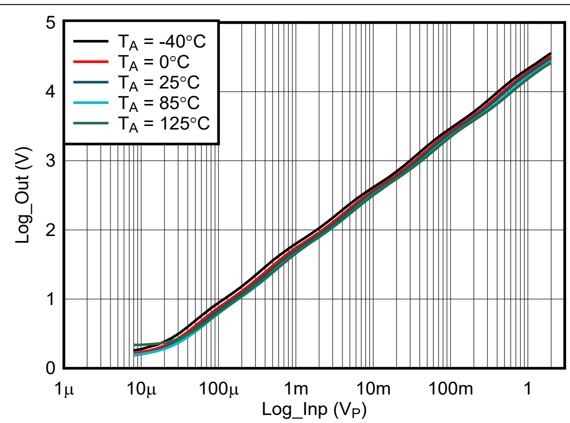
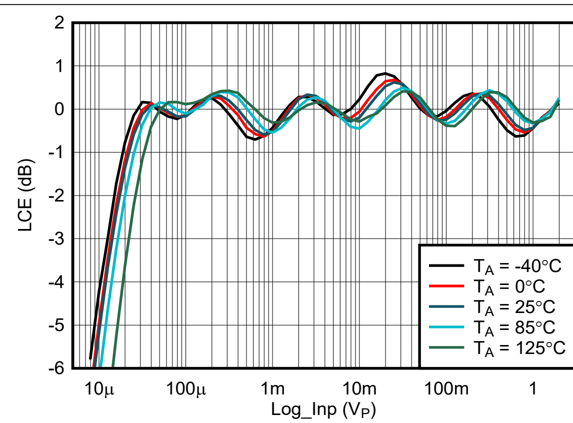


図 5-4. AFE Log-Conformance Error for Different Frequencies



f = 1MHz

図 5-5. Log-Detector Output at Different Temperature Points

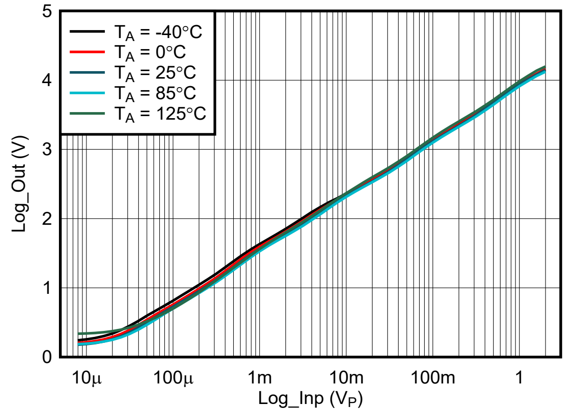


f = 1MHz

図 5-6. Log-Detector Conformance Error for Different Temperature Points

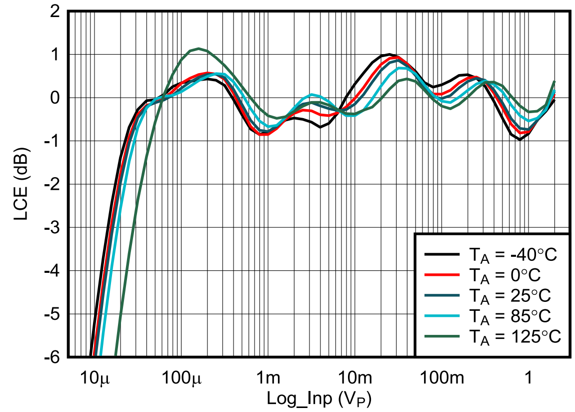
5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block



f = 20MHz

図 5-7. Log-Detector Output at Different Temperature Points



f = 20MHz

図 5-8. Log-Detector Conformance Error for Different Temperature Points

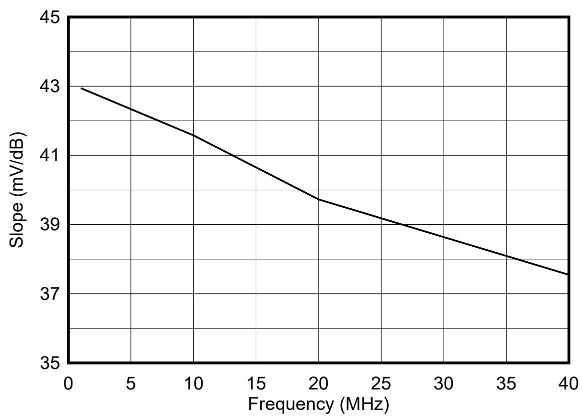
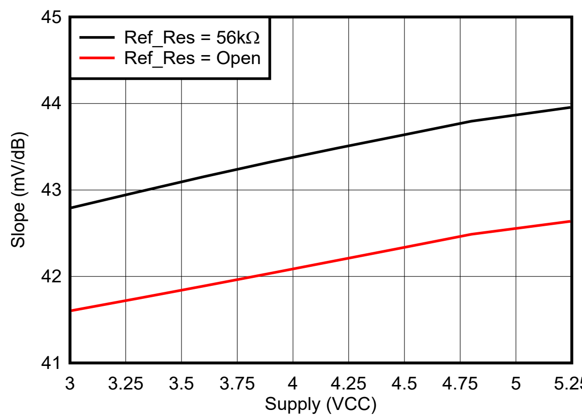


図 5-9. Log-Detector Slope Variation with Input Signal Frequency

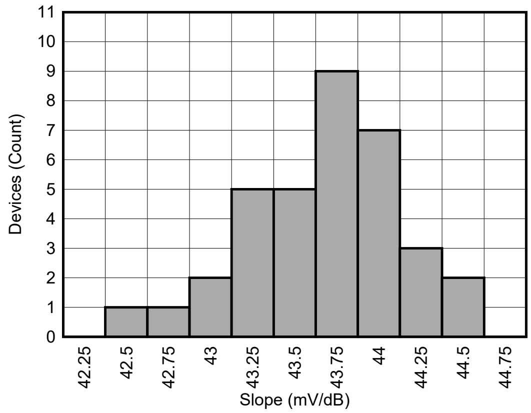


R_F = 43kΩ, f = 1MHz

図 5-10. Log-Detector Slope Variation vs Supply

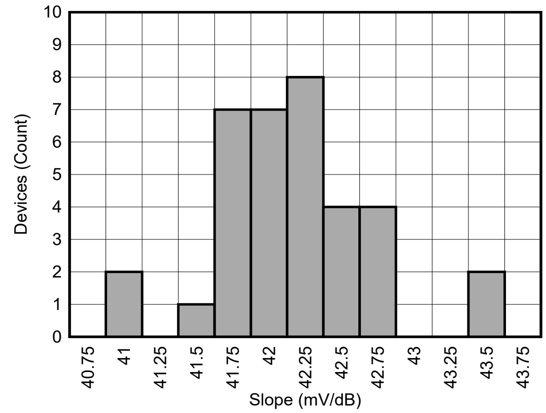
5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block



Ref_Res = 56kΩ μ = 43.55mV/dB σ = 0.44mV/dB

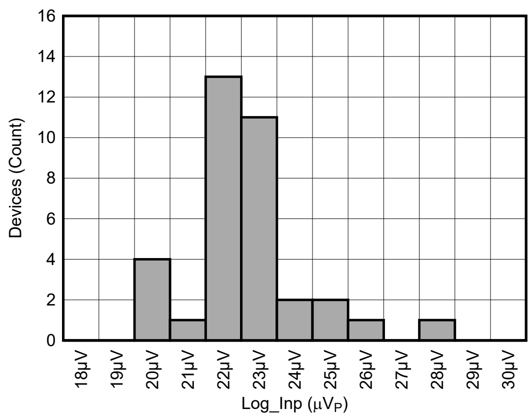
図 5-11. Log-Detector Slope Histogram With Ref_Res



Ref_Res = Open μ = 42.03mV/dB σ = 0.53mV/dB

Units tested from the same lot

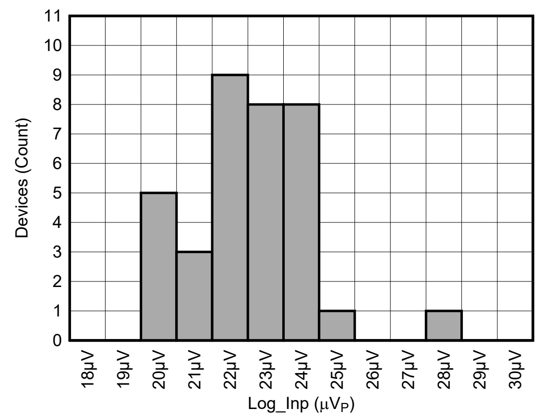
図 5-12. Log-Detector Slope Histogram Without Ref_Res



LCE = ±1dB, μ = 22.15μV_P σ = 1.59μV_P

f = 1MHz

図 5-13. Minimum Input Sensitivity of Log_Detector



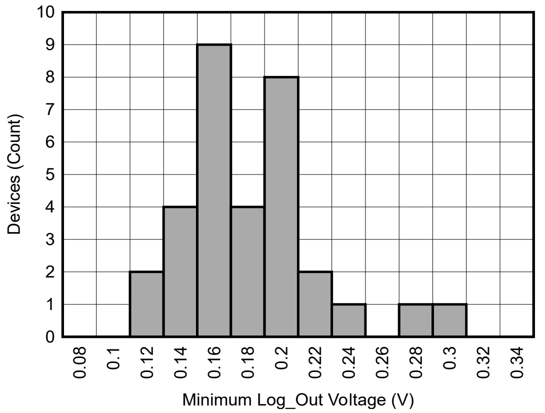
LCE = ±2dB, μ = 22.14μV_P σ = 1.67μV_P

f = 20MHz

図 5-14. Minimum Input Sensitivity of Log_Detector

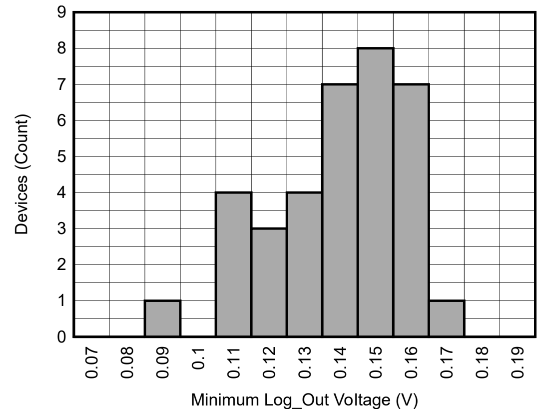
5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block



50Ω + 10nF at Log_Inp to AGND μ = 0.17V σ = 0.04V

図 5-15. Minimum Output Voltage at Log_Out



10nF at Log_Inp to AGND μ = 0.13V σ = 0.018V

図 5-16. Minimum Output Voltage at Log_Out

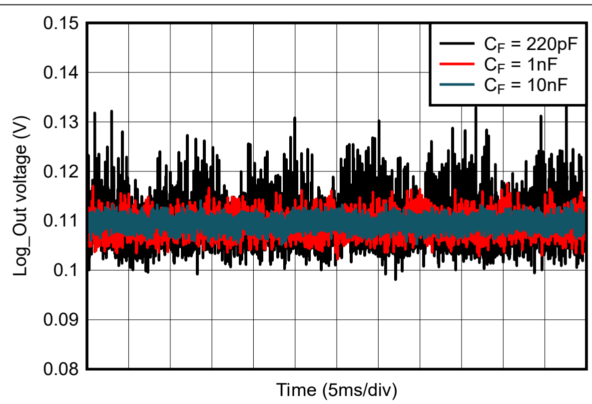


図 5-17. Minimum Log_Out Voltage vs Time

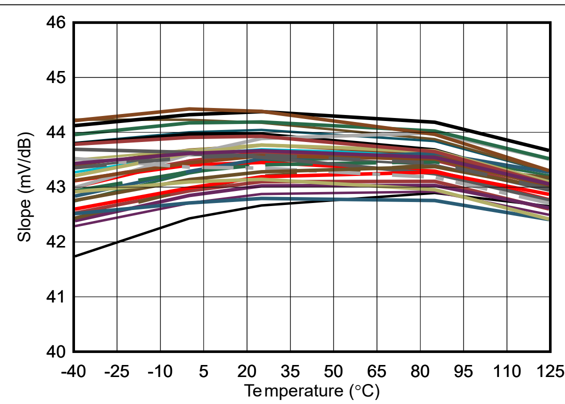
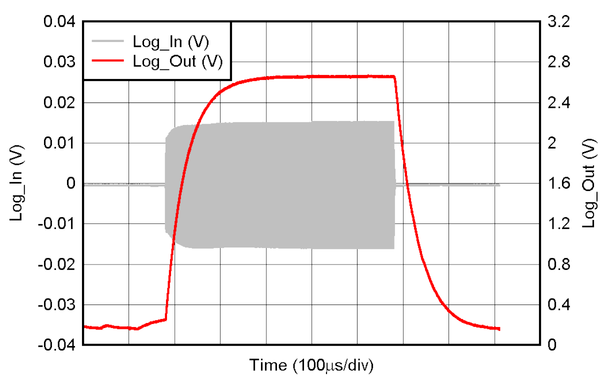
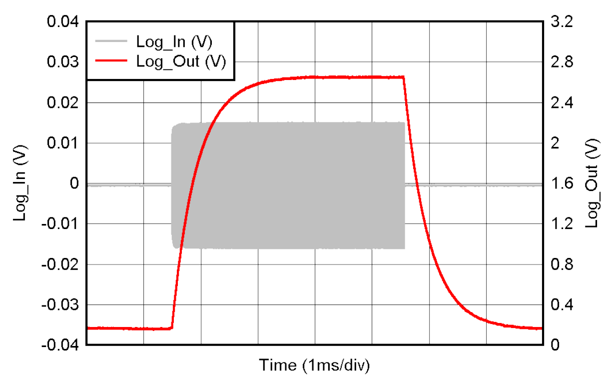


図 5-18. Slope Variation vs Temperature



f = 1MHz, C_F = 1nF

図 5-19. Log-Detector Rise and Fall Time

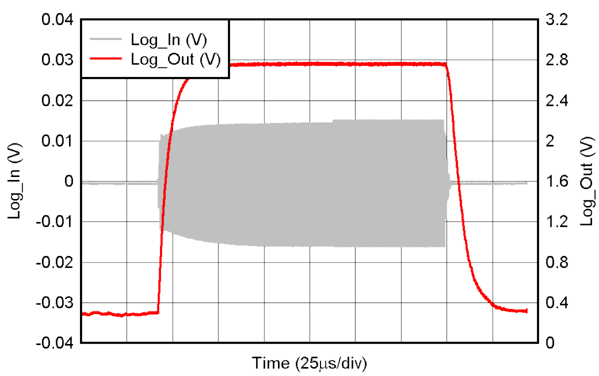


f = 1MHz, C_F = 10nF

図 5-20. Log-Detector Rise and Fall Time

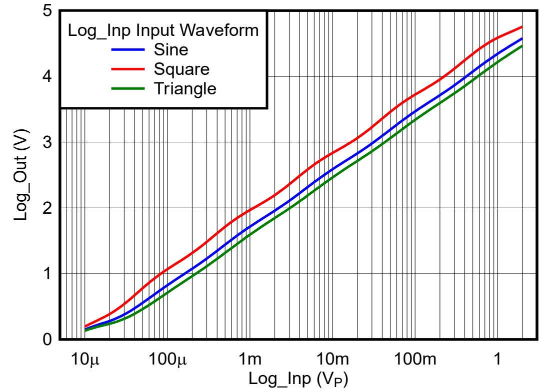
5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block



f = 1MHz, C_F = 100pF

図 5-21. Log-Detector Rise and Fall Time



f = 1MHz

図 5-22. Log-Detector output for Various Input Waveforms

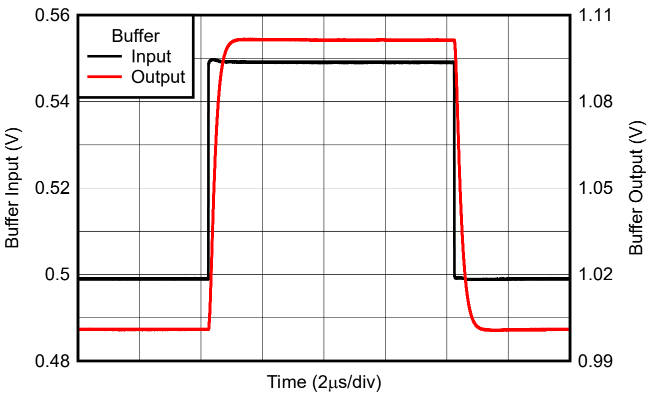


図 5-23. Small-Signal Step Response: Buffer

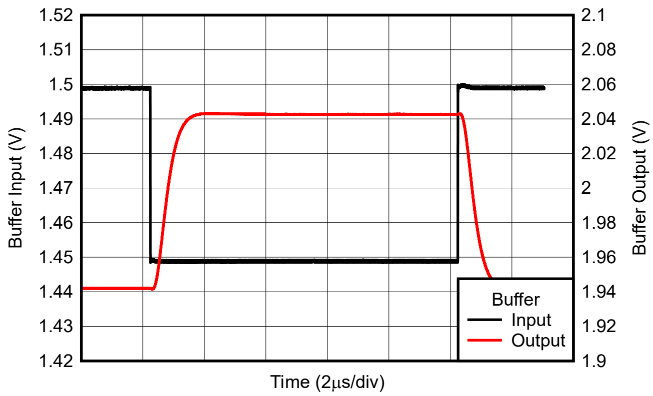


図 5-24. Small-Signal Step Response: Inverting Buffer

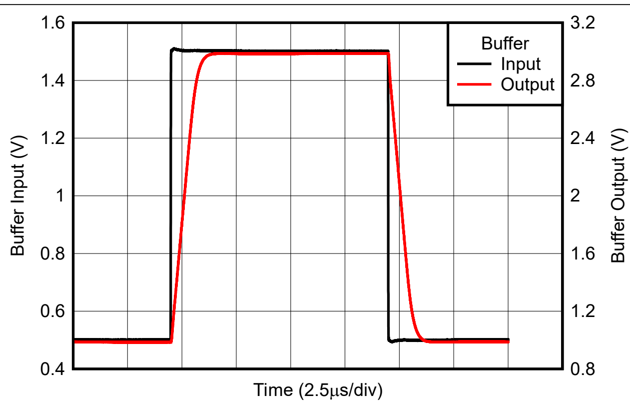


図 5-25. Large-Signal Step Response: Buffer

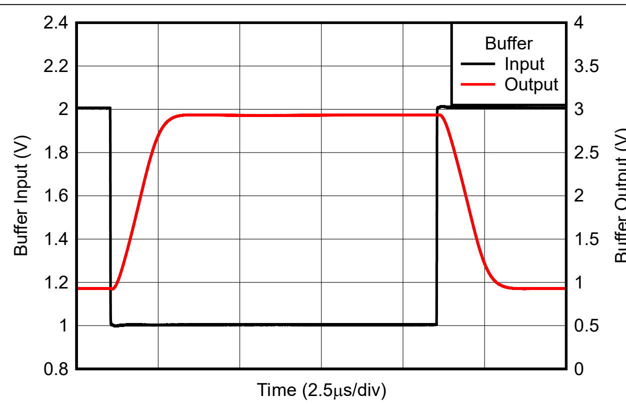


図 5-26. Large-Signal Step Response: Inverting Buffer

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block

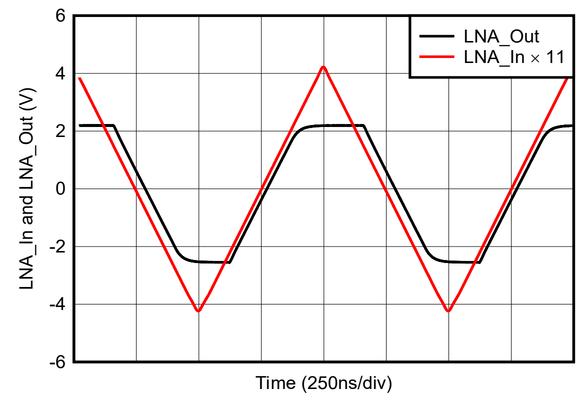
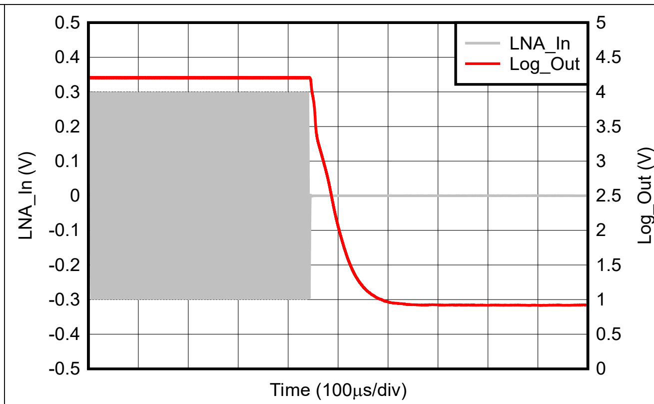
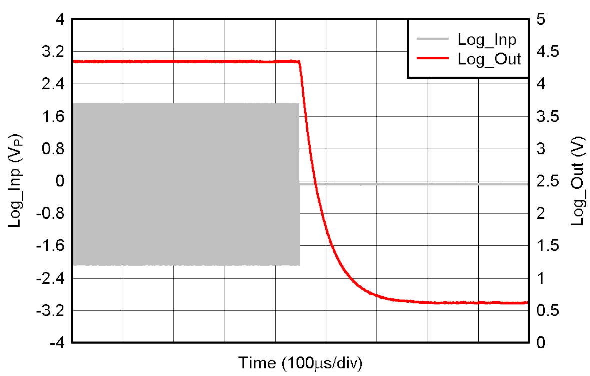


図 5-27. LNA Overdrive Recovery



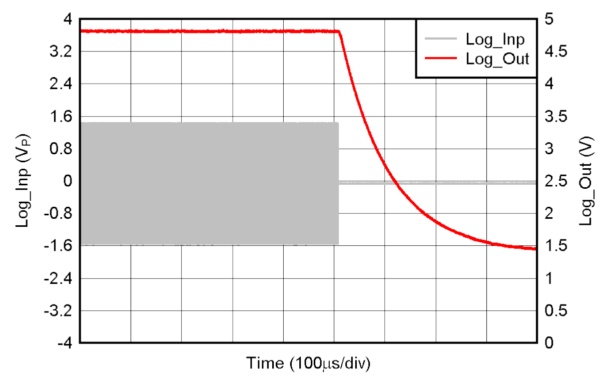
BPF = 180kHz, C_F = 220pF

図 5-28. AFE Overdrive Recovery



C_F = 200pF , Log_Inp = $4V_P$

図 5-29. Log-Detector Input Stage Overdrive



C_F = 200pF, R_F = 100kΩ

図 5-30. Log-Detector Output Stage Overdrive

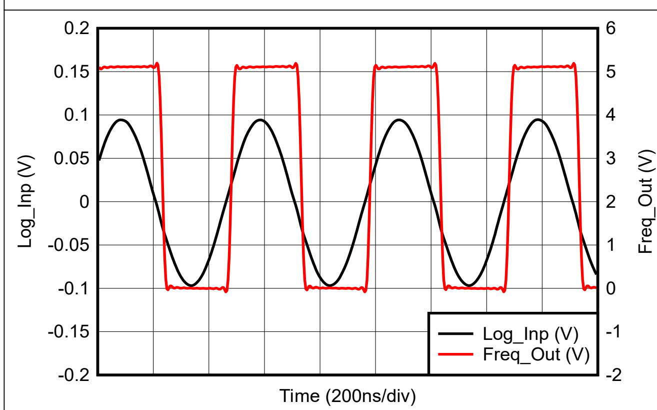
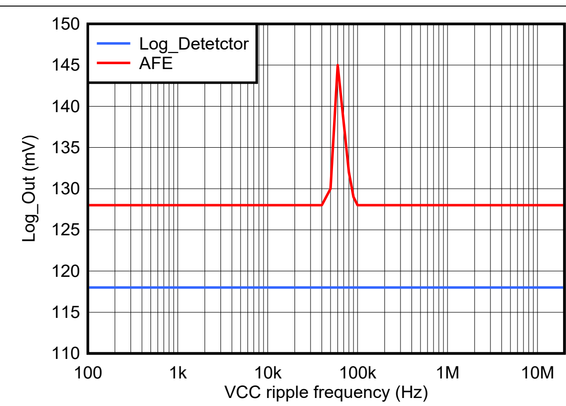


図 5-31. Frequency Detector Output Waveform

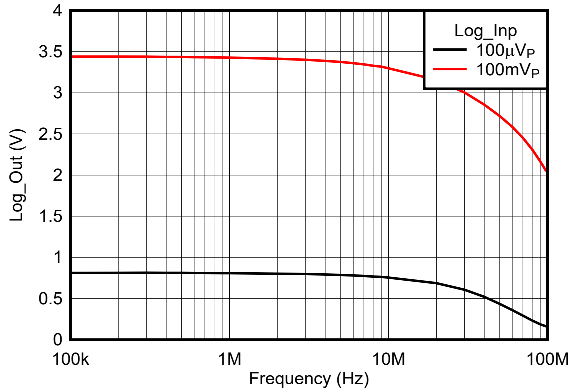


AFE; BPF = 65kHz, RC filter on VCC of R = 50Ω, C = 12µF

図 5-32. Output vs 100mVpp Ripple Injected on VCC

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block



R_F = 42.2kΩ, Offset_Cap = 100nF

図 5-33. Slope vs Frequency

5.9 Typical Characteristics: VCC = 3.3V

at T_A = 25°C, VCC = 3.3V, C_F = 1nF, R_F = 30kΩ (slope = 30mV/dB), Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm (unless otherwise noted); for AFE, 2nd-order BPF centered around frequency *f* with gain = –7dB used between LNA and Log Detector block

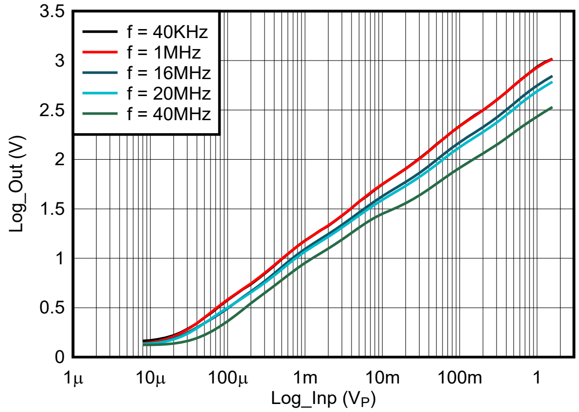


図 5-34. Log-Detector Output at Various Frequencies

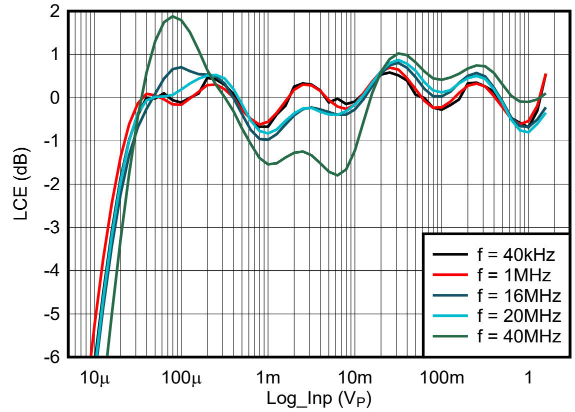


図 5-35. Log-Detector Conformance Error for Different Frequencies

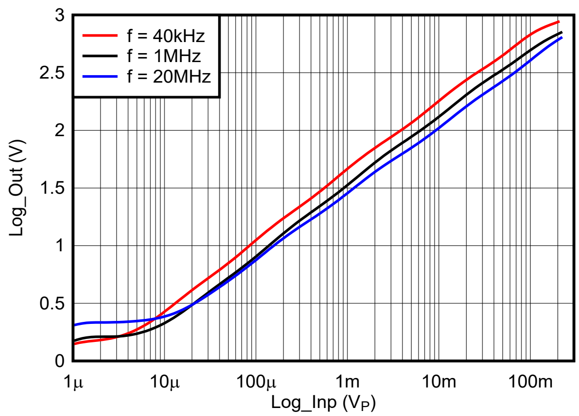


図 5-36. AFE Output at Various Frequencies

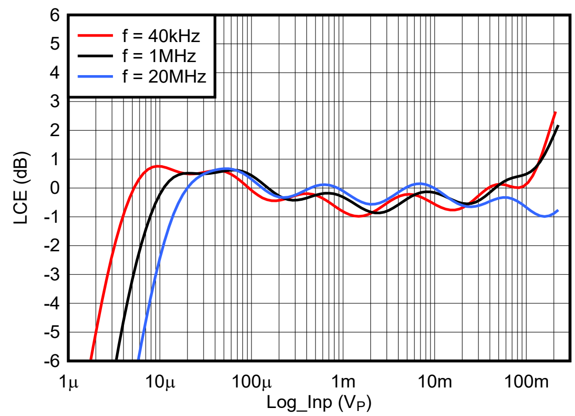
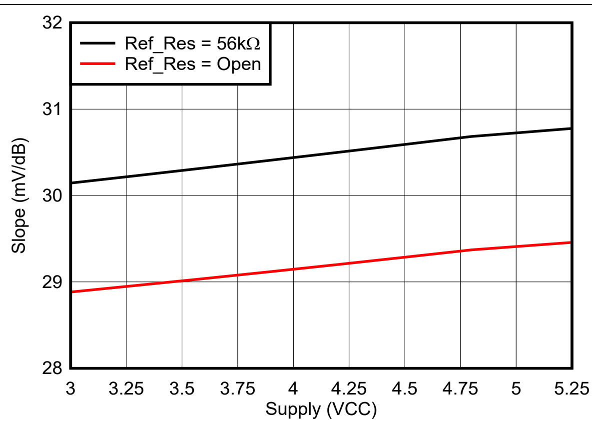


図 5-37. AFE Log-Conformance Error for Different Frequencies



R_F = 30kΩ, f = 1MHz

図 5-38. Log-Detector Slope Variation vs Supply

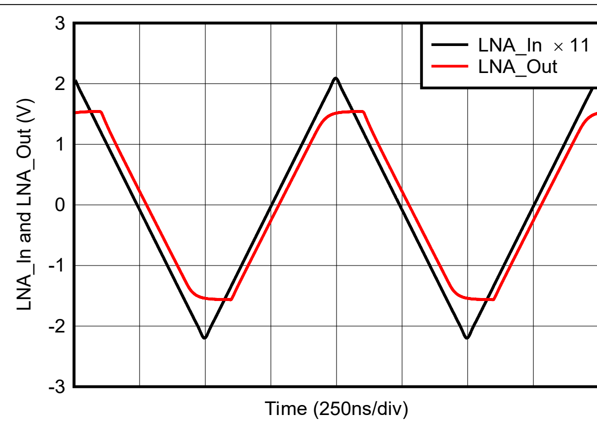


図 5-39. LNA Overdrive Recovery

6 Parameter Measurement Information

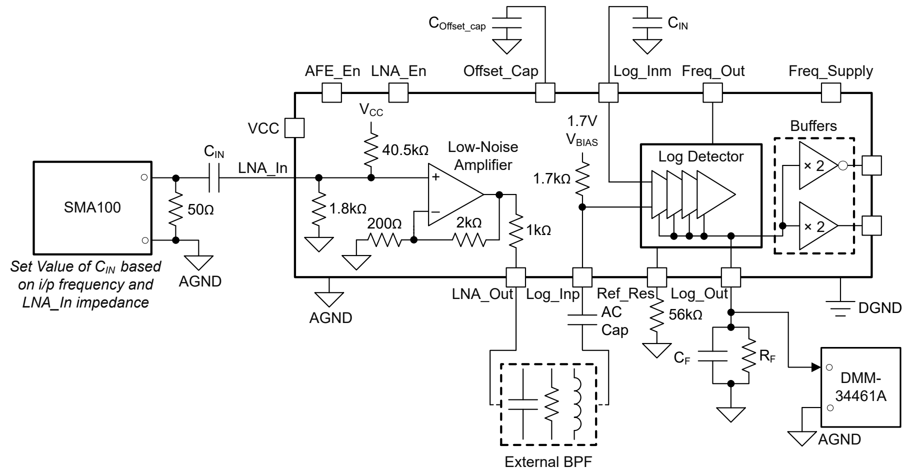


図 6-1. AFE (LNA + Log Detector) Slope Characterization

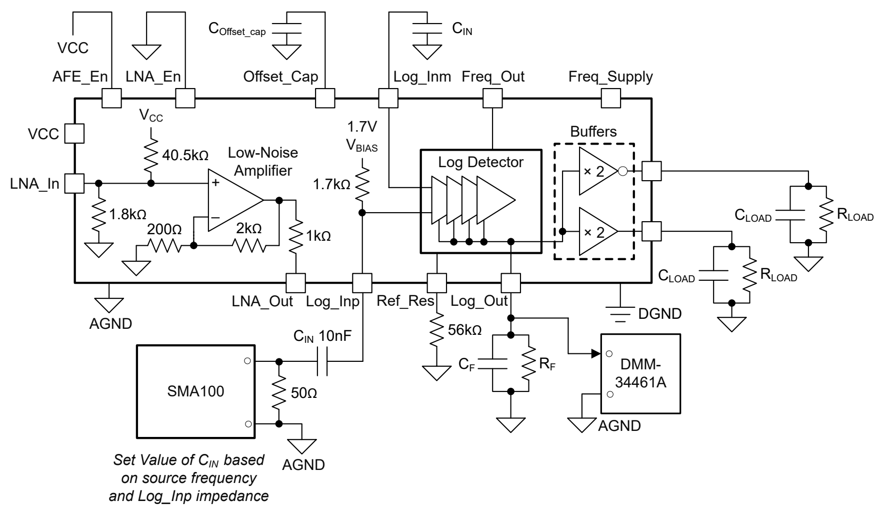


図 6-2. Log Detector Slope Characterization

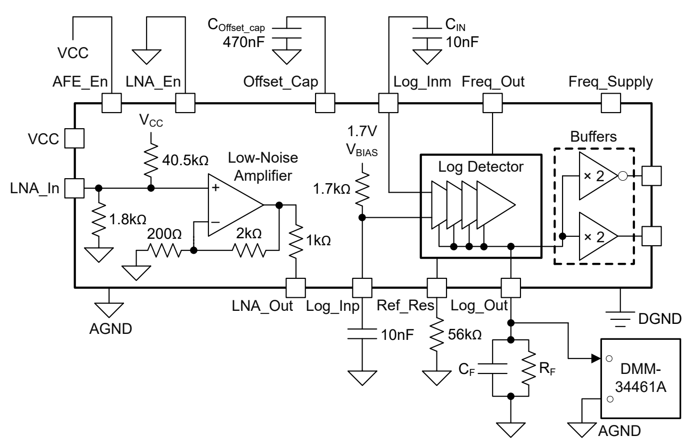


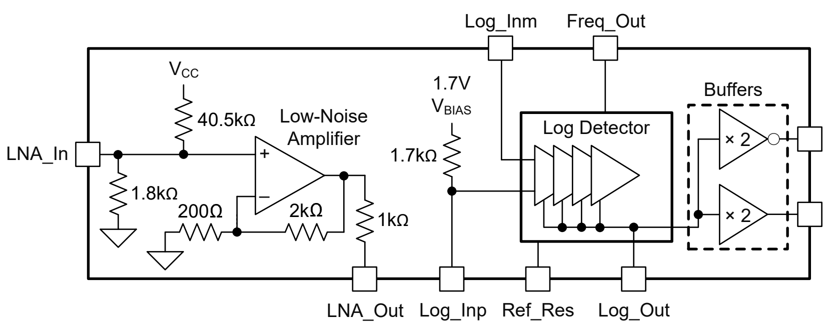
図 6-3. Log Detector Minimum Output Voltage Measurement

7 Detailed Description

7.1 Overview

The LOG300 is a highly sensitive analog front-end system for power measurements of up to 40MHz signals with a typical dynamic range of 98dB. The LOG300 is intended for use in a wide variety of applications like ultrasonic Rx signal chains, amplitude demodulation, signal power measurement, grid monitoring and so on. The LOG300 provides an analog envelope of an amplitude proportional to the log of the input signal. This behavior provides the application circuit precise input signal amplitude measurement without the need of high-speed signal acquisition components. The integrated frequency-detect feature enables zero-crossing and frequency measuring capability of the incoming signal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Offset Correction Loop (OCL)

The LOG300 comes with an internal offset correction loop (OCL) designed to correct for any small offset voltage errors due to external factors or due to the internal gain mismatch. The LOG300 internal gain blocks offer very high gain; therefore, any small error voltage is sufficient to saturate the respective gain block resulting in degradation of dynamic range.

The Offset_Cap (see セクション 6) sets the time constant of the offset correction loop. Set the value of the OCL pole to less than the incoming signal frequency so that the OCL does not respond to the incoming signal. Use the following formula to calculate the value of Offset_Cap based on the frequency of the incoming signal.

$$C_{Offset\_Cap}\left(nF\right) \geq \frac{6000}{Frequency\ of\ input\ signal\ (kHz)} \quad (1)$$

Where

- Offset capacitor must never be less than 1nF. If the formula yields a value of C_{Offset_Cap} less than 1nF, use 1nF.
- Using a value of C_{Offset_Cap} greater than the calculated value using above equation is acceptable since the OCL loop is set to a lower frequency.

7.3.2 Single and Differential Input

The Log Detector block of the LOG300 supports both single-ended and differential input signals. Irrespective of the type of input signal, the impedances from the Log_Inp and Log_Inm pins to AGND have to be matched.

The requirement for impedance matching arises from the fact that any supply noise or externally coupled noise passes through these impedances and generates an input voltage. If the impedances are mismatched at the two inputs a differential voltage is seen by the Log Detector block thereby increasing the minimum output voltage at the Log_Out pin. This results in degradation of the dynamic range.

Impedance matching for differential input case can be easily achieved by replicating source impedance on both pins.

However for single-ended inputs, impedance matching can be quite complex. If board space is not limited TI recommends to copy the input structure at the Log_Inp pin as, is on to the Log_Inm input. Please take note of the default internal output impedance of the LNA of 1kΩ when copying the structure to the Log_Inm pin.

If the above recommendation is not possible, match the impedances between the two pins at the frequency with the highest probability of noise coupling. For example if the VCC supply is being derived by a DC/DC converter switching at a frequency of 500kHz, using option 1 gives the best impedance matching between Log_Inp and Log_Inm. If the VCC ripple is at 100kHz then both option 1 and option 2 result in the same rejection response.

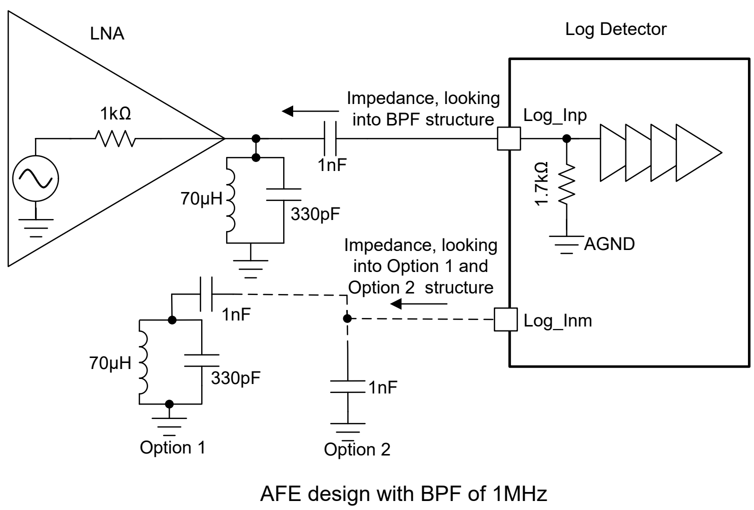


図 7-1. Impedance Structure at Log_Inp and Log_Inm

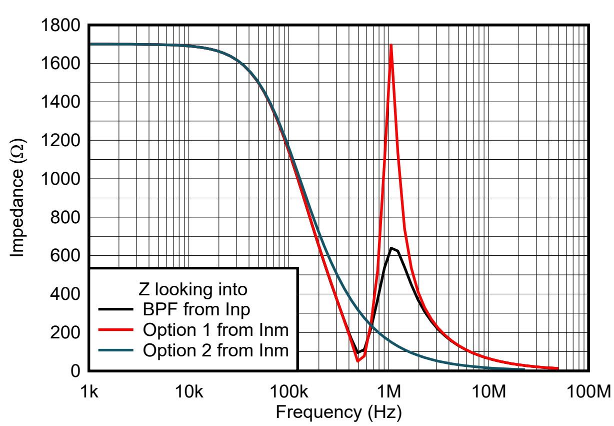


図 7-2. Impedance vs Frequency at Log_Inp and Log_Inm

7.3.3 Input Frequency Detect

The Log_Out pin creates an envelope proportional to the incoming signal; therefore, the frequency and phase information of the input signal is lost. The frequency detect feature enables the LOG300 to recover this frequency information. The frequency detect pin toggles at the same frequency as the input, and can therefore be used to calculate the input signal frequency or the input signal zero crossing points.

The internal circuit consists of a comparator with one of the inputs connected to the pin Log_In bias voltage and the other input of the comparator connected to the last stage of the Log Detector gain block (see 図 7-3). Log_In is ac coupled; therefore, the incoming signal is biased to the internal bias voltage.

The comparator compares the gained Log_In (both single-ended and differential) signal biased at the internal bias voltage with the DC internal bias voltage, thereby toggling at every instance of a zero crossing. If the incoming signal is not a symmetric waveform or consists of multiple frequency content, the frequency detect feature compares the zero crossings of the incoming signal.

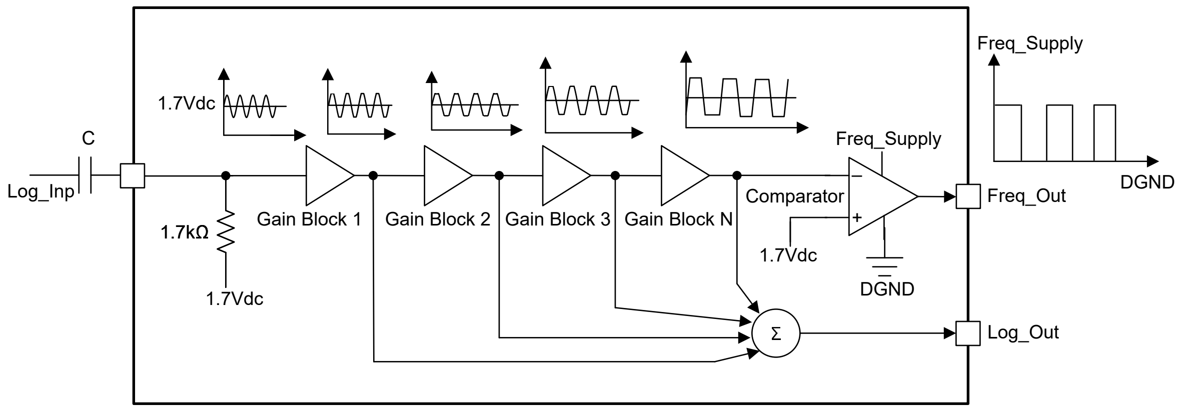


図 7-3. Internal Block Diagram for Frequency Detect

7.4 Device Functional Modes

The LOG300 offers three functional modes:

- AFE Disabled
  - In this mode, the complete AFE (LOG300) is disabled and consumes only about 100µA.
- LNA Disabled
  - In this mode, the LNA is disabled, while the Log Detector block is still operational. See セクション 5.6 for detailed parameters in this mode.
  - Typically, this mode is used when the input sensitivity required is relaxed and the application prioritizes a lower quiescent current. Disabling the LNA helps save 2mA of quiescent current originally consumed by the LNA.
- Normal operating mode
  - In this mode, all blocks of the LOG300 are operational. See セクション 5.7 for detailed parameters such as power consumption, acceptable supply, and input output range.
  - This mode can be entered by floating the LNA_En and AFE_En pins or by tying them to VCC.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LOG300 is a good fit for multiple applications involving ultrasound receive signal measurement, power, and energy measurements. The wide dynamic range and high input sensitivity makes the LOG300 an excellent option for applications such as the example in セクション 8.2.1 involving measurement of low amplitude signals without the need of expensive, high-bandwidth, low-noise components.

8.2 Typical Application

8.2.1 Ultrasonic Distance Measurement

This design example demonstrates the circuit calculations and discrete component selection around the LOG300 to achieve a highly sensitive receive signal chain for a typical ultrasonic distance based measurement sensor.

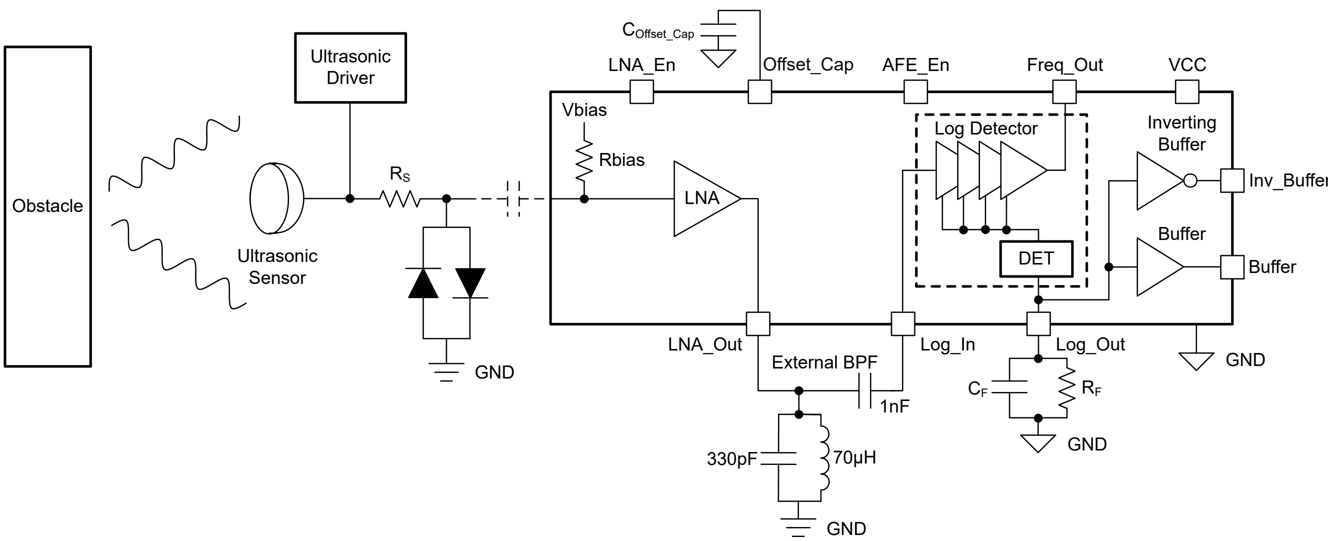


図 8-1. Ultrasonic Distance Sensor

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Supply (VCC)	5V
Minimum input signal measuring capability	7µV_P
Maximum input signal measuring capability: Linear	200mV_P
Maximum input signal handling capability (V_{max})	100V_P
Frequency of Tx and Rx signal	1MHz
Log_Out; Output range	0.5V to 4.5V

8.2.1.2 Detailed Design Procedure

The LOG300 supports a 5V VCC. Add a 10Ω and 10μF || 10nF close to the VCC pin to provide sufficient decoupling and immunity from external noise. This supply filter has a pole of 1.59kHz that is sufficiently less than the frequency of interest, which is 1MHz.

The absolute maximum voltage rating of pin LNA_In is ±1V. Add a back-to-back diode along with a series resistor (R_S) at the input of the LNA (see also 図 8-1). The back-to-back diode protects the LNA_In pin from being exposed to any high voltages, especially during the transmit operation. Choose the series resistance value in accordance to the maximum power rating (P_{MAX}) of the back-to-back diode. The added series resistor contributes to the input noise and deteriorates the minimum input sensitivity.

$$R_S = \frac{(0.7V \times (V_{max} - 0.7V))}{P_{max}} \tag{2}$$

The maximum expected output voltage of the LNA with a back-to-back diode placed at the input is:

$$11V/V \times 0.7V_P = 7.7V_P \tag{3}$$

Since the LNA is only powered from a 5V supply; the maximum output is only $2.5V_P$.

The maximum input for the Log_Inp pin is $1.7V_P$ for 5VCC (see also セクション 5.1); therefore, add a band-pass filter (BPF) of appropriate attenuation in the pass-band region so that the detector block absolute maximum voltage rating is not violated. In this particular case, ensure that the BPF has an attenuation of at least −3.3dB. A BPF of −4.3dB is shown in 図 8-1.

Choose an Offset_Cap value based on セクション 7.3.1.

Choose the value of C_F based on the required rise time of the Log_Out pin voltage (V_{Log_Out}). A lower-value C_F improves the rise time at the cost of higher ripple on the output envelope. For reference plots see also セクション 5.8. Connect an oscilloscope at the Log_Out pin, triggered during the receive burst operation, to find the correct balance between the required rise time and the acceptable ripple.

The R_F resistor decides the input-to-output slope. The value of R_F in kΩ equals the input-to-output slope in mV/dB. In this example, calculate R_F using the below set of equations:

$$\text{Slope}\left(\text{mV/dB}\right) = R_F\,k\Omega = \frac{(\text{Saturated output voltage} - \text{Minimum output voltage})}{(20 \times \log(\text{Maximum LNA\_In} / \text{Minimum LNA\_In}))} \tag{4}$$

$$\text{Slope}\left(\text{mV/dB}\right) = R_F\,k\Omega = \frac{(4.5V - 0.5V)}{(20 \times \log(200mV - 7\mu V))} \tag{5}$$

$$\text{Slope}\,(\text{mV/dB}) = 44\text{mV/dB, hence use } R_F\,k\Omega = 44k\Omega \tag{6}$$

注

The maximum and minimum Log_Out values have been relaxed to design for the output to operate well within the linear range. R_F accuracy effects the slope accuracy.

The voltage measured at Log_Out can be traced back to calculate the input amplitude using the below equation:

$$\text{Log\_Out}_A = \text{Slope} \times 20 \times \text{Log}\left(\frac{\text{Log\_In}_A}{\text{Log\_In}_B}\right) + \text{Log\_Out}_B \tag{7}$$

$$\text{Log\_In}_A = 10^{\left(\frac{\text{Log\_Out}_A - \text{Log\_Out}_B}{\text{Slope} \times 20}\right)} \times \text{Log\_In}_B \tag{8}$$

Where : A stands for values of Log_Out and Log_In at the required measurement point and B stands for Log_Out and Log_In values at a known input value measured during factory calibration or production.

8.2.1.3 Application Curves

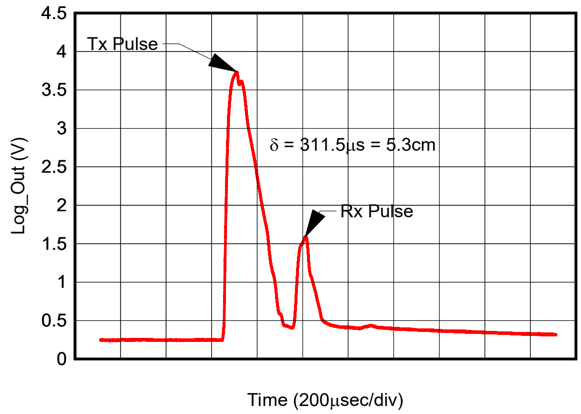


図 8-2. Log_Out Response for Ultrasonic Distance Measurement

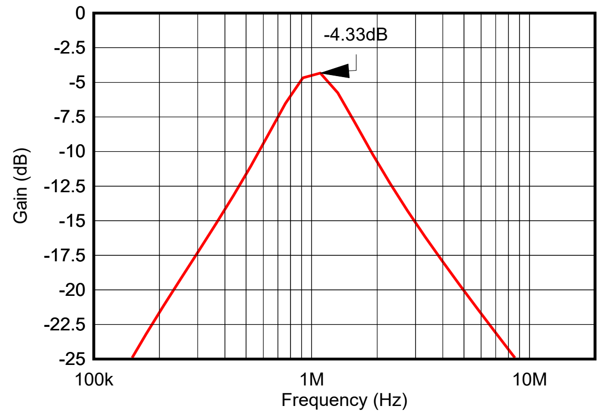


図 8-3. Band-Pass Filter Frequency Response

8.3 Power Supply Recommendations

The LOG300 contains two supply pins. The analog power supply pin (VCC) and the frequency detect block supply pin (Freq_Supply). Both pins can be biased at any voltage between 3V to 5.25V with respect to the AGND. While both these pins are connected to different circuitry internally, TI recommends to connect both of these pins to the same potential. Provide separate decoupling capacitors, resistors, and ferrite beads to these supply pins (see セクション 8.4.2) to maintain sufficient immunity against cross coupling.

The LOG300 is sensitive to the noise coupling through the supply pins. Use a low-pass filter on the supply line with a cutoff frequency less than the incoming frequency signal.

For example if the incoming signal is 100kHz, and the band-pass filter has been tuned to achieve a center frequency of 100kHz, design a RC filter on the supply with a cut off frequency of at least 10kHz. For a higher signal frequency the RC values start diminishing to smaller values and hence the cut off frequency can be parked to any appropriate value.

An external band-pass filter if used between the LNA and the LOG detector block, along with a low-pass filter on the supply pins provides enough power-supply rejection to keep Log_Out unaffected.

8.4 Layout

8.4.1 Layout Guidelines

Follow these instructions to improve the performance and noise immunity of the LOG300:

- Provide a star connection style supply for Freq_supply and VCC. This connection enables better noise immunity and decoupling.
- Design Log_Inp, Log_Inm and LNA_In traces with guard traces to improve immunity against noise pickup. Use shielding when possible to improve radiated noise immunity.
- Place small capacitors on the AFE and LNA enable pins to allow high-frequency noise to be grounded before entering into the device.
- As per セクション 7.3.2 the impedance seen from Log_Inp and Log_Inm to the external circuit must be the same. The trace length to Log_Inp and Log_Inm must be kept similar to keep impedance matched.
- Keep minimal capacitance at the Freq_Out pin either by placing the load circuit close to the pin or by removing the analog ground plane under the output trace or both.
- Dedicate one layer of the PCB for a solid analog ground pour to terminate all the capacitors used across the pins using sufficient vias.

8.4.2 Layout Example

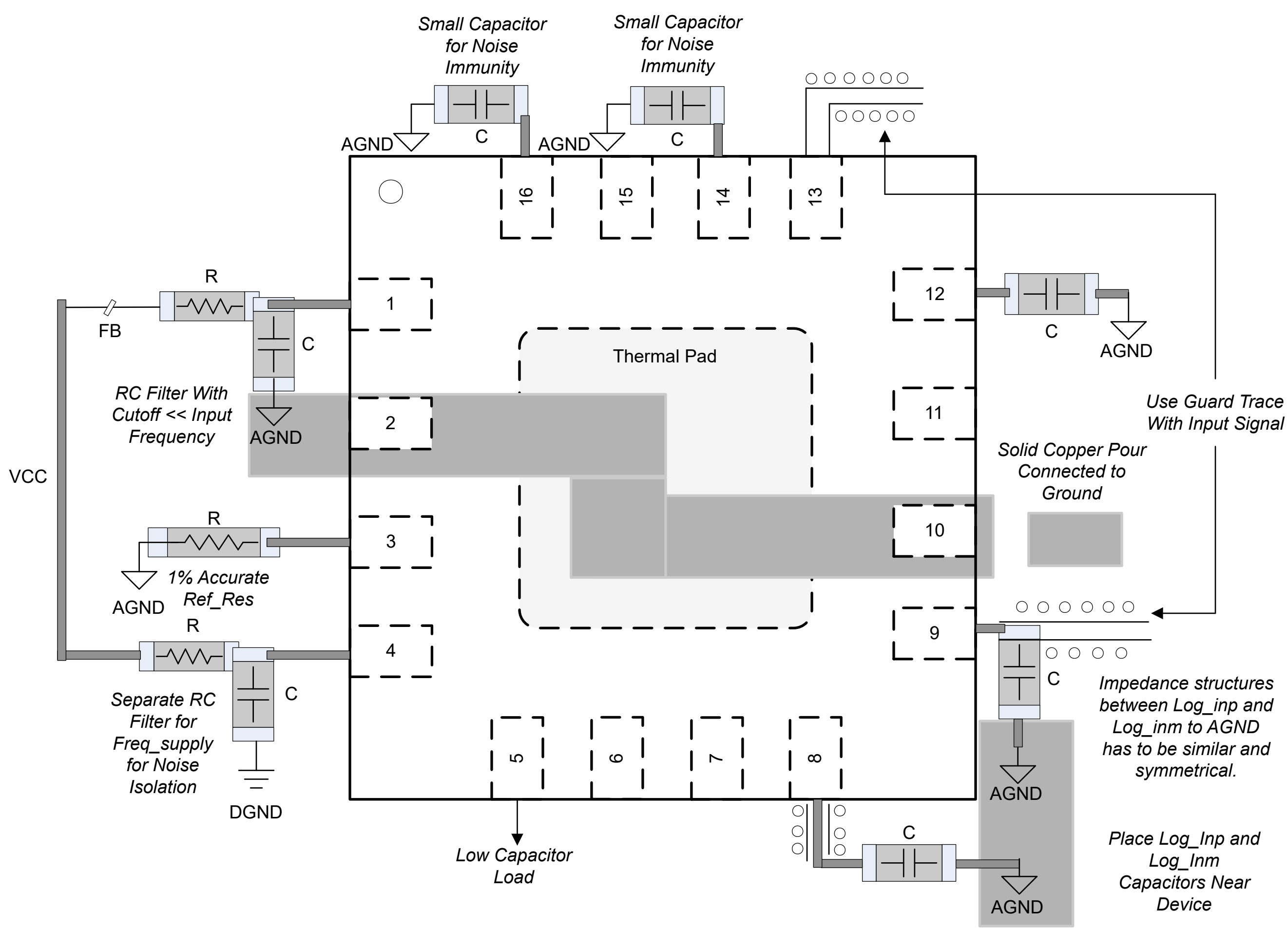


図 8-4. Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2024) to Revision B (December 2024) **Page**

- データシートに RGT パッケージを追加 1
- Added minimum output voltage for RGT package 7
- Changed minimum output voltage at T_A = –40°C to +125°C in Electrical Charecteristics LNA + Log Detector (AFE) 9
- Updated Figure 5-34, *Log-Detector Output at Various Frequencies*, to fix broken X-axis scale 17
- Updated Figure 7-1, *Impedance Structure at Log_Inp and Log_Inm* 20
- Updated Figure 7-2, *Impedance vs Frequency at Log_Inp and Log_Inm* 20

Changes from Revision * (September 2024) to Revision A (October 2024)	Page
• 文書のステータスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LOG300DR	Active	Production	SOIC (D) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LOG300D
LOG300DR.B	Active	Production	SOIC (D) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LOG300D
LOG300RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LOG300
LOG300RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LOG300

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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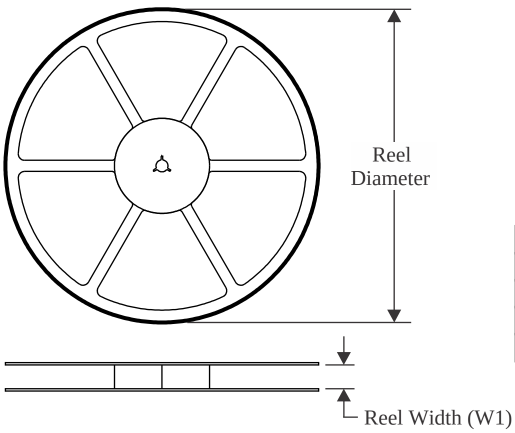
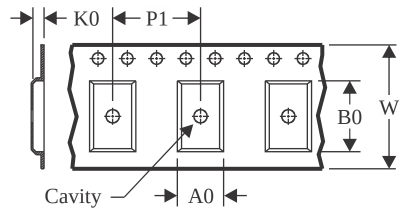
TAPE AND REEL INFORMATION

REEL DIMENSIONS

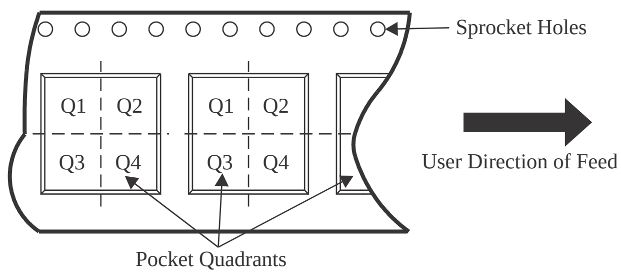


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

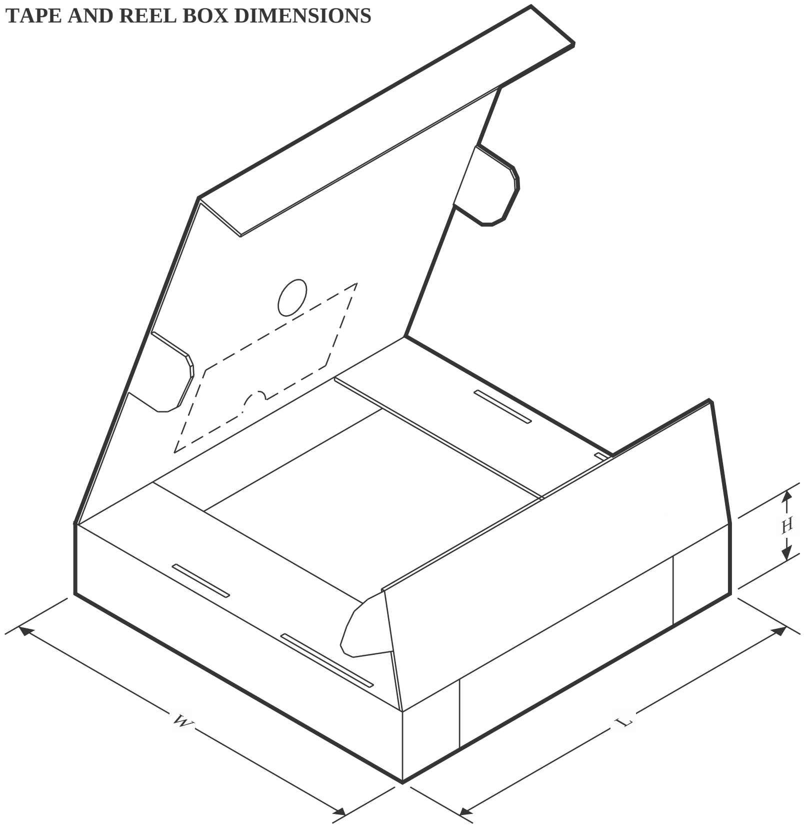
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

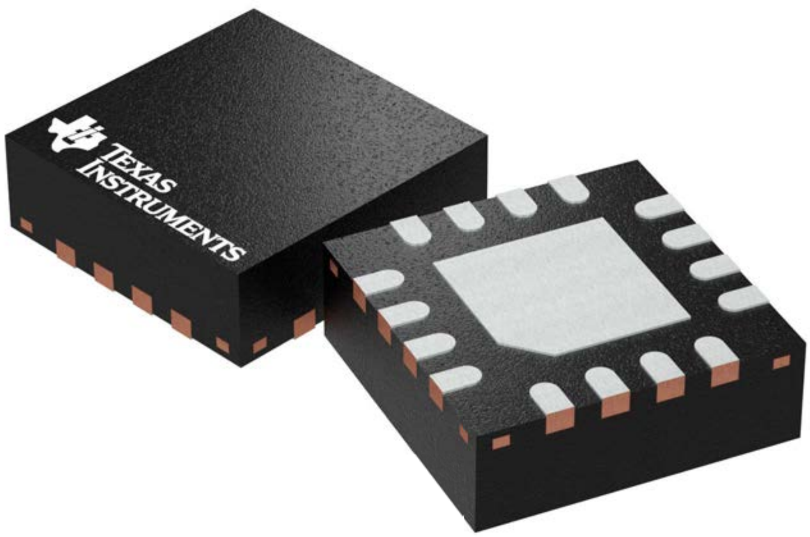
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LOG300DR	SOIC	D	16	3000	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
LOG300RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

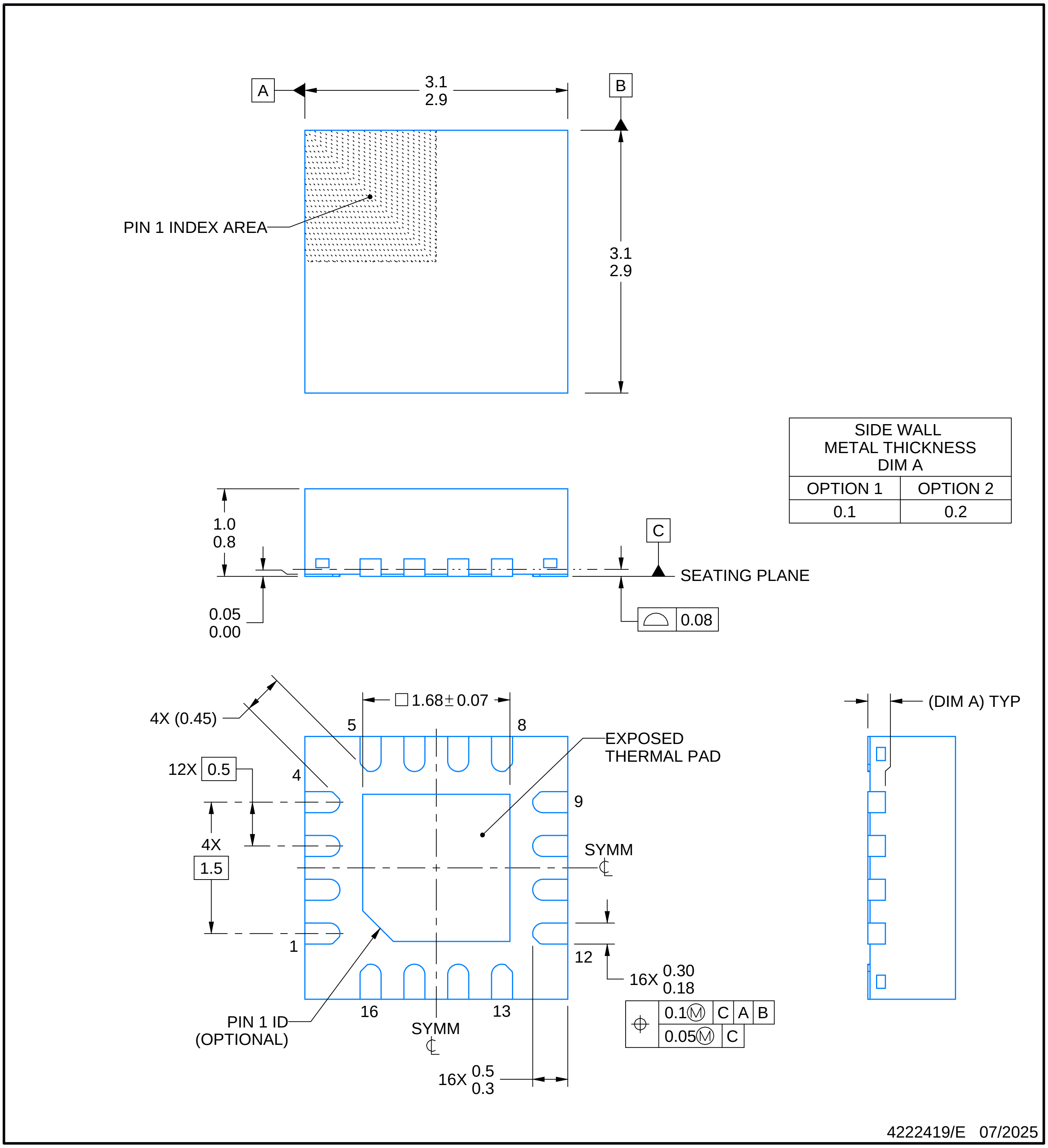


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LOG300DR	SOIC	D	16	3000	353.0	353.0	32.0
LOG300RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0



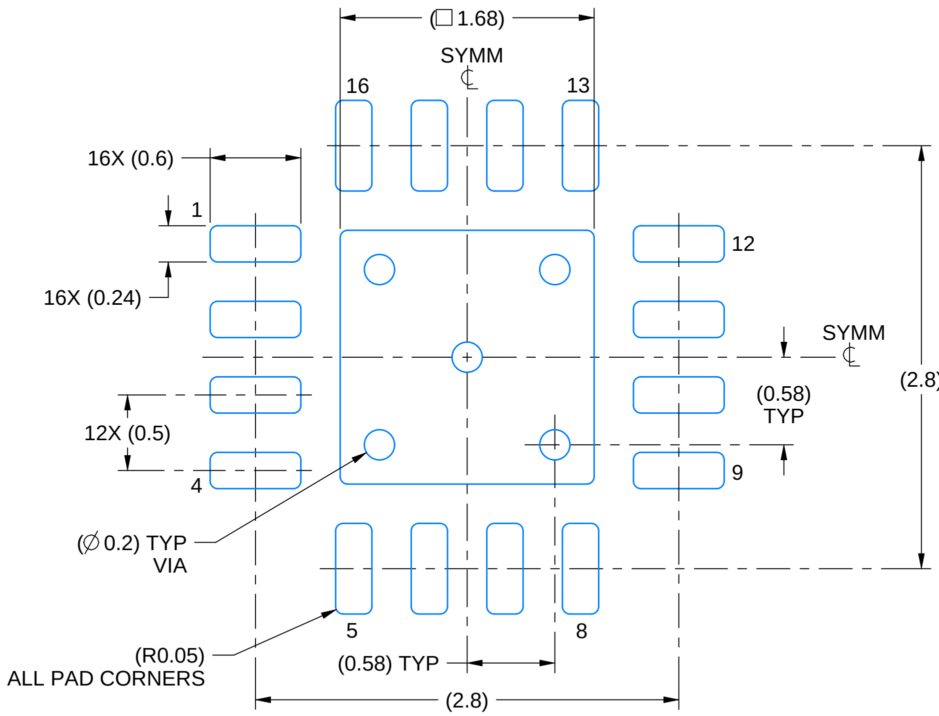
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



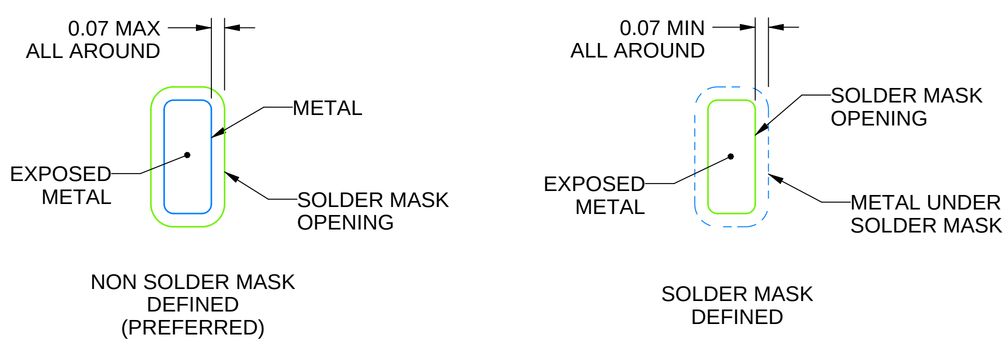
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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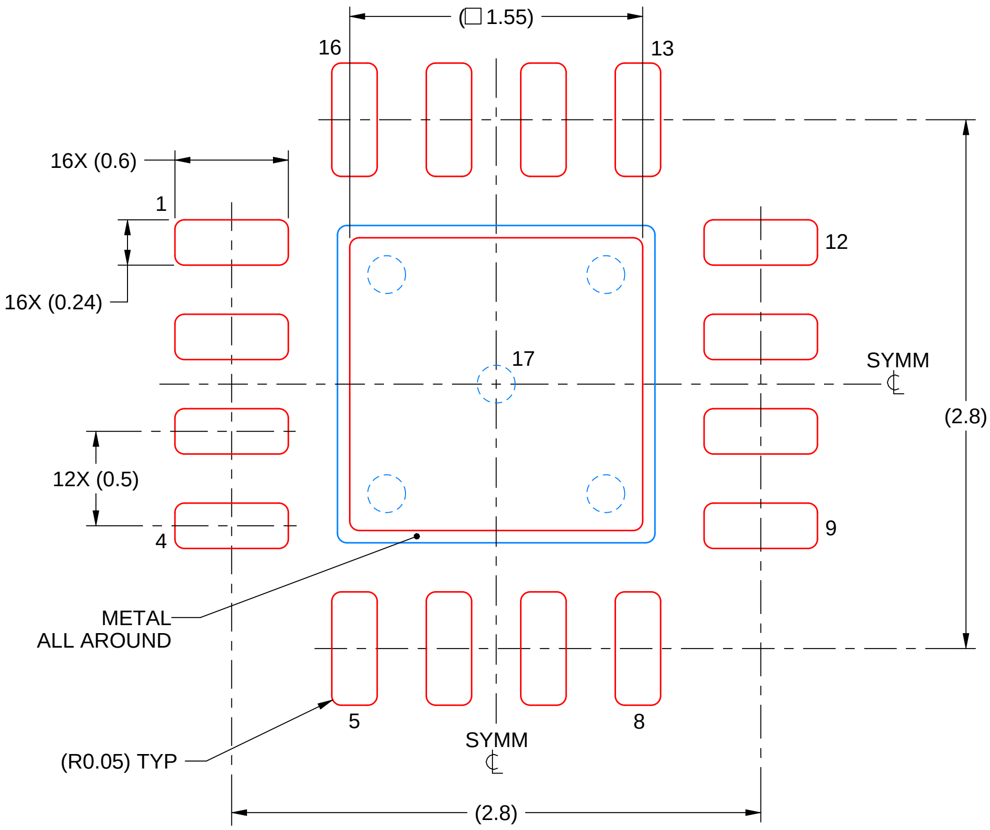
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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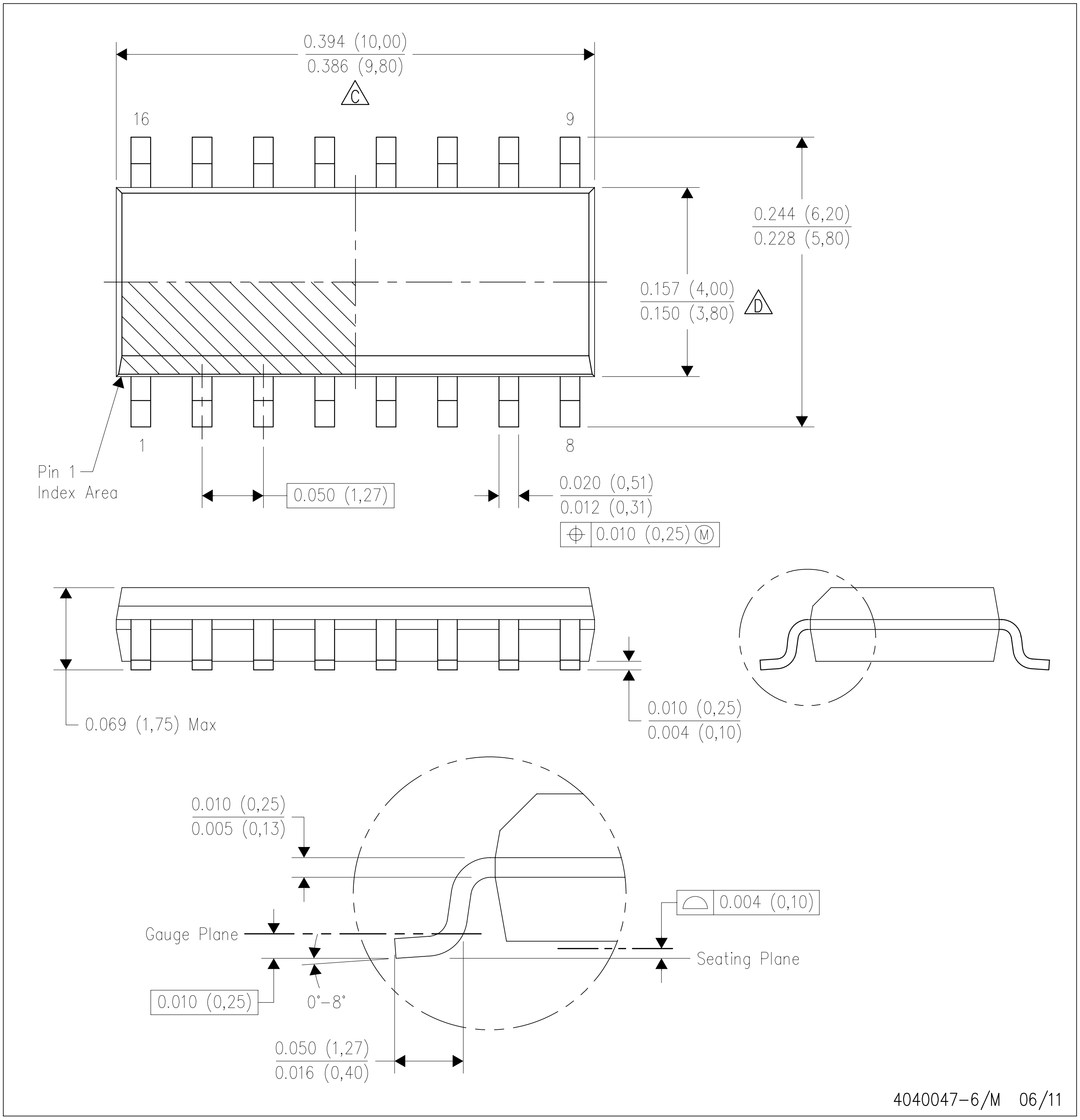
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

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