TEXAS INSTRUMENTS
LMZM23601
JAJSER9C – DECEMBER 2017 – REVISED MARCH 2023

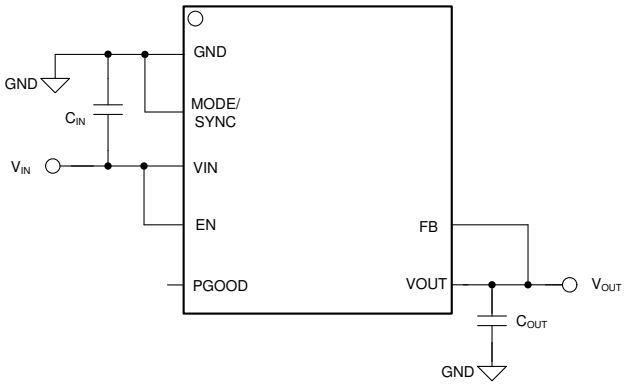
LMZM23601 36V、1A、3.8mm × 3mm パッケージの降圧 DC/DC 電源モジュール

1 特長

- 4V～36V の広い動作入力電圧範囲
- 1.2V～15V 可変、および 3.3V または 5V の固定出力電圧オプション
- 1A の出力電流
- 5V および 3.3V 出力の設計では入力と出力のコンデンサのみ必要
- 片面レイアウトの 27mm^2 ソリューション・サイズ
- 無負荷時の消費電流: 28µA
- シャットダウン時電流: 2µA
- パワー・グッド・フラグ
- 外部周波数同期
- MODE 選択ピン
  - 強制 PWM モードによる固定周波数動作
  - 自動 PFM モードによる軽負荷時の高効率
- 制御ループ補償、ソフト・スタート、電流制限、UVLO を内蔵
- 3.8mm × 3mm × 1.6mm の小型パッケージ
- WEBENCH® Power Designer により、LMZM23601 を使用するカスタム設計を作成

2 アプリケーション

- センサ・トランスミッタ
- 試験 / 測定機器
- グリッド・インフラ
- スペースの制約が厳しいアプリケーション



DC/DC コンバータ、固定出力オプション (24V ～ 5V、1A) の回路図

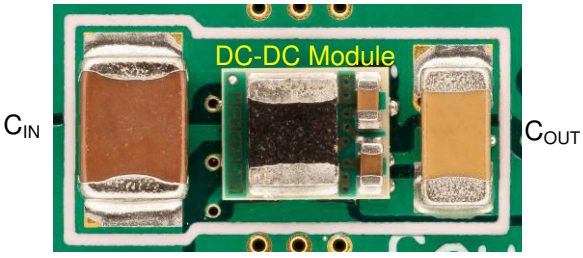
3 概要

LMZM23601 はインダクタが内蔵された電源モジュールで、スペースに制約のある産業用アプリケーションに特化して設計されています。5V と 3.3V の 2 つの固定出力電圧オプションと、1.2V～15V の範囲で可変 (ADJ) の出力電圧オプションで供給されます。LMZM23601 は 4V～36V の入力電圧範囲に対応し、最大 1000mA の出力電流を供給できます。この電源モジュールは非常に使いやすく、5V および 3.3V 出力の設計では、必要な外付け部品はわずか 2 つです。LMZM23601 のすべての特長は、性能重視で低 EMI の、スペースに制限のある産業用アプリケーションに最適化されています。オープン・ドレインのパワー・グッド出力により、システムの真の状態が示されるため、スーパーバイザ部品を追加する必要がなく、コストと基板面積を削減できます。PWM モードと PFM モードとのシームレスな移行、および無負荷時の消費電流がわずか 28µA であることから、負荷電流の範囲全体にわたって高い効率と優れた過渡応答が確保されます。LMZM23601 は 500mA の電流を出力できる LMZM23600 とピン互換で、簡単に出力電流をスケーリングできます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
LMZM23601	SIL (MicroSiP™、10)	3.80mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



片面レイアウト、ソリューション・サイズの 24V～5V の 1A の DC/DC コンバータ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2019) to Revision C (March 2023) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- 商標の情報を更新 1
- Changed the VIN to GND MAX from 42 to 40 5
- Updated the *Functional Block Diagram* 16

Changes from Revision A (April 2018) to Revision B (May 2019) — **Page**

- 可変出力範囲の最小値を 2.5V から 1.2V に変更 1
- Added Maximum input voltage vs output voltage graph for V_{OUT} < 2.5 V, Power dissipation and Output current vs ambient temperature graphs for 1.2-V and 1.8-V outputs 10
- Added information on maximum input voltage for V_{OUT} < 2.5 V 23
- Added output capacitance requirements for 1.2-V and 1.8-V outputs 24
- Added guidance on feedback resistor values for lower output voltages 25
- Added typical application curves for 1.2-V and 1.8-V outputs 27

Changes from Revision * (December 2017) to Revision A (April 2018) — **Page**

- 量産データのデータシートの初版、WEBENCH 用のリンクを追加 1

Device Comparison

表 5-1. LMZM23601 Device Options

PART NUMBER	OUTPUT VOLTAGE	PACKAGE QTY (1)
LMZM23601SILR	Adjustable	3000
LMZM23601V3SILR	3.3 V	3000
LMZM23601V5SILR	5 V	3000
LMZM23601SILT	Adjustable	250
LMZM23601V3SILT	3.3 V	250
LMZM23601V5SILT	5 V	250

(1) See Package Option Addendum for tape and reel details as well as links used to order parts.

5 Pin Configuration and Functions

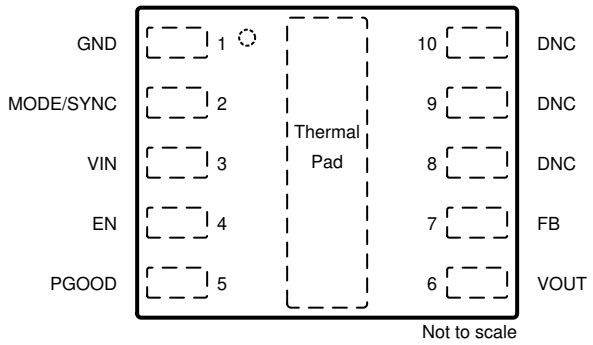


図 5-1. SIL 10-Pin MicroSiP™ Package Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	G	Ground for all circuitry. Reference point for all voltages.
2	MODE/ SYNC	I	This pin is a multifunction mode control input which is tolerant of voltages up to the input voltage. With this input tied LOW, the device is in Auto PFM mode with automatic transition between PFM and PWM with diode emulation at light load. TI recommends this mode when the application requires high efficiency at light load. With this input tied HIGH, the device is in forced PWM mode. The device switches at the internal clock frequency. TI recommends this mode when the application requires constant switching frequency across the entire load current. With a valid synchronization signal at this pin, the device switches in forced PWM mode at the external clock frequency and synchronized with it at the rising edge of the clock. Do not float this pin.
3	VIN	P	Input supply to the regulator. Connect a high-quality bypass capacitors directly to this pin and the GND pin (pin 1).
4	EN	I	Enable input to the regulator. HIGH = ON, LOW = OFF. This pin can be connected to VIN. Do not float.
5	PGOOD	O	Open-drain, power-good output. Connect to a suitable voltage supply through a current limiting resistor. HIGH = power is good, LOW = fault. This output terminal is LOW when EN is LOW.
6	VOUT	O	Output voltage terminal. This pin is internally connected to one terminal of the integrated inductor. Connect an output filter capacitor from VOUT to GND and place the capacitor as close as possible to the VOUT pin.
7	FB	I	Feedback input to the regulator. If using the fixed 3.3-V or 5-V options of the device, connect this pin to the positive end of the output filter capacitor (the VOUT node). If using the adjustable output option of the device connect this to the feedback voltage divider and keep this node as small as possible on the board layout.
8	DNC	O	Do not connect. Leave floating. This pin provides access to the internal VCC voltage of the device.
9	DNC	O	Do not connect. Leave floating. This pin provides access to the internal BOOT voltage for the high side MOSFET driver.
10	DNC	O	Do not connect. Leave floating. This pin provides access to the internal SW voltage of the device.
Thermal Pad	—	G	This terminal is internally connected to GND and provides a wide thermal connection from the IC to the PCB. Connect to electrical ground plane for adequate heat sinking.
G = Ground, I = Input, O = Output, P = Power			

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN to GND	–0.3	40	V
SW to GND	–0.3	V_{IN} + 0.3	V
BOOT to SW	–0.3	3.6	V
EN to GND	–0.3	42	V
VOUT to GND	-0.3	16	V
FB to GND (3.3-V and 5-V options)	–0.3	16	V
FB to GND (ADJ option)	–0.3	5.5	V
PGOOD to GND	–0.3	16	V
PGOOD sink current		8	mA
MODE/SYNC to GND	–0.3	42	V
VCC to GND	-0.3	3.6	V
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4		36	V
V_{OUT}	Output voltage (5 V)	0		5	V
	Output voltage (3.3 V)	0		3.3	V
	Output voltage (ADJ)	1.2		15	V
I_{OUT}	Output current (1 A)	0		1	A
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMZM2360x SIL (µSIP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3	°C/W

THERMAL METRIC(1)		LMZM2360x SIL (µSIP) 10 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	20	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise stated. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK						
V_{FB}	Initial output voltage accuracy (3.3-V and 5-V fixed output)	V_{IN} = 4 V to 36 V, open loop	–1.5%		1.5%	
V_{FB}	Reference voltage (ADJ option)	V_{IN} = 4 V to 36 V, open loop	0.985	1	1.015	V
I_{FB}	Input current from FB to GND (ADJ option)	FB = 1 V		20		nA
CURRENT						
I_Q	Operating quiescent current; measured at VIN pin	V_{IN} = 12 V, V_{FB} = +10%, V_{OUT} = 5 V		7		µA
		V_{IN} = 12 V, V_{FB} = +10%, V_{OUT} = 5 V, T_J = 85°C			16	µA
		V_{IN} = 12 V, V_{FB} = +10%, V_{OUT} = 5 V, T_J = 125°C			18	
		V_{IN} = 24 V, V_{FB} = +10%, V_{OUT} = 5 V		12		
		V_{IN} = 24 V, V_{FB} = +10%, V_{OUT} = 5 V, T_J = 85°C			24	
		V_{IN} = 24 V, V_{FB} = +10%, V_{OUT} = 5 V, T_J = 125°C			26	
I_B	Bias current into the VOUT pin	V_{IN} = 24 V, V_{FB} = +10%, V_{OUT} = 5 V, Mode = 0 V		48	80	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0 V, V_{IN} = 12 V, T_J = 25°C		1.8		µA
		EN = 0 V, V_{IN} = 12 V, T_J = 85°C			3	
		EN = 0 V, V_{IN} = 24 V, T_J = 25°C		5		
		EN = 0 V, V_{IN} = 24 V, T_J = 85°C			10	
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{IN_UVLO}	Minimum input voltage to operate	Rising	3.1	3.5	3.85	V
$V_{IN\_UVLO\_HYST}$	UVLO hysteresis		0.2	0.25	0.3	V

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise stated. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD FLAG (PGOOD)						
V_{PGOOD_OV}	PGOOD upper threshold voltage	Rising, % of Vout	103.5%	106.7%	109%	
V_{PGOOD_UV}	PGOOD lower threshold voltage	Falling, % of Vout	92%	94.7%	97%	
V_{PGOOD_GUARD}	Magnitude of PGOOD lower threshold difference from steady state output voltage.	Steady state output voltage PGOOD threshold read at the same T_J and V_{IN}	4%			
V_{PGOOD_HYST}	PGOOD hysteresis as a percent of output voltage set point			1.4%		
V_{PGOOD_VALID}	Minimum input voltage for proper PGOOD function	50-µA pullup to PGOOD pin, EN = 0 V, T_J = 25°C		1.0	1.5	V
t_{RESET_FILTER}	Glitch filter time constant for PGOOD function			190		µs
V_{OL}	Low-level PGOOD function output voltage	50-µA pullup to PGOOD pin, V_{IN} = 1.5 V, EN = 0 V			0.4	V
		0.5-mA pullup to PGOOD pin, V_{IN} = 12 V, EN = 0 V			0.4	
		1-mA pullup to PGOOD pin, V_{IN} = 12 V, EN = 3.3 V			0.4	
R_{PGOOD_RDSON}	RDSON of the PGOOD output pull down			50	110	Ω
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	V_{IN} = 24 V, 5-V and 3.3-V fixed output options	675	750	825	kHz
		V_{IN} = 24 V, ADJ output options	890	1000	1090	
		V_{IN} = 36 V, 5-V and 3.3-V fixed output options		750		
		V_{IN} = 36 V, ADJ output options		800		
FREQUENCY SYNCHRONIZATION AND MODE						
f_{SYNC}	Sync frequency range	5-V and 3.3-V fixed output options V_{OUT} + $V_{DROPOUT}$ < V_{IN} < 36 V	500		825	kHz
		ADJ output options V_{OUT} + $V_{DROPOUT}$< V_{IN} < 28 V	700		1100	
D_{SYNC}	Sync input duty cycle range	2.3 V < HIGH state input < 5.5 V	25%		75%	
V_{MODE_HIGH}	MODE/SYNC input logic HIGH voltage to enter FPWM mode		1.5			V
V_{MODE_LOW}	MODE/SYNC input logic LOW voltage to enter AUTO PFM mode				0.4	V
I_{MODE}	MODE/SYNC leakage current	V_{IN} = 12 V, $V_{MODE/SYNC}$ = 3.3 V		1		µA
		V_{IN} = 12 V, $V_{MODE/SYNC}$ = 12V		5		
t_{MODE}	MODE transition time to FPWM	V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT}= 20 mA		300		µs
	MODE transition time to AUTO PFM	V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 20 mA		300		
CURRENT LIMIT PROTECTION						
$I_{L\text{-}HS}$	high-side switch current limit	Duty cycle approaches 0%	1.45	1.81	2.2	A
$I_{L\text{-}LS}$	low-side switch current limit		1	1.2	1.43	A
$I_{L\text{-}ZC}$	Zero-cross current limit	MODE/SYNC = logic LOW		–0.01		A

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise stated. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{L-NEG}	Low-side reverse current limit (positive current ino the SW pin to GND)	MODE/SYNC = logic HIGH	0.5	0.8		A
POWER STAGE CHARACTERISTICS						
HS R_{DS-ON}	High-side MOSFET on-resistance			220		mΩ
LS R_{DS-ON}	Low-side MOSFET on-resistance			200		mΩ
t_{ON-MIN}	Minimum high-side on-time	I_{OUT} = 500 mA		50	80	ns
$t_{OFF-MIN}$	Minimum high-side off-time	I_{OUT} = 500 mA, ADJ		62	100	ns
D_{MAX}	Maximum switch duty cycle	5-V and 3.3-V fixed output options		93%		
		ADJ option		91%		
		While in frequency foldback		97%		
L	Integrated inductor - inductance			10		µH
L_{DCR}	Integrated inductor - DCR			390		mΩ
ENABLE						
V_{EN}	Enable input threshold voltage	Rising	1.7		1.92	V
V_{EN_HYST}	Enable input threshold hysteresis		0.42		0.52	V
V_{EN_WAKE}	Enable input wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 12 V		2.7		µA
VCC REGULATOR						
V_{CC}	Internal V_{CC} voltage	V_{IN} = 12 V, V_{OUT} < 3.3 V		3.05		V
		V_{IN} = 12 V, V_{OUT} ≥ 3.3V		3.15		
V_{CC_UVLO}	Internal V_{CC} voltage input UVLO	V_{IN} rising	2.23	2.73	3.25	V
$V_{CC\_UVLO\_HYST}$	Internal V_{CC} voltage input UVLO hysteresis	Hysteresis below VCC_UVLO	150		240	mV
SOFT START						
t_{SS}	Soft-start time	Time for V_{REF} to ramp from 0% to 90%	1.8	3.5	5.5	ms
t_{EN_LV}	Turnon delay with low V_{IN}	V_{IN} < 4.2 V		4		ms
t_{EN}	Turnon delay	V_{IN} = 12 V		0.7		ms
t_W	Short circuit wait time (hiccup time)			8.0		ms
THERMAL PROTECTION						
T_{SD}	Thermal shutdown	Rising threshold		155		°C
T_{SD_HYST}	Thermal shutdown hysteresis			15		°C

6.6 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{Q-VIN}	Input current to the DC-DC converter while in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, fixed output option, EN connected to V_{IN}		25		µA
		V_{IN} =12 V, V_{OUT} = 5 V, I_{OUT} = 0 A, fixed output option, EN connected to V_{IN}		32		
		V_{IN} =24 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, fixed output option, EN connected to V_{IN}		24		
		V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 0 A, fixed output option, EN connected to V_{IN}		28		
EFFICIENCY						
Efficiency	Typical efficiency 12-V input	V_{IN} =12 V, V_{OUT} = 5 V, I_{OUT} = 1 A		87%		
Efficiency	Typical efficiency 12-V input	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A		81%		
Efficiency	Typical efficiency 24-V input	V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 1 A		85%		
Efficiency	Typical efficiency 24-V input	V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A		79%		
Efficiency	Typical efficiency 24-V input	V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 1 A		92%		

6.7 Typical Characteristics

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.

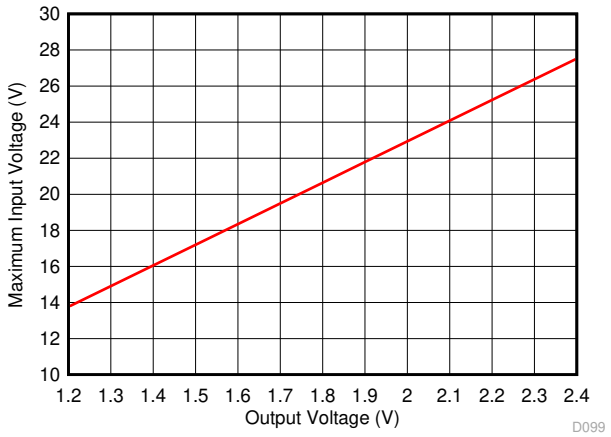
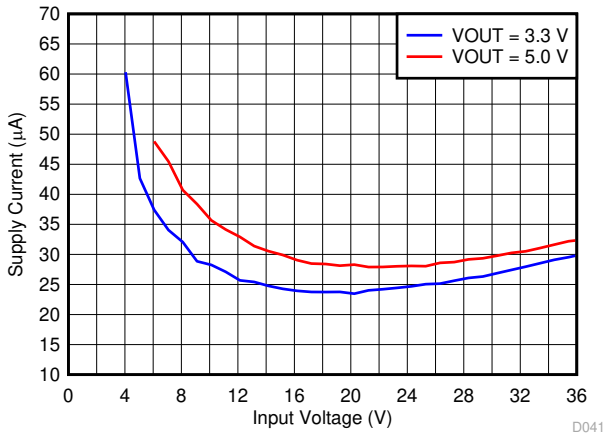
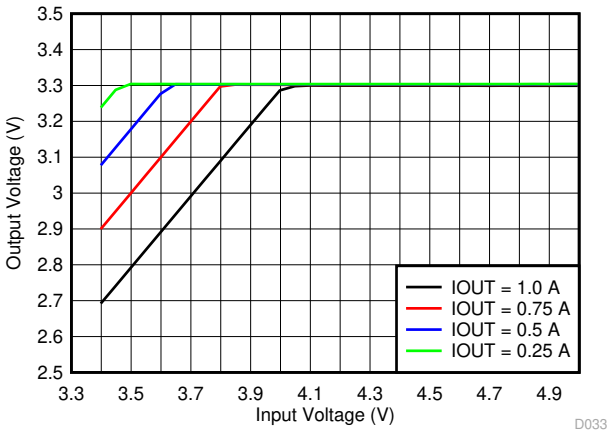


図 6-1. Maximum Input Voltage for V_{OUT} < 2.5V



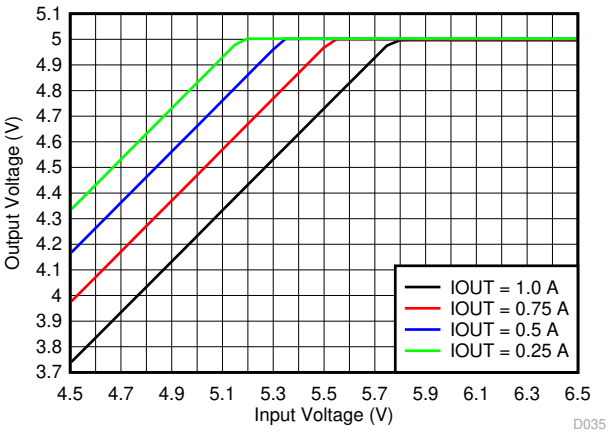
Fixed output voltage options
Output voltage in regulation
EN = VIN
Load = Open

図 6-2. Input Supply Current



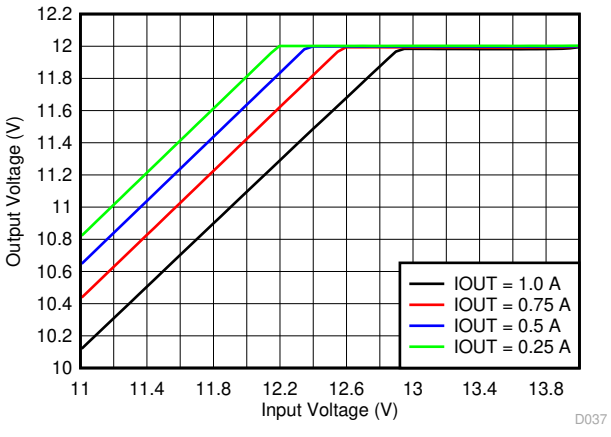
V_{OUT} = 3.3 V

図 6-3. Dropout Voltage



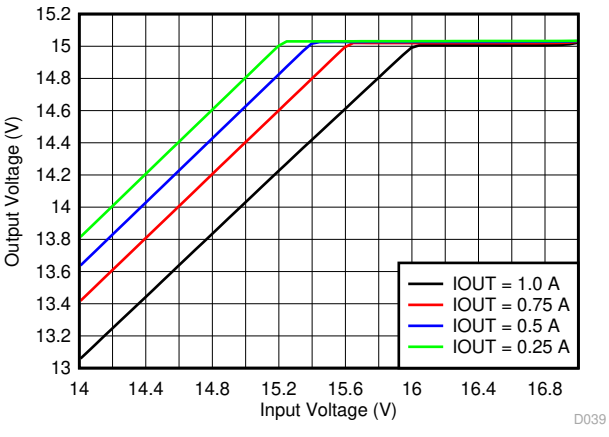
V_{OUT} = 5 V

図 6-4. Dropout Voltage



V_{OUT} = 12 V

図 6-5. Dropout Voltage

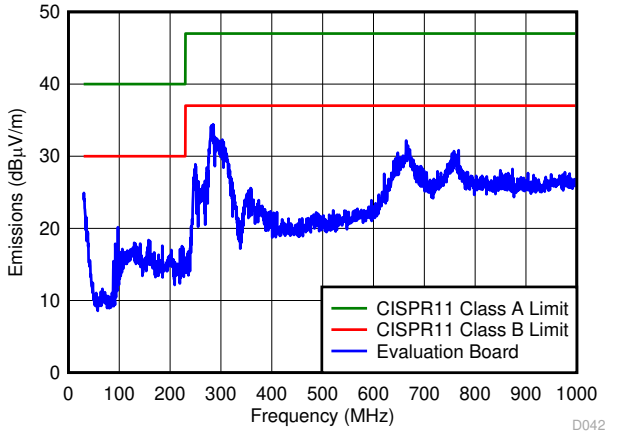


V_{OUT} = 15 V

図 6-6. Dropout Voltage

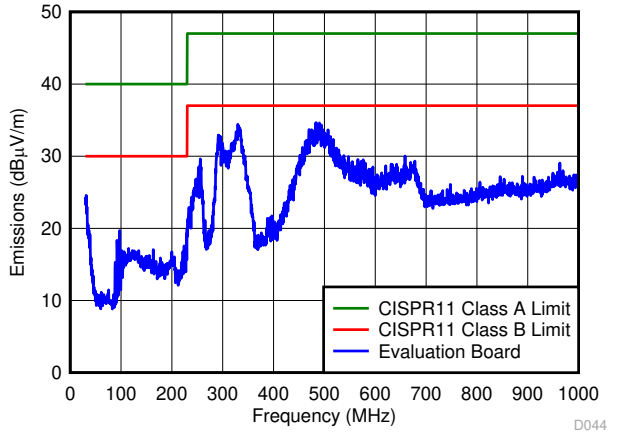
6.7 Typical Characteristics (continued)

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 1 A
Default EVM Layout with added 3 × 100pF 0603 C_{IN}

図 6-7. Radiated EMI



V_{IN} = 24 V I_{OUT} = 1 A V_{OUT} = 5 V
Default EVM BOM with GND Plane as Top Layer

図 6-8. Radiated EMI

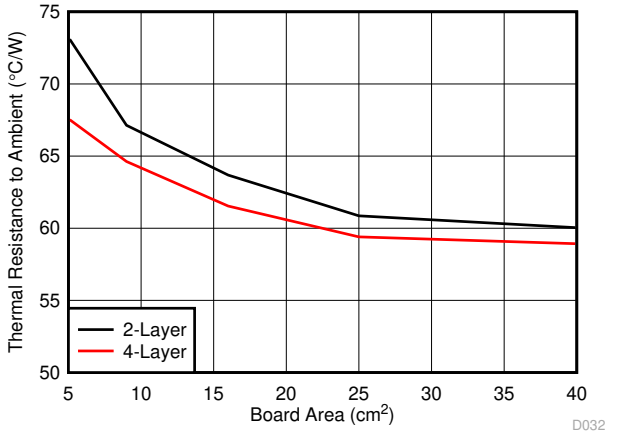
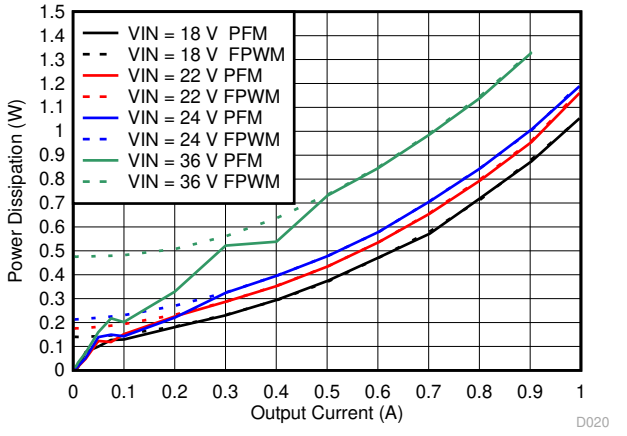
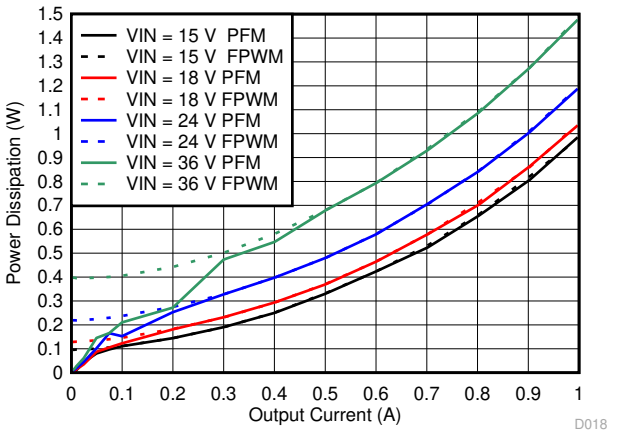


図 6-9. Package Thermal Resistance vs Board Copper Area, No Air Flow



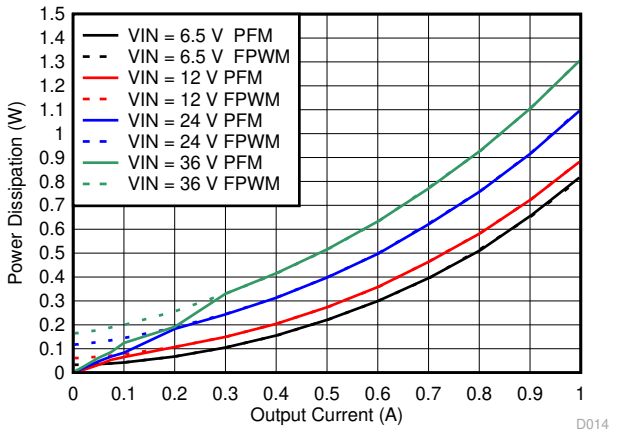
V_{OUT} = 15 V

図 6-10. Power Dissipation



V_{OUT} = 12 V

図 6-11. Power Dissipation

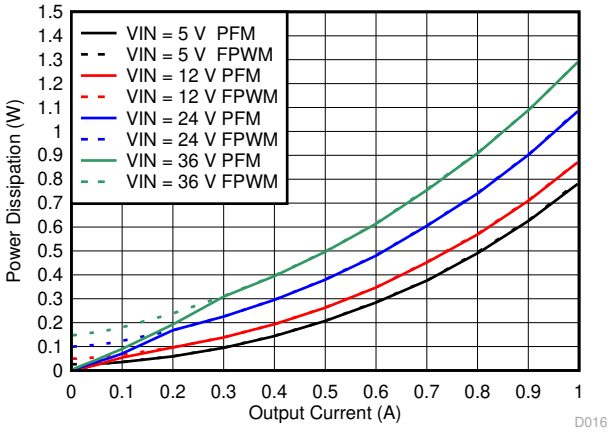


V_{OUT} = 5 V

図 6-12. Power Dissipation

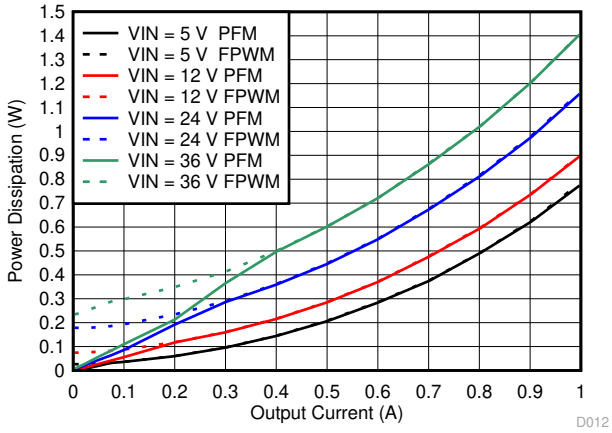
6.7 Typical Characteristics (continued)

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.



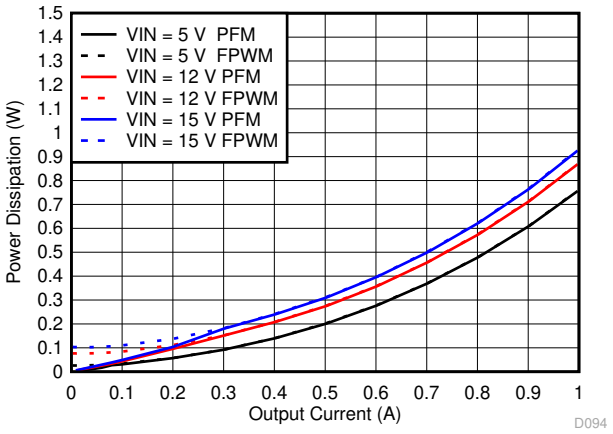
V_{OUT} = 3.3 V

図 6-13. Power Dissipation



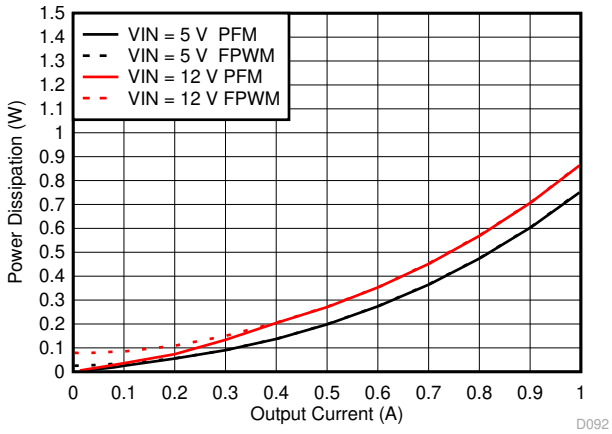
V_{OUT} = 2.5 V

図 6-14. Power Dissipation



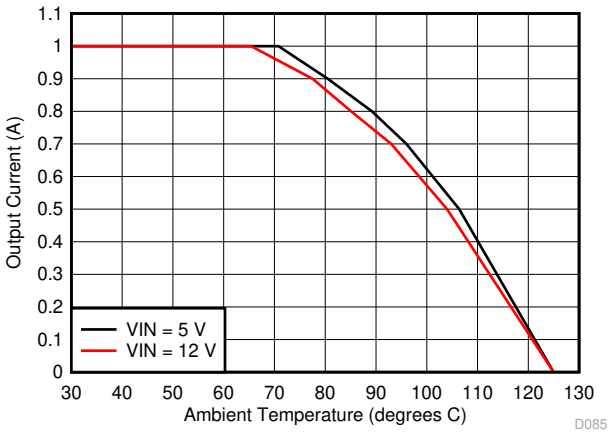
V_{OUT} = 1.8 V

図 6-15. Power Dissipation



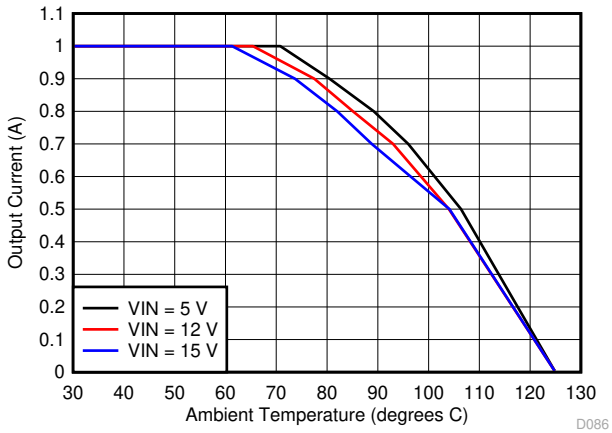
V_{OUT} = 1.2 V

図 6-16. Power Dissipation



V_{OUT} = 1.2 V R_θ = 58°C/W

図 6-17. Ambient Temperature vs Output Current

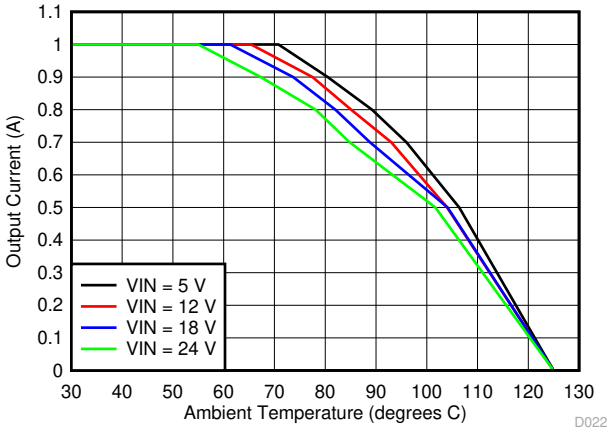


V_{OUT} = 1.8V R_θ = 58°C/W

図 6-18. Ambient Temperature vs Output Current

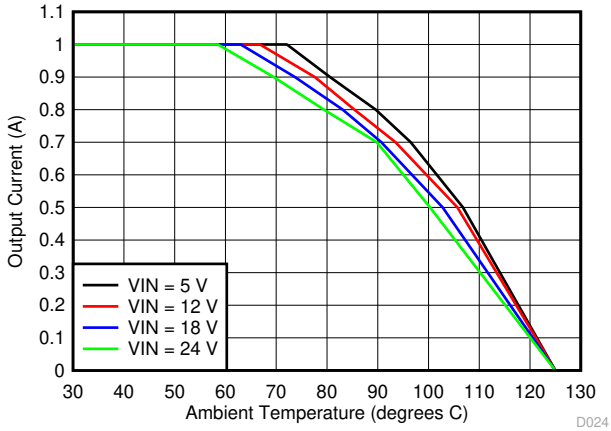
6.7 Typical Characteristics (continued)

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.



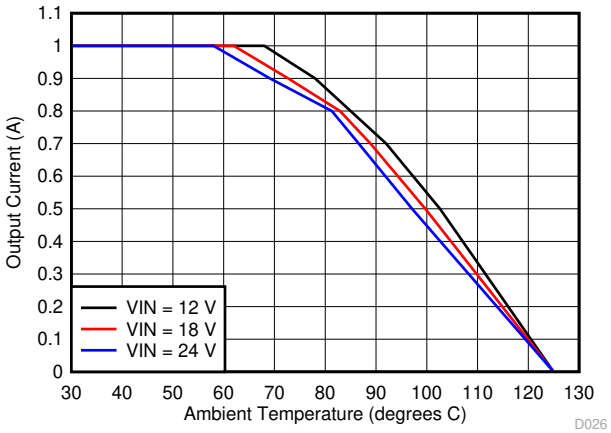
V_{OUT} = 2.5 V R_θ = 58°C/W

図 6-19. Ambient Temperature vs Output Current



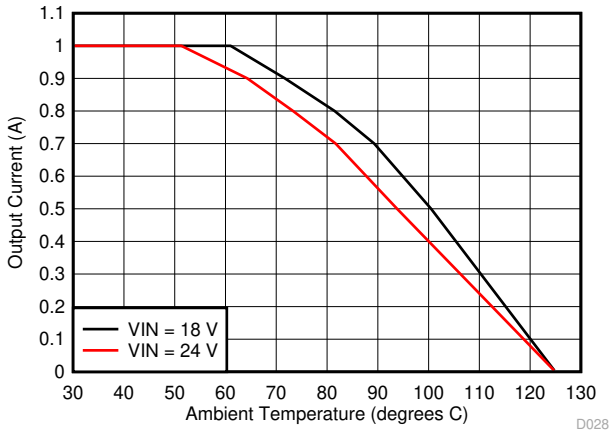
V_{OUT} = 3.3 V R_θ = 58°C/W

図 6-20. Ambient Temperature vs Output Current



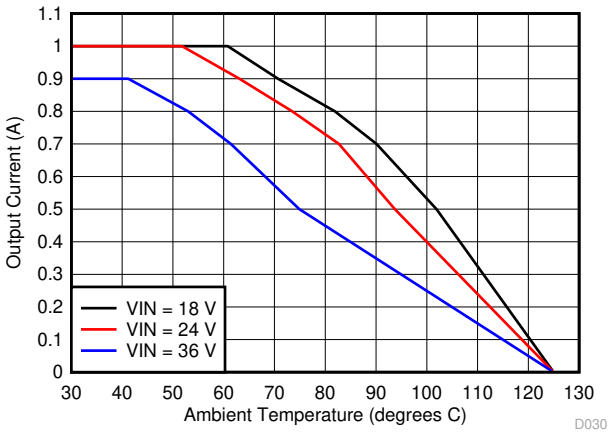
V_{OUT} = 5 V R_θ = 58°C/W

図 6-21. Ambient Temperature vs Output Current



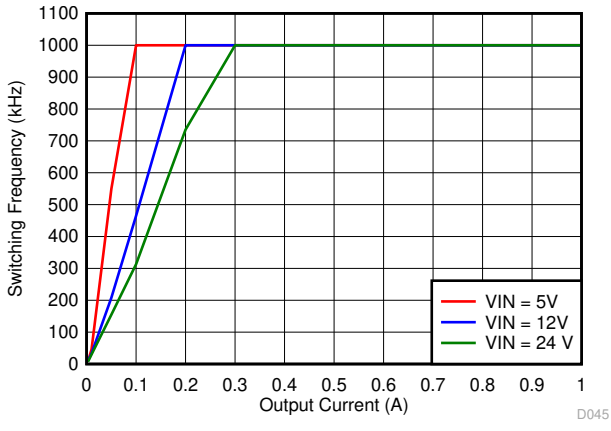
V_{OUT} = 12 V R_θ = 58°C/W

図 6-22. Ambient Temperature vs Output Current



V_{OUT} = 15 V R_θ = 58°C/W

図 6-23. Ambient Temperature vs Output Current

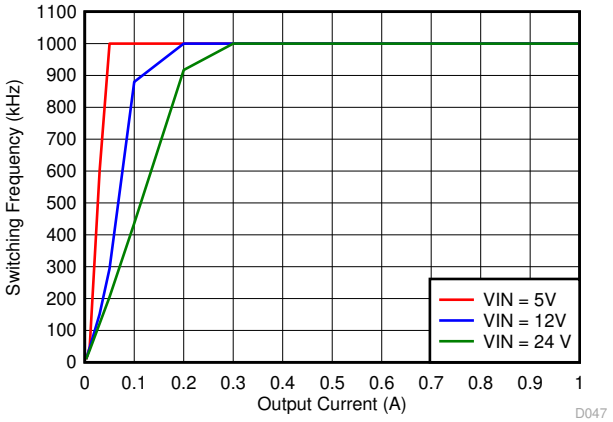


V_{OUT} = 2.5 V

図 6-24. Auto PFM Mode Switching Frequency vs Output Current

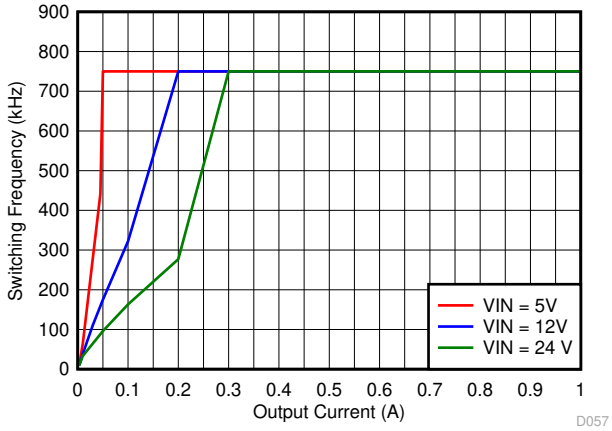
6.7 Typical Characteristics (continued)

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.



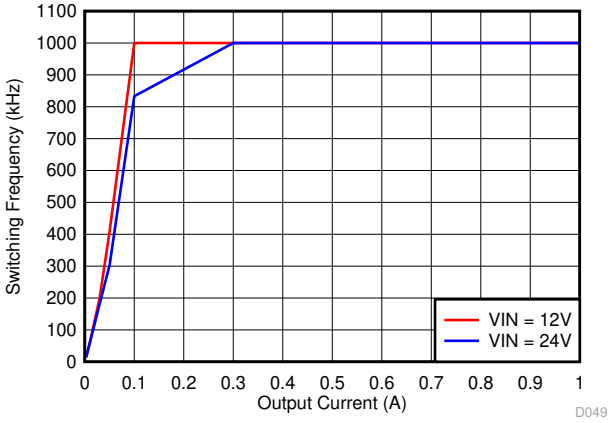
V_{OUT} = 3.3 V Adjustable Option

図 6-25. Auto PFM Mode Switching Frequency vs Output Current



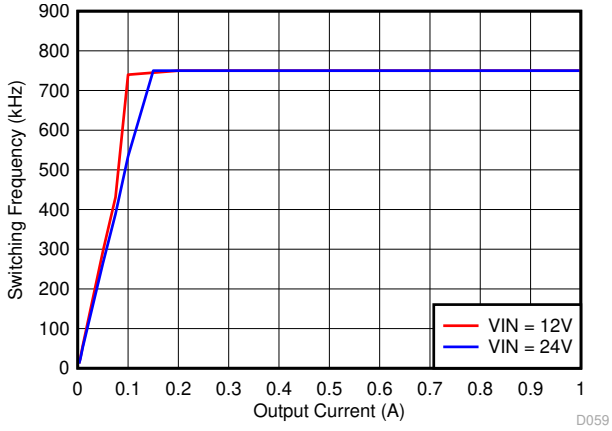
V_{OUT} = 3.3 V Fixed Option

図 6-26. Auto PFM Mode Switching Frequency vs Output Current



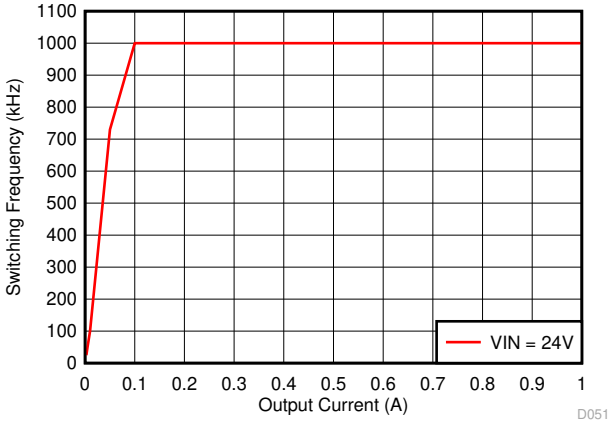
V_{OUT} = 5 V Adjustable Option

図 6-27. Auto PFM Mode Switching Frequency vs Output Current



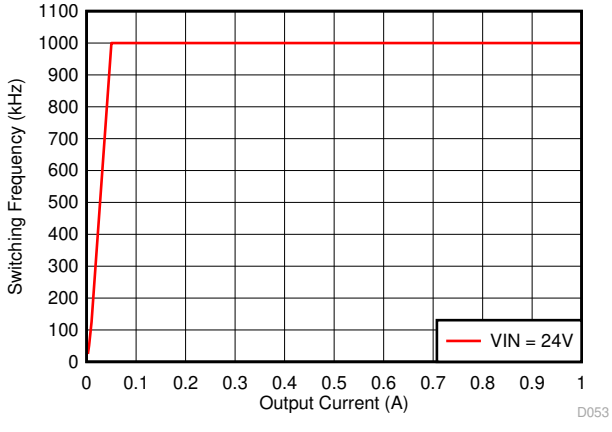
V_{OUT} = 5 V Fixed Option

図 6-28. Auto PFM Mode Switching Frequency vs Output Current



V_{OUT} = 12 V

図 6-29. Auto PFM Mode Switching Frequency vs Output Current



V_{OUT} = 15 V

図 6-30. Auto PFM Mode Switching Frequency vs Output Current

6.7 Typical Characteristics (continued)

V_{IN} = 24 V, T_A = 25°C (unless otherwise noted). Refer to default evaluation board layout and bill of materials.

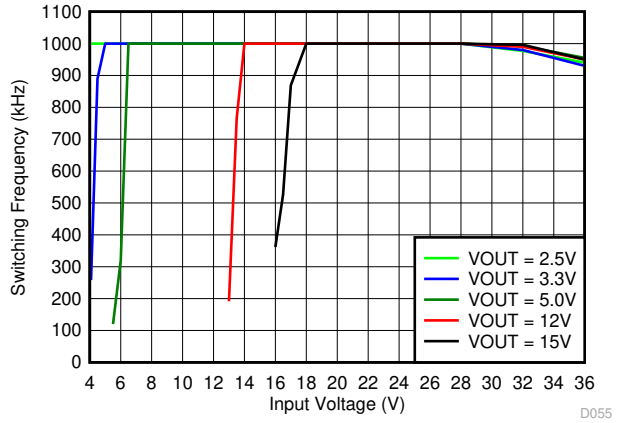


図 6-31. Switching Frequency vs Input Voltage for Adjustable Output Options at Full Load

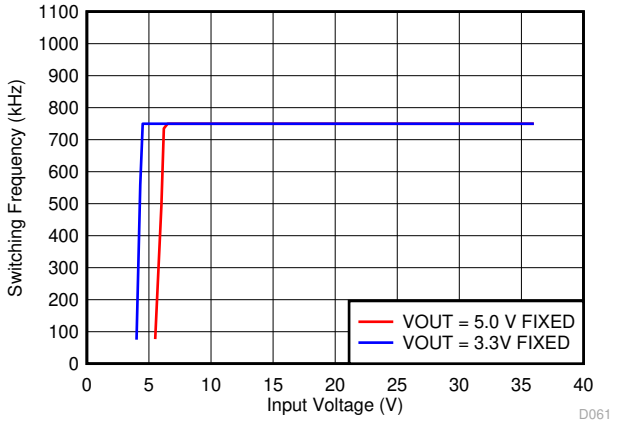


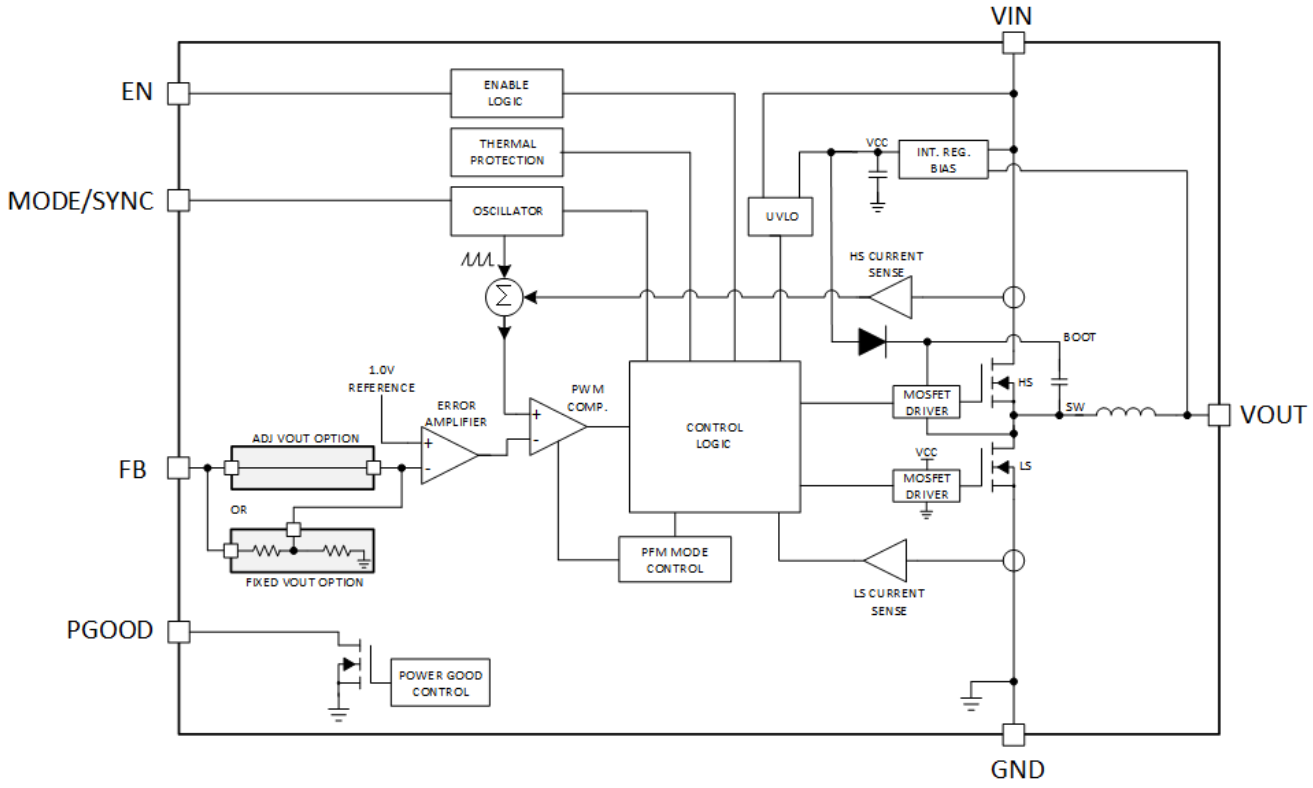
図 6-32. Switching Frequency vs Input Voltage for Fixed Output Options at Full Load

7 Detailed Description

7.1 Overview

The LMZM23601 is a 4-V to 36-V wide-input voltage range, low quiescent current, high-performance DC/DC module designed specifically for space-constrained industrial applications. The device is available in an adjustable output voltage option with 1.2-V to 15-V output range, as well as fixed 5-V and 3.3-V output options. The high level of integration and innovative packaging technology utilized in this power module makes it possible to design a 5-V or a 3.3-V 1-A DC/DC converter with only an input capacitor and an output capacitor in just 27 mm² of available board space.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Scheme

The LMZM23601 power module utilizes peak-current-mode-control architecture. This enables the use of wide range of input voltages while maintaining constant switching frequency and good input and output transient response. The device can be used with 5-V, 12-V, or 24-V typical industrial input voltage rail. The short minimum on- and off-times ensure constant frequency regulation over a wide range of input to output voltage conversion ratios. The adjustable (ADJ) output voltage option operates at 1000-kHz switching frequency. The minimum on- and off- times allow for a duty factor window of 5% to 91% at 1000-kHz switching frequency. If the input voltage exceeds approximately 28 V on the ADJ version, the frequency is smoothly reduced from 1000 kHz as a function of input voltage. The switching frequency reduction allows output voltage regulation and the current mode control to operate with a duty factor below 5%. The fixed 5-V and 3.3-V output options operate at 750 kHz nominal switching frequency and the frequency foldback at high input voltage is not active or needed.

The control architecture also uses frequency foldback at low input voltage to achieve low dropout voltage, maintaining output regulation as the input voltage falls close to output voltage. The frequency foldback at low input voltage is active for the ADJ as well as the 5-V and 3.3-V output options. The reduction in frequency is smooth and continuous and is activated as the off-time approaches the minimum value. Under these conditions, the LMZM23601 device operates much like a constant off-time converter allowing the maximum duty cycle to reach 97%. This feature allows output voltage regulation with very low dropout.

The LMZM23601 features exceptional conversion efficiency at light load. As the load current is reduced, the LMZM23601 transitions to light-load mode if the MODE/SYNC terminal is pulled low. In light-load mode the device uses diode emulation to reduce the RMS inductor current and the switching frequency is reduced. The fixed voltage versions (3.3-V and 5-V) do not need an external voltage divider connected to FB, which results in saving two components and lower standby current when the load is in standby. As a result, the consumed supply current is only 24 µA (typical) with 24-V to 3.3-V conversion and 28 µA (typical) with 24-V to 5-V conversion, while the output is regulated with no load.

7.3.2 Soft-Start Function

The LMZM23601 features an internally programmed soft-start time. The soft-start time is fixed internally at about 4 ms and is achieved by ramping the internal reference. The device starts up properly even if there is a voltage present on output before the activation of the LMZM23601. In such cases, there is no switching until the output voltage value programmed by the ramping reference voltage is above the pre-biased output value. After the prebiased voltage level is reached by the reference ramp, the switching starts, and the output ramps up smoothly from the pre-biased value up to the final output voltage.

7.3.3 Enable and External UVLO Function

Some applications can require a precision enable or custom input voltage lockout (UVLO) functionality. Setting up external UVLO based on the application needs prevents the converter from trying to regulate the output voltage until after the input voltage has reached a desired minimum level. Such function can be used to lower the current demand from the input supply as the supply is still starting up.

The LMZM23601 features a precision enable (EN) input terminal. The EN input logic has two internal thresholds. The first rising threshold is at 0.9V typical. Its purpose is to wake up the internal VCC regulator to bias the internal circuitry. The EN rising threshold to start switching is 1.8V (typical) with 0.5V (typical) hysteresis. A voltage divider from VIN to EN can be used to set the VIN voltage at which the regulator starts the voltage conversion. The EN terminal is rated for up to the input voltage and can be connected directly to VIN for an always-on operation. Pulling the EN pin below 0.4 V puts the LMZM23601 in shutdown mode. In shutdown mode and 12-V input voltage the LMZM23601 only consumes 1.8 µA (typical) of input current.

7.3.4 Current Limit

The LMZM23601 devices features two current limits inside the IC. A coarse high side or peak current limit is provided to protect against faults. The high-side current limit limits the duration of the on-period of the high-side power MOSFET during a given clock cycle. A precision cycle-by-cycle valley current limit prevents excessive average output current. A new switching cycle is not initiated until the inductor current drops below the valley current limit.

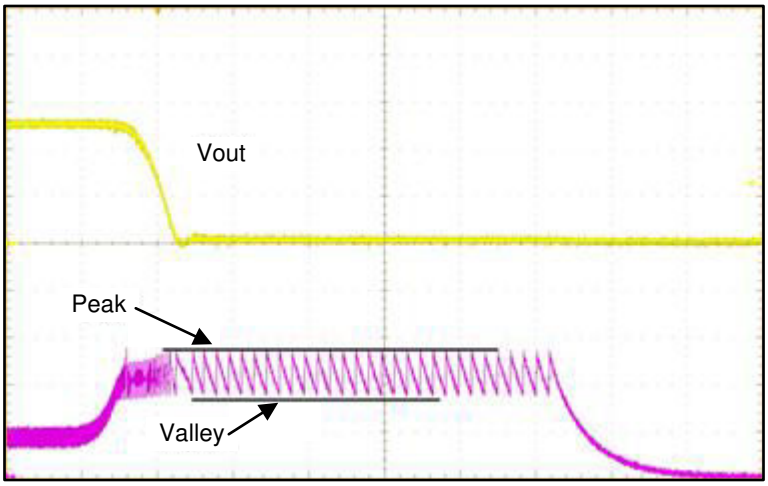


図 7-1. Current Limit Operation During Output Short Circuit

図 7-1 shows the response of the LMZM23601 device to a short circuit on the output: The peak current limit prevents excessive peak current while the valley current limit prevents excessive average inductor current. After a small number of cycles, hiccup mode is activated.

7.3.5 Hiccup Mode

To prevent excessive heating and power consumption under sustained output short-circuit conditions, a hiccup mode operation is included in the control logic. If an over current condition is maintained on the output, the LMZM23601 device shuts off both power MOSFETs and waits for a hiccup interval, t_W, of approximately 8 ms. After the wait period, the device restarts operation beginning with a soft-start time interval.

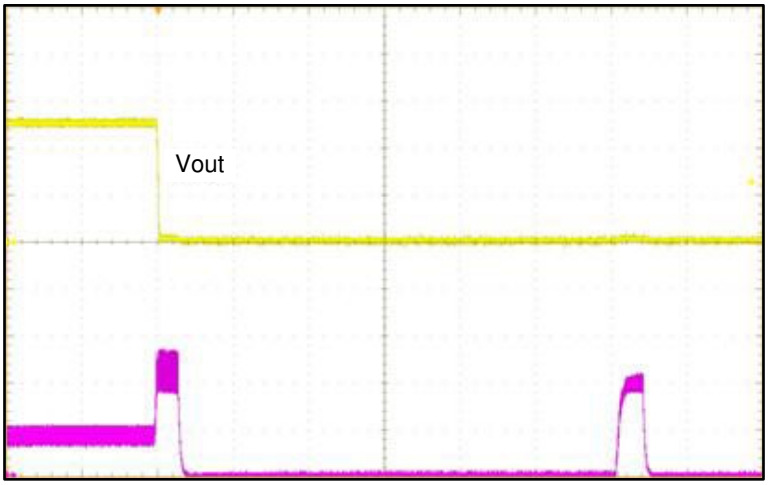


図 7-2. Hiccup Operation

図 7-2 shows hiccup mode operation: The LMZM23601 attempts to restart periodically, following a hiccup wait interval. If the fault at the output is still present, another hiccup wait interval is initiated, followed by another restart attempt. This sequence continues until the output short circuit is removed. When the output short circuit is removed, the output ramps up during the next restart sequence.

7.3.6 Power Good (PGOOD) Function

The LMZM23601 has a built-in power-good signal presented at the PGOOD terminal. This signal indicates whether the output voltage is within the regulation window. The PGOOD terminal is an open-drain output that requires a pullup resistor to a nominal voltage source of 15 V or less. The absolute maximum PGOOD sink

current is 8 mA. Typically, TI recommends a pullup resistor value between 10 kΩ and 100 kΩ. Refer to *Electrical Characteristics* for the power-good thresholds and hysteresis for undervoltage and overvoltage detection.

7.3.7 MODE/SYNC Function

7.3.7.1 Forced PWM Mode

When constant frequency operation is more important than light load efficiency, the MODE/SYNC input of the LMZM23601 device must be pulled high or a valid synchronization input must be provided. This activates forced-PWM-mode operation. After activated, this feature ensures that the switching frequency stays constant across the entire load current range, while operating between the minimum and maximum duty cycle limits. The diode emulation feature is turned off in this mode. This means that the device remains in CCM under light loads. The switching frequency in forced PWM mode is only reduced when the input voltage-to-output voltage ratio results in minimum on-time limitation (ADJ version only) or minimum off-time limitation near dropout.

This feature can be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually, preventing perturbation of output voltage. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulators output to its input.

7.3.7.2 Auto PFM Mode

If the MODE/SYNC terminal is held low the LMZM23601 device enables automatic power-saving-mode transition at light load. With high load the LMZM23601 regulates the output using normal PWM operation. When the load is light, the control logic smoothly transitions to PFM operation and diode emulation. In this mode, the high side MOSFET is turned on for one or more pulses to provide energy to the load. The on-time of the high side in this mode depends on the input voltage level and a pre-programmed internal $I_{PEAK-MIN}$ current level. The higher the input voltage is, the shorter the on-time is. At this point, there is a longer off-time during which the output is still in the regulation window because the load is light, and the output is not getting discharged as quickly. The duration of the off-time depends on the load current level. Lighter load results in longer off-time. This mode of operation results in excellent conversion efficiency at very light load. When auto-PFM mode is used, the output voltage at no load is approximately 1% higher than FPWM operation.

7.3.7.3 Dropout Mode

When the input voltage level decreases and approaches the output voltage level, the buck regulator reaches its maximum duty cycle or minimum off-time requirement for each switching cycle. At this point the output is no longer regulated and follows the input voltage minus the voltage drops from V_{IN} to V_{OUT}.

To maximize the input voltage range for which the output is still regulated, the LMZM23601 features frequency foldback at low input voltage. This operation extends the switching period and, for a given fixed minimum off-time, it prolongs the maximum duty cycle of the regulator. As a result, the output voltage can still be well regulated even as the input voltage level is very close to the output voltage. This feature can be useful for battery applications (maximizing the useful battery range) or in applications where large input voltage variations can be expected.

7.3.7.4 SYNC Operation

Synchronizing the switching frequency of multiple regulators in a single system is often desirable. This technique results in better defined EMI behavior and can reduce the need for capacitance on some power rails. The LMZM23601 MODE/SYNC input allows synchronization to an external clock. The LMZM23601 implements an in-phase locking scheme – the rising edge of the clock signal provided to the input of the LMZM23601 device corresponds to turning on the high-side MOSFET device. This function is implemented using phase locking over a limited frequency range eliminating large glitches upon initial application of an external clock. The clock fed into the LMZM23601 device replaces the internal free-running clock but does not affect frequency foldback operation. The foldback function takes over and the output voltage continues to be well regulated using frequency reduction when duty factors outside of the normal duty cycle range are reached. When the device is synchronized to the lower end of the synchronization range the internal inductor sees higher peak currents. For high current ripple designs (for example, high input voltage and 12-V and 15-V output designs), the maximum current capability of the device can be derated.

The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC function logic always prioritizes the proper regulation of the output voltage. 表 7-1 summarizes the MODE/SYNC function and the operating switching frequency with various conditions. See セクション 6.7 for frequency foldback vs input voltage behavior.

表 7-1. Switching Frequency and MODE/SYNC Function

DEVICE	SWITCHING FREQUENCY				
	MODE/SYNC	LIGHT LOAD	FULL LOAD	VIN > 28 V	IN DROPOUT MODE
ADJ Output	Logic LOW = Auto PFM	Reduced (save power)	Fixed 1000 kHz	Reduced (maintain regulation)	Reduced (maintain regulation)
	Logic HIGH = FPWM	Fixed 1000 kHz	Fixed 1000 kHz	Reduced (maintain regulation)	Reduced (maintain regulation)
	Valid F_{SYNC} Input	F_{SYNC}	F_{SYNC}	Reduced (maintain regulation)	Reduced (maintain regulation)
Fixed 3.3-V Output or 5-V Output	Logic LOW = Auto PFM	Reduced (save power)	Fixed 750 kHz	Fixed 750 kHz	Reduced (maintain regulation)
	Logic HIGH = FPWM	Fixed 750 kHz	Fixed 750 kHz	Fixed 750 kHz	Reduced (maintain regulation)
	Valid F_{SYNC} Input	F_{SYNC}	F_{SYNC}	F_{SYNC}	Reduced (maintain regulation)

7.3.8 Thermal Protection

The LMZM23601 monitors its junction temperature (T_J) and shuts off if the it gets too hot. The thermal shutdown threshold for the junction is typically 155°C. Both, high-side and low-side power MOSFETs are turned off until the junction temperature has decreased under the hysteresis level, typically 15°C below the shutdown temperature.

7.4 Device Functional Modes

7.4.1 Shutdown

The LMZM23601 device shuts down most internal circuitry and high-side and low-side power MOSFETs under any of the following conditions:

1. EN is low
2. VIN is below the falling UVLO threshold
3. Junction temperature exceeds T_{SD} threshold

The PGOOD flag remains operational with input voltage as low as 1.5 V.

7.4.2 FPWM Operation

If MODE/SYNC is above the $V_{MODE/SYNC}$ high threshold or a valid synchronizing is applied to MODE/SYNC, constant frequency operation is maintained across load. The ADJ option of the device folds back the frequency when V_{IN} exceeds 28 V typical so that the output voltage can be properly regulated. See 表 7-1 for all use cases and options. FPWM mode requires negative current be allowed in the inductor if the load is light. If a large negative load is present, operation is halted by a reverse current limit, I_{L-NEG}.

7.4.3 Auto PFM Mode Operation

If MODE/SYNC is below the $V_{MODE/SYNC}$ low threshold, reverse current in the inductor is not allowed. This feature is called diode emulation. While the load is heavy, the regulator uses PWM mode to control the output. If the load is light, the control logic transitions to PFM mode. The switching frequency is reduced, resulting in excellent energy savings while regulation is maintained. Because the frequency is reduced and switching pulses can come in groups, the output voltage ripple can increase slightly. Under this condition, the output ripple can be reduced by increasing the output capacitance.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LMZM23601 device is a step-down power module, typically used to efficiently convert a high DC input voltage to a lower DC output voltage with a maximum output current of up to 1 A. The following sections describe a simple design procedure for creating a DC/DC converter design with these modules.

8.2 Typical Applications

The LMZM23601 module requires very few external components for a complete DC/DC converter design. If the output voltage for the application is 3.3 V or 5 V, the fixed output voltage option of the LMZM23601 device can be used. In such cases, the design is as simple as adding only an input and an output capacitor. The adjustable output voltage version of the device allows the user to set the output voltage between 1.2 V and 15 V with the addition of two feedback resistors to the bill of materials.

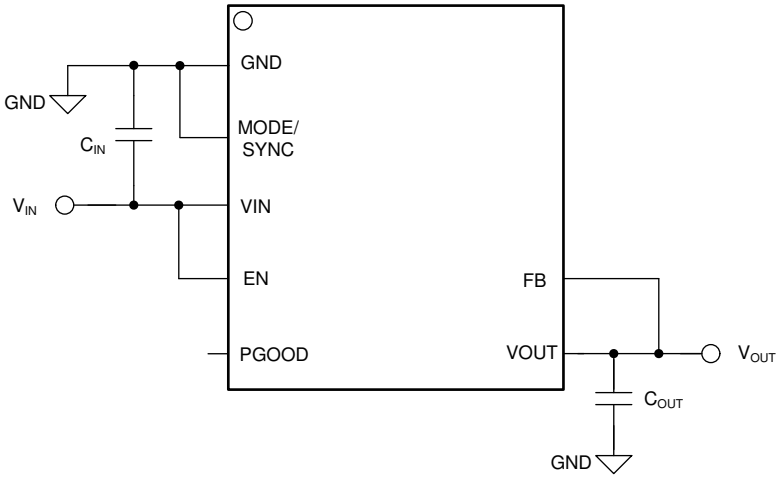


図 8-1. Fixed 5-V or 3.3-V Typical Application Circuit

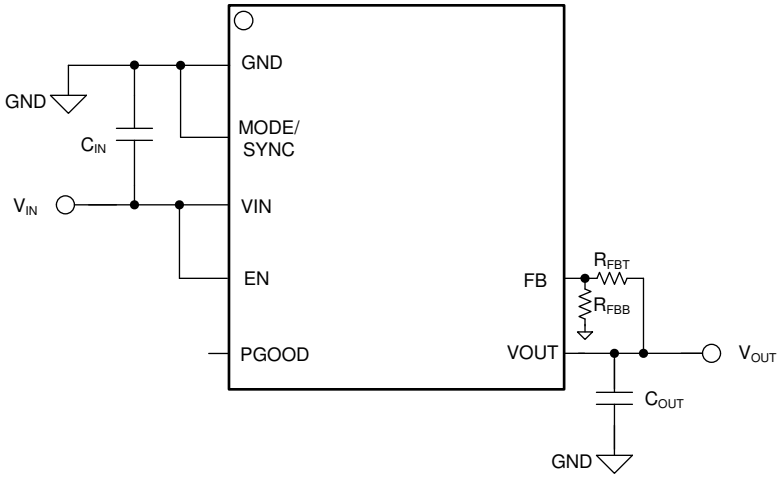


図 8-2. Adjustable 1.2-V to 15-V Output Typical Application Circuit

8.2.1 Design Requirements

8.2.1.1 Maximum Input Voltage for V_{OUT} < 2.5 V

For designs requiring V_{OUT} less than 2.5 V the maximum input voltage is limited by the switching frequency and the minimum on-time. See 図 8-3.

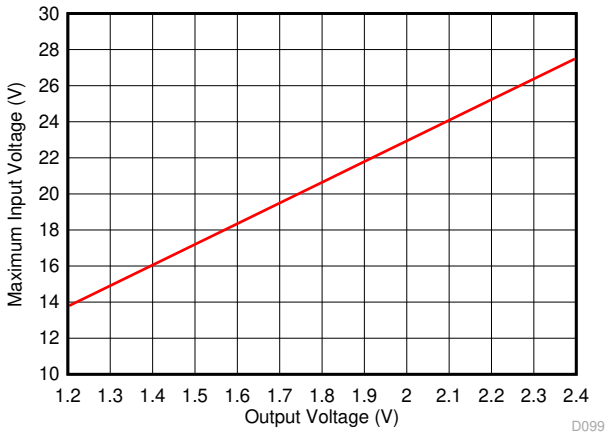


図 8-3. Maximum Input Voltage for V_{OUT} < 2.5 V

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE	COMMENT
Input voltage range	8 V to 36 V	This range covers a typical 12-V or 24-V industrial supply
Output voltage	5 V	Fixed or adjustable output voltage can be used
Output current range	No load to 1 A	

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZM23601device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.

2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Input Capacitor Selection

The input capacitor selection and placement on the board layout is very important for any buck converter design. This component provides the pulsing high di/dt current every switching cycle and reduces the input voltage ripple seen by the buck converter. Use a good-quality 10-µF, 1210 (3225) case size, X5R or X7R ceramic capacitor with sufficient voltage rating on the input of the device. Alternatively, in applications with strict size constraints and more stable input voltage it is possible to use a 10-µF, 1206 (3216) case size or a parallel combination of 2 × 4.7-µF, 0805 (2012), X5R or X7R capacitors. Ceramic capacitors have a DC bias dependence on their effective capacitance and can de-rate their value significantly when used at higher bias voltage. TI recommends ceramic capacitors with ≥ 50-V rating when using the device with a 24-V input supply. TI recommends ceramic capacitors with ≥ 25-V rating when using the device with a 12-V input supply.

Just like with any buck converter, place the input capacitor as close as possible and next to the LMZM23601. Connect the capacitor directly to the VIN (pin 3) and GND (pin 1) terminals of the device. This placement ensures that the area of the high di/dt current loop in the buck converter is kept to a minimum, resulting in the lowest possible inductance in the switching current path. The proper placement of the *input capacitor* in any buck converter helps to keep the *output noise* of the converter to a minimum. See 表 8-2 for several input capacitor choices.

表 8-2. Input Capacitor Selection

VALUE	VOLTAGE RATING	CASE SIZE	DIELECTRIC	QUANTITY	VENDOR	PART NUMBER
10 µF	50 V	1210 (3225)	X7R	1	TDK	C3225X7R1H106M250AC
10 µF	50 V	1210 (3225)	X7R	1	MuRata	GRJ32ER71H106KE11
10 µF	50 V	1206 (3216)	X5R	1	TDK	C3216X5R1H106K160AB
4.7 µF	50 V	0805 (2012)	X5R	2	TDK	C2012X5R1H475K125AB

For this design example a single 10-µF, 50-V 1210 X7R capacitor is used.

8.2.2.3 Output Capacitor Selection

TI recommends low-ESR ceramic capacitors for output capacitors. There is a requirement for minimum capacitance on the output of the LMZM23601 to ensure stable operation. The minimum output capacitance requirement depends on the output voltage setting. There is also a maximum capacitance value for stability and to limit the in-rush supply current. Excessive output capacitance can result in excessive current to be drawn from the input supply during startup. If the overcurrent condition is persistent during start-up, the over current protection of the LMZM23601 can activate and affect the normal output voltage ramp up. In extreme cases, the セクション 7.3.5 operation can be activated during start-up if the maximum output capacitance is exceeded.

Refer to 表 8-3 for the minimum, recommended, and maximum output capacitance values for each output voltage. For this example with a 5-V output a 22-µF capacitor can be used.

表 8-3. Output Capacitor

OUTPUT VOLTAGE	MINIMUM OUTPUT CAPACITANCE	RECOMMENDED OUTPUT CAPACITANCE	MAXIMUM OUTPUT CAPACITANCE
1.2 V	82 µF	100 µF	470 µF
1.8 V	68 µF	82 µF	470 µF
2.5 V	47 µF	68 µF	390 µF
3.3 V	22 µF	33 µF	330 µF
5 V	15 µF	22 µF	220 µF
12 V	10 µF	15 µF	200 µF
15 V	10 µF	15 µF	200 µF

8.2.2.4 Feedback Voltage Divider for Adjustable Output Voltage Versions

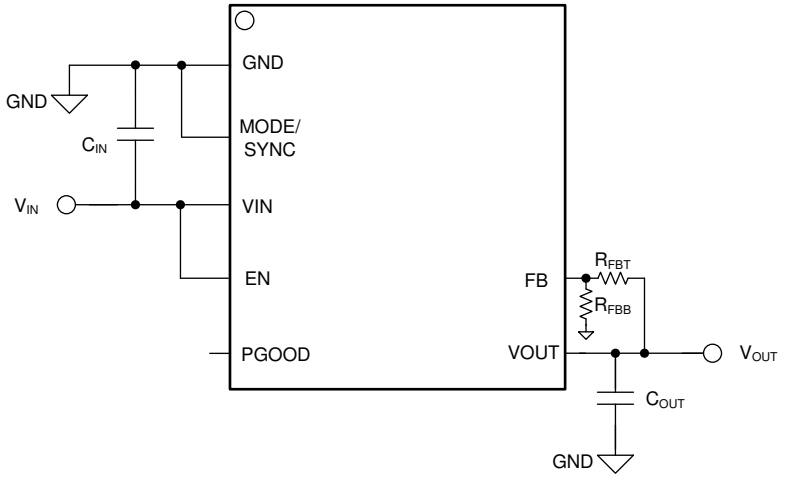


図 8-4. Adjustable 1.2-V to 15-V Output Typical Application Circuit

The adjustable version of the LMZM23601 regulates the output voltage such that the FB node voltage is equal to the internal V_{REF} voltage of 1 V. The output voltage is then set by a feedback voltage divider formed by two external resistors, R_{FBT} and R_{FBB}.

$$V_{OUT} = V_{REF} \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \quad (1)$$

The range of adjustable output voltage is 1.2 V to 15 V.

Choose a value for R_{FBT} in the kΩ range, and calculate the bottom resistor R_{FBB} using 式 2:

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (2)$$

For V_{OUT} < 3.0 V, TI recommends to allow 20 µA of static load current on the output. This can be achieved by limiting the maximum resistance of the feedback divider. For example, for V_{OUT} = 2 V, the maximum total feedback resistance (R_{FBB}+ R_{FBT}) must be 100 kΩ or less.

For this design example the output voltage is set to 5 V. The fixed 5-V output voltage option of the LMZM23601 can be used without any feedback resistors. If the adjustable output option is used for this design condition, the top feedback resistor R_{FBT} can be set to 102 kΩ. The R_{FBB} value results in 25.5 kΩ.

8.2.2.5 R_{PU} - PGOOD Pullup Resistor

The PGOOD terminal of the LMZM23601 is an open-drain output. If the application requires a power-good flag, use a 100-kΩ pullup resistor from the PGOOD terminal to an external voltage rail. If a power-good function is not necessary, the PGOOD terminal can be left floating.

8.2.2.6 V_{IN} Divider and Enable

If the application requires custom input UVLO level higher than the internal UVLO, a voltage divider can be connected from V_{IN} to the EN terminal to set the turnon threshold.

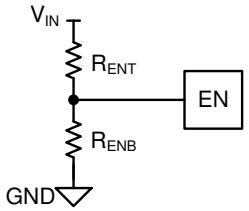


図 8-5. Enable Divider to Set External UVLO Threshold

Choose the top resistor R_{ENB} between 10 kΩ and 50 kΩ and calculate the R_{ENT} according to 式 3.

$$R_{ENT} = \left(\frac{V_{START}}{V_{EN}} - 1 \right) \times R_{ENB}$$

$$V_{STOP} = V_{START} \times \left(1 - \frac{V_{EN\_HYST}}{V_{EN}} \right) \quad (3)$$

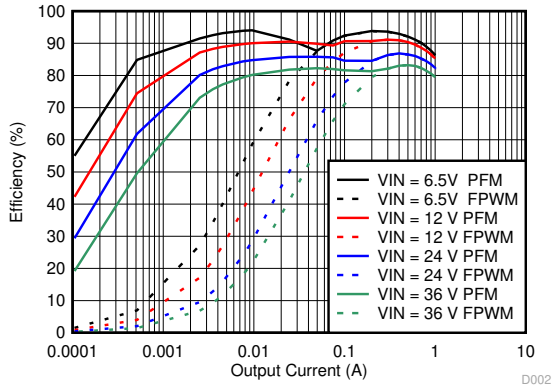
where

- V_{START} is the rising input voltage level at which switching starts. Choose this value based on the application requirements.
- V_{STOP} is the input voltage at which switching stops
- V_{EN} is the rising threshold on EN; see *Electrical Characteristics*
- V_{EN_HYST} is the hysteresis on the EN threshold; see *Electrical Characteristics*

8.2.3 Application Curves

Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, T_A = 25°C.

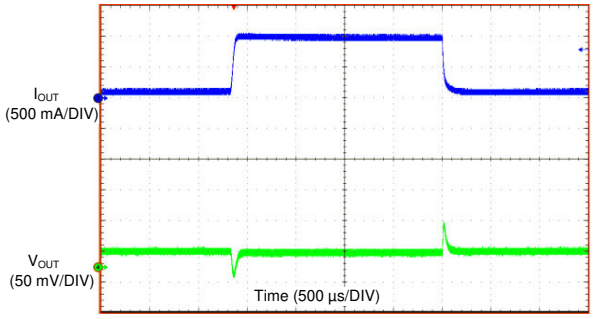
8.2.3.1 V_{OUT} = 5 V



MODE = Low for Auto PFM Mode
MODE = High for FPWM Mode

5-V Adjustable Output

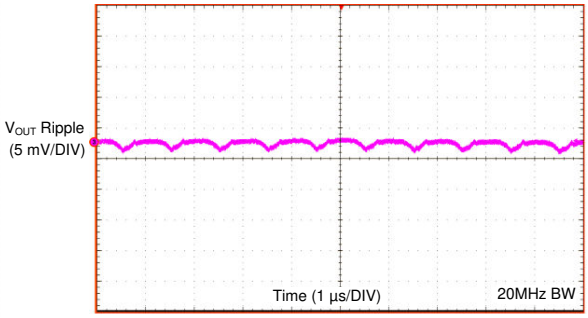
図 8-6. Efficiency



5-V Adjustable Output
10% to 100% Load Step

MODE = High

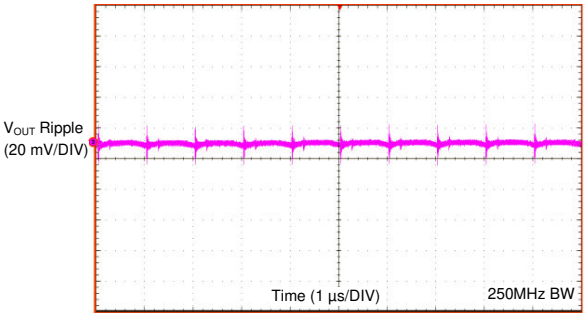
図 8-7. Load Transient



5-V Adjustable Output

I_{OUT} = 1 A

図 8-8. Output Ripple 20 MHz BW



5-V Adjustable Output

I_{OUT} = 1 A

図 8-9. Output Ripple 250-MHz BW

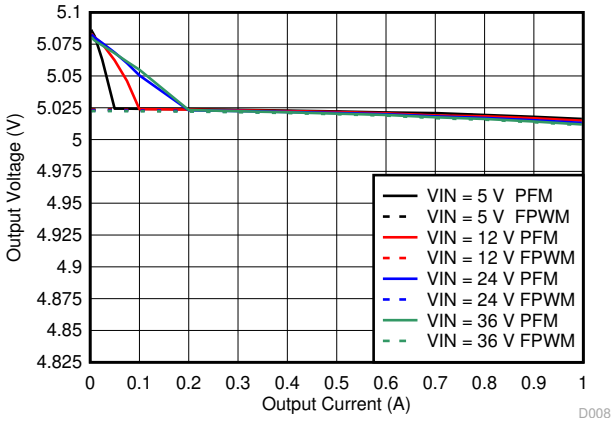


図 8-10. Line and Load Regulation

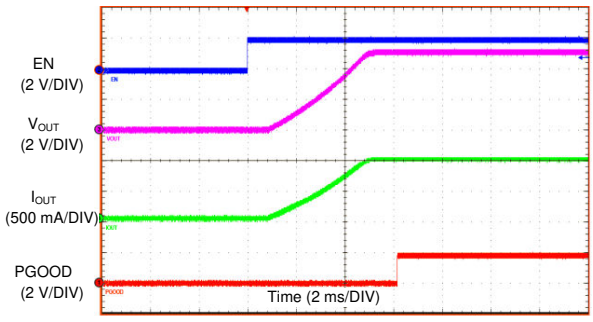
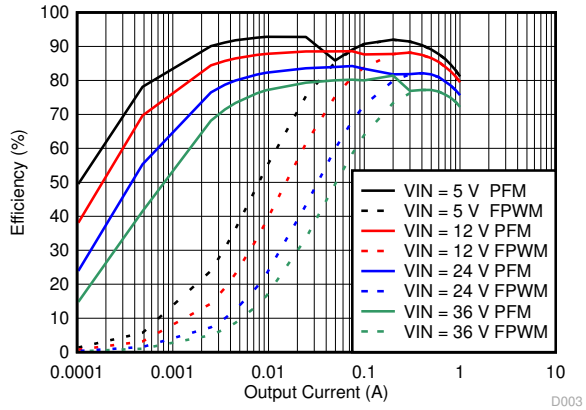


図 8-11. Start-up With 24-V Input

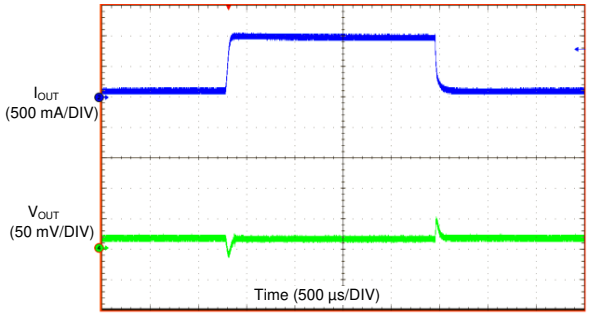
8.2.3.2 V_{OUT} = 3.3 V



MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode

3.3-V Adjustable Output

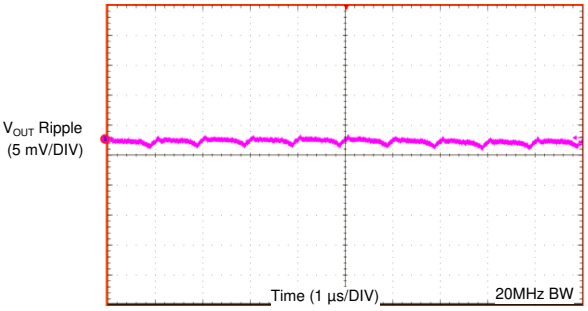
図 8-12. Efficiency



3.3-V Adjustable Output
10% to 100% Load Step

MODE = High

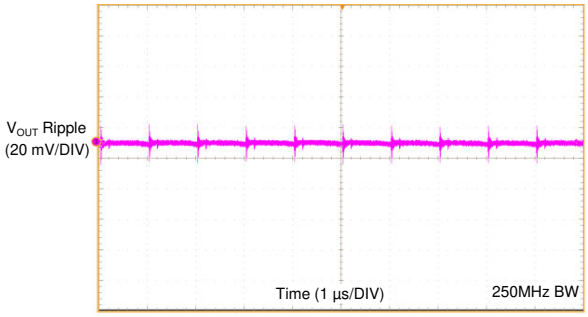
図 8-13. Load Transient



3.3-V Adjustable Output

I_{OUT} = 1 A

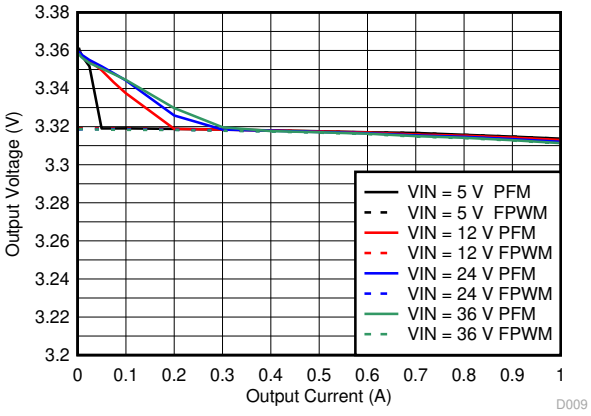
図 8-14. Output Ripple 20-MHz BW



3.3-V Adjustable Output

I_{OUT} = 1 A

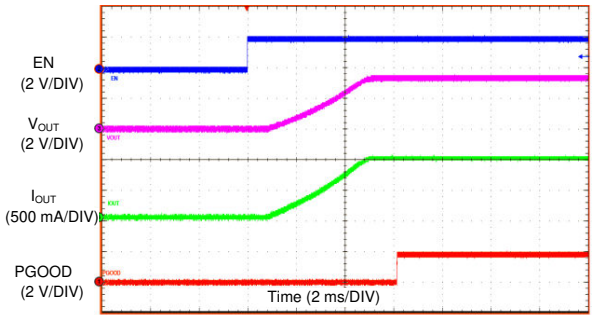
図 8-15. Output Ripple 250 MHz BW



MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode

3.3-V Adjustable Output

図 8-16. Line and Load Regulation

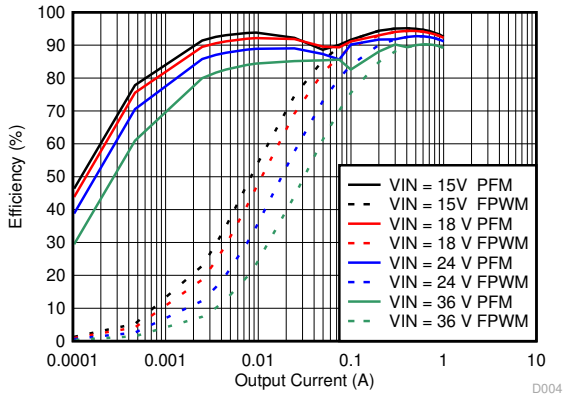


3.3-V Adjustable Output

Toggle Enable

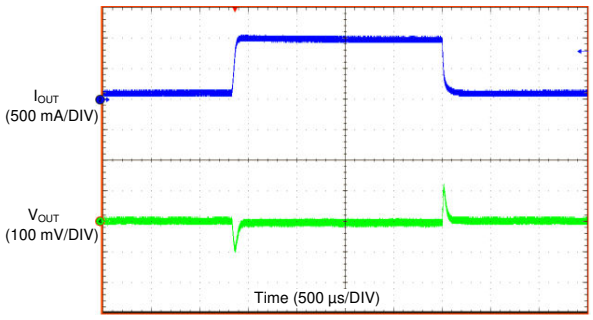
図 8-17. Start-up With 24-V Input

8.2.3.3 V_{OUT} = 12 V



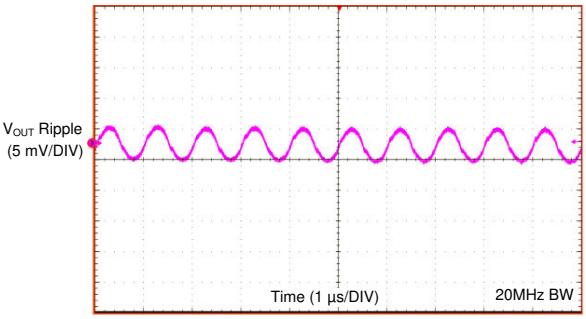
MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode
12-V Adjustable Output

図 8-18. Efficiency



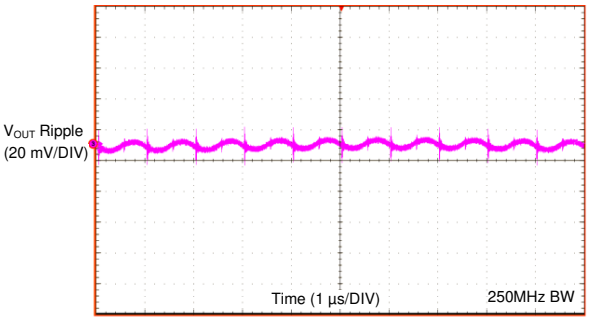
12-V Adjustable Output
10% to 100% Load Step
MODE = High

図 8-19. Load Transient



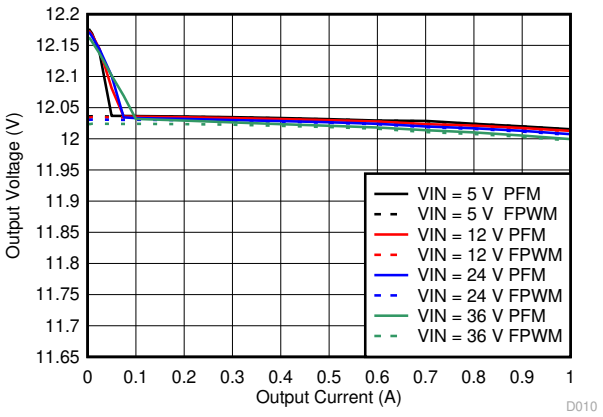
12-V Adjustable Output
I_{OUT} = 1 A

図 8-20. Output Ripple 20-MHz BW



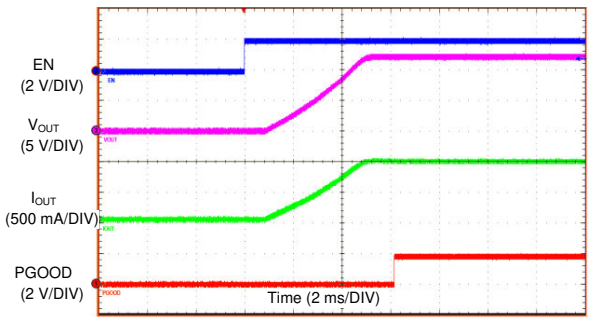
12-V Adjustable Output
I_{OUT} = 1 A

図 8-21. Output Ripple 250-MHz BW



MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode
12-V Adjustable Output

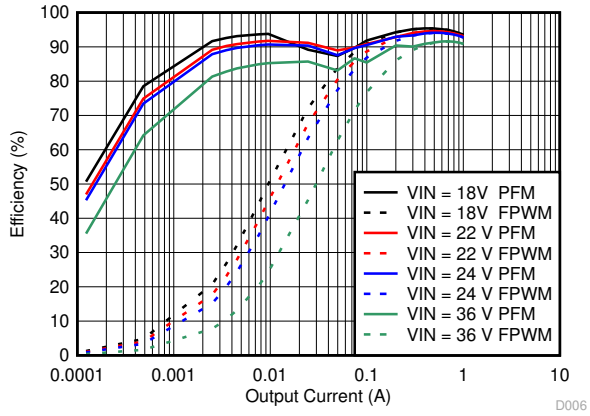
図 8-22. Line and Load Regulation



12-V Adjustable Output
Toggle Enable

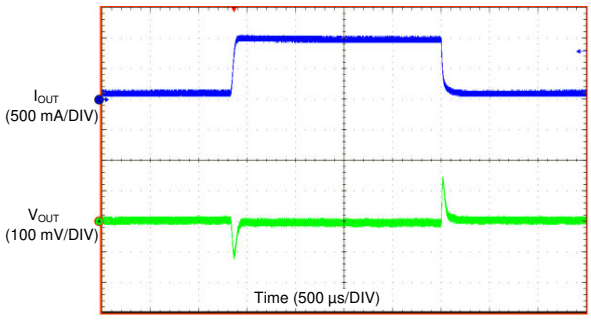
図 8-23. Start-up With 24-V Input

8.2.3.4 V_{OUT} = 15 V



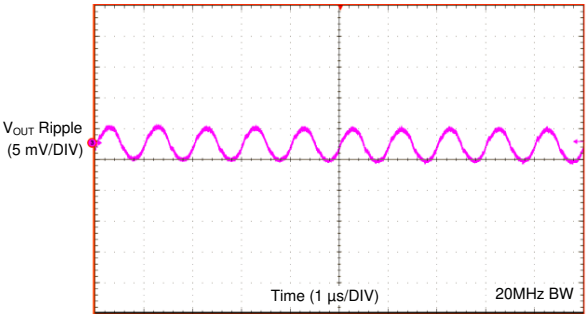
MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode
15-V Adjustable Output

図 8-24. Efficiency



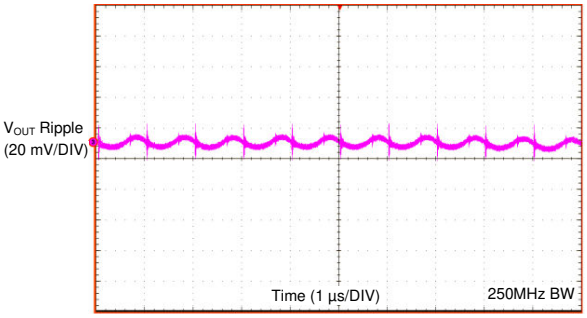
15-V Adjustable Output
10% to 100% Load Step
MODE = High

図 8-25. Load Transient



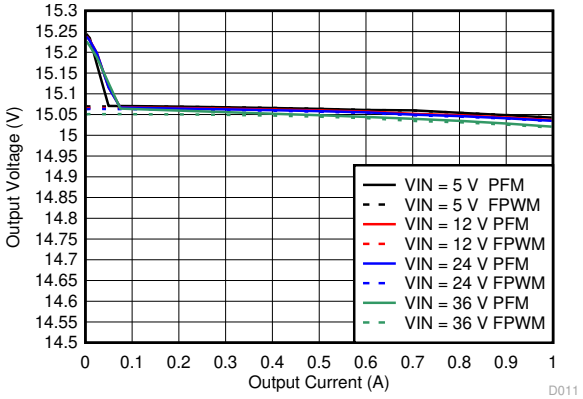
15-V Adjustable Output
I_{OUT} = 1 A

図 8-26. Output Ripple 20-MHz BW



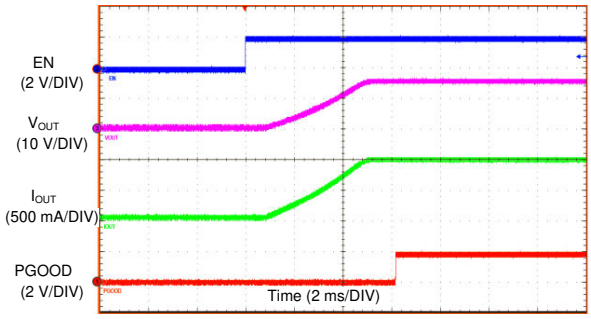
15-V Adjustable Output
I_{OUT} = 1 A

図 8-27. Output Ripple 250-MHz BW



MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode
15-V Adjustable Output

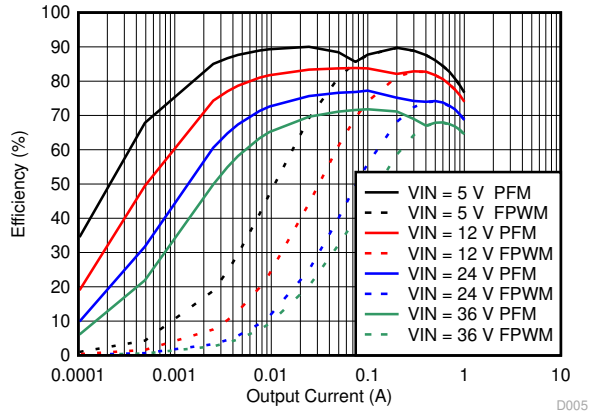
図 8-28. Line and Load Regulation



15-V Adjustable Output
Toggle Enable

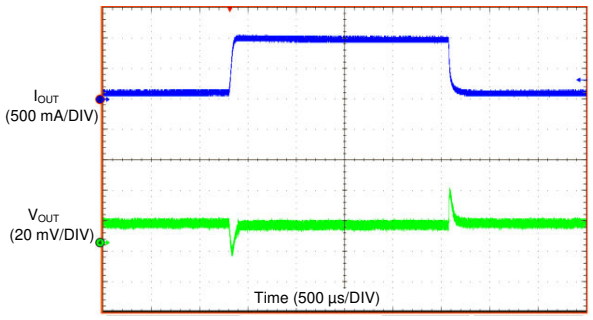
図 8-29. Start-up with 24-V Input

8.2.3.5 V_{OUT} = 2.5 V



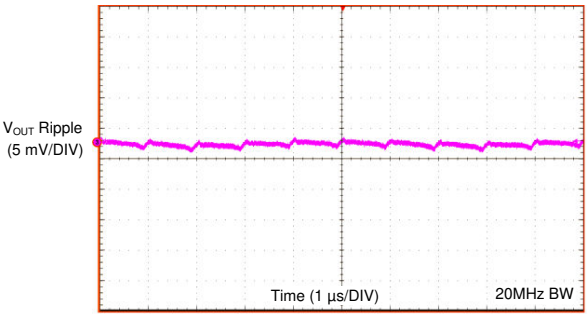
MODE = High for FPWM Mode
MODE = Low for Auto PFM Mode
2.5-V Adjustable Output

図 8-30. Efficiency



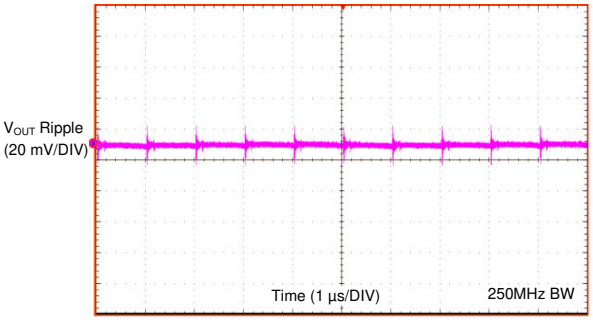
2.5-V Adjustable Output
10% to 100% Load Step
MODE = High

図 8-31. Load Transient



2.5-V Adjustable Output
I_{OUT} = 1 A

図 8-32. Output Ripple 20-MHz BW



2.5-V Adjustable Output
I_{OUT} = 1 A

図 8-33. Output Ripple 250-MHz BW

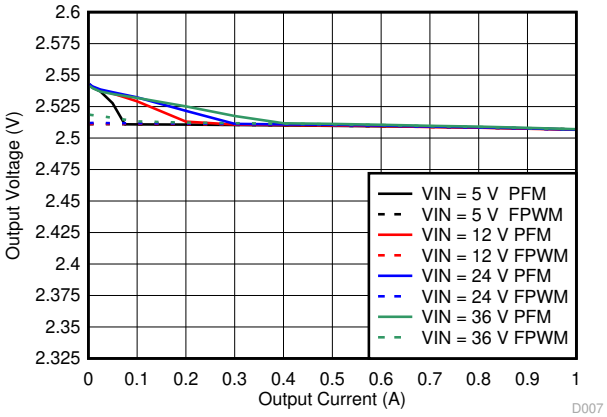


図 8-34. Line and Load Regulation

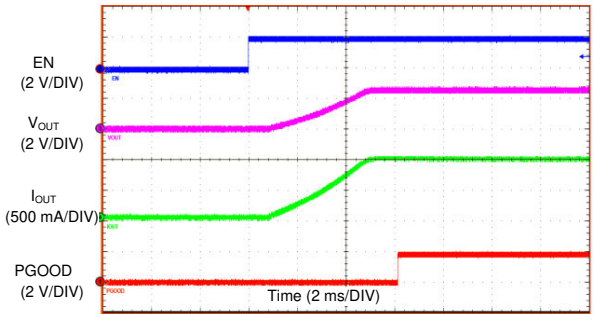
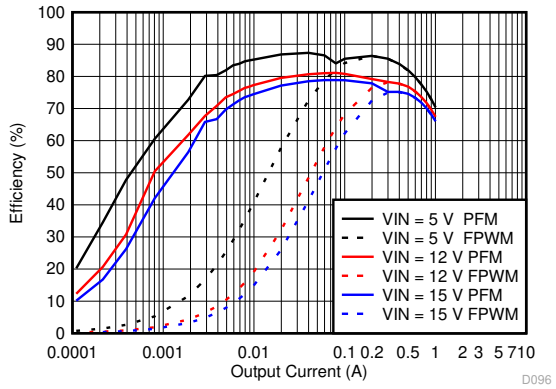


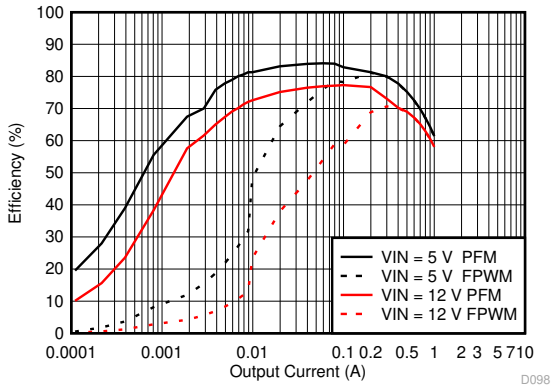
図 8-35. Start-up with 24-V Input

8.2.3.6 V_{OUT} = 1.2 V and V_{OUT} = 1.8 V



MODE = Low for Auto PFM Mode 1.8-V Adjustable Output
MODE = High for FPWM Mode

図 8-36. Efficiency for V_{OUT} = 1.8 V



MODE = Low for Auto PFM Mode 1.2-V Adjustable Output
MODE = High for FPWM Mode

図 8-37. Efficiency for V_{OUT} = 1.2 V

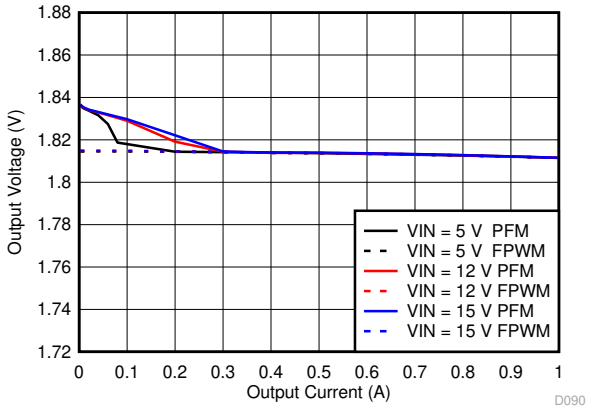


図 8-38. Line and Load Regulation for V_{OUT} = 1.8 V

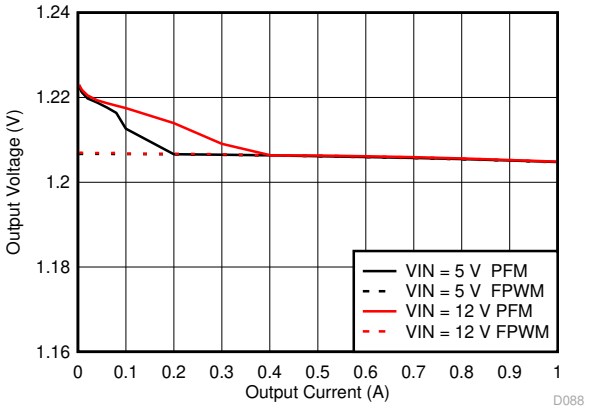
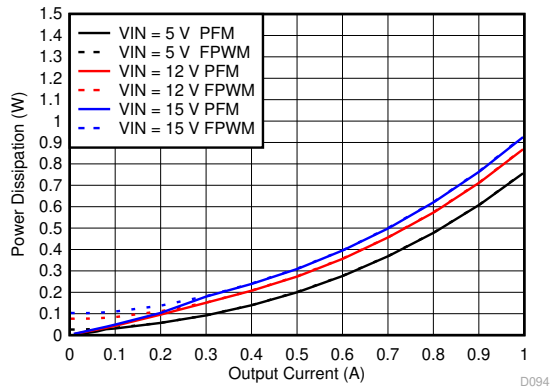
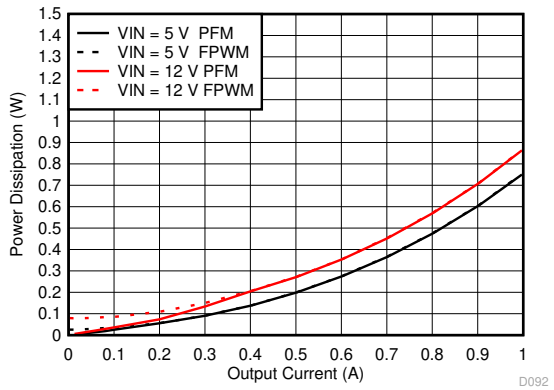


図 8-39. Line and Load Regulation for V_{OUT} = 1.2 V



MODE = Low for Auto PFM Mode 1.8-V Adjustable Output
MODE = High for FPWM Mode

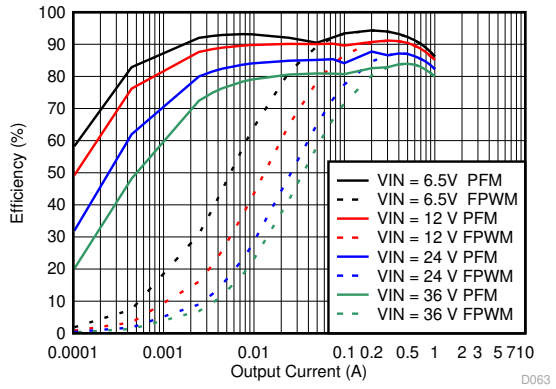
図 8-40. Power Dissipation for V_{OUT} = 1.8 V



MODE = Low for Auto PFM Mode 1.2-V Adjustable Output
MODE = High for FPWM Mode

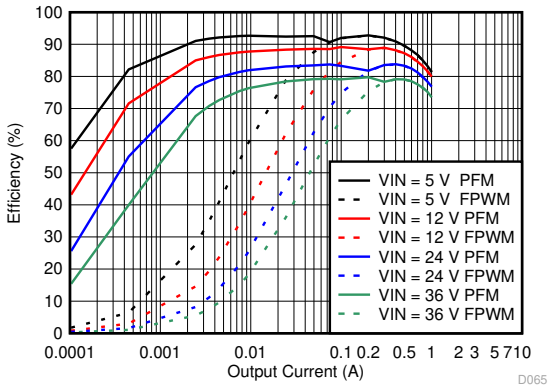
図 8-41. Power Dissipation for V_{OUT} = 1.2 V

8.2.3.7 V_{OUT} = 5 V and 3.3 V Fixed Output Options



MODE = Low for Auto PFM Mode 5-V Fixed Output
MODE = High for FPWM Mode

図 8-42. Efficiency for V_{OUT} = 5 V



MODE = Low for Auto PFM Mode 3.3-V Fixed Output
MODE = High for FPWM Mode

図 8-43. Efficiency for V_{OUT} = 3.3 V

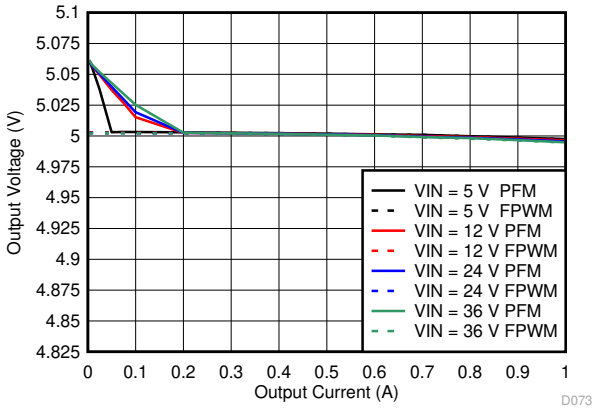


図 8-44. Line and Load Regulation for V_{OUT} = 5 V

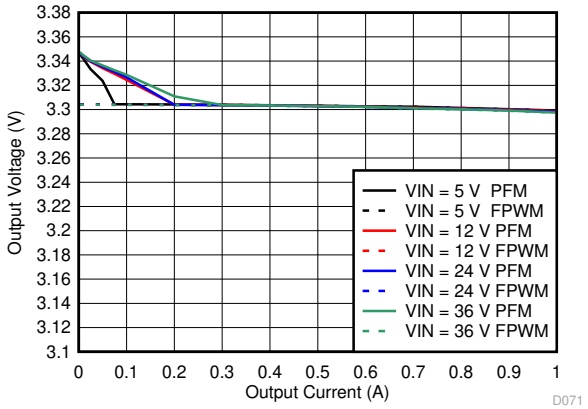
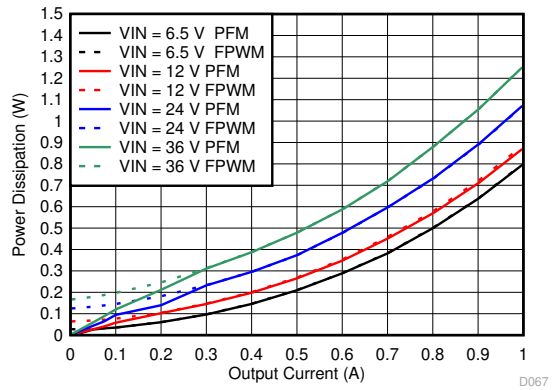
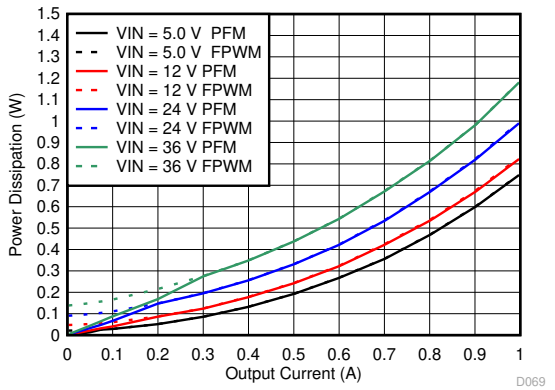


図 8-45. Line and Load Regulation for V_{OUT} = 3.3 V



MODE = Low for Auto PFM Mode 5-V Fixed Output
MODE = High for FPWM Mode

図 8-46. Power Dissipation for V_{OUT} = 5 V



MODE = Low for Auto PFM Mode 3.3-V Fixed Output
MODE = High for FPWM Mode

図 8-47. Power Dissipation for V_{OUT} = 3.3 V

8.3 Best Design Practices

- Do not: Exceed the absolute maximum ratings of the device.
- Do not: Exceed the ESD ratings of the device.
- Do not: Exceed the recommended operating conditions.
- Do not: Allow the EN or MODE/SYNC terminals to float.
- Do not: Allow the output voltage to exceed the input voltage, nor go below ground.
- Do: Follow all of the guidelines and suggestions found in this data sheet, before committing your design to production.
- Do: Review your designs with TI Application Engineers on the E2E forum.

8.4 Power Supply Recommendations

8.4.1 Supply Voltage Range

The voltage of the input supply must not exceed the absolute maximum ratings and the recommended operating conditions of the LMZM23601.

8.4.2 Supply Current Capability

The input supply must be able to supply the required input current to the LMZM23601 converter. The required input current depends on the application's minimum input voltage, the required maximum output current, the output voltage, and the converter efficiency η for this condition.

$$I_{IN} \geq \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMIN} \times \eta} \tag{4}$$

As an example, assuming that the adjustable output voltage version of the LMZM23601 is used for a 5-V, 1-A output converter design with 12-V minimum input voltage. The conversion efficiency for this condition is about 85%. The required input current from the supply is 0.49 A, so TI recommends an input power supply with ≥ 0.5 A current capability.

8.4.3 Supply Input Connections

Long input connection cables can cause issues with the normal operation of any buck converter. Some of the issues can be a voltage drop in the input voltage or stability probes because of the added series input inductance.

8.4.3.1 Voltage Drops

Using long input wires to connect the supply to the input of any converter adds impedance in series with the input supply. This impedance can cause a voltage drop at the VIN pin of the converter when the output of the converter is loaded. If the input voltage is near the minimum input operating voltage for the design, this added voltage drop can cause the converter to drop out or reset. If long wires are used during testing, TI recommends adding some bulk (for example, electrolytic) capacitance at the input of the converter.

8.4.3.2 Stability

The added inductance of long input cables together with the ceramic (and low ESR) input capacitor can result in an underdamped RLC network at the input of the buck converter. This circuit can cause instability, or overvoltage transients at the VIN pin each time the input supply is cycled on and off. If long wires are used, TI recommends adding some electrolytic bulk capacitance in parallel with the ceramic input capacitor. The ESR of the bulk capacitor improves the damping. Use an electrolytic capacitor with a capacitance at least four times larger than the ceramic input capacitance.

$$C_{BULK} \geq 4 \times C_{CER} \tag{5}$$

The required ESR from the bulk capacitor depends on the cable inductance.

$$ESR_{BULK} \geq \sqrt{\frac{L_{CABLE}}{C_{CER}}} \quad (6)$$

For example, two cables (one for VIN and one for GND), each 1 meter (approximately 3 feet) long with approximately 1-mm diameter (18 AWG), placed 1 cm (approximately 0.4 inch) apart forms a rectangular loop resulting in about 1.2 µH of inductance. The inductance in this example can be decreased to almost half if the input wires are twisted. Based on a 10-µF ceramic input capacitor, the recommended parallel C_{BULK} is ≥ 40 µF. Using a 47-µF capacitor is sufficient. Based on about 1.2 µH of inductance and 10 µF of ceramic input capacitance, the recommended ESR of the bulk capacitor is 0.35 Ω or larger. See *TI User Guide, Simple Success with Conducted EMI for DC/DC Converters* for more details on input filter design.

8.5 Layout

8.5.1 Layout Guidelines

Good board layout is essential for the proper operation of any switching regulator. A poor layout can ruin an otherwise perfect schematic design. The good news is that it is relatively easy to achieve an optimized layout when using a module because some of the critical nodes for the board layout are internal to the device. To have a good layout with this module, the designer must follow these main objectives:

1. *Minimize the inductance in the switching current path of the converter*. The switching current path in the buck converter is formed by the input capacitor and the power switches (for example, MOSFETs). A **common mistake** in many buck converter layouts is placing the input capacitor far from the IC. This introduces inductance in the switching current path, which leads to high frequency ringing on the switching node, which results in high frequency noise coupled all the way to the output voltage. The **input capacitor** placement affects the amount of **noise on the output** in a buck converter. Place the input capacitor as close as possible, right next to the LMZM23601 ensures that the switching current path area is kept to a minimum. This results in the lowest possible inductance in the path of high di/dt current.
2. *Protect any sensitive nodes in the converter design.* The feedback node is usually a sensitive area of the converter and needs to be away from any noise sources. The fixed 5-V and 3.3-V output voltage versions of the LMZM23601 have the feedback resistors internal to the device, and the sensitive node is inside the module. However, if the adjustable option is used, then two feedback resistors are required to set the output voltage. A **common mistake** in many layouts is placing the divider close to the load, far from the device, and then using a long feedback trace back to the regulator. A long feedback trace can potentially pick up noise from other nearby circuits. TI recommends placing the feedback divider as close as possible to the LMZM23601 device so that the feedback node is as small as possible.
3. *Provide enough copper for heat dissipation.* The board copper provides a thermal resistance path for the heat to flow out of the package and dissipate into the environment. Place a *dog-bone* shape of ground (GND) copper under the module for proper heat sinking. Also, place thermal vias to provide a heat path to the other board layers. TI recommends an unbroken GND plane or GND area of copper on the top and bottom layers.

8.5.1.1 Thermal Design

Thermal design is an important aspect of any power regulator design. Every supply dissipates some power, and providing sufficient copper area for proper heat dissipation is important. The package thermal resistance curves vs PCB copper area along with the power dissipation curves in *セクション 6.7* can be used to estimate the necessary copper area for the design. Consider 式 7 and 図 8-48.

$$R_\theta \leq \frac{125\,℃ - T_{A\_MAX}}{P_D} \quad (7)$$

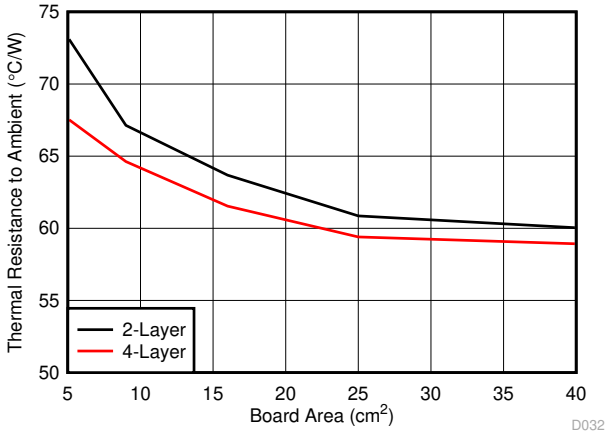


図 8-48. Package Thermal Resistance vs Board Copper Area

As an example, consider a typical application of 24-V input 5-V output with 0.8 A of output current and estimate the required heat-sinking area. For this example consider a maximum ambient temperature T_{A_MAX} of 75°C and no air flow or additional heat sinking besides the PCB layers. Calculate the maximum allowed package thermal resistance for this design specification.

From *セクション 6.7*, it can be seen that the power dissipation for 24-V input, 5-V output, and 0.8A load is 0.75 W. Based on 式 7, for this power dissipation level and 75°C maximum ambient temperature, the maximum package thermal resistance must be less than 66.7°C/W. To achieve this thermal resistance with a 2-layer board, the approximate area of the board copper must be at least 9 cm^2.

8.5.2 Layout Examples

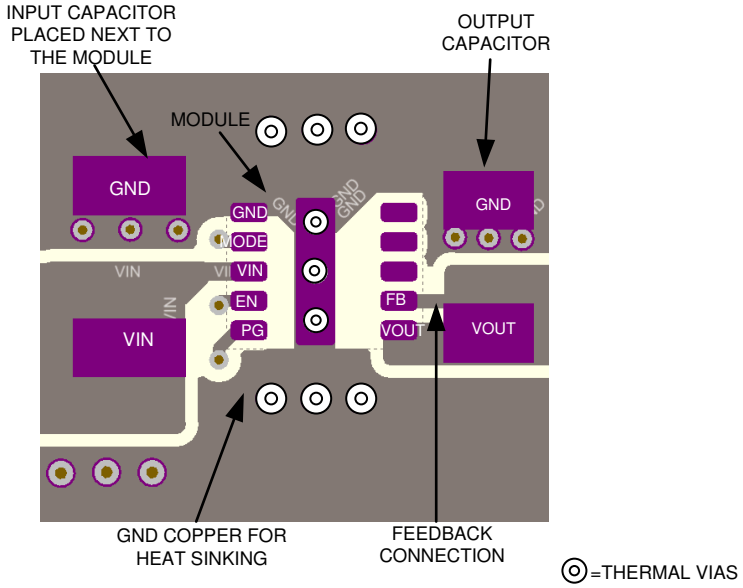


図 8-49. Layout Example With Fixed Output Version

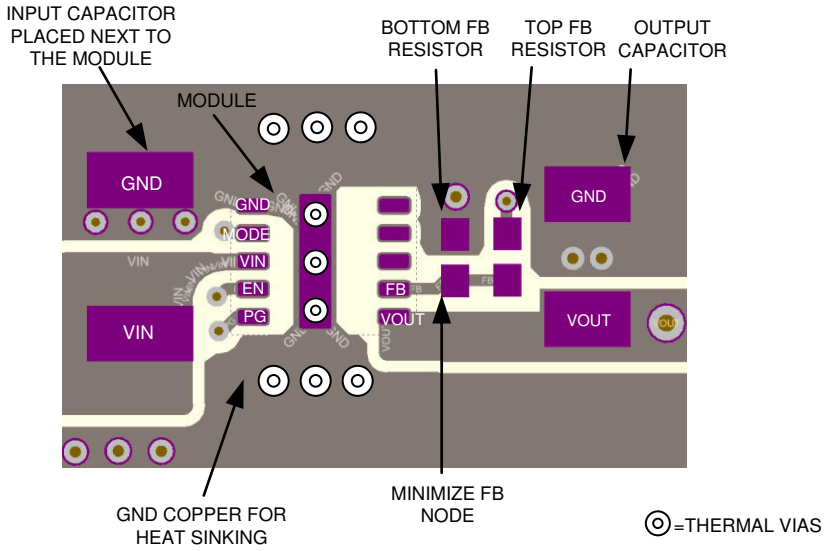


図 8-50. Layout Example With Adjustable Output Version

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZM23601 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation request the following:

Texas Instruments, *Inverting Application for the LMZM23601 and LMZM23600* application report

Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report

Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

Texas Instruments, *AN-1229 Simple Switcher PCB Layout Guidelines* application report

Texas Instruments, *Using New Thermal Metrics* application report

Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report

Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report

Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application report

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

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WEBENCH® is a registered trademark of Texas Instruments.
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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

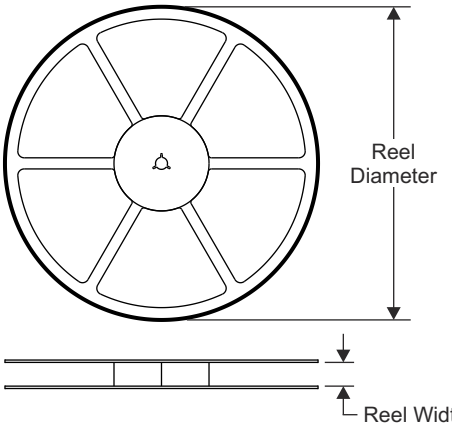
テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

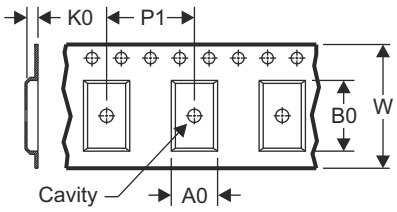
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

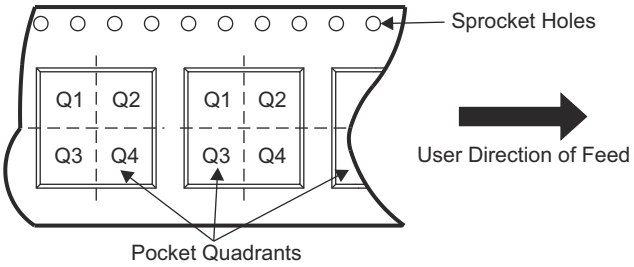


TAPE DIMENSIONS



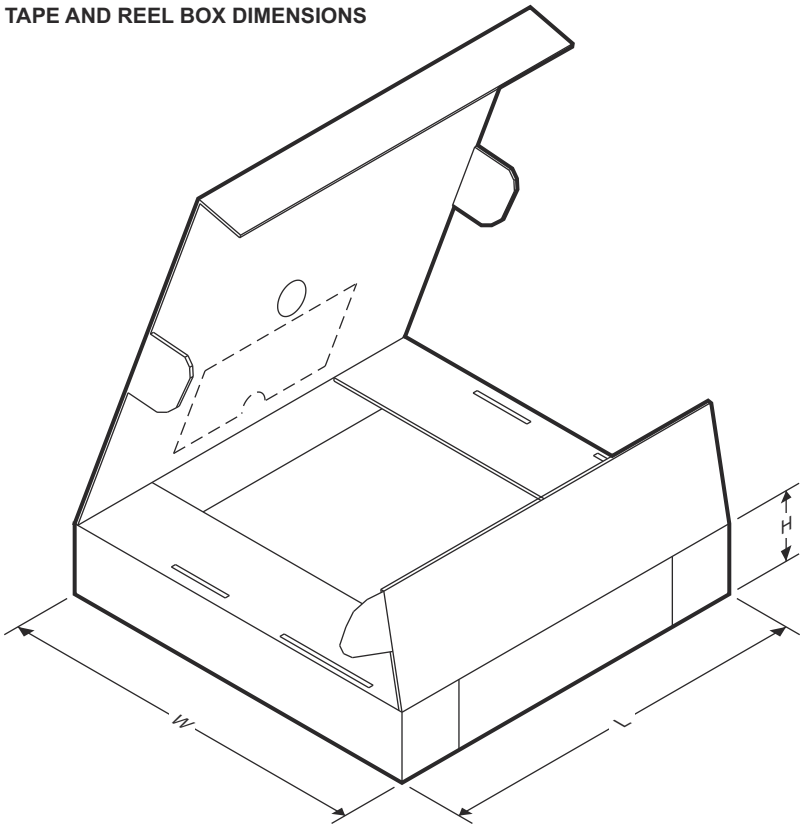
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZM23601SILR	uSiP	SIL	10	3000	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2
LMZM23601SILT	uSiP	SIL	10	250	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2
LMZM23601V3SILR	uSiP	SIL	10	3000	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2
LMZM23601V3SILT	uSiP	SIL	10	250	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2
LMZM23601V5SILR	uSiP	SIL	10	3000	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2
LMZM23601V5SILT	uSiP	SIL	10	250	330.0	12.4	3.27	4.07	1.78	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



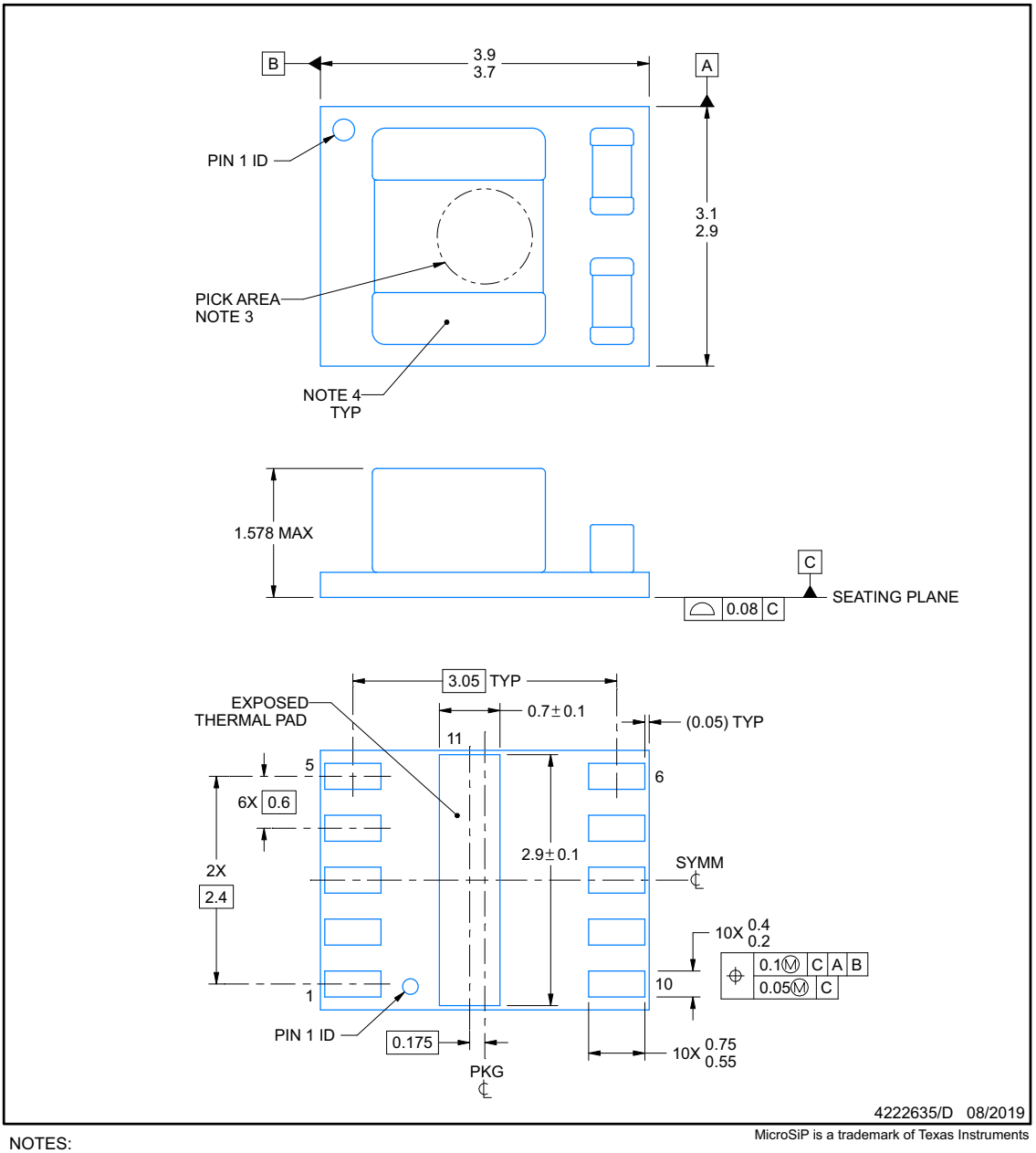
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZM23601SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
LMZM23601SILT	uSiP	SIL	10	250	383.0	353.0	58.0
LMZM23601V3SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
LMZM23601V3SILT	uSiP	SIL	10	250	383.0	353.0	58.0
LMZM23601V5SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
LMZM23601V5SILT	uSiP	SIL	10	250	383.0	353.0	58.0

PACKAGE OUTLINE

SIL0010A

uSiP™ - 1.578 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

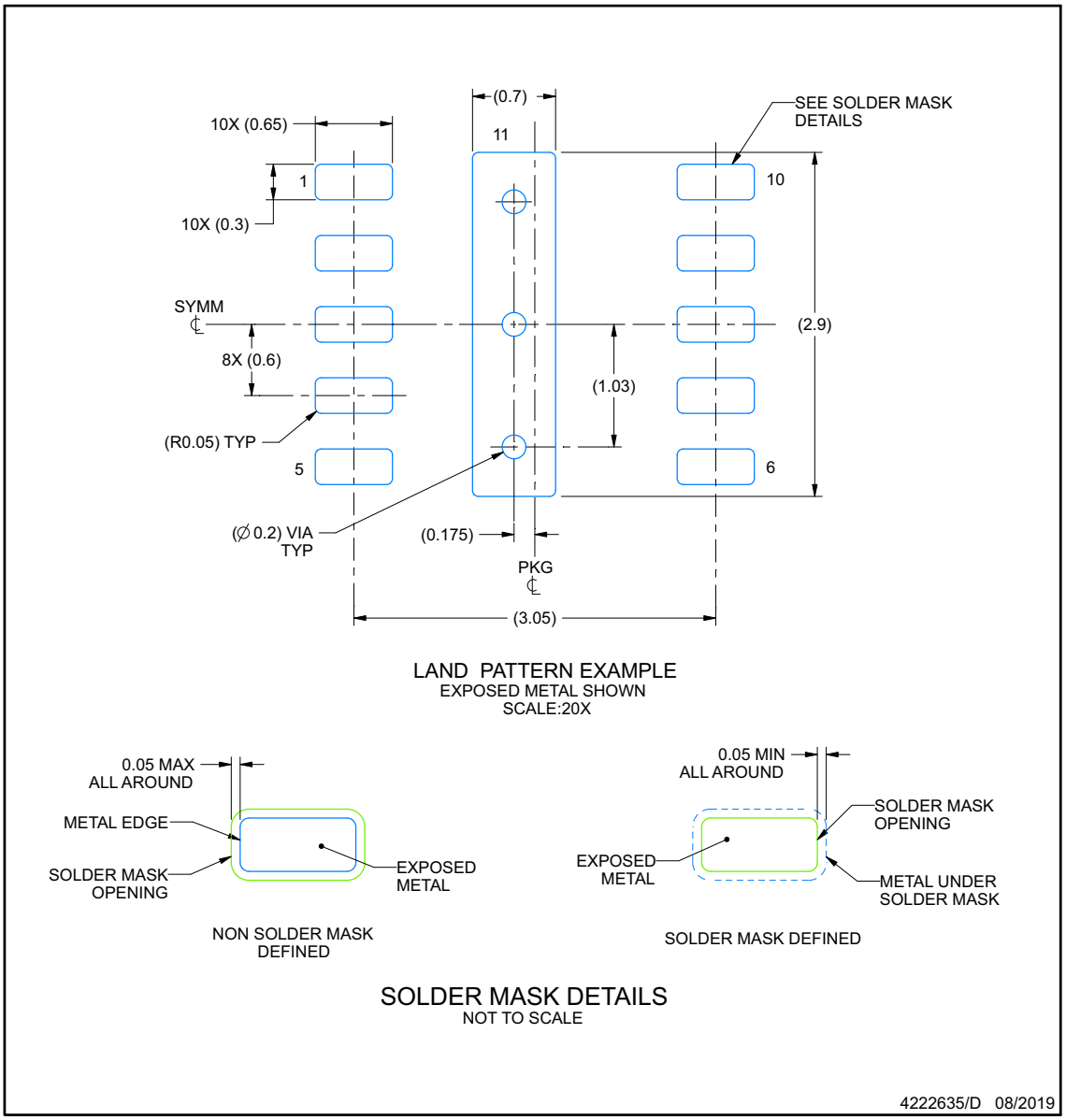
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.1 mm or smaller recommended.
4. Location, size and quantity of components are for reference only and could vary.
5. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

SIL0010A

uSiP™ - 1.578 mm max height

MICRO SYSTEM IN PACKAGE



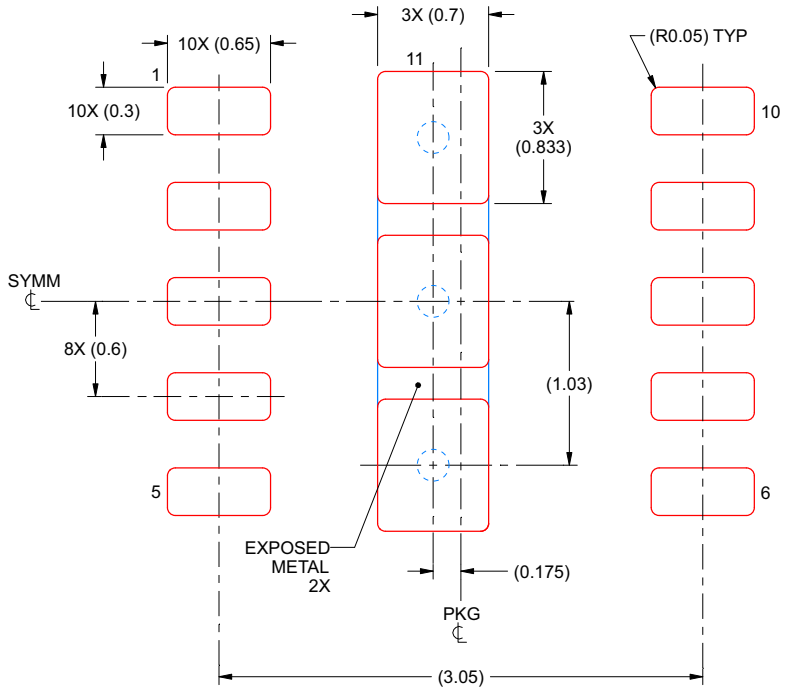
NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

SIL0010A — **uSiP™ - 1.578 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222635/D 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZM23601SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4B A
LMZM23601SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4B A
LMZM23601SILR.B	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMZM23601SILT	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4B A
LMZM23601SILT.A	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4B A
LMZM23601SILT.B	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4B A
LMZM23601V3SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4I A
LMZM23601V3SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4I A
LMZM23601V3SILR.B	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMZM23601V3SILT	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4I A
LMZM23601V3SILT.A	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4I A
LMZM23601V3SILT.B	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4I A
LMZM23601V5SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4H A
LMZM23601V5SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4H A
LMZM23601V5SILR.B	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMZM23601V5SILT	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4H A
LMZM23601V5SILT.A	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4H A
LMZM23601V5SILT.B	Active	Production	uSiP (SIL) | 10	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	4H A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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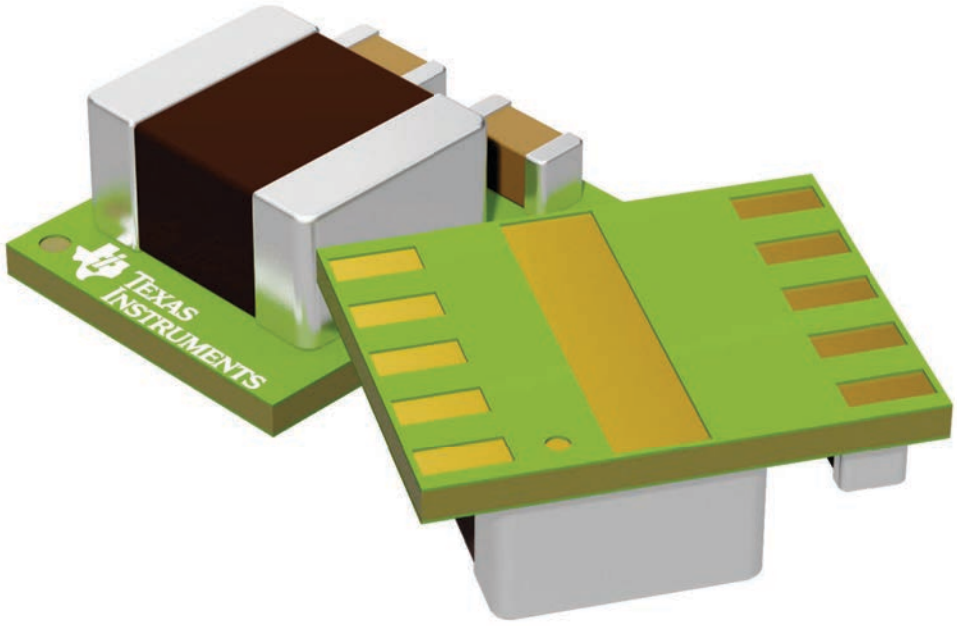
GENERIC PACKAGE VIEW

SIL 10

uSIP™

MICRO SYSTEM IN PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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