LMX1204 低ノイズ、高周波 JESD バッファ / 逓倍器 / 分周器

1 特長

- 出力周波数:300MHz～12.8GHz
- 超低ノイズ
  - ノイズ フロア (6GHz 出力):-161dBc/Hz
  - 1/f ノイズ (6GHz 出力、10kHz オフセット):-154dBc/Hz
  - ジッタ (12kHz～20MHz):5fS
  - 付加ジッタ (DC～f_{CLK}):<30fs
- 対応する SYSREF 出力を備えた 4 つの高周波クロック
  - ÷1 (バッファ モード)、÷2、3、4、5、6、7、8 をサポートする共有デバイダ
  - ×1 (フィルタ モード)、×2、×3、×4 をサポートする共有 PLL ベースのマルチプライヤ
- LOGICLK 出力と対応する SYSREF 出力
  - 個別の分周バンク上
  - ÷1、2、4 プリデバイダ
  - ÷1 (バイパス)、2、…、1023 ポストデバイダ
- 8 つのプログラム可能な出力電力レベル
- 同期された SYSREF クロック出力
  - 508 遅延ステップの調整は、12.8GHz でそれぞれ 2.5ps 未満
  - ジェネレータモードとリピータモード
  - SYSREFREQ ピンのウィンドウ処理機能によりタイミングを最適化します
- すべてのデバイダおよび複数のデバイスに対する SYNC 機能
- 2.5V の動作電圧
- 動作温度:-40℃～85℃

2 アプリケーション

- 試験 & 測定:
  - オシロスコープ
  - ワイヤレス機器テスター
  - 広帯域デジタイザ
- 航空宇宙 & 防衛:
  - レーダー
  - 電子戦
  - シーカー フロント エンド
  - 軍需品
  - フェーズド アレイ アンテナ / ビーム フォーミング
- 汎用:
  - データ コンバータのクロック供給
  - クロック バッファの分配 / 分周

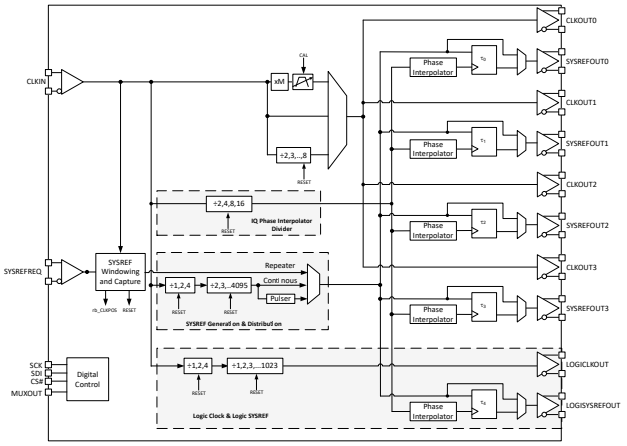
3 概要

このデバイスは高い周波数に対応し、ジッタが非常に小さいため、信号対雑音比の劣化なく、高精度クロック、高周波データ コンバータを容易に実現できます。4 つの高周波クロック出力のそれぞれと、より大きな分周器範囲を持つ追加の LOGICLK 出力は、SYSREF 出力クロック信号と対になります。JESD インターフェイスの SYSREF 信号は、内部で生成するか、入力として渡されて、デバイス クロックに再度クロックされます。データ コンバータのクロック供給アプリケーションでは、クロックのジッタをデータ コンバータのアパーチャ ジッタよりも小さくすることが重要です。4 つより多いデータ コンバータにクロックを供給する必要があるアプリケーションでは、複数のデバイスを使用して、必要なすべての高周波クロックと SYSREF 信号を分配する、さまざまなカスケード接続アーキテクチャを開発できます。このデバイスはジッタが小さくノイズ フロアが低いため、超低ノイズのリファレンス クロック ソースと組み合わせると、特にサンプリングが 3GHz を超える場合に、データ コンバータのクロック供給用の模範的な選択肢になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMX1204	RHA (VQFN、40)	6.00mm × 6.00mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ブロック図

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4 Pin Configuration and Functions

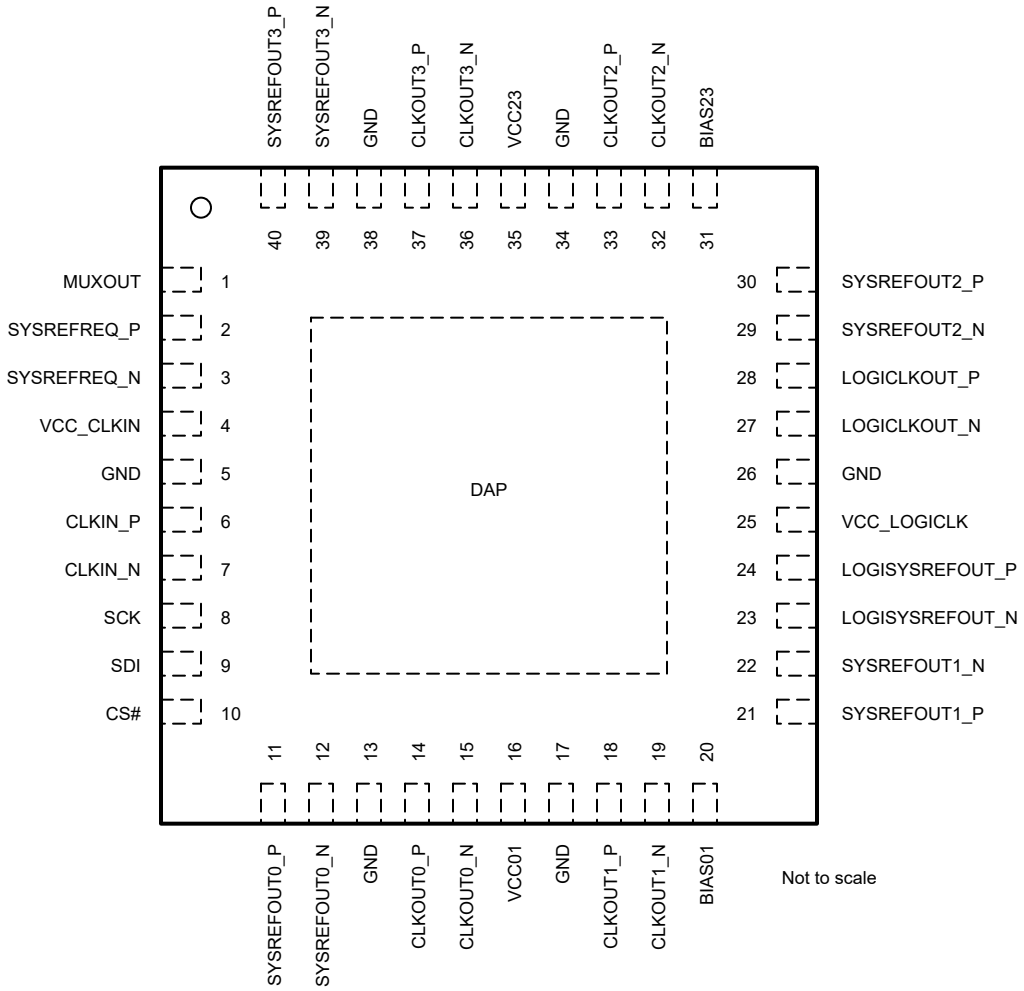


図 4-1. RHA Package 40-Pin VQFN Top View

表 4-1. Pin Functions

NAME	NO.	TYPE(1)	DESCRIPTION
BIAS01	20	BYP	If not using the multiplier, this pin can be left open. If using the multiplier, bypass this pin to GND with a 10-nF capacitor for optimal noise performance.
BIAS23	31	BYP	If not using the multiplier, this pin can be left open. If using the multiplier, bypass this pin to GND with a 10-µF and 0.1-µF capacitor for optimal noise performance.
CLKIN_N	7	I	Differential reference input clock. Internal 50-Ω termination. AC-couple with a capacitor appropriate to the input frequency (typically 0.1 µF or smaller). If using single-ended, terminate unused side with a series AC-coupling capacitor 50-Ω resistor to GND.
CLKIN_P	6		
CLKOUT0_N	15	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required.
CLKOUT0_P	14		
CLKOUT1_N	19		
CLKOUT1_P	18		
CLKOUT2_N	32		
CLKOUT2_P	33		
CLKOUT3_N	36		
CLKOUT3_P	37		
CS#	10	I	SPI chip select. High impedance CMOS input. Accepts up to 3.3 V.
DAP	DAP	GND	Ground these pins.
GND	5,13,17,26,34,38		
LOGICLKOUT_N	27	O	Differential clock output pair. Selectable CML, LVDS, or LVPECL format. Programmable common-mode voltage.
LOGICLKOUT_P	28		
LOGISYSREFOUT_N	23	O	Differential clock output pair. Selectable CML, LVDS, or LVPECL format. Programmable common-mode voltage.
LOGISYSREFOUT_P	24		
MUXOUT	1	O	Multiplexed pin serial data readback and lock status of the multiplier.
SCK	8	I	SPI clock. High impedance CMOS input. Accepts up to 3.3 V.
SDI	9	I	SPI data input. High impedance CMOS input. Accepts up to 3.3 V.
SYSREFREQ_N	3	I	Differential SYSREF request input for JESD204B support. Internal 50-Ω AC coupled to internal common-mode voltage or capacitor to GND. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2 to 2 V.
SYSREFREQ_P	2		
SYSREFOUT0_N	12	O	Differential SYSREF CML output pairs for JESD204B support. Supports AC and DC coupling with programmable common-mode voltage of 0.6 to 2 volts.
SYSREFOUT0_P	11		
SYSREFOUT1_N	22		
SYSREFOUT1_P	21		
SYSREFOUT2_N	29		
SYSREFOUT2_P	30		
SYSREFOUT3_N	39		
SYSREFOUT3_P	40		
VCC_CLKIN	4	PWR	Connect to a 2.5-V supply. Recommend a shunt high frequency capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF) farther away.
VCC_LOGICLK	25		
VCC01	16		
VCC23	35		

(1) I = Input, O = Output, GND = Ground, PWR = Power, BYP = Bypass

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Power supply voltage	–0.3	2.75	V
V_{IN}	DC Input Voltage (SCK, SDI, CSB)	GND	3.6	V
V_{IN}	DC Input Voltage (SYSREFREQ)	GND	V_{DD} + 0.3	V
V_{IN}	AC Input Voltage (CLKIN)		V_{DD}	Vpp
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.4	2.5	2.6	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

SYMBOL	THERMAL METRIC (1)	VALUE	UNIT
		RHA (VQFN)	
		40 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Consumption							
I_{CC}	Supply Current (1)	Powered up, all outputs and SYSREF on			1050		mA
		Powered up, all outputs on, all SYSREF off			600		
		Powered up, all outputs and SYSREF off			265		
		Powered down(2)			11		
SYSREF							
f_{SYSREF}	SYSREF output frequency	Generator mode				200	MHz
		Repeater mode				100	MHz
Δt	SYSREF delay step size	f_{CLKIN} = 12.8 GHz			3		ps
t_{RISE}	Rise time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		120		ps
			LVDS		120		ps
			LVPECL		230		ps
t_{FALL}	Fall time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		120		ps
			LVDS		120		ps
			LVPECL		170		ps
V_{OD}	Differential output voltage	SYSREFOUT			0.85		Vpp
		LOGISYSREFOUT	CML		0.4		Vp
			LVDS		0.4		Vp
			LVPECL		0.8		Vp
$V_{SYSREFCM}$	Common mode voltage	SYSREFOUT	CML SYSREFOUTx_PWR=4 100 Ω Differential Load		0.8		V
SYSREFREQ Pins							
$V_{SYSREFIN}$	Voltage input range	AC differential voltage		0.8		2	Vpp
V_{CM}	Input common mode	Differential 100 Ω Termination, DC coupled Set externally		1.2	1.3	2	V
Clock Input							
f_{IN}	Input frequency			0.3		12.8	GHz
P_{IN}	Input power	Single-ended power at CLKIN_P or CLKIN_N		0		10	dBm
Clock Outputs							
f_{OUT}	Output frequency	Divide-by-2		0.15		6.4	GHz
f_{OUT}	Output frequency	Buffer Mode		0.3		12.8	
f_{OUT}	Output frequency	x1 (filter mode) , x2, x3, x4		3.2		6.4	
f_{OUT}	Output frequency	LOGICLK output		1		800	MHz
t_{CAL}	Calibration-time	Multiplier calibration time	f_{IN} = 3.2 GHz; x2 f_{SMCLK} = 28 MHz		750		µs
p_{OUT}	Output power	Single-Ended	$f_{CLKLOUT}$= 6 GHz OUTx_PWR = 7		4		dBm
t_{RISE}	Rise time (20% to 80%)	f_{CLKOUT} = 300 MHz			45		ps
t_{FALL}	Fall time (20% to 80%)	f_{CLKOUT} = 300 MHz			45		ps
Propagation Delay and Skew							
$\lvert t_{SKEW} \rvert$	Magnitude of skew between outputs	CLKOUTx to CLKOUTy, not LOGICLK			1	15	ps

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Noise, Jitter, and Spurs							
J_{CKx}	Additive jitter	Additive Jitter. 12k to 100 MHz integration bandwidth.	Buffer Mode		5		fs, rms
			Filter Mode		12		
			x2 Multiplier		16		
			x3 Multiplier		21		
			x4 Multiplier		26		
Flicker	1/f flicker noise	Slew Rate > 8 V/ns, f_{CLK} = 6 GHz	Buffer Mode		-154		dBc/Hz
NF	Noise Floor	f_{OUT} = 6 GHz; f_{Offset} ≥ 100 MHz	Buffer Mode		-161		dBc/Hz
NF			Divide-by-2		-160.5		
NF			Multiplier (x1, x2,x3,x4)		–161.5		
NFL	Noise Floor	LOGICLK output, 300 MHz	CML		-150.5		dBc/Hz
NFL			LVDS		-151.5		
NFL			LVPECL		-153.5		
H2	Second harmonic	f_{OUT} = 6 GHz (differential), Buffer Mode			-25		dBc
		f_{OUT} = 6 GHz (single-ended), Buffer Mode			-13		
		f_{OUT} = 6 GHz, single-ended, Divide by 2			-16		
H1/2	Input clock leakage spur	f_{OUT} = 6 GHz (single-ended)	x2 (f_{SPUR} = 3 GHz)		-40		dBc
H1/3			x3 (f_{SPUR} = 2 GHz)		–50		
H1/4			x4 (f_{SPUR} = 1.5 GHz)		-54		dBc
I_{SPUR}	LOGICLK to CLKOUT	f_{SPUR} = 300 MHz (differential)			–70		dBc
Digital Interface (SCK, SDI, CS#, MUXOUT)							
V_{IH}	High-level input voltage	SCK, SDI, CS#		1.4		3.3	V
V_{IL}	Low-level input voltage			0		0.4	
V_{OH}	High-level output voltage	I_{OH} = 5 mA		1.4		Vcc	
		I_{OH} = 0.1 mA		2.2		Vcc	
V_{OL}	Low-level output voltage	I_{OL} = 5 mA				0.45	
I_{IH}	High-level input current			-42		42	uA
I_{IL}	Low-level input current			–25		25	

(1) Unless Otherwise Stated, f_{CLKIN}=6 GHz, CLK_MUX=Buffer, All clocks on with OUTx_PWR=7, SYSREFREQ_MODE=1
(2) For powered down mode, if the LOGISYSREFOUT field is set to LVPECL mode AND the LVPECL resistors are placed, this powerdown current increases to approximately 40 mA.

5.6 Timing Requirements

			MIN	NOM	MAX	UNIT
Timing Requirements						
f_{SPI}	SPI Read/Write Speed				2	MHz
t_{CE}	Clock to enable low time		20			ns
t_{CS}	Clock to data wait time		20			ns
t_{CH}	Clock to data hold time		20			ns
t_{CWH}	Clock pulse width high		100			ns
t_{CWL}	Clock pulse width low		100			ns
t_{CES}	Enable to clock setup time		20			ns
t_{EWH}	Enable pulse width high		50			ns
t_{CD}	Falling clock edge to data wait time		100			ns

5.7 Timing Diagram

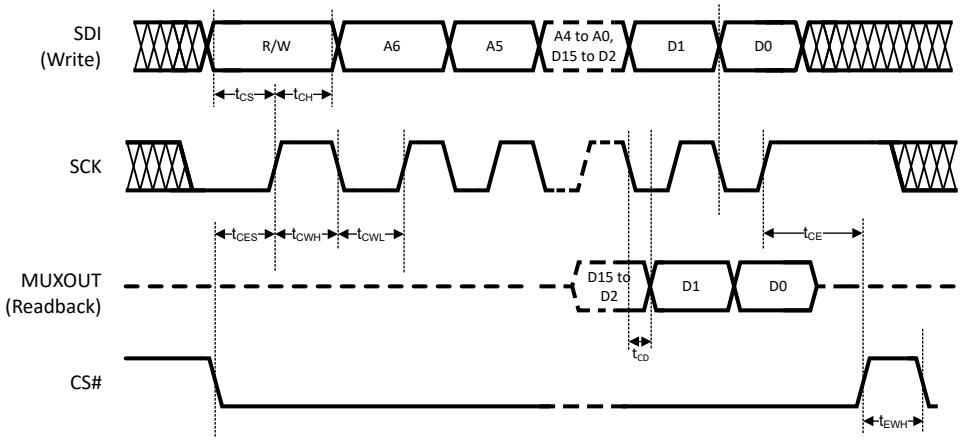


図 5-1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

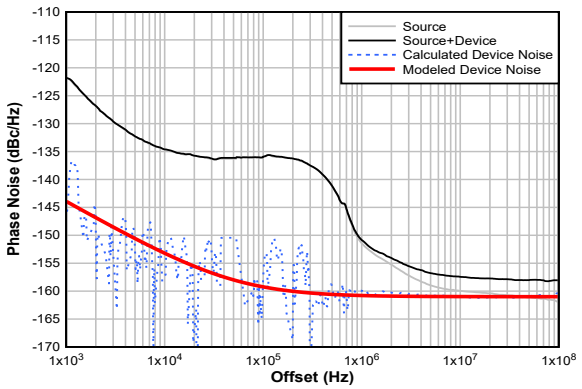
- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CS# must be held low for data to be clocked. The device ignores clock pulses if CS# is held high.
- Recommended SPI settings for this device are CPOL=0 and CPHA=0.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CS# line high on the device that is not to be clocked.

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin is always be low for the address portion of the transaction.
- The data on MUXOUT is clocked out at the falling edge of SCK. In other words, the readback data is available at the MUXOUT pin t_{CD} after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.
- The MUXOUT pin does not automatically tri-state after a readback transaction completes. When sharing the SPI bus readback pin with other devices, set MUXOUT_EN=0 after all readback transactions from device are complete to manually tri-state the MUXOUT pin, permitting other devices to control the readback line.
- The values read back, even for R/W bits are not always the value written but rather an internal device state that takes into account the programmed value as well as other factors, such as pin states.

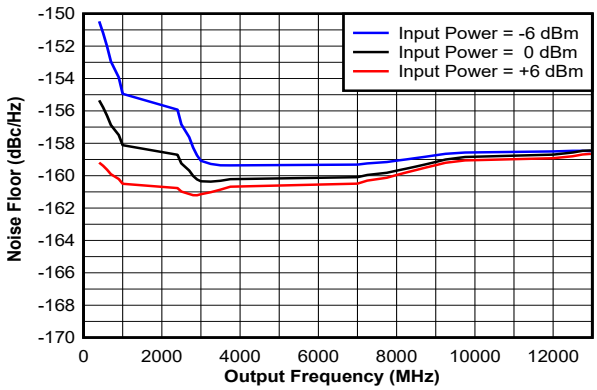
5.8 Typical Characteristics

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.



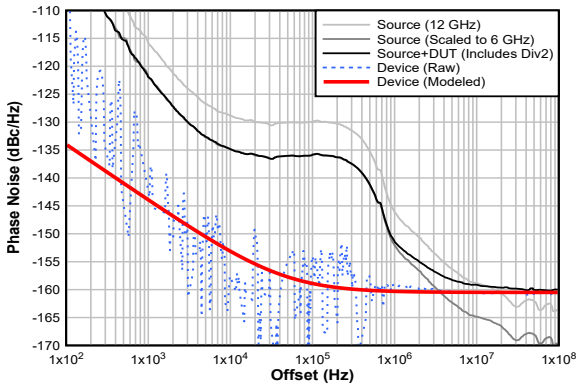
Noise Floor = –161 dBc/Hz, 1/f Noise = –154 dBc/Hz @ 10 kHz, Integrates to 28 fs jitter from 100 Hz to 6 GHz offset

図 5-2. Buffer Phase Noise Plot at 6 GHz Output



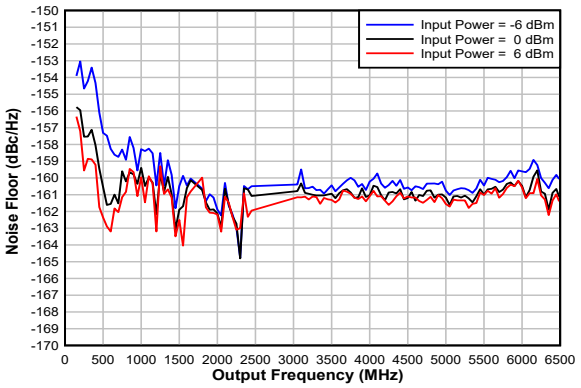
Stated input power is applied at each pin.

図 5-3. Noise Floor in Buffer Mode



Noise Floor = –160.5 dBc/Hz, 1/f Noise = –154 dBc/Hz @ 10 kHz, Integrates to 30 fs jitter from 100 Hz to 6 GHz offset

図 5-4. Divide by 2 Phase Noise Plot at 6 GHz Output



Stated input power is applied at each pin.

図 5-5. Noise Floor With Divide by 2

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.

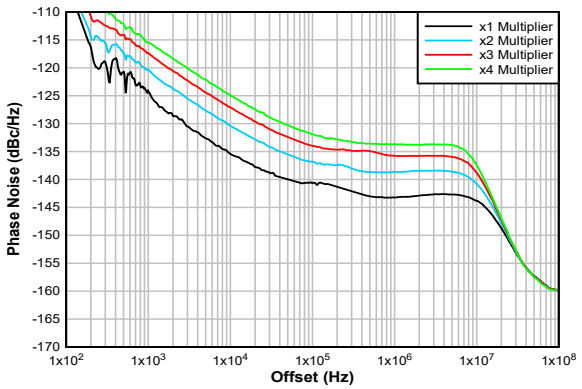
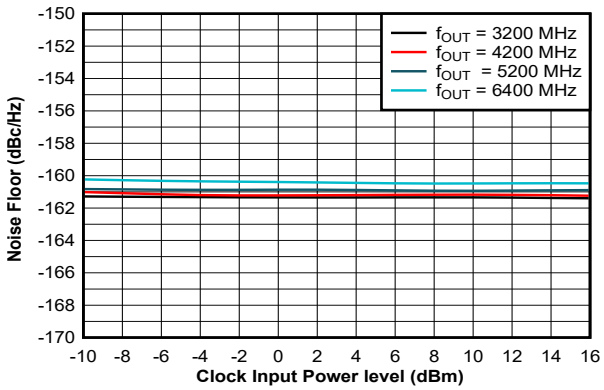


図 5-6. Multiplier Phase Noise Plot at 6 GHz Output



注

Input power in graph is differential.

図 5-7. Noise Floor in Multiply x2 Mode

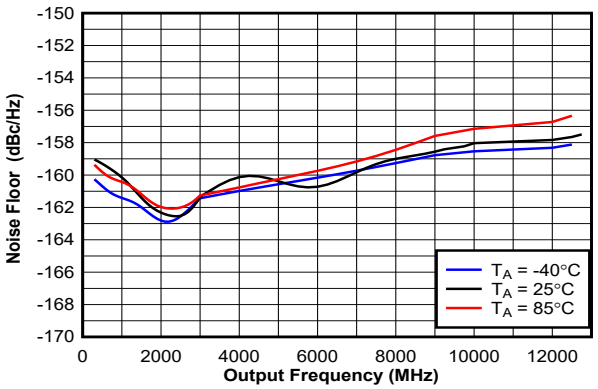


図 5-8. Noise Floor in Buffer Mode

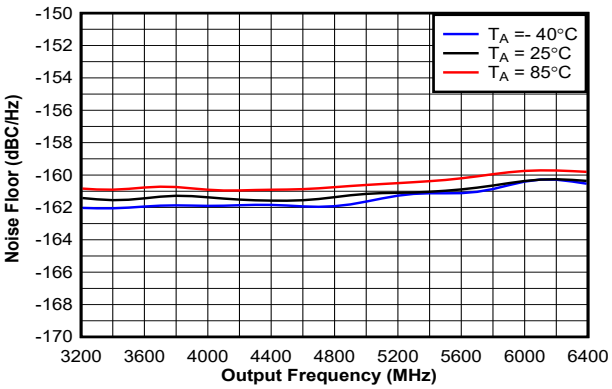


図 5-9. Noise Floor in x2 Multiplier Mode

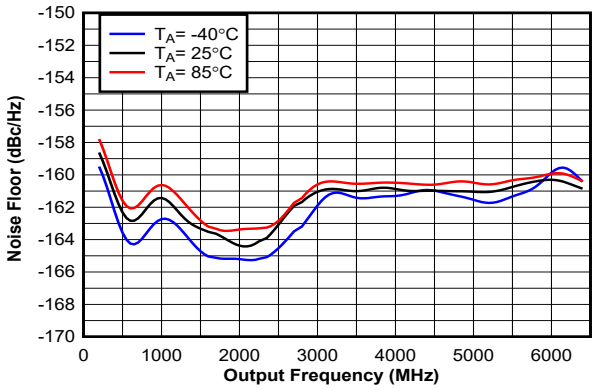


図 5-10. Noise Floor in Divide by 2 Mode

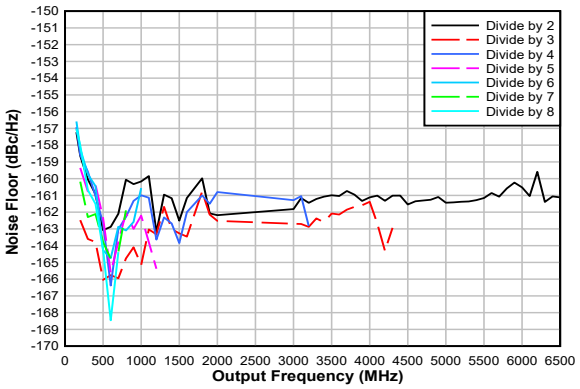
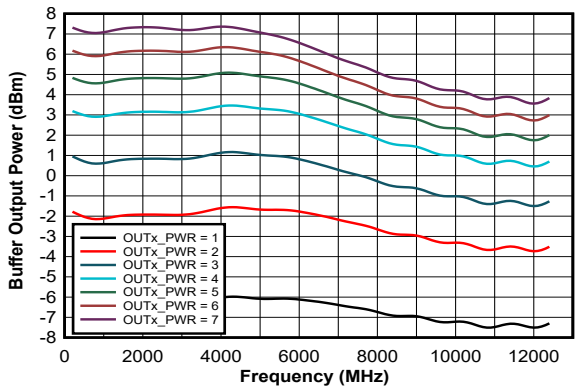


図 5-11. Noise Floor in Divider Mode

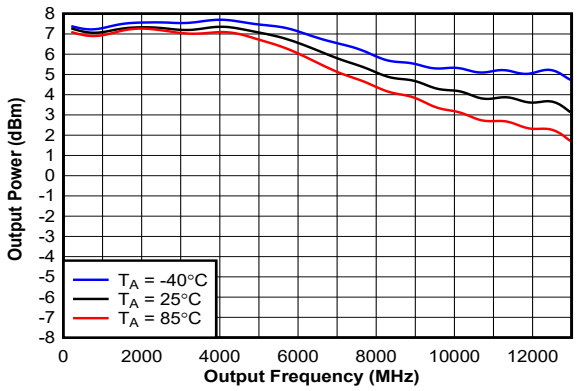
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.



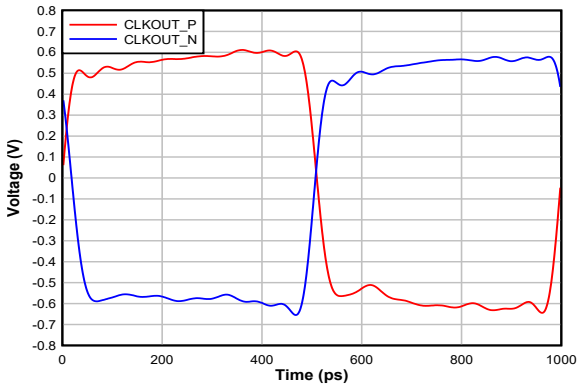
Applies to all modes except divider mode with odd divide (which has slightly lower power).

図 5-12. Single-Ended Output Power



CLKOUTx_PWR = 7

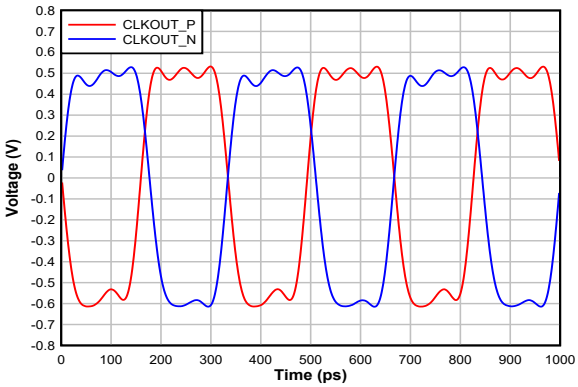
図 5-13. Single-Ended Output Power



注

CLKOUTx_PWR=7

図 5-14. CLKOUT Waveform at 1 GHz



注

CLKOUTx_PWR=7

図 5-15. CLKOUT Waveform at 3 GHz

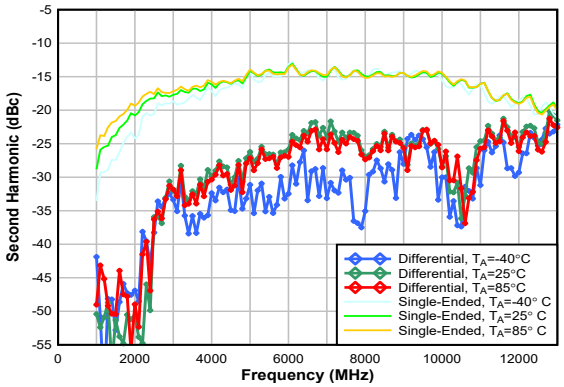


図 5-16. Second Harmonic in Buffer Mode

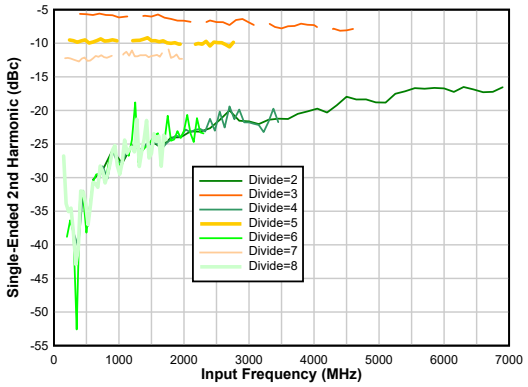


図 5-17. Second Harmonic in Divide Mode (Single-Ended)

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.

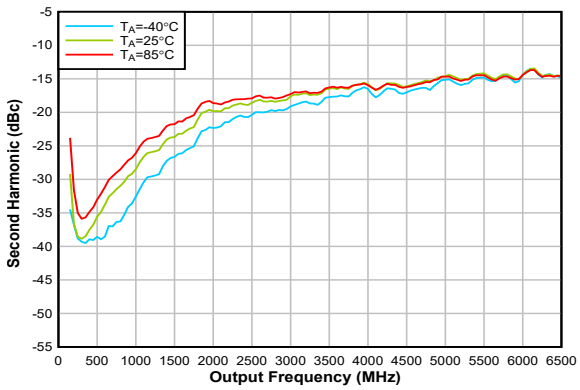


図 5-18. Second Harmonic in Divide by 2 Mode (Single-Ended)

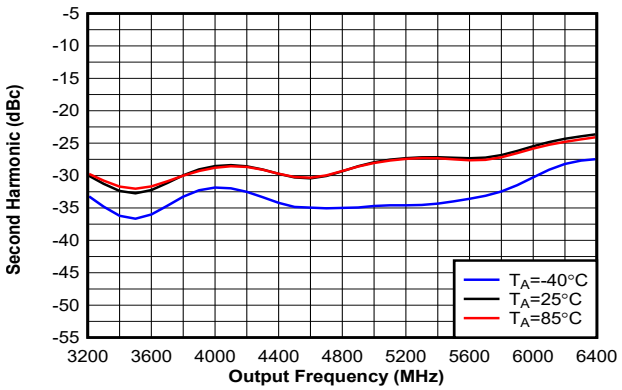
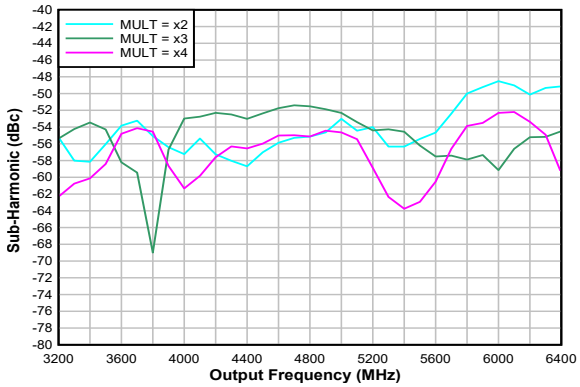


図 5-19. Second Harmonic in Multiply X2 Mode (Differential)



注

Output is differential.

図 5-20. Multiplier Sub-Harmonics (Harmonic Frequency = Output Frequency / M)

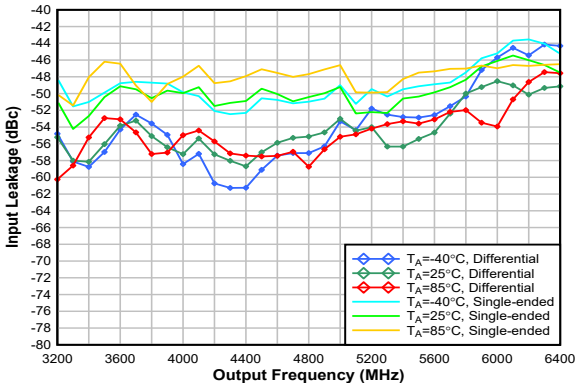


図 5-21. Multiplier 1/2 Sub-Harmonic in X2 Mode

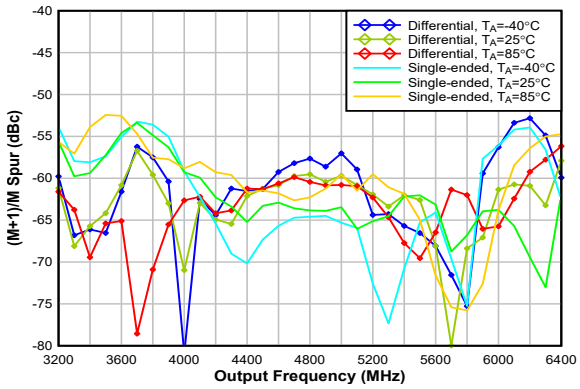


図 5-22. Multiplier Intermodulation Spur (MULT=2)

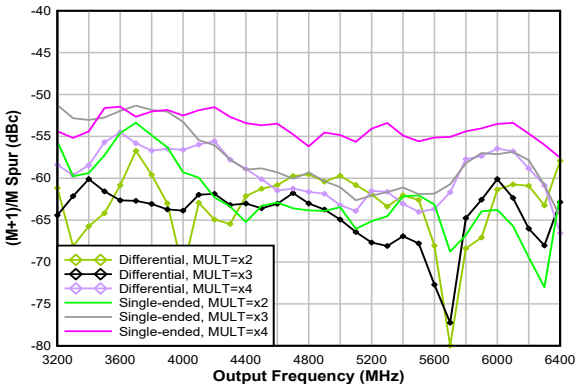
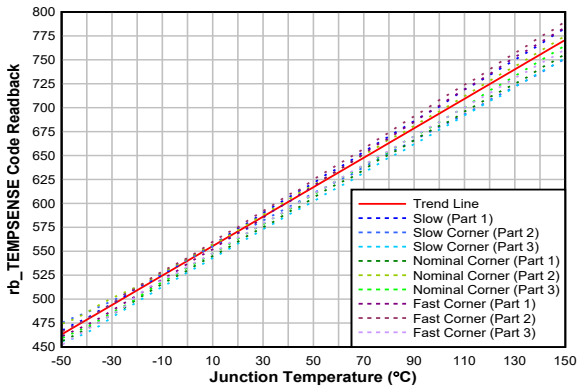


図 5-23. Multiplier Intermodulation (M+1)/M Spur

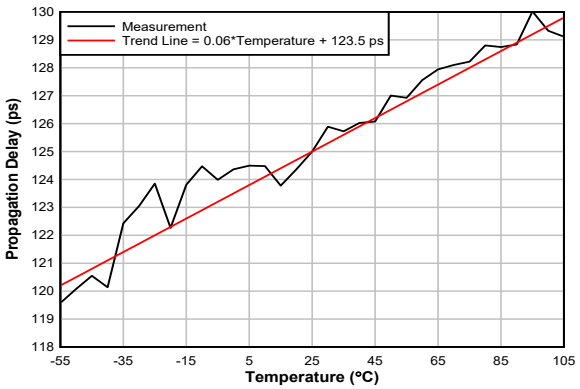
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.



Measured in power-down mode to make Junction Temperature = Ambient temperature.

図 5-24. Temperature Sensor Readback



Over 30 devices and 3 corner lots, propagation delay varied 1.1 ps over process and 7 ps overall when the temperature is held at a constant 25°C.

図 5-25. Propagation Delay

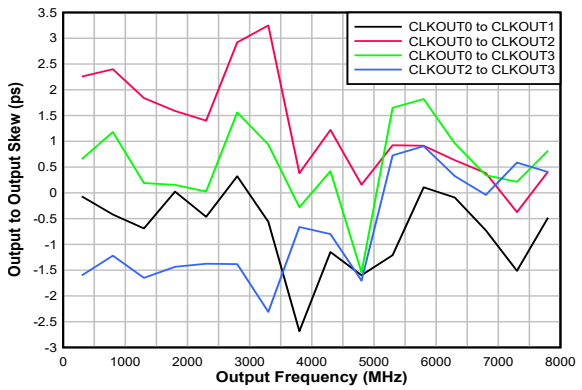
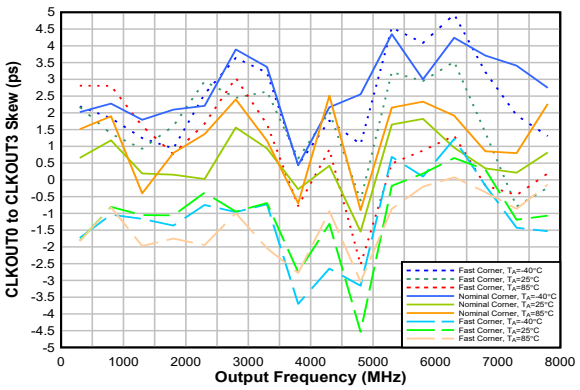


図 5-26. Output to Output Skew



Main source of skew variation is frequency and measurement error. Other observed sources of variation include about 3 ps over process corners and 1.5 ps over temperature.

図 5-27. Output to Output Skew Variation for CLKOUT0 to CLKout3

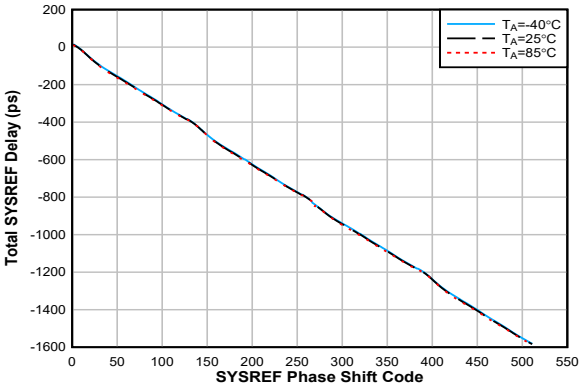


図 5-28. SYSREF Delay vs. Temperature and Code (Fout = 10 GHz)

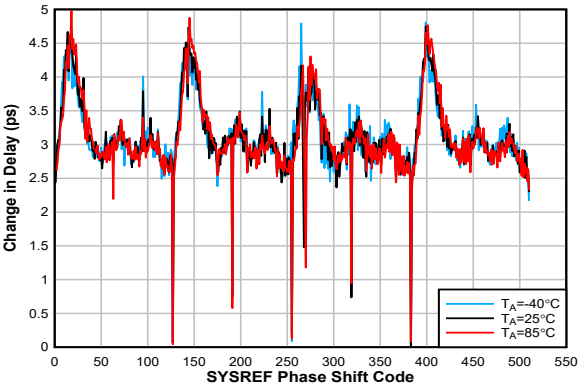


図 5-29. SYSREF Delta Delay vs. Temperature and Code (Fout=10 GHz)

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.

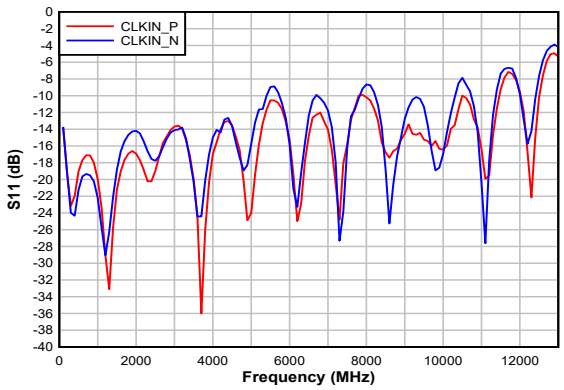


図 5-30. CLKIN S11 Magnitude

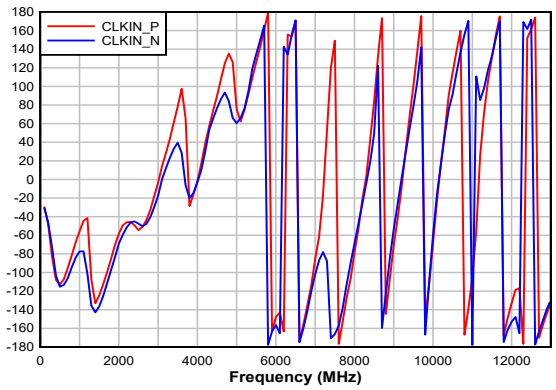


図 5-31. CLKIN S11 Phase

6 Detailed Description

6.1 Overview

The LMX1204 has four main clock outputs and another LOGICLK output. The main clock outputs are all the same frequency. This frequency can be the same, divided, or multiplied relative to the input clock. Each of these clock outputs has programmable power level. The LOGICLK output frequency is independent and typically lower frequency than the other four main clocks and has programmable output format (CML, LVDS, LVPECL) and power level.

The SYSREF can be generated by either repeating the input from the SYSREFREQ pins, or internally generated. There is an internal SYSREF windowing feature that allows the internal timing of the device to be adjusted to optimize setup/hold times of the SYSREFREQ input with respect to the CLKIN input. This feature assumes that the delay between the SYSREF edge and the next rising clock edge is consistent. Each of the five outputs has a corresponding SYSREF output that has individual delays and programmable common mode. For the LOGISYSREF output, the output format is programmable as CML, LVDS, or LVPECL.

6.1.1 Range of Dividers and Multiplier

There are dividers that allow the main and LOGICLK outputs to be a divided value of the input clock. The main clock outputs also have a multiplier. In addition to this, dividers are used for SYSREF generation in generator mode as well as generation of the delay block.

表 6-1. Range of Dividers and Multiplier

CATEGORY			RANGE	COMMENTS
Main Clocks	Buffer			
	Divider		2, 3, 4, … 8	Odd divides (except 1) do not have 50% duty cycle
	Multiplier		1,2, 3, 4	x1 Multiplier and Filter mode are the same thing.
LOGICLK	Divide	PreDivide	1, 2, 4	TotalDivide = PreDivide × Divide Odd divides (except 1) do not have 50% duty cycle
		Divide	1, 2, 3, … 1023	
SYSREF	Divide for frequency generation	PreDivide	1,2, 4	Pre-divides clock for phase interpolator. TotalDivide = PreDivide×Divide Odd divides do not have 50% duty cycle
		Divide	2, 3, 4,… 4095	
	Divide for delay generation	Divide	2, 4, 8, 16	This divide is set according to the input frequency.

6.2 Functional Block Diagram

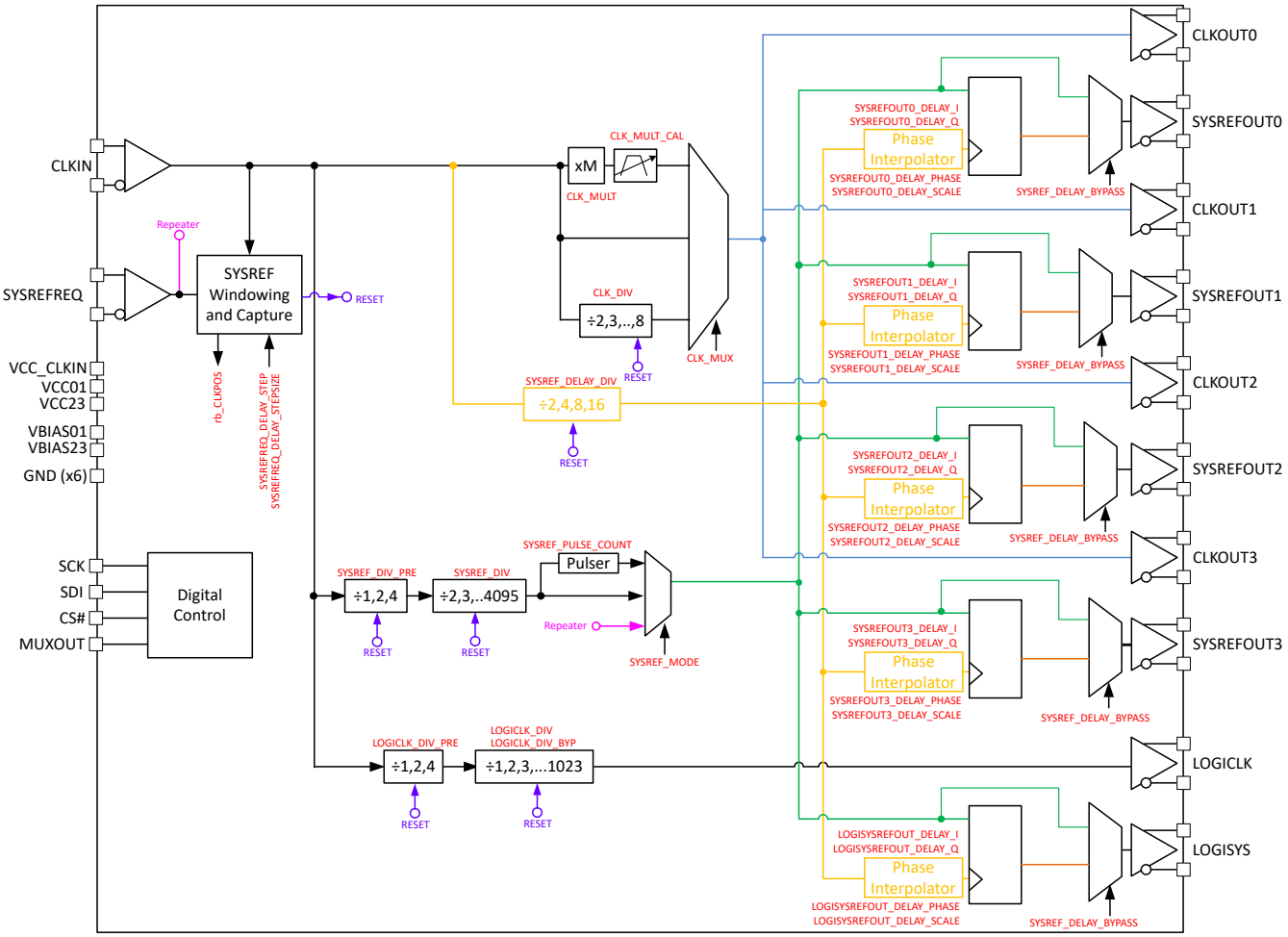


図 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power On Reset

When the device is powered up, the power on reset (POR) resets all registers to a default state as well as resets all state machines and dividers. For the power on reset state, all SYSREF outputs are disabled and all the dividers are bypassed; the device functions as a 4-output buffer. Users must wait 100 µs after the power supply rails before programming other registers to verify that the RESET is finished. If the power on reset happens when there is no device clock present, the device functions properly, however, the current changes once an input clock is presented.

\Performing a software power on reset by writing RESET=1 in the SPI bus is both possible and generally good practice. The RESET bit self-clears once any other register is written to. The SPI bus can be used to override these states to the desired settings.

Although the device does have an automatic power on reset, the device can be impacted by different ramp rates on the different supply pins, especially in the presence of a strong input clock signal. Performing a software reset after POR is recommended. This reset can be done by programming RESET=1. The reset bit can be cleared by programming any other register or setting RESET back to zero. Even at maximum allowed SPI bus speed, the software reset event always completes before the subsequent SPI write.

6.3.2 Temperature Sensor

The junction temperature can be read back for purposes such as characterization or to make adjustments based on temperature. Such adjustments can include adjusting CLKOUTx_PWR to make the output power more stable or using external or digital delays to compensate for changes in propagation delay over temperature.

The junction temperature is typically higher than the ambient temperature due to power dissipation from the outputs and other functions on the device. 式 1 shows the relationship between the code read back and the junction temperature.

$$\text{Temperature} = 0.65 \times \text{Code} - 351 \quad (1)$$

式 1 is based on a best-fit line created from three devices from slow, nominal, and fast corner lots (nine parts total). The worst-case variation of the actual temperature from the temperature predicted by the best-fit line is 13°C, which works out to 20 codes.

6.3.3 Clock Outputs

This device has four main output clocks which share a common frequency. This does not include the additional lower frequency LOGICLK output.

6.3.3.1 Clock Output Buffers

The output buffers have a format that is open collector with an integrated pullup resistor, similar to CML.

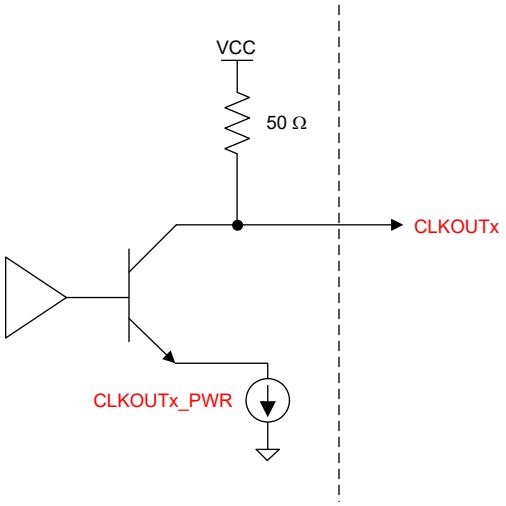


図 6-2. CLKOUT Output Buffer

The CLKOUTx_EN bits can enable the output buffers. The output power of the buffers can be individually set with the CLKOUTx_PWR field. However, these fields only control the output buffer, not the internal channel path that drives this buffer. To power down the entire path, disable the CHx_EN bit.

表 6-2. Clock Output Power

CHx_EN	INTERNAL CHANNEL PATH	CLKOUTx_EN	CLKOUTx_PWR	OUTPUT BUFFER
0	Powered Down	Don't Care	Don't Care	Powered Down
1	Powered Up	0	Don't Care	Powered Down
		1	0	Minimum
			1	
			...	
			7	Maximum

6.3.3.2 Clock MUX

The four main clocks must be the same frequency, but this frequency can be bypassed, multiplied, or divided. This is determined by the CLK_MUX word.

表 6-3. Clock MUX

CLK_MUX	OPTION	VALUES SUPPORTED
0	Buffer Mode	÷1 (bypass)
1	Divider Mode	÷2, 3, 4, 5, 6, 7, and 8
2	Multiplier Mode	x1 (filter mode), x2, x3, x4

6.3.3.3 Clock Divider

Set the CLK_MUX to Divided to a divide value by 2, 3, 4, 5, 6, 7, or 8. This is set by the CLK_DIV word. When using the clock divider, any change to the input frequency requires the CLK_DIV_RST bit to be toggled from 1 to 0.

表 6-4. Clock Divider

CLK_DIV	DIVIDE	DUTY CYCLE
0	Reserved	n/a
1	2	50%
2	3	33%

表 6-4. Clock Divider (続き)

CLK_DIV	DIVIDE	DUTY CYCLE
3	4	50%
4	5	40%
5	6	50%
6	7	43%
7	8	50%

6.3.3.4 Clock Multiplier and Filter Modes

6.3.3.4.1 General Information About the Clock Multiplier

The clock multiplier can be used to multiply up the input clock frequency by a factor of ×1, ×2, ×3, or ×4. The multiply value is set by the CLK_MULT field. As the multiplier is PLL-based and includes an integrated VCO, the multiplier has a state machine clock, requires calibration, has a lock detect feature, and can be used as a tunable filter. Note that if the multiplier is not being used, there is no need for the state machine clock or the lock detect feature.

6.3.3.4.2 State Machine Clock for the Clock Multiplier

The state machine clock frequency, f_{SMCLK}, is derived by dividing down the input clock frequency by a programmed divider value. The state machine clock is also necessary for the multiplier calibration and lock detect. If there are concerns about the state machine clock creating spurs, then the state machine can be shut off provided that the multiplier calibration is not running and the lock detect feature is not being used.

6.3.3.4.2.1 State Machine Clock

If not using the clock multiplier, the state machine clock must be disabled by setting SMCLK_EN=0 to minimize crosstalk and spurs. However, when using the clock multiplier, the state machine clock is required to run the calibration engine when the frequency is changed and also used to have the lock detect continuously monitor if the PLL-based clock multiplier is in lock. The state machine clock must be less than 30MHz. Consult the register map document for more details.

6.3.3.4.3 Calibration for the Clock Multiplier

For optimal phase noise, the VCO in the multiplier divides up the frequency range into many different bands and cores and has optimized amplitude settings for each one of these bands. For this reason, upon initial use, or whenever the frequency is changed, a calibration routine needs to be run to determine the correct core, frequency band, and amplitude setting. Calibration is performed by programming the R0 register with a valid input signal. Increasing the speed of the state machine clock speeds up the multiplier calibration time. To provide reliable multiplier calibration, the state machine clock frequency needs to be at least twice the SPI write speed, but no more than 30MHz. Whenever the CLK_MUX mode is changed or the multiplier is calibrated for the first time, the calibration time is substantially longer, on the order of 5ms.

6.3.3.4.4 Using the x1 Clock Multiplier as a Filter

As the multiplier is PLL based, the multiplier acts as a programmable filter that attenuates noise, spurs, harmonics, and sub-harmonics that are outside the PLL loop bandwidth (about 10MHz). Filter mode (x1 Multiplier) allows the user to use the clock multiplier as a tunable filter with 10MHz bandwidth that has lower additive noise than the higher multiply values. In this filter mode, the spurs are first amplified by the input stage and then attenuated by the loop filter making this mode most effective for filtering spurs at offsets of 100MHz or higher. Note that the filter mode is different than buffer mode because filter mode filters the input frequency, but adds more close in phase noise. A x1 multiplier value does not support the SYNC operation. At frequencies above 4.2GHz, there is a possibility of the subharmonics at Fref/3. These subharmonics can be eliminated by using the filter at the output.

6.3.3.4.5 Lock Detect for the Clock Multiplier

The lock detect status of the multiplier can be read back through the rb_LD field or from the MUXOUT pin. The state machine clock must be running for the lock detect to work properly.

6.3.4 Device Functional Modes Configurations

The device can configure in high frequency clock buffer, divider or multiplier mode. Each mode requires the below register configurations for functioning.

表 6-5. Configurations for Device Functional Modes

REGISTER ADDRESS	BIT	FIELD	FUNCTION	BUFFER	DIVIDER	MULTIPLIER
R25	2:0	CLK_MUX	Select the mode	1	2	3
R25	5:3	CLK_DIV / CLK_MULT	Select the division or multiplication value	x	CLK_DIV 0x1 = ÷2 0x2 = ÷3 0x3 = ÷4 0x4 = ÷5 0x5 = ÷6 0x6 = ÷7 0x7 = ÷8	CLK_MULT 0x2 = x2 0x3 = x3 0x4 = x4
R2	5	SMCLK_EN	Enables the state machine clock generator	x	x	1
R2	9:6	SMCLK_DIV_PRE	Sets pre-divider for state machine clock	x	x	Pre-clock divider for state machine clock 0x2 = ÷2 0x4 = ÷4 0x8 = ÷8
R3	2:0	SMCLK_DIV	Sets state machine clock divider	x	x	Additional SMCLK divider to keep output frequency must be ≤ 30 MHz. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = ÷8 0x4 = ÷16 0x5 = ÷32 0x6 = ÷64 0x7 = ÷128
R0	All	Calibrate Multiplier	Calibrate the PLL based multiplier	x	x	Write R0 for calibrate multiplier

6.3.5 LOGICLK Output

The LOGICLK output can be used to drive devices using lower frequency clocks, such as FPGAs. The LOGICLK output has a programmable output format and a corresponding SYSREF output.

6.3.5.1 LOGICLK Output Format

The LOGICLK output format can be programmed to LVDS, LVPECL, and CML modes. Depending on the format, the common mode can be programmable or external components can be required (see 表 6-6).

表 6-6. LOGICLK Formats and Properties

LOGICLKOUT_FMT	FORMAT	EXTERNAL COMPONENTS REQUIRED	OUTPUT LEVEL	COMMON MODE
0	LVDS	None	Fixed	Programmable through LOGICLKOUT_VCM
1	LVPECL	Emitter Resistors	Fixed	Not programmable
2	CML	Pullup Resistors 50 Ω to V_{CC}	Programmable through LOGICLKOUT_PWR	Not programmable
3	Invalid			

6.3.5.2 LOGICLK_DIV_PRE and LOGICLK_DIV Dividers

The LOGICLK_DIV_PRE divider and LOGICLK_DIV dividers are used for the LOGICLK output. The LOGICLK_DIV_PRE divider is necessary to divide the frequency down to verify that the input to the LOGICLK_DIV divider is 3.2GHz or less. When LOGICLK_DIV is not even and not bypassed, the duty cycle is not 50%. Both the LOGICLK dividers are synchronized by the SYNC feature, which allows synchronization across multiple devices.

表 6-7. Minimum N-Divider Restrictions

f_{CLKIN} (MHz)	LOGICLK_DIV_PRE	LOGICLK_DIV	TOTAL DIVIDE RANGE
f_{CLKIN} ≤ 3.2 GHz	÷1, 2, 4	÷1, 2, 3, …1023	[1, 2, ...1023] [2, 4, ... 2046] [4, 8, 4092]
3.2GHz < f_{CLKIN}≤ 6.4 GHz	÷2, 4	÷1, 2, 3, …1023	[4, ... 2046] [4, 8, 4092]
f_{CLKIN} > 6.4 GHz	÷4	1, 2, 3, …1023	[8, 4092]

6.3.6 SYSREF

SYSREF allows a low frequency JESD204B/C compliant signal to be produced that is reclocked to a main or LOGICLK output. The delays between the CLKOUT and SYSREF outputs are adjustable with software. The SYSREF output can be configured as a generator using the internal SYSREF divider, or as a repeater duplicating the signal on the SYSREFREQ pins. The SYSREF generator for both the main clocks and the LOGICLK output are the same.

表 6-8. SYSREF Modes

SYSREF_MODE	DESCRIPTION
0	**Generator Mode** Internal generator creates a continuous stream of SYSREF pulses. The SYSREFREQ pins or the SYSREFREQ_SPI bit can be used to gate the SYSREF divider from the channels for improved noise isolation without disrupting the synchronization of the SYSREF dividers. The SYSREFREQ pins or the SYSREFREQ_SPI bit must be high for a SYSREF output to come out.
1	**Pulser** Internal generator generates a burst of 1 - 16 pulses that is set by SYSREF_PULSE_COUNT that occurs after a rising edge on the SYSREFREQ pins or after changing SYSREFREQ_SPI bit from 0 to 1 (assuming SYSREFREQ pins to be forced to a low state).
2	**Repeater Mode** SYSREFREQ pins input are reclocked to clock outputs and then delayed in accordance to the SYSREF_DELAY_BYPASS field before sent to the SYSREFOUT output pins.

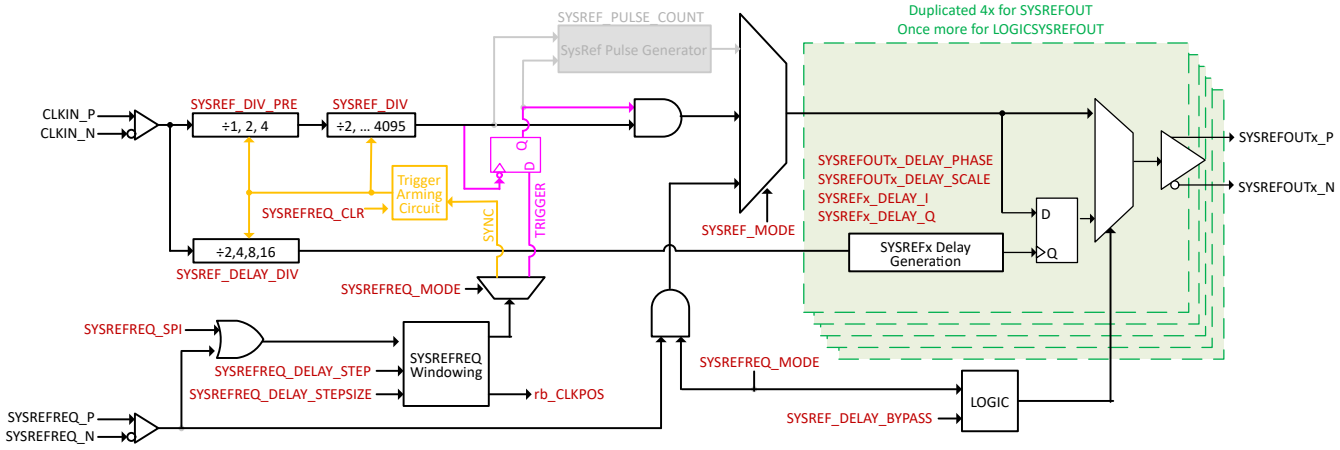


図 6-3. Functional Block Diagram of SYSREF Circuitry in Generator Mode

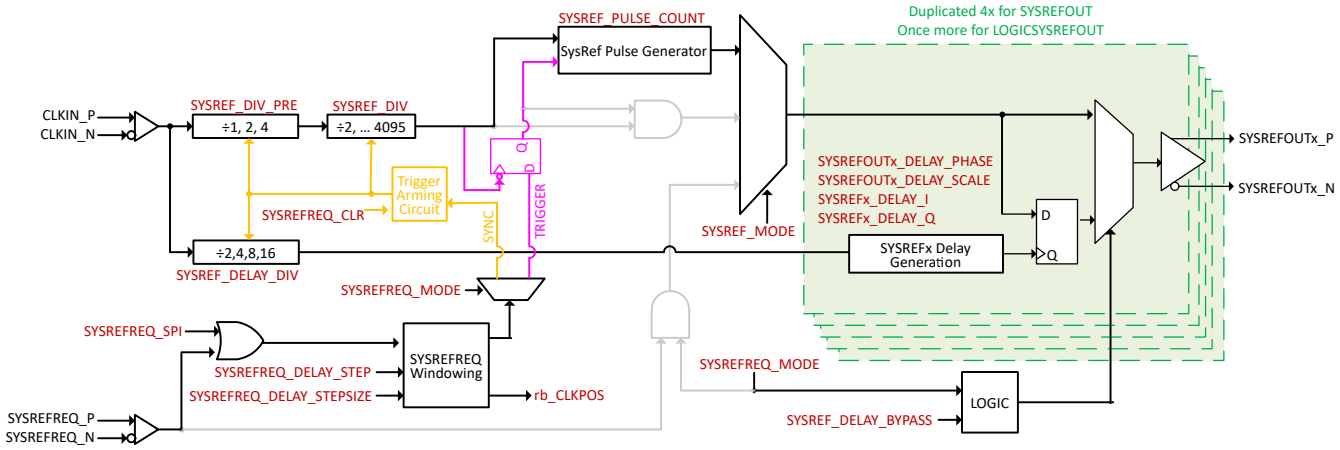


図 6-4. Functional Block Diagram of SYSREF Circuitry in Pulser Mode

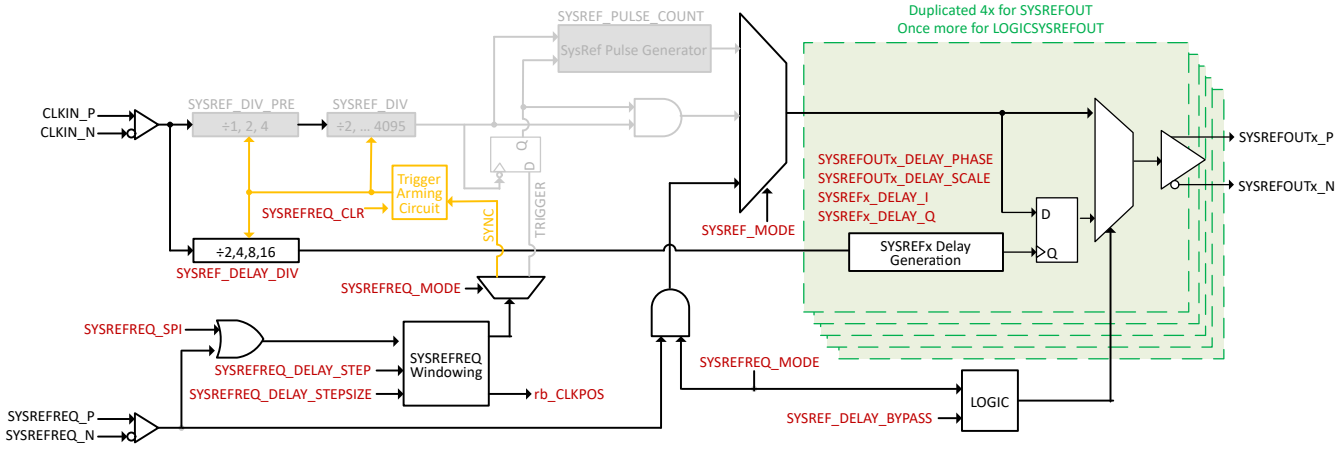


図 6-5. Functional Block Diagram of SYSREF Circuitry in Repeater Mode

To operate the SYSREFREQ_SPI bit controlled SYSREF output (Pulser) and SYNC, set the SYSREFREQ pins to low logic state externally. For example, make sure the SYSREFREQ_N pin is at a higher level (400mV) than the SYSREFREQ_P pin and maintain the input common-mode voltage requirement.

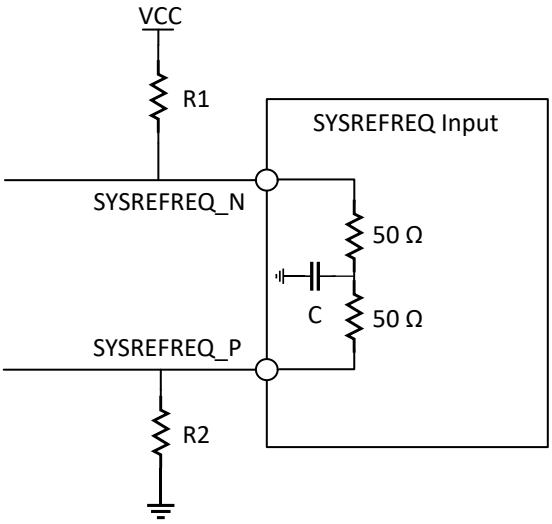


図 6-6. SYSREFREQ Pin Logic Low Setup

As an example, to maintain the minimum 400mV voltage difference for a VCC of 2.5V, the current draw through 100Ω is 4mA. In this example, keep the SYSREFREQ_P pin at 1.4V DC, set the R2 to 350Ω and the R1 to 175 Ω with 1.8V at SYSREFREQ_N pin.

6.3.6.1 SYSREF Output Buffers

6.3.6.1.1 SYSREF Output Buffers for Main Clocks (SYSREFOUT)

The SYSREF outputs within the clock output channels have the same output buffer structure as the clock output buffer, with the addition of circuitry to adjust the common-mode voltage. The SYSREF outputs are CML outputs with a common-mode voltage that can be adjusted with the SYSREFOUTx_VCM field, and the output level that can be programmed with the SYSREFOUTx_PWR field. This feature is to allow DC coupling. Note that the CLKOUT outputs do not have adjustable common-mode voltage and must be AC coupled for optimal noise performance.

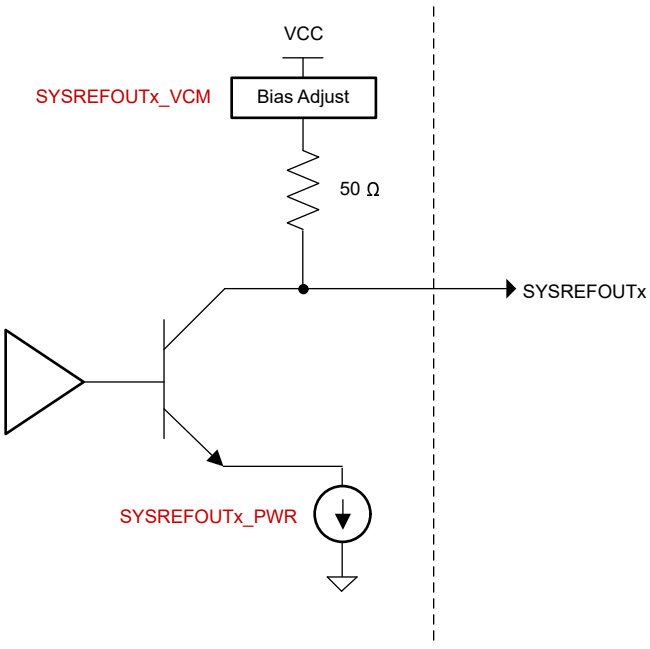


図 6-7. SYSREF Output Buffer

The common-mode voltage and output power are interrelated and can be simulated assuming a 100Ω differential load and no DC path to ground. The common mode voltage and output are interrelated as shown in 表 6-9. As there is a restriction required for long term reliability that $V_{CM} – V_{OD}/2 \geq 0.5$ V combinations of V_{CM} and V_{OD} that do not satisfy this constraint are excluded from the table.

表 6-9. Single-Ended Voltage (V_{OD}) and Common Mode Voltage (V_{CM})

SYSREFOUTx_PWR	SYSREFOUTx_VCM	V_{OD}	V_{CM}
0	0	0.31	0.91
	1	0.31	1.06
	2	0.31	1.23
	3	0.32	1.41
	4	0.32	1.58
	5	0.33	1.75
	6	0.33	1.94
	7	0.34	2.11
1	0	0.34	0.59
	1	0.35	0.76
	2	0.35	0.96
	3	0.35	1.19
	4	0.36	1.39
	5	0.36	1.59
	6	0.36	1.82
	7	0.36	2.03
2	0	0.39	0.46
	1	0.42	0.52
	2	0.44	0.69
	3	0.46	0.96
	4	0.46	1.2
	5	0.47	1.43
	6	0.48	1.7
	7	0.49	1.94
3	2	0.48	0.53
	3	0.51	0.74
	4	0.53	1.02
	5	0.54	1.27
	6	0.55	1.59
	7	0.56	1.87
4	3	0.56	0.59
	4	0.59	0.83
	5	0.61	1.13
	6	0.62	1.47
	7	0.64	1.79
5	3	0.58	0.54
	4	0.64	0.69
	5	0.67	0.98
	6	0.69	1.37
	7	0.71	1.72

表 6-9. Single-Ended Voltage (V_{OD}) and Common Mode Voltage (V_{CM}) (続き)

SYSREFOUTx_PWR	SYSREFOUTx_VCM	V_{OD}	V_{CM}
6	5	0.73	0.84
	6	0.75	1.26
	7	0.78	1.64
7	5	0.78	0.73
	6	0.82	1.15
	7	0.84	1.57

6.3.6.1.2 SYSREF Output Buffer for LOGICLK

The LOGISYSREFOUT output supports the three formats of LVDS, LVPECL, and CML. The LOGISYSREFOUT_EN enables the output buffer and LOGISYSREF_FMT sets the format. LVDS mode allows programmable common mode, LVPECL and CML require external components, and CML allows programmable output power (see 表 6-10).

表 6-10. LOGISYSREFOUT Output Buffer Configuration

LOGISYSREFOUT_EN	LOGISYSREF_FMT	LOGISYSREF FORMAT	EXTERNAL TERMINIATION REQUIRED	OUTPUT POWER	OUTPUT COMMON MODE
0	Powered Down				
1	0	LVDS	None	Fixed	Programmable with LOGISYSREF_VCM
	1	LVPECL	Emitter Resistors	Fixed	Fixed
	2	CML	Pullup resistors 50 Ω to V_{CC}	Controlled by LOGISYSREF_PWR	LOGISYSREF_VCM has no impact, but this changes with LOGISYSREF_PWR.
	3	Reserved			

6.3.6.2 SYSREF Frequency and Delay Generation

The SYSREF circuitry can produce an output signal that is synchronized to f_{CLKIN}. This output can be a single pulse, series of pulses, or a continuous stream of pulses. In generator mode, the SYSREF_DIV_PRE and SYSREF_DIV values are used to divide the CLKIN frequency to a lower frequency that is reclocked to the output. In repeater mode, this signal is instead input at the SYSREFREQ pins. For each of the outputs, there is an independent delay control.

表 6-11. SYSREF Modes

SYSREF_MODE	DESCRIPTION
0	**Generator Mode (Continuous)** Internal generator creates a continuous stream of SYSREF pulses. The SYSREFREQ pins or the SYSREFREQ_SPI field can be used to gate the SYSREF divider from the channels for improved noise isolation without disrupting the synchronization of the SYSREF dividers. The SYSREFREQ pins or the SYSREFREQ_SPI field must be high for a SYSREF output to come out.
1	**Generator Mode (Pulser)** Internal generator generates a burst of 1 - 16 pulses that is set by SYSREF_PULSE_COUNT that occurs after a rising edge on the SYSREFREQ pins
2	**Repeater Mode** SYSREFREQ pins are reclocked to clock outputs and then delayed in accordance to the SYSREF_DELAY_BYPASS field before being sent to the SYSREFOUT outputs.

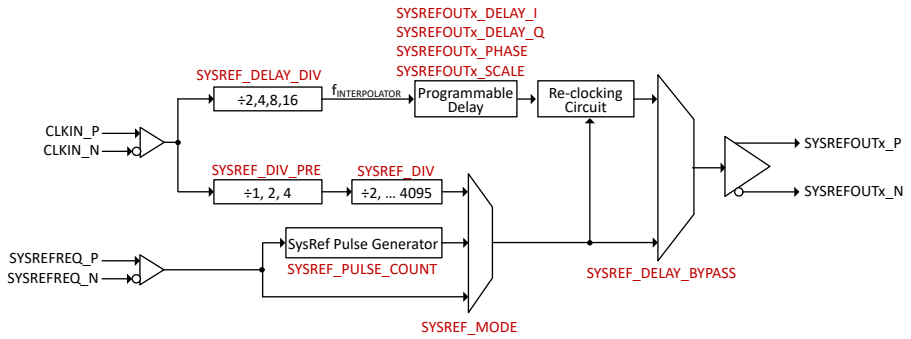


図 6-8. SYSREF Generator Diagram

For the frequency of the SYSREF output in generator mode, the SYSREF_DIV_PRE divider is necessary to verify that the input of the SYSREF_DIV divider is not more than 3.2 GHz.

表 6-12. SYSREF_DIV_PRE Setup

f_{CLKIN}	SYSREF_DIV_PRE	TOTAL SYSREF DIVIDE RANGE
3.2 GHz or Less	÷1, 2, or 4	÷2,3,4,...16380
3.2 GHz < f_{CLKIN} ≤ 6.4 GHz	÷2 or 4	÷4,6,8, … 16380
f_{CLKIN} > 6.4 GHz	÷4	÷8,12,16, … 16380

For the delay, the input clock frequency is divided by SYSREF_DELAY_DIV to generate $f_{INTERPOLATOR}$. This has a restricted range as shown in 表 6-13. Note also that when SYSREF_DELAY_BYPASS=0 or 2 (delaygen engaged for generator mode), and SYSREF_MODE = 0 or 1 (a generator mode) the SYSREF output frequency must be a multiple of the phase interpolator frequency.

$f_{INTERPOLATOR}$ % f_{SYSREF} = 0.

表 6-13. SYSREF Delay Setup

f_{CLKIN}	SYSREF_DELAY_DIV	SYSREFx_DELAY_SCALE	$f_{INTERPOLATOR}$
6.4 GHz < f_{CLKIN} ≤ 12.8GHz	16	0	0.4 to 0.8 GHz
3.2 GHz < f_{CLKIN} ≤ 6.4 GHz	8	0	0.4 to 0.8 GHz
1.6 GHz < f_{CLKIN} ≤ 3.2 GHz	4	0	0.4 to 0.8 GHz
0.8 GHz < f_{CLKIN} ≤1.6 GHz	2	0	0.4 to 0.8 GHz
0.4 GHz < f_{CLKIN} ≤ 0.8 GHz	2	1	0.2 to 0.4 GHz
0.3 GHz < f_{CLKIN} ≤ 0.4 GHz	2	2	0.15 to 0.2 GHz

The maximum delay is equal to the phase interpolator period and there are 4x127 = 508 different delay steps. Use 式 2 to calculate the size of each step.

$$DelayStepSize = 1/(f_{INTERPOLATOR} \times 508) = SYSREF\_DELAY\_DIV/(f_{CLKIN} \times 508) \quad (2)$$

Use 式 3 to calculate the total delay.

$$TotalDelay = DelayStepSize \times StepNumber \quad (3)$$

表 6-14 shows the number of steps for each delay.

表 6-14. Calculation of StepNumber

SYSREFx_DELAY_PHASE	STEPNUMBER
3	127 - SYSREFx_DELAY_I
2	254 - SYSREFx_DELAY_Q

表 6-14. Calculation of StepNumber (続き)

SYSREFx_DELAY_PHASE	STEPNUMBER
0	381 - SYSREFx_DELAY_I
1	508 - SYSREFx_DELAY_Q

The SYSREF_DELAY_BYPASS field selects between the delay generator output and the repeater mode bypass signal. When SYSREF_MODE is set to continuous or pulser mode, TI recommends to set SYSREF_DELAY_BYPASS to generator mode. If SYSREF_MODE is set to repeater mode, TI recommends to set SYSREF_DELAY_BYPASS to bypass mode.

6.3.6.3 SYSREFREQ pins and SYSREFREQ_SPI Field

The SYSREFREQ pins are multipurpose and can be used for SYNC, SYSREF requests, and SYSREF Windowing. These pins can be DC or AC coupled and have dual 50-Ω, single-ended termination with programmable common-mode support.

In addition to these pins, the SYSREFREQ_SPI field can be set to 1 to emulate the same effect as forcing these pins high, simplifying hardware in some cases.

6.3.6.3.1 SYSREFREQ Pins Common-Mode Voltage

The SYSREFREQ_P and SYSREFREQ_N pins can be driven either AC or DC coupled. When driven AC coupled, the common-mode voltage can be adjusted with the SYSREFREQ_VCM bit.

表 6-15. SYSREFREQ Pin Common-Mode Voltage

SYSREFREQ_VCM	COMMON-MODE VOLTAGE
0	1.3V AC-coupled
1	1.1V AC-coupled
2	1.5V AC-coupled
3	No Bias (DC Coupled)

6.3.6.3.2 SYSREFREQ Windowing Feature

The SYSREF windowing can be used to internally calibrate the timing between the SYSREFREQ and CLKIN pins to optimize setup and hold timing and trim out any mismatches between SYSREFREQ and CLKIN paths. This feature requires that the timing from the SYSREFREQ rising edge to the CLKIN rising edge is consistent. The timing from the SYSREFREQ rising edge to the CLKIN rising edges can be tracked with the rb_CLKPOS field. Once the timing to the rising edge of the CLKIN pin is found, then the SYSREFREQ rising edge can be internally adjusted with the SYSREFREQ_DELAY_STEP and SYSREF_DELAY_STEPSIZE fields to optimize setup or hold times.

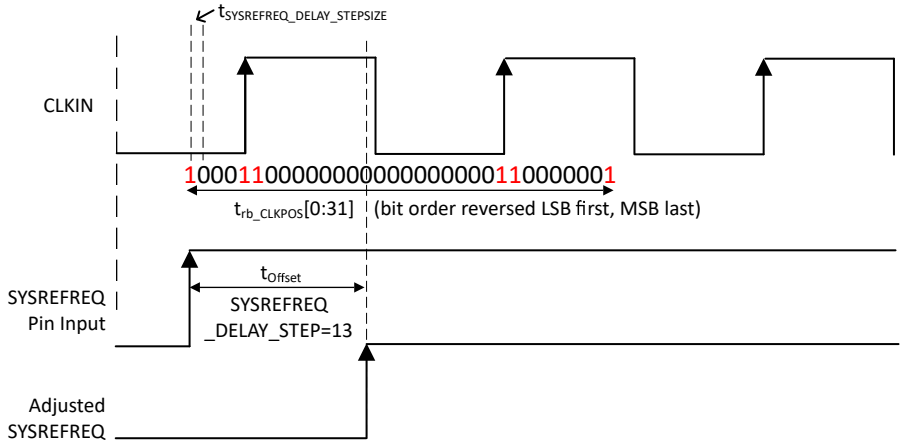


図 6-9. SYSREFREQ Internal Timing Adjustment

6.3.6.3.2.1 General Procedure Flowchart for SYSREF Windowing Operation

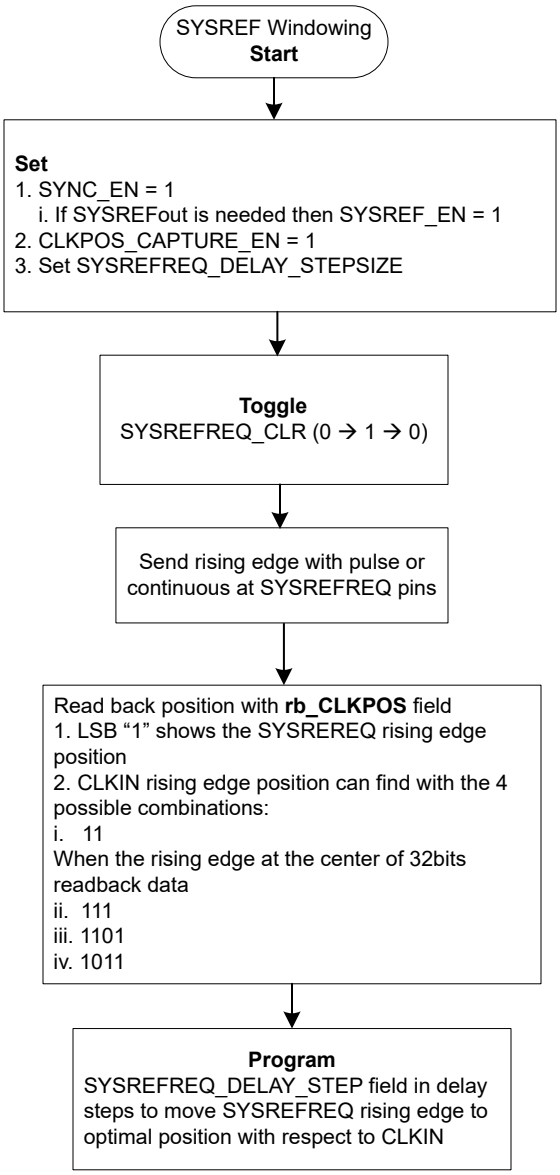


図 6-10. Flowchart for SYSREF Windowing Operation

表 6-16. SYSREFREQ_DELAY_STEPSIZE

INPUT FREQUENCY	RECOMMENDED SYSREFREQ_DELAY_STEPSIZE	DELAY (ps)
1.4GHz < f_{CLKIN} ≤ 2.7 GHz	0	22.25
2.4 GHz < f_{CLKIN} ≤ 4.7 GHz	1	13
3.1 GHz < f_{CLKIN} ≤ 5.7 GHz	2	10.5
f_{CLKIN} ≥ 4.5 GHz	3	7.75

6.3.6.3.2.2 SYSREFREQ Repeater Mode With Delay Gen (Retime)

SYSREF repeater mode with delay enabled is possible with LMX to LMX fanout devices by retiming the SYSREFout at different edge of IQ gen. This retiming can have the delay margin between CLKIN and SYSREFREQ inputs based on SYSREF_DELAY_DIV value.

表 6-17 shows how the total delay margin for the SYSREF windowing relates the various SYSREF settings.

表 6-17. SYSREF Phase Adjust Settings for Retime in Repeater Mode

SYSREF_DELAY_DIV	POSITION CODE SELECTED DURING SYNC	EDGE FOR MAX MARGIN	TOTAL MARGIN IN CLKIN CYCLE	SYSREFx_DELAY_PHASE	SYSREFx_DELAY_Q	SYSREFx_DELAY_I
/2	Before 1**st** edge	I	-1, +1	"11"	0	127
	After 1**st** edge	Qz	-1, +1	"01"	127	0
	After 2**nd** edge	Iz	-1, +1	"00"	0	127
/4	Before 1**st** edge	Qz	-2, +2	"01"	127	0
	After 1**st** edge	Iz	-2, +2	"00"	0	127
	After 2**nd** edge	Q	-2, +2	"10"	127	0
/8	Before 1**st** edge	Qz	-5, +3	"01"	127	0
	After 1**st** edge	Qz	-4, +4	"01"	127	0
	After 2**nd** edge	Qz	-3, +5	"01"	127	0
/16	Before 1**st** edge	I	-9, +7	"11"	0	127
	After 1**st** edge	I	-8, +8	"11"	0	127
	After 2**nd** edge	I	-7, +9	"11"	0	127

Repeater retime mode is required to perform the SYSREF windowing in the initial phase to synchronize the SYSREF_DELAY_DIV in multiple devices. The user can later choose the SYSREFx_DELAY_PHASE, SYSREF_DELAY_Q and SYSREFx_DELAY_I settings for the selected edge for the SYNC.

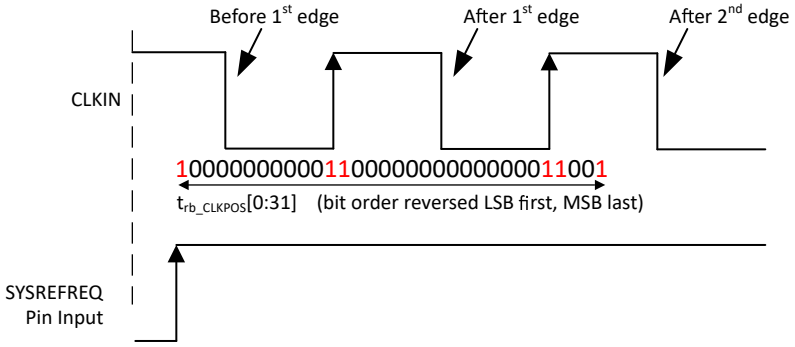


図 6-11. SYSREF Windowing to Select the Edge Position for SYNC

This configuration must set the device in **SYSREF_MODE** R17[1:0] value "2" (Repeater mode) and **SYSREF_DELAY_BYPASS** R72[1:0] value "2" (Delay gen engaged in all modes).

For Glitch Free Output

- Keep the same state for the SYSREFREQ pin when switching from request mode to windowing mode and back to request mode. For example, if the SYSREFREQ pin is high (or low) when windowing mode starts, make sure the pin state is high (or low) again after windowing mode ends before programing CLKPOS_CAPTURE_EN.
- The SYSREFREQ pin must be set low when switching from or to SYNC mode.

Other Pointers With SYSREF Windowing

- The SYSREFREQ pins need to be held high for a minimum time of $3/f_{CLKIN}$ + 1.6ns and only after this time rb_CLKPOS field is valid.

- If the user infers multiple valid SYSREFREQ_DELAY_STEP values from rb_CLKPOS registers to avoid setup-hold violations, choosing the lowest valid SYSREFREQ_DELAY_STEP is recommended to minimize variation over temperature.

If Using SYNC Feature

- Only one SYSREFREQ pin rising edge is permitted per 75 input clock cycles
- SYSREFREQ has to stay high for >6 clock cycles

6.3.7 SYNC Feature

The SYNC feature allows the user to synchronize the CLK_DIV, LOGICLK_DIV, LOGICLK_DIV_PRE, SYSREF_DIV, SYSREF_DIV_PRE, and SYSREF_DELAY_DIV dividers so that the phase offset can be made consistent between power cycles. This allows multiple devices to be synchronized. This synchronization dividers can only be done through the SYSREFREQ pin, not the software.

6.4 Device Functional Modes

表 6-18 shows the different modes for the device. The CLK_MUX field allows the user to configure the device as a buffer, divider, or multiplier. The SYSREF can also be enabled as well for applications that need this feature.

表 6-18. Device Configurations

CLK_MUX	CLK_DIV / CLK_MULT	SYSREF_EN	FUNCTIONAL MODE
1	x	0	Buffer
		1	Buffer w/SYSREF
2	2,3,4,..,8	0	Divider
		1	Divider w/SYSREF
3	2,3,4	0	Multiplier
		1	Multiplier w/SYSREF

7 Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	POWERDOWN	0	RESET
R2	0	0	0	0	0	0	SMCLK_DIV_PRE				SMCLK_EN	0	0	0	1	1
R3	CH3_EN	CH2_EN	CH1_EN	CH0_EN	LOGIC_MUTE_CAL	CH3_MUTE_CAL	CH2_MUTE_CAL	CH1_MUTE_CAL	CH0_MUTE_CAL	0	0	0	0	SMCLK_DIV		
R4	0	0	CLKOUT1_PWR			CLKOUT0_PWR			SYSREFOUT3_EN	SYSREFOUT2_EN	SYSREFOUT1_EN	SYSREFOUT0_EN	CLKOUT3_EN	CLKOUT2_EN	CLKOUT1_EN	CLKOUT0_EN
R5	0	SYSREFOUT2_PWR			SYSREFOUT1_PWR			SYSREFOUT0_PWR			CLKOUT3_PWR			CLKOUT2_PWR		
R6	LOGICLKOUT_EN	SYSREFOUT3_VCM			SYSREFOUT2_VCM			SYSREFOUT1_VCM			SYSREFOUT0_VCM			SYSREFOUT3_PWR		
R7	0	LOGISYSREFOUT_VCM		LOGICLKOUT_VCM		LOGISYSREFOUT_PREDRV_PWR		LOGICLKOUT_PREDRV_PWR		LOGISYSREFOUT_PWR			LOGICLKOUT_PWR			LOGISYSREFOUT_EN
R8	0	0	0	0	0	0	0	LOGICLK_DIV_PRE			1	LOGIC_EN	LOGISYSREFOUT_FMT		LOGICLKOUT_FMT	
R9	SYSREFREQ_VCM		SYNC_EN	LOGICLK_DIV_PD	LOGICLK_DIV_BYPASS	0	LOGICLK_DIV									
R11	rb_CLKPOS															
R12	rb_CLKPOS[31:16]															
R13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SYSREFREQ_DELAY_STEPSIZE	
R14	0	0	0	0	0	0	0	SYNC_MUTE_PD	0	0	0	0	0	CLKPOS_CAPTURE_EN	SYSREFREQ_MODE	SYSREFREQ_LATCH
R15	0	0	0	0	SYSREF_DIV_PRE		1	SYSREF_SP_EN	SYSREF_EN	SYSREFREQ_DELAY_STEP						SYSREFREQ_CLR
R16	SYSREF_PULSE_COUNT				SYSREF_DIV											
R17	0	0	0	0	0	SYSREF0_DELAY_I							SYSREF0_DELAY_PHASE	SYSREF_MODE		
R18	SYSREF1_DELAY_I							SYSREF1_DELAY_PHASE	SYSREF0_DELAY_Q							
R19	SYSREF2_DELAY_I							SYSREF2_DELAY_PHASE	SYSREF1_DELAY_Q							
R20	SYSREF3_DELAY_I							SYSREF3_DELAY_PHASE	SYSREF2_DELAY_Q							
R21	LOGISYSREF_DELAY_I							LOGISYSREF_DELAY_PHASE	SYSREF3_DELAY_Q							
R22	SYSREF1_DELAY_SCALE		SYSREF0_DELAY_SCALE		SYSREF_DELAY_DIV			0	0	LOGISYSREF_DELAY_Q						
R23	EN_TEMPSENSE	1	MUXOUT_EN	0	0	0	0	0	0	MUXOUT_SEL	LOGISYSREF_DELAY_SCALE		SYSREF3_DELAY_SCALE		SYSREF2_DELAY_SCALE	
R24	0	0	0	0	rb_TEMPSENSE											EN_TS_COUNT
R25	0	0	0	0	0	0	1	0	0	CLK_DIV_RST	CLK_DIV (CLK_MULT)			CLK_MUX		
R28	0	0	0	FORCE_VCO	VCO_SEL			0	0	0	0	0	1	0	0	0

R29	0	0	0	0	0	1	0	1	CAPCTRL							
R33	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0
R34	0	0	0	0	0	1	0	0	1	1	0	0	0	1	0	1
R65	0	1	0	0	0	1	0	rb_VCO_SEL					0	0	0	0
R67	0	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1
R72	0	0	0	0	0	0	0	0	0	0	0	0	PULSER_LATCH	SYSREFREQ_SPI	SYSREF_DELAY_BYPASS	
R75	0	0	0	0	0	0	rb_LD		0	0	0	0	0	0	1	1
R79	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
R86	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R90	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

7.1 LMX1204 Registers

表 7-1 lists the memory-mapped registers for the Device registers. All register addresses not listed in 表 7-1 are undocumented addresses and can be considered reserved. Writing to undocumented addresses can prevent the device from working as intended. Unless specifically instructed by TI, do not write to undocumented addresses.

The recommended initial programming sequence starts by writing R0 with RESET = 0x1, followed by writing all registers required for the desired configuration in descending order (largest to smallest address). Registers related to specific features can be skipped if those features are not used, or if desired values do not differ from reset values. Several registers are documented only to allow readback of certain multiplier values, and can be omitted from initial programming or ignored entirely if the multiplier is not used.

表 7-1. LMX1204 Registers

Address	Acronym	Features Requiring This Register	Section
0x0	R0	Powerdown, Reset, Multiplier Mode Calibration	Go
0x2	R2	Multiplier Mode (State Machine Clock)	Go
0x3	R3	Multiplier Mode (State Machine Clock), Output Enables	Go
0x4	R4	Output Enables, CLKOUT Power	Go
0x5	R5	CLKOUT Power, SYSREFOUT Power	Go
0x6	R6	LOGICLK Enable, SYSREFOUT Power/VCM	Go
0x7	R7	LOGICLK and LOGISYSREF	Go
0x8	R8	LOGICLK and LOGISYSREF	Go
0x9	R9	LOGICLK Divider, SYNC, SYSREFREQ	Go
0xB	R11	SYSREFREQ Windowing (readback)	Go
0xC	R12	SYSREFREQ Windowing (readback)	Go
0xD	R13	SYSREFREQ Windowing	Go
0xE	R14	SYSREFREQ Windowing, SYNC, SYSREF	Go
0xF	R15	SYSREFREQ Windowing, SYNC, SYSREF	Go
0x10	R16	SYSREF	Go
0x11	R17	SYSREF, SYSREFOUT Delay	Go
0x12	R18	SYSREFOUT Delay	Go
0x13	R19	SYSREFOUT Delay	Go
0x14	R20	SYSREFOUT Delay	Go
0x15	R21	SYSREFOUT Delay	Go
0x16	R22	SYSREFOUT Delay	Go
0x17	R23	Temperature Sensor, MUXOUT, SYSREFOUT Delay	Go
0x18	R24	Temperature Sensor	Go
0x19	R25	Multiplier Mode, Divider Mode	Go
0x1C	R28	Multiplier Mode (optional, partial assist calibration)	Go
0x1D	R29	Multiplier Mode (optional, partial assist calibration)	Go
0x21	R33	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x22	R34	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x41	R65	Multiplier Mode (read-only, optional, for partial assist calibration)	Go
0x43	R67	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x48	R72	SYSREF	Go
0x4B	R75	Multiplier Mode (read-only, optional, lock detect)	Go
0x4F	R79	LOGICLK Divider (RESERVED, optional, for divider bypass)	Go
0x56	R86	MUXOUT (RESERVED, optional, for tri-state)	Go
0x5A	R90	LOGICLK Divider (RESERVED, optional, for divider bypass)	Go

Complex bit access types are encoded to fit into small table cells. Device Access Type Codes shows the codes that are used for access types in this section.

表 7-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

7.1.1 R0 Register (Offset = 0x0) [Reset = 0x0000]

R0 is shown in 表 7-3.

Return to the Summary Table.

表 7-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0x0000	Reserved (not used).
2	POWERDOWN	R/W	0x0	Sets the device in a low-power state. The states of other registers are maintained.
1	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
0	RESET	R/W	0x0	Soft Reset. Resets the entire logic and registers (equivalent to power-on reset). Self-clearing on next register write.

7.1.2 R2 Register (Offset = 0x2) [Reset = 0x0223]

R2 is shown in 表 7-4.

Return to the Summary Table.

表 7-4. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x00	Reserved (not used).
10	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
9:6	SMCLK_DIV_PRE	R/W	0x8	Sets pre-divider for state machine clock. The state machine clock is divided from CLKIN. The output of the pre-divider must be ≤ 1600 MHz. Values other than those listed below are reserved. 0x2 = ÷2 0x4 = ÷4 0x8 = ÷8
5	SMCLK_EN	R/W	0x1	Enables the state machine clock generator. Only required to calibrate the multiplier, and for multiplier lock detect (including on MUXOUT pin). If the multiplier is not used, or if the multiplier lock detect feature is not used, the state machine clock generator can be disabled to minimize crosstalk.
4:0	RESERVED	R/W	0x03	Reserved. If this register is written, set these bits to 0x03.

7.1.3 R3 Register (Offset = 0x3) [Reset = 0xFF86]

R3 is shown in 表 7-5.

Return to the Summary Table.

表 7-5. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH3_EN	R/W	0x1	Enables CH3 (CLKOUT3, SYSREFOUT3). Setting this bit to 0x0 completely disables all CH3 circuitry, overriding the state of other powerdown/enable bits.
14	CH2_EN	R/W	0x1	Enables CH2 (CLKOUT2, SYSREFOUT2). Setting this bit to 0x0 completely disables all CH2 circuitry, overriding the state of other powerdown/enable bits.
13	CH1_EN	R/W	0x1	Enables CH1 (CLKOUT1, SYSREFOUT1). Setting this bit to 0x0 completely disables all CH1 circuitry, overriding the state of other powerdown/enable bits.
12	CH0_EN	R/W	0x1	Enables CH0 (CLKOUT0, SYSREFOUT0). Setting this bit to 0x0 completely disables all CH0 circuitry, overriding the state of other powerdown/enable bits.
11	LOGIC_MUTE_CAL	R/W	0x1	Mutes LOGIC outputs (LOGICLKOUT, LOGISYSREFOUT) during multiplier calibration.
10	CH3_MUTE_CAL	R/W	0x1	Mutes CH3 (CLKOUT3, SYSREFOUT3) during multiplier calibration.
9	CH2_MUTE_CAL	R/W	0x1	Mutes CH2 (CLKOUT2, SYSREFOUT2) during multiplier calibration.
8	CH1_MUTE_CAL	R/W	0x1	Mutes CH1 (CLKOUT1, SYSREFOUT1) during multiplier calibration.
7	CH0_MUTE_CAL	R/W	0x1	Mutes CH0 (CLKOUT0, SYSREFOUT0) during multiplier calibration.
6:3	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
2:0	SMCLK_DIV	R/W	0x6	Sets state machine clock divider. Further divides the output of the state machine clock pre-divider. Input frequency from SMCLK_DIV_PRE must be ≤ 1600 MHz. Output frequency must be ≤ 30 MHz. Divide value is 2^{SMCLK_DIV}. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = ÷8 0x4 = ÷16 0x5 = ÷32 0x6 = ÷64 0x7 = ÷128

7.1.4 R4 Register (Offset = 0x4) [Reset = 0x360F]

R4 is shown in 表 7-6.

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表 7-6. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:11	CLKOUT1_PWR	R/W	0x6	Sets the output power of CLKOUT1. Larger values correspond to higher output power.
10:8	CLKOUT0_PWR	R/W	0x6	Sets the output power of CLKOUT0. Larger values correspond to higher output power.
7	SYSREFOUT3_EN	R/W	0x0	Enables SYSREFOUT3 output buffer.
6	SYSREFOUT2_EN	R/W	0x0	Enables SYSREFOUT2 output buffer.
5	SYSREFOUT1_EN	R/W	0x0	Enables SYSREFOUT1 output buffer.
4	SYSREFOUT0_EN	R/W	0x0	Enables SYSREFOUT0 output buffer.
3	CLKOUT3_EN	R/W	0x1	Enables CLKOUT3 output buffer.
2	CLKOUT2_EN	R/W	0x1	Enables CLKOUT2 output buffer.
1	CLKOUT1_EN	R/W	0x1	Enables CLKOUT1 output buffer.
0	CLKOUT0_EN	R/W	0x1	Enables CLKOUT0 output buffer.

7.1.5 R5 Register (Offset = 0x5) [Reset = 0x4936]

R5 is shown in 表 7-7.

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表 7-7. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:12	SYSREFOUT2_PWR	R/W	0x4	Sets the output power of SYSREFOUT2. Larger values correspond to higher output power. SYSREFOUT2_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
11:9	SYSREFOUT1_PWR	R/W	0x4	Sets the output power of SYSREFOUT1. Larger values correspond to higher output power. SYSREFOUT1_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
8:6	SYSREFOUT0_PWR	R/W	0x4	Sets the output power of SYSREFOUT0. Larger values correspond to higher output power. SYSREFOUT0_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
5:3	CLKOUT3_PWR	R/W	0x6	Sets the output power of CLKOUT3. Larger values correspond to higher output power.
2:0	CLKOUT2_PWR	R/W	0x6	Sets the output power of CLKOUT2. Larger values correspond to higher output power.

7.1.6 R6 Register (Offset = 0x6) [Reset = 0x36D6]

R6 is shown in 表 7-8.

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表 7-8. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOGICLKOUT_EN	R/W	0x0	Enables the LOGICLKOUT output buffer.
14:12	SYSREFOUT3_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT3. SYSREFOUT3_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
11:9	SYSREFOUT2_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT2. SYSREFOUT2_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
8:6	SYSREFOUT1_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT1. SYSREFOUT1_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
5:3	SYSREFOUT0_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT0. SYSREFOUT0_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
2:0	SYSREFOUT3_PWR	R/W	0x4	Sets the output power of SYSREFOUT3. Larger values correspond to higher output power. SYSREFOUT3_VCM must be set properly to bring the output common-mode voltage within permissible limits.

7.1.7 R7 Register (Offset = 0x7) [Reset = 0x0000]

R7 is shown in 表 7-9.

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表 7-9. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:13	LOGISYSREFOUT_VCM	R/W	0x0	Sets the output common mode of LOGISYSREFOUT in LVDS format. Other output formats (CML, LVPECL) ignore this field. 0x0 = 1.2 V 0x1 = 1.1 V 0x2 = 1.0 V 0x3 = 0.9 V
12:11	LOGICLKOUT_VCM	R/W	0x0	Sets the output common mode of LOGICLKOUT in LVDS format. Other output formats (CML, LVPECL) ignore this field. 0x0 = 1.2 V 0x1 = 1.1 V 0x2 = 1.0 V 0x3 = 0.9 V
10:9	LOGISYSREFOUT_PREDRV_PWR	R/W	0x0	Sets the output power of the LOGISYSREFOUT pre-driver. Larger values correspond to higher output power. Default value is sufficient for typical use.
8:7	LOGICLKOUT_PREDRV_PWR	R/W	0x0	Sets the output power of the LOGICLKOUT pre-driver. Larger values correspond to higher output power. Default value is sufficient for typical use.
6:4	LOGISYSREFOUT_PWR	R/W	0x0	Sets the output power of LOGISYSREFOUT in CML format. Larger values correspond to higher output power. Other output formats (LVDS, LVPECL) ignore this field. Valid range is 0x0 to 0x3.
3:1	LOGICLKOUT_PWR	R/W	0x0	Sets the output power of LOGICLKOUT in CML format. Larger values correspond to higher output power. Other output formats (LVDS, LVPECL) ignore this field. Valid range is 0x0 to 0x3.
0	LOGISYSREFOUT_EN	R/W	0x0	Enables LOGISYSREFOUT output buffer.

7.1.8 R8 Register (Offset = 0x8) [Reset = 0x0120]

R8 is shown in 表 7-10.

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表 7-10. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0x00	Reserved (not used).
8:6	LOGICLK_DIV_PRE	R/W	0x4	Sets pre-divider value for logic clock divider. Output of the pre-divider must be ≤ 3.2 GHz. Values other than those listed below are reserved. 0x1 = ÷1 0x2 = ÷2 0x4 = ÷4
5	RESERVED	R/W	0x1	Reserved. If this register is written, set this bit to 0x1.
4	LOGIC_EN	R/W	0x0	Enables LOGICLK subsystem (LOGICLKOUT, LOGISYSREFOUT). Setting this bit to 0x0 completely disables all LOGICLKOUT and LOGISYSREFOUT circuitry, overriding the state of other powerdown/enable bits.
3:2	LOGISYSREFOUT_FMT	R/W	0x0	Selects the output driver format of the LOGISYSREFOUT output. LVDS allows for common mode control with LOGISYSREFOUT_VCM field. CML allows for output power control with LOGISYSREFOUT_PWR field. CML format requires external 50-Ω pull-up resistors. LVPECL requires external 220-Ω emitter resistors to GND when AC-coupled, or 50-Ω to VCC - 2 V (0.5 V) when DC-coupled. See also R7 Register. 0x0 = LVDS 0x1 = LVPECL 0x2 = CML 0x3 = Reserved
1:0	LOGICLKOUT_FMT	R/W	0x0	Selects the output driver format of the LOGICLKOUT output. LVDS allows for common mode control with LOGICLKOUT_VCM field. CML allows for output power control with LOGICLKOUT_PWR field. CML format requires external 50-Ω pull-up resistors. LVPECL requires external 220-Ω emitter resistors to GND when AC-coupled, or 50-Ω to VCC - 2 V (0.5 V) when DC-coupled. See also R7 Register. 0x0 = LVDS 0x1 = LVPECL 0x2 = CML 0x3 = Reserved

7.1.9 R9 Register (Offset = 0x9) [Reset = 0x001E]

R9 is shown in 表 7-11.

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表 7-11. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSREFREQ_VCM	R/W	0x0	Sets the internal DC Bias for the SYSREFREQ pins. Bias must be enabled for AC-coupled inputs; but can be enabled and overdriven, or disabled, for DC-coupled inputs. SYSREFREQ DC pin voltage must be in the range of 0.7 V to VCC, including minimum and maximum signal swing. 0x0 = 1.3 V 0x1 = 1.1 V 0x2 = 1.5 V 0x3 = Disabled (DC-coupled only)
13	SYNC_EN	R/W	0x0	Enables synchronization path for the dividers and allows the clock position capture circuitry to be enabled. Used for multi-device synchronization. Redundant if SYSREF_EN = 0x1.
12	LOGICLK_DIV_PD	R/W	0x0	Disables the LOGICLK divider. LOGICLK pre-divider remains enabled. Used to reduce current consumption when bypassing the LOGICLK divider. When LOGICLK_DIV_PRE = 0x2 or 0x4, this bit must be set to 0x0.
11	LOGICLK_DIV_BYPASS	R/W	0x0	Bypasses the LOGICLK divider, deriving LOGICLK output directly from the pre-divider. Used to achieve divide-by-1 when LOGICLK_DIV_PRE = 0x1. When LOGICLK_DIV_PRE = 0x2 or 0x4, this bit must be set to 0x0. When LOGICLK_DIV_BYPASS = 0x1, set R90[6:5] = 0x3 and R79[9:8] = 0x0. When LOGICLK_DIV_BYPASS = 0x0, if R90[6:5] = 0x3 due to previous user setting, set R90[6:5] = 0x0. When LOGICLK_DIV_BYPASS = 0x1, the LOGICLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation. See also R79 Register and R90 Register.
10	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
9:0	LOGICLK_DIV	R/W	0x1E	Sets LOGICLK divider value. Maximum input frequency from LOGICLK_DIV_PRE must be ≤ 3200 MHz. The maximum LOGICLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation. 0x0: Reserved 0x1: Reserved 0x2: ÷2 0x3: ÷3 ... 0x1FF: ÷1023

7.1.10 R11 Register (Offset = 0xB) [Reset = 0xFFFF]

R11 is shown in 表 7-12.

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表 7-12. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_CLKPOS[15:0]	R	0xFFFF	Stores a snapshot of the CLKIN signal rising edge positions relative to a SYSREFREQ rising edge, with the snapshot starting from the LSB and ending at the MSB. Each bit represents a sample of the CLKIN signal, separated by a delay determined by the SYSREFREQ_DELAY_STEPSIZE field. The first and last bits of rb_CLKPOS are always set, indicating uncertainty at the capture window boundary conditions. CLKIN rising edges are represented by every sequence of two set bits from LSB to MSB, including bits at the boundary conditions. The position of the CLKIN rising edges in the snapshot, along with the CLKIN signal period and the delay step size, can be used to compute the value of SYSREFREQ_DELAY_STEP which maximizes setup and hold times for SYNC signals on the SYSREFREQ pins. See also R12 Register, R13 Register, R14 Register, and R15 Register.

7.1.11 R12 Register (Offset = 0xC) [Reset = 0xFFFF]

R12 is shown in 表 7-13.

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表 7-13. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_CLKPOS[31:16]	R	0xFFFF	MSBs of rb_CLKPOS field. See also R11 Register, R13 Register, R14 Register, and R15 Register.

7.1.12 R13 Register (Offset = 0xD) [Reset = 0x0003]

R13 is shown in 表 7-14.

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表 7-14. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0x0000	Reserved (not used).
1:0	SYSREFREQ_DELAY_STEPSIZE	R/W	0x3	Sets the step size of the delay element used in the SYSREFREQ path, both for SYSREFREQ input delay and for clock position captures. The recommended frequency range for each step size creates the maximum number of usable steps for a given CLKIN frequency. The ranges include some overlap to account for process and temperature variations. If the CLKIN frequency is covered by an overlapping span, larger delay step sizes improve the likelihood of detecting a CLKIN rising edge during a clock position capture. However, since larger values include more delay steps, larger step sizes have greater total delay variation across PVT relative to smaller step sizes. See also R11 Register, R12 Register, R14 Register, and R15 Register. 0x0 = 28 ps (1.4 GHz to 2.7 GHz) 0x1 = 15 ps (2.4 GHz to 4.7 GHz) 0x2 = 11 ps (3.1 GHz to 5.7 GHz) 0x3 = 8 ps (4.5 GHz to 12.8 GHz)

7.1.13 R14 Register (Offset = 0xE) [Reset = 0x0002]

R14 is shown in 表 7-15.

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表 7-15. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
8	SYNC_MUTE_PD	R/W	0x0	Removes the mute condition on the SYSREFOUT and LOGISYSREFOUT pins during SYNC mode (SYSREFREQ_MODE = 0x0). Since the SYNC operation also resets the SYSREF dividers, the mute condition is usually desirable, and this bit can be left at the default value.
7:3	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
2	CLKPOS_CAPTURE_EN	R/W	0x0	Enables the windowing circuit which captures the clock position in the rb_CLKPOS registers with respect to a SYSREF edge. The windowing circuit must be cleared by toggling SYSREFREQ_CLR high then low before a clock position capture. The first rising edge on the SYSREFREQ pins after clearing the windowing circuit triggers the capture. The capture circuitry greatly increases supply current, and does not need to be enabled to delay the SYSREFREQ signal in SYNC or SYSREF modes. Once the desired value of SYSREFREQ_DELAY_STEP is determined, set this bit to 0x0 to minimize current consumption. If SYNC_EN = 0x0 and SYSREF_EN = 0x0, the value of this bit is ignored, and the windowing circuit is disabled. See also R11 Register, R12 Register, R13 Register, and R15 Register.
1	SYSREFREQ_MODE	R/W	0x1	Selects the function of the SYSREFREQ pins. 0x0 = SYNC Pin 0x1 = SYSREFREQ Pin
0	SYSREFREQ_LATCH	R/W	0x0	Latches the internal SYSREFREQ state to logic high on the first rising edge of the SYSREFREQ pins. This latch can be cleared by setting SYSREFREQ_CLR to 0x1, or bypassed by setting SYSREFREQ_LATCH to 0x0. See also R15 Register.

7.1.14 R15 Register (Offset = 0xF) [Reset = 0x0901]

R15 is shown in 表 7-16.

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表 7-16. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved (not used).
11:10	SYSREF_DIV_PRE	R/W	0x2	Sets the SYSREF pre-divider. Maximum output frequency must be ≤ 3.2 GHz. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = Reserved
9:8	RESERVED	R/W	0x1	Reserved. If this register is written, set these bits to 0x1.
7	SYSREF_EN	R/W	0x0	Enables SYSREF subsystem (and SYNC subsystem when SYSREFREQ_MODE = 0x0). Setting this bit to 0x0 completely disables all SYNC, SYSREF, and clock position capture circuitry, overriding the state of other powerdown/enable bits *except* SYNC_EN. If SYNC_EN = 0x1, the SYNC path and clock position capture circuitry are still enabled, regardless of the state of SYSREF_EN.
6:1	SYSREFREQ_DELAY_STEP	R/W	0x0	Sets the delay line step for the external SYSREFREQ signal. Each delay line step delays the SYSREFREQ signal by an amount equal to SYSREFREQ_DELAY_STEP x SYSREFREQ_DELAY_STEPSIZE. In SYNC mode, the value for this field can be determined based on the rb_CLKPOS value to satisfy the internal setup and hold time of the SYNC signal with respect to the CLKIN signal. In SYSREF Repeater Mode, the value for this field can be used as a coarse global delay. Values greater than 0x3F are invalid. Since larger values include more delay steps, larger values have greater total step size variation across PVT relative to smaller values. Refer to the data sheet or the device TICS Pro profile for detailed description of the delay step computation procedure. See also R11 Register, R12 Register, R13 Register, and R14 Register.
0	SYSREFREQ_CLR	R/W	0x1	Clears SYSREFREQ_LATCH, which resets the SYSREFREQ input latch, the internal divider synchronization retimers, and the clock position capture flip-flops comprising rb_CLKPOS. When set, holds the internal SYSREFREQ signal low in all modes except SYSREF repeater mode, overriding the state of SYSREFREQ_SPI. This bit must be set and cleared once before the SYNC or clock position capture operations are performed. See also R14 Register.

7.1.15 R16 Register (Offset = 0x10) [Reset = 0x1003]

R16 is shown in 表 7-17.

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表 7-17. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	SYSREF_PULSE_COUNT	R/W	0x1	Programs the number of pulses generated in pulser mode. The pulser is a counter gating the SYSREF divider; consequently, the pulse duration and frequency are equal to the duty cycle and frequency of the SYSREF divider output, respectively. 0x0: Reserved 0x1: 1 pulse 0x2: 2 pulses ... 0xF: 15 pulses
11:0	SYSREF_DIV	R/W	0x3	Sets the SYSREF divider. Maximum input frequency from SYSREF_DIV_PRE must be ≤ 3200 MHz. Maximum output frequency must be ≤ 100 MHz. Odd divides (with duty cycle != 50%) are only allowed when the delay generators are bypassed. See also R72 Register. 0x0: Reserved 0x1: Reserved 0x2: ÷2 0x3: ÷3 ... 0xFFF: ÷4095

7.1.16 R17 Register (Offset = 0x11) [Reset = 0x07F0]

R17 is shown in 表 7-18.

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表 7-18. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved (not used).
10:4	SYSREFOUT0_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DELAY_I + SYSREFOUT0_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register.
3:2	SYSREFOUT0_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT0 delay generator retimer. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
1:0	SYSREF_MODE	R/W	0x0	Controls how the SYSREF signal is generated or repeated. See also SYSREF_DELAY_BYPASS in R79 Register for additional configuration options. 0x0 = Continuous (Generator Mode) 0x1 = Pulser (Generator Mode) 0x2 = Repeater (Repeater Mode) 0x3 = Reserved

7.1.17 R18 Register (Offset = 0x12) [Reset = 0xFE00]

R18 is shown in 表 7-19.

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表 7-19. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT1_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT1 delay generator. Must satisfy SYSREFOUT1_DELAY_I + SYSREFOUT1_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R19 Register and R22 Register.
8:7	SYSREFOUT1_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT1 delay generator retimer. Consult the data sheet for configuration instructions. See also R19 Register and R22 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT0_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DELAY_I + SYSREFOUT0_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R17 Register and R22 Register.

7.1.18 R19 Register (Offset = 0x13) [Reset = 0xFE00]

R19 is shown in 表 7-20.

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表 7-20. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT2_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT2 delay generator. Must satisfy SYSREFOUT2_DELAY_I + SYSREFOUT2_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register.
8:7	SYSREFOUT2_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT2 delay generator retimer. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT1_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT1 delay generator. Must satisfy SYSREFOUT1_DELAY_I + SYSREFOUT1_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register.

7.1.19 R20 Register (Offset = 0x14) [Reset = 0xFE00]

R20 is shown in 表 7-21.

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表 7-21. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT3_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT3 delay generator. Must satisfy SYSREFOUT3_DELAY_I + SYSREFOUT3_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R21 Register and R23 Register.
8:7	SYSREFOUT3_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT3 delay generator retimer. Consult the data sheet for configuration instructions. See also R21 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT2_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT2 delay generator. Must satisfy SYSREFOUT2_DELAY_I + SYSREFOUT2_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R19 Register and R23 Register.

7.1.20 R21 Register (Offset = 0x15) [Reset = 0xFE00]

R21 is shown in 表 7-22.

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表 7-22. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	LOGISYSREFOUT_DELAY_I	R/W	0x7F	Sets the delay step for the LOGISYSREFOUT delay generator. Must satisfy LOGISYSREFOUT_DELAY_I + LOGISYSREFOUT_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R22 Register and R23 Register.
8:7	LOGISYSREFOUT_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the LOGISYSREFOUT delay generator retimer. Consult the data sheet for configuration instructions. See also R22 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT3_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT3 delay generator. Must satisfy SYSREFOUT3_DELAY_I + SYSREFOUT3_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register.

7.1.21 R22 Register (Offset = 0x16) [Reset = 0x0800]

R22 is shown in 表 7-23.

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表 7-23. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSREFOUT1_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT1 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R18 Register and R19 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
13:12	SYSREFOUT0_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT0 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R17 Register and R18 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
11:9	SYSREF_DELAY_DIV	R/W	0x4	Sets the delay generator clock division, determining $f_{INTERPOLATOR}$ and the delay generator resolution. Values other than those listed below are reserved. See also R23 Register. 0x0 = ÷2 (≤ 1.6 GHz) 0x1 = ÷4 (1.6 GHz to 3.2 GHz) 0x2 = ÷8 (3.2 GHz to 6.4 GHz) 0x4 = ÷16 (6.4 GHz to 12.8 GHz)
8:7	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
6:0	LOGISYSREFOUT_DELAY_Q	R/W	0x0	Sets the delay step for the LOGISYSREFOUT delay generator. Must satisfy LOGISYSREFOUT_DELAY_I + LOGISYSREFOUT_DELAY_Q = 0x7F. See also R21 Register and R23 Register.

7.1.22 R23 Register (Offset = 0x17) [Reset = 0x4000]

R23 is shown in 表 7-24.

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表 7-24. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EN_TEMPSENSE	R/W	0x0	Enables the on-die temperature sensor. Temperature sensor counter (EN_TS_COUNT) must also be enabled for readback. See also R24 Register.
14	RESERVED	R/W	0x1	Reserved. If this register is written, set this bit to 0x1.
13	MUXOUT_EN	R/W	0x0	Enables or tri-states the MUXOUT pin driver. See also R86 Register. 0x0 = Tri-State 0x1 = Push-Pull
12:7	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
6	MUXOUT_SEL	R/W	0x0	Selects MUXOUT pin function. 0x0 = Lock Detect (Multiplier Only) 0x1 = SDO (SPI readback)
5:4	LOGISYSREFOUT_DELAY_SCALE	R/W	0x0	Sets the frequency range of the LOGISYSREFOUT delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R21 Register and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
3:2	SYSREFOUT3_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT3 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R20 Register, R21 Register, and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
1:0	SYSREFOUT2_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT2 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R19 Register, R20 Register, and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved

7.1.23 R24 Register (Offset = 0x18) [Reset = 0x0FFE]

R24 is shown in 表 7-25.

Return to the Summary Table.

表 7-25. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:12	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
11:1	rb_TEMPSENSE	R	0x7FF	Output of on-die temperature sensor. Readback code can be converted to junction temperature (in °C) according to the following equation: T_J = 0.65 * rb_TEMPSENSE - 351
0	EN_TS_COUNT	R/W	0x0	Enables temperature sensor counter. Temperature sensor (EN_TEMPSENSE) must be enabled for accurate data. See also R23 Register.

7.1.24 R25 Register (Offset = 0x19) [Reset = 0x0211]

R25 is shown in 表 7-26.

Return to the Summary Table.

表 7-26. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	0x004	Reserved. If this register is written, set these bits to 0x004.
6	CLK_DIV_RST	R/W	0x0	Resets the main clock divider. If the clock divider value is changed during operation, set this bit high then low after setting the new divider value. Synchronizing the device with the SYSREFREQ pins in SYSREFREQ_MODE = 0x0 and SYNC_EN = 0x1 also resets the main clock divider. This bit has no effect when outside of Divider Mode.
5:3	CLK_DIV CLK_MULT	R/W	0x2	CLK_DIV and CLK_MULT are aliases for the same field. When CLK_MUX = 0x2 (Divider Mode), sets the clock divider equal to CLK_DIV + 1. Valid range is 0x1 to 0x7. Setting CLK_DIV = 0x0 disables the main clock divider and reverts to buffer mode. When CLK_MUX = 0x3 (Multiplier Mode), sets the multiplier equal to CLK_MULT. Valid range is 0x1 to 0x4. Setting CLK_MULT to an invalid value disables the multiplier and reverts to buffer mode. When CLK_MUX = 0x1 (buffer mode), this field is ignored.
2:0	CLK_MUX	R/W	0x1	Selects the function of the device. Multiplier Mode requires writing several other registers (R33, R34, and R67) to values differing from POR defaults, as well as configuring the state machine clock (R2 and R3), before multiplier calibration. Writing any value to R0 (as long as POWERDOWN = 0x0 and RESET = 0x0) triggers a multiplier calibration. Values other than those listed below are reserved. 0x1 = Buffer Mode 0x2 = Divider Mode 0x3 = Multiplier Mode

7.1.25 R28 Register (Offset = 0x1C) [Reset = 0x0A08]

R28 is shown in 表 7-27.

Return to the Summary Table.

表 7-27. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved (not used).
12	FORCE_VCO	R/W	0x0	Forces the PLL VCO of the multiplier to the value selected by VCO_SEL. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.
11:9	VCO_SEL	R/W	0x5	User specified start VCO for multiplier PLL. When FORCE_VCO = 0x0, multiplier calibration starts from the VCO set by this field. When FORCE_VCO = 0x1, this field sets the VCO core used by the multiplier. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.
8:0	RESERVED	R/W	0x008	Reserved. If this register is written, set these bits to 0x008.

7.1.26 R29 Register (Offset = 0x1D) [Reset = 0x05FF]

R29 is shown in 表 7-28.

Return to the Summary Table.

表 7-28. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved (not used).
12:8	RESERVED	R/W	0x5	Reserved. If this register is written, set these bits to 0x05.
7:0	CAPCTRL	R/W	0xFF	Sets the starting value for the VCO tuning capacitance during multiplier calibration. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.

7.1.27 R33 Register (Offset = 0x21) [Reset = 0x7777]

R33 is shown in 表 7-29.

Return to the Summary Table.

表 7-29. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x7777	Reserved. If the Multiplier Mode is used, set to 0x5666 before calibration. Otherwise, writing this register can be skipped.

7.1.28 R34 Register (Offset = 0x22) [Reset = 0x0000]

R34 is shown in 表 7-30.

Return to the Summary Table.

表 7-30. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:0	RESERVED	R/W	0x0000	Reserved. If the Multiplier Mode is used, set to 0x04C5 before calibration. Otherwise, writing this register can be skipped.

7.1.29 R65 Register (Offset = 0x41) [Reset = 0x45F0]

R65 is shown in 表 7-31.

Return to the Summary Table.

表 7-31. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x22	Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set these bits to 0x22. Readback can differ from default and written values.
8:4	rb_VCO_SEL	R	0x1F	Readback PLL VCO of the multiplier core selection. Can be optionally used in conjunction with VCO_SEL and FORCE_VCO fields to improve calibration time. 0xF = VCO5 0x17 = VCO4 0x1B = VCO3 0x1D = VCO2 0x1E = VCO1
3:0	RESERVED	R/W	0x0	Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set these bits to 0x0.

7.1.30 R67 Register (Offset = 0x43) [Reset = 0x50C8]

R67 is shown in 表 7-32.

Return to the Summary Table.

表 7-32. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x50C8	Reserved. If the Multiplier Mode is used, set to 0x51CB before calibration. Otherwise, writing this register can be skipped.

7.1.31 R72 Register (Offset = 0x48) [Reset = 0x0000]

R72 is shown in 表 7-33.

Return to the Summary Table.

表 7-33. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:4	RESERVED	R/W	0x000	Reserved. Set to 0x000.
3	PULSER_LATCH	R/W	0x0	Latches the pulser input when programmed to 0x1. When this bit is set, external signals on SYSREFREQ pins in pulser mode (SYSREF_MODE = 0x1) can not trigger the pulser more than once, until this bit is cleared. This bit is provided to enable changing SYSREF_MODE in repeater mode without risk of accidentally triggering the pulser.
2	SYSREFREQ_SPI	R/W	0x0	Trigger SYSREFREQ using SPI. Setting this bit emulates the behavior of a logic HIGH at SYSREFREQ pins. External signals on SYSREFREQ pins are ignored while this bit is set.
1:0	SYSREF_DELAY_BYPASS	R/W	0x0	Option to bypass delay generator retiming. Under normal circumstances (SYSREF_DELAY_BYPASS = 0) the delay generator is engaged for continuous or pulser modes (Generator Modes), and bypassed in Repeater Mode. Generally this configuration is desirable: the delay generators rely on a signal generated by the SYSREF_DELAY_DIV from the CLKIN frequency, so the Generator Mode SYSREF signal is always well-aligned to the delay generator; in repeater mode, external signal sources can typically utilize a different delay mechanism. In certain cases, bypassing the delay generator retiming in Generator Mode by setting SYSREF_DELAY_BYPASS = 0x1 can substantially reduce the device current consumption if the SYSREF delay can be compensated at the JESD receiver. In other cases, retiming the SYSREFREQ signal to the delay generators by setting SYSREF_DELAY_BYPASS = 0x2 can improve the accuracy of the SYSREF output phase with respect to the CLKIN phase, or can vary the delay of individual outputs independently, as long as coherent phase relationship exists between the interpolator divider phase and the SYSREFREQ phase. 0x0 = Engage in Generator Mode, Bypass in Repeater Mode 0x1 = Bypass in All Modes 0x2 = Engage in All Modes 0x3 = Reserved

7.1.32 R75 Register (Offset = 0x4B) [Reset = 0xE716]

R75 is shown in 表 7-34.

Return to the Summary Table.

表 7-34. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0x39	Read-only. Writes to these bits are ignored. Readback can differ from default values.
9:8	rb_LD	R	0x3	Multiplier PLL Lock Detect. Read-only. Field value has no meaning if device is not in Multiplier Mode. 0x0 = Unlocked (VTUNE low) 0x1 = Reserved 0x2 = Locked 0x3 = Unlocked (VTUNE high)
7:4	RESERVED	R	0x1	Read-only. Writes to these bits are ignored. Readback can differ from default values.
3:0	RESERVED	R/W	0x6	Reserved. Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set to 0x6.

7.1.33 R79 Register (Offset = 0x4F) [Reset = 0x0104]

R79 is shown in 表 7-35.

Return to the Summary Table.

表 7-35. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:0	RESERVED	R/W	0x0104	Reserved. Set to 0x0104 immediately after setting LOGICLK_DIV_BYPASS = 0x1; R90 must also be written immediately afterward. If LOGICLK_DIV_BYPASS is not used or set to 0x0, this register does not need to be written and can be skipped. See also R90 Register.

7.1.34 R86 Register (Offset = 0x56) [Reset = 0x0000]

R86 is shown in 表 7-36.

Return to the Summary Table.

表 7-36. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x0000	Reserved. This register must be set to 0x0004 to allow MUXOUT_EN to tri-state the MUXOUT pin after SPI readback. If SPI readback is not required, or if tri-state is not required on the MUXOUT pin, writing this register can be skipped, forcing MUXOUT_EN to 0x1 (push-pull mode).

7.1.35 R90 Register (Offset = 0x5A) [Reset = 0x0000]

R90 is shown in 表 7-37.

Return to the Summary Table.

表 7-37. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x00	Reserved (not used).
15:0	RESERVED	R/W	0x00	Reserved. Set to 0x60 immediately after setting LOGICLK_DIV_BYPASS = 0x1 and setting R79 = 0x0104. If LOGICLK_DIV_BYPASS is not used or left at the default value, this register does not need to be written and can be skipped. However, if transitioning from LOGICLK_DIV_BYPASS = 0x1 to 0x0, this register must be re-written to 0x00. See also R79 Register.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 SYSREFREQ Input Configuration

The SYSREFREQ pins support single-ended or differential input in AC or DC coupling mode. The SYSREFREQ pins have an internal 50-Ω termination with capacitive ground, which acts as 100-Ω differential.

図 8-1 shows the generic SYSREFREQ input circuit recommendation to support all AC/DC, single-ended or differential inputs. Some of the discrete components in 図 8-1 are just placeholder for individual input signal (single-ended or differential input) and AC or DC coupled input.

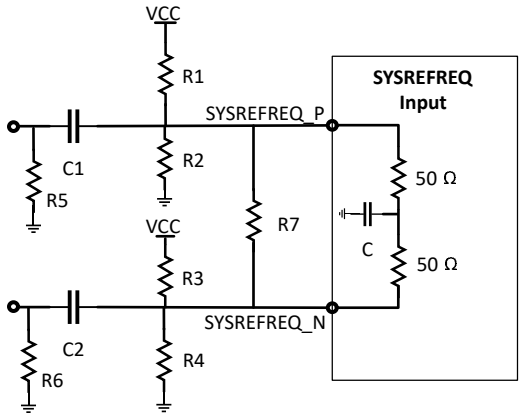

図 8-1. SYSREFREQ Input Circuit Recommendations

The following figures show the individual circuit diagram for each configurations:

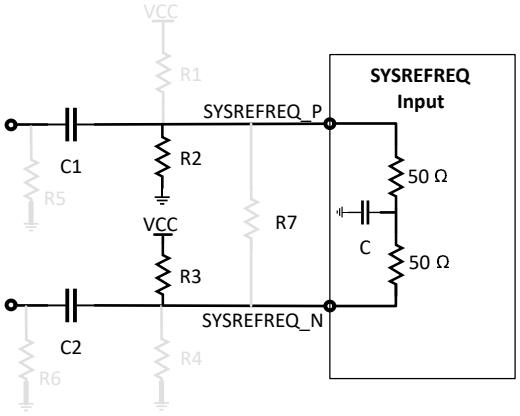

図 8-2. AC-Coupled Differential Input

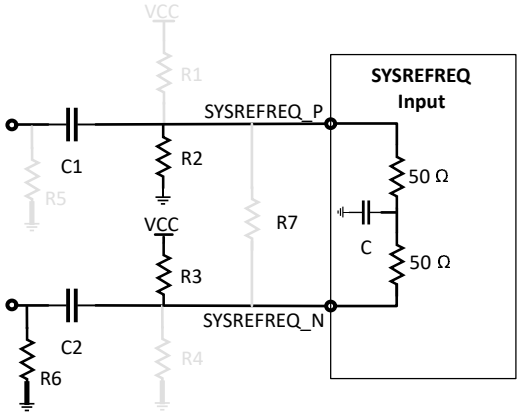

図 8-3. AC-Coupled, Single-Ended Input

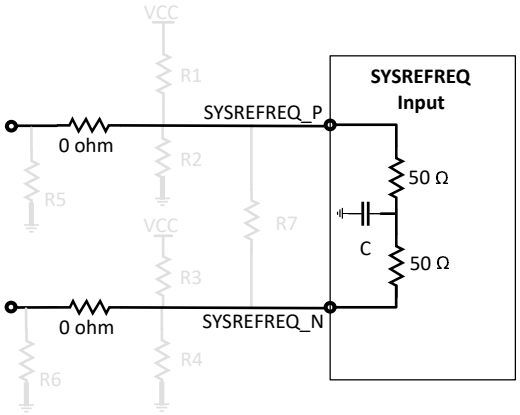

図 8-4. DC-Coupled Differential Input

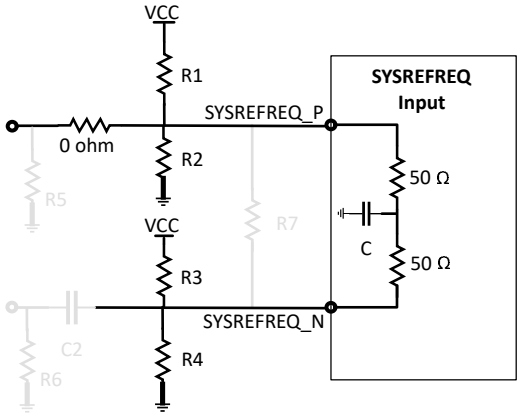

図 8-5. DC-Coupled, Single-Ended Input

1. AC coupled differential and single-ended input configurations required the resistor terminations (R2 and R3) to create the VCM at each pin and resistor values must select to maintain greater than 150-mV potential difference between pin P and pin N.
   a. As an example, to create the VCM of 1.5 V at pin P and 1.65 V at pin N, with the 2.5 V VCC, set R3 = 550 Ω and R2 = 1 kΩ
   b. For single-ended input configuration, place R6 = 50 Ω to avoid any reflection at complementary input pin.
2. DC coupled differential and single-ended input configuration required to have the source common-mode voltage matched with the device input common mode specifications.
   a. For single-ended input configuration, keep the R1, R2, R3 and R4 resistors. This method creates the same common-mode voltage at both pins, and the resistive dividers create 75 Ω at pin P and 50 Ω Thevenin's equivalent at pin N.
   b. As an example, to have the common-mode voltage of 1.35 V at each pin, set the resistive divider components values to R1 = 130 Ω, R2 = 165 Ω, R3 = 86.6 Ω and R4 = 110 Ω with the 2.5V VCC.

8.1.2 Reducing SYSREF Common Mode Voltages

For DC coupled SYSREF applications, some data converters can require a lower common voltage for the SYSREF outputs than the output can support. For these applications, a resistive divider can be used to reduce the common mode voltage. However, when a path to ground is there, the loading inherently reduces the common mode voltage. For a few test cases, the common mode voltage is measured as shown in.表 8-1. Note that this table is for the SYSREFOUTx pins, not the LOGISYSREFout pins.

表 8-1. Impact of Load to GND (Both Pins) on Single-Ended V_{OD} and V_{CM} for SYSREFOUTx_PWR=SYSREFOUTx_VCM=7

Load to GND	\V_{OD}	V_{CM}	VOL
50-Ω	0.72	0.79	0.43
78-Ω	0.86	0.99	0.56
100-Ω	0.96	1.07	0.59
215-Ω	1.13	1.33	0.76

Once the load as seen by the SYSREFOUTx pins is known, the V_{OD} and V_{CM} voltage at those pins can be known. From this point, a resistive divider can be used to create the desired V_{OD} and V_{CM} voltages as shown in 図 8-6 and 図 8-7.

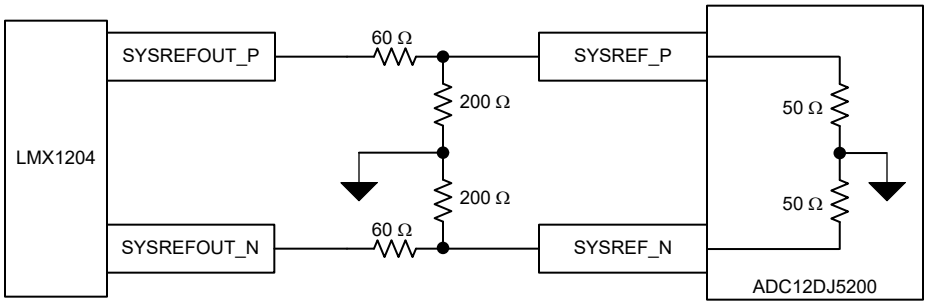

図 8-6. Reducing V_{CM} With Resistive Dividers (Case 1)

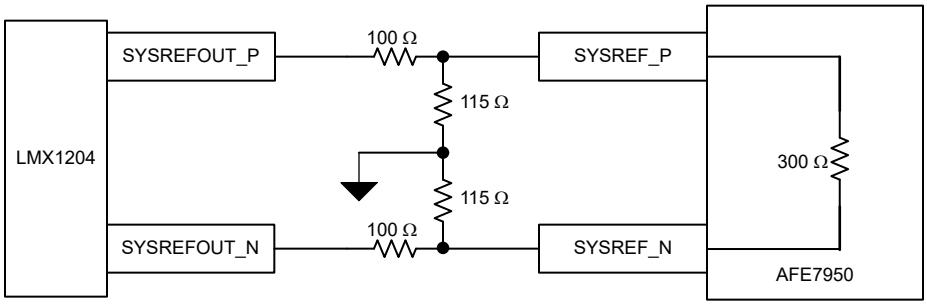

図 8-7. Reducing V_{CM} With Resistive Dividers (Case 2)

These examples lead to the calculations in 表 8-2. Note that the resistive divider reduces the V_{OD}, V_{CM}, and ΔV_{CM} (typical variation in V_{CM}).

表 8-2. Calculated Voltage Values

Where Measured	Parameter	ADC12DJ5200	AFE7950
At LMX1204	R_{Load} (Ω)	100	215
	V_{OD} (V)	0.96	1.13
	V_{CM}	1.065	1.328
	ΔV_{CM}	0.2	0.2
External Resistors	R1(Ω)	60	100
	R2 (Ω)	200	115
At Data Converter	R3 (Ω)	50	None
	Rp (Ω)	None	300
	R2 || R3 (Ω)	40	None
	2R2 || Rp(Ω)	200	130.1887
	VOD Ratio	0.4	0.394286
	VCM Ratio	0.4	0.534884
Critical Voltages at Data Converter	V_{ID} (V)	0.384	0.445543
	V_{CM} (V)	0.426	0.710326
	ΔV_{CM} (V)	0.08	0.106977

8.1.3 Current Consumption

The current consumption varies as a function of the setup condition. By adding up all the block currents shown in 表 8-3, a reasonable estimate of the current for any setup condition can be obtained.

表 8-3. Current Consumption per Block

BLOCK		CONDITION (s)		CURRENT (mA)
Device Core		CLK_MUX = Buffer Mode		294
		CLK_MUX = Divide Mode		260
		CLK_MUX = Multiply Mode	SMCLK_EN=0	540
			SMCLK_EN=1	560
SYSREF SYNC Windowing	Core	SYSREF_EN=1		80
	Delay Generator	Generator Mode (SYSREF_MODE=0,1)		53
		Repeater Mode (SYSREF_MODE=2)		40
	Windowing Circuitry	Windowing Circuitry (CLKPOS_CAPTURE_EN=1)	SYSREF_MODE=0,1	113
			SYSREF_MODE=2	0
	SYSREF Pulser	SYSREF_MODE=1		7
CLKOUT (Per active clock channel)	Core	SYSREF_EN=0		25
		SYSREF_EN = 1	Delay Not Used	30
			Delay Used	40
	Output Buffer	CHx_EN = CLKOUTx_EN=1		4+6*CLKOUTx_PWR
SYSREFOUT	Core	SYSREFOUT_EN = CHx_EN = 1		74 + SYSREFOUTx_PWR*5
	Output Buffer	SYSREFOUT_EN = CHx_EN = 1 (SYSREFOUTx_PWR and SYSREFOUTx_VCM can interact which makes the output buffer current lower than the formula predicts in some cases)		2*SYSREFOUTx_PWR + 2*SYSREFOUTx_VCM
LOGICLKOUT	Core	LOGIC_EN=1 LOGICLKOUT_EN=1	SYSREF_EN=0	49
			SYSREF_EN=1	59
	Output Buffer		CML(R_P=50Ω)	16+1*LOGICLKOUT_PWR
			LVDS	12
			LVPECL	30
LOGISYSREFOUT	Core	LOGIC_EN=1 LOGISYSREFOUT_EN=1	SYSREF_EN=0	0
			SYSREF_EN=1	55
	Output Buffer	LOGIC_EN=1 LOGISYSREFOUT_EN=1	CML(R_P=50Ω)	16+1*LOGICLKOUT_PWR
			LVDS	12
			LVPECL	30

This device can consume a significant amount of current if all the output clocks, LOGICLK, multiplier, and multiplier are all enabled. Turning off the SYSREF output buffers when not actively sending SYSREF pulses to conserve current is recommended to mitigate current consumption.

8.1.4 Treatment of Unused Pins

In many cases, not all pins are needed. 表 8-4 gives recommendation on handling of these unused pins.

表 8-4. Treatment of Unused or Partially Used Pins

PIN(S)	TREATMENT
All Vcc Pins	These pins must always be connected to the supply. If the block that this powers (as implied by the pin name) is not used, then the bypassing can be minimized or eliminated.
SYSREFREQ	If driving single-ended AC coupled, the complimentary input must have a AC-coupling capacitor to ground. If driving single-ended DC coupled, complimentary input must be externally biased at required VCM with Thevenin's equivalent. If using continuous SYSREF Generator mode, these pins can be either used to turn the output buffers on and off or they can be left floating. If left floating, use SYSREFREQ_SPI to control the output gating. If not using SYSREF at all, pins can be left open.

表 8-4. Treatment of Unused or Partially Used Pins (続き)

PIN(S)	TREATMENT
CLKIN Complementary Input	If driving single-ended, the complementary input must have a AC-coupling capacitor and 50 Ω to ground.
BIAS01 and BIAS23	These pins can be left open if multiplier is not used.
CLKOUT SYSREFOUT LOGICLKOUT LOGISYSREFOUT	These pins can be left open if not used.

8.2 Typical Application

For this application, the additive noise impact of using the LMX1204 as a ×2 multiplier is explored when added to the LMX2820 3-GHz output clock. This particular setup uses a single-ended clock to drive the LMX1204 to combine two EVMs together, but driving the setup differentially is generally recommended.

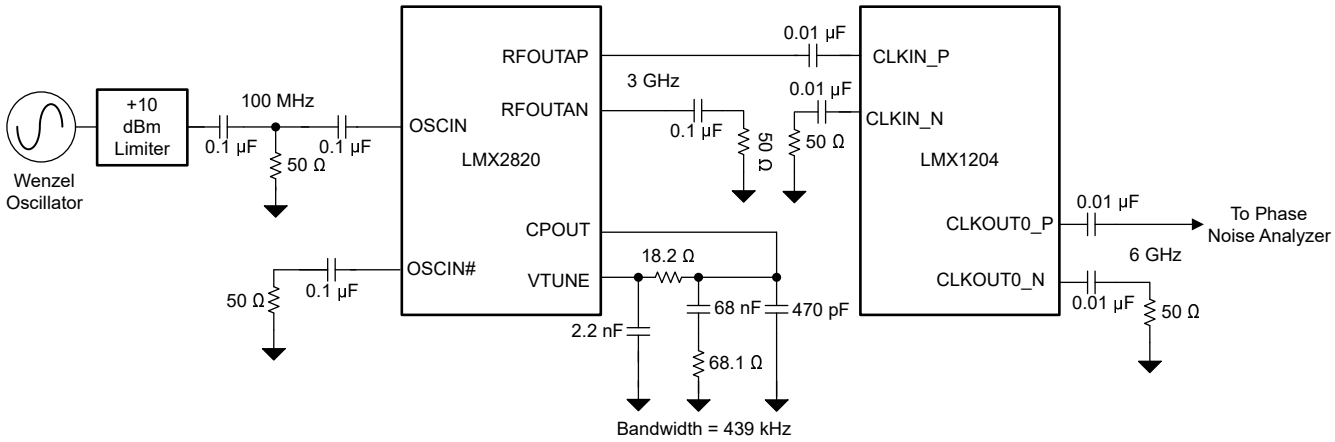

図 8-8. Typical Application Schematic

8.2.1 Design Requirements

表 8-5 shows the design parameters for this example.

If not all outputs or SYSREF are used, TI recommends to compress the layout to minimize trace lengths, especially that of the input trace.

表 8-5. Design Parameters

PARAMETER	VALUE
LMX2820 Input Frequency	100 MHz
LMX2820 Output Frequency	3 GHz
LMX1204 Input Clock Frequency	3 GHz
LMX1204 Output Clock Frequency	6 GHz
Multiplier Value	x2

8.2.2 Detailed Design Procedure

In this example, a 3-GHz input clock is being multiplied up to a 6-GHz input clock. The external components do not change that much based on internal configuration. The TICS Pro software is very useful in calculating the necessary register values and configuring the device.

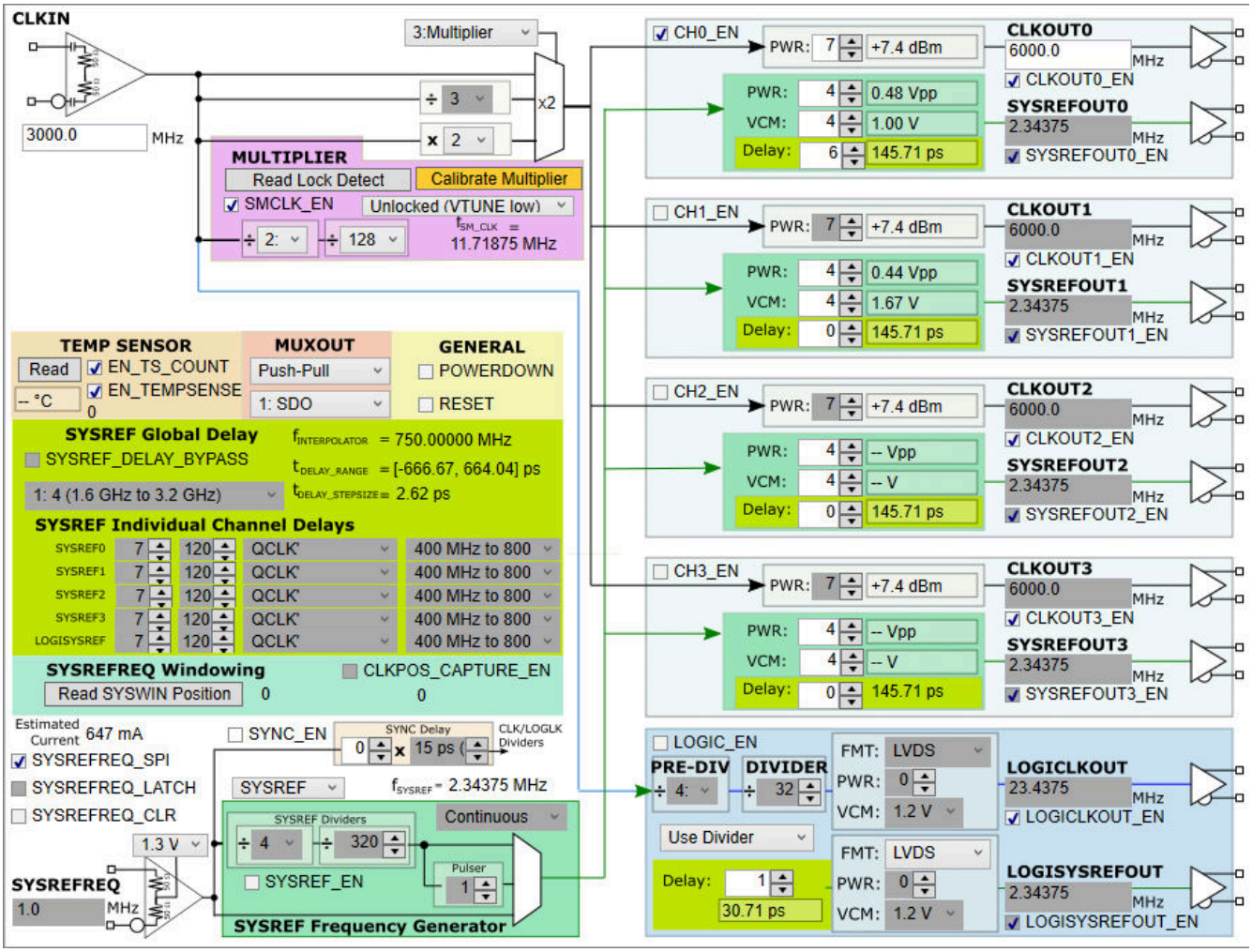

図 8-9. LMX1204 TICS Pro Setup

8.2.3 Application Curve

In 図 8-10, the total plot is the sum of the noise of the LMX1204 multiplier noise and the LMX2820 3-GHz output (scaled to 6 GHz by adding 6 dB). Note that the LMX1204 does increase the phase noise in the 1-MHz to 20-MHz range, but beyond 20 MHz, the input multiplier actually filters the output noise floor.

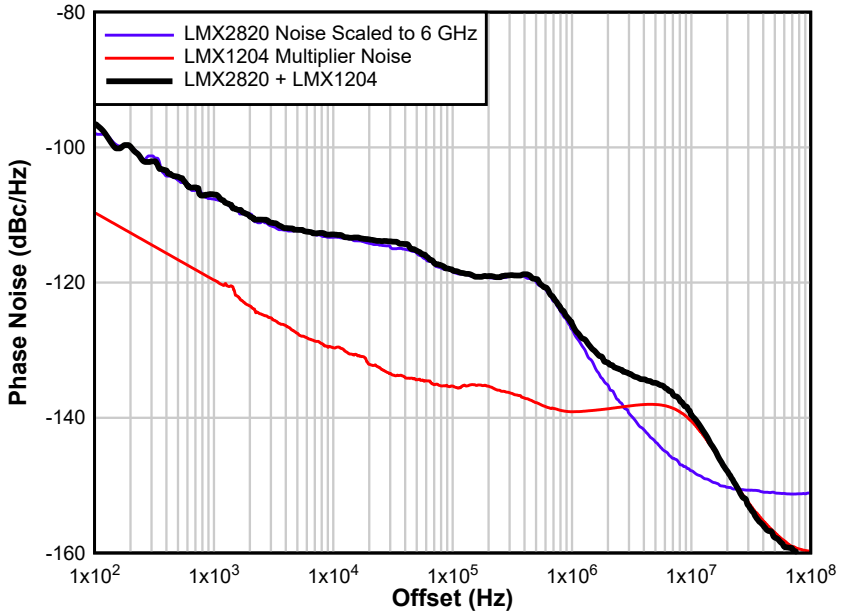

図 8-10. Multiplier Output Frequency

8.3 Power Supply Recommendations

This devices uses a 2.5-V supply for the whole device. A direct connection to a switching power supply likely results in unwanted spurs at the output. Bypassing can be done individually at all the power pins. TI recommends placing smaller capacitors with higher frequency of minimum impedance on the same layer as the device, as close to the pins as possible. The frequencies of nearly all signals in the device are 100 MHz or greater, therefore larger value bypass capacitors with low frequency of minimum impedance are only used for internal LDO stability, and the distance to the device (and the loop inductance of the bypass path) can be larger. Isolate the supply pins for the clocks and the LOGICLK with a small resistor or ferrite bead if both are being used simultaneously. See the *Pin Configuration and Functions* section for additional recommendations for each pin.

注

This device has minimal PSRR due to the low operating voltage and internal filtering by LDOs. Connecting this device to a low noise supply that does not have excessive spurious noise is important.

8.4 Layout

8.4.1 Layout Guidelines

- If using an output single-ended, terminate the complementary side so that the impedance as seen looking out from the complementary side is similar to side that is used.
- GND pins on the outer perimeter of the package can be routed on the package back to the DAP.
- Minimize the length of the CLKIN trace for optimal phase noise. Poor matching can degrade the noise floor.
- Verify that the DAP on device is well-grounded with many vias.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- Be aware that if all the outputs and SYSREF are operating, the current consumption can be high enough to exceed the recommended internal junction temperature of 125°C; a heat sink can be necessary.

8.4.2 Layout Example

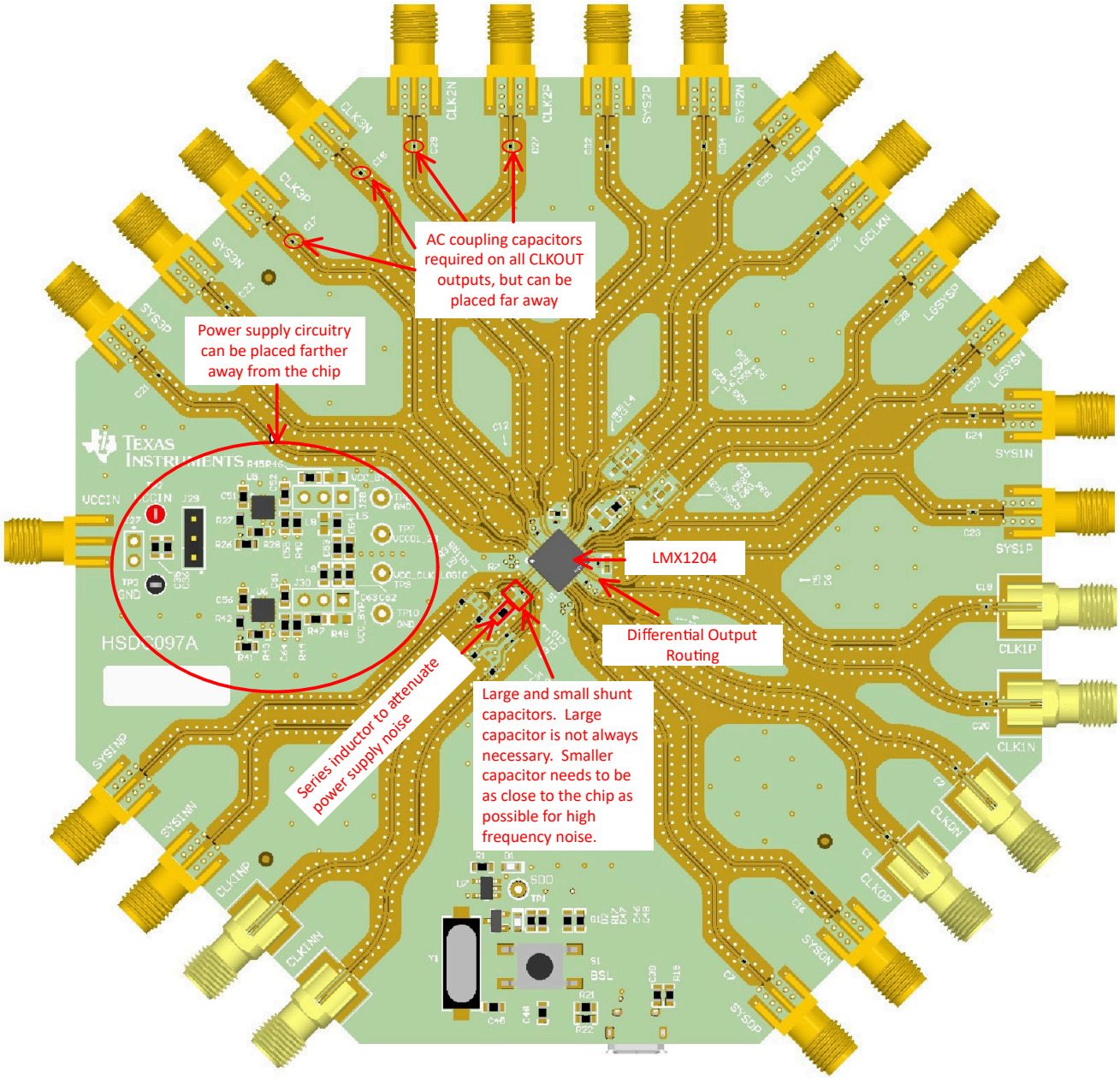

図 8-11. Layout Example

9 Device and Documentation Support

9.1 Device Support

TI offers an extensive line of development tools and software to simulate the device performance and program the device.

表 9-1. Development Tools and Software

TOOL	TYPE	DESCRIPTION
PLLatinum™ Sim	Software	Simulates phase noise in all modes
TICS Pro	Software	Programs the device with a user-friendly GUI with interactive feedback and hex register export.

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, *Cascaded LMX1204 Phase-Error Analysis*, application note
- Texas Instruments, *LMX1204 Multiplier Clock Distribution Drives Large Phased-Array Systems*, application note
- Texas Instruments, *Getting the Most of Your Data Converter Clocking System Using LMX1204*, application note

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2022) to Revision B (February 2024) **Page**

- 「特長」に「ジッタ:5fS」を追加 ... 1
- Updated SPI timing diagram and readback comments ... 8
- Changed the *Typical Characteristics* section for production data release ... 9
- Updated Functional Block Diagram ... 16
- Added that filter mode does not work with SYNC mode ... 19
- Updated VOD/VCM values in table ... 23
- Updated SYSREF windowing and repeater mode added ... 27
- Added SYSREF Windowing Flowchart ... 28
- Added AYSREF Repeater Mode with Delay Gen (Retime) ... 28
- Added Register Map ... 31
- Added SYSREFREQ Input Configuration Section ... 56
- Added Reducing SYSREF Common Mode Voltages section ... 57

Changes from Revision * (July 2021) to Revision A (August 2022) **Page**

- データシート ステータスを「事前情報」から「量産データ」に変更 ... 1
- データシートにフィルタ モードの情報を追加 ... 1
- Added descriptions for POR, multiplier, filter mode, common mode voltage, and other topics in the *Detailed Description* section ... 15
- Changed register and field definitions from pre-production to production ... 33
- Changed 表 8-3 ... 58
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section ... 62

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX1204RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX1204
LMX1204RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX1204
LMX1204RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX1204
LMX1204RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX1204

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

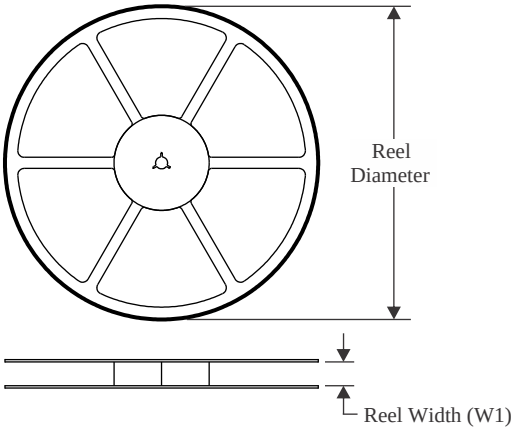
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

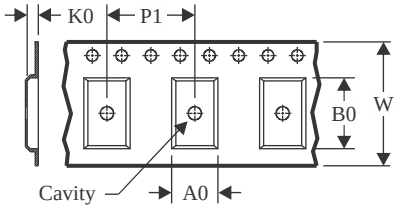
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

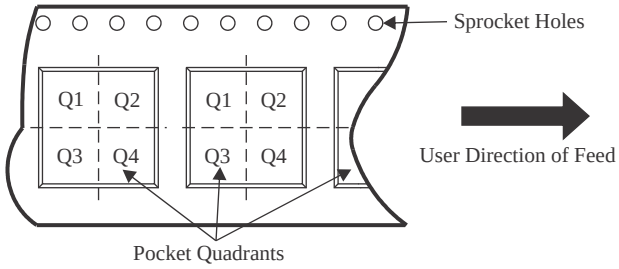


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

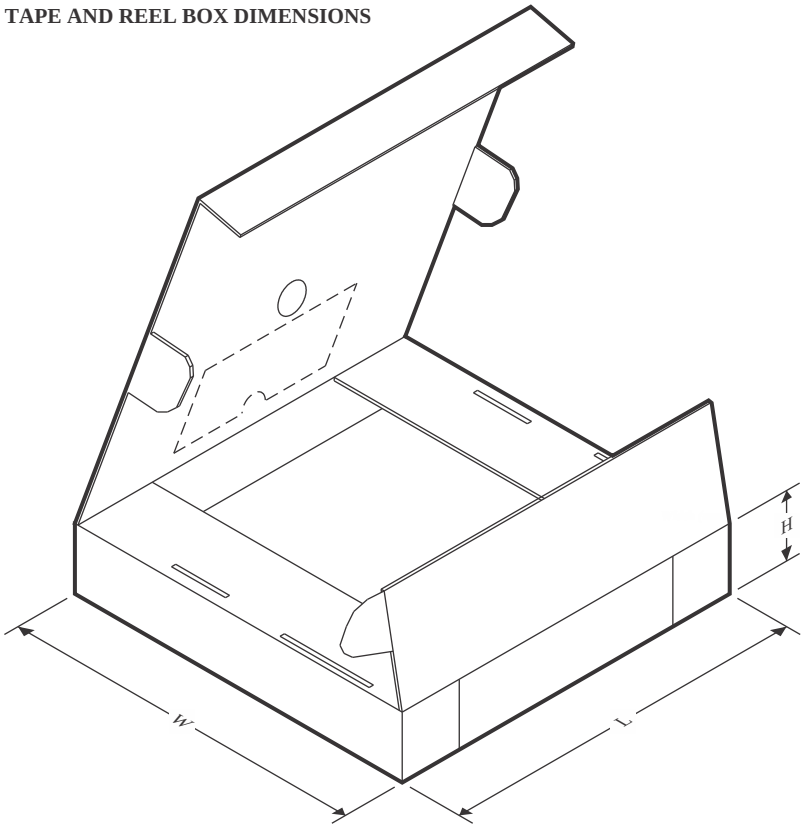
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX1204RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMX1204RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX1204RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
LMX1204RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

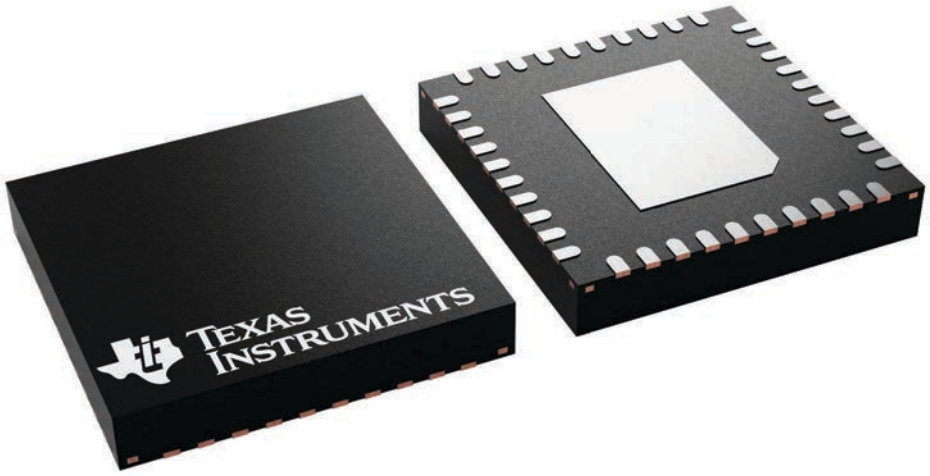
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



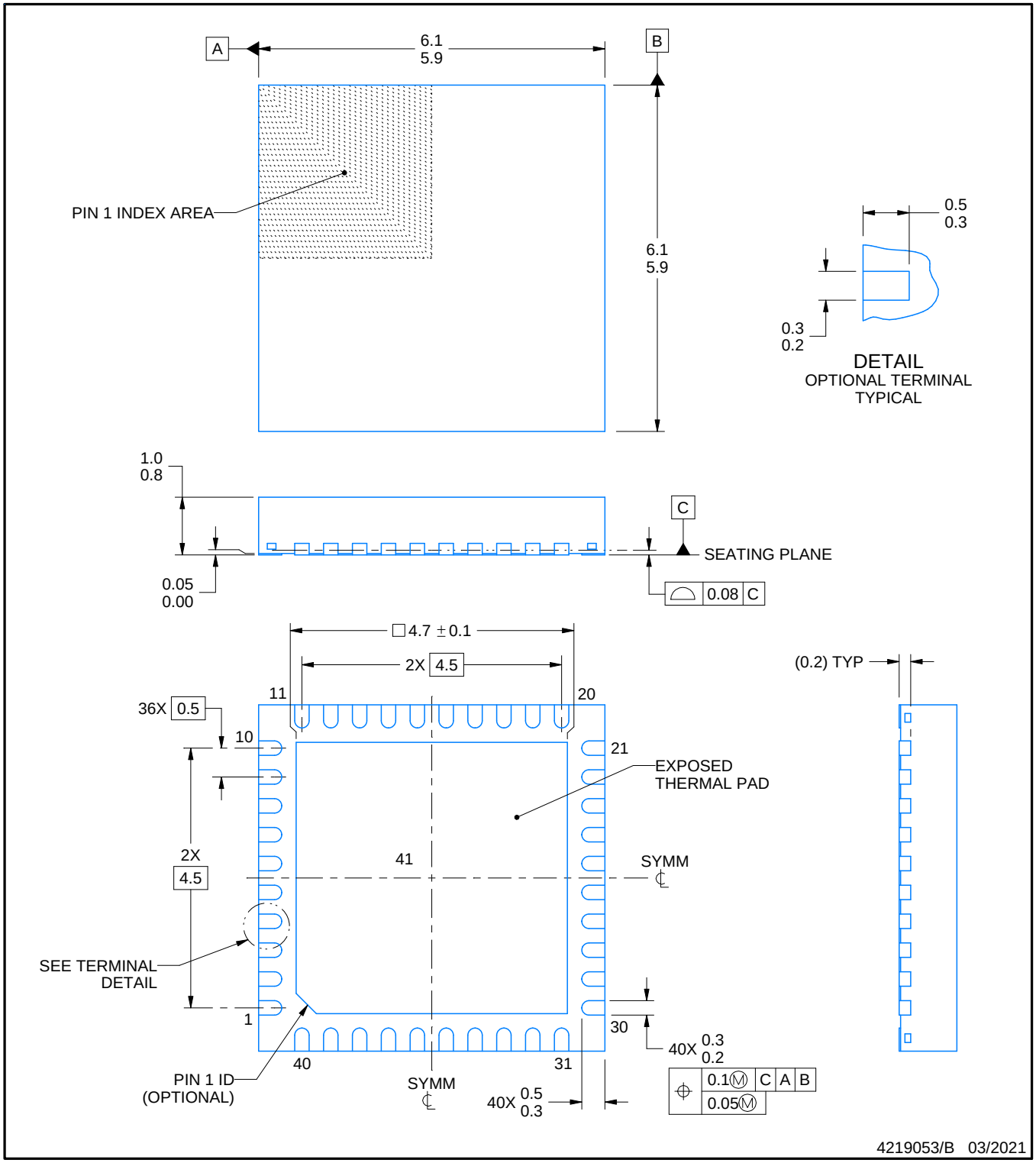
4225870/A

RHA0040C

PACKAGE OUTLINE

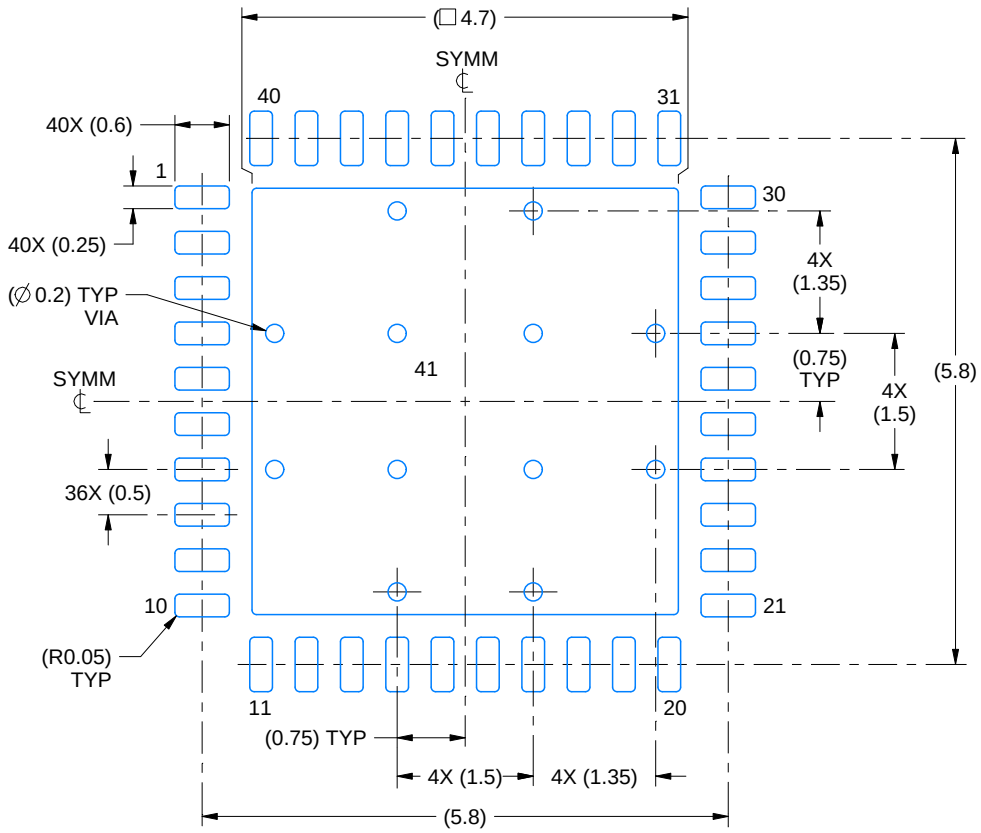
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

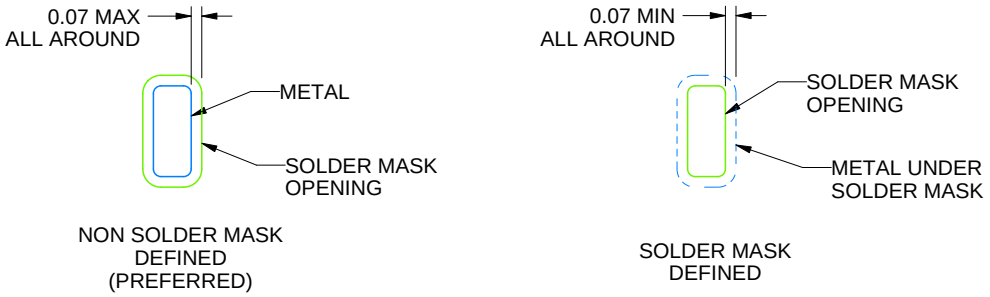


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

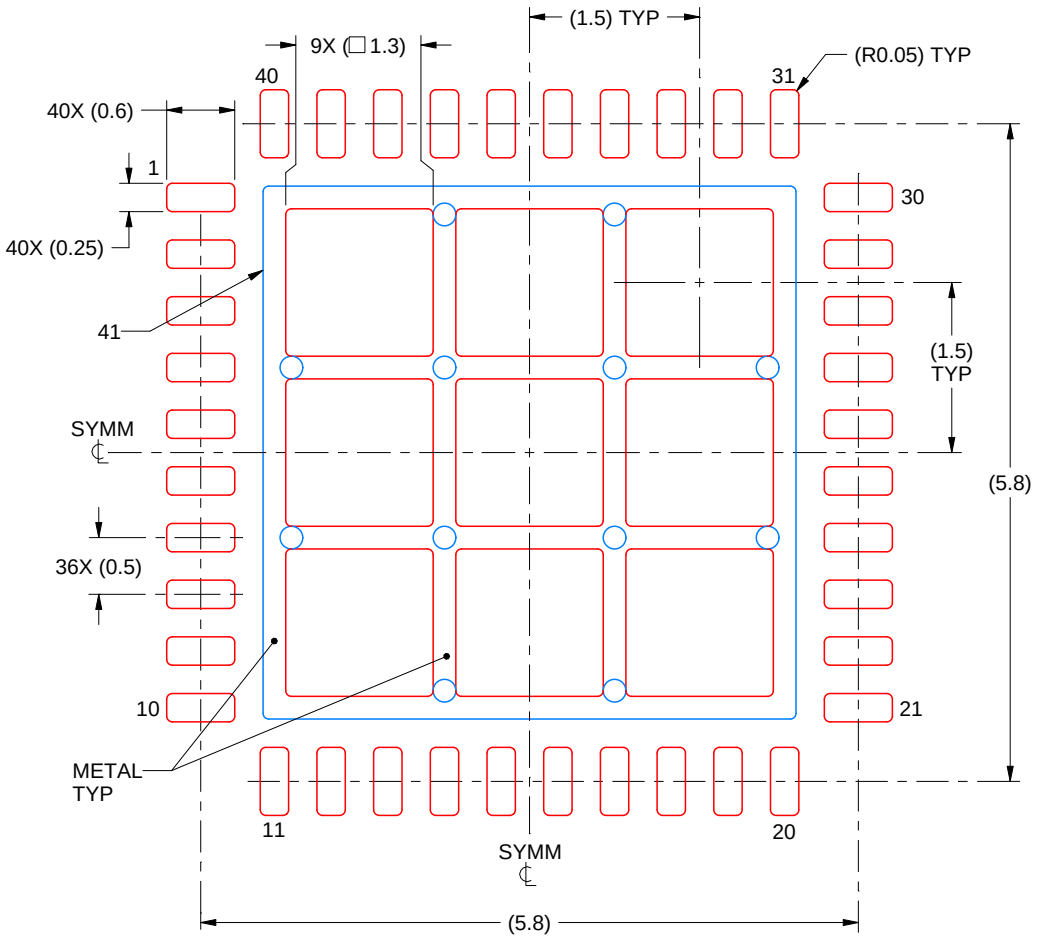


SOLDER MASK DETAILS

4219053/B 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/B 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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