TEXAS INSTRUMENTS
LMR66430-EP
JAJSR66 – SEPTEMBER 2024

LMR66430-EP 36V、3A、超小型同期整流降圧コンバータ

1 特長

- 広い入力電圧範囲
  - 3.35V～36V の立ち上がりエッジ
  - 2.7V～36V の立ち下がりエッジ
  - 絶対最大電圧 42V
- 132mΩ および 75mΩ の MOSFET を内蔵
- 低 EMI 要件に対して最適化:
  - デュアル ランダム スペクトラム拡散により、ピーク放射を低減
  - 軽負荷時の固定周波数の FPWM モードと F_{SW} 同期を MODE/SYNC ピンで選択可能
  - 調整可能な F_{SW}:200kHz～2.2MHz (RT ピンで調整)
- 小さなソリューション サイズとわずかな部品コスト:
  - ウェッタブル フランクと内部鉛フリーはんだを使った 2.6mm × 2.6mm 拡張 HotRod™ QFN パッケージ
  - 内部制御ループ補償

2 アプリケーション

- 防衛および航空宇宙アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - -55℃～150℃の温度範囲に対応する接合部温度
  - 長期にわたる製品ライフ サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ
- 医療用
- 試験および測定機器
- モータードライブ

3 概要

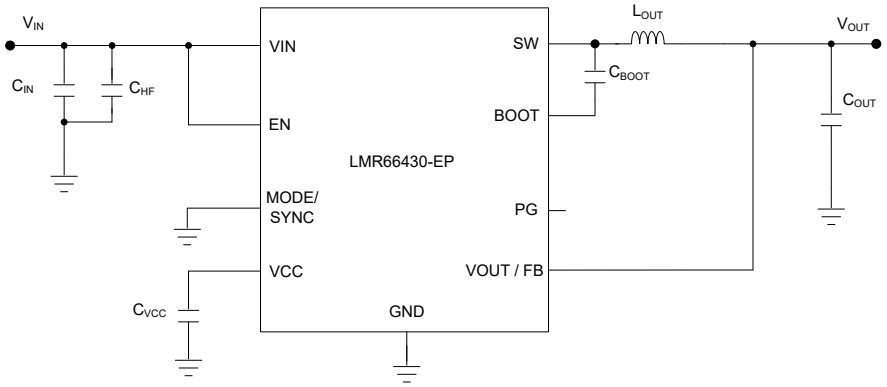
LMR66430-EP は、拡張 HotRod QFN パッケージに封止された小型の 36V、3A 同期整流降圧型 DC/DC コンバータです。この使いやすいコンバータは 2.7V～36V の広い入力電圧範囲 (起動後または動作を開始した後) と最大 42V の過渡電圧に対応しています。

LMR66430-EP は、特に常時オンのアプリケーションの低スタンバイ電力要件を満たすように設計されています。自動モードは、軽負荷動作時の周波数フォールドバックを可能にするため、軽負荷効率を高めることができます。パルス幅変調 (PWM) モードとパルス周波数変調 (PFM) モードの間のシームレスな移行と非常に小さな MOSFET オン抵抗により、負荷範囲全体にわたって非常に優れた効率を確保しています。この制御アーキテクチャ (ピーク電流モード) および機能セットは、超小型の設計サイズと最小限の出力容量に最適です。本デバイスは、デュアル ランダム拡散スペクトラム (DRSS)、低 EMI の拡張 HotRod QFN パッケージ、最適化されたピン配置を使用して入力フィルタのサイズを最小化しています。MODE/SYNC および RT ピンのバリアントを使って周波数を設定する (同期させる) ことで、ノイズの影響を受けやすい周波数帯域を回避できます。重要な高電圧ピンの間に NC ピンを配置することで、ピン間の短絡の可能性を低減しています。LMR66430-EP の豊富な機能セットは、広範な産業用最終機器を簡単に実装できるように設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMR66430-EP	RXB (VQFN-FCRLF、14)	2.6mm × 2.6 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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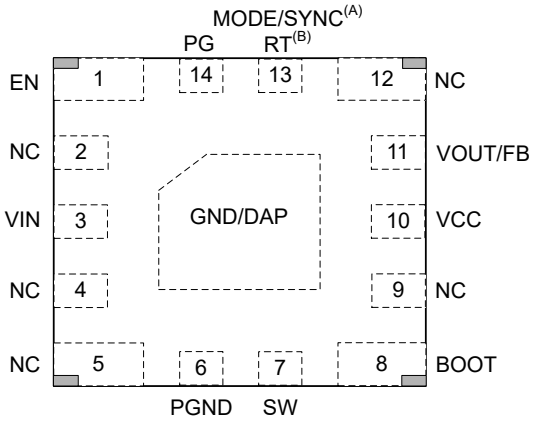
4 Device Comparison Table

Orderable Part Number (1)	Output Current	Output Voltage	External Sync	F_{SW}	Internal Capacitors	Spread Spectrum
LMR66430MB3RXBRNEP	3A	3.3V fixed / adjustable	Yes (PFM / FPWM selectable)	Fixed 1MHz	No	Yes
LMR66430R3RXBRNEP	3A	3.3V fixed / adjustable	No (Default PFM at light load)	Adjustable with RT resistor	No	No

(1) For more information on device orderable part numbers, see *Device Nomenclature*.

5 Pin Configuration and Functions



A. Pin 13 is factory-set for fixed switching frequency MODE/SYNC variants only.
B. See *Device Comparison Table* for more details. Pin 13 is factory-set for externally adjustable switching frequency RT variants only.

図 5-1. RXB 14-Pin (2.6mm × 2.6mm) Enhanced HotRod™ VQFN-FCRLF Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float this pin.*
NC	2	—	No internal connection to device
VIN	3	P	Input supply to regulator. High-quality bypass capacitors must be added directly between this pin and PGND.
NC	4	—	No internal connection to device
NC	5	—	No internal connection to device
PGND	6	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
SW	7	P	Regulator switch node. Connect to the power inductor.
BOOT	8	P	Bootstrap supply voltage for internal high-side driver. An external 0.1µF, 16V capacitor is required between this pin and SW.
NC	9	—	No internal connection to device
VCC	10	A	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1µF capacitor from this pin to GND.
VOUT/FB	11	A	Fixed output options and adjustable output options are available with the VOUT/FB pin variant. Connect to the output voltage node for fixed V_{OUT}. See *セクション 7.3.7* for how to select feedback resistor divider values. See *Device Comparison Table* for more details. The FB function can be used to adjust the output voltage. Connect to tap point of feedback voltage divider. *Do not float this pin.*
NC	12	—	No internal connection to device
RT or MODE/ SYNC	13	A	For the *RT variant*, the switching frequency can be adjusted from 200kHz to 2.2MHz. For the *MODE/SYNC variant*, the device can operate in user-selectable PFM/FPWM mode and can be synchronized to an external clock. *Do not float this pin.*
PG	14	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. This pin goes low when EN = low. This pin can be open or grounded when not used.
GND/DAP	—	G	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.
A = Analog, P = Power, G = Ground			

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to GND	–0.3	42	V
Voltages	SW to GND	–0.3	42.3	V
Voltages	BOOT to SW	–0.3	5.5	V
Voltages	VCC to GND	–0.3	5.5	V
Voltages	VOUT/FB to GND	–0.3	16	V
Voltages	SYNC/MODE or RT to GND	–0.3	5.5	V
Voltages	PG to GND	–0.3	20	V
Voltages	EN to GND	–0.3	42	V
Temperature	T_J, Junction temperature	–55	150	°C
Temperature	T_{stg}, Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –55°C to 150°C (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range for start-up	3.35	36	V
	Input voltage range after start-up	2.7	36	V
V_{OUT}	Output voltage range with adjustable output voltage setup	1	18	V
I_{OUT}	LMR66430-EP continuous DC output current range	0	3	A
T_J	Operating junction temperature	–55	150	°C

6.4 Thermal Information

The value of $R_{\theta JA}$ in this table is only valid for comparison with other packages. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

THERMAL METRIC (1)		LMR66430-EP VQFN 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC)	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –55°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 13.5V, VOUT = 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{INMIN}	Input voltage rising threshold for start-up	Before start-up	3.2	3.35	3.5	V
	Input voltage falling threshold	Once operating	2.45	2.7	3	V
$I_{SD(VIN)}$	Shutdown quiescent current at VIN pin	EN = 0V		0.25	1	µA
I_{BIAS}	Non-switching input current at VOUT/FB	Fixed 3.3Vout, $V_{VOUT/FB}$ = 3.47V		4.2	6.5	µA
$I_{QVIN(nonsw)}$	Non-switching input current; measured at VIN pin (1)	Fixed 3.3V V_{OUT}, $V_{VOUT/FB}$ = 3.47V		1.2	2.3	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	EN wakeup threshold		0.5	0.7	1	V
$V_{EN-VOUT}$	Precision enable rising threshold for V_{OUT}		1.16	1.23	1.3	V
$V_{EN-HYST}$	Enable hysteresis below $V_{EN-VOUT}$		0.3	0.35	0.4	V
I_{LKG-EN}	Enable pin input leakage current	V_{EN} = V_{IN} = 13.5V		10		nA
INTERNAL LDO (VCC PIN)						
V_{CC}	VCC pin output voltage	V_{FB} = 0V, I_{VCC} = 1mA	3.1	3.3	3.45	V
VOLTAGE FEEDBACK (VOUT/FB PIN)						
V_{OUT}	Output voltage accuracy for fixed V_{OUT}	3.3V V_{OUT}, V_{IN} = 3.6V to 36V, FPWM mode	3.27	3.3	3.32	V
V_{FB}	Internal reference voltage accuracy	V_{OUT} = 1V, V_{IN} = 3.0V to 36V, FPWM Mode	0.99	1.00	1.01	V
$I_{FB(LKG)}$	FB input current	Adjustable configuration, FB = 1V		10		nA
CURRENT LIMITS						
$I_{PEAKMAX}$	High-side peak current limit		3.8	4.4	5	A
I_{VALMAX}	Low-side valley current limit		2.9	3.5	4	A
$I_{PEAKMIN}$	Minimum peak current limit	Auto mode	0.45	0.69	0.95	A
I_{NEGMIN}	Low-side valley current negative limit	FPWM mode	–1.5	–1.3	–1	A
I_{ZC}	Zero-cross current limit	Auto mode	30	80	135	mA
POWER GOOD (PG PIN)						
PG_{OV}	PG upper threshold - rising	% of VOUT/FB (Fixed or Adj. output)	104	108	111	%
PG_{UV}	PG upper threshold - falling	% of VOUT/FB (Fixed or Adj. output)	89	91	94.2	%

6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature range of –55°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 13.5V, VOUT = 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG_{HYST}	PG recovery hysteresis for OV	% of VOUT/FB target regulation voltage	1.7	2	2.3	%
	PG recovery hysteresis for UV	% of VOUT/FB target regulation voltage	1.9	3.3	4.6	%
V_{PG-VAL}	Minimum V_{IN} for PG function	V_{EN} = 0V, R_{PG_PU} = 10kΩ			1.5	V
R_{PG}	PG ON resistance	V_{EN} = 3.3V, 200µA pullup current			100	Ω
R_{PG}	PG ON resistance	V_{EN} = 0V, 200µA pullup current			100	Ω
t_{RESET_FILTER}	PG deglitch delay at falling edge		25	40	75	µs
t_{PG_ACT}	Delay time to PG high signal		1.35	2.5	4	ms
SOFT START						
t_{SS}	Time from first SW pulse to VOUT/FB at 90% of set point		2	3.5	4.6	ms
t_{HICCUP}	Time in hiccup before retry soft start		30	50	75	ms
OSCILLATOR (SYNC/MODE PIN)						
$t_{PULSE\_H\_ATE}$	High level pulse minimum duration needed to be recognized as a valid clock signal (2)				100	ns
$t_{PULSE\_L\_ATE}$	Low level pulse minimum duration needed to be recognized as a valid clock signal (2)				100	ns
t_{SYNC_THRESH}	High/Low level pulse maximum duration to be recognized as a valid clock signal		6	9	12.5	µs
$F_{SW(1MHz)}$	Switching Frequency with fixed 1 MHz		900	1000	1060	kHz
V_{MODE_L}	SYNC/MODE input voltage low level threshold				1	V
V_{MODE_H}	SYNC/MODE input voltage high level threshold		1.65			V
OSCILLATOR (RT PIN)						
$F_{SW(1MHz)}$	Switching frequency with Internal fixed 1 MHz setting	RT pin tied to V_{CC}	900	1000	1060	kHz
$F_{SW(2p2MHz)}$	Switching frequency with fixed 2.2MHz	RT pin tied to GND	2050	2200	2350	kHz
$F_{SW(Adj)}$	Accuracy of external frequency, 400kHz	R_{RT} = 39.2kΩ 0.1% resistor	340	400	460	kHz
SWITCH NODE						
t_{ON-MIN}	Minimum HS switch on-time	FPWM mode I_{OUT} = 1A, 2.2MHz fixed		65	76	ns
$t_{OFF-MIN}$	Minimum HS switch off-time			60	85	ns
t_{ON-MAX}	Maximum HS switch on-time	HS timeout in dropout	6	9	13	µs
POWER STAGE						
V_{BOOT_UVLO}	Voltage on BOOT pin compared to SW which will turnoff high-side switch			2.1		V
$R_{DSON-HS}$	High-side MOSFET on-resistance	Load = 1A		132	260	mΩ
$R_{DSON-LS}$	Low-side MOSFET on-resistance	Load = 1A		75	140	mΩ

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(2) The high/low level clock pulse duration must be equal to or greater than the value shown.

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5V.

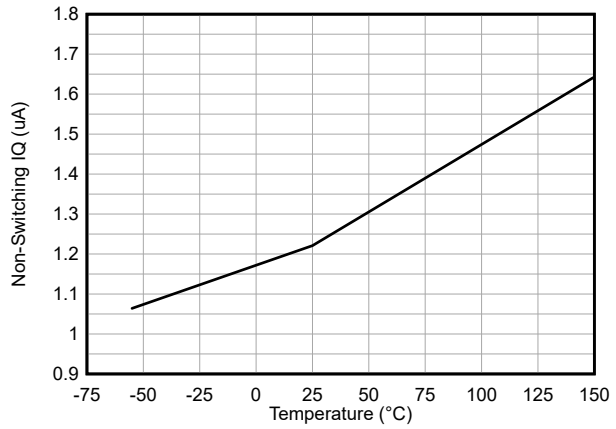


図 6-1. Nonswitching Input Current ($I_{QVIN(nonsw)}$) vs Temperature

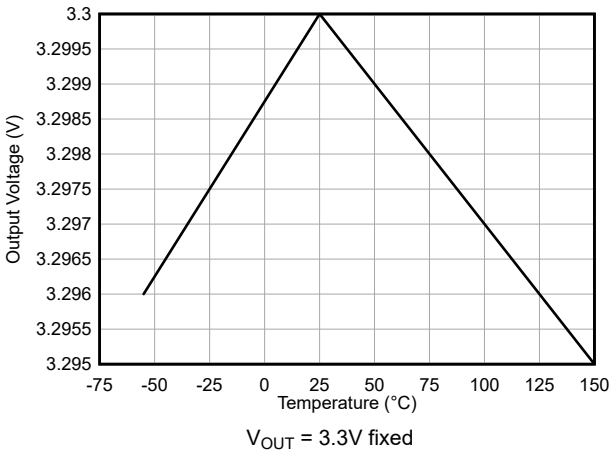


図 6-2. Output Voltage Accuracy vs Temperature

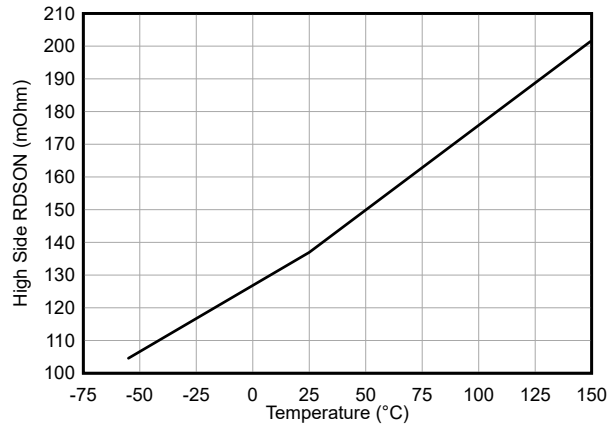


図 6-3. High Side MOSFET On Resistance ($R_{DSON-HS}$) vs. Temperature

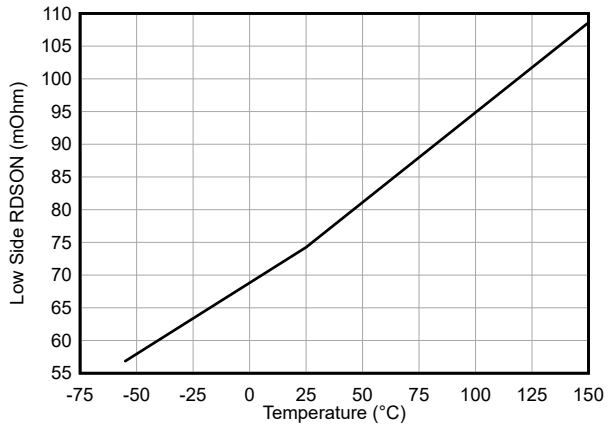


図 6-4. Low Side MOSFET On Resistance ($R_{DSON-LS}$) vs. Temperature

7 Detailed Description

7.1 Overview

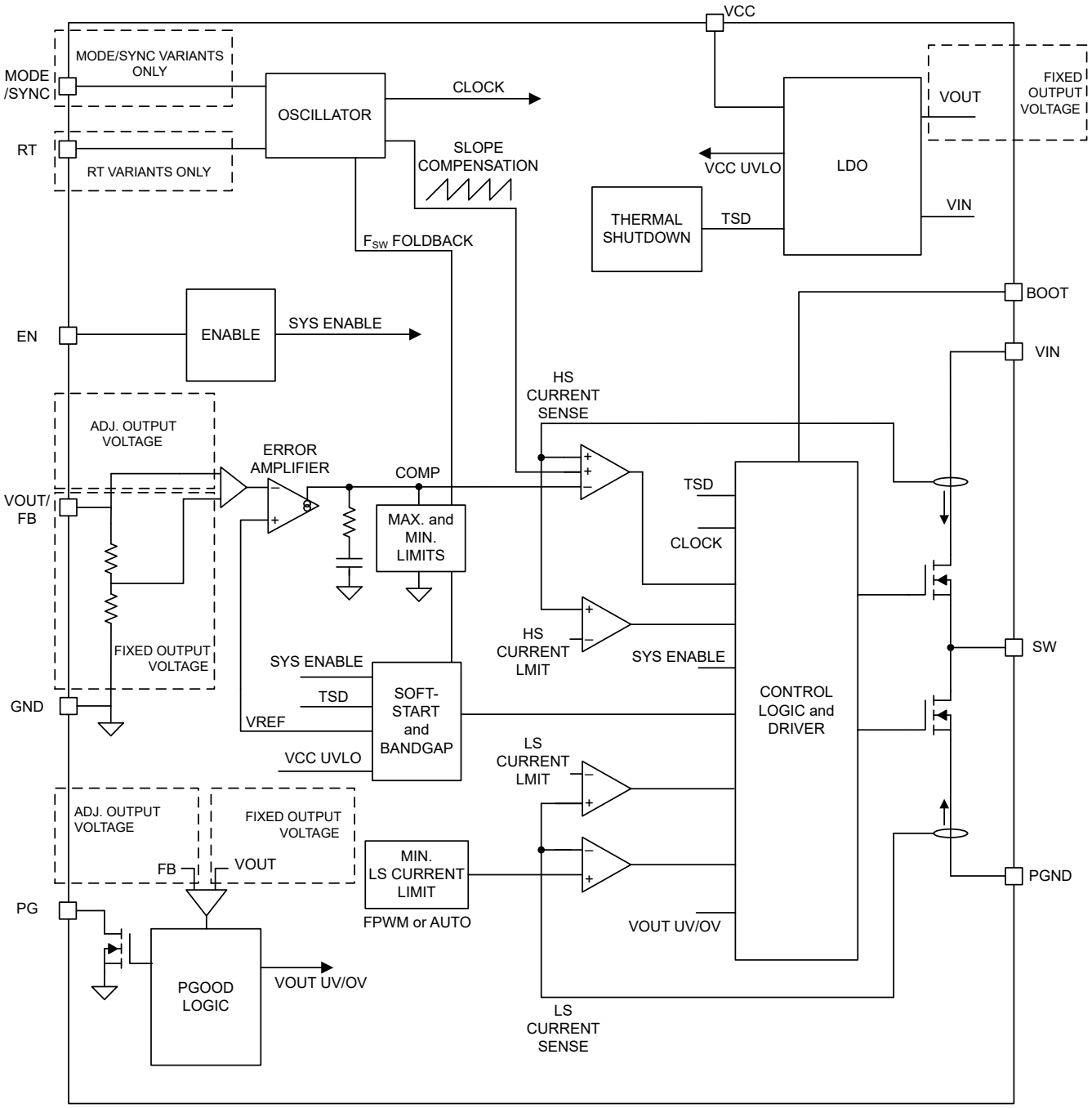
The LMR66430-EP is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of duty ratio and the switching frequencies, including sub-AM band at 400kHz and above AM band at 2.2MHz. During wide input transients, if the minimum on time or the minimum off time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the device to maintain the output voltage regulation. With an internally compensated design optimized for minimal output capacitors, the system design process with the device is simplified significantly compared to other buck regulators available in the market.

The device is designed to minimize external component cost and design size while operating in all demanding industrial environments. The device family includes variants that can be set up to operate over a wide switching frequency range, from 200kHz to 2.2MHz, with the correct resistor selection from the RT pin to ground. To further reduce system cost, the PG output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR66430-EP family is designed to reduce EMI/EMC emissions by introducing a dual random spread spectrum (DRSS) switching frequency dithering scheme, using the enhanced HotRod QFN package where no bond wires are used. Also, available is the MODE/SYNC feature that allows synchronization to an external clock. Together, these features reduce the need for any common-mode choke or shielding or any elaborate input filter design scheme, greatly reducing the complexity and cost of the EMI/EMC mitigation measures.

The device comes in an ultra-small, 2.6mm × 2.6mm, enhanced HotRod QFN package, allowing for quick optical inspection along with specially designed corner anchor pins for reliable board level solder connections.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the LMR66430-EP family of devices. The part stays shut down as long as the EN pin voltage is less than $V_{EN-WAKE}$ = 0.7V (typical). During the shutdown, the input current drawn by the device typically drops down to 0.25µA (V_{IN} = 13.5V). With the voltage at the EN pin greater than $V_{EN-WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN-VOUT}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN-VOUT}$−$V_{EN-HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN-WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the V_{IN} input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The various EN threshold parameters and the values are listed in the *Electrical Characteristics*. 図 7-2 shows the precision enable behavior and 図 7-3 shows a typical remote EN start-up waveform in an application. After EN goes high, after a delay of about 2.5ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 3.5ms (t_{ss}). After a delay of about 2.5ms (t_{PG_ACT}), the PG flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN. Check セクション 8.2.3.9 for component selection.

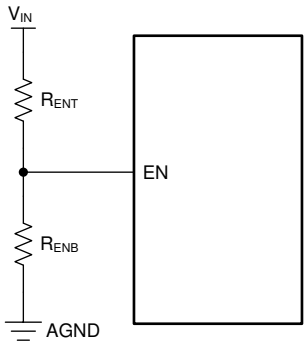


図 7-1. VIN UVLO Using the EN Pin

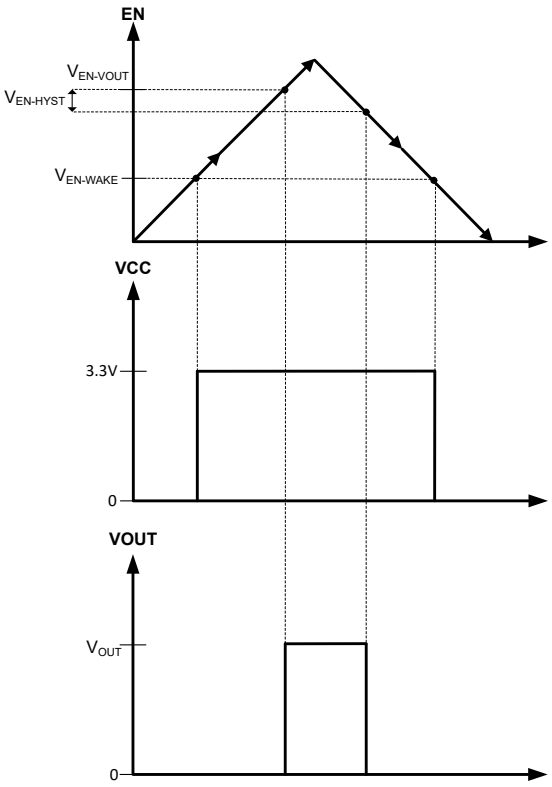


図 7-2. Precision Enable Behavior

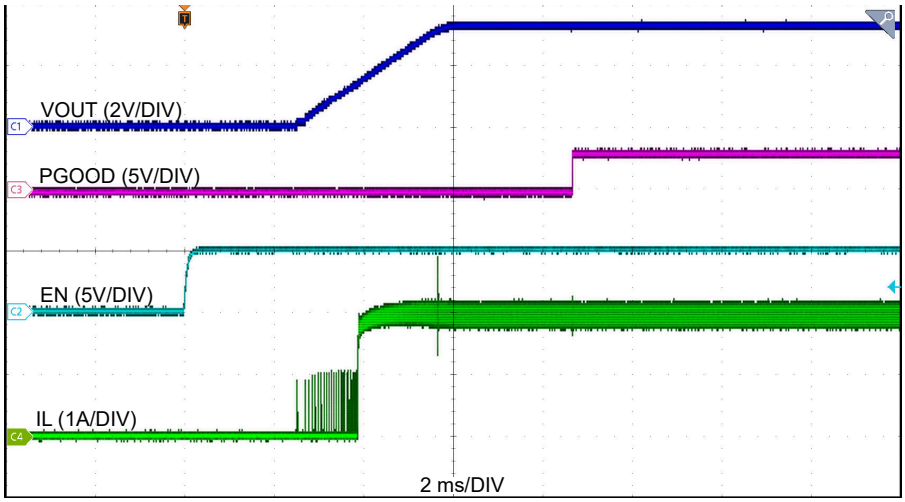


図 7-3. Enable Start-Up V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A

7.3.2 External CLK SYNC (with MODE/SYNC)

Synchronized operation of multiple regulators in a single system is often desirable for a well-defined system level performance. The select variants in the device with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The device implements an in-phase locking scheme, where the rising edge of the clock signal, provided to the MODE/SYNC pin of the device, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL), eliminating any large glitches. The external clock fed into the device replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well regulated. The device

remains in FPWM mode and operates in CCM for light loads when synchronization input is provided. The range of frequencies permitted by the device is given by f_{SYNC} and is provided in the *Electrical Characteristics*.

The MODE/SYNC input pin in the device can operate in one of three selectable modes:

- Auto mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See セクション 7.4.3.2 for more details.
- FPWM mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See セクション 7.4.3.3 for more details.
- SYNC mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off time or minimum on time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, the device operates as though in FPWM mode: diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

7.3.2.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the device are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, a valid sync signal must be applied. 表 7-1 shows a summary of the pulse dependent mode selection settings.

表 7-1. Pulse-Dependent Mode Selection Settings

Mode/Sync Input	Mode
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

図 7-4 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The device transitions to a new mode of operation after the time, t_{MODE}. 図 7-4 and 図 7-5 show the details.

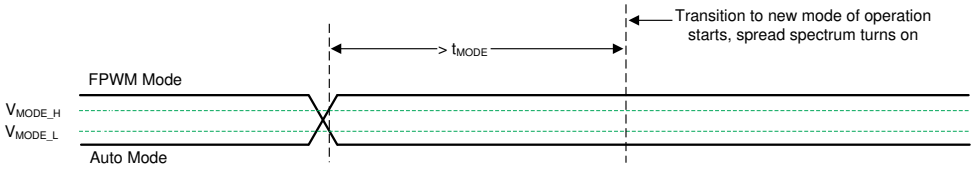


図 7-4. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the device enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

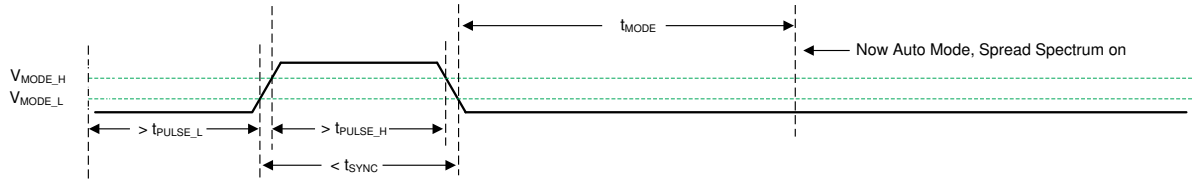


図 7-5. Transition from SYNC Mode to Auto Mode

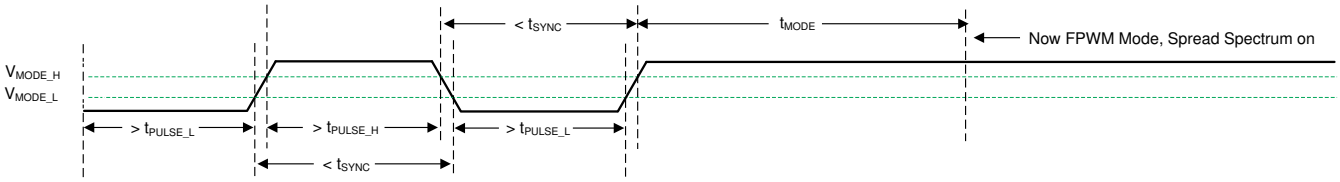


図 7-6. Transition from SYNC Mode to FPWM Mode

7.3.3 Adjustable Switching Frequency (with RT)

The select variants in the device family with the RT pin allow the power designers to set any desired operating frequency between 200kHz and 2.2MHz in the applications. See 図 7-7 to determine the resistor value needed for the desired switching frequency. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See 表 7-2 for selection on programming the RT pin.

表 7-2. RT Pin Setting

RT Input	Switching Frequency
VCC	1MHz
GND	2.2MHz
RT to GND	Adjustable according to 図 7-7
Float (not recommended)	No switching

式 1 can be used to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency.

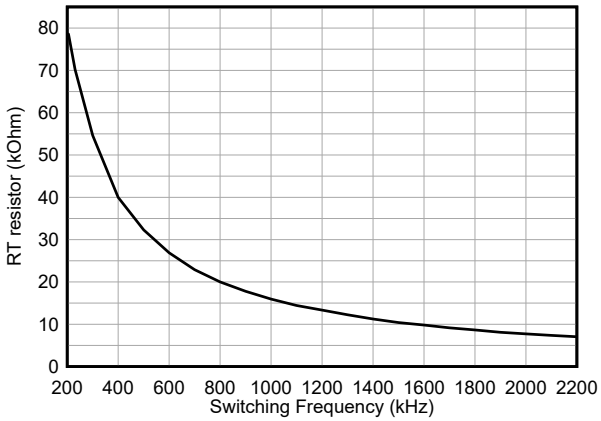


図 7-7. RT Values vs Frequency

7.3.4 Power-Good Output Operation

The power-good feature using the PG pin of the device can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation

for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 7-8. 表 7-3 gives a more detailed breakdown of the PG operation. Here, $V_{PG_{UV}}$ is defined as the PG_{UV} scaled version of V_{OUT} (target regulated output voltage) and $V_{PG_{HYST}}$ as the PG_{HYST} scaled version of V_{OUT}, where both PG_{UV} and PG_{HYST} are listed in the *Electrical Characteristics*. During the initial power up, a total delay of 8.5ms (typical) is encountered from the time $V_{EN-VOUT}$ is triggered to the time that the power good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power good remains valid as long as the input voltage, V_{PG-VAL}, is greater 1.5V (maximum).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. The power-good output scheme can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PG pin can be open or grounded. Limit the current into this pin to ≤ 4mA.

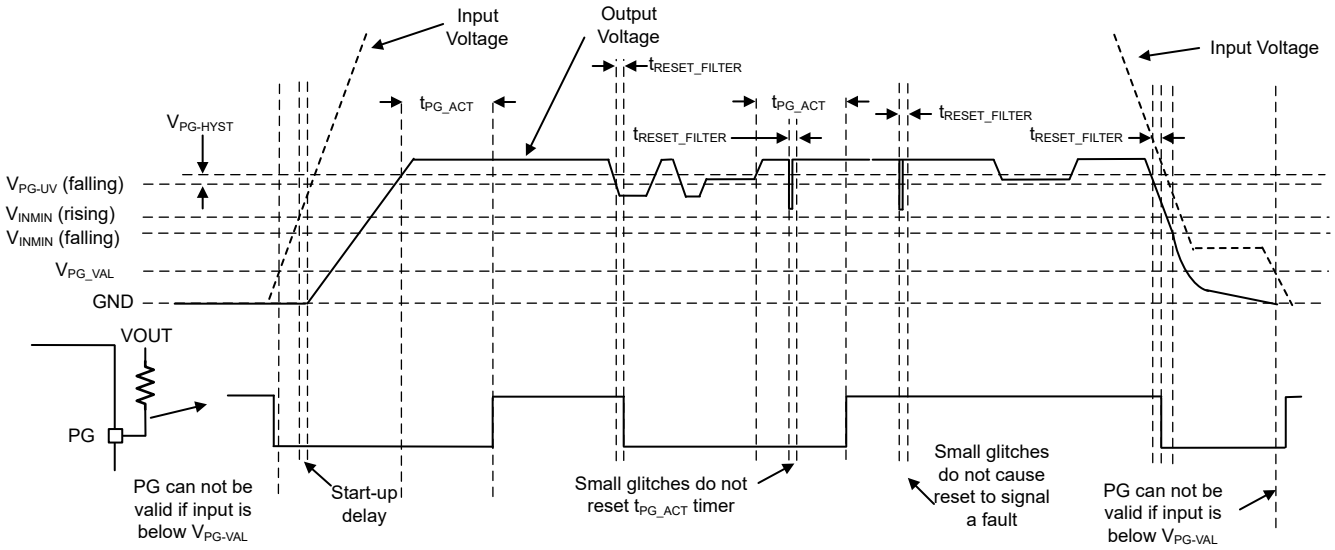


図 7-8. Power-Good Operation (OV Events Not Included)

表 7-3. Fault Conditions for PG (Pull Low)

Fault Condition Initiated	Fault Condition Ends (After Which t_{PG_ACT} Must Pass Before PG Output Is Released)
$V_{OUT} < V_{PG_{UV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PG_{UV}} + V_{PG_{HYST}} < V_{OUT} < V_{PG_{OV}} - V_{PG_{HYST}}$
$V_{OUT} > V_{PG_{OV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD(trip)}$	$T_J < T_{SD(trip)} - T_{SD(hyst)}$ AND output voltage in regulation
$EN < V_{EN-VOUT} - V_{EN-HYST}$	$EN > V_{EN-VOUT}$ AND output voltage in regulation

7.3.5 Internal LDO, VCC, and VOUT/FB Input

The device uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or VOUT/FB (in fixed-output variants). In the fixed-output variants, after the device is active but has yet to regulate, the VCC rail continues to draw power from the input voltage, V_{IN}, until the VOUT/FB voltage reaches > 3.15V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.3V in both adjustable and fixed output variants. During start-up, VCC momentarily exceeds the normal operating voltage and then drops to the normal operating voltage.

7.3.6 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to make sure the HS switch is turned on. The internal 0.1µF capacitor that is connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW + VCC). The boot diode is integrated on the device die to minimize physical design size. The CBOOT rail has a UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.1V. If the BOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

7.3.7 Output Voltage Selection

In the device family, an adjustable output or fixed output voltage option is configurable for every device variant (see セクション 4). For an adjustable output, the user needs an external resistor divider connection between the output voltage node, the device FB pin, and the system GND, as shown in 図 7-9. The adjustable output voltage operation uses a 1V internal reference voltage.

When using the fixed-output configuration from the device family, simply connect the FB pin (identified as VOUT/FB pin for fixed-output variants in the rest of the data sheet) to the system output voltage node. See セクション 4 for more details.

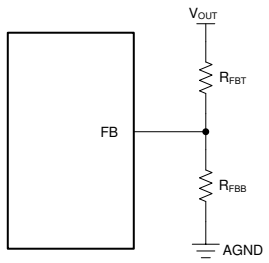


図 7-9. Setting Output Voltage for Adjustable Output Variant

In adjustable output voltage configuration, an additional feedforward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See セクション 8.2.3.8 for more details. No additional resistor divider or feedforward capacitor is needed in fixed-output variants.

Programming the output voltage can be achieved by selecting the top feedback resistance, R_{FBT} (that is, 100kΩ), then calculating for R_{FBB} (式 2). The additional criteria is that the minimum value for the parallel combination of R_{FBT} and R_{FBB} is greater than 5kΩ (式 3).

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \tag{2}$$

$$5\ k\Omega < R_{FBT} \| R_{FBB} \tag{3}$$

7.3.8 Spread Spectrum

In the LMR66430-EP family of devices, spread spectrum is a factory option. To find which parts have spread spectrum enabled, see セクション 4.

Spread spectrum reduces peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LMR66430-EP implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LMR66430-EP uses a spread of frequencies, which can spread energy smoothly across the

FM and TV bands. The device implements dual random spread spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional pseudo-random jumps at the switching frequency

The advantage of DRSS is the equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the LMR66430-EP also allows the user to further reduce the output voltage ripple caused by the spread spectrum modulating pattern.

The spread spectrum is only available while the clock of the device is free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning spread spectrum off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on time reaches minimum on time. See the *Electrical Characteristics*
- The clock is synchronized with an external clock.

7.3.9 Soft Start and Recovery from Dropout

When designing with the LMR66430-EP, slow rise in output voltage due to recovery from dropout and soft start must be considered as two separate operating conditions, as shown in 図 7-10 and 図 7-11. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a prebias start-up.

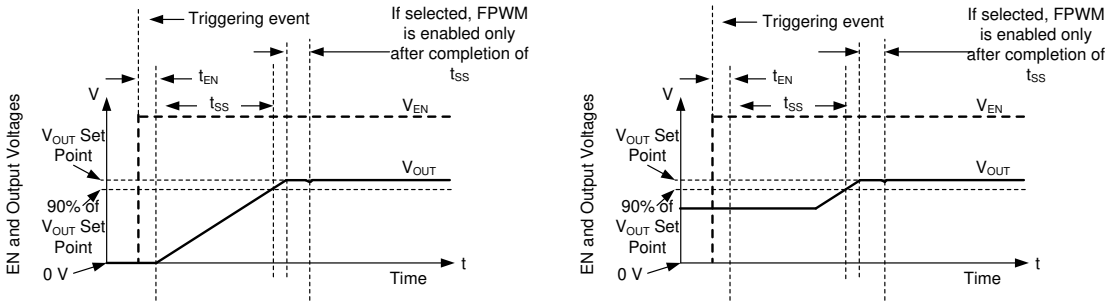


図 7-10. Soft Start With and Without Prebias Voltage

7.3.9.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.

- If the device is set to FPWM, the device continues to operate in that mode during the recovery from dropout. If output voltage was suddenly pulled up by an external supply, the LMR66430-EP can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

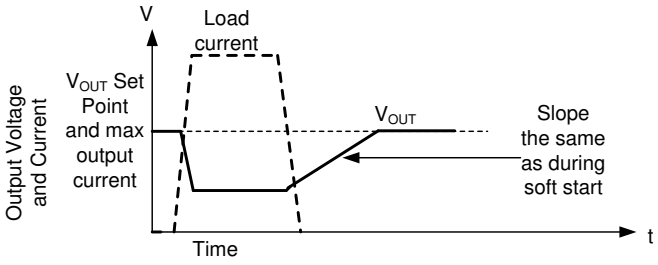


図 7-11. Recovery from Dropout

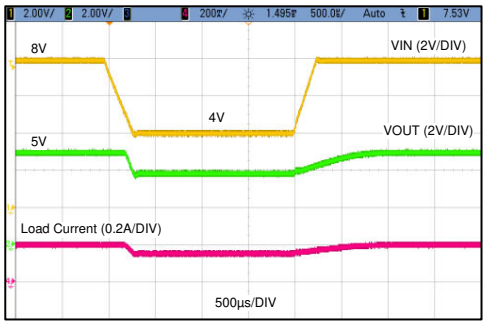


図 7-12. Typical Output Recovery from Dropout from 8V to 4V

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the set point is removed, the output climbs at the same speed as during start-up. 図 7-12 shows an example of this behavior.

7.3.10 Current Limit and Short Circuit

The device is protected from over current conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs. High-side MOSFET over current protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through the switch is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This limit is called the low-side current limit, I_{VALMAX} in 図 7-13. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

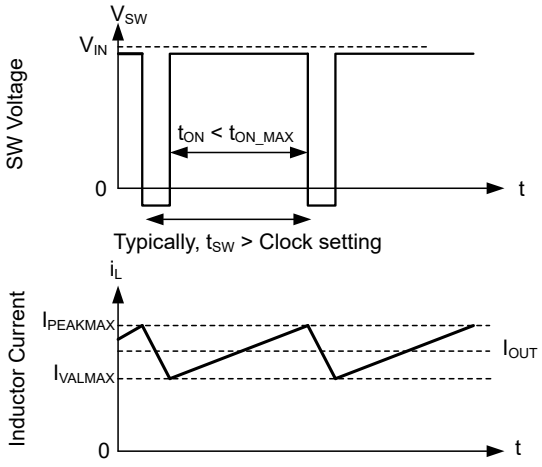


図 7-13. Current Limit Waveforms

Because the current waveform assumes values between $I_{PEAKMAX}$ and I_{VALMAX}, the maximum output current is very close to the average of these two values unless duty factor is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

The LMR66430-EP employs hiccup over current protection if there is an extreme overload, and the following conditions are met:

- Output voltage is below approximately 0.4 times the output voltage set point.
- Greater than t_{SS} has passed since soft start has started.
- The part is not operating in dropout, which is defined as having a minimum off time controlled duty cycle.

In hiccup mode, the device shuts down and attempts to soft start after t_{HICCUP}. Hiccup mode helps reduce the device power dissipation under severe over current conditions and short circuits. See 図 7-14.

After the overload is removed, the device recovers as though in soft start; see 図 7-15.

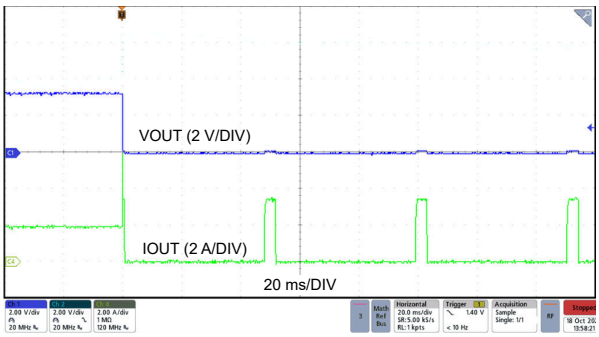


図 7-14. Hiccup Entry

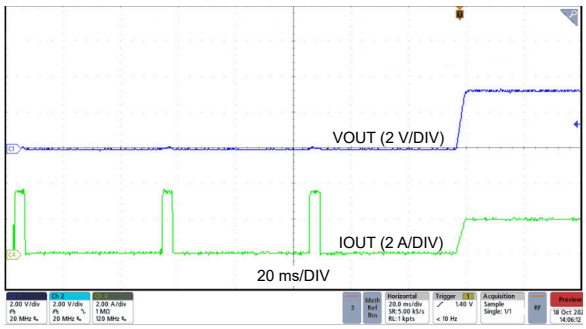


図 7-15. Hiccup Exit

7.3.11 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 153°C (typical). When the junction temperature falls below 153°C (typical), the device attempts another soft start.

While the device is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced

current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.3.12 Input Supply Current

The device is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The VOUT/FB pin in the fixed-output voltage variants is the input to the LDO that powers the majority of the control circuits. By connecting the VOUT/FB input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN}.

$$I_{Standby} = I_{QVIN(nonsw)} + I_{LKG-EN} + I_{BIAS} \times \frac{V_{OUT}}{\eta_{eff} \times V_{IN}} \quad (4)$$

where

- $I_{Standby}$ is the total standby (switching) current consumed by the operating (switching) buck converter when unloaded.
- $I_{QVIN(nonsw)}$ is the non-switching current drawn from the V_{IN} terminal. See セクション 6.5 for details.
- I_{LKG-EN} is current drawn by the EN terminal. Include this current if EN is connected to VIN. See セクション 6.5 for details.
- I_{BIAS} is the non-switching bias current drawn by the BIAS LDO. See セクション 6.5 for details.
- η_{eff} is the light-load efficiency of the buck converter. η_{eff} = 0.8 can be used under normal operating conditions.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4V, both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 250nA.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3V typical. The precision enable circuitry is ON after VCC is above the UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above the precision enable threshold. The device also employs UVLO protection. If the VCC voltage is below the UVLO level, the output of the converter is turned off.

7.4.3 Active Mode

The device is in active mode whenever the EN pin is above $V_{EN-VOUT}$, V_{IN} is high enough to satisfy V_{INMIN}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows the device to start up when the applied input voltage exceeds the minimum V_{INMIN}.

In active mode, depending on the load current, input voltage, and output voltage, the device is in one of five modes:

- *Continuous conduction mode (CCM)* with fixed switching frequency when load current is above half of the inductor current ripple
- *Auto mode* – light load operation: PFM when switching frequency is decreased at very light load
- *FPWM mode* – light load operation: Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple
- *Minimum on time*: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- *Dropout mode*: When switching frequency is reduced to minimize voltage dropout

7.4.3.1 CCM Mode

The following operating description of the device refers to セクション 7.2 and to the waveforms in 図 7-16. In CCM, the device supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (5)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (6)$$

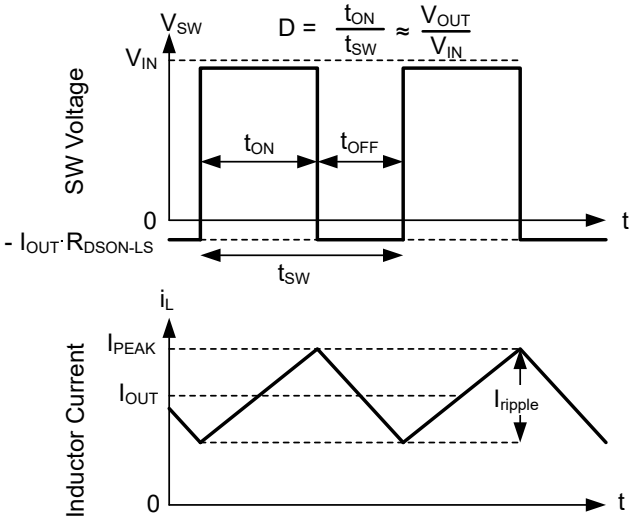


図 7-16. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.3.2 Auto Mode – Light Load Operation

The LMR66430-EP can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. Note that for output voltages between 1V and 2V multi-pulsing behavior can be observed on the switch node waveform when the device transitions from PFM to PWM mode. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the device operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

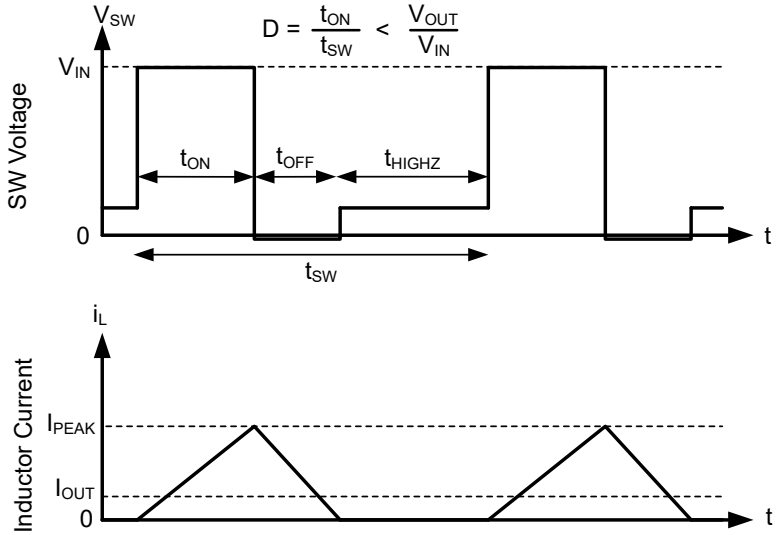
The light load operation is employed in the device only in auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation. See 図 7-17.
- Frequency reduction. See 図 7-17.

Note that while these two features operate together to improve light load efficiency, these features operate independently.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



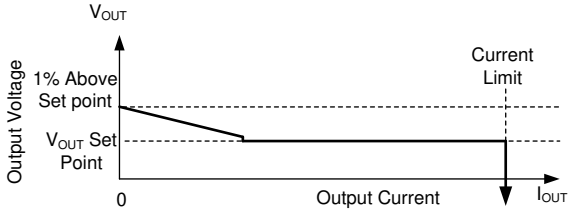
In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM, which is equivalent to the statement that diode emulation is active.

図 7-17. PFM Operation

The device has a minimum peak inductor current setting (see $I_{PEAKMIN}$ in the *Electrical Characteristics*) while in auto mode. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.3.2.2 Frequency Reduction

The device reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



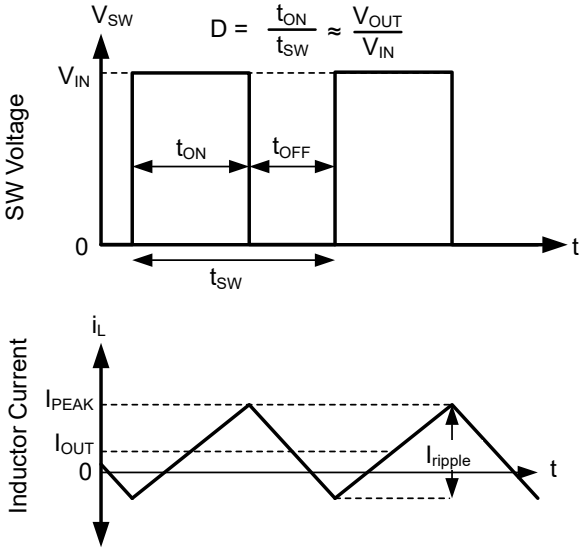
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

図 7-18. Steady State Output Voltage Versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM mode can be used to reduce or eliminate this offset.

7.4.3.3 FPWM Mode – Light Load Operation

In FPWM mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see the *Electrical Characteristics* for reverse current limit values.



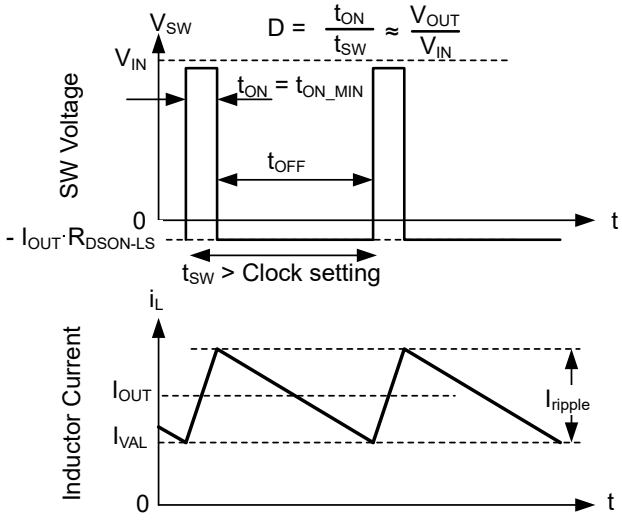
In FPWM mode, continuous conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

図 7-19. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults that involve output being pulled up.

7.4.3.4 Minimum On-Time (High Input Voltage) Operation

The device continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This action is accomplished by using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because the on time is fixed at the minimum value, this type of operation resembles that of a device using a constant on-time (COT) control scheme; see the following figure.

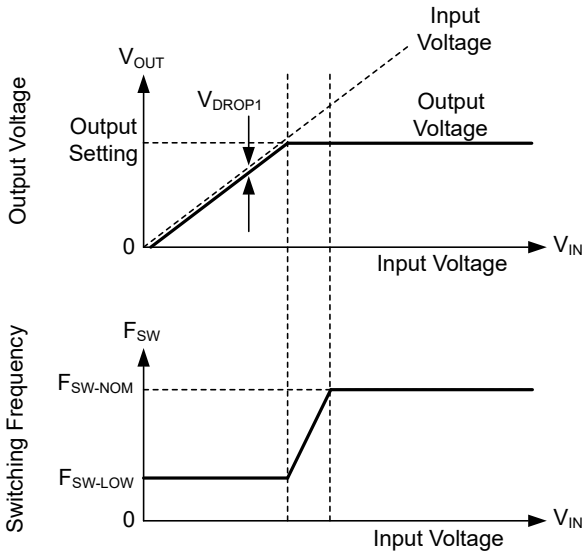


In valley control mode, minimum inductor current is regulated, not peak inductor current.

図 7-20. Valley Current Mode Operation

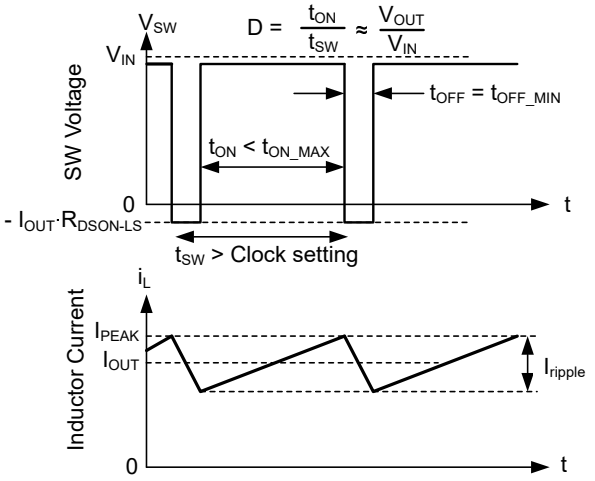
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency the duty cycle is limited by minimum off time. After this limit is reached, as shown in 図 7-22, and the clock frequency was to be maintained, the output voltage can fall. Instead of allowing the output voltage to drop, the device extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on time, t_{ON-MAX}, of approximately 9µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. As shown in 図 7-21, if input voltage is low enough so that output voltage cannot be regulated even with an on time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP1}. For additional information on recovery from dropout, refer to 図 7-11.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at F_{SW-LOW} which is approximately 110kHz, input voltage tracks output voltage.

図 7-21. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

図 7-22. Dropout Waveforms

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR66430-EP step-down DC-to-DC converters are typically used to convert a higher DC voltage to a lower DC voltage. The LMR66430-EP supports a maximum output current of 3A. The following design procedure can be used to select components for the LMR66430-EP.

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All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

As a quick-start guide, 表 8-1 provides typical component values for a range of the most common output voltages.

表 8-1. Typical External Component Values for Adjustable Output LMR66430-EP

f_{SW} (kHz) (1)	V_{OUT}	L (µH)	Nominal C_{OUT} (Rated Capacitance)	Minimum C_{OUT}(Effective Capacitance)(2)	R_{FBT} (kΩ)(3)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF} (4)
400	3.3V	10	3 × 22µF	60µF	100	43.2	4.7µF	0.1µF	1µF	33pF
1000		4.7								
2200		2.2	2 × 22µF	40µF						
400	5V	10	3 × 22µF	60µF	100	24.9				
1000		4.7								
2200		2.2	2 × 22µF	40µF						

(1) Inductor values are calculated based on typical V_{IN} = 12V.
(2) Minimum C_{OUT} values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) For R_{FBT} and R_{FBB} values outside the range stated above, see セクション 7.3.7.
(4) See セクション 8.2.3.8 for more information.

表 8-2. Typical External Component Values for Fixed Output LMR66430-EP

f_{SW} (kHz) (1)	V_{OUT}	L (µH)	Nominal C_{OUT} (Rated Capacitance)	Minimum C_{OUT}(Effective Capacitance)(2)	R_{FBT}	R_{FBB} (3)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3V	10	3 × 22µF	60µF	0	DNP	4.7µF	DNP	1µF	DNP
1000		4.7	3 × 22µF							
2200		2.2	2 × 22µF	40µF						

(1) Inductor values are calculated based on typical V_{IN} = 12V.
(2) Minimum C_{OUT} values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) DNP = Do Not Populate.

8.2.1 LMR66430-EP Design Guide

図 8-1 illustrates a (fixed) 3.3V output design with LMR66430MB3RXBNEP. The design procedure that follows must be mimicked for any LMR66430-EP design. Guidance is given for different design parameters than this particular design and orderable used. Please read this section in entirety.

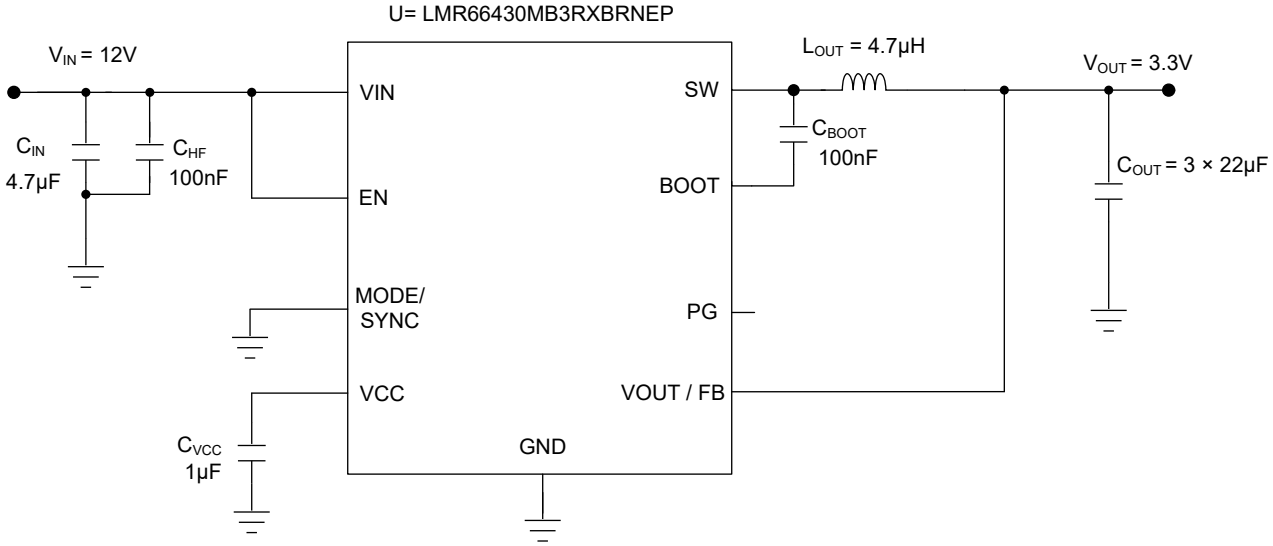


図 8-1. LMR66430-EP, 1MHz, (Fixed) 3.3V Application Circuit

8.2.2 Design Requirements

セクション 8.2.3 provides a detailed design procedure based on 表 8-3.

表 8-3. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12V (4V to 36V)
Output voltage	3.3V
Output current	0A to 3A
Switching frequency	1000kHz

8.2.3 Detailed Design Procedure

The following design procedure applies to 図 8-1 and 表 8-2.

8.2.3.1 Choosing the Switching Frequency

The switching frequency selection has an impact on several items in the design. Two aspects which are often looked at are design size and efficiency. A higher switching frequency results in smaller, external passives, with the tradeoff of increased power dissipation.

LMR66430-EP offers two orderables (セクション 4). LMR66430MB3RXBRNEP is used in this design example. The device operates at 1MHz, nominally, when operated in auto mode. The mode can be configured for FPWM to allow 1MHz, CCM operation, even at light-loads. LMR66430R3RXBRNEP allows for synchronization to an external clock as well. Refer to the MODE/SYNC section and specifications for more information.

This design requires 3A, peak load current. At 12VIN, 3.3VOUT (fix), with a 3A load, the power dissipation is 1.5W (図 8-5). 図 8-12 shows that a total power dissipation of 1.5W (inductor and IC) causes the case temperature to rise approximately 55°C above ambient. Assuming minimal, additional power loss at hot temperature, the design must be operable up to 85°C, as the ambient temperature plus the case temperature rise (approximate junction temperature) is below the maximum junction rating. This does assume that the end-design has similar thermal performance to the EVM. If hypothesized that the design has poorer thermal performance to the EVM, please consult 図 8-3. This figure shows how board thermal performance is impacted by shrinking the copper board area on all layers in a 4-layer PCB.

LMR66430MB3RXBRNEP operates at a fixed 1MHz frequency. In the case the power dissipation is found to be unsatisfactory for design requirements consider selecting LMR66430R3RXBRNEP, which can be configured for a lower switching frequency to reduce power dissipation. If neither is a feasible option, consult with TI to find an alternative power solution.

8.2.3.2 Setting the Output Voltage

LMR66430-EP can be configured for a fixed, 3.3V output or an adjustable output with an external feedback divider. LMR66430MB3RXBRNEP can output 3.3V by connecting V_{OUT} / FB directly to the output capacitor. Refer to *Output Voltage Selection* for information on how to configure LMR66430-EP for adjustable output voltage.

8.2.3.3 Inductor Selection

The buck inductor inductance and power rating must be considered. The inductance is selected so the peak-to-peak ripple current and is between 20% to 40% (K = 0.2 to 0.4) of the device rated current (example 3A for LMR66430-EP). This design uses a ripple factor K, of 0.2, having 式 7 yield a standard value of 4.7µH.

$$L_{OUT} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} = \frac{(12V - 3.3V)}{1MHz \times 0.2 \times 3} \times \frac{3.3V}{12V} \cong 4.7\mu H \quad (7)$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{PEAKMAX}$ (see the *Electrical Characteristics*). This size makes sure that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low

value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{VALMAX}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, there are more core losses at frequencies above about 1MHz.

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a general rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

8.2.3.4 Output Capacitor Selection

LMR66430-EP allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Refer to 表 8-1 and 表 8-2 for 5V and 3.3V output capacitor values. Based on 表 8-2, for a fixed 3.3V output design, the user can choose the recommended 3 × 22µF ceramic output capacitor for this example.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic capacitor placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1nF to 100nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

8.2.3.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7µF is required on the input of the LMR66430-EP. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. For this example, a 4.7µF, 50V, X7R (or better) ceramic capacitor is chosen, in addition to a lower ESL, 100nF capacitor in parallel.

Using an electrolytic capacitor on the input in parallel with the ceramic capacitor is often desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from the following equation and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

8.2.3.6 C_{BOOT}

The LMR66430-EP requires an external, high quality, 0.1µF capacitor placed between the BOOT and SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. TI recommends a 16V, X7R, MLCC capacitor.

8.2.3.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1µF, 16V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see セクション 7.3.4). A value in the range of 10kΩ to 100kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3V; see the *Electrical Characteristics* for limits.

8.2.3.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to make sure that the desired output voltage is established when configuring for adjustable output voltages. 式 9 must be followed to make sure C_{FF} remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}/1V}}{1.2E6} \tag{9}$$

This design utilizes the device in fixed output configuration. A feed-forward capacitor is integrated onto the IC along with the feedback divider and as a result, an external one is not needed.

8.2.3.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This needed can be accomplished by using the circuit shown in 図 8-2. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then 式 10 and 式 11 are used to calculate R_{ENT} and V_{OFF}, respectively.

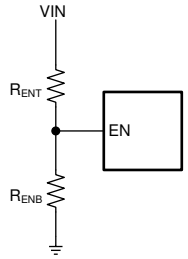


図 8-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \tag{10}$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{EN-VOUT}}\right) \tag{11}$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

This design has EN tied to VIN pin. The device attempts to regulate to 3.3V when the V_{IN} voltage exceeds V_{INMIN} (rising) and EN voltage exceeds $V_{EN-VOUT}$ (*Electrical Characteristics*). The output voltage can be below the setpoint if V_{IN} is close in value to V_{OUT} due to I-R drops in the circuit and a duty cycle which is slightly below 100%.

8.2.3.10 Maximum Ambient Temperature

The LMR66430-EP dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device, and PCB combination. The maximum junction temperature for the LMR66430-EP must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 12 shows the relationships between the important parameters. See that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current.

The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. For more information, refer to the *Semiconductor and IC Package Thermal Metrics* application report.

This design case temperature is measured in 図 8-12. The temperature gradient between top case and junction is often only a few degrees (celsius), so this measurement can determine the thermal margin on a given design

$$I_{OUT}\Big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \tag{12}$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The IC junction temperature can be estimated for a given operating condition using 式 13.

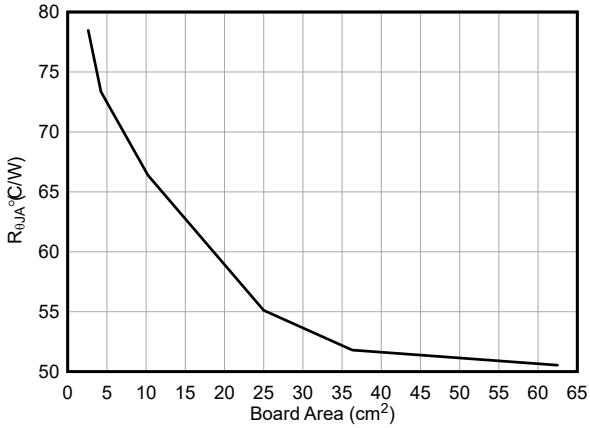
$$T_J \cong T_A + R_{\theta JA} \times \text{IC Power Loss} \tag{13}$$

where

- T_J is the IC junction temperature (°C).
- T_A is the ambient temperature (°C).
- $R_{\theta JA}$ is the thermal resistance (°C/W).
- IC power loss is the power loss for the IC (W).

The IC power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance.

The following figure is provided to estimate the thermal resistance of the IC for a particular board area.



The device operating conditions are as follows: $12V_{IN}$, $3.3V_{OUT}$, 3A load, 2.2MHz, 23ºC ambient (Pdiss =1.9W). 4 layer board, GND plane on mid-layer one, 2.8mil thick copper on each layer. $R_{\theta JA}$ is power dependent, so careful analysis is required.

図 8-3. $R_{\theta JA}$ vs Board Area

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application report
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- *Semiconductor and IC Package Thermal Metrics* application report
- *Thermal Design Made Simple with LM43603 and LM43602* application report
- *PowerPAD™ Thermally Enhanced Package* application report
- *PowerPAD™ Made Easy* application report
- *Using New Thermal Metrics* application report
- *PCB Thermal Calculator*

8.2.4 Application Curves

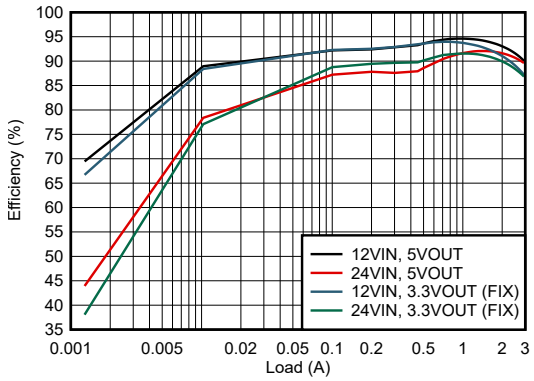


図 8-4. LMR66430MB3RBXNEP Efficiency (Mode = Auto)

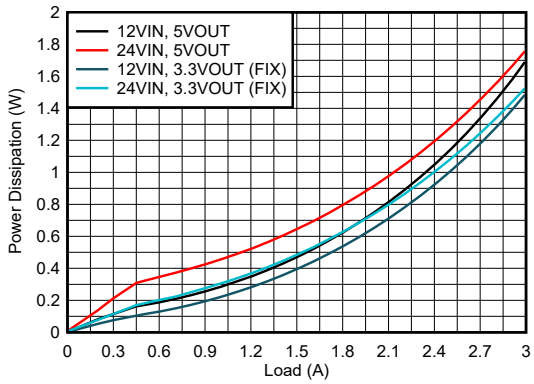


図 8-5. LMR66430MB3RBXNEP Power Dissipation (Mode = Auto)

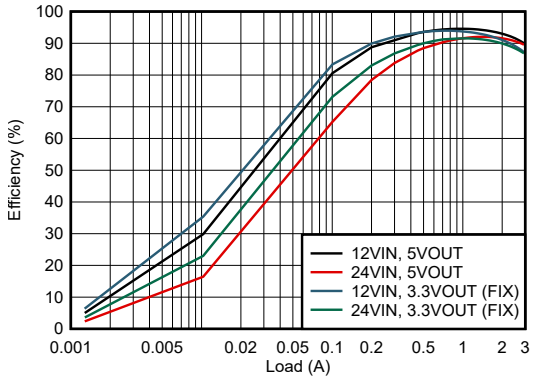


図 8-6. LMR66430MB3RBXNEP Efficiency (Mode = FPWM)

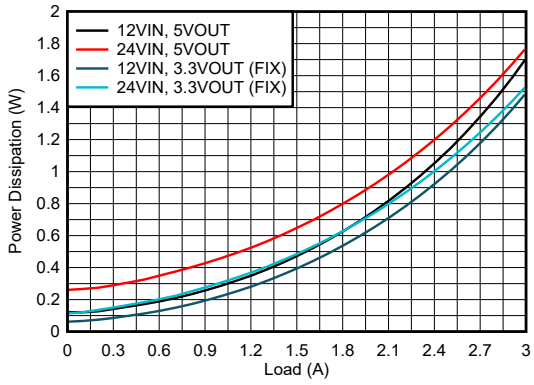
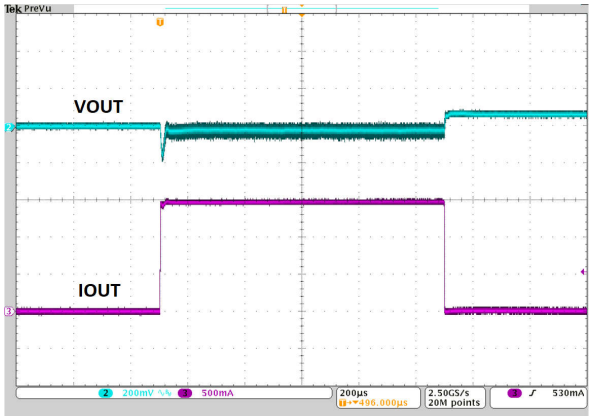


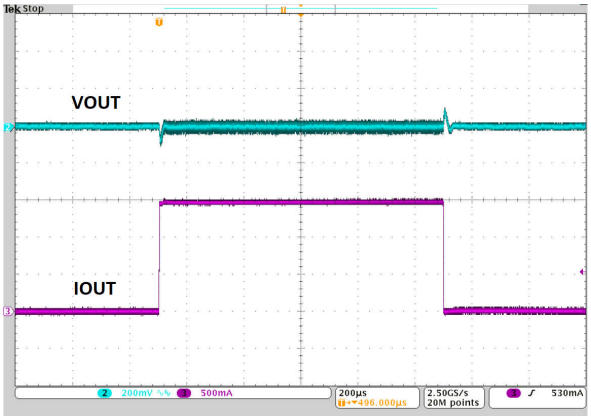
図 8-7. LMR66430MB3RBXNEP Power Dissipation (Mode = FPWM)



LMR66430MB3RBXNEP
0A to 1.5A,1A/µs

V_{OUT} = 3.3V (Fix)
Mode = auto

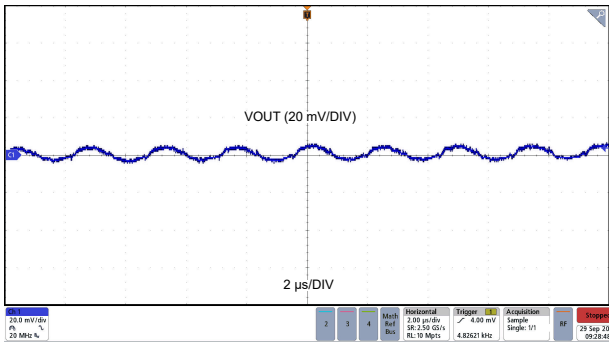
図 8-8. Load Transient



LMR66430MB3RBXNEP
0A to 1.5A,1A/µs

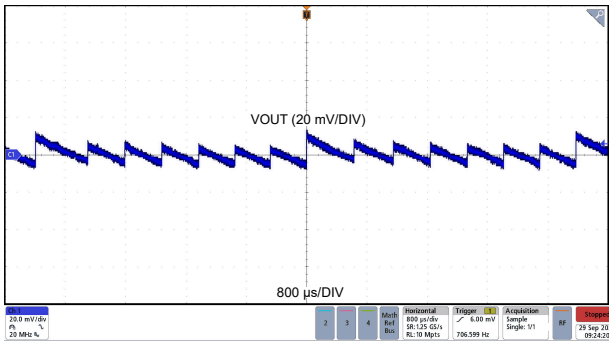
V_{OUT} = 3.3V (Fix)
Mode = FPWM

図 8-9. Load Transient



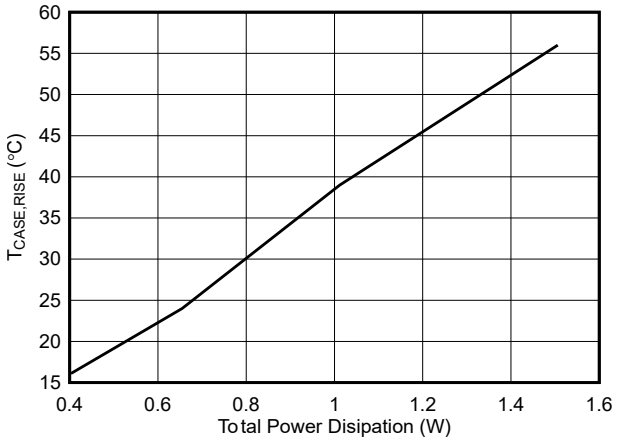
LMR66430MB3RBXNEP 3A load

図 8-10. Output Voltage Ripple



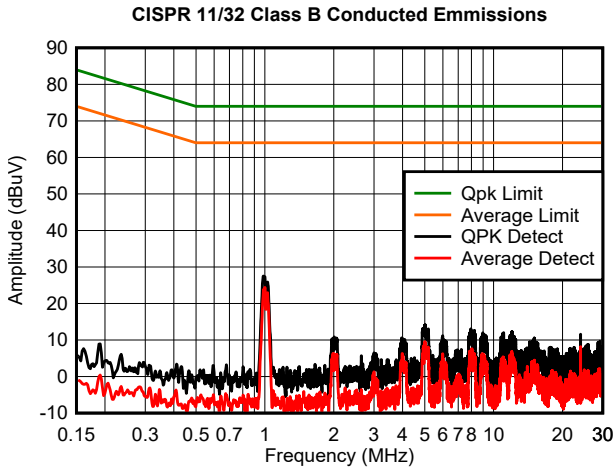
LMR66430MB3RBXNEP 0A load

図 8-11. Output Voltage Ripple



IC	Inductor	Ambient Temperature
LMR66430MB3RBXNEP	XGL5030-472	22°C

図 8-12. LMR66430-2EVM Thermal Performance



V_{IN} = 12V	V_{OUT} = 3.3V	Fsw = 1MHz
Load = 3A	LMR66430-2EVM	FB1=5.6µH, C5 = 4.7µF

図 8-13. CISPR 11/32, Class B, Conducted EMI

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make a project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Specifications* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with the following equation.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (14)$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This usage can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 8-14. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible

to reduce the parasitic inductance. 図 8-15 shows a recommended layout for the critical components of the LMR66430-EP.

- *Place the input capacitors as close as possible to the VIN and GND terminals.*
- *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
- *Place C_{BOOT} close to the device with short and wide traces to the BOOT and SW pins* If an external C_{BOOT} capacitor is desired.
- *Place the feedback divider as close as possible to the V_{OUT} / FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to V_{OUT} / FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
- *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat-sinking.* As stated in セクション 8.2.3.10, enough copper area must be used to make sure of a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep the switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies* application report
- *Simple Switcher PCB Layout Guidelines* application report
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

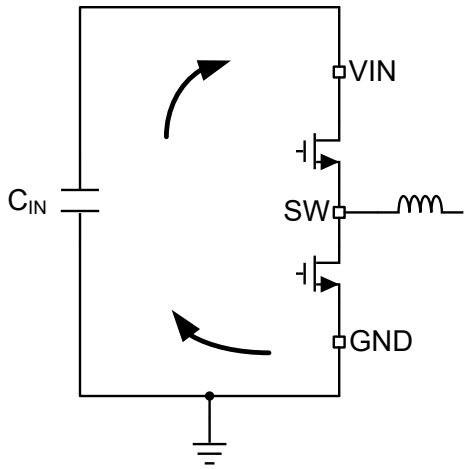


図 8-14. Current Loops With Fast Edges

8.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See 図 8-15 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2oz / 1oz / 1oz / 2oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

8.5.2 Layout Example

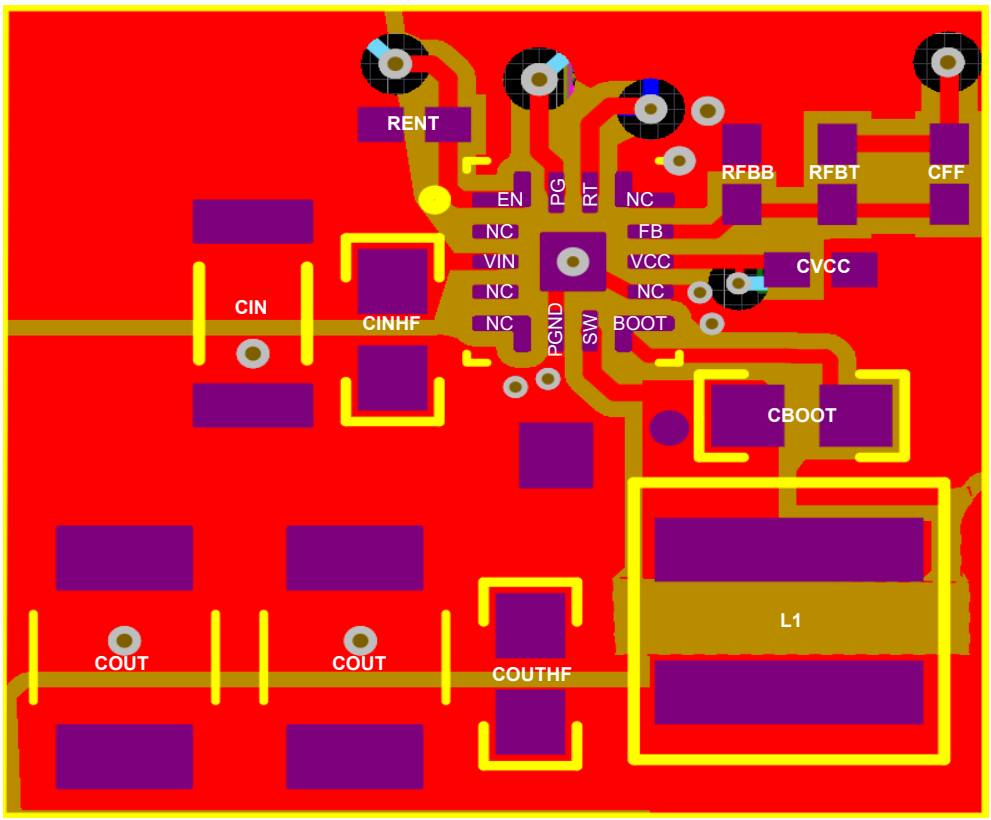


図 8-15. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Device Nomenclature

図 9-1 shows the device naming nomenclature of the LMR66430-EP. See セクション 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

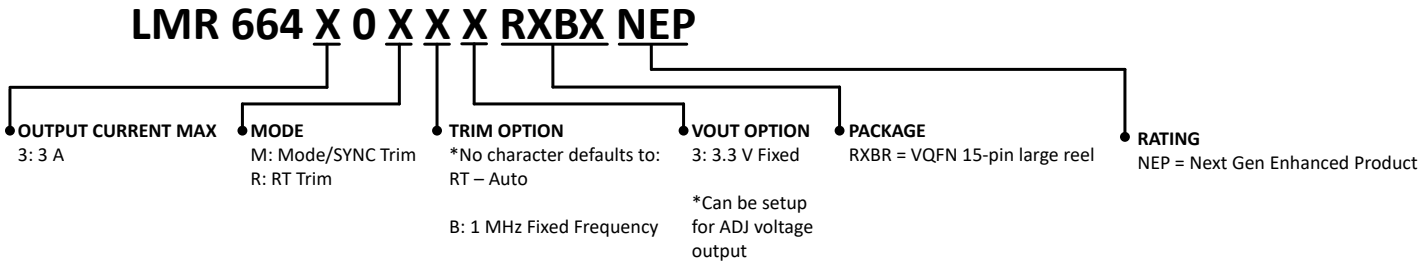

図 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight* application report
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Simple Switcher PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

9.3 ドキュメントの更新通知を受け取る方法

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

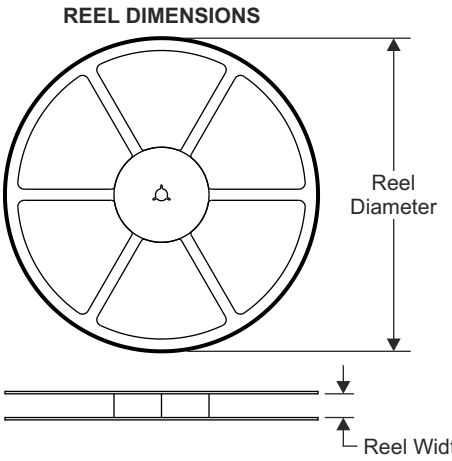
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

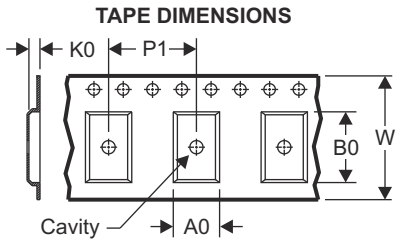
DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

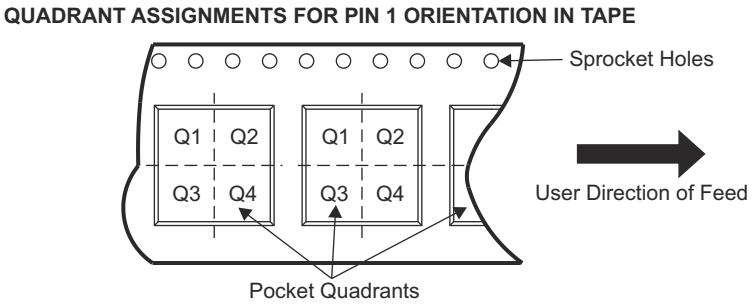
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



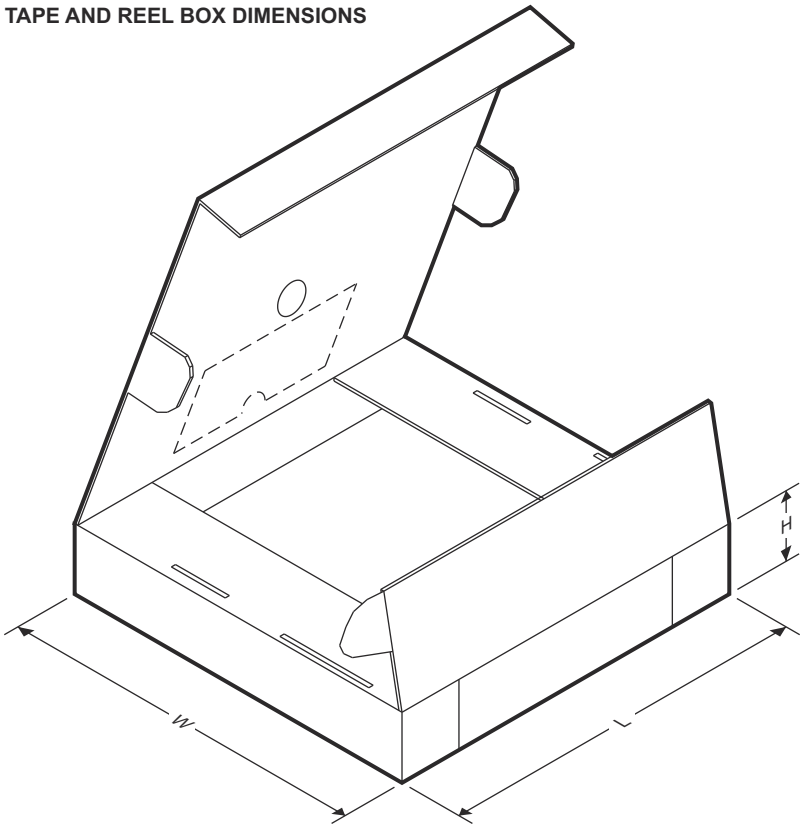


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR66430MB3RXBRNEP	VQFN-FCRLF	RXB	14	3000	330.0	12.4	2.9	2.9	1.3	8.0	12.0	Q2
LMR66430R3RXBRNEP	VQFN-FCRLF	RXB	14	3000	330.0	12.4	2.9	2.9	1.3	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR66430MB3RXBRNEP	VQFN-FCRLF	RXB	14	3000	367.0	367.0	35.0
LMR66430R3RXBRNEP	VQFN-FCRLF	RXB	14	3000	367.0	367.0	35.0

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR66430MB3RXBRNEP	Active	Production	VQFN-FCRLF (RXB) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	MB3NE
LMR66430MB3RXBRNEP.A	Active	Production	VQFN-FCRLF (RXB) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	MB3NE
LMR66430R3RXBRNEP	Active	Production	VQFN-FCRLF (RXB) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	R3NE
LMR66430R3RXBRNEP.A	Active	Production	VQFN-FCRLF (RXB) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	R3NE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMR66430-EP :

- Catalog : LMR66430
- Automotive : LMR66430-Q1

NOTE: Qualified Version Definitions:

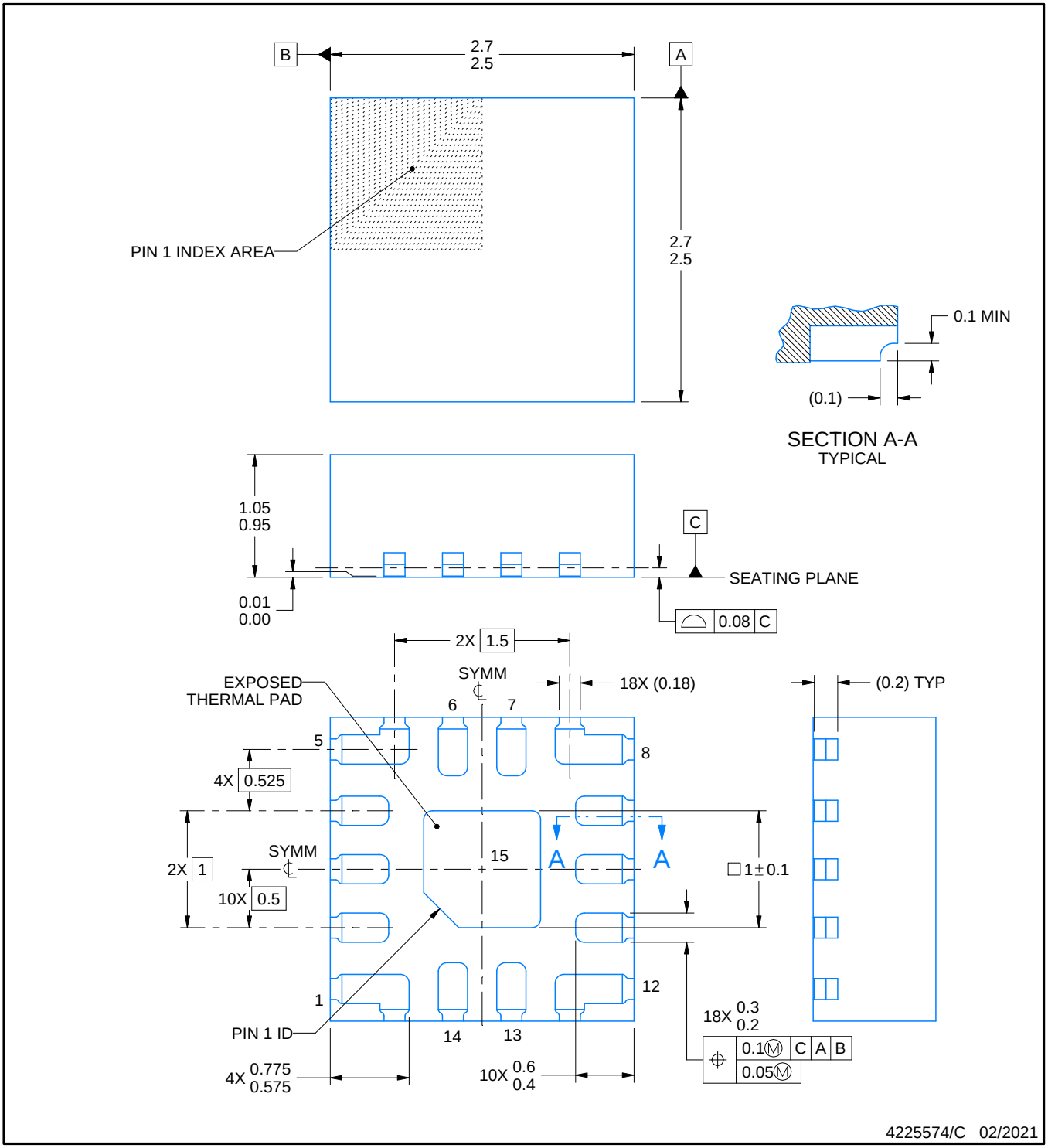
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

RXB0014A

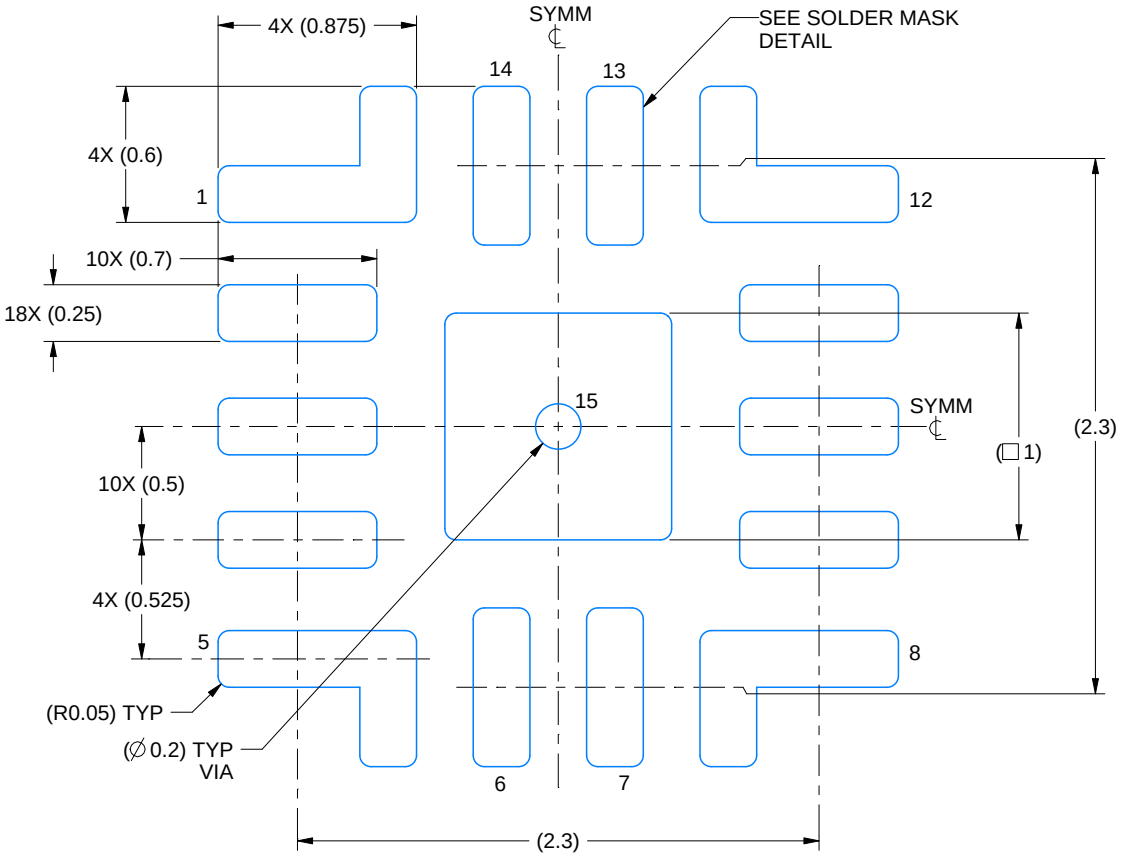
VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

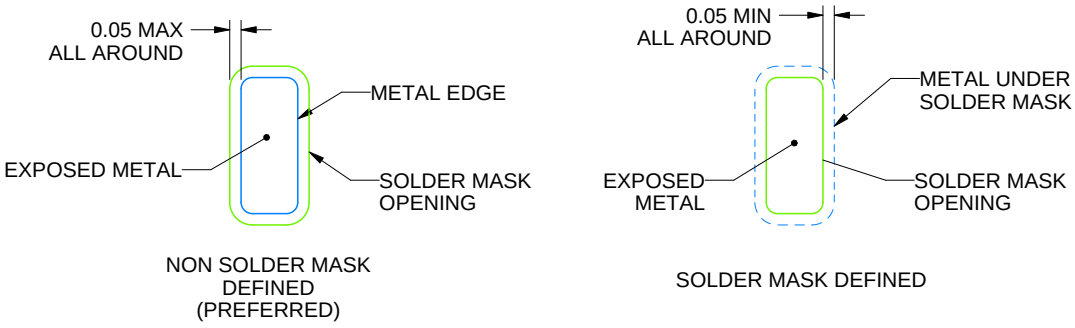


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

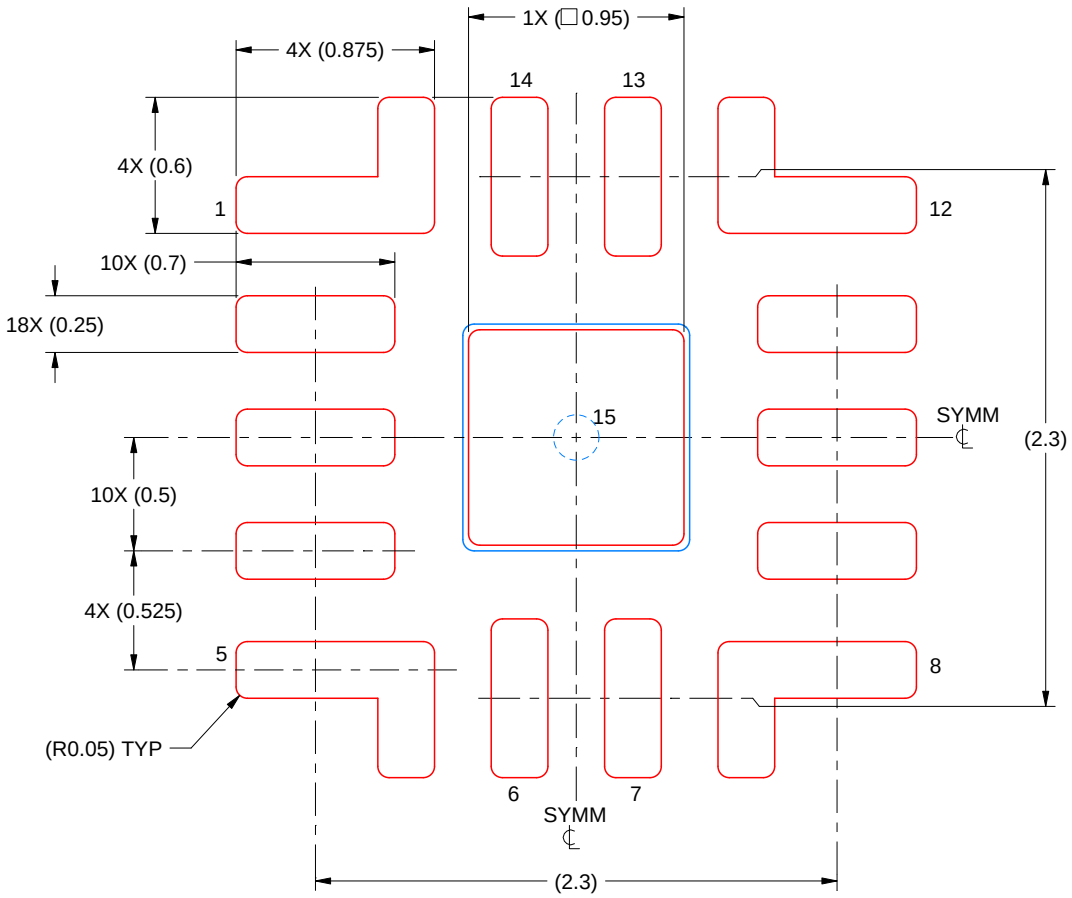


SOLDER MASK DETAILS

4225574/C 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 15
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225574/C 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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