LMR33640 SIMPLE SWITCHER® 3.8～36V、4A 同期整流降圧型コンバータ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な産業用アプリケーション向けの構成
  - 入力電圧範囲：3.8V～36V
  - 出力電圧範囲：1V～24V
  - ピーク電流モード制御
  - 接合部温度範囲：-40℃～+125℃
  - 使いやすい SOIC パッケージ
- スケーラブルな産業用電源に最適
  - 次の製品とピン互換
    - LMR33610、LMR33620、LMR33630 (36V、1A、2A、3A)
    - LMR36510、LMR36520 (65V、1A、2A)
  - 400kHz と 1MHz の周波数
  - 補償機能を内蔵しているためソリューションの小型化、コストの低減、設計の簡素化が可能
- 高効率のソリューション
  - ピーク効率：95% 超
  - 低いシャットダウン時静止電流：5μA
  - 低い動作時静止電流：24μA
- 柔軟なシステム・インターフェイス
  - パワー・グッド・フラグおよび高精度イネーブル
- WEBENCH® Power Designer により、LMR33640 を使用するカスタム設計を作成
- TPSM53604 モジュールを使用して、開発期間を短縮

2 アプリケーション

- モーター・ドライブ・システム：ドローン、AC インバータ、VF ドライブ、サーボ
- 工場およびビルディング・オートメーション・システム：PLC、HMI、HVAC システム、エレベータのメイン制御パネル
- 広い入力電圧範囲の DC/DC 電源

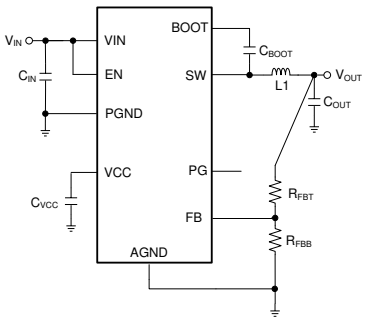
3 概要

LMR33640 SIMPLE SWITCHER® レギュレータは使いやすい同期整流降圧 DC/DC コンバータで、堅牢な産業用アプリケーション向けに、クラス最高の効率を実現しています。最大 36V の入力から最大 4A の負荷電流を駆動でき、軽負荷時の効率と出力精度も優れています。パワー・グッド・フラグや高精度イネーブルなどの特長から、広範なアプリケーションにおいて、柔軟で使いやすいソリューションとなります。軽負荷時には、効率向上のため自動的に周波数をフォールドバックします。保護機能として、サーマル・シャットダウン、入力低電圧誤動作防止、サイクル単位の電流制限、ヒカップ短絡保護機能が搭載されています。統合と内部補償により、多くの外付け部品が不要で、PCB レイアウトが単純になるようにピン配置が設計されています。本デバイスの一連の機能は、広範な最終機器の実装が簡単になるよう設計されています。LMR33640 は LMR33610、LMR33620、LMR33630 (36V、1A/2A/3A)、LMR36510 (65V、1A)、LMR36520 (65V、2A) とピン互換性があり、拡張性の高い SIMPLE SWITCHER 電源ファミリを構成しています。そのため、基板レイアウトの変更に伴うコストと労力が最小限で済みます。LMR33640 は 8 ピンの HSOIC パッケージで供給されます。

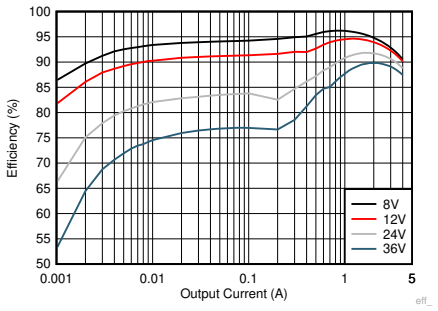
製品情報

部品番号	パッケージ(1) (1 ページ)	本体サイズ (公称)
LMR33640	HSOIC (8)	5.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



効率と出力電流の関係 V_{OUT} = 5V、400kHz、HSOIC

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2020) to Revision C (November 2020) **Page**

- *「特長」*に機能安全の箇条書き項目を追加.....1
- 文書全体にわたって表、図、相互参照の採番方法を更新.....1

Changes from Revision A (October 2019) to Revision B (May 2020) **Page**

- *「特長」に TPSM53604 のリンクを追加*.....1

Changes from Revision * (September 2019) to Revision A (October 2019) **Page**

- デバイスのステータスを事前情報から量産データに変更.....1

5 Device Comparison Table

DEVICE OPTION	RATED CURRENT	SWITCHING FREQUENCY
LMR33640ADDA	4 A	400 kHz
LMR33640DDDA	4 A	1000 kHz

6 Pin Configuration and Functions

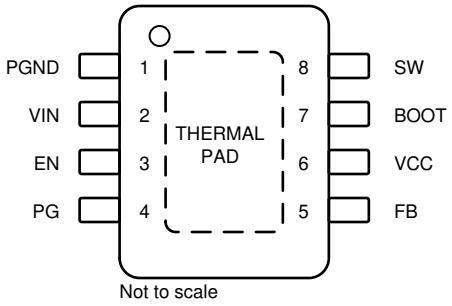


図 6-1. 8-Pin HSOIC with PowerPAD™ DDA Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	1	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
VIN	2	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND.
EN	3	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; *Do not* float.
PG	4	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
FB	5	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. *Do not* float. *Do not* ground.
VCC	6	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to PGND.
BOOT	7	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin.
SW	8	P	Regulator switch node. Connect to power inductor.
AGND	THERMAL PAD	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.
A = Analog, P = Power, G = Ground			

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	–0.3	38	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	FB to AGND	–0.3	5.5	
	PG to AGND(2)	0	22	
	AGND to PGND	–0.3	0.3	
	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 100-ns transients	–3.5	38	
	BOOT to SW	–0.3	5.5	
	VCC to AGND(4)	–0.3	5.5	
T_J	Junction temperature(3)	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
(3) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.
(4) Under some operating conditions the VCC LDO voltage may increase beyond 5.5V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±2500	V
		Charged-device model (CDM) (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating temperature range of –40°C to 125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN (2)	0	V_{IN}	
	PG(2)	0	18	
Adjustable output voltage	V_{OUT} (3)	1	24	V
Output current	I_{OUT}	0	4	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *セクション 7.5*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The maximum output voltage can be extended to 95% of V_{IN}; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information, see セクション 7.1.

THERMAL METRIC(1) (2)		LMR33640 DDA (HSOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see the セクション 7.1.

7.5 Electrical Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Minimum operating input voltage				3.8	V
I_Q	Non-switching input current; measured at VIN pin (2)	V_{FB} = 1.2 V		24	34	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	µA
ENABLE						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Hysteresis below V_{EN-H}; falling		100		mV
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
INTERNAL SUPPLIES						
VCC	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{BOOT-UVLO}$	Bootstrap voltage undervoltage lock-out threshold(3)			2.2		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage; ADJ option		0.985	1	1.015	V
I_{FB}	Current into FB pin; ADJ option	FB = 1 V		0.2	50	nA
CURRENT LIMITS						
I_{SC}	High-side current limit	LMR33640	4.8	5.5	6.2	A
I_{LIMIT}	Low-side current limit	LMR33640	3.9	4.5	5	A
$I_{PEAK-MIN}$	Minimum peak inductor current	LMR33640		0.824		A

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ZC}	Zero current detector threshold			-0.106		A
SOFT START						
t_{SS}	Internal soft-start time		2.9	4	6	ms
POWER GOOD (PG PIN)						
$V_{PG-HIGH-UP}$	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-HIGH-DN}$	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
$V_{PG-LOW-UP}$	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
$V_{PG-LOW-DN}$	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t_{PG}	Power-good glitch filter delay(1)		60		170	µs
R_{PG}	Power-good flag R_{DSON}	V_{IN} = 12 V, V_{EN} = 4 V		76	150	Ω
		V_{EN} = 0 V		35	60	
V_{IN-PG}	Minimum input voltage for proper PG function	50-µA, EN = 0 V			2	V
V_{PG}	PG logic low output	50-µA, EN = 0 V, V_{IN} = 2V			0.2	V
OSCILLATOR						
f_{SW}	Switching frequency		860	1000	1140	kHz
f_{SW}	Switching frequency		340	400	460	kHz
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	DDA package		95	160	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	DDA package		66	110	mΩ

(1) See *セクション 8.3.1* for details.
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge C_{BOOT}.

7.6 Timing Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

			MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time	DDA package		75	108	ns
$t_{OFF-MIN}$	Minimum switch off-time	DDA package		50	85	ns
t_{ON-MAX}	Maximum switch on-time			7	9	µs

7.7 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. *These specifications are not ensured by production testing.*

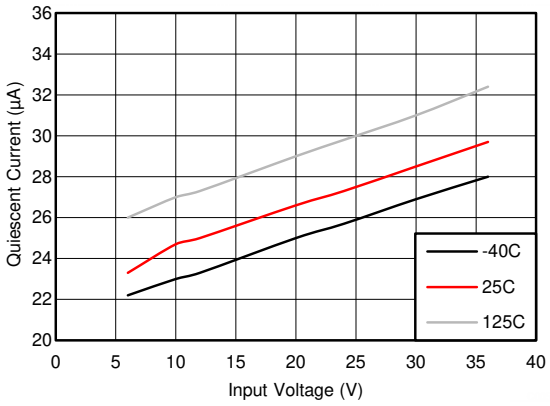
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range	V_{OUT} = 3.3 V, I_{OUT}= 0 A	3.8		36	V
V_{OUT}	Output voltage regulation for V_{OUT} = 5 V(1)	V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 0 A to 4 A	–1.6%		2.5%	
		V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 1 A to 4 A	–1.6%		1.5%	
	Output voltage regulation for V_{OUT} = 3.3 V(1)	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 0 A to 4 A	–1.6%		2.5%	
		V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 1 A to 4 A	–1.6%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ		25		µA
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5 V, I_{OUT} = 1A Dropout at –1% of regulation, f_{SW} = 140 kHz		150		mV
D_{MAX}	Maximum switch duty cycle(2)	V_{IN} = V_{OUT} = 12 V, I_{OUT} = 1 A		98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		165		°C
		Recovery temperature		148		°C

(1) Deviation is with respect to V_{IN} = 12 V, I_{OUT} = 1 A.

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / ($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$). D_{MAX} = $t_{ON\text{-}MAX}$ /($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$).

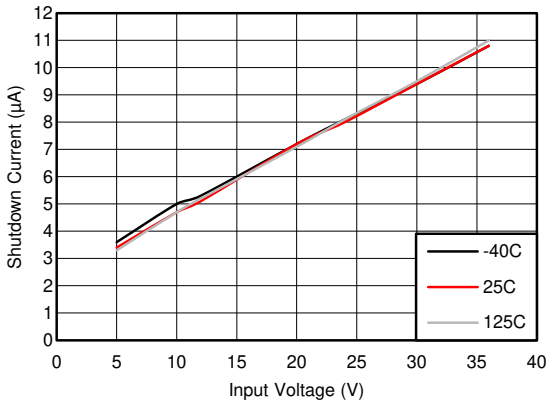
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: T_A = 25°C and V_{IN} = 12 V, f_{SW} = 400 kHz



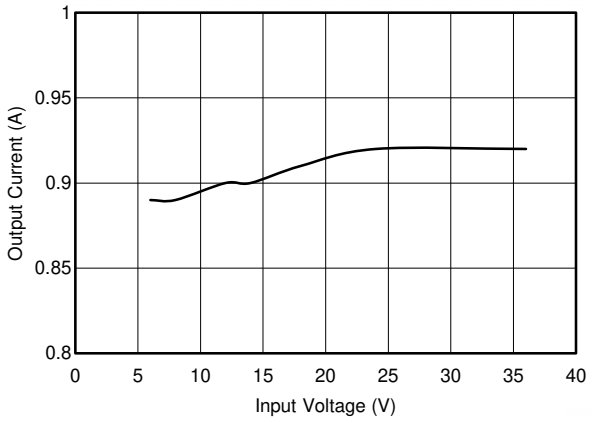
V_{FB} = 1.2 V

図 7-1. Non-Switching Input Supply Current



EN = 0 V

図 7-2. Shutdown Supply Current



V_{OUT} = 0 V f_S = 400 kHz See 図 9-21

図 7-3. Short-Circuit Output Current

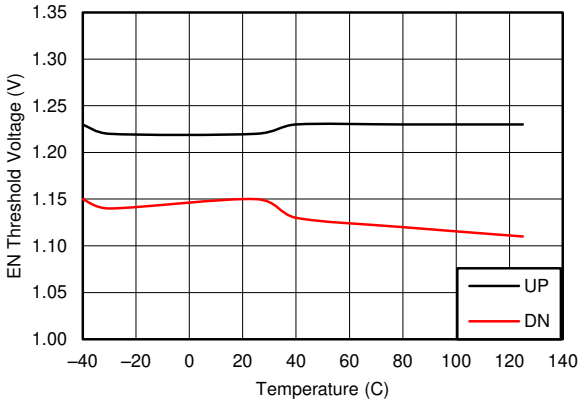
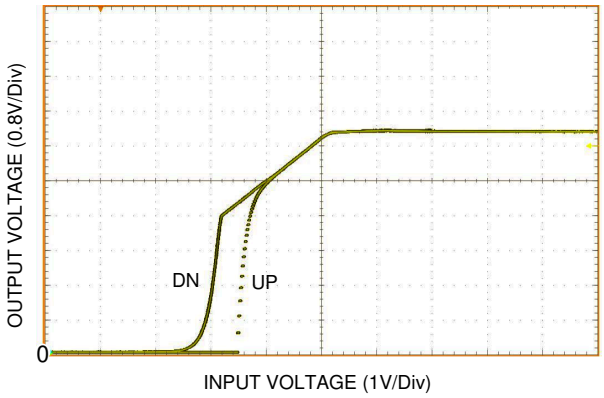
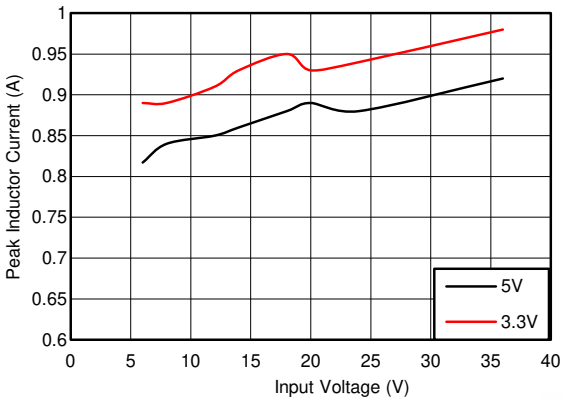


図 7-4. Precision Enable Thresholds



I_{OUT} = 1 mA See 図 9-21

図 7-5. UVLO Thresholds



I_{OUT} = 0 A V_{OUT} = 5 V See 図 9-21
f_{SW} = 400 kHz

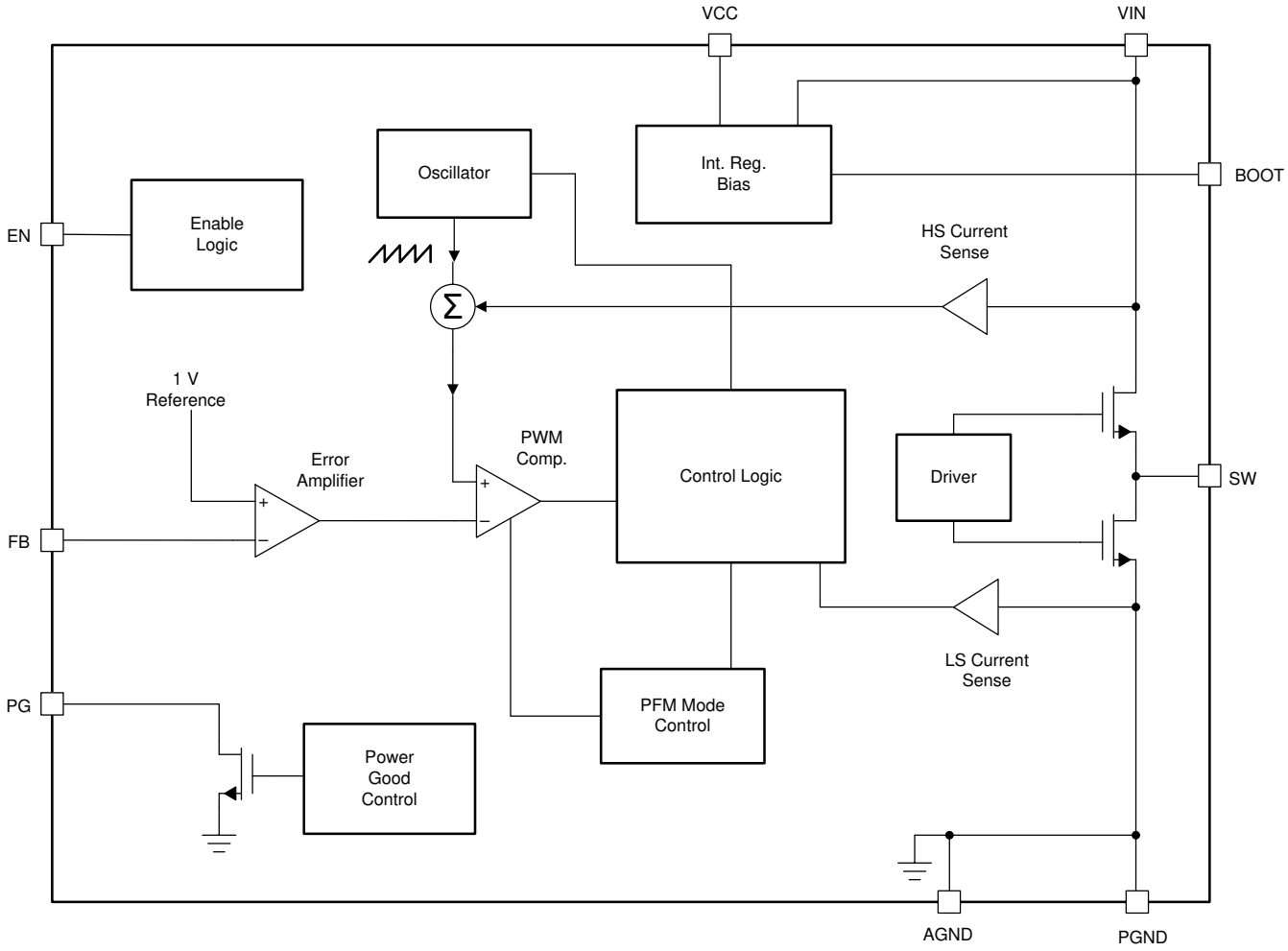
図 7-6. $I_{PEAK-MIN}$

8 Detailed Description

8.1 Overview

The LMR33640 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. Advanced high-speed circuitry allows the device to regulate from an input voltage of 36 V, while providing an output voltage of 3.3 V at a switching frequency of 400 kHz. The innovative architecture allows the device to regulate a 3.3 V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM, depending on the load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation, allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation, which reduces design time and requires fewer external components than externally compensated regulators.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33640 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in *セクション 7.5*. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to 図 8-1 and 図 8-2. During initial power up, a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open-drain NMOS and requires an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT} through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and approximately 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

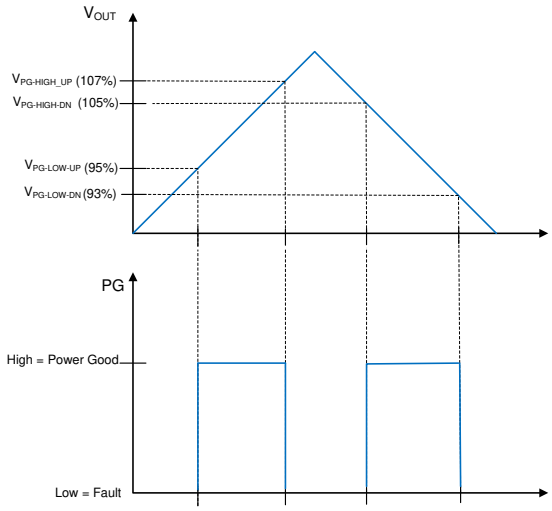


図 8-1. Static Power-Good Operation

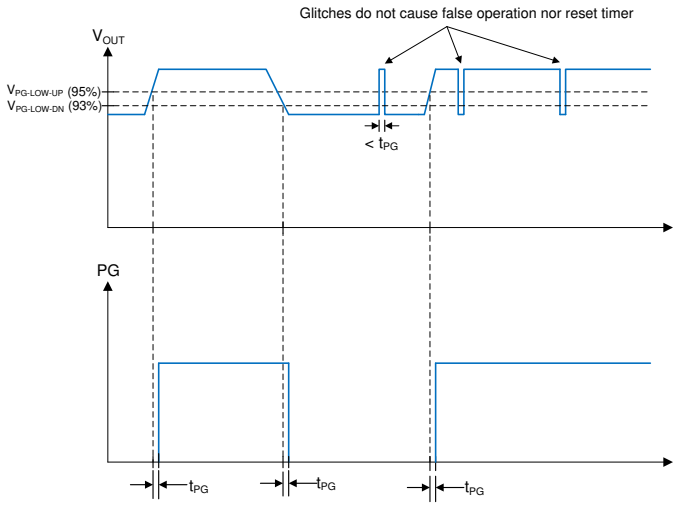


図 8-2. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see *セクション 9.2.2.9*). Applying a voltage greater than or equal to V_{EN-VCC_H} causes the device to enter standby mode, which powers the internal VCC, but does not produce an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and begin the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. 図 8-3 shows this behavior. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in *セクション 7.5*.

The LMR33640 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. 図 8-4 shows a typical start-up waveform, indicating typical timings. The rise time of the output voltage is about 4 ms (see *セクション 7.5*).

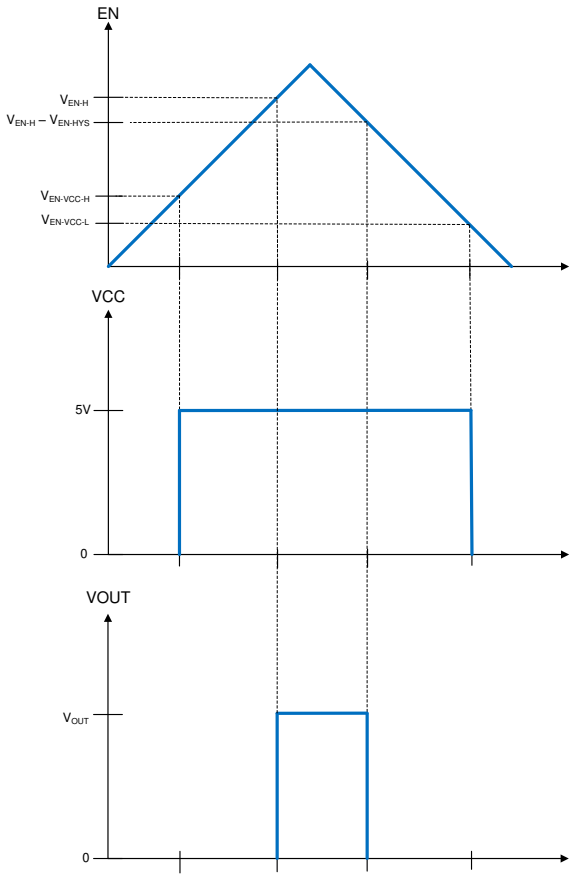


図 8-3. Precision Enable Behavior

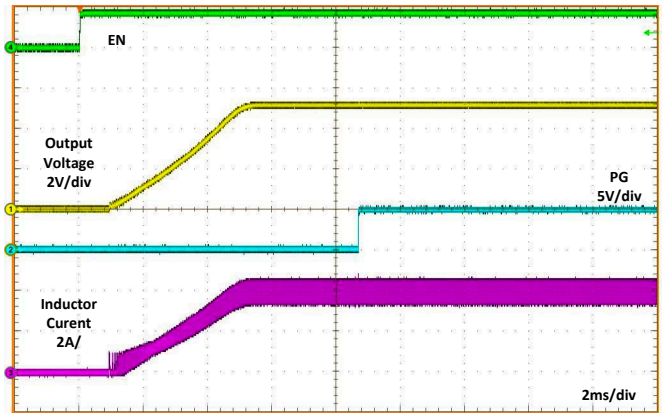


図 8-4. Typical Start-up Behavior V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 4 A

8.3.3 Current Limit and Short Circuit

The LMR33640 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current run-away during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the *Glossary*). The typical value of this current limit is found under I_{ZC} in *セクション 7.5*.

When the device is overloaded, the valley of the inductor current may not reach below I_{LIMIT}, (see セクション 7.5) before the next clock cycle. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, I_{SC} (see セクション 7.5), the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 式 1.

$$I_{OUT}|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If during current limit, the voltage on the FB input falls below about 0.4 V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for t_{HC} (see the *System Characteristics* section), or about 94 ms, and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in 図 8-5, as long as the short-circuit condition persists. This mode of operation reduces the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode (see セクション 7.8). Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in 図 8-6.

図 8-7 shows the overall output voltage versus the output current characteristic.

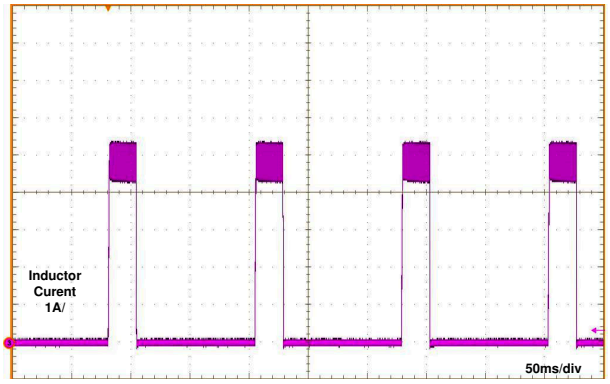


図 8-5. Inductor Current Burst in Short-Circuit Mode

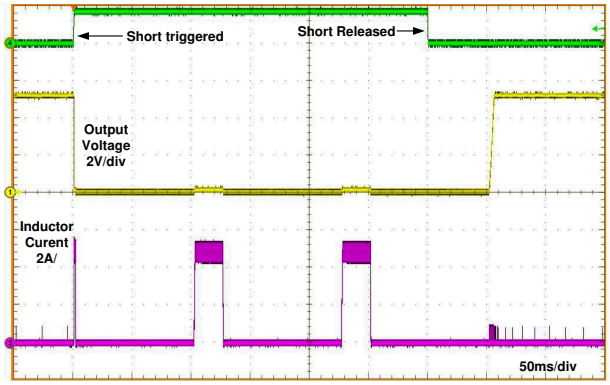


図 8-6. Short-Circuit Transient and Recovery V_{IN} = 12 V, V_{OUT} = 5 V

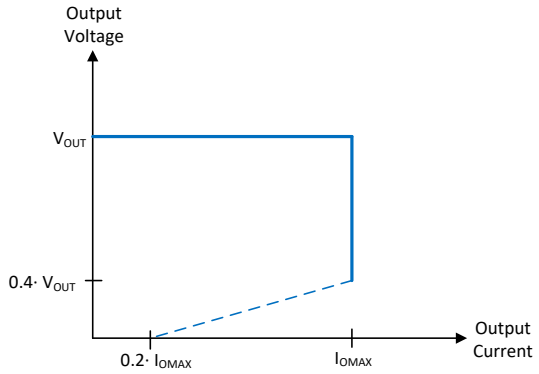


図 8-7. Output Voltage versus Output Current in Current Limit

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33640 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V, the device is ready to receive an EN signal and start up. When VCC falls below

approximately 3 V, the device shuts down, regardless of EN status. Since the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C, the device shuts down; re-start occurs when the temperature falls to about 148°C .

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in *セクション 9.2.3*. The output current at which the device changes modes depends on the input voltage, inductor value, and the output voltage. For output currents above the curve, the device is in PWM mode. For currents below the curve, the device is in PFM. The curves apply for a nominal switching frequency of 400 kHz and the BOM shown in 表 9-3. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode, the regulator operates as a constant frequency converter using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low-output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load. 図 8-8 and 図 8-9 show typical switching waveforms in PFM and PWM. See *セクション 9.2.3* for output voltage variation with load in auto mode.

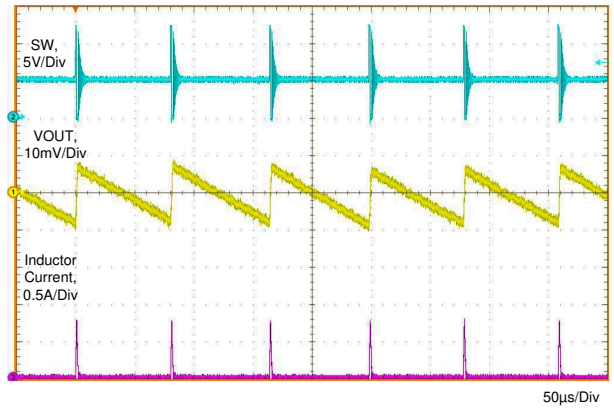


図 8-8. Typical PFM Switching Waveforms V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 10 mA

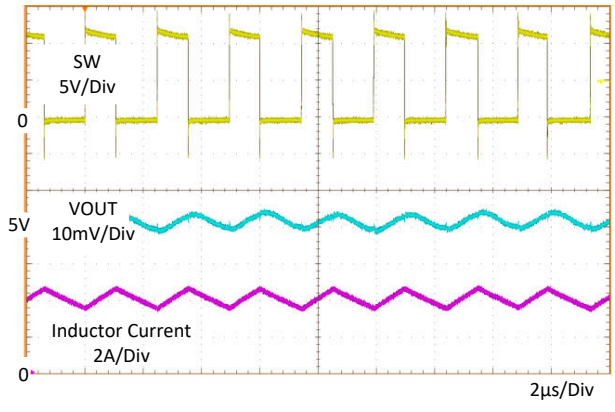


図 8-9. Typical PWM Switching Waveforms V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 4 A, f_S = 400 kHz

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value. Beyond this point, the switching can become erratic, and the output voltage can fall out of regulation. To avoid

this problem, the LMR33640 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical dropout characteristics can be found in 図 8-10, 図 8-11, and 図 8-12.

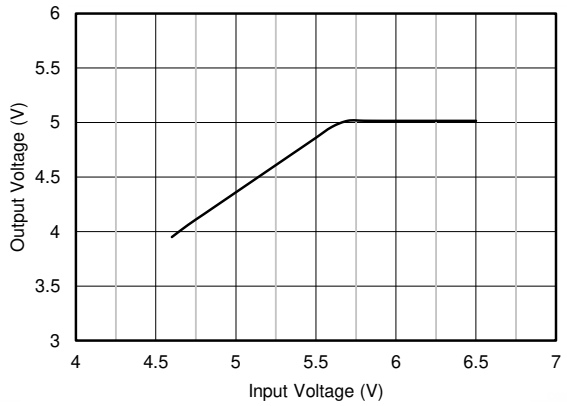


図 8-10. Overall Dropout Characteristic V_{OUT} = 5 V, I_{OUT} = 4 A

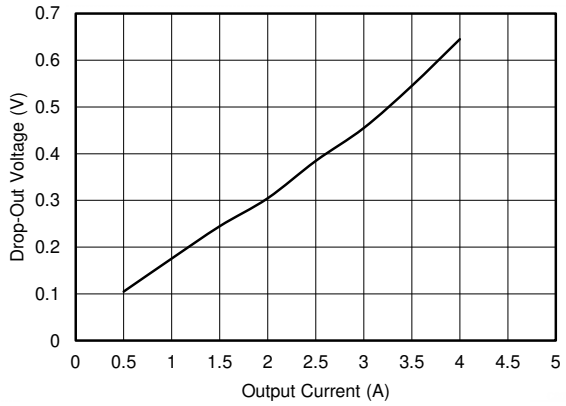


図 8-11. Typical Dropout Voltage vs Output Current in Frequency Fold-back f_{SW} = 140 kHz

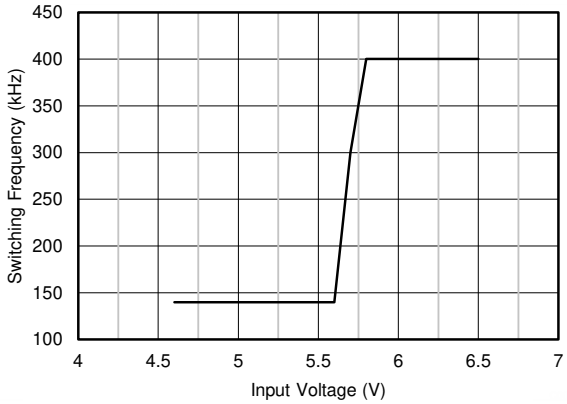


図 8-12. Typical Switching Frequency in Dropout Mode V_{OUT} = 5 V, f_{SW} = 400 kHz

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To extend the minimum controllable duty cycle, the LMR33640 automatically reduces the switching frequency when the minimum on-time limit is reached. This way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage before frequency foldback occurs is found in 式 2. The values of t_{ON} and f_{SW} can be found in *セクション 7.5*. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \quad (2)$$

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR33640 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 4 A. The following design procedure can be used to select components for the LMR33640. Alternately, the WEBENCH design tool can be used to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

Note

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

図 9-1 shows a typical application circuit for the LMR33640. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick-start guide, 表 9-1 provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application.

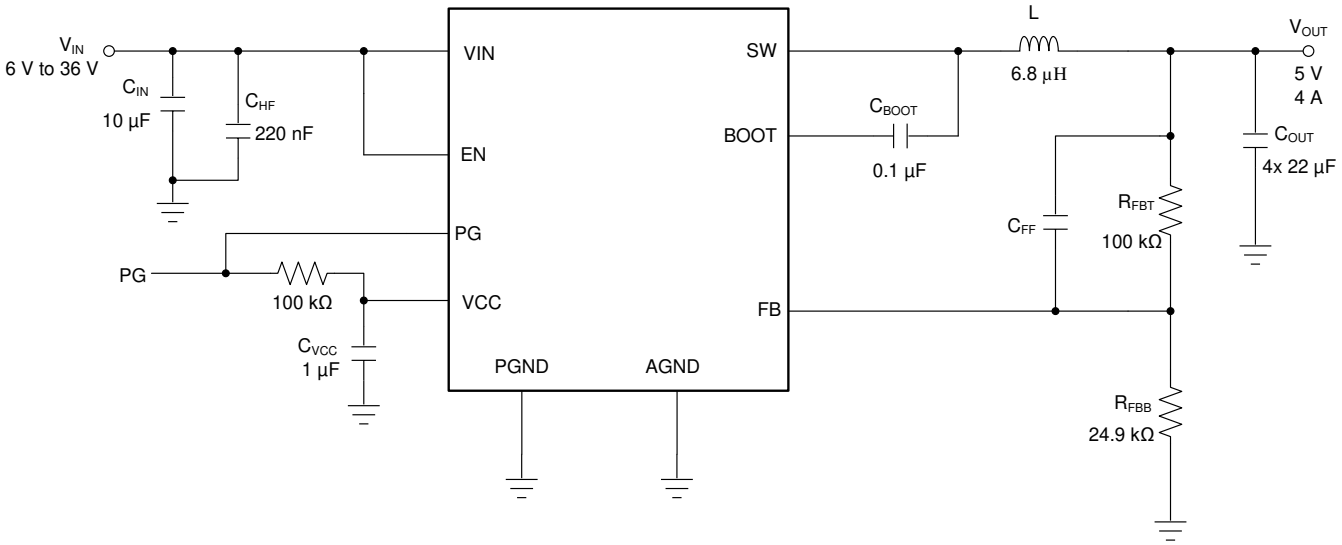


図 9-1. Example Application Circuit (400 kHz)

9.2.1 Design Requirements

表 9-1 provides the parameters for our detailed design procedure example.

表 9-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 4 A
Switching frequency	400 kHz

表 9-2. Typical External Component Values

f_{SW}(kHz)	V_{OUT} (V)	L (µH)	TYPICAL C_{OUT}	MINIMUM C_{OUT}	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN} + C_{HF}	C_{BOOT}	C_{VCC}
400	3.3	6.8	4 ×22 µF	3 ×22 µF	100 k	4.32 k	10 µF + 220 nF	100 nF	1 µF
400	5	6.8	4 ×22 µF	3 ×22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF
1000	3.3	3.3	3 ×22 µF	2 ×22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF
1000	5	3.3	3 ×22 µF	2 ×22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF

9.2.2 Detailed Design Procedure

The following design procedure applies to 図 9-1 and 表 9-1.

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR33640 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting the Output Voltage

The output voltage of LMR33640 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in *セクション 7.5*. The divider network is comprised of R_{FBT} and R_{FBB} and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity and reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBT}, then a feedforward capacitor must be used across this resistor to provide adequate loop-phase margin (see the *セクション 9.2.2.8* section). Once R_{FBT} is selected, use 式 3 to select R_{FBB}. V_{REF} is nominally 1 V (see *セクション 7.5* for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{3}$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must be used. 式 4 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.3, giving a calculated inductance of 6.08 µH. The next standard value of 6.8 µH is used.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{4}$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{SC}. This ensures that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT}. To avoid subharmonic oscillation, the inductance value must not be less than that given in 式 5. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must not be less than about 10% of the device maximum rated current under nominal conditions.

$$L \geq 0.23 \cdot \frac{V_{OUT}}{F_{SW}} \tag{5}$$

9.2.2.4 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements rather than the output voltage ripple. Use 式 6 to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which are required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D)\right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT}\left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)}\right)\right]}$$

$$D = \frac{V_{OUT}}{V_{IN}} \tag{6}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from セクション 9.2.2.3

Once the output capacitor and ESR have been calculated, 式 7 can be used to check the peak-to-peak output voltage ripple, V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \quad (7)$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example, a ΔV_{OUT} of ≤ 350 mV for an output current step of ΔI_{OUT} = 4 A is required. 式 6 gives a minimum value of about 80 µF and a maximum ESR of 77 mΩ. Assuming a 20% tolerance and a 10% bias de-rating, you arrive at a minimum capacitance of about 110 µF. This can be achieved with a bank of 4 × 22-µF, 16-V, ceramic capacitors in the 1210 case size or 5 × 22-µF for a worst case. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to build up the required value of capacitance. When using a mixture of aluminum and ceramic capacitors, use the minimum recommended value of ceramics and add aluminum electrolytic capacitors as needed.

In general, use a capacitor of at least 10 V for output voltages of 3.3 V or less, while a capacitor of 16 V or more must be used for output voltages of 5 V and above.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance must be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LMR33640. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 10-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated from 式 8 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

9.2.2.6 C_{BOOT}

The LMR33640 requires a boot-strap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function. A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see *セクション 7.5* for limits. Do not short this output to ground or any other external voltage.

9.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help mitigate this effect. Use 式 9 to estimate the value of C_{FF}. The value found with 式 9 is a starting point. Use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{9}$$

9.2.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 図 9-2. The input voltage at which the device turns on is designated V_{ON} while the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 10 is used to calculate R_{ENT} and V_{OFF}.

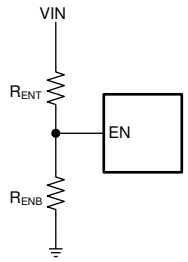


図 9-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right) \tag{10}$$

where

- V_{ON} = V_{IN} turnon voltage

- V_{OFF} = V_{IN} turnoff voltage

9.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the LMR33640 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum internal die temperature for the LMR33640 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in セクション 7.4 is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}\big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{11}$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature
- Air flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The HSOIC (DDA) package uses a die attach paddle or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of $R_{\theta JA}$ versus copper board area can be found in 図 9-3. The copper area given in the graph is for each layer; the top and bottom layers are 2 oz copper each, while the inner layers are 1 oz. 図 9-4 shows the typical curves of maximum output current versus ambient temperature This data was taken with a device and PCB combination, giving an $R_{\theta JA}$ as noted in the graph. Remember that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.

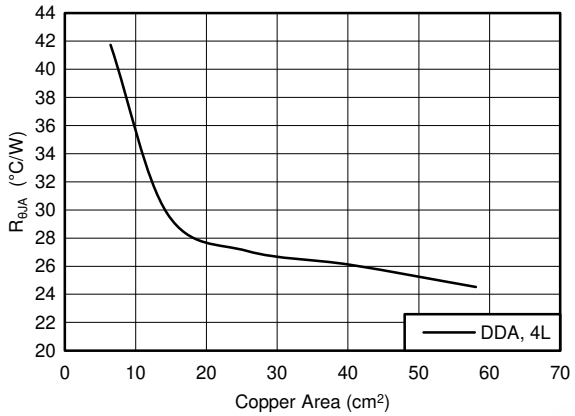


図 9-3. Typical $R_{\theta JA}$ versus Copper Area for a Four-Layer Board

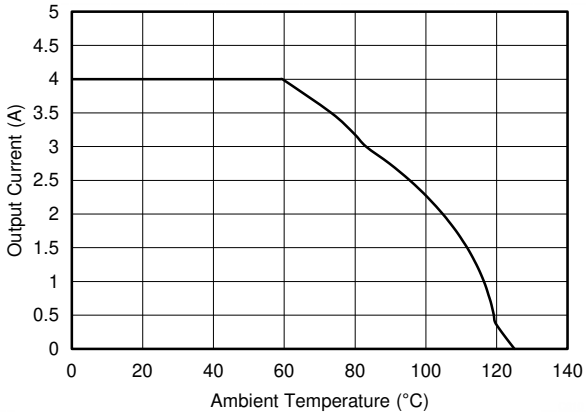


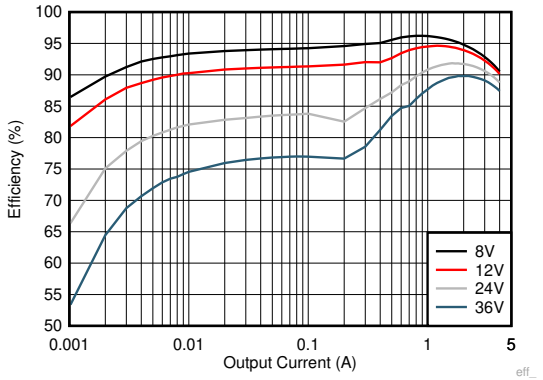
図 9-4. Maximum Output Current versus Ambient Temperature V_{IN} = 12 V, V_{OUT} = 5 V, $R_{\theta JA}$ = 30°C/W, f_{SW} = 400 kHz

Use the following resources as a guide to optimal thermal PCB design and to estimate $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight Not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43604 And LM43602 Application Report*
- *PowerPAD Thermally Enhanced Package Application Report*
- *PowerPAD Made Easy Application Report*
- *Using New Thermal Metrics Application Report*

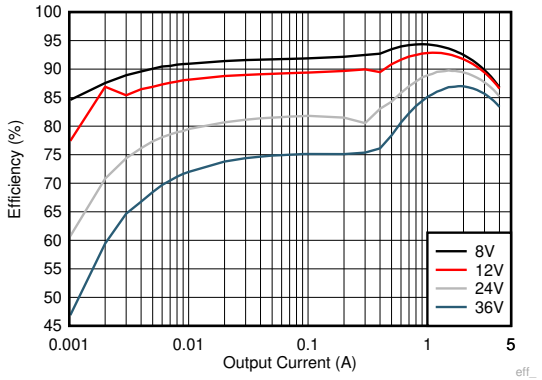
9.2.3 Application Curves

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. 図 9-21 shows the circuit with the appropriate BOM from 表 9-3.



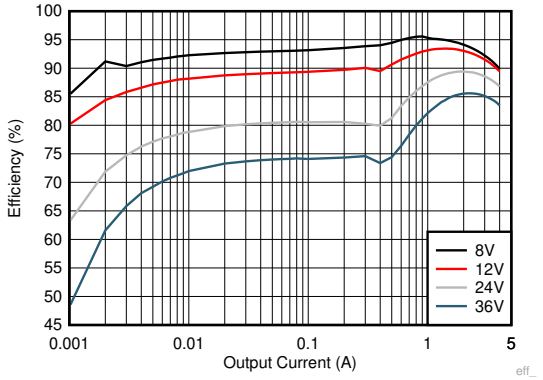
V_{OUT} = 5 V f_{SW} = 400 kHz

図 9-5. Efficiency



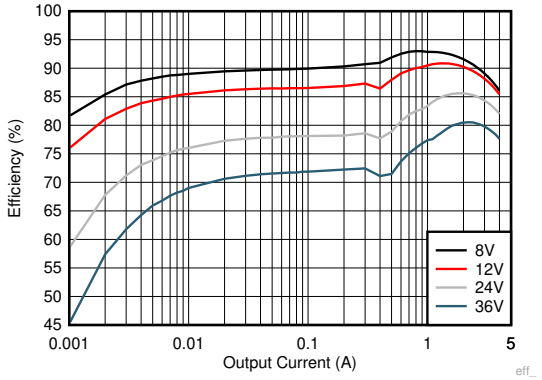
V_{OUT} = 3.3 V f_{SW} = 400 kHz

図 9-6. Efficiency



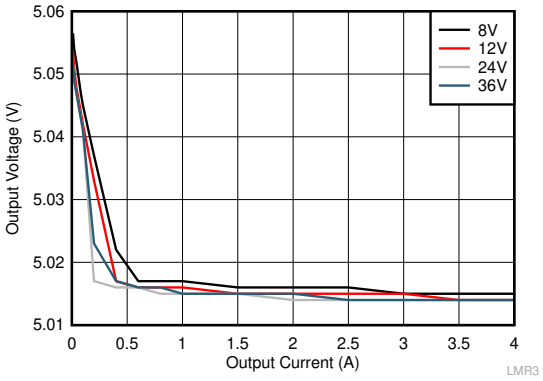
V_{OUT} = 5 V f_{SW} = 1000 kHz

図 9-7. Efficiency



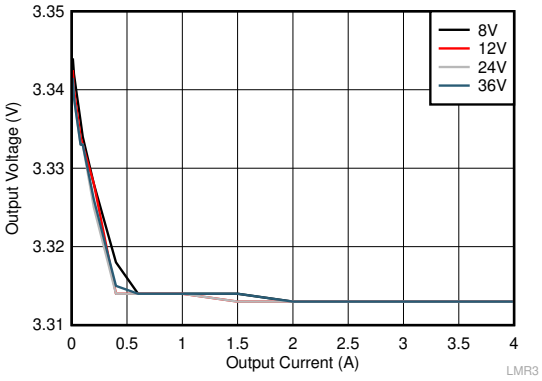
V_{OUT} = 3.3 V f_{SW} = 1000 kHz

図 9-8. Efficiency



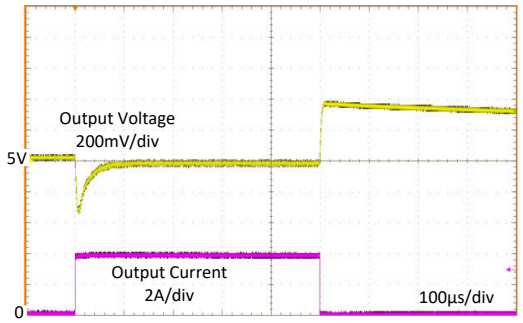
V_{OUT} = 5 V

図 9-9. Line and Load Regulation



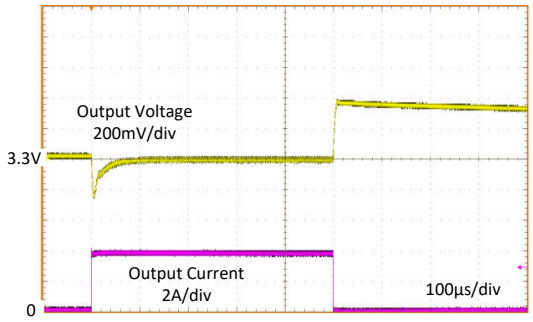
V_{OUT} = 3.3 V

図 9-10. Line and Load Regulation



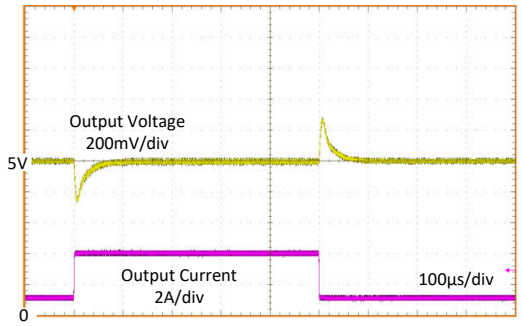
V_{IN} = 12 V
V_{OUT} = 5 V
f_{SW} = 400 kHz
I_{OUT} = 0 A to 4 A

図 9-11. Load Transient



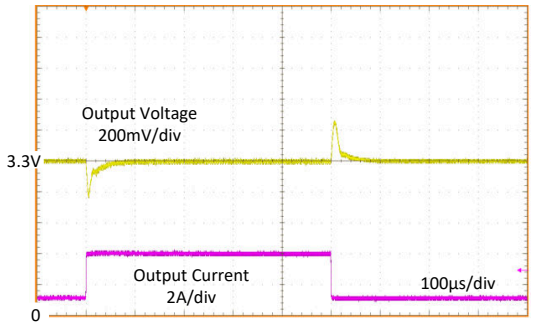
V_{IN} = 12 V
V_{OUT} = 3.3 V
f_{SW} = 400 kHz
I_{OUT} = 0 A to 4 A

図 9-12. Load Transient



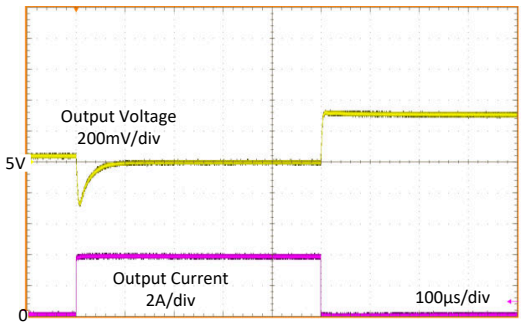
V_{IN} = 12 V
V_{OUT} = 5 V
f_{SW} = 400 kHz
I_{OUT} = 1 A to 4 A

図 9-13. Load Transient



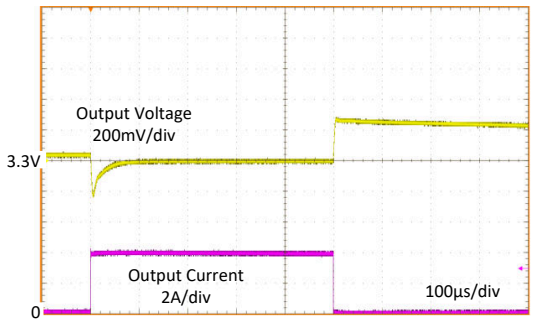
V_{IN} = 12 V
V_{OUT} = 3.3 V
f_{SW} = 400 kHz
I_{OUT} = 1 A to 4 A

図 9-14. Load Transient



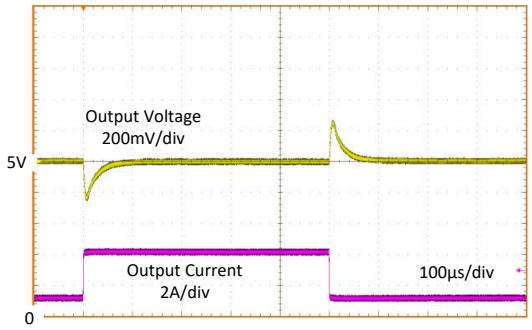
V_{IN} = 12 V
V_{OUT} = 5 V
f_{SW} = 1000 kHz
I_{OUT} = 0 A to 4 A

図 9-15. Load Transient



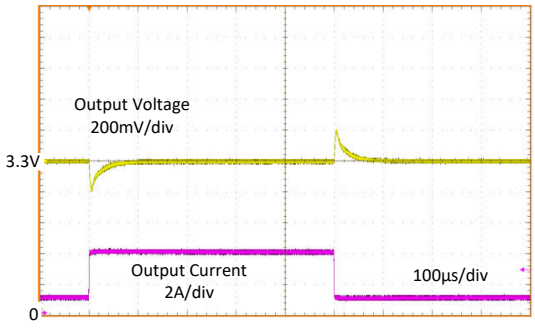
V_{IN} = 12 V
V_{OUT} = 3.3 V
f_{SW} = 1000 kHz
I_{OUT} = 0 A to 4 A

図 9-16. Load Transient



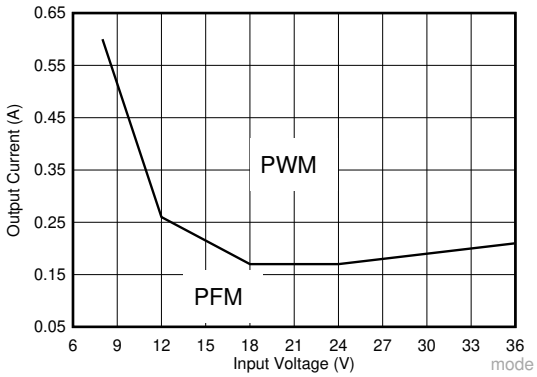
V_{IN} = 12 V V_{OUT} = 5 V
f_{SW} = 1000 kHz I_{OUT} = 1 A to 4 A

図 9-17. Load Transient



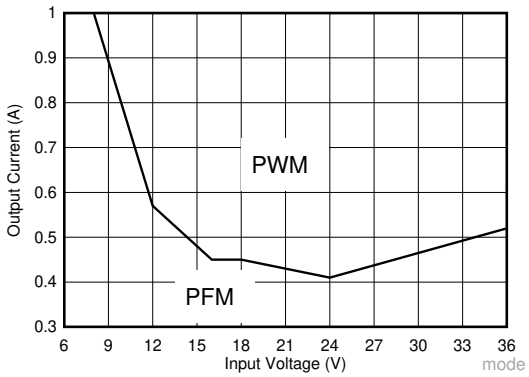
V_{IN} = 12 V V_{OUT} = 3.3 V
f_{SW} = 1000 kHz I_{OUT} = 1 A to 4 A

図 9-18. Load Transient



f_{SW} = 400 kHz V_{OUT} = 5 V

図 9-19. Load Transient



f_{SW} = 1000 kHz V_{OUT} = 5 V

図 9-20. Load Transient

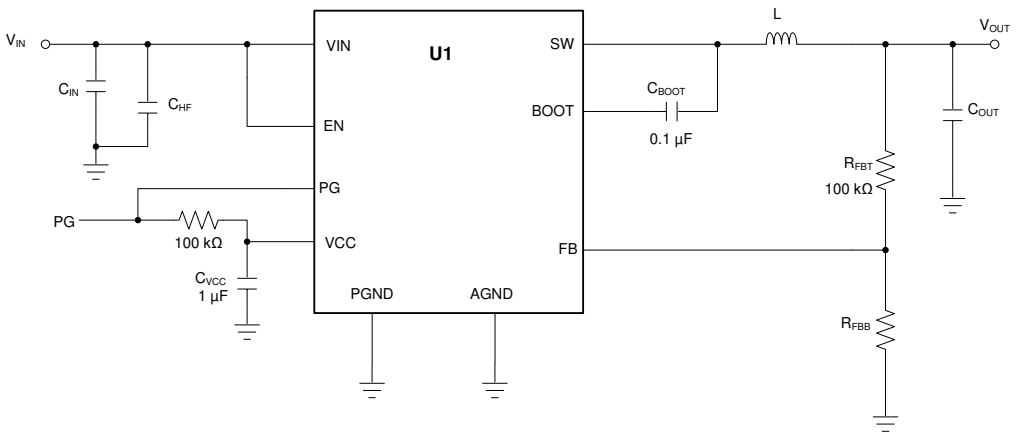


図 9-21. Circuit for Application Curves

表 9-3. BOM for Typical Application Curves

V_{OUT} (1)	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
3.3 V	400 kHz	43.3 kΩ	3 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 18 mΩ	LMR33640ADDA
5 V	400 kHz	24.9 kΩ	3 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 18 mΩ	LMR33640ADDA
3.3 V	1000 kHz	43.3 kΩ	3 × 22 µF	1 × 10 µF + 1 × 220 nF	3.3 µH, 16 mΩ	LMR33640DDDA
5 V	1000 kHz	24.9 kΩ	3 × 22 µF	1 × 10 µF + 1 × 220 nF	3.3 µH, 16 mΩ	LMR33640DDDA

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

9.3 What to Do and What Not to Do

- **Don't:** Exceed the *ESD Ratings*.
- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *Recommended Operating Conditions*.
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. Use the information in the *Maximum Ambient Temperature* section.
- **Do:** Follow all the guidelines and/or suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see the *Support Resources*).

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the recommendations found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 12.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{12}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help to damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters User Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output is recommended.

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground, as shown in 図 11-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupts the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 11-1 shows the recommended layout for the critical components of the LMR33640.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place the bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short and wide traces to the BOOT and SW pins.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and also a heat dissipation path.
6. *Connect the thermal pad to the ground plane.* The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
7. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. *Provide enough PCB area for proper heat sinking.* As stated in *セクション 9.2.2.10*, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

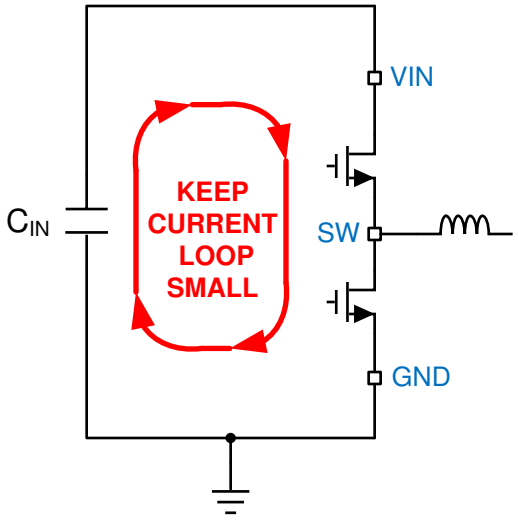


図 11-1. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 4 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. For the best heat dissipation, use as much copper as possible for system ground plane and on the top and bottom layers. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low-current conduction impedance, proper shielding, and lower thermal resistance.

11.2 Layout Example

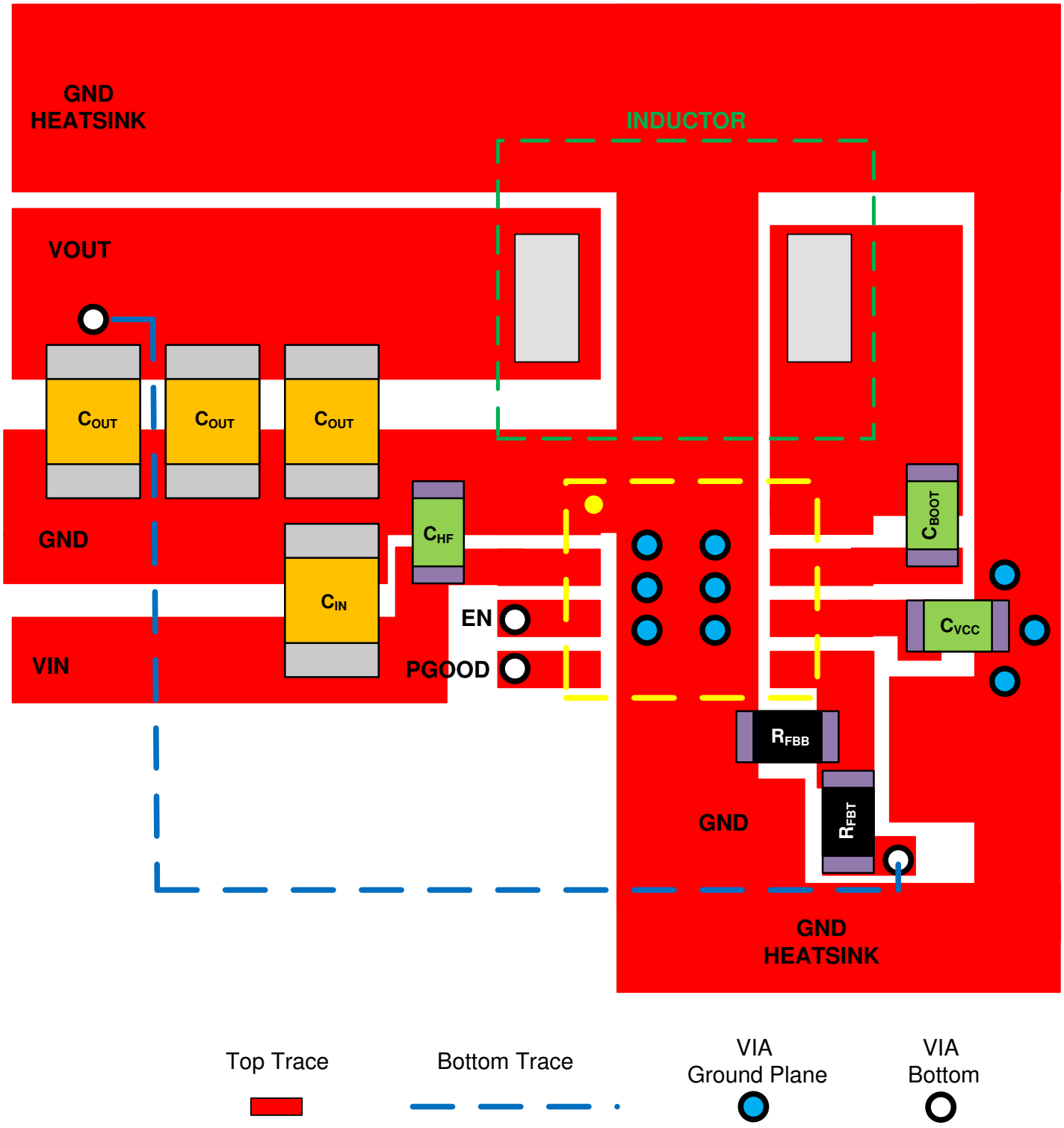


図 11-2. Example Layout for HSOIC (DDA) Package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM33630 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight Application Report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Thermal Design Made Simple with LM43604 And LM43602 Application Report*
- Texas Instruments, *PowerPAD Thermally Enhanced Package Application Report*
- Texas Instruments, *PowerPAD Made Easy Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies Application Report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines Application Report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

PowerPAD™ is a trademark of TI.
TI E2E™ is a trademark of Texas Instruments.
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WEBENCH® is a registered trademark of Texas Instruments.
is a registered trademark of TI.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR33640ADDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33640A
LMR33640ADDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33640A
LMR33640ADDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33640A
LMR33640ADDARG4.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33640A
LMR33640DDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33640D
LMR33640DDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33640D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

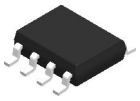
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

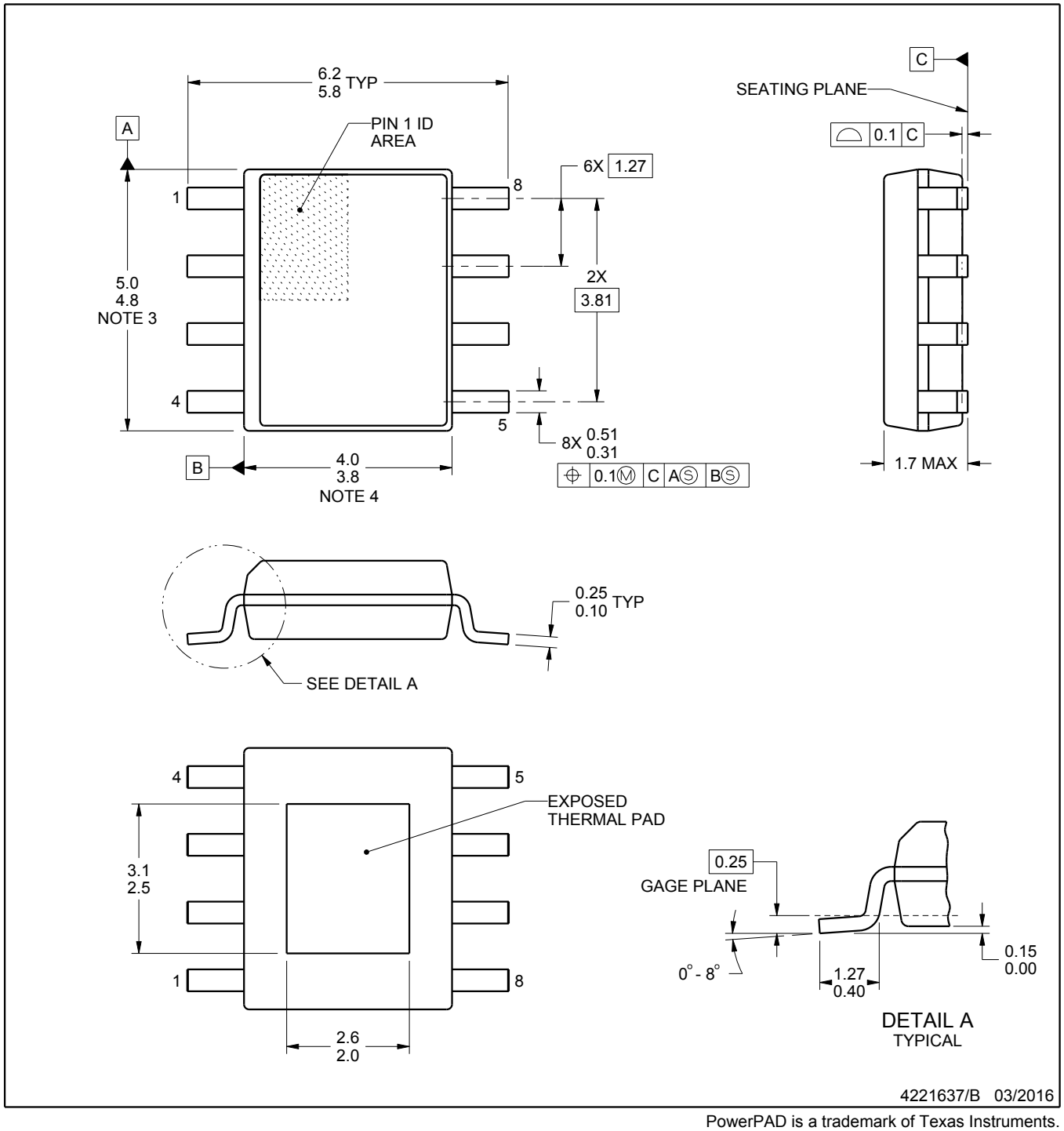


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

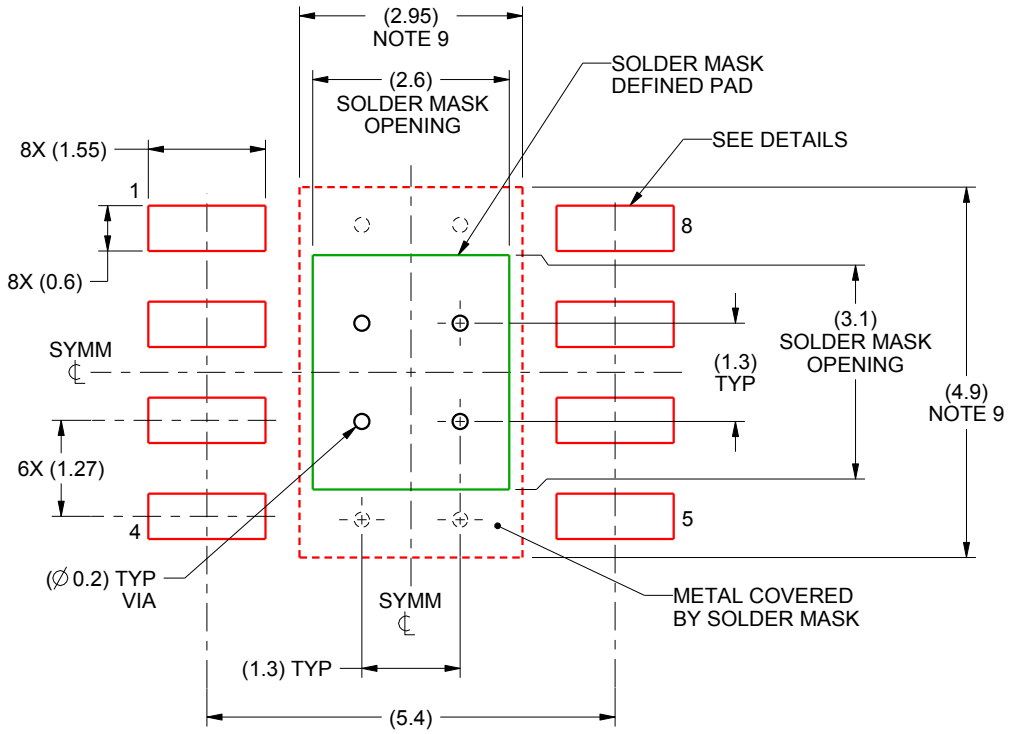
PLASTIC SMALL OUTLINE



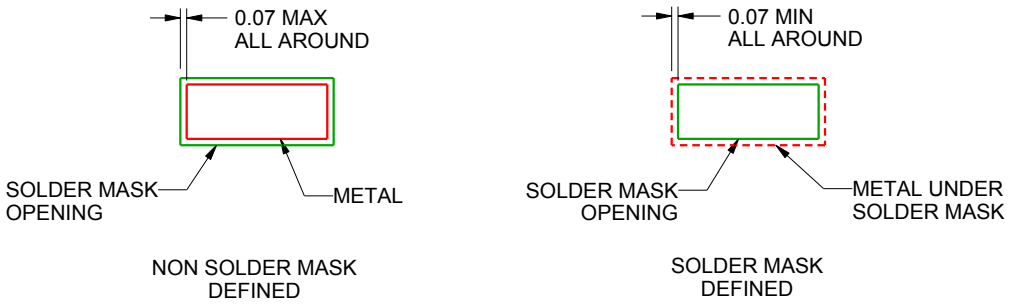
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

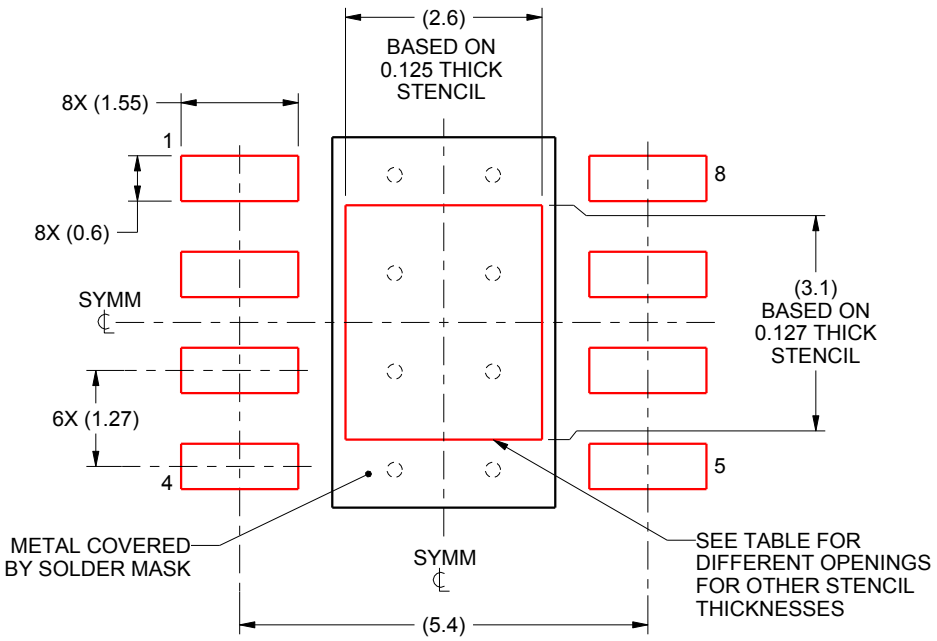


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

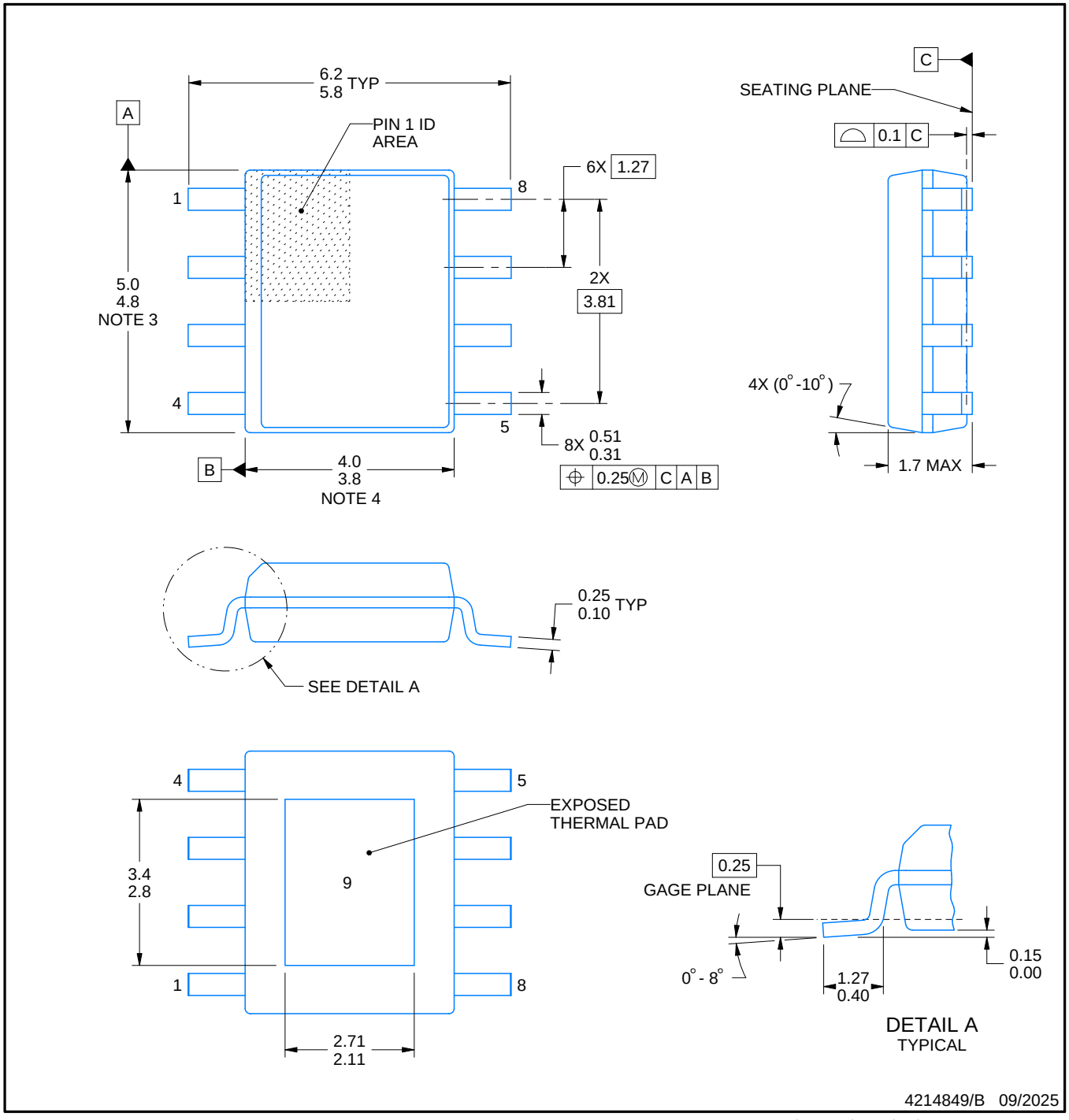
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

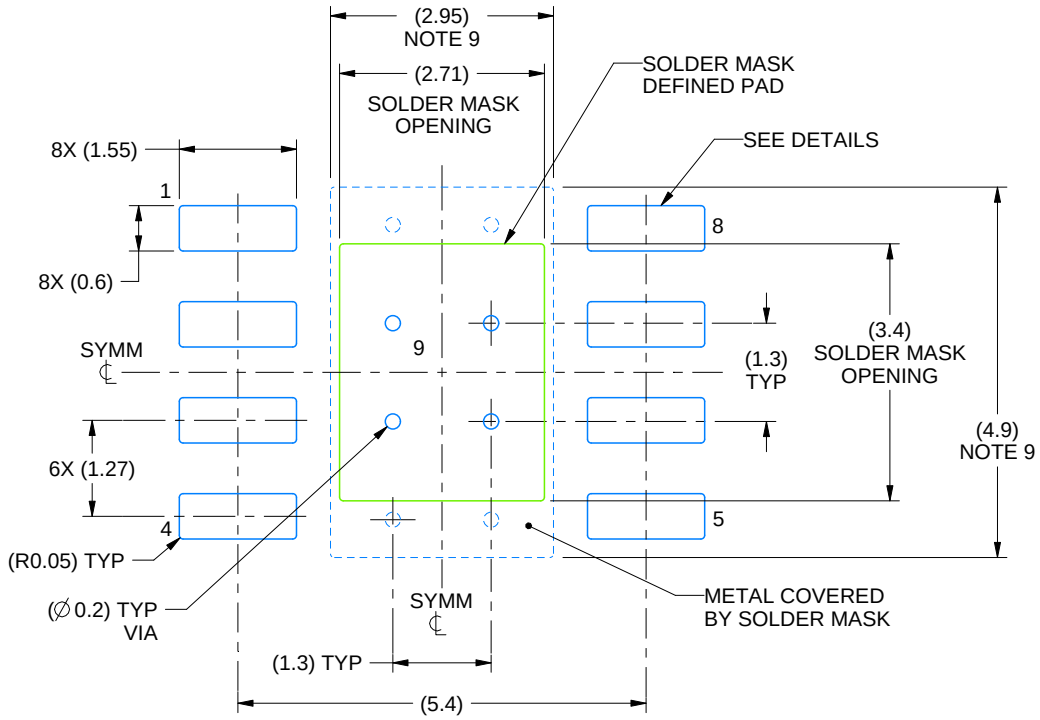
PLASTIC SMALL OUTLINE



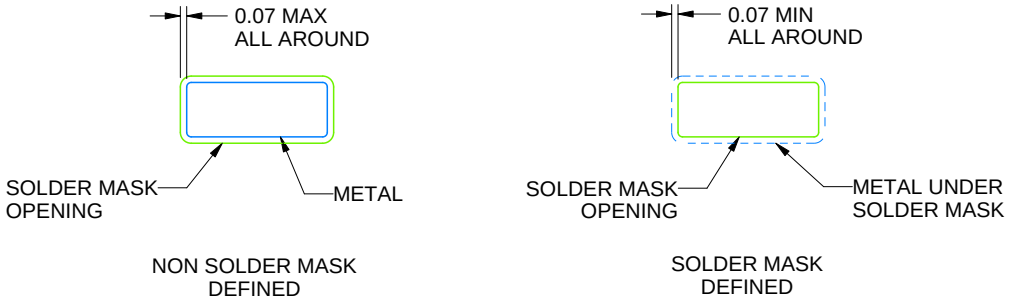
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

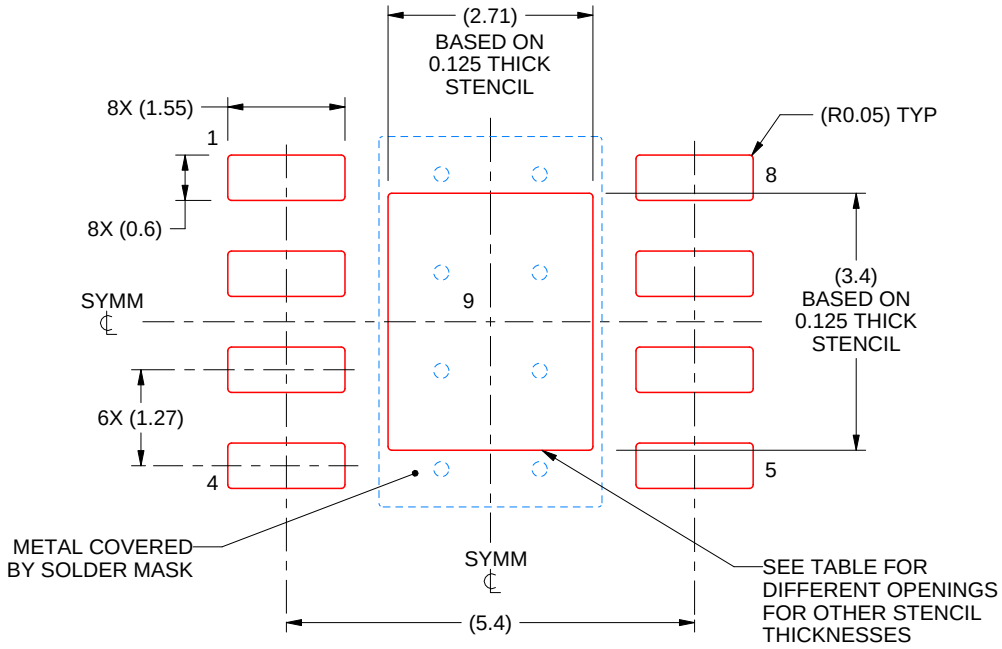
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月