



# LMP92064 Precision Low-Side, 125-kSps Simultaneous Sampling, Current Sensor and Voltage Monitor With SPI

## 1 Features

- Two Simultaneous Sampling 12-Bit ADCs
  - Conversion Rate: 125 kSps (Minimum)
- 12-Bit Current Sense Channel
  - Input-referred Offset:  $\pm 15\ \mu\text{V}$
  - Common-mode Voltage Range:  $-0.2\ \text{V}$  to  $2\ \text{V}$
  - Maximum Differential Input Voltage:  $75\ \text{mV}$
  - Fixed Gain:  $25\ \text{V/V}$
  - Gain Error:  $\pm 0.75\%$  (Maximum)
  - Bandwidth ( $-3\text{dB}$ ):  $70\ \text{kHz}$
  - DC PSRR:  $100\ \text{dB}$
  - DC CMRR:  $110\ \text{dB}$
- 12-Bit Voltage Channel
  - INL:  $\pm 1\ \text{LSB}$
  - Offset Error:  $\pm 2\ \text{mV}$  (Maximum)
  - Gain Error:  $\pm 0.75\%$  (Maximum)
  - Maximum Input Voltage:  $2.048\ \text{V}$
  - Bandwidth:  $100\ \text{kHz}$
- Internal Reference
- SPI Frequency: Up to  $20\ \text{MHz}$
- Temperature Range:  $-40^\circ\text{C}$  to  $105^\circ\text{C}$
- 16-Pin WSON Package

## 2 Applications

- Enterprise Servers
- Telecommunications
- Power Management

## 3 Description

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. This analog frontend (AFE) includes a precision current sense amplifier to measure a load current across a shunt resistor and a buffered voltage channel to measure the voltage supply of the load. The current and voltage channels are sampled simultaneously by independent 125-kSps, 12-bit ADC converters, allowing for very accurate power calculations in unidirectional sensing applications.

The LMP92064 includes an internal  $2.048\text{-V}$  reference for the ADCs, eliminating the need of an external reference and reducing component count and board space.

A host can communicate with the LMP92064 using a four-wire SPI interface running at speeds of up to  $20\ \text{MHz}$ . The fast SPI interface lets the user take advantage of the higher bandwidth ADC to capture fast varying signals. The four-wire interface with dedicated unidirectional input and output lines also allows for an easy interface to digital isolators in applications where isolation is required.

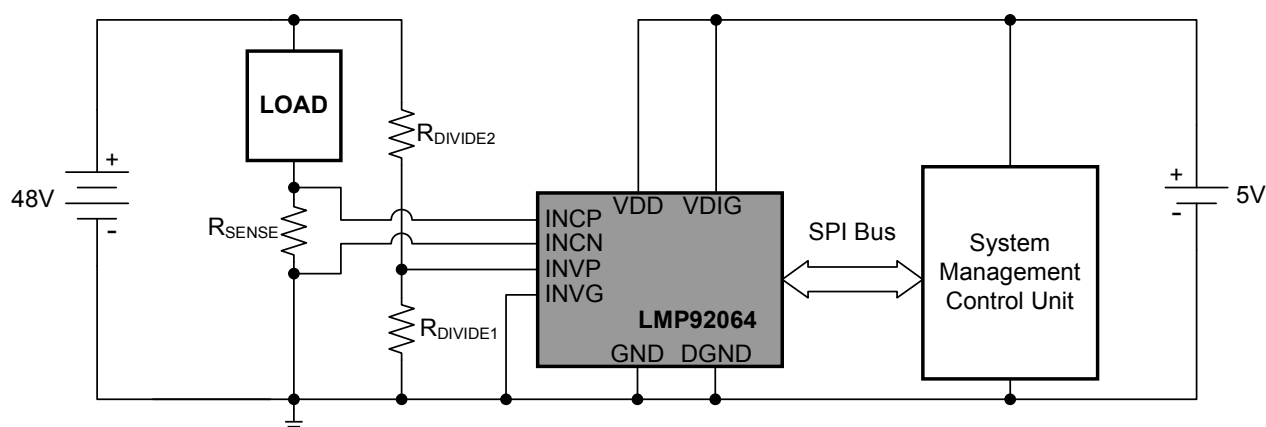
The LMP92064 operates from a single  $4.5\text{-V}$  to  $5.5\text{-V}$  supply and includes a separate digital supply pin. The LMP92064 is specified over a temperature range of  $-40^\circ\text{C}$  to  $105^\circ\text{C}$ , and is available in a  $5\text{-mm} \times 4\text{-mm}$  16-Pin WSON package.

**Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)                          |
|-------------|-----------|------------------------------------------|
| LMP92064    | WSON (16) | $5.00\ \text{mm} \times 4.00\ \text{mm}$ |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**



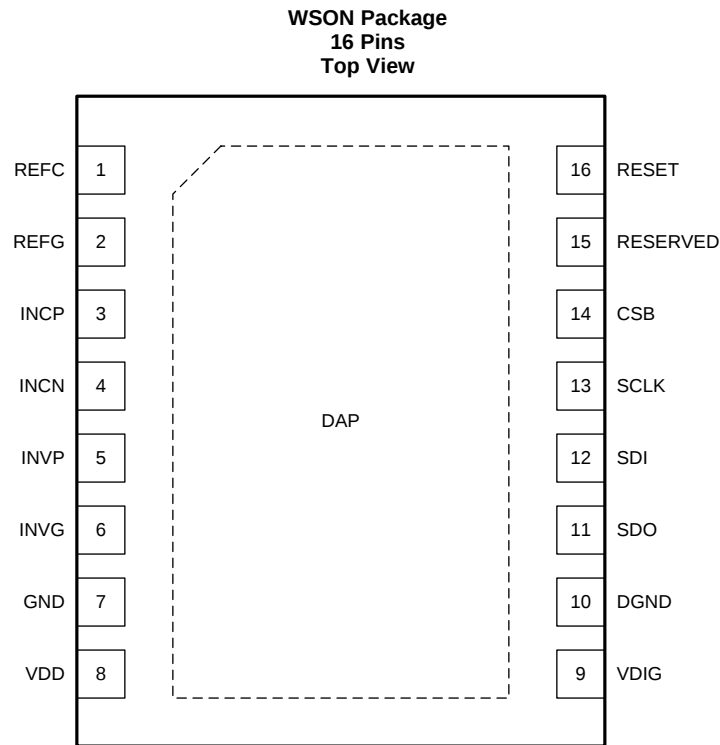
## Table of Contents

|                                                |           |                                                                  |           |
|------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 7.3 Feature Description.....                                     | <b>10</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | 7.4 Device Functional Modes.....                                 | <b>11</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | 7.5 Register Maps .....                                          | <b>13</b> |
| <b>4 Revision History</b> .....                | <b>2</b>  | <b>8 Application and Implementation</b> .....                    | <b>17</b> |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b>  | 8.1 Application Information.....                                 | <b>17</b> |
| <b>6 Specifications</b> .....                  | <b>4</b>  | 8.2 Typical Application .....                                    | <b>17</b> |
| 6.1 Absolute Maximum Ratings .....             | <b>4</b>  | <b>9 Power Supply Recommendations</b> .....                      | <b>21</b> |
| 6.2 ESD Ratings.....                           | <b>4</b>  | <b>10 Layout</b> .....                                           | <b>21</b> |
| 6.3 Recommended Operating Conditions.....      | <b>4</b>  | 10.1 Layout Guidelines .....                                     | <b>21</b> |
| 6.4 Thermal Information .....                  | <b>4</b>  | 10.2 Layout Example .....                                        | <b>22</b> |
| 6.5 Electrical Characteristics.....            | <b>5</b>  | <b>11 Device and Documentation Support</b> .....                 | <b>23</b> |
| 6.6 Timing Requirements .....                  | <b>6</b>  | 11.1 Trademarks .....                                            | <b>23</b> |
| 6.7 Typical Characteristics .....              | <b>7</b>  | 11.2 Electrostatic Discharge Caution.....                        | <b>23</b> |
| <b>7 Detailed Description</b> .....            | <b>10</b> | 11.3 Glossary .....                                              | <b>23</b> |
| 7.1 Overview .....                             | <b>10</b> | <b>12 Mechanical, Packaging, and Orderable Information</b> ..... | <b>23</b> |
| 7.2 Functional Block Diagram .....             | <b>10</b> |                                                                  |           |

## 4 Revision History

| Changes from Original (June 2013) to Revision A                                                                                                                                                                                                                                                                                                                                                                                                     | Page     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <ul style="list-style-type: none"> <li>Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul> | <b>1</b> |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN      |     | I/O <sup>(1)</sup> | DESCRIPTION                                             |
|----------|-----|--------------------|---------------------------------------------------------|
| NAME     | NO. |                    |                                                         |
| REFC     | 1   | —                  | Internal reference bypass capacitor pin                 |
| REFG     | 2   | G                  | Internal reference ground                               |
| INCP     | 3   | I                  | Positive current channel input                          |
| INCN     | 4   | I                  | Negative current channel input                          |
| INV P    | 5   | I                  | Positive voltage channel input                          |
| INV G    | 6   | G                  | Ground reference for the negative voltage channel input |
| GND      | 7   | G                  | Analog ground                                           |
| VDD      | 8   | P                  | Analog power supply                                     |
| VDIG     | 9   | P                  | Digital power supply                                    |
| DGND     | 10  | G                  | Digital ground                                          |
| SDO      | 11  | O                  | SPI Bus push-pull serial data digital output            |
| SDI      | 12  | I                  | SPI Bus serial data digital input                       |
| SCLK     | 13  | I                  | SPI Bus clock digital input                             |
| CSB      | 14  | I                  | SPI Bus chip select bar digital input                   |
| RESERVED | 15  | —                  | Reserved (Do not connect)                               |
| RESET    | 16  | I                  | Reset (high-active)                                     |
| DAP      | n/a | —                  | No connection (Do not connect)                          |

(1) G = Ground, I = Input, O = Output, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

 over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

|                                       | MIN                             | MAX     | UNIT |
|---------------------------------------|---------------------------------|---------|------|
| Analog Supply Voltage (VDD)           | −0.3                            | 6.0     | V    |
| Digital Supply Voltage (VDIG)         | VDD−0.3                         | VDD+0.3 |      |
| Voltage at Input Pins <sup>(3)</sup>  | −0.3                            | VDD+0.3 | V    |
| Junction Temperature                  |                                 | 150     | °C   |
| Mounting temperature                  | Infrared or convection (20 sec) |         | 260  |
|                                       |                                 |         | °C   |
| Storage temperature, T <sub>stg</sub> | −65                             | 150     | °C   |

- (1) All voltages are measured with respect to GND = DGND = 0 V, unless otherwise specified.
- (2) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (3) When the input voltage (VIN), at any pin exceeds power supplies (VIN < GND or VIN > VDD), the current at that pin must not exceed 5 mA, and the voltage (VIN) at that pin must not exceed 6.0 V. See *Pin Description* for additional details of input circuitry.

### 6.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                               | MIN | MAX | UNIT |
|-------------------------------|-----|-----|------|
| Analog Supply Voltage (VDD)   | 4.5 | 5.5 | V    |
| Digital Supply Voltage (VDIG) | VDD | VDD | V    |
| Temperature Range             | −40 | 105 | °C   |

- (1) All voltages are measured with respect to GND = DGND = 0 V, unless otherwise specified.

### 6.4 Thermal Information

Over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC <sup>(1)</sup>                              | LMP92064 | UNIT |
|------------------------------------------------------------|----------|------|
|                                                            | NHR      |      |
|                                                            | 16 PINS  |      |
| R <sub>θJA</sub> Package thermal resistance <sup>(2)</sup> | 44       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The package thermal impedance is calculated in accordance with JESD 51-7. The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub> or the number given in [Absolute Maximum Ratings](#), whichever is lower.

## 6.5 Electrical Characteristics

Typical specifications are at 25°C. All specifications are at  $4.5\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ ,  $\text{VDIG} = \text{VDD}$  and  $-0.2\text{ V} \leq \text{VCM} \leq 2\text{ V}$ , unless otherwise specified.

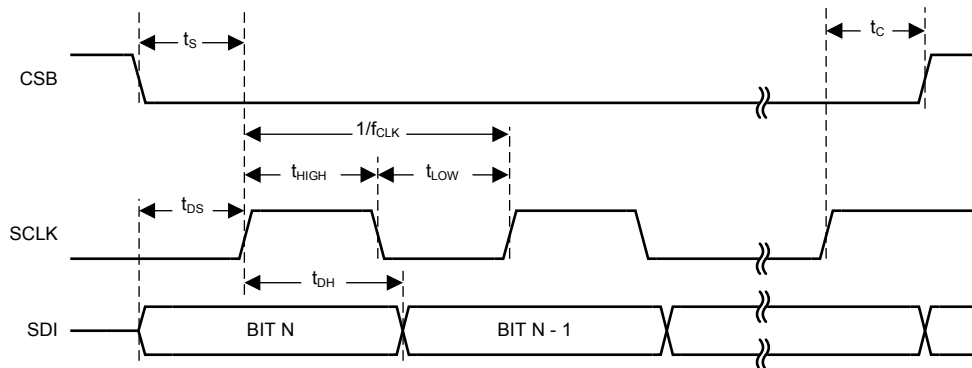
| PARAMETER                            |                                          | TEST CONDITIONS              | MIN            | TYP    | MAX        | UNIT |
|--------------------------------------|------------------------------------------|------------------------------|----------------|--------|------------|------|
| CURRENT SENSE INPUT CHANNEL          |                                          |                              |                |        |            |      |
| V <sub>OS</sub>                      | Input-referred Offset Voltage            |                              | ±15            |        | μV         |      |
|                                      |                                          | Temperature extremes         | -60            | 60     |            |      |
| TCV <sub>OS</sub>                    | Input-referred Offset Voltage Drift      |                              | ±280           |        | nV/°C      |      |
|                                      | Long-term Stability                      |                              | 0.3            |        | μV/mo      |      |
|                                      | Resolution                               |                              | 12<br>20       |        | Bits<br>μV |      |
| INL                                  | Integral Non-Linearity Error             |                              | ±1%<br>±0.025% |        | LSB        |      |
| DNL                                  | Differential Non-Linearity Error         |                              | ±0.5           |        | LSB        |      |
| DC CMRR                              | Common-Mode Rejection Ratio              | −0.2 V ≤ VCM ≤ 2 V           | 110            |        | dB         |      |
| DC PSRR                              | Power Supply Rejection Ratio             | 4.5 V ≤ VDD ≤ 5.5 V          | 100            |        | dB         |      |
| CMVR                                 | Common-Mode Voltage Range                | Low VCM                      | −0.2           |        | V          |      |
|                                      |                                          | High VCM                     | 2              |        |            |      |
| V <sub>DIFF(MAX)</sub>               | Maximum Differential Input Voltage Range |                              | 75             |        | mV         |      |
| A <sub>V</sub>                       | Current Shunt Amplifier Gain             |                              | 25             |        | V/V        |      |
|                                      | Current Sense Channel Gain               |                              | 50             |        | kCode/V    |      |
| GE                                   | Gain Error (CSA, VREF and ADC)           | Temperature extremes         | -0.75%         | 0.75 % |            |      |
| GD                                   | Gain Drift                               |                              | ±25            |        | ppm/°C     |      |
| RIN                                  | Input Impedance                          |                              | 100            |        | GΩ         |      |
| BW                                   | −3dB Bandwidth                           |                              | 70             |        | kHz        |      |
| VOLTAGE INPUT CHANNEL                |                                          |                              |                |        |            |      |
|                                      | Offset Error (Buffer and ADC)            | Temperature extremes         | -2             | 2      |            | mV   |
|                                      | Resolution                               |                              | 12             |        | Bits       |      |
| INL                                  | Integral Non-Linearity Error             |                              | ±1%<br>±0.025% |        | LSB        |      |
| DC PSRR                              | Power Supply Rejection Ratio             |                              | 70             |        | dB         |      |
| V <sub>CHVP</sub>                    | Full-Scale Input Voltage                 |                              | 2.048          |        | V          |      |
| A <sub>V</sub>                       | Buffer Amplifier Gain                    |                              | 1              |        | V/V        |      |
|                                      | Voltage Sense Channel Gain               |                              | 2              |        | kCode/V    |      |
| GE                                   | Gain Error (Buffer, VREF and ADC)        | Temperature extremes         | -0.75%         | 0.75 % |            |      |
| RIN                                  | Input Impedance                          |                              | 100            |        | GΩ         |      |
| BW                                   | Bandwidth <sup>(1)</sup>                 |                              | 100            |        | kHz        |      |
| DIGITAL INPUT/OUTPUT CHARACTERISTICS |                                          |                              |                |        |            |      |
| V <sub>IH</sub>                      | Logical “1” Input Voltage                | Temperature extreme          | 0.7*VDIG       |        | V          |      |
| V <sub>IL</sub>                      | Logical “0” Input Voltage                | Temperature extreme          | 0.3*VDIG       |        | V          |      |
| V <sub>OH</sub>                      | Logical “1” Output Voltage               | I <sub>SOURCE</sub> = 300 μA |                |        | V          |      |
|                                      |                                          | Temperature extreme          | VDIG<br>−0.15  |        |            |      |
| V <sub>OL</sub>                      | Logical “0” Output Voltage               | I <sub>SINK</sub> = 300 μA   |                |        | V          |      |
|                                      |                                          | Temperature extreme          | DGND<br>+0.15  |        |            |      |
| SUPPLY CHARACTERISTICS               |                                          |                              |                |        |            |      |
| I <sub>VDD</sub>                     | Analog Supply Current                    |                              | 11             |        | mA         |      |
| I <sub>VDIG</sub>                    | Digital Supply Current                   |                              | 2              |        | mA         |      |

(1) No analog filter; limited by sampling rate.

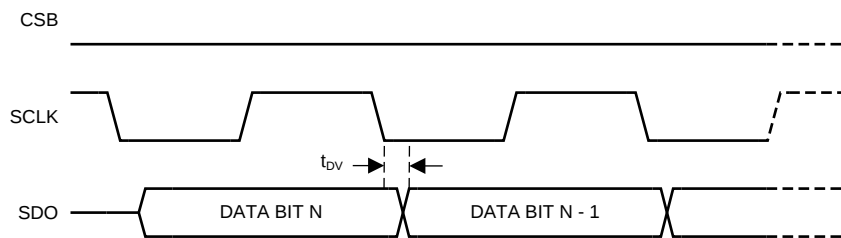
## 6.6 Timing Requirements

Typical specifications are at 25°C. All specifications are at 4.5 V ≤ VDD ≤ 5.5 V, VDIG = VDD and a 20 pF capacitive load on SDO, unless otherwise specified.

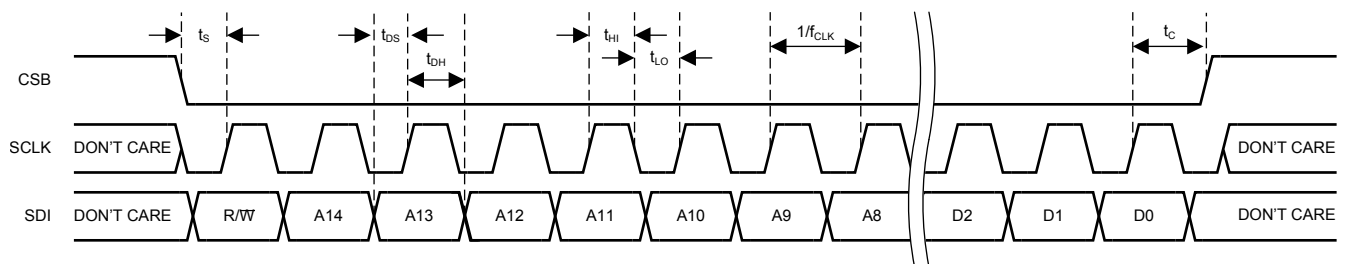
|            |                                                 | MIN | MAX | UNIT |
|------------|-------------------------------------------------|-----|-----|------|
| $t_{DS}$   | SDI to SCLK rising edge setup time              | 10  |     | ns   |
| $t_{DH}$   | SCLK rising edge to SDI hold time               | 10  |     | ns   |
| $f_{CLK}$  | Frequency of SCLK                               | 100 |     | Hz   |
|            |                                                 |     | 20  | MHz  |
| $t_{HIGH}$ | High width of SPI clock                         | 25  |     | ns   |
| $t_{LOW}$  | Low width of SPI clock                          | 25  |     | ns   |
| $t_S$      | CSB falling edge to SCLK rising edge setup time | 10  |     | ns   |
| $t_C$      | SCLK rising edge to CSB rising edge hold time   | 30  |     | ns   |
| $t_{DV}$   | SCLK falling edge to valid SDO readback data    |     | 20  | ns   |
| $t_{RST}$  | Reset pin pulse width                           | 3.5 |     | ns   |
| $t_{CONV}$ | Conversion rate of all channels                 | 125 |     | kSps |



**Figure 1. Serial Control Port Timing – Write**



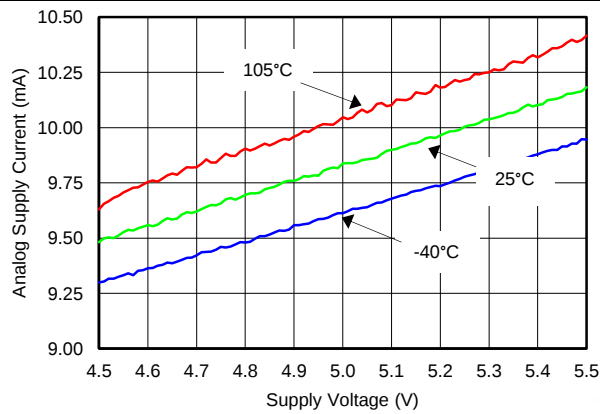
**Figure 2. Serial Control Port Timing – Read**



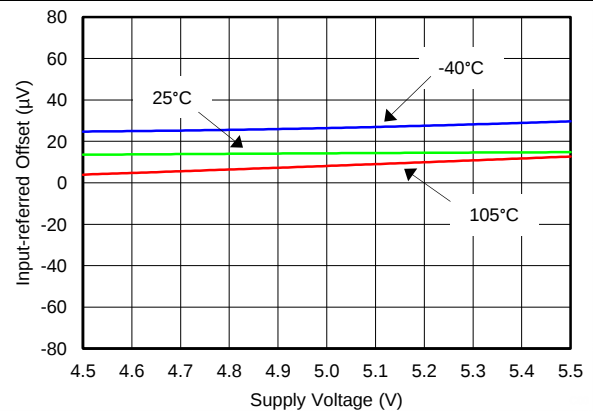
**Figure 3. Serial Control Port Write – MSB First, 16-Bit Instruction, Timing Measurements**

## 6.7 Typical Characteristics

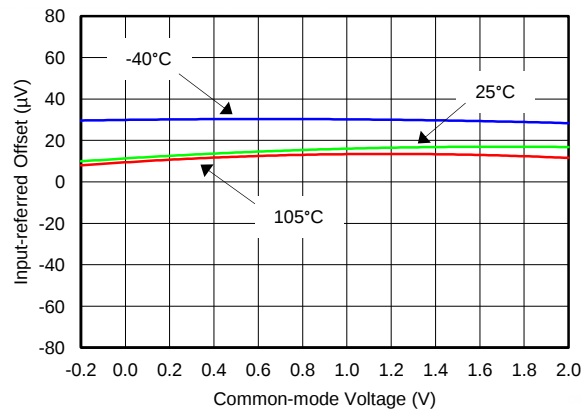
All plots at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $V_{DIG} = 5.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$  and  $GND = DGND = 0\text{ V}$ , unless otherwise specified.



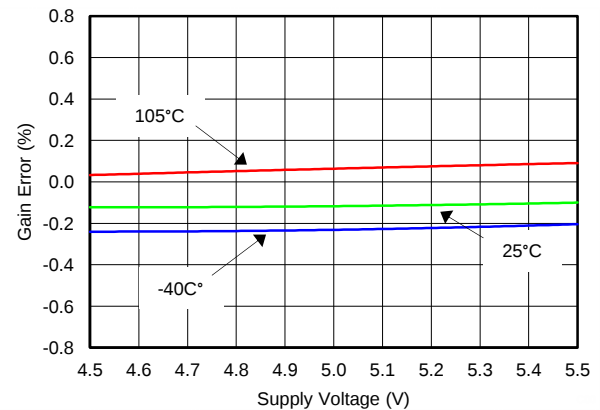
**Figure 4. Analog Supply Current vs Supply Voltage**



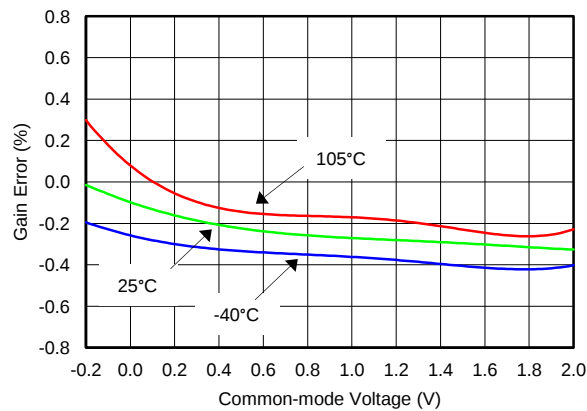
**Figure 5. Input-Referred Offset vs Supply Voltage (Current Channel)**



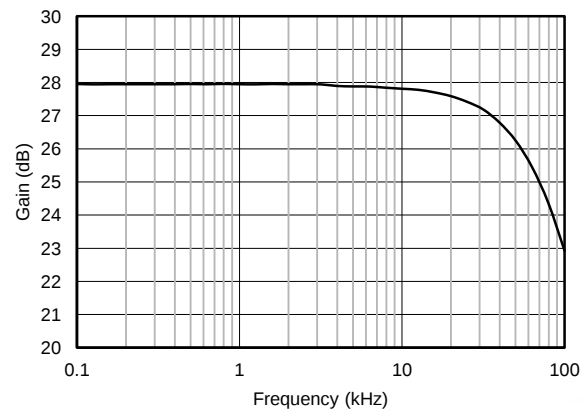
**Figure 6. Input-Referred Offset vs Common-Mode Voltage (Current Channel)**



**Figure 7. Gain Error vs Supply Voltage (Current Channel)**



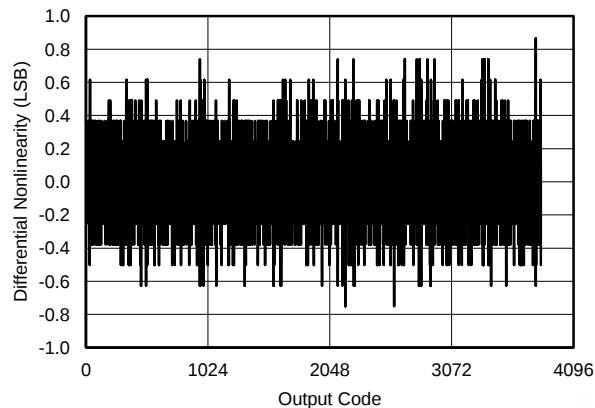
**Figure 8. Gain Error vs Common-Mode Voltage (Current Channel)**



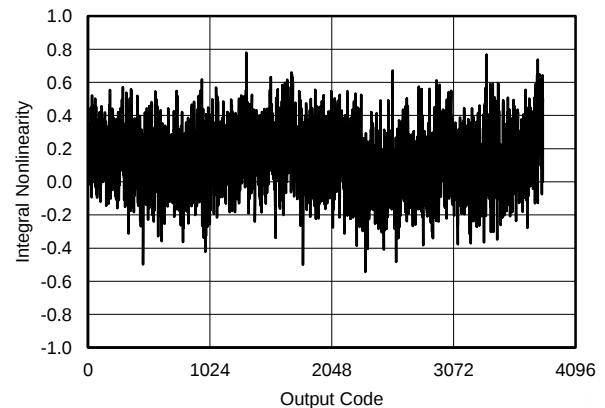
**Figure 9. Gain vs Frequency (Current Channel)**

## Typical Characteristics (continued)

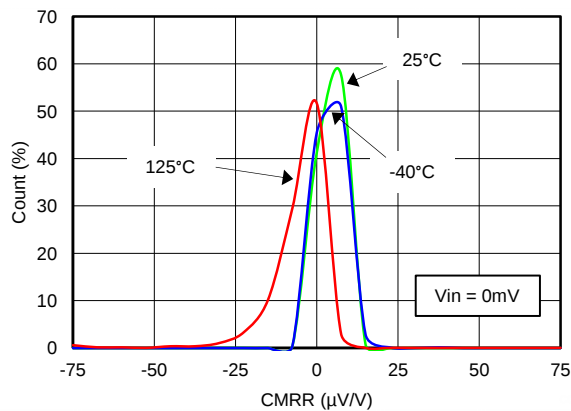
All plots at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $V_{DIG} = 5.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$  and  $GND = DGND = 0\text{ V}$ , unless otherwise specified.



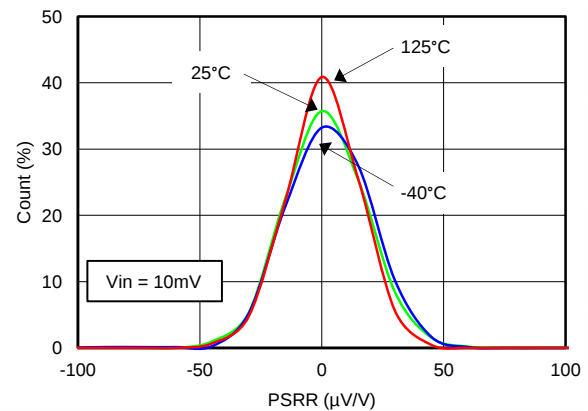
**Figure 10. Differential Nonlinearity (Current Channel)**



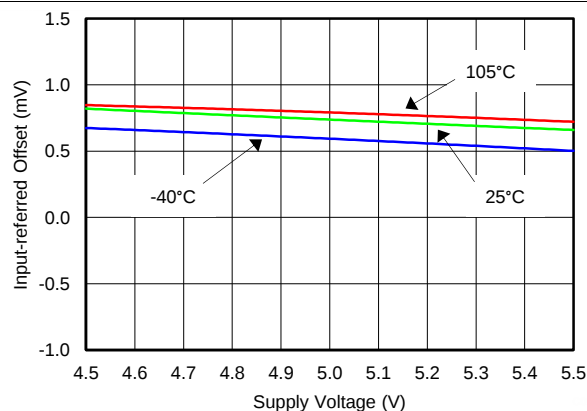
**Figure 11. Integral Nonlinearity (Current Channel)**



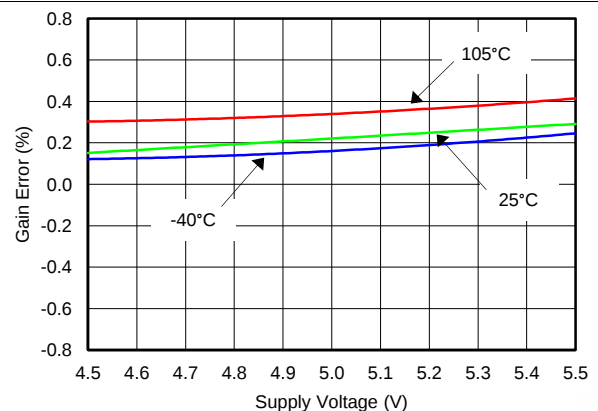
**Figure 12. Common-Mode Rejection Ratio Distribution (Current Channel)**



**Figure 13. Power Supply Rejection Ratio Distribution  $V_{cm} = -0.2\text{ V}$  (Current Channel)**



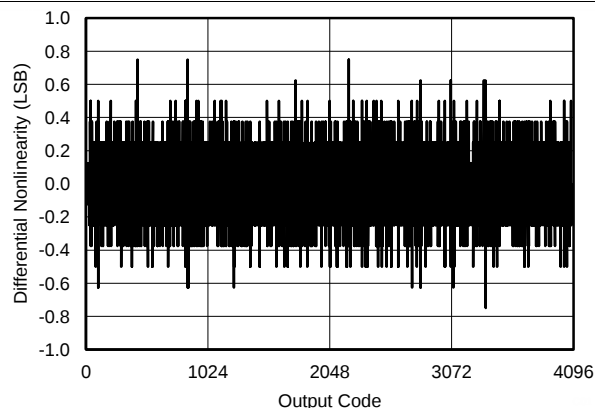
**Figure 14. Input-Referred Offset  $V_{ssupply}$  Voltage (Voltage Channel)**



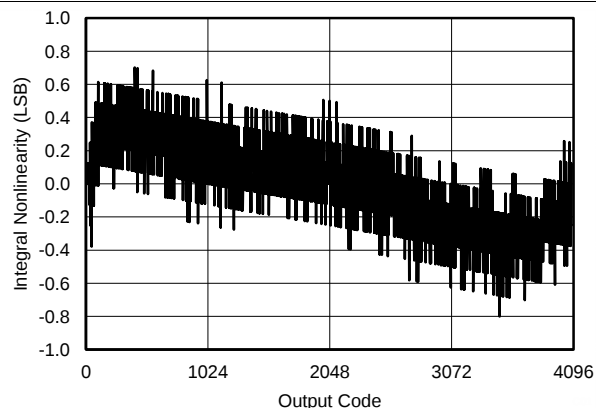
**Figure 15. Gain Error vs Supply Voltage (Voltage Channel)**

## Typical Characteristics (continued)

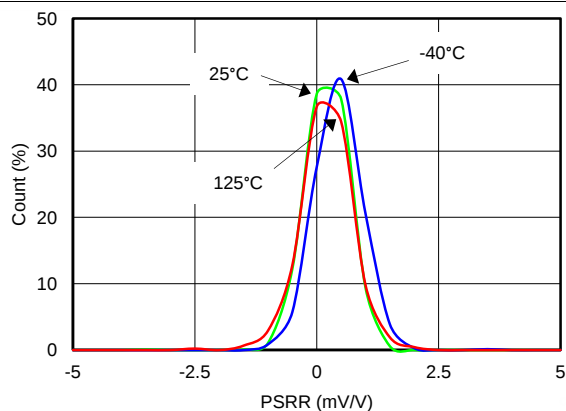
All plots at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $V_{DIG} = 5.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$  and  $GND = DGND = 0\text{ V}$ , unless otherwise specified.



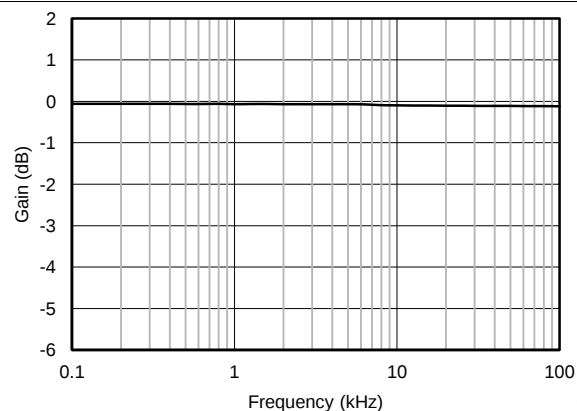
**Figure 16. Differential Nonlinearity (Voltage Channel)**



**Figure 17. Integral Nonlinearity (Voltage Channel)**



**Figure 18. Power Supply Rejection Ratio Distribution (Voltage Channel)**



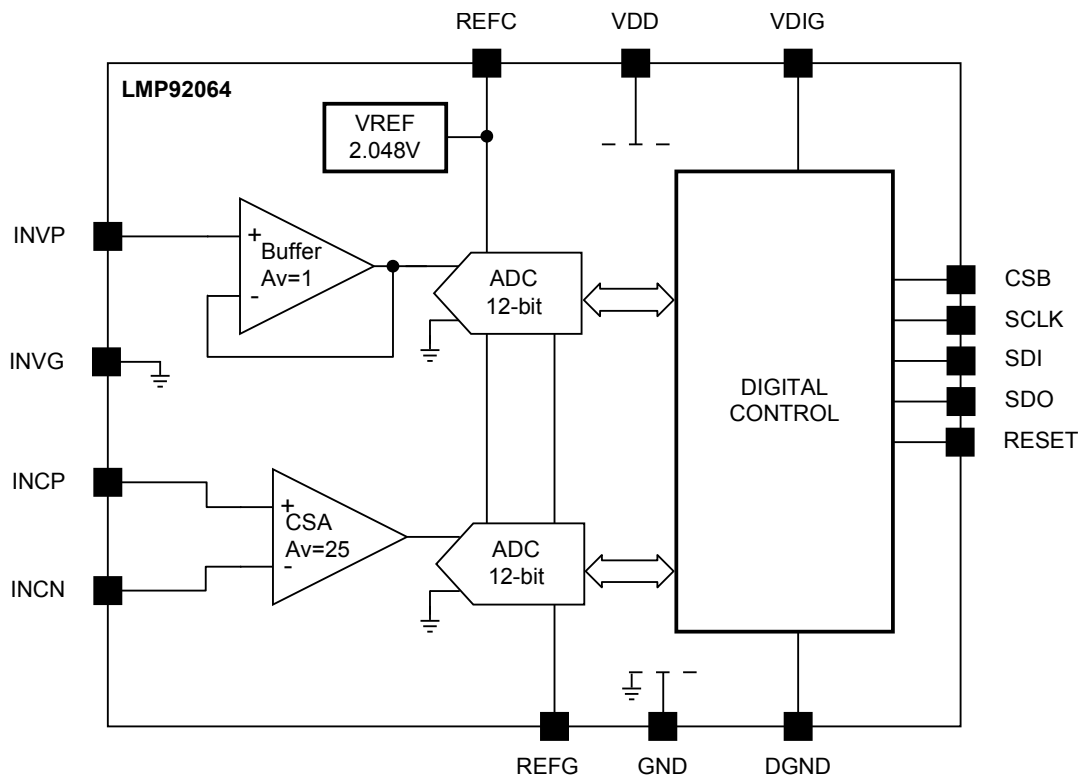
**Figure 19. Gain vs Frequency (Voltage Channel)**

## 7 Detailed Description

### 7.1 Overview

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. The analog front-end includes a precision current sense amplifier to measure a load current across a shunt resistor and a buffered voltage channel to measure the voltage supply of the load.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Current Sense Input Channel

The current sensing channel of the LMP92064 has a high impedance differential amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is stored as a right-justified 16-bit number as shown in [Table 1](#), where the 4 most significant bits are always 0. Due to an offset auto-calibration feature of the current sense channel path, the top 256 codes are clipped at code 3840, denoted by the trailing zeros found in the equivalent binary code of the maximum positive input voltage.

The output data of the current sense channel is accessible on registers [0x0203](#) and [0x0202](#).

**Table 1. Ideal Current Channel Input Voltages and Output Codes**

| DESCRIPTION                    | ANALOG VALUE                | DIGITAL OUTPUT          |          |
|--------------------------------|-----------------------------|-------------------------|----------|
| Full scale range               | $V_{FS} = 81.92 \text{ mV}$ | BINARY CODE<br>[B15:B0] | HEX CODE |
| Least significant bit (LSB)    | $V_{FS} / 4096$             |                         |          |
| Maximum Positive Input Voltage | $V_{FS} - 256 \text{ LSB}$  | 0000 1111 0000 0000     | 0x0F00   |
| Zero                           | 0 V                         | 0000 0000 0000 0000     | 0x0000   |

### 7.3.2 Current Sense Input Channel Common-Mode and Differential Voltage Range (Dynamic Range Considerations)

The input voltage should be in the range of  $-0.2\text{ V}$  to  $2\text{ V}$ . The input can withstand voltage up to  $V_{DD} + 0.3\text{ V}$  absolute maximum but the operational range is limited to  $2\text{ V}$ . Operation below  $-0.2\text{ V}$  or above  $2\text{ V}$  on either input pin will introduce severe gain errors and nonlinearity.

The maximum differential voltage (defined as the voltage difference between INCP and INCN) for which the part is designed to work is  $75\text{ mV}$ . Larger differential or common mode input voltages will not damage the part (as long as the input pins remain between  $GND - 0.3\text{ V}$  and  $V_{DD} + 0.3\text{ V}$ ), however, exposure for extended periods may affect device reliability. The ADC output code will not roll over and will clip at minimum or maximum scale when the maximum differential voltage is exceeded.

### 7.3.3 Voltage Sense Input Channel

The voltage sensing channel of the LMP92064 has a high impedance buffer amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is also stored as a right-justified 16-bit number as shown in [Table 2](#), where the 4 most significant bits are always 0.

The output data of the voltage sense channel is accessible on registers [0x0201](#) and [0x0200](#).

**Table 2. Ideal Voltage Channel Input Voltages and Output Codes**

| DESCRIPTION                    | ANALOG VALUE              | DIGITAL OUTPUT          |          |
|--------------------------------|---------------------------|-------------------------|----------|
| Full scale range               | $V_{FS} = 2.048\text{ V}$ | BINARY CODE<br>[B15:B0] | HEX CODE |
| Least significant bit (LSB)    | $V_{FS} / 4096$           |                         |          |
| Maximum Positive Input Voltage | $V_{FS} - 1\text{ LSB}$   | 0000 1111 1111 1111     | 0x0FFF   |
| Zero Code Voltage              | $0\text{ V}$              | 0000 0000 0000 0000     | 0x0000   |

### 7.3.4 Reference

The LMP92064 includes an internal  $2.048\text{-V}$  band-gap reference for the ADCs, which eliminates the need of an external reference and reduces component count and board space. The REFC pin is provided to allow bypassing this internal reference for low noise operation. A  $1\text{-}\mu\text{F}$  ceramic decoupling capacitor is required between the REFC and REFG pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

### 7.3.5 Reset

There are two methods to reset the LMP92064. A soft reset is done by setting bit7=1 in the [CONFIG\\_A](#) register. In a soft reset, the SPI state machine and the contents of registers [0x0000](#) and [0x0001](#) are unaffected.

A hardware reset is done by connecting the RESET pin of the LMP92064 to VDIG. If the pin is driven by a switch or a GPIO, TI recommends adding an external RC filter to prevent reset glitches.

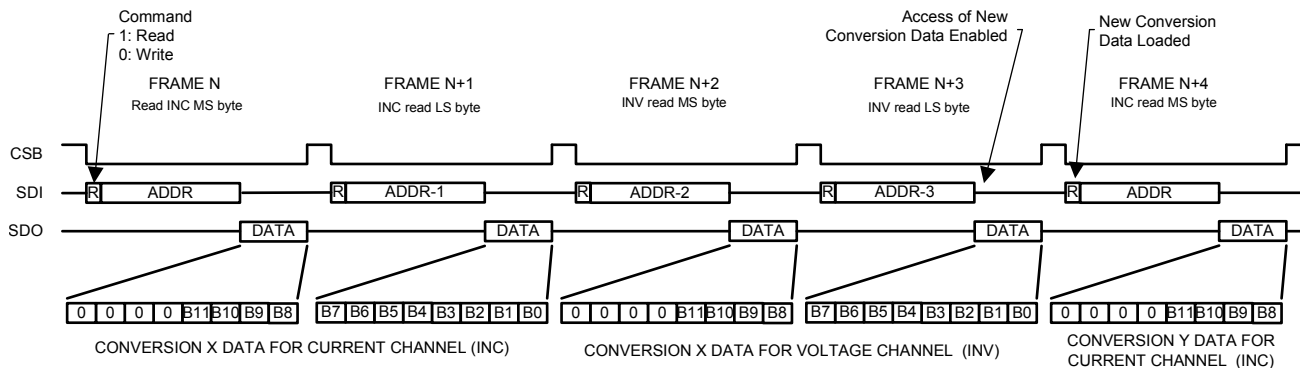
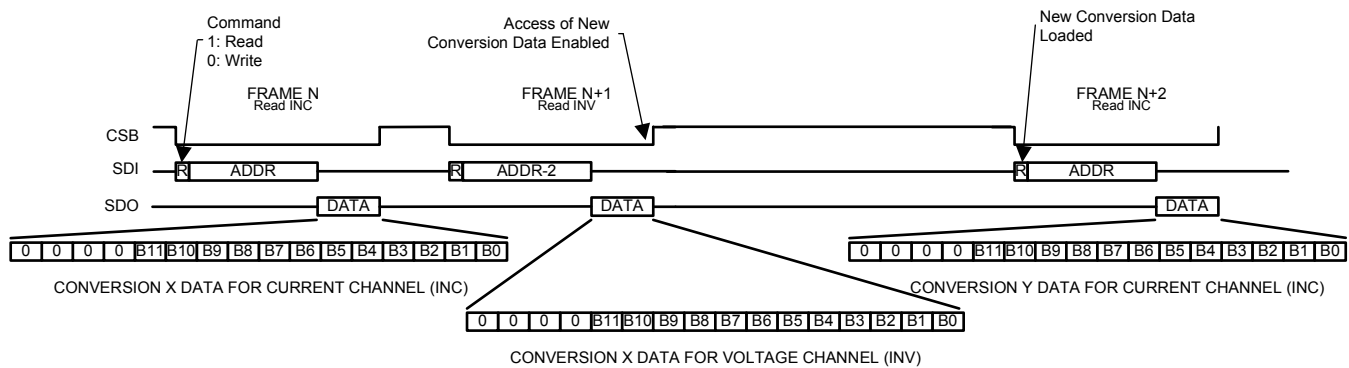
### 7.3.6 Device Power-Up Sequence

The sources providing power to the analog and digital supply pins of the LMP92064,  $V_{DD}$  and  $VDIG$ , must ramp up at the same time to have a proper power-on reset (POR) event. The easiest way to achieve it is to tie  $V_{DD}$  and  $VDIG$  to the same power source using a star configuration.

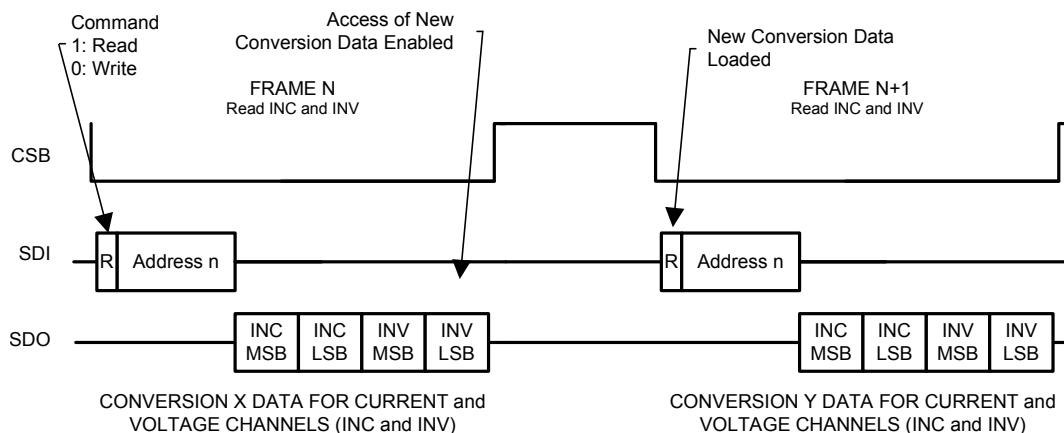
## 7.4 Device Functional Modes

### 7.4.1 ADC Operation

The LMP92064 includes two 12-bit ADCs that are continuously running in the background. The device is configured, and data is read, using a four-wire SPI interface: CSB, SCLK, SDO and SDI. The device outputs its data on SDO, and the data for both channels is synchronized such that all data read would be from the same instant in time. New conversion data for both channels will only be made available after all registers are read in descending sequential order (addresses [0x0203](#)-[0x0200](#)). All registers must be read otherwise new conversion data will not be available. Three different output data formats are available as detailed in [Figure 20](#), [Figure 21](#) and [Figure 22](#).

**Device Functional Modes (continued)**

**Figure 20. Timing Diagram With Byte Read Frames**

**Figure 21. Timing Diagram With Word Read Frames**

The register address to read can automatically decrement if the CSB line is kept low longer. For example, to read all the conversion data, keep the CSB line low for 48 SPI clock cycles (16 clocks for command/address, 8 clocks for MSB of current channel, 8 clocks for LSB of current channel, 8 clocks for MSB of voltage channel and 8 clocks for LSB of voltage channel). The read command should start from address 0x0203.


**Figure 22. Timing Diagram With All Data Read Frames**

## 7.5 Register Maps

1. If written to, Reserved bits must be written to 0, unless otherwise indicated.
2. Read back value of Reserved bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown in the register map. Any other value can cause unexpected results.

**Table 3. Register Map**

| REGISTER NAME              | REGISTER DESCRIPTION                     | ADDRESS          | ACCESS | DEFAULT      |
|----------------------------|------------------------------------------|------------------|--------|--------------|
| <a href="#">CONFIG_A</a>   | Interface Configuration A                | 0x0000           | R/W    | 0x18         |
| <a href="#">CONFIG_B</a>   | Interface Configuration B                | 0x0001           | R/W    | 0x00         |
| Reserved                   | Reserved                                 | 0x0002           | R/W    | 0x00         |
| <a href="#">CHIP_TYPE</a>  | Chip Type                                | 0x0003           | RO     | 0x07         |
| <a href="#">CHIP_ID</a>    | Chip ID                                  | 0x0004<br>0x0005 | RO     | 0x00<br>0x04 |
| <a href="#">CHIP_REV</a>   | Chip Revision                            | 0x0006           | RO     | 0x01         |
| <a href="#">MFR_ID</a>     | Manufacturer ID                          | 0x000C<br>0x000D | RO     | 0x51<br>0x04 |
| <a href="#">REG_UPDATE</a> | Register Update                          | 0x000F           | R/W    | 0x00         |
| <a href="#">CONFIG_REG</a> | LMP92064 Specific Configuration Register | 0x0100           | R/W    | 0x00         |
| <a href="#">STATUS</a>     | Status Register                          | 0x0103           | RO     | N/A          |
| <a href="#">DATA_VOUT</a>  | Voltage Channel Output Data              | 0x0200<br>0x0201 | RO     | N/A          |
| <a href="#">DATA_COUT</a>  | Current Channel Output Data              | 0x0202<br>0x0203 | RO     | N/A          |

**Table 4. CONFIG\_A: Interface Configuration A**

| ADDR   | BIT 7 | BIT 6 | BIT 5   | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|-------|-------|---------|-------|-------|-------|-------|-------|
| 0x0000 | RESET | DDIR  | ADDRDIR | SDDIR |       |       |       |       |

|       |                        |                                                                                                       |     |
|-------|------------------------|-------------------------------------------------------------------------------------------------------|-----|
| [7]   | RESET <sup>(1)</sup>   | Soft reset (self-clearing)<br>0: Normal (default)<br>1: Reset                                         | R/W |
| [6]   | DDIR                   | Data direction<br>0: Data is transmitted MSB first (default)                                          | RO  |
| [5]   | ADDRDIR <sup>(2)</sup> | Multiple-read auto-address direction<br>0: Address auto-decrements (default)                          | RO  |
| [4]   | SDDIR                  | Serial data direction<br>1: Unidirectional; SDI is used for write and SDO is used for read (default)  | RO  |
| [3:0] |                        | Bits [3:0] should always mirror [7:4] as follows:<br>[3] = [4]<br>[2] = [5]<br>[1] = [6]<br>[0] = [7] | R/W |

(1) Contents of register 0x0000 and 0x0001 and SPI state machine are unaffected

(2) Address 0x0000 will wrap to 0x7FFF

**Table 5. CONFIG\_B: Interface Configuration B**

| ADDR   | BIT 7  | BIT 6    | BIT 5     | BIT 4    | BIT 3 | BIT 2    | BIT 1 | BIT 0    |
|--------|--------|----------|-----------|----------|-------|----------|-------|----------|
| 0x0001 | STREAM | Reserved | BUFREG_RD | Reserved |       | Reserved |       | Reserved |

|       |                          |                                             |  |  |  |  |  |     |
|-------|--------------------------|---------------------------------------------|--|--|--|--|--|-----|
| [7]   | STREAM                   | Stream                                      |  |  |  |  |  | RO  |
|       |                          | 0: Streaming is on (default)                |  |  |  |  |  |     |
| [6]   | Reserved                 | Reserved                                    |  |  |  |  |  | RO  |
|       |                          | 0 (default)                                 |  |  |  |  |  |     |
| [5]   | BUFREG_RD <sup>(1)</sup> | Active/buffered register read-back          |  |  |  |  |  | R/W |
|       |                          | 0: Read back from active register (default) |  |  |  |  |  |     |
|       |                          | 1: Read back from buffered register         |  |  |  |  |  |     |
| [4:3] | Reserved                 | Reserved                                    |  |  |  |  |  | RO  |
|       |                          | 00 (default)                                |  |  |  |  |  |     |
| [2:1] | Reserved                 | Reserved                                    |  |  |  |  |  | RO  |
|       |                          | 00 (default)                                |  |  |  |  |  |     |
| [0]   | Reserved                 | Reserved                                    |  |  |  |  |  | RO  |
|       |                          | 0 (default)                                 |  |  |  |  |  |     |

(1) Only double-buffered register affected: 0x0100

**Table 6. CHIP\_TYPE: Chip Type**

| ADDR   | BIT 7     | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|-----------|-------|-------|-------|-------|-------|-------|-------|
| 0x0003 | CHIP_TYPE |       |       |       |       |       |       |       |

|       |           |                     |  |  |  |  |  |    |
|-------|-----------|---------------------|--|--|--|--|--|----|
| [7:0] | CHIP_TYPE | Chip type           |  |  |  |  |  | RO |
|       |           | 0x07: Precision ADC |  |  |  |  |  |    |

**Table 7. CHIP\_ID: Chip ID LSB**

| ADDR   | BIT 7       | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 0x0004 | CHIP_ID_LSB |       |       |       |       |       |       |       |

|       |             |                             |  |  |  |  |  |    |
|-------|-------------|-----------------------------|--|--|--|--|--|----|
| [7:0] | CHIP_ID_LSB | Chip ID LSB                 |  |  |  |  |  | RO |
|       |             | 0x00 (Manufacturer defined) |  |  |  |  |  |    |

**Table 8. CHIP\_ID: Chip ID MSB**

| ADDR   | BIT 7       | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 0x0005 | CHIP_ID_MSB |       |       |       |       |       |       |       |

|       |             |                             |  |  |  |  |  |    |
|-------|-------------|-----------------------------|--|--|--|--|--|----|
| [7:0] | CHIP_ID_MSB | Chip ID MSB                 |  |  |  |  |  | RO |
|       |             | 0x04 (Manufacturer defined) |  |  |  |  |  |    |

**Table 9. CHIP\_REV: Chip Revision**

| ADDR   | BIT 7    | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|----------|-------|-------|-------|-------|-------|-------|-------|
| 0x0006 | CHIP_REV |       |       |       |       |       |       |       |

[7:0] CHIP\_REV      Chip REV      RO  
0x01

**Table 10. MFR\_ID: Manufacturer ID LSB**

| ADDR   | BIT 7      | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|------------|-------|-------|-------|-------|-------|-------|-------|
| 0x000C | MFR_ID_LSB |       |       |       |       |       |       |       |

[7:0] MFR\_ID\_LSB      Manufacturer ID LSB      RO  
0x51

**Table 11. MFR\_ID: Manufacturer ID MSB**

| ADDR   | BIT 7      | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|------------|-------|-------|-------|-------|-------|-------|-------|
| 0x000D | MFR_ID_MSB |       |       |       |       |       |       |       |

[7:0] MFR\_ID\_MSB      Manufacturer ID MSB      RO  
0x04

**Table 12. REG\_UPDATE: Register Update**

| ADDR   | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0         |
|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 0x000F |       |       |       |       |       |       |       | BUFREG_UPDATE |

[7:1] Reserved      Reserved      RO  
0 (default)

[0] BUFREG\_UPDATE<sup>(1)</sup>      Buffered register update (self clearing)      R/W  
0: No action (default)  
1: Transfer buffered register contents to active register

(1) Register 0x0100 is buffered.

**Table 13. CONFIG\_REG: Lmp92064 Specific Configuration Register**

| ADDR   | BIT 7    | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|----------|-------|-------|-------|-------|-------|-------|-------|
| 0x0100 | Reserved |       |       |       |       |       |       |       |

[7:0] Reserved<sup>(1)</sup>      Reserved for future use      R/W  
0x00 (default)

(1) This register is double-buffered; register 0x000F must be set to 1 to transfer the contents from the buffer to the active register.

**Table 14. STATUS: Status Register**

| ADDR   | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0  |
|--------|-------|-------|-------|-------|-------|-------|-------|--------|
| 0x0103 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | STATUS |

[7:1] Unused      Unused      RO  
Always read 7'b0

[0] STATUS      Status      RO  
0: Device is not ready for conversion  
1: Device is ready for conversion

**Table 15. DATA\_VOUT: Voltage Channel Output Data LSB**

| ADDR   | BIT 7         | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|---------------|-------|-------|-------|-------|-------|-------|-------|
| 0x0200 | VOUT_DATA_LSB |       |       |       |       |       |       |       |

[7:0] VOUT\_                      Voltage output data least significant byte                      RO  
DATA\_LSB

**Table 16. DATA\_VOUT: Voltage Channel Output Data MSB**

| ADDR   | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3         | BIT 2 | BIT 1 | BIT 0 |
|--------|-------|-------|-------|-------|---------------|-------|-------|-------|
| 0x0201 | 0     | 0     | 0     | 0     | VOUT_DATA_MSB |       |       |       |

[7:4] Unused                      Unused                      RO  
0000 (default)

[3:0] VOUT\_                      Voltage output data most significant byte                      RO  
DATA\_MSB

**Table 17. DATA\_COUT: Current Channel Output Data LSB**

| ADDR   | BIT 7         | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------|---------------|-------|-------|-------|-------|-------|-------|-------|
| 0x0202 | COUT_DATA_LSB |       |       |       |       |       |       |       |

[7:0] COUT\_                      Current output data least significant byte                      RO  
DATA\_LSB

**Table 18. DATA\_COUT: Current Channel Output Data MSB**

| ADDR   | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3         | BIT 2 | BIT 1 | BIT 0 |
|--------|-------|-------|-------|-------|---------------|-------|-------|-------|
| 0x0203 | 0     | 0     | 0     | 0     | COUT_DATA_MSB |       |       |       |

[7:4] Unused                      Unused                      RO  
0000 (default)

[3:0] COUT\_                      Current output data most significant byte                      RO  
DATA\_MSB

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. The device is typically used to measure a load current by means of a current sense resistor connected in series with a load. Use the following design procedure to select the main components of a simple current and voltage monitoring application using the LMP92064.

### 8.2 Typical Application

In this example, the LMP92064 is used to sense the load current flowing through the sense resistor, R1. Additionally, the voltage across R3 can be sensed to calculate the bus voltage.

The load that will be monitored is operating from a  $-48\text{-V}$  bus. Because the GND pin of the LMP92064 is connected to the  $-48\text{-V}$  bus,  $-48\text{ V}$  becomes the ground reference for the device.

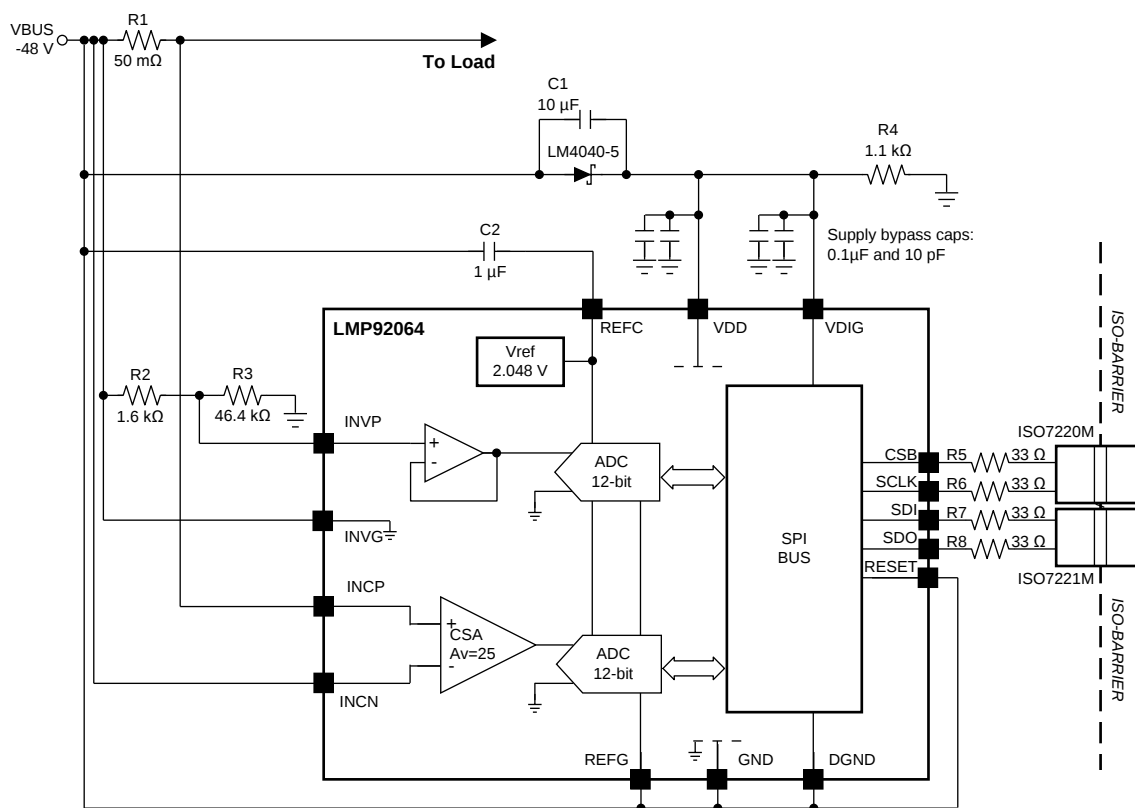


Figure 23. Typical Application Diagram

## Typical Application (continued)

### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 19](#) as the application parameters.

**Table 19. Design Parameters**

| DESIGN PARAMETER      | EXAMPLE VALUE |
|-----------------------|---------------|
| Bus Voltage           | -48 V         |
| Bus Voltage Variation | ±2%           |
| Supply Voltage        | 5 V           |
| SPI Clock             | 12 MHz        |
| Maximum Load Current  | 1 A           |
| Resolution            | 1 mA          |

### 8.2.2 Detailed Design Procedure

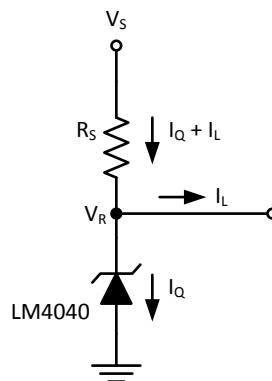
#### 8.2.2.1 Digital Isolators

The ISO7220M and ISO7221M isolators are used for this example. Please refer to the ISO722x documentation for device specific information. These devices support data rates of up to 150 Mbps and provide a low propagation delay necessary for bi-directional SPI communication at 12 MHz.

#### 8.2.2.2 Supply Voltage for the LMP92064

A 5-V supply is required for the LMP92064. The LM4040-5 reference is used to generate the required voltage from the load's -48-V supply. The LM4040-N is a precision micropower shunt voltage reference and is available in several fixed breakdown voltage options. The LM4040-5 provides the required 5-V breakdown voltage.

In a conventional shunt regulator application ([Figure 24](#)), the LM4040-5 requires a current limiting resistor connected between the positive supply voltage and the LM4040-5.



**Figure 24. Shunt Regulator**

The value of the resistor is determined by the positive supply voltage ( $V_S$ ), the load current ( $I_L$ ), the reference operating current ( $I_Q$ ), and the LM4040-5's reverse breakdown voltage ( $V_R$ ).

$$R_S = \frac{V_S - V_R}{I_L + I_Q} \quad (1)$$

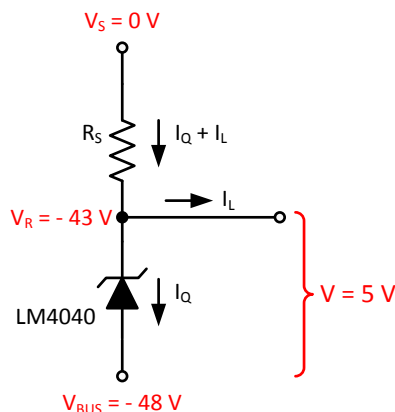
### 8.2.2.3 Series Resistor for the Shunt Regulator

The selection of  $R_S$  should satisfy two main conditions:

- $R_S$  should be small enough to supply at least the minimum acceptable  $I_Q$  to the LM4040-5 even when the supply voltage is at its minimum and the load current is at its maximum value.
- $R_S$  should be large enough so that the current flowing through the LM4040-5 is less than 15 mA when the supply voltage is at its maximum and the load current is at its minimum.

The minimum operating current of the LM4040AIM3-5/NOPB is 80  $\mu$ A and its maximum operating current is 15 mA.

The typical supply current of the LMP92064 is 13 mA. The measured average current of the circuit, including the isolators, is 38 mA.



**Figure 25. Shunt Regulator Voltages**

From Figure 25,  $V_S = 0$  V and  $V_R = -43$  V.  $R_S$  can be calculated as follows:

$$R_S = \frac{0 \text{ V} - (-43 \text{ V})}{38 \text{ mA} + 80 \mu\text{A}} = 1129 \Omega \quad (2)$$

Choosing a smaller resistor, like a 1.1-k $\Omega$  resistor, will result in about 39.1 mA to flowing through  $R_S$ , providing a margin of 1 mA above the required 38.08 mA.

A variation in the bus voltage ( $V_{BUS}$ ) of  $\pm 2\%$  would result in less than  $\pm 0.87$  mA of current variation. Given the additional current margin obtained by the 1.1-k $\Omega$  resistor, the shunt regulator would still have more than the required 80  $\mu$ A of operating current.

The power rating of the series resistor should be selected according to the expected power to be dissipated. In normal operation, the resistor would dissipate  $43 \text{ V} \times 39 \text{ mA} = 1.677 \text{ W}$ .

Excess current not used by the LMP92064 and isolators circuits will be burned by in the LM4040-5, and this current should never exceed 15 mA.

### 8.2.2.4 Voltage Channel Input Resistor Divider

The input buffer amplifier of the LMP92064's voltage channel can tolerate high source impedances, which enables scaling the bus voltage with the use of an external resistor divider. The accuracy of the voltage measurements depends on the accuracy of the components used for the resistor divider as well as the impedance of the divider.

In this example, the voltage channel can sense the voltage across  $R_2$  (see Figure 23). The main voltage should be scaled to a range below 2.048V by the resistive divider. If the resistive divider is always connected to the bus voltage, the series resistance of  $R_2 + R_3$  should be adjusted (while keeping their ratio constant) to limit the current across the resistors within a permissible range for the application.

For simplicity,  $R_2$  is set to 1.6k $\Omega$  and  $R_3$  is set to 46.4 k $\Omega$ . The bus voltage of 48 V results in 1.6 V across  $R_2$  and the current flowing through  $R_2$  and  $R_3$  is 1 mA.

### 8.2.2.5 Sense Resistor Selection

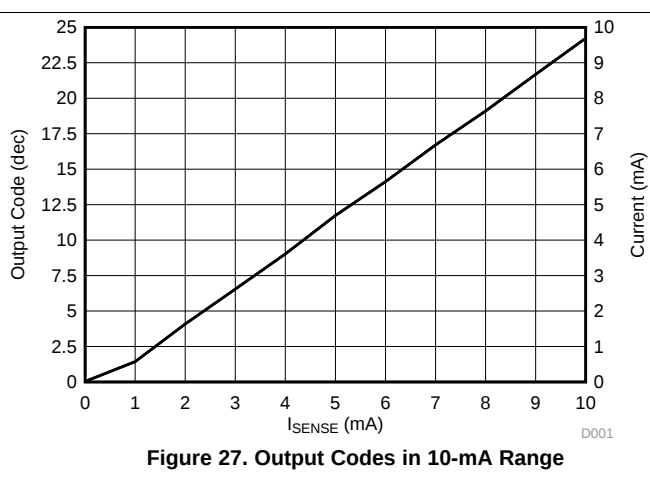
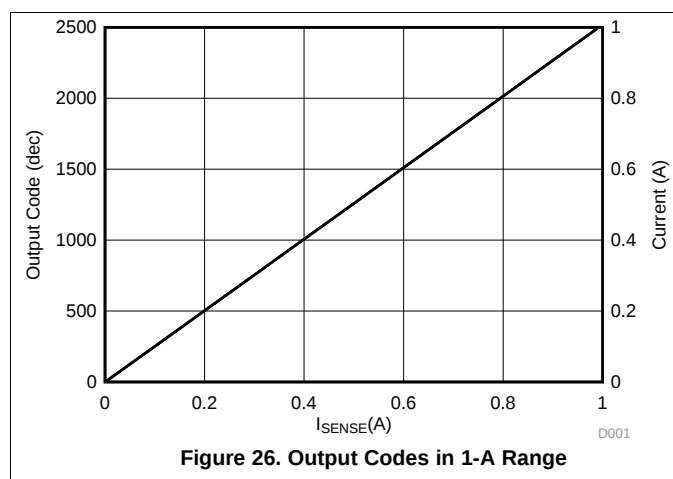
The accuracy of the current measurement depends heavily on the accuracy of the current sense resistor. Its value depends on the application and it is a compromise between signal accuracy, maximum permissible voltage loss and power dissipation in the current sense resistor. High resistance values provide better accuracy at lower currents by minimizing the effects of offset, while low resistance values of minimize voltage loss in the load supply section, but at the expense of low-end accuracy.

In this example, the maximum sense voltage at the input of the current sense channel of the LMP92064 is 75 mV. Given the maximum load current requirement of 1 A, the sense resistor should be selected to be smaller than 75 mΩ.

The resolution at the input of the current sense channel of the device is 20 μV / code. To observe a change in the output code for a 1 mA change in sense current, the sense resistor should be larger than 20 mΩ.

### 8.2.3 Application Curves

The data in the following curves was collected using a 50 mΩ sense resistor, which results in a conversion factor of 2.5 codes/mA. The sense current for the first curve was increased in steps of 100 mA up to 1 A. The sense current for the second curve was increased in steps of 1 mA up to 10 mA. The data was acquired asynchronously at a rate of 2000 samples per second, and each data point is the resulting average of 260 samples.



## 9 Power Supply Recommendations

To decouple the LMP92064 from AC noise on the power supply, it is recommended to use a 0.1- $\mu$ F bypass capacitor between the VDD and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10- $\mu$ F bypass capacitor may further reduce the supply noise. In addition, the VDIG power pin should also be decoupled to DGND with a 0.1- $\mu$ F bypass capacitor. Do not forget that these capacitors must be rated for the full supply voltage (2x the maximum voltage is recommended for the capacitor working voltage rating).

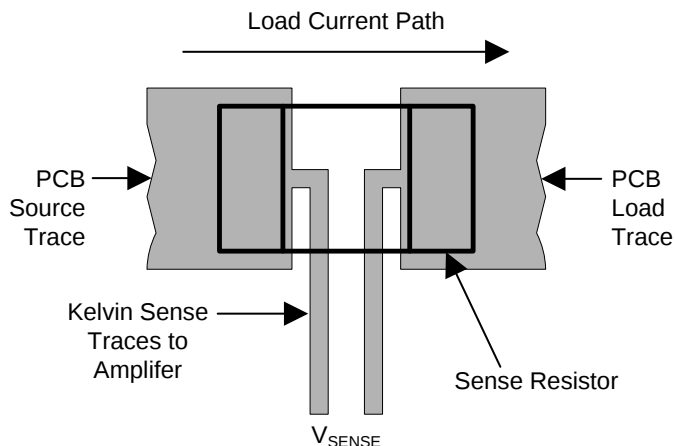
## 10 Layout

### 10.1 Layout Guidelines

- Connect the sense resistor pads directly to the INCP and INCN inputs of the LMP92064 using “Kelvin” or “4-wire” connection techniques. See the [Current Input Error Sources and Layout Considerations](#) section for more information.
- Bypass capacitors should be placed in close proximity to the supply pins. It is recommended to use a 0.1- $\mu$ F capacitor on each supply pin. Additional bypass capacitors can be used.
- A 1- $\mu$ F ceramic bypass capacitor should be placed in close proximity to the REFC pin.
- The SPI signals traces should be routed close together.
- Series resistors should be placed at the SPI sources.

#### 10.1.1 Current Input Error Sources

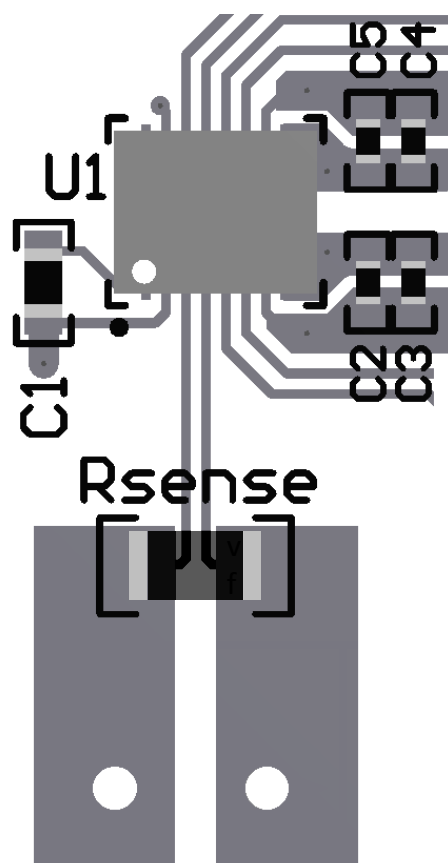
The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (<100 m $\Omega$ ), trace resistance shared with the load can cause significant errors. TI recommends connecting the sense resistor pads directly to the INCP and INCN inputs of the LMP92064 using “Kelvin” or “4-wire” connection techniques. An example is shown in [Figure 28](#).



**Figure 28. 4-Wire "Kelvin" Sensing Technique**

Because the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. The traces should be one continuous piece of copper from the sense resistor pad to the LMP92064 input pin pad, and ideally on the same layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat. To minimize noise pickup and thermal errors, the input traces should be treated as a signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines.

## 10.2 Layout Example



**Figure 29. Layout Schematic**

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LMP92064SD/NOPB</a>  | Active        | Production           | WSO (NHR)   16 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |
| LMP92064SD/NOPB.A                | Active        | Production           | WSO (NHR)   16 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |
| <a href="#">LMP92064SDE/NOPB</a> | Active        | Production           | WSO (NHR)   16 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |
| LMP92064SDE/NOPB.A               | Active        | Production           | WSO (NHR)   16 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |
| <a href="#">LMP92064SDX/NOPB</a> | Active        | Production           | WSO (NHR)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |
| LMP92064SDX/NOPB.A               | Active        | Production           | WSO (NHR)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 105   | L92064              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP92064SD/NOPB  | WSO          | NHR             | 16   | 1000 | 177.8              | 12.4               | 4.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |
| LMP92064SDE/NOPB | WSO          | NHR             | 16   | 250  | 177.8              | 12.4               | 4.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |
| LMP92064SDX/NOPB | WSO          | NHR             | 16   | 4500 | 330.0              | 12.4               | 4.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP92064SD/NOPB  | WSO          | NHR             | 16   | 1000 | 208.0       | 191.0      | 35.0        |
| LMP92064SDE/NOPB | WSO          | NHR             | 16   | 250  | 208.0       | 191.0      | 35.0        |
| LMP92064SDX/NOPB | WSO          | NHR             | 16   | 4500 | 356.0       | 356.0      | 36.0        |



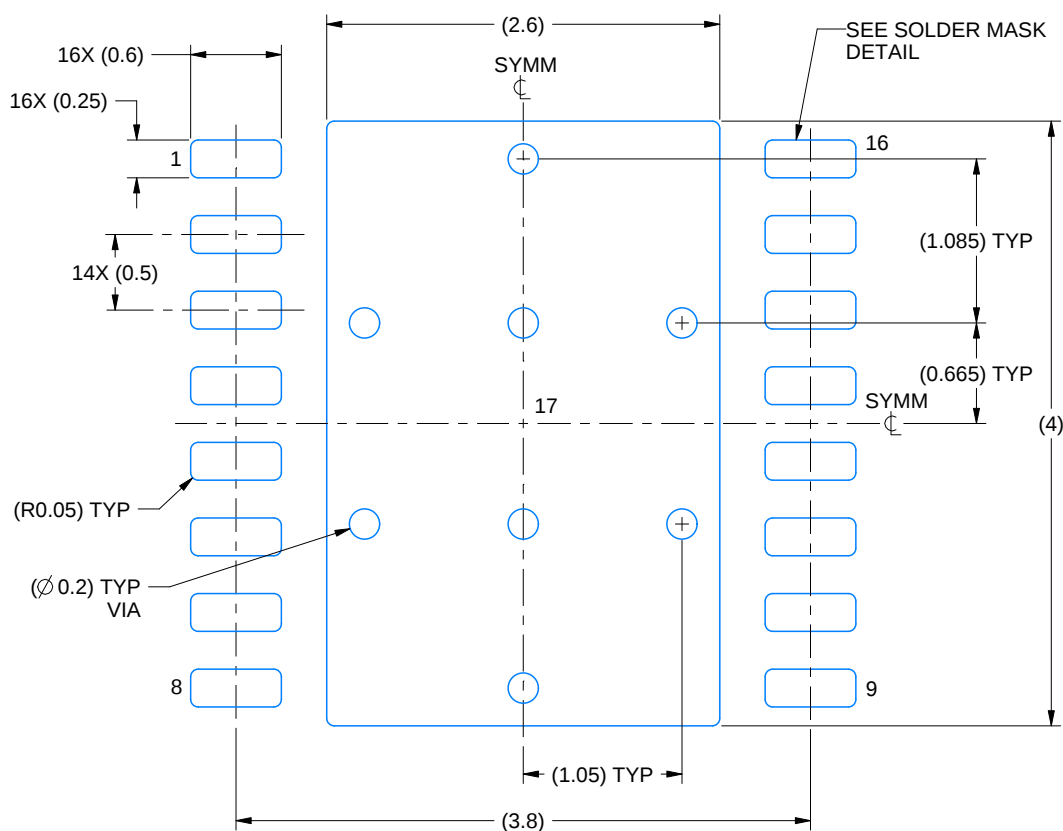
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

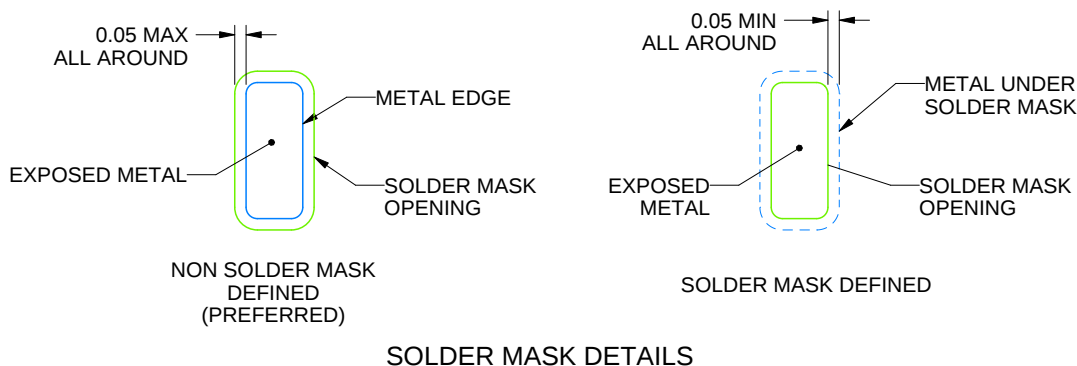
NHR0016B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4214932/B 08/2025

NOTES: (continued)

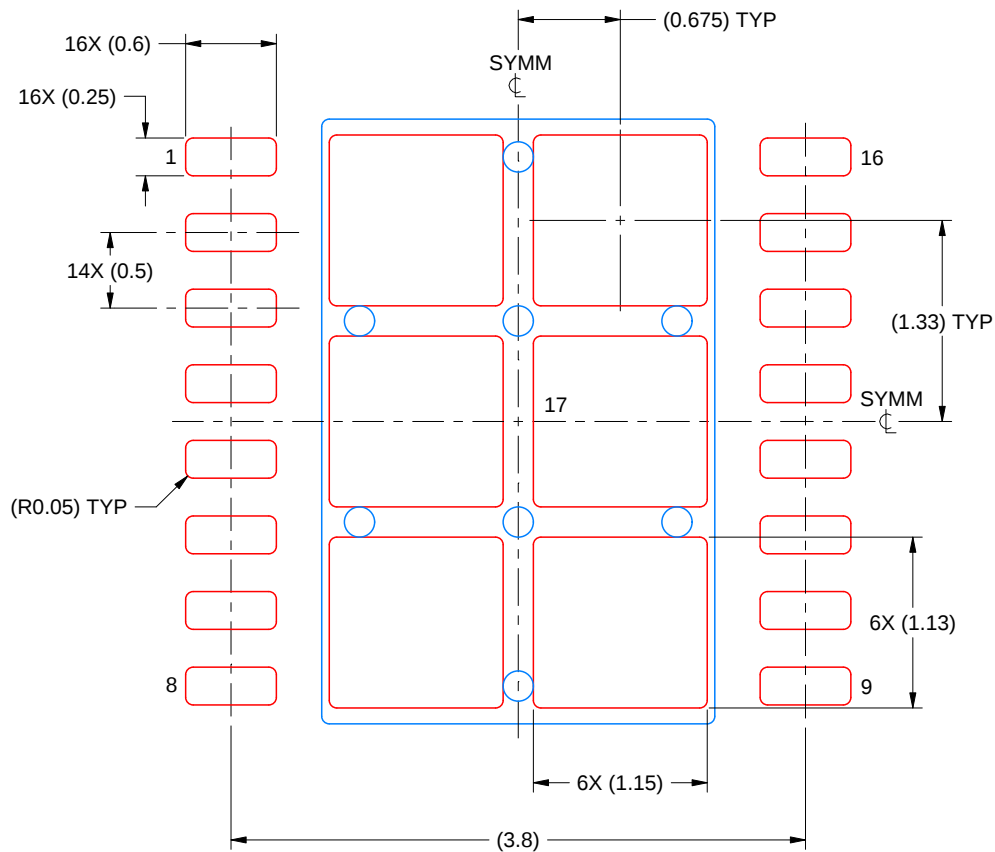
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

NHR0016B

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4214932/B 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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