TEXAS INSTRUMENTS
LMK60E2-150M, LMK60E0-156257
LMK60A0-148351, LMK60A0-148M
JAJSCC0C – JUNE 2016 – REVISED NOVEMBER 2017

LMK60XX 高性能低ジッタ発振器

1 特長

- 低ノイズ、高性能
  - ジッタ: 150fs RMS (標準値)、Fout > 100MHz
  - PSRR: –60dBc、堅牢な電源ノイズ耐性
- 対応出力フォーマット
  - LVPECLおよびLVDS: 最高800MHz
  - HCSL: 最大400MHz
- 合計周波数公差：±50ppm (LMK60X2)、±25ppm (LMK60X0)
- 動作電圧: 3.3V
- 工業用温度範囲: -40℃～+85℃
- 7mm× 5mmの6ピン・パッケージ、業界標準の7050 XOパッケージとピン互換

2 アプリケーション

- 水晶振動子、SAW、またはシリコン・ベースの発振器に代わる高性能の代替品
- スイッチ、ルータ、ネットワーク・ライン・カード、ベースバンド・ユニット(BBU)、サーバ、ストレージ/SAN
- 試験/測定機器
- 医療用画像処理
- FPGA、プロセッサ接続

3 概要

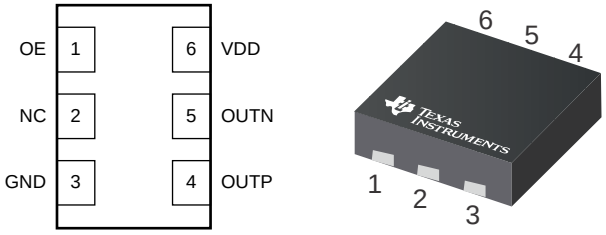
LMK60XXデバイスは低ジッタの発振器で、一般的に使用されるリファレンス・クロックを生成します。このデバイスは、任意のリファレンス・クロック周波数をサポートするよう工場であらかじめプログラムされ、出力フォーマットとしてLVPECLおよびLVDSで最高800MHz、HCSLで最高400MHzをサポートします。内部的な電力コンディショニングにより、電源リップル除去(PSRR)が非常に優れているため、電力供給ネットワークのコストと複雑性を減らすことができます。単一の3.3V±5%電源で動作します。

製品情報(1)

型番	出力周波数(MHz)とフォーマット	総合周波数安定性(ppm)	パッケージ/サイズ
LMK60E2-150M	150 LVPECL	±50	6ピンQFM、7mm×5mm
LMK60E0-156257	156.257 LVPECL	±25	
LMK60A0-148351	148 + 32/91 LVDS	±25	
LMK60A0-148M	148.5 LVDS	±25	

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ピン配置



目次

4 改訂履歴

Revision B (December 2016) から **Revision C** に変更 **Page**

- LMK60A0-148351の新規リリース ... 1
- LMK60A0-148Mの新しいリリース ... 1

Revision A (August 2016) から **Revision B** に変更 **Page**

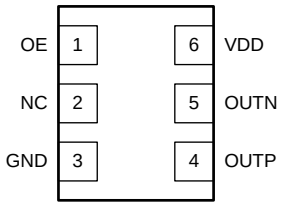
- LMK60E2-150M00をLMK60E2-150Mに変更 ... 1
- LMK60E2-156Mを削除し、独立のデータシートに移動 ... 1

2016年6月発行のものから更新 **Page**

- LMK60E0-156257の新規リリース ... 1

5 Pin Configuration and Functions

SIA Package
6-pin QFM
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device ground
VDD	6	Analog	3.3-V power supply
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential output pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No connect
OE	1	LVCMOS	Output enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			120	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC(1)		LMK60XX (2) (3) (4) SIA (QFM) 6 PINS			UNIT
		Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.2	46.4	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	n/a	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.7	n/a	n/a	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	17.6	22.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	41.5	40.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4 layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3-mm diameter).
(4) ψJB (junction to board) is used when the main heat flow is from the junction to the GND pad. See the *Layout Guidelines* section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL(2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device current consumption when output is disabled	OE = GND		136		mA

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 Ω termination resistors, from total power dissipation.

6.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)		10		800	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\lvert V_{OD} \rvert$		V
V_{OS}	Output common-mode voltage			VDD – 1.55		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			150	250	ps
ODC	Output duty cycle(3)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

6.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(1)		10		800	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\|V_{OD}\|$		V
V_{OS}	Output common-mode voltage			1.2		V
t_R / t_F	Output rise/fall time (20% to 80%)(2)			150	250	ps
ODC	Output duty cycle(2)		45%		55%	
R_{OUT}	Differential output impedance			125		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

6.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		10		400	MHz
V_{OH}	Output high voltage		600		850	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage(2)(3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew rate(4)		0.8		2	V/ns
ODC	Output duty cycle(4)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

6.10 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	LMK60X2: All output formats, frequency bands and device junction temperature up to 125°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (10 years)	–50		50	ppm
		LMK60X0: All output formats, frequency bands and device junction temperature up to 115°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (5 years at 40°C)	–25		25	ppm

(1) Ensured by characterization.

6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable voltage droop(2)				0.1	V
$t_{STARTUP}$	Start-up time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Ensured by characterization.
(2) Ensured by design.

6.12 PSRR Characteristics(1)

VDD = 3.3 V, T_A = 25°C, FS[1:0] = NC, NC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple(2)(3) at 156.25-MHz output, all output types	Sine wave at 50 kHz		–60		dBc
		Sine wave at 100 kHz		–60		
		Sine wave at 500 kHz		–60		
		Sine wave at 1 MHz		–60		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π*f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.13 PLL Clock Output Jitter Characteristics(1)(2)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter(3) (12 kHz – 20 MHz)	f_{OUT} ≥ 100 MHz, All output types		150	250	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

6.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.15 Typical Characteristics

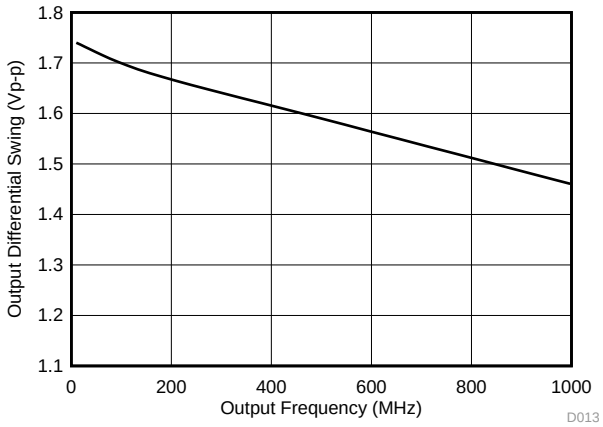


Figure 1. LVPECL Differential Output Swing vs Frequency

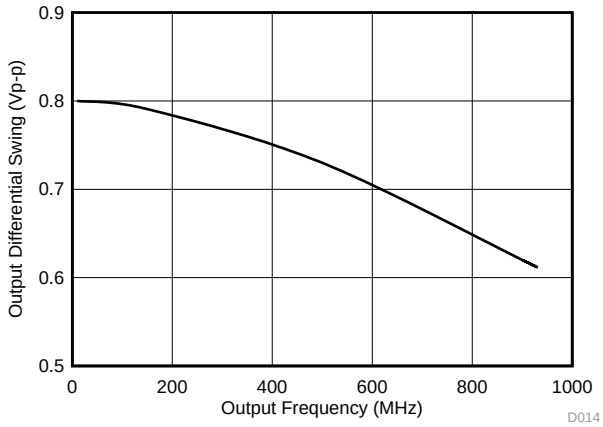


Figure 2. LVDS Differential Output Swing vs Frequency

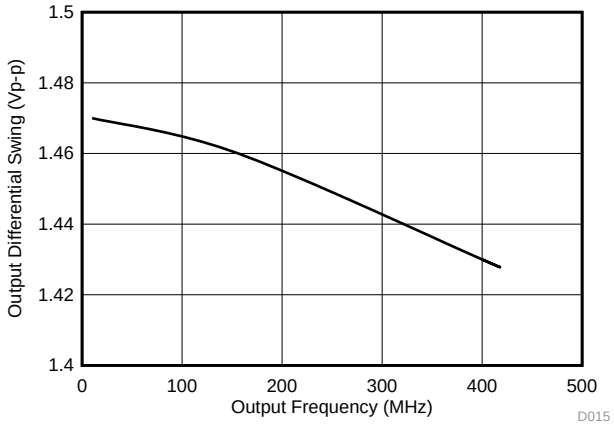


Figure 3. HCSL Differential Output Swing vs Frequency

7 Parameter Measurement Information

7.1 Device Output Configurations

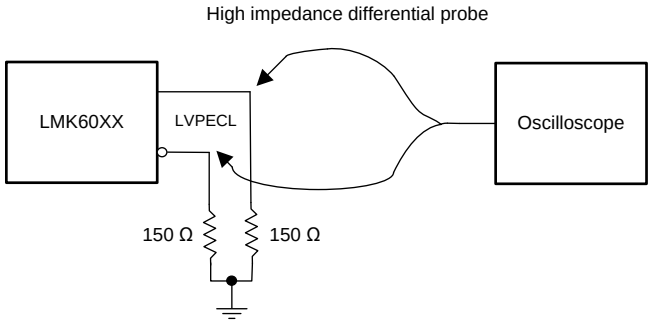


Figure 4. LVPECL Output DC Configuration During Device Test

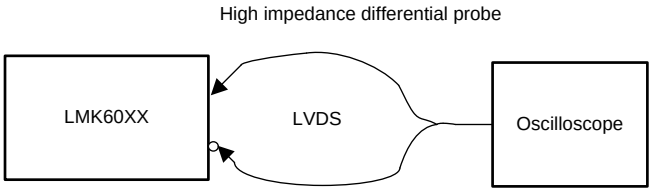


Figure 5. LVDS Output DC Configuration During Device Test

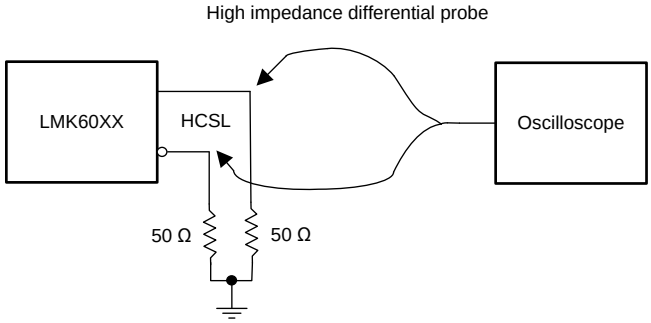


Figure 6. HCSL Output DC Configuration During Device Test

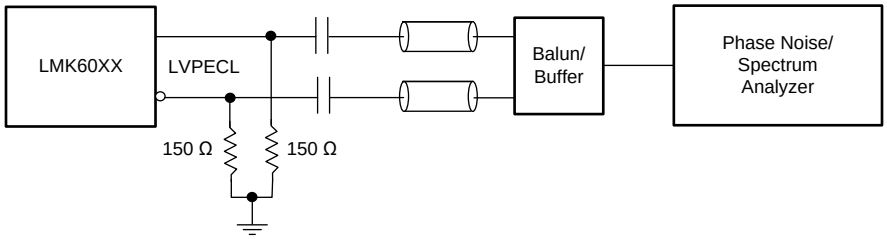


Figure 7. LVPECL Output AC Configuration During Device Test

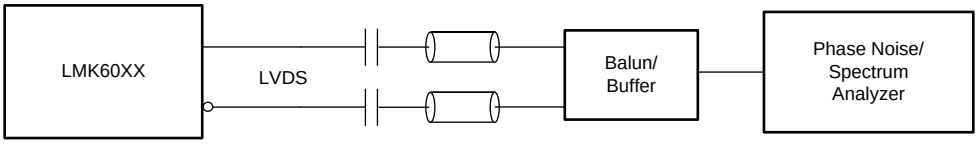


Figure 8. LVDS Output AC Configuration During Device Test

Device Output Configurations (continued)

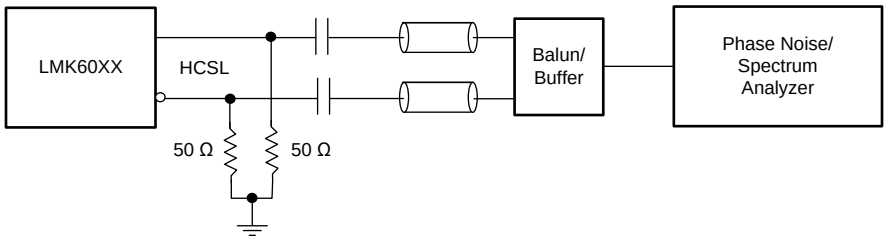


Figure 9. HCSL Output AC Configuration During Device Test

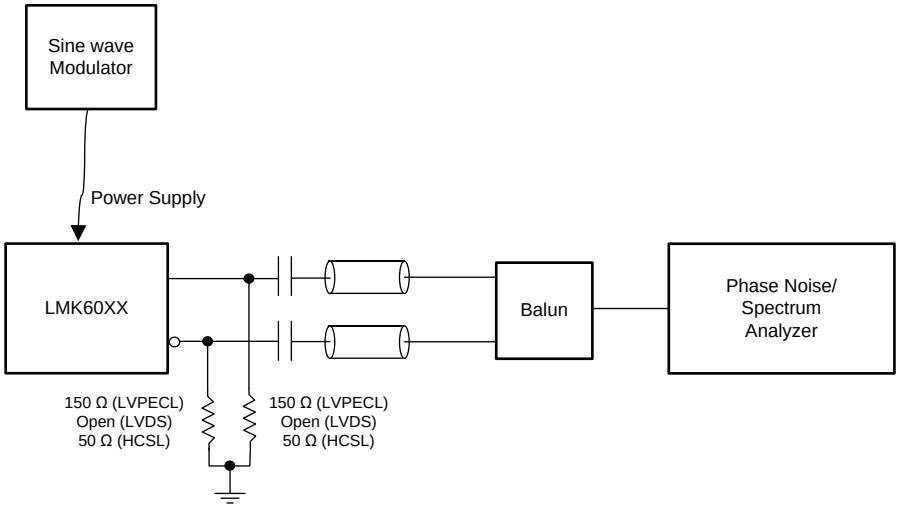


Figure 10. PSRR Test Setup

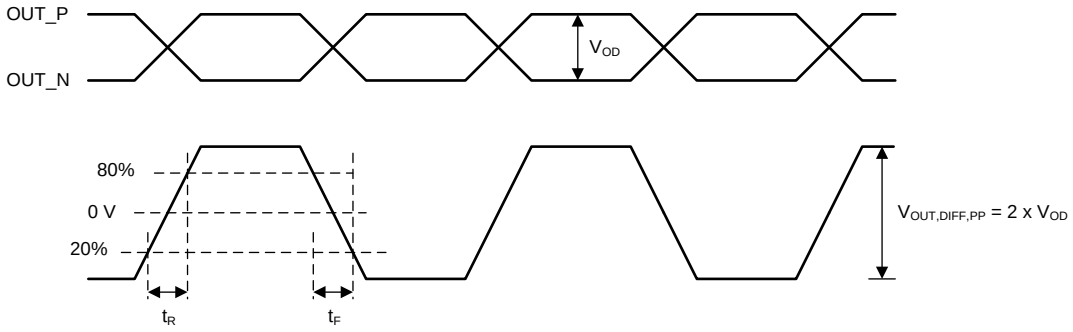


Figure 11. Differential Output Voltage and Rise/Fall Time

8 Power Supply Recommendations

For best electrical performance of LMK60XX, TI recommends using a combination of 10 µF, 1 µF and 0.1 µF on its power supply bypass network. TI also recommends using component side mounting of the power supply bypass capacitors, and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 12 shows the layout recommendation for power supply decoupling of LMK60XX.

9 Layout

9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK60XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

9.1.1 Ensuring Thermal Reliability

The LMK60XX is a high performance device. Therefore pay careful attention to device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in Figure 12, to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK60XX and its junction temperature.

$$T_B = T_J – \Psi_{JB} * P \quad (1)$$

where

- T_B: PCB temperature around the LMK60XX
- T_J: Junction temperature of LMK60XX
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK60XX (37.7°C/W without airflow)
- P: On-chip power dissipation of LMK60XX

To ensure that the maximum junction temperature of LMK60XX is below 120°C, it can be calculated that the maximum PCB temperature without airflow should be at 90°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK60XX, TI recommends routing vias into decoupling capacitors and then into the LMK60XX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high-frequency current flow. Figure 12 shows the layout recommendation for LMK60XX.

Layout Guidelines (continued)

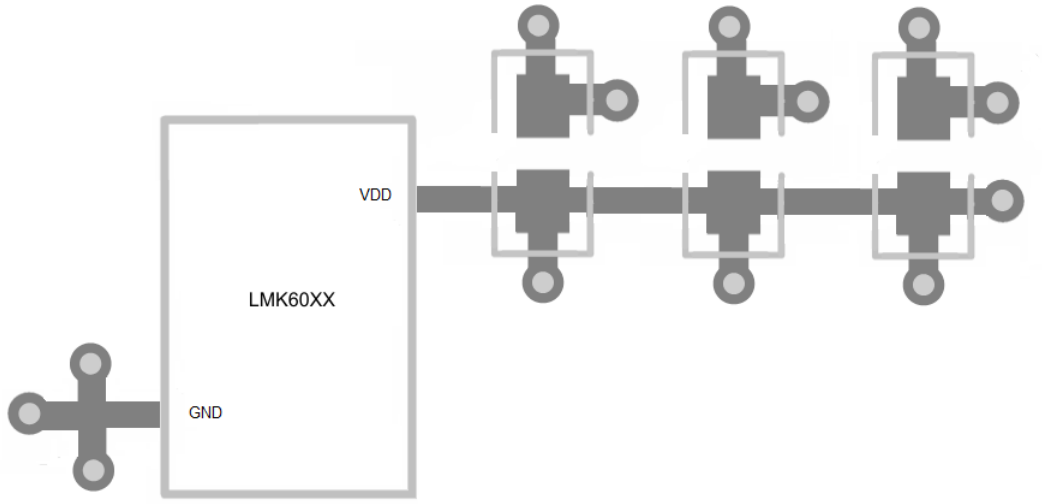


Figure 12. LMK60XX Layout Recommendation for Power Supply and Ground

9.1.3 Recommended Solder Reflow Profile

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK60XX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

10 デバイスおよびドキュメントのサポート

10.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMK60E2-150M	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMK60E0-156257	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

10.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

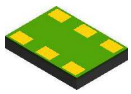
10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

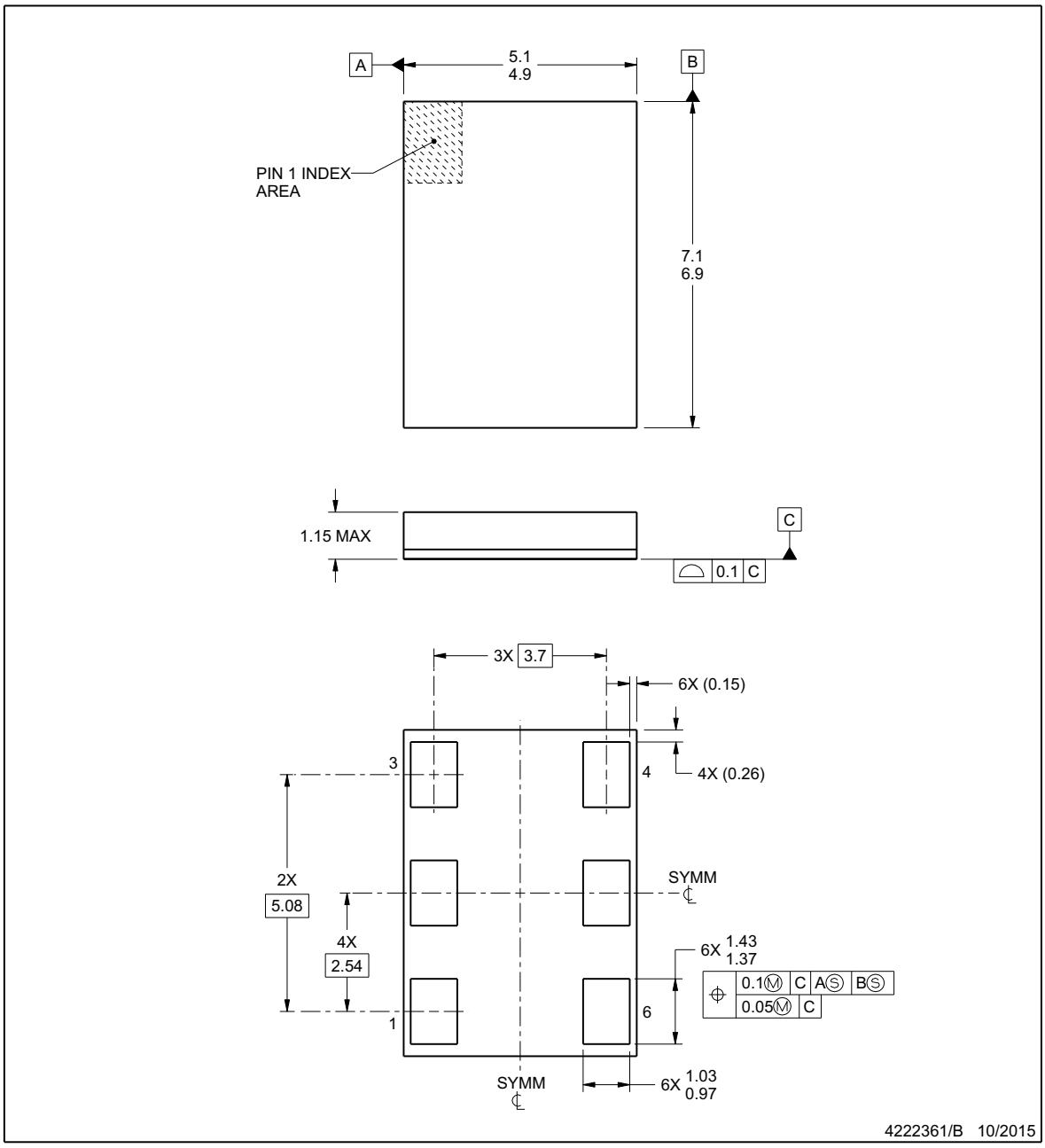


PACKAGE OUTLINE

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



NOTES:

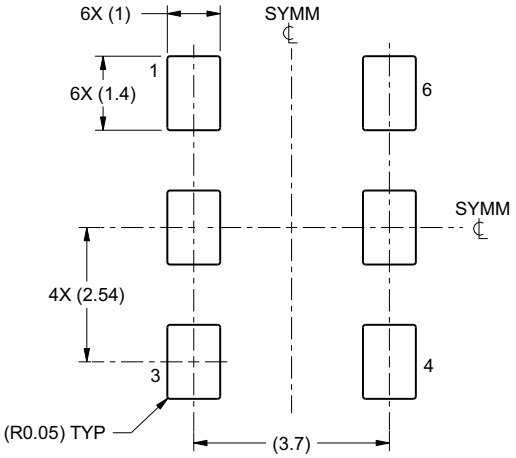
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

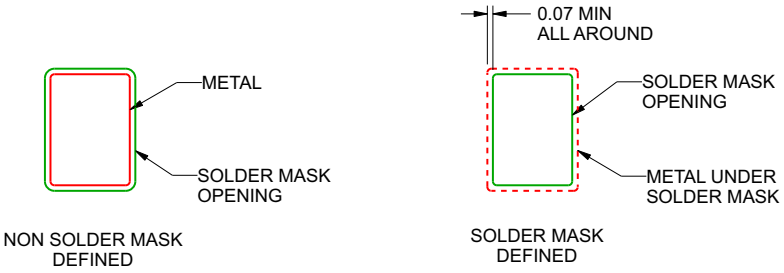
SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4222361/B 10/2015

NOTES: (continued)

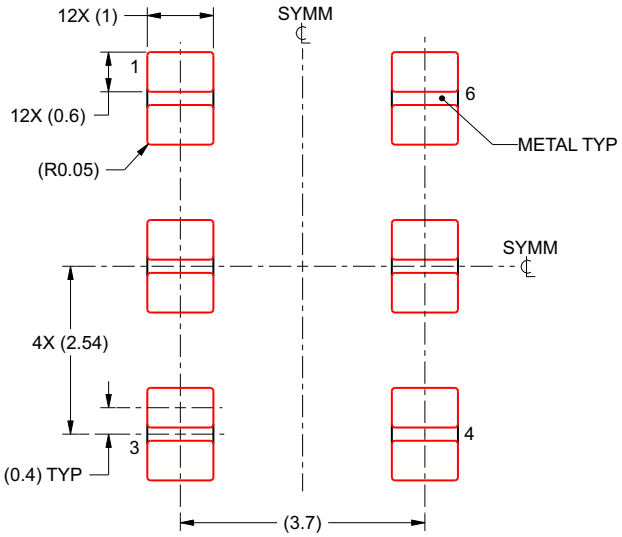
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 86%
SCALE:10X

4222361/B 10/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK60A0-148M35SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M35SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M50SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M50SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60E0-156257SIAR	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAR.A	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAR.B	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60E0-156257SIAT	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAT.A	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAT.B	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60E2-150M00SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK60E2-150M00SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月