LMK1D121x 低付加ジッタ LVDS バッファ

1 特長

- 高性能 LVDS クロック・バッファ・ファミリ：最大 2GHz
  - 2:12 差動バッファ (LMK1D1212)
  - 2:16 差動バッファ (LMK1D1216)
- 電源電圧：1.71V ~ 3.465V
- 小さい付加ジッタ：156.25MHz 時、12kHz ~ 20MHz の範囲で最大 60fs RMS
  - 非常に小さい位相ノイズフロア：-164dBc/Hz (標準値)
- 非常に小さい伝搬遅延：575ps (最大値)
- 出力スキュー：20ps (最大値)
- 高スイング LVDS (昇圧モード)：AMP_SEL = 1 の場合、500mV VOD (標準値)
- ユニバーサル入力は LVDS、LVPECL、LVCMOS、HCSL、CML の信号レベルに対応
- LVDS リファレンス電圧 V_{AC_REF} は、容量性結合入力に使用可能
- 産業用温度範囲：-40℃ ~ 105℃
- 以下に示すパッケージで供給
  - LMK1D1212：6mm × 6mm、40 ピン VQFN (RHA)
  - LMK1D1216：7mm × 7mm、48 ピン VQFN (RGZ)

2 アプリケーション

- テレコミュニケーションおよびネットワーク機器
- 医療用画像処理
- 試験 / 測定機器
- ワイヤレス・インフラ
- 業務用オーディオ、ビデオ、サイネージ

3 概要

LMK1D1212 クロック・バッファは、2 つのクロック入力 (IN0 および IN1) のいずれか 1 つを 12 ペアの差動 LVDS クロック出力 (OUT0 ~ OUT11) に分配します。このとき、クロック分配のスキューを最小限に抑えます。同様に LMK1D1216 は、16 ペアの差動 LVDS クロック出力 (OUT0 ~ OUT15) に分配します。LMK1D121x ファミリは、入力マルチプレクサに 2 つのクロック源を接続できます。入力は、LVDS、LVPECL、LP-HCSL、HCSL、CML、LVCMOS のいずれかに対応可能です。

LMK1D121x は、50Ω 伝送経路の駆動に特化して設計されています。シングルエンド・モードで入力を駆動する場合は、未使用の負入力ピンに適切なバイアス電圧を印加する必要があります (図 9-6 参照)。

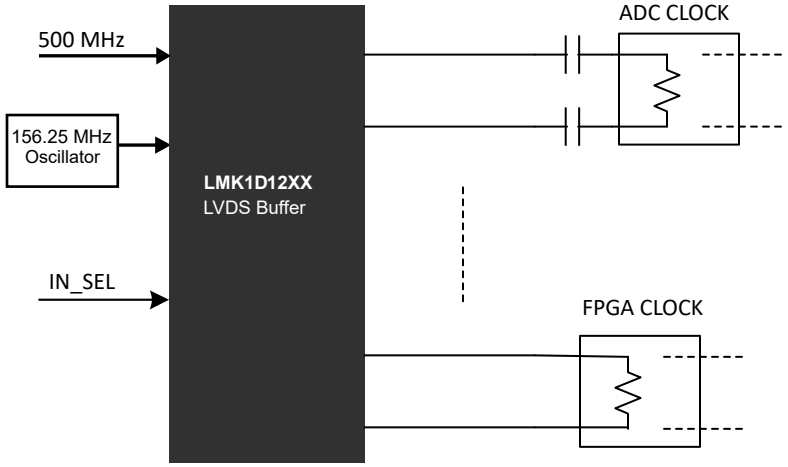
IN_SEL ピンは、どの入力を出力に転送するかを選択します。このピンがオープンのままの場合、出力はディセーブルになります (静的ロジック LOW)。このデバイスは、フェイルセーフ機能をサポートしています。さらに、このデバイスは入力ヒステリシスを備えており、入力信号が存在しないときに出力がランダムに発振することを防止します。

このデバイスは、1.8V、2.5V または 3.3V 電源で動作し、-40℃ ~ 105℃ (周囲温度) で動作が規定されています。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
LMK1D1212	VQFN (40)	6.00mm × 6.00mm
LMK1D1216	VQFN (48)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーションの例

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2021) to Revision A (April 2023)	Page
• Added Device Comparison Table for TI LMK1D devices	3
• Changed the LMK1D1212 IN0_N pin number from pin 9 to pin 8	4
• Changed the LMK1D1212 IN0_P pin number from pin 8 to pin 9	4
• Changed the LMK1D1216 IN0_N pin number from pin 10 to pin 9	4
• Changed the LMK1D1216 IN0_P pin number from pin 9 to pin 10	4
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	21

5 Device Comparison Table

Device	Device Type	Features	Output Swing	Package	Body Size
LMK1D2108	Dual 1:8	Global output enable and swing control via pin control	350 mV 500 mV	VQFN (48)	7.00 mm x 7.00 mm
LMK1D2106	Dual 1:6	Global output enable and swing control via pin control	350 mV 500 mV	VQFN (40)	6.00 mm x 6.00 mm
LMK1D2104	Dual 1:4	Global output enable and swing control via pin control	350 mV 500 mV	VQFN (28)	5.00 mm x 5.00 mm
LMK1D2102	Dual 1:2	Global output enable and swing control via pin control	350 mV 500 mV	VQFN (16)	3.00 mm x 3.00 mm
LMK1D1216	2:16	Global output enable control via pin control	350 mV 500 mV	VQFN (48)	7.00 mm x 7.00 mm
LMK1D1212	2:12	Global output enable control via pin control	350 mV 500 mV	VQFN (40)	6.00 mm x 6.00 mm
LMK1D1208P	2:8	Individual output enable control via pin control	350 mV 500 mV	VQGN (40)	6.00 mm x 6.00 mm
LMK1D1208I	2:8	Individual output enable control via I2C	350 mV 500 mV	VQFN (40)	6.00 mm x 6.00 mm
LMK1D1208	2:8	Global output enable control via pin control	350 mV	VQFN (28)	5.00 mm x 5.00 mm
LMK1D1204P	2:4	Individual output enable control via pin control	350 mV	VQGN (28)	5.00 mm x 5.00 mm
LMK1D1204	2:4	Global output enable control via pin control	350 mV	VQFN (16)	3.00 mm x 3.00 mm

6 Pin Configuration and Functions

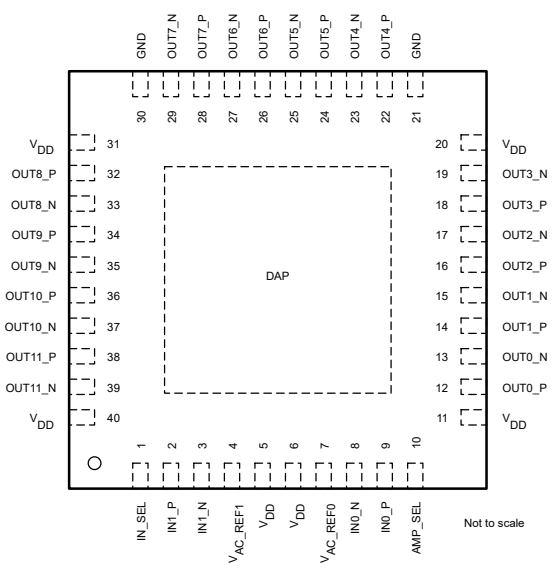


図 6-1. LMK1D1212: RHA Package 40-Pin VQFN Top View

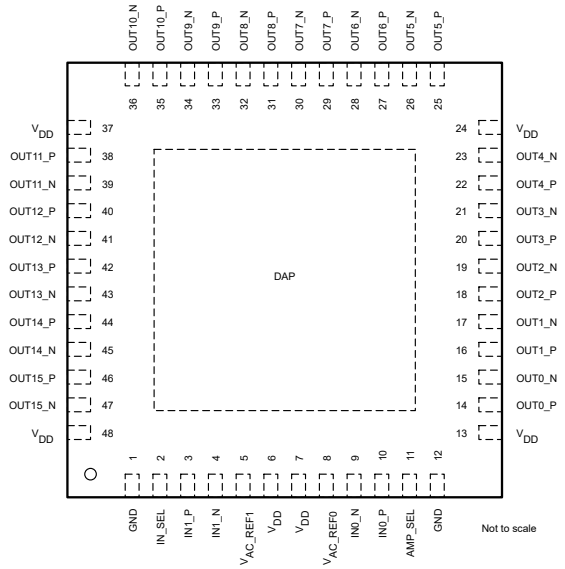


図 6-2. LMK1D1216: RGZ Package 48-Pin VQFN Top View

表 6-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	LMK1D1212	LMK1D1216		
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT				
IN0_P	9	10	I	Primary: Differential input pair or single-ended input
IN0_N	8	9		
IN1_P	2	3	I	Secondary: Differential input pair or single-ended input. Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N.
IN1_N	3	4		
INPUT SELECT				
IN_SEL	1	2	I	Input Selection with an internal 500-kΩ pullup and 320-kΩ pulldown resistor; selects input port. See 表 9-2.
AMPLITUDE SELECT				
AMP_SEL	10	11	I	Output amplitude swing select with an internal 500-kΩ pullup and 320-kΩ pulldown. See 表 9-3.
BIAS VOLTAGE OUTPUT				
V_{AC_REF0}	7	8	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF capacitor to GND on this pin.
V_{AC_REF1}	4	5		
DIFFERENTIAL CLOCK OUTPUT				
OUT0_P	12	14	O	Differential LVDS output pair number 0
OUT0_N	13	15		
OUT1_P	14	16	O	Differential LVDS output pair number 1
OUT1_N	15	17		
OUT2_P	16	18	O	Differential LVDS output pair number 2
OUT2_N	17	19		

表 6-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	LMK1D1212	LMK1D1216		
OUT3_P	18	20	O	Differential LVDS output pair number 3
OUT3_N	19	21		
OUT4_P	22	22	O	Differential LVDS output pair number 4
OUT4_N	23	23		
OUT5_P	24	25	O	Differential LVDS output pair number 5
OUT5_N	25	26		
OUT6_P	26	27	O	Differential LVDS output pair number 6
OUT6_N	27	28		
OUT7_P	28	29	O	Differential LVDS output pair number 7
OUT7_N	29	30		
OUT8_P	32	31	O	Differential LVDS output pair number 8
OUT8_N	33	32		
OUT9_P	34	33	O	Differential LVDS output pair number 9
OUT9_N	35	34		
OUT10_P	36	35	O	Differential LVDS output pair number 10
OUT10_N	37	36		
OUT11_P	38	38	O	Differential LVDS output pair number 11
OUT11_N	39	39		
OUT12_P	—	40	O	Differential LVDS output pair number 12
OUT12_N	—	41		
OUT13_P	—	42	O	Differential LVDS output pair number 13
OUT13_N	—	43		
OUT14_P	—	44	O	Differential LVDS output pair number 14
OUT14_N	—	45		
OUT15_P	—	46	O	Differential LVDS output pair number 15
OUT15_N	—	47		
SUPPLY VOLTAGE				
V_{DD}	5, 6, 11, 20, 31, 40	6, 7, 13, 24, 37, 48	P	Device power supply (1.8 V, 2.5 V, or 3.3 V)
GROUND				
GND	21, 30	1, 12	G	Ground
MISC				
DAP	DAP	DAP	G	Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	3.6	V
V_O	Output voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_J	Junction temperature		135	°C
T_{stg}	Storage temperature (2)	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device unpowered

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90 % of VDD)	0.1		20	ms
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		135	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMK1D1212 RHA (VQFN) 40 PINS	LMK1D1216 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	21.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	12.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13	12.8	°C/W

THERMAL METRIC(1)		LMK1D1212 RHA (VQFN) 40 PINS	LMK1D1216 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_{STAT}	Core supply current, static (LMK1D1212)	All outputs enabled and unterminated, f = 0 Hz		65		mA
IDD_{STAT}	Core supply current, static (LMK1D1216)	All outputs enabled and unterminated, f = 0 Hz		70		mA
IDD_{100M}	Core supply current (LMK1D1212)	All outputs enabled, R_L = 100 Ω, f =100 MHz		105	130	mA
IDD_{100M}	Core supply current (LMK1D1216)	All outputs enabled, R_L = 100 Ω, f =100 MHz		120	150	mA
IN_SEL/AMP_SEL CONTROL INPUT CHARACTERISTICS (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
Vd_{I3}	Tri-state input	Open		0.4 × V_{CC}		V
V_{IH}	Input high voltage	Minimum input voltage for a logical "1" state in table 1	0.7 × V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Maximum input voltage for a logical "0" state in table 1	–0.3		0.3 × V_{CC}	V
I_{IH}	Input high current	V_{DD} can be 1.8V, 2.5V, or 3.3V with V_{IH} = V_{DD}			30	µA
I_{IL}	Input low current	V_{DD} can be 1.8V, 2.5V, or 3.3V with V_{IH} = V_{DD}	–30			µA
$R_{pull-up}$	Input pullup resistor			500		kΩ
$R_{pull-down}$	Input pulldown resistor			320		kΩ
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input	DC		250	MHz
V_{IN_S-E}	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4		3.465	V
dVIN/dt	Input Slew Rate (20% to 80% of the amplitude)		0.05			V/ns
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{IH} = 3.465 V			60	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{IL} = 0 V	–30			µA
C_{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input			2	GHz
$V_{IN,DIFF(p-p)}$	Differential input voltage peak-to-peak {2 × (V_{INP} – V_{INN})}	V_{ICM} = 1 V (V_{DD} = 1.8 V)	0.3		2.4	V_{PP}
		V_{ICM} = 1.25 V (V_{DD} = 2.5 V/3.3 V)	0.3		2.4	
V_{ICM}	Input common-mode voltage	$V_{IN,DIFF(P-P)}$ > 0.4 V (V_{DD} = 1.8 V/2.5 V/3.3 V)	0.25		2.3	V
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{INP} = 2.4 V, V_{INN} = 1.2 V			30	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{INP} = 0 V, V_{INN} = 1.2 V	–30			µA
C_{IN_SE}	Input capacitance (Single-ended)	at 25°C		3.5		pF

VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS DC OUTPUT CHARACTERISTICS						
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	250	350	450	mV
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	400	500	650	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
$V_{OC(SS)}$	Steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V)	1		1.2	V
		$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V)	1.1		1.375	
$V_{OC(SS)}$	Steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V), AMP_SEL = 1	0.8		1.05	V
		$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V), AMP_SEL = 1	0.9		1.15	
$\Delta_{VOC(SS)}$	Change in steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
$\Delta_{VOC(SS)}$	Change in steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
LVDS AC OUTPUT CHARACTERISTICS						
V_{ring}	Output overshoot and undershoot	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, f_{OUT} = 491.52 MHz	–0.1		0.1	V_{OD}
V_{OS}	Output AC common-mode voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω		50	100	mV_{pp}
V_{OS}	Output AC common-mode voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1		75	150	mV_{pp}
I_{OS}	Short-circuit output current (differential)	V_{OUTP} = V_{OUTN}	–12		12	mA
$I_{OS(cm)}$	Short-circuit output current (common-mode)	V_{OUTP} = V_{OUTN} = 0	–24		24	mA
t_{PD}	Propagation delay	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (1)	0.3		0.575	ns
$t_{SK, O}$	Output skew	Skew between outputs with the same load conditions (12 and 16 channels) ((2))			20	ps
$t_{SK, PP}$	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			200	ps
$t_{SK, P}$	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (3)	–20		20	ps
$t_{RJIT(ADD)}$	Random additive Jitter (rms)	f_{IN} = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12 kHz to 20 MHz, with output load R_{LOAD} = 100 Ω		45	60	fs, RMS

VDD = 1.8 V ± 5 %, –40°C ≤T_A ≤ 105°C. Typical values are at VDD = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise	Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R_{LOAD} = 100 Ω	PN_{1kHz}		–143		dBc/Hz
		PN_{10kHz}		–150		
		PN_{100kHz}		–157		
		PN_{1MHz}		–160		
		PN_{floor}		–164		
MUX_{ISO}	Mux Isolation	f_{IN} = 156.25 MHz. The difference in power level at f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_R/t_F	Output rise and fall time	20% to 80% with R_{LOAD} = 100 Ω			300	ps
t_R/t_F	Output rise and fall time	20% to 80% with RLOAD = 100 Ω (AMP_SEL= 1)			300	ps
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{LOAD} = 100 µA	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) V_{DD} = 2.5 V/ 3.3 V						
PSNR	Power Supply Noise Rejection ($f_{carrier}$ = 156.25 MHz)	10 kHz, 100 mVpp ripple injected on V_{DD}		–70		dBc
		1 MHz, 100 mVpp ripple injected on V_{DD}		–50		

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
(3) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

7.6 Typical Characteristics

図 7-1 and 図 7-2 capture the variation of the LMK1D1216 current consumption with input frequency, supply voltage, and AMP_SEL. The LMK1D1212 follows a similar trend. 図 7-3 and 図 7-4 show the variation of the differential output voltage (VOD) swept across frequency for AMP_SEL = 0 and AMP_SEL = 1. This result is applicable to LMK1D1212 as well.

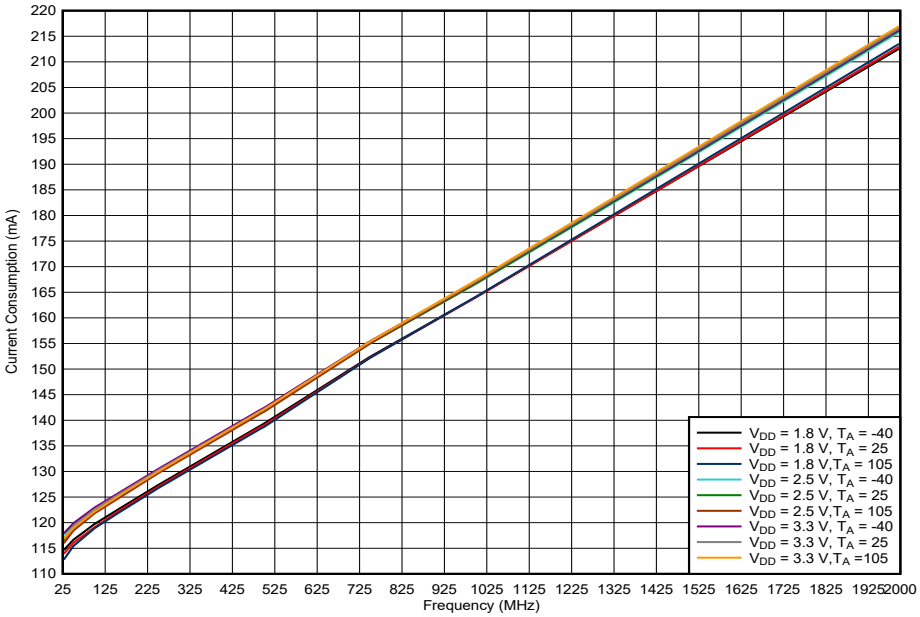


図 7-1. LMK1D1216 Current Consumption vs. Frequency, AMP_SEL = 0

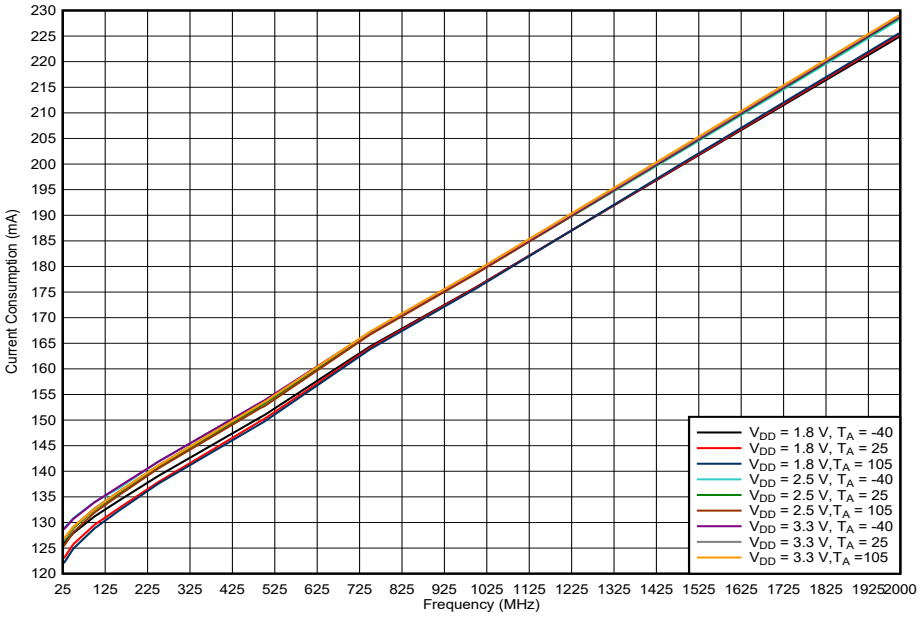


図 7-2. LMK1D1216 Current Consumption vs. Frequency, AMP_SEL = 1

7.6 Typical Characteristics

図 7-1 and 図 7-2 capture the variation of the LMK1D1216 current consumption with input frequency, supply voltage, and AMP_SEL. The LMK1D1212 follows a similar trend. 図 7-3 and 図 7-4 show the variation of the differential output voltage (VOD) swept across frequency for AMP_SEL = 0 and AMP_SEL = 1. This result is applicable to LMK1D1212 as well.

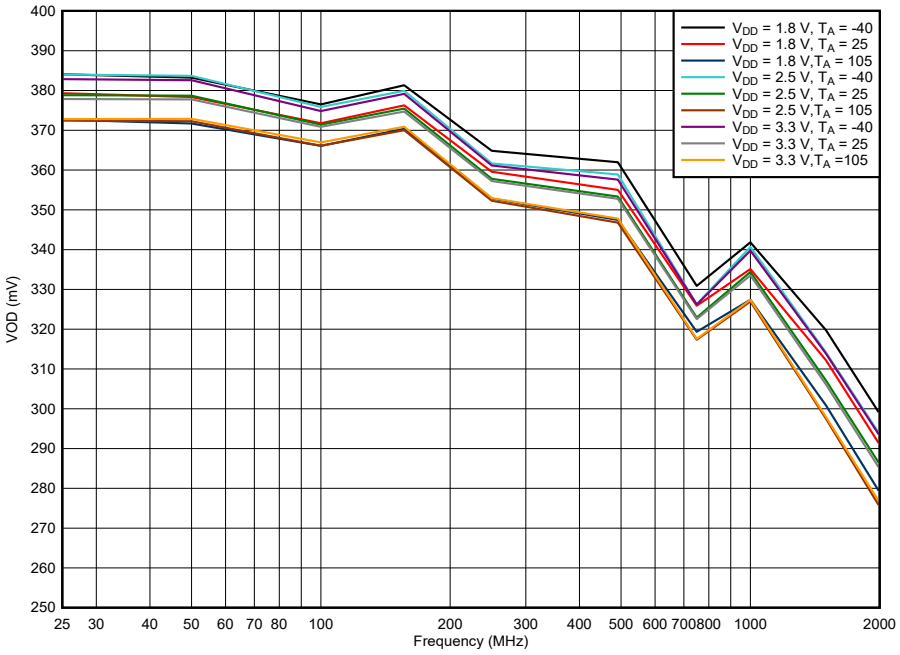


図 7-3. LMK1D1216 VOD vs. Frequency, AMP_SEL = 0

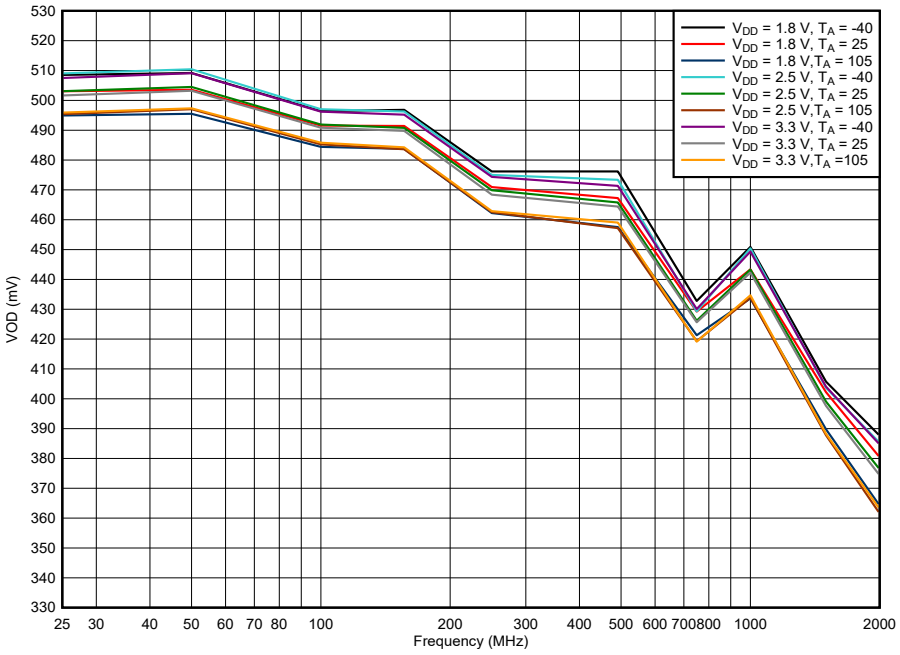


図 7-4. LMK1D1216 VOD vs. Frequency, AMP_SEL = 1

8 Parameter Measurement Information

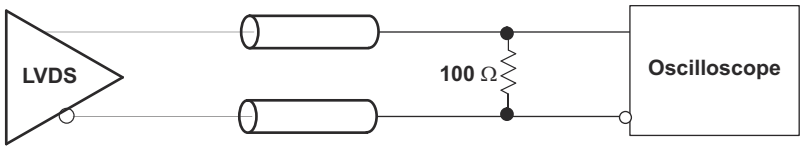


図 8-1. LVDS Output DC Configuration During Device Test

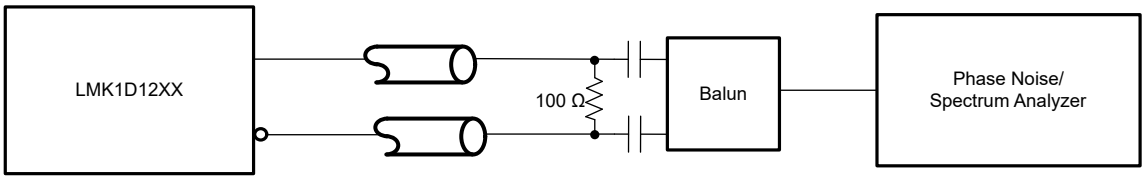


図 8-2. LVDS Output AC Configuration During Device Test

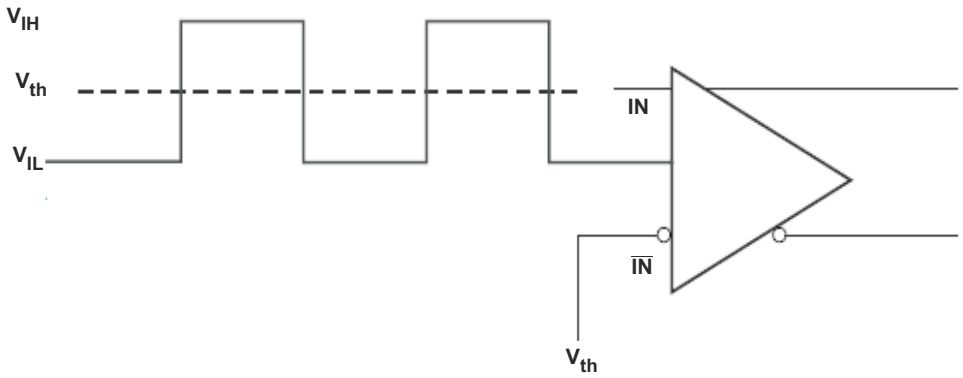


図 8-3. DC-Coupled LVCMOS Input During Device Test

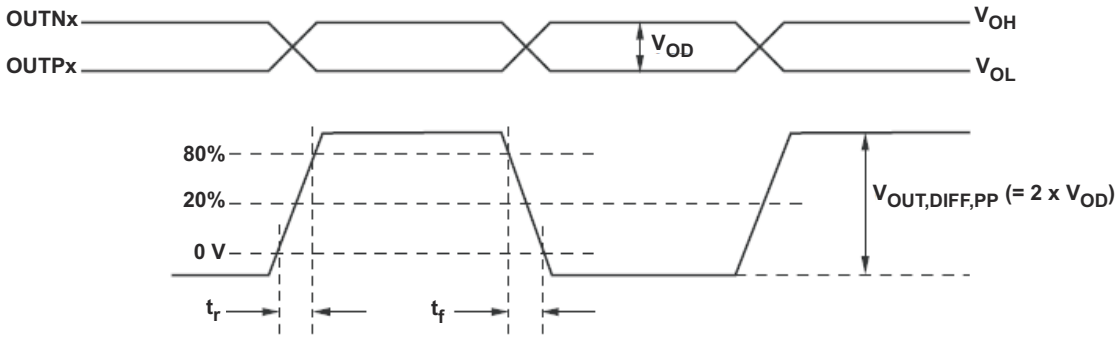
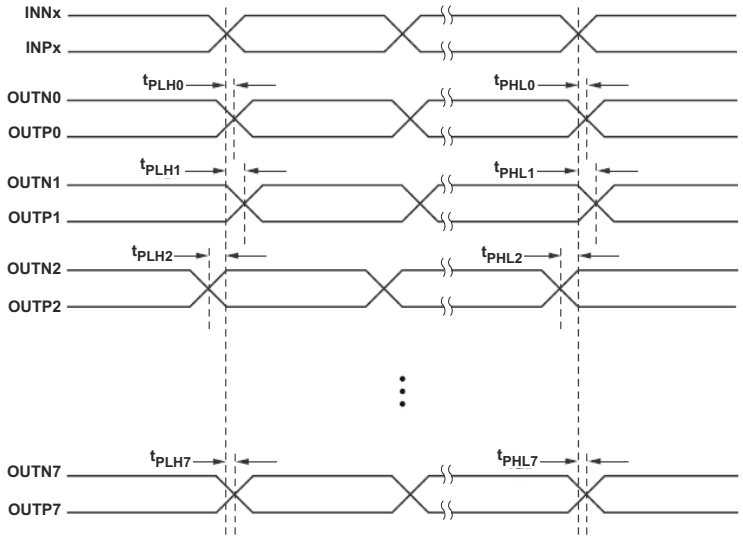


図 8-4. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..7)

B. Part-to-part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..7)

図 8-5. Output Skew and Part-to-Part Skew

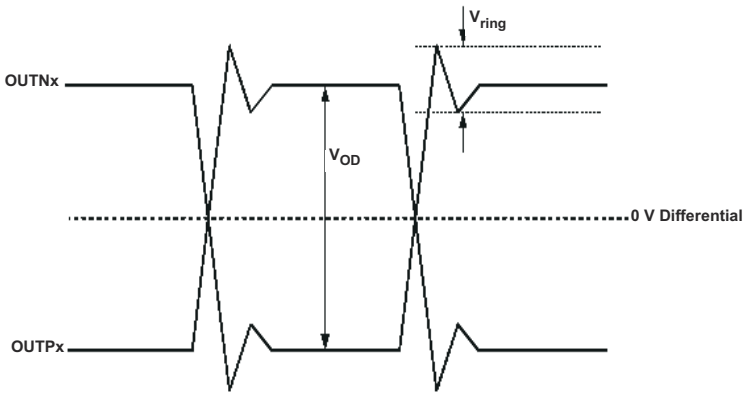


図 8-6. Output Overshoot and Undershoot

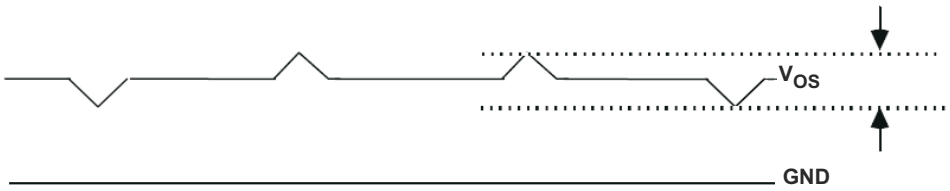


図 8-7. Output AC Common Mode

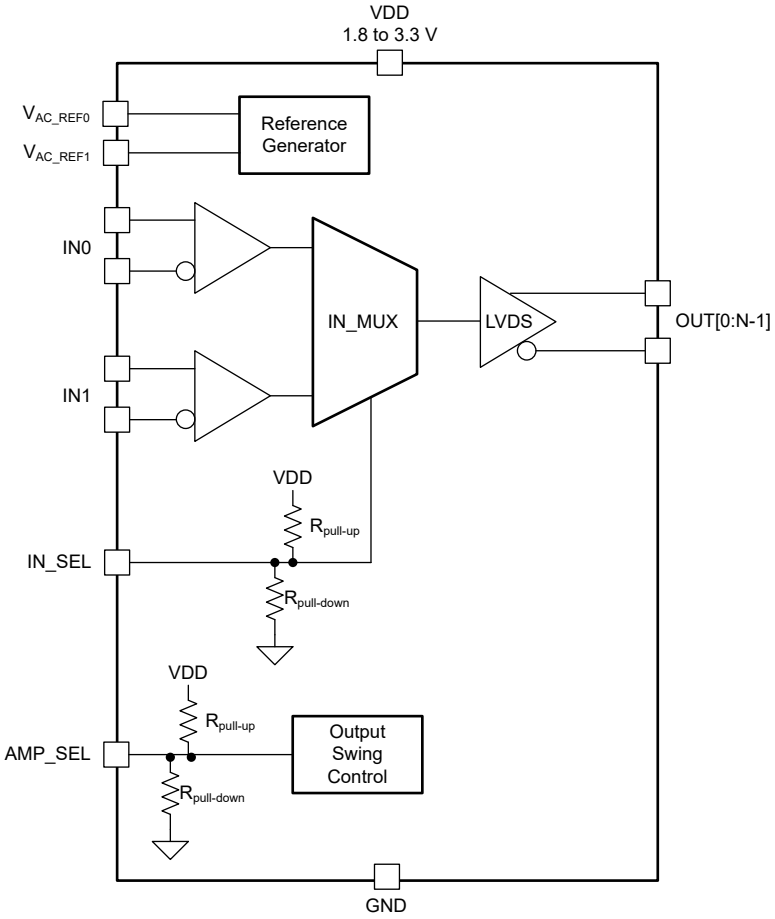
9 Detailed Description

9.1 Overview

The LMK1D121x LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D121x, AC coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

9.2 Functional Block Diagram



9.3 Feature Description

The LMK1D121x is a low additive jitter LVDS fan-out buffer that can generate up to 12 (LMK1D1212) or 16 (LMK1D1216) copies of two selectable LVPECL, LVDS, LP-HCSL, HCSL, or LVCMOS inputs. The LMK1D121x can accept reference clock frequencies up to 2 GHz while providing low output skew.

表 9-1 lists the LMK1D1212 and LMK1D1216outputs divided into two banks.

表 9-1. Output Bank

Bank	LMK1D1212	LMK1D1216
0	OUT0 to OUT5	OUT0 to OUT7
1	OUT6 to OUT11	OUT8 to OUT15

Apart from providing a very low additive jitter and low output skew, the LMK1D121x has an input select pin (IN_SEL) and an output amplitude control pin (AMP_SEL).

9.3.1 Fail-Safe Input and Hysteresis

The LMK1D121x family of devices is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to *セクション 7* for more information on the maximum input supported by the device. User should note that incorporating the fail-safe inputs also results in a slight increase in clock input pin capacitance.

The device also incorporates an input hysteresis which prevents random oscillation in absence of an input signal. Furthermore, this feature allows the input pins to be left open.

9.3.2 Input Mux

The LMK1D121x family of devices has a 2:1 input mux. This feature allows the user to select between the two clock inputs using the IN_SEL pin and fan out the input to the outputs. More information on the input selection is provided in the next section.

9.4 Device Functional Modes

The two inputs of the LMK1D121x are internally muxed together and can be selected through the control pin (see 表 9-2). Unused inputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D121x to provide greater system flexibility.

表 9-2. Input Selection

IN_SEL	ACTIVE CLOCK INPUT
0	IN0_P, IN0_N
1	IN1_P, IN1_N
Open	None(1)

(1) The input buffers are disabled and the outputs are static.

The output amplitude of the banks of the LMK1D121x can be selected through the amplitude selection pin (see 表 9-3). The higher output amplitude mode (boosted swing LVDS mode) can be used in applications which require higher amplitude either for better noise performance (higher slew rate) or if the receiver has swing requirements which the standard LVDS swing cannot meet.

表 9-3. Amplitude Selection

AMP_SEL	OUTPUT AMPLITUDE (mV)
0	Bank 0: boosted LVDS swing (500 mV) Bank 1: standard LVDS swing (350 mV)
OPEN	Bank 0: standard LVDS swing (350 mV) Bank 1: standard LVDS swing (350 mV)
1	Bank 0: boosted LVDS swing (500 mV) Bank 1: boosted LVDS swing (500 mV)

9.4.1 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D121x can be connected to LVDS receiver inputs with DC and AC coupling as shown in 図 9-1 and 図 9-2, respectively.

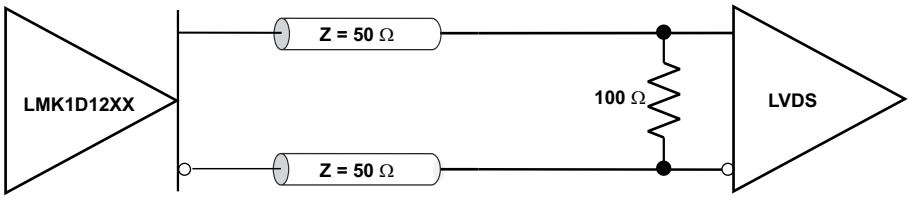


図 9-1. Output DC Termination

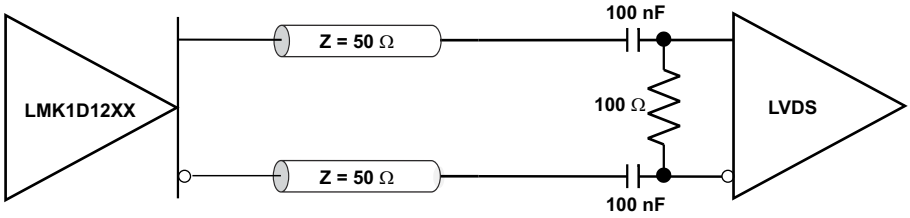


図 9-2. Output AC Termination (With the Receiver Internally Biased)

9.4.2 Input Termination

The LMK1D121x inputs can be interfaced with LVDS, LVPECL, LP-HCSL, HCSL, CML, or LVCMOS drivers.

LVDS drivers can be connected to LMK1D121x inputs with DC and AC coupling as shown 図 9-3 and 図 9-4, respectively.

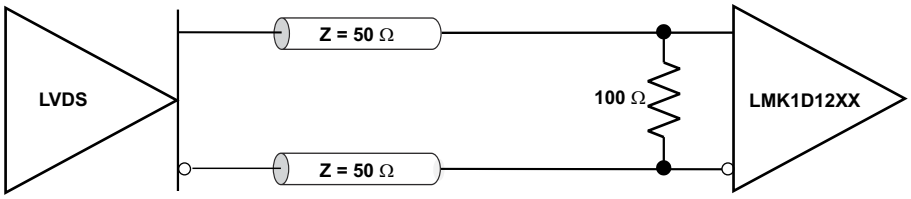


図 9-3. LVDS Clock Driver Connected to LMK1D121x Input (DC-Coupled)

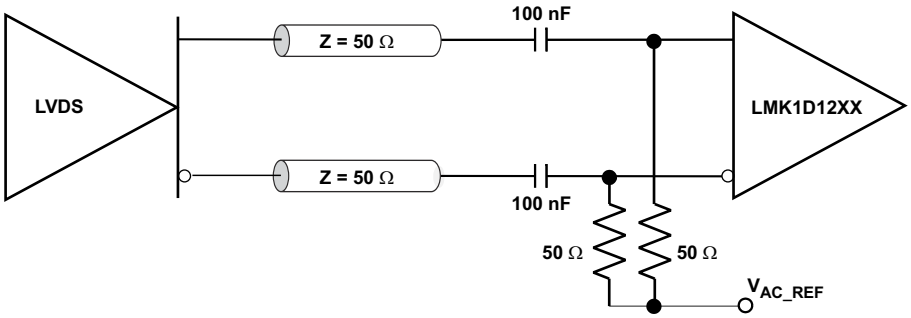


図 9-4. LVDS Clock Driver Connected to LMK1D121x Input (AC-Coupled)

図 9-5 shows how to connect LVPECL inputs to the LMK1D121x. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

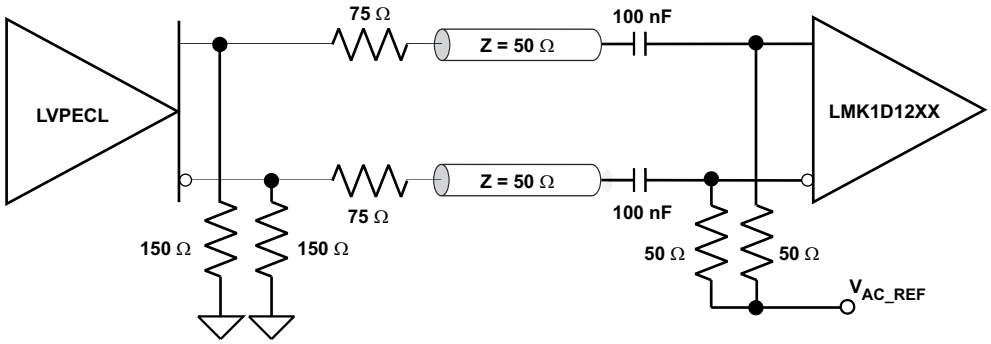


図 9-5. LVPECL Clock Driver Connected to LMK1D121x Input

図 9-6 shows how to couple a LVCMOS clock input to the LMK1D121x directly.

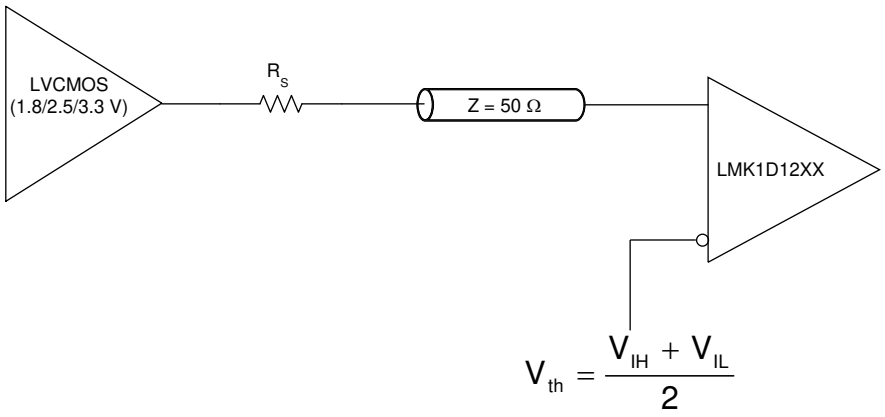


図 9-6. 1.8-V, 2.5-V, or 3.3-V LVCMOS Clock Driver Connected to LMK1D121x Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK1D121x is a low additive jitter universal to LVDS fan-out buffer with 2 selectable inputs. The small package size, low output skew, and low additive jitter make for a flexible device in demanding applications.

10.2 Typical Application

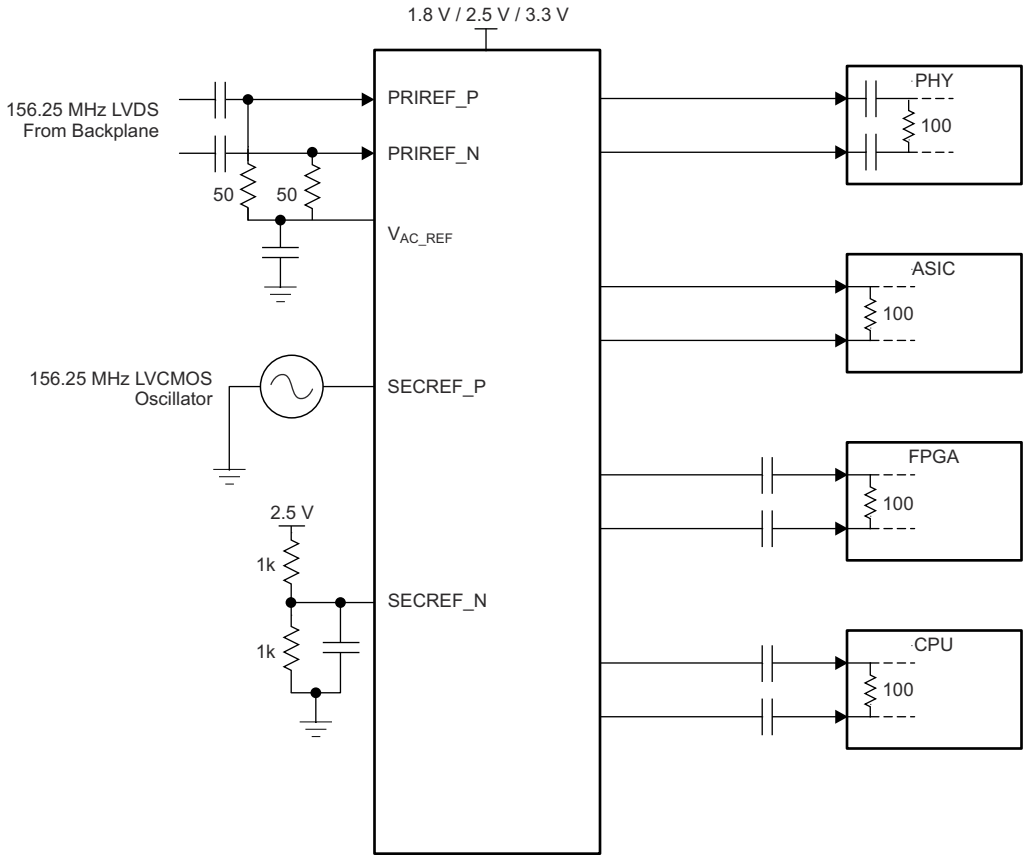


図 10-1. Fan-Out Buffer for Line Card Application

10.2.1 Design Requirements

The LMK1D121x shown in 図 10-1 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC coupling with an LVDS driver such as the LMK1D121x. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D121x. Again, no additional components are required.
- The FPGA requires external AC coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- Unused outputs of the LMK1D121x device are terminated differentially with a 100-Ω resistor for optimum performance.

10.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

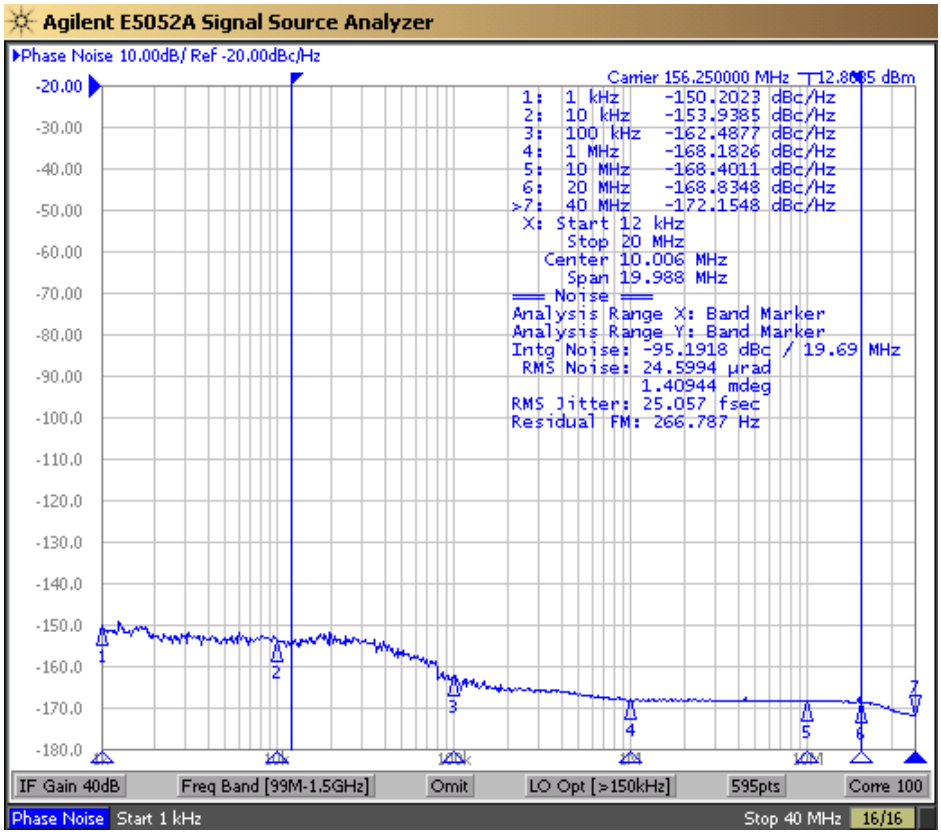
TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In this example, the PHY, ASIC, FPGA, and CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043).

10.2.3 Application Curves

This section shows the low additive noise for the LMK1D1216. The low noise 156.25-MHz source with 25-fs RMS jitter, shown in 図 10-2, drives the LMK1D1216, resulting in 46.9-fs RMS when integrated from 12 kHz to 20 MHz (図 10-3). The resultant additive jitter is a low 39.7-fs RMS for this configuration. Note that this result applies to the LMK1D1212 device as well.



Note: Reference signal is a low-noise Rhode and Schwarz SMA100B

図 10-2. LMK1D1216 Reference Phase Noise, 156.25 MHz, 25-fs RMS (12 kHz to 20 MHz)

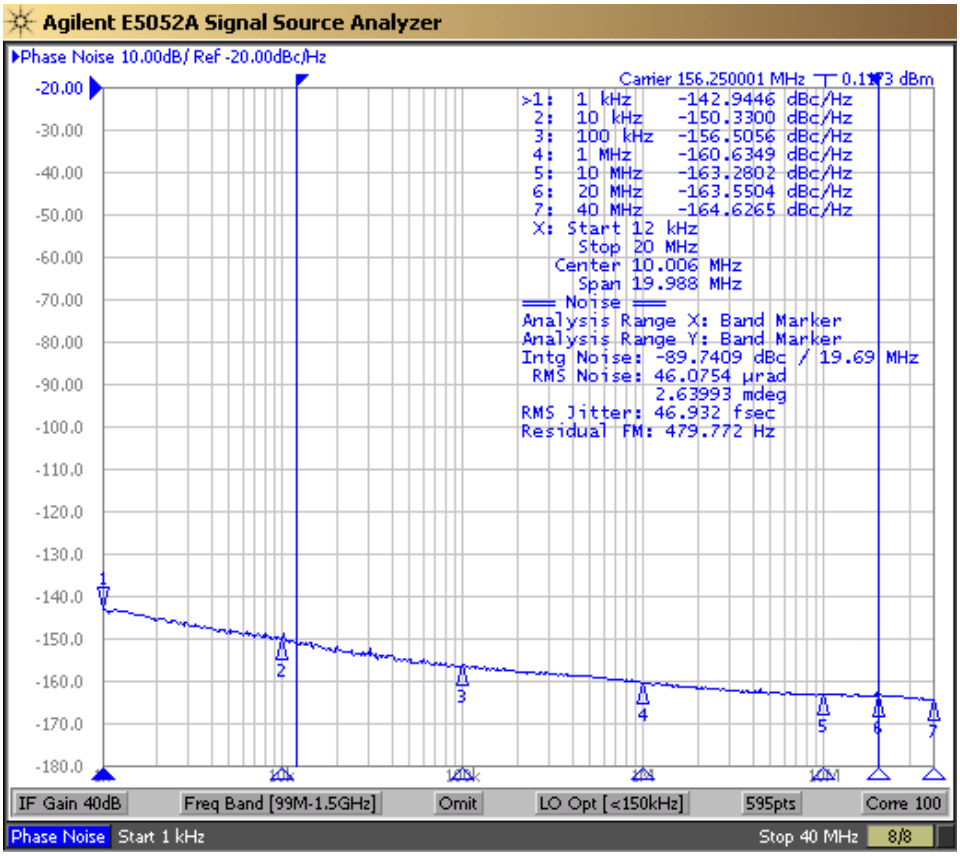


図 10-3. LMK1D1216 Output Phase Noise, 156.25 MHz, 46.9-fs RMS (12 kHz to 20 MHz)

10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These ferrite beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

図 10-4 shows this recommended power-supply decoupling method.

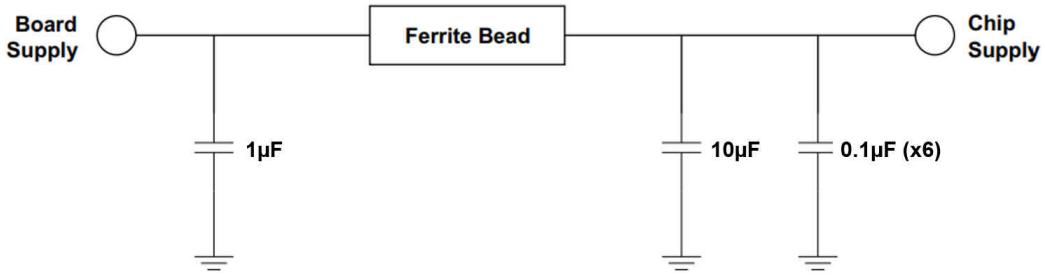


図 10-4. Power Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. 図 10-5 and 図 10-6show the recommended top layer and via patterns for the 40-pin package (LMK1D1212).

10.4.2 Layout Examples

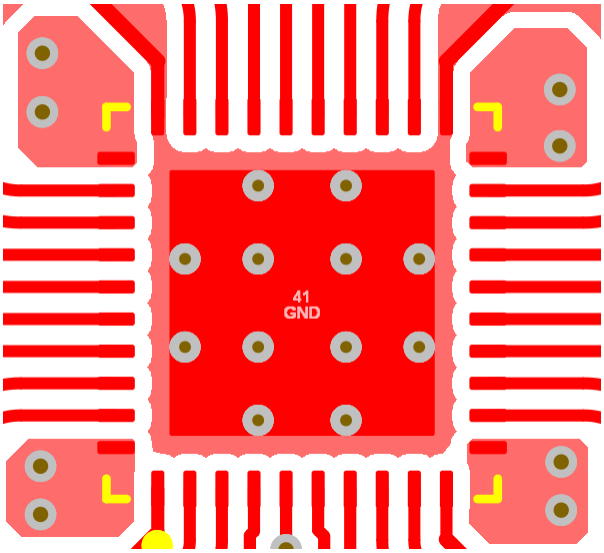


図 10-5. PCB layout example for LMK1D1212, Top Layer

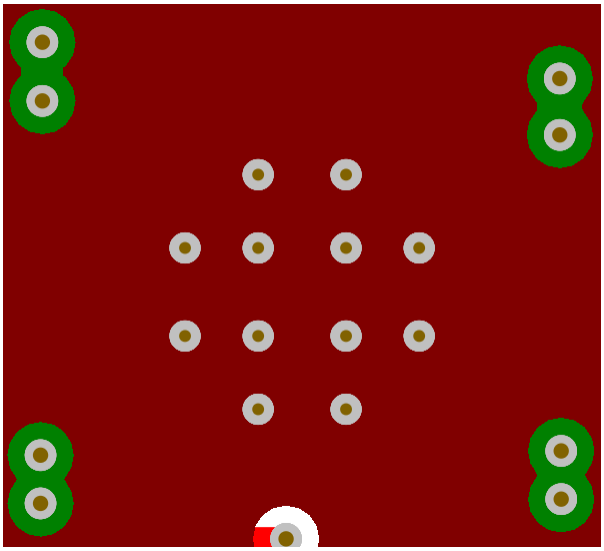


図 10-6. PCB Layout Example for LMK1D1212, GND Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* user's guide
- Texas Instruments, *Power Consumption of LVPECL and LVDS* Analog design journal
- Texas Instruments, *Using Thermal Calculation Tools for Analog Components* application report

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1D1212RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1212
LMK1D1212RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1212
LMK1D1212RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1212
LMK1D1212RHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1212
LMK1D1216RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216
LMK1D1216RGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216
LMK1D1216RGZRG4	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216
LMK1D1216RGZRG4.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216
LMK1D1216RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216
LMK1D1216RGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1216

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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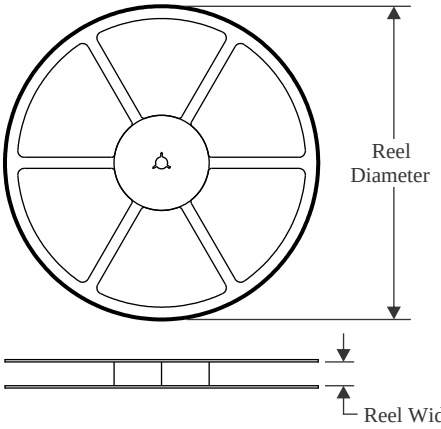
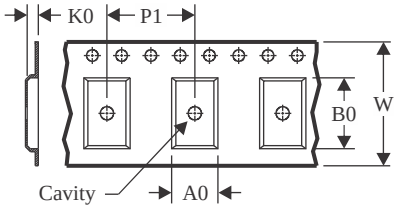
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

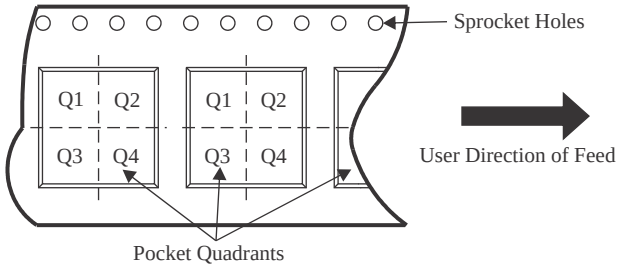


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

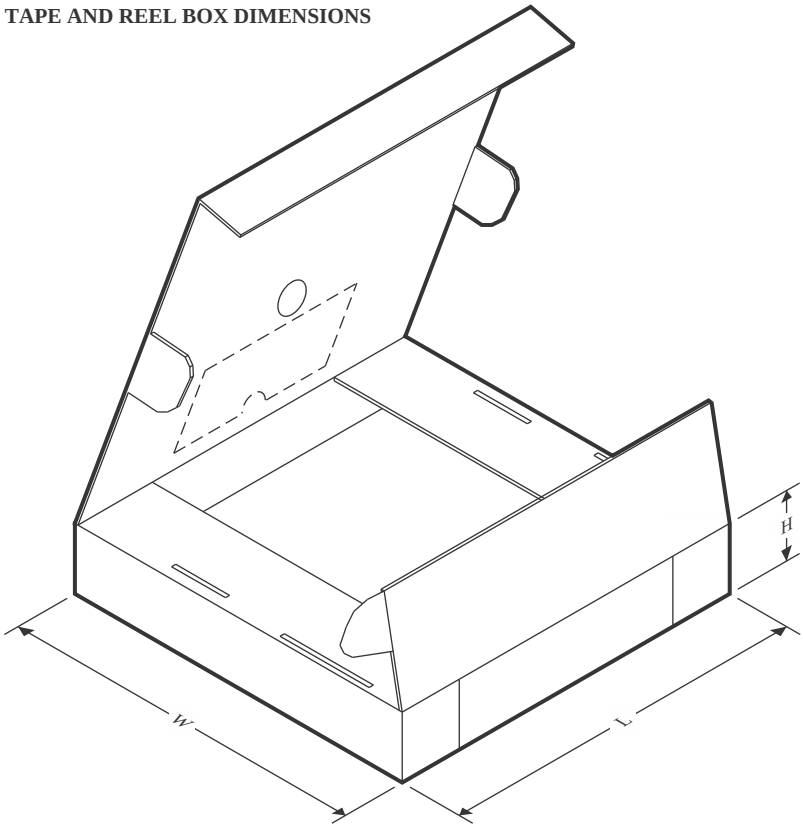
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1212RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMK1D1212RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMK1D1216RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
LMK1D1216RGZRG4	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
LMK1D1216RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1212RHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
LMK1D1212RHAT	VQFN	RHA	40	250	210.0	185.0	35.0
LMK1D1216RGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
LMK1D1216RGZRG4	VQFN	RGZ	48	2500	367.0	367.0	35.0
LMK1D1216RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

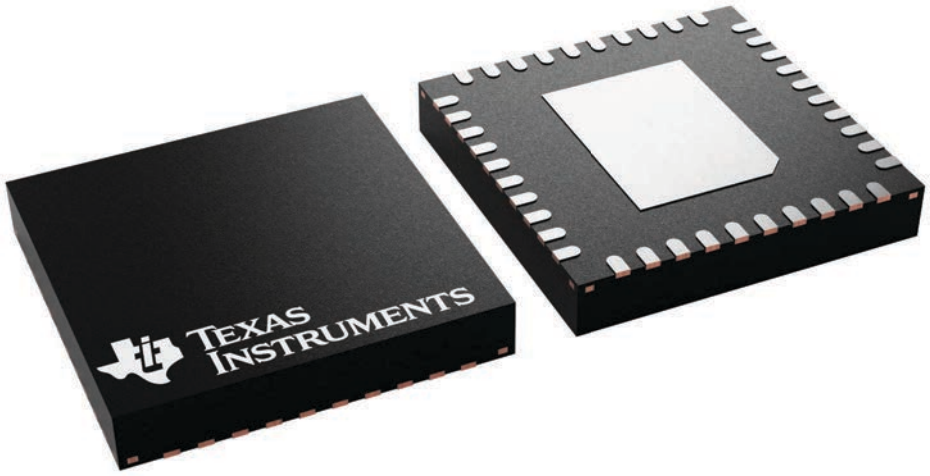
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



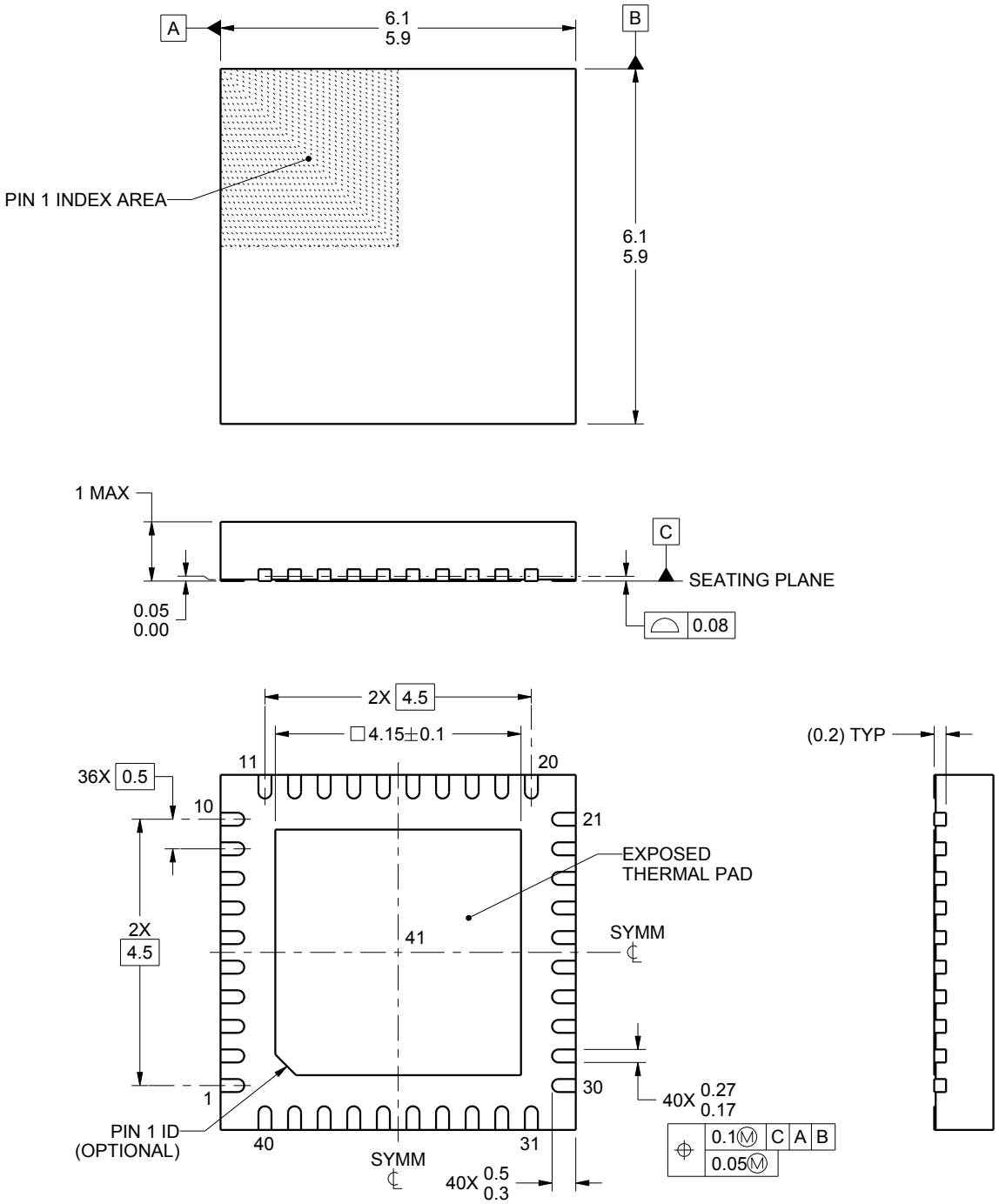
4225870/A

PACKAGE OUTLINE

RHA0040B

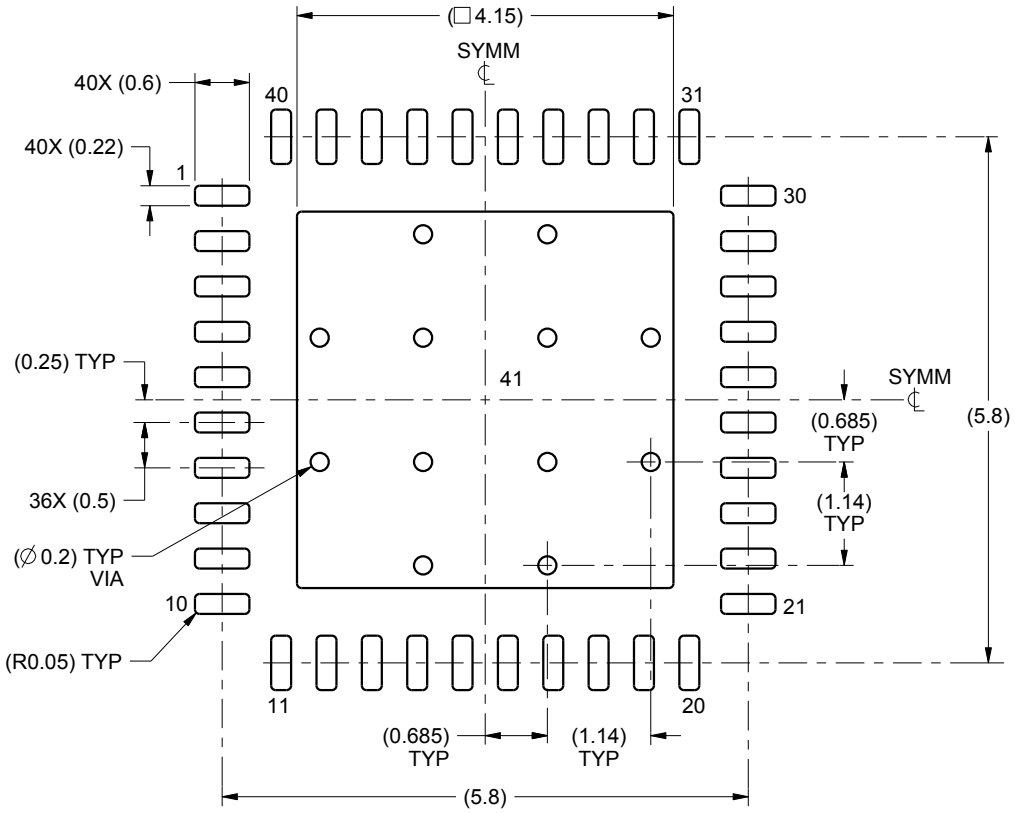
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

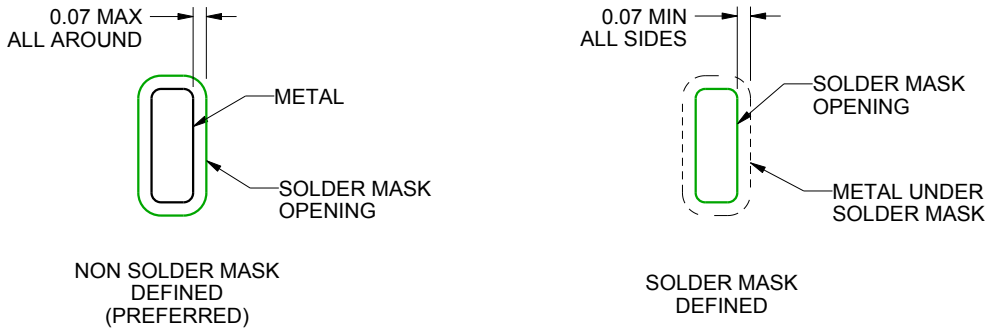


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

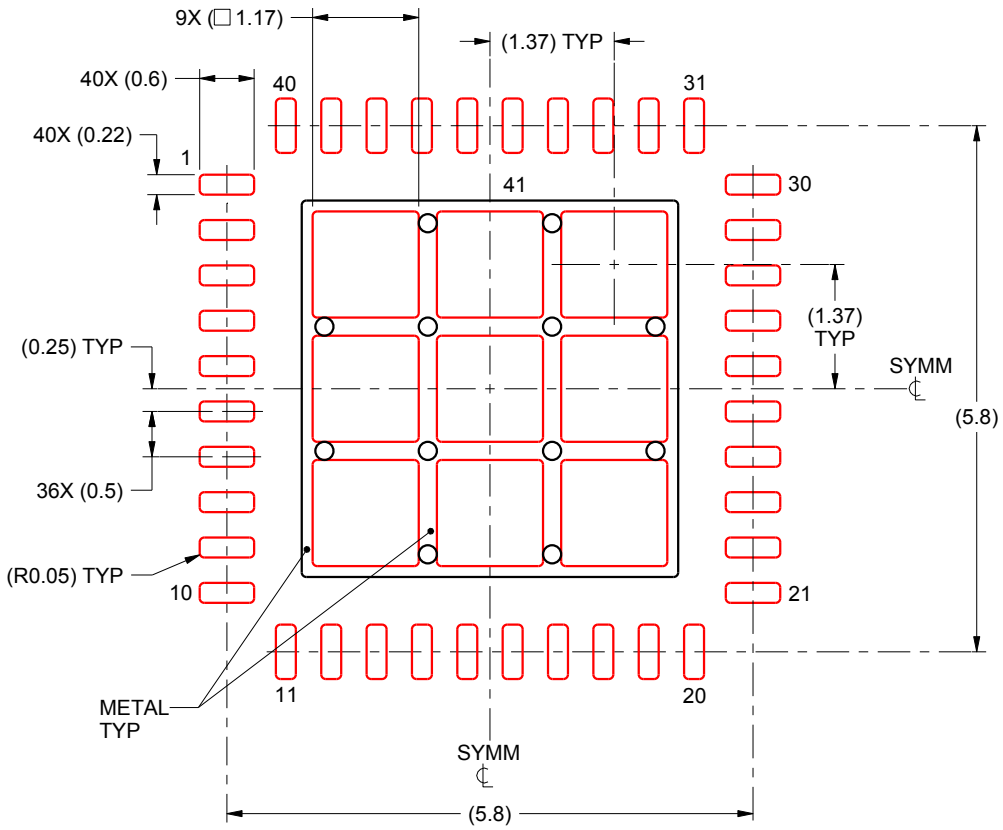


SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

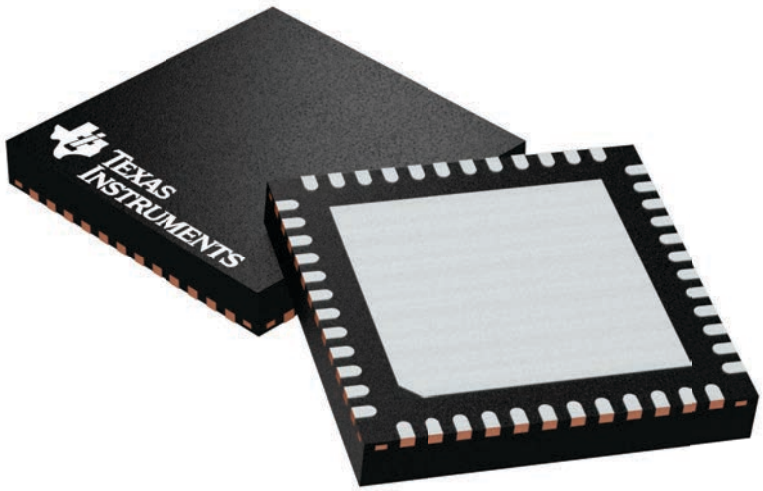
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

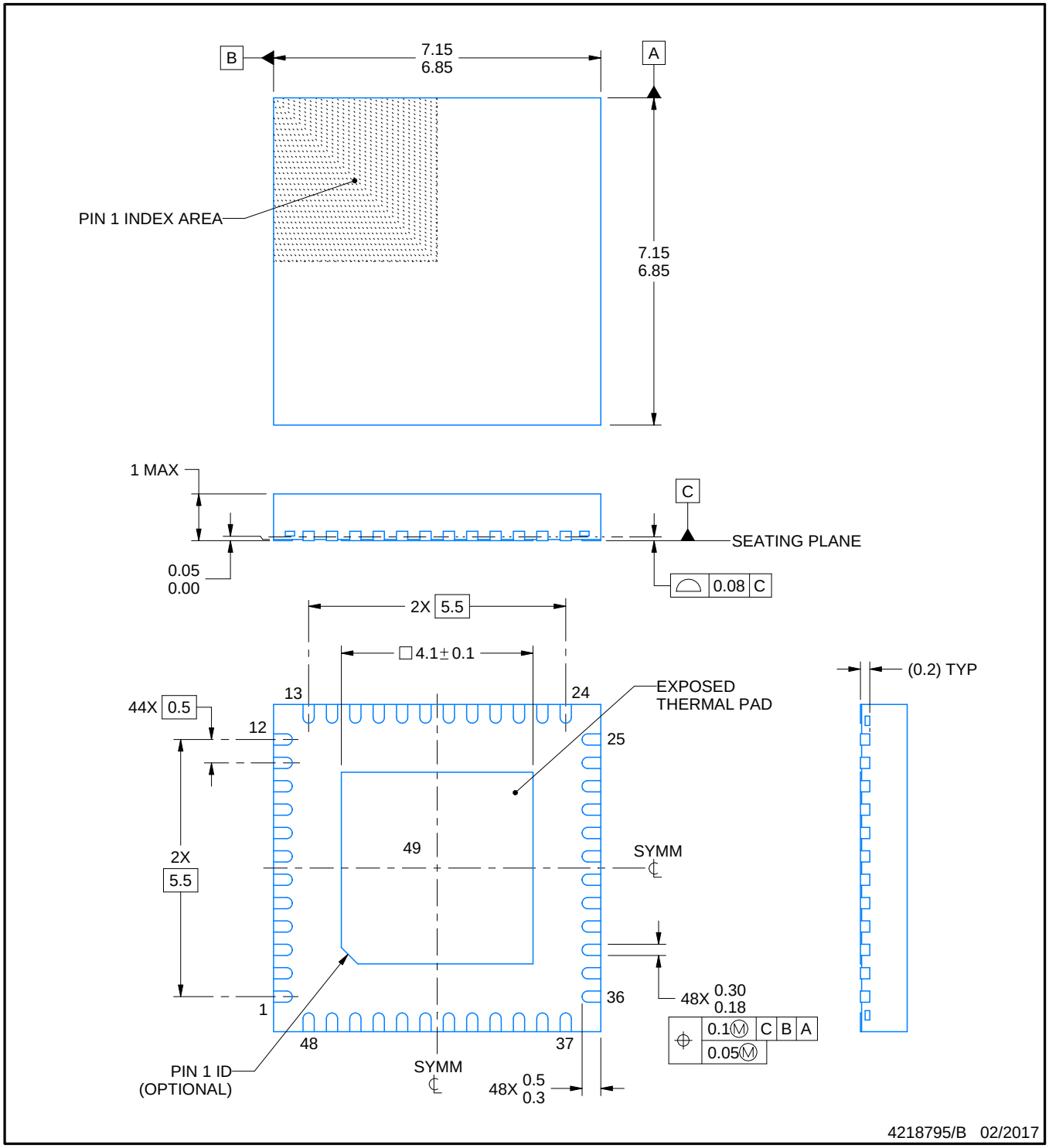
4224671/A

RGZ0048B

PACKAGE OUTLINE

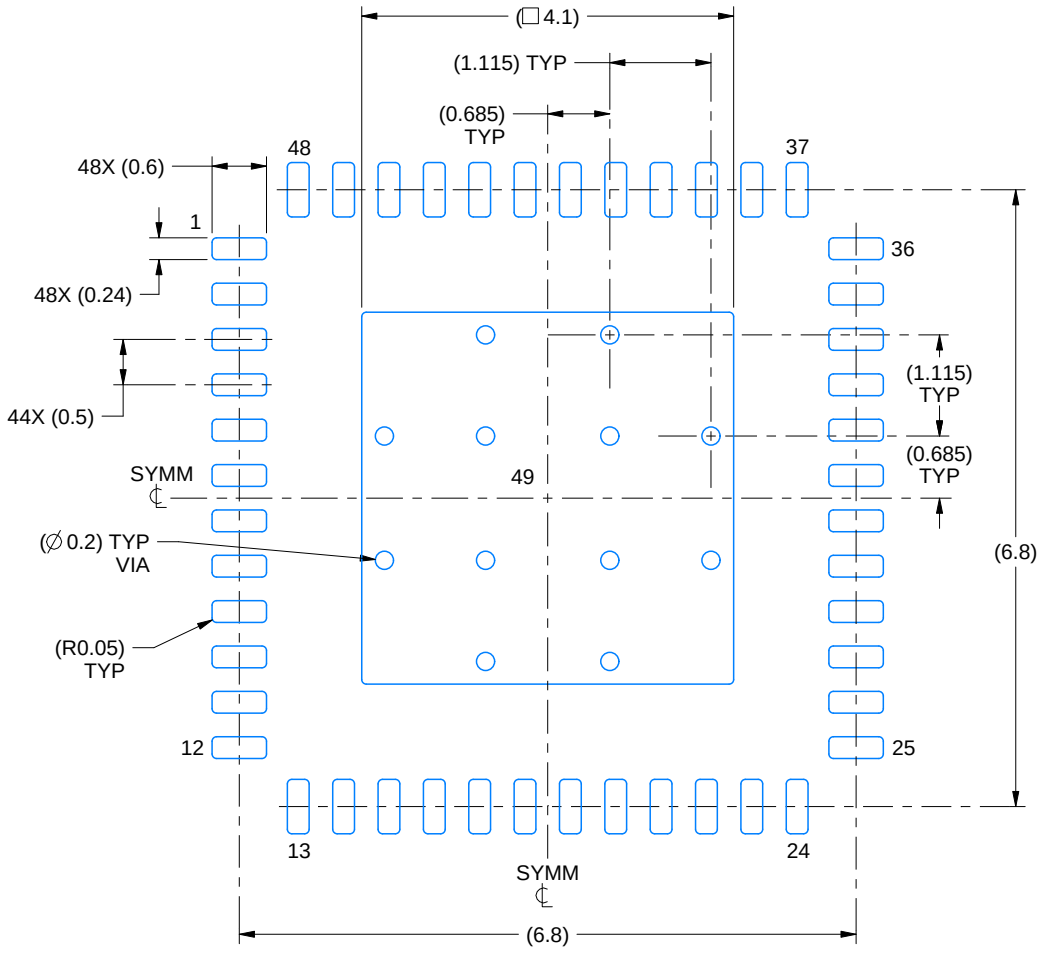
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

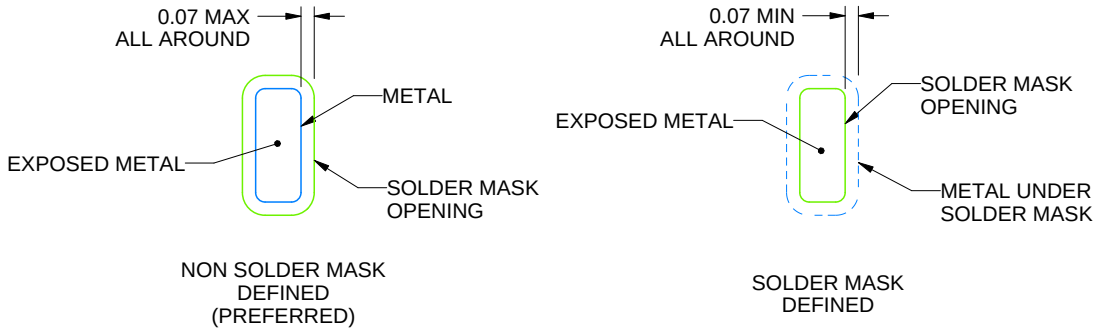


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

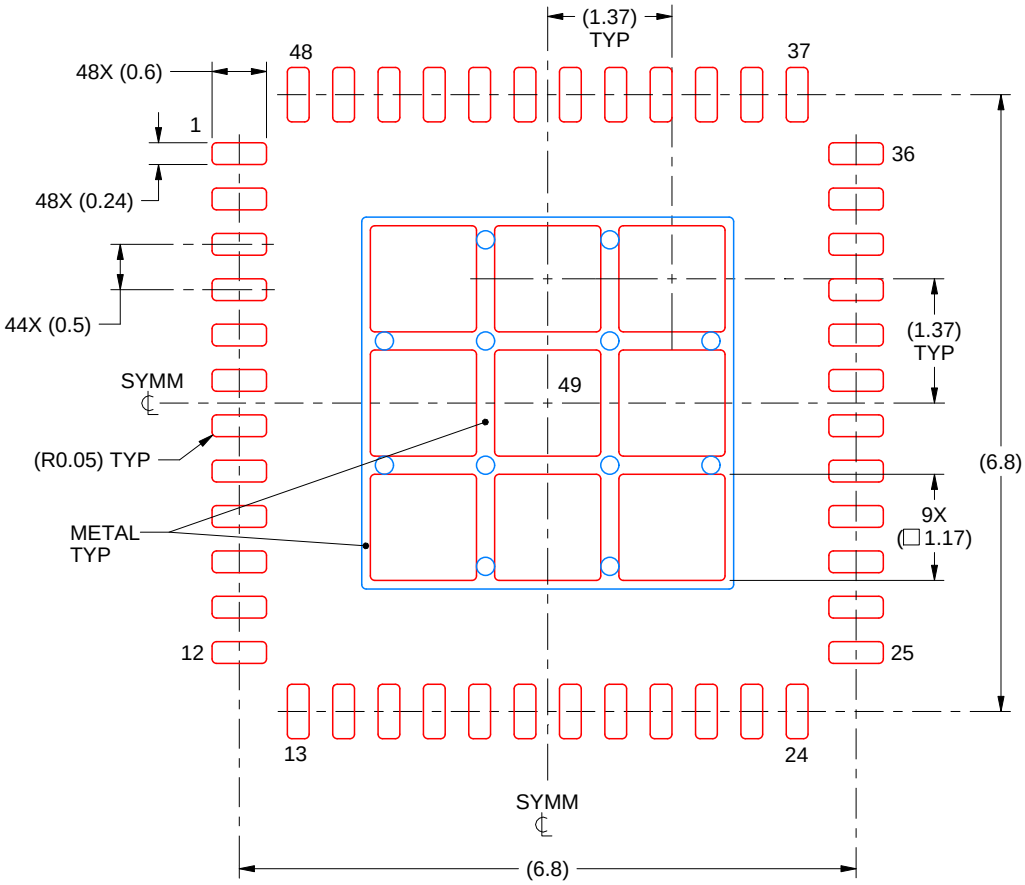


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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