LMK1D1208P ピン制御 OE、低付加ジッタ LVDS バッファ

1 特長

- 2 入力、8 出力 (2:8) 高性能 LVDS クロック・バッファ・ファミリ
- 出力周波数:最大 2GHz
- 個別の出力イネーブル / ディセーブル用ハードウェア・ピン
- 電源電圧:1.8V / 2.5V / 3.3V ±5%
- 小さい付加ジッタ:156.25MHz 時、12kHz～20MHz の範囲で最大 60fs rms
  - 非常に小さい位相ノイズ・フロア:-164dBc/Hz (標準値)
- 非常に小さい伝搬遅延:575ps (最大値)
- 出力スキュー:20ps (最大値)
- フェイルセーフ入力
- ユニバーサル入力は LVDS、LVPECL、LVCMOS、HCSL、CML の信号レベルに対応
- LVDS リファレンス電圧 V_{AC_REF} は、容量性結合入力に使用可能
- 産業用温度範囲:-40℃～105℃
- パッケージ:
  - 6mm × 6mm、40 ピン VQFN (RHA)

2 アプリケーション

- テレコミュニケーションおよびネットワーク機器
- 医療用画像処理
- 試験 / 測定機器
- ワイヤレス・インフラ
- 業務用オーディオ、ビデオ、サイネージ

3 概要

LMK1D1208P クロック・バッファは、2 つのクロック入力 (IN0 および IN1) のいずれか 1 つを 8 ペアの差動 LVDS クロック出力 (OUT0～OUT7) に分配します。このとき、クロック分配のスキューを最小限に抑えます。入力は LVDS、LVPECL、LVCMOS、HCSL、CML のいずれかに対応可能です。

LMK1D1208P は、50Ω 伝送経路の駆動に特化して設計されています。シングルエンド・モードで入力を駆動する場合は、未使用の負入力ピンに適切なバイアス電圧を印加する必要があります (図 9-6 参照)。IN_SEL ピンは、どの入力を出力に転送するかを選択します。このデバイスは、フェイルセーフ入力機能をサポートしています。さらに、このデバイスは入力ヒステリシスを備えており、入力信号が存在しないときに出力がランダムに発振することを防止します。

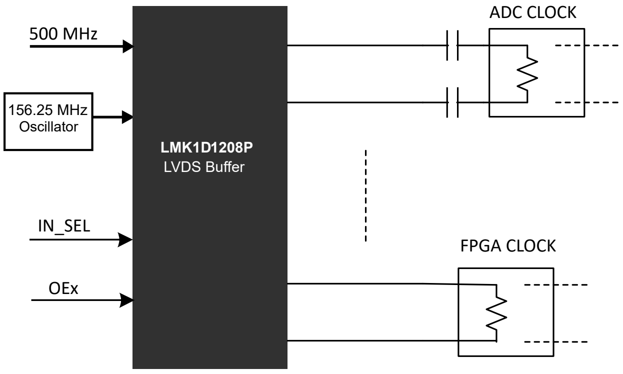
各 LVDS 差動出力は、対応する OEx ピンをロジック HIGH「1」に設定するとイネーブルになります。このピンがロジック LOW「0」に設定されている場合、出力がディセーブルされて HIGH Z 状態になり、消費電力の低減につながります。

このデバイスは、1.8V、2.5V または 3.3V 電源で動作し、-40℃～105℃ (周囲温度) で動作が規定されています。

パッケージ情報

部品番号	パッケージ[1]	パッケージ・サイズ (公称) [2]
LMK1D1208P	VQFN (40)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーションの例

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2021) to Revision A (June 2023) — **Page**

- 表のタイトルを「製品情報」から「パッケージ情報」に変更。.......... 1
- Added the *Device Comparison* table for LMK1Dxxxx buffer family of devices.......... 3
- Moved the *Power Supply Recommendations* and *Layout* section to the *Application and Implementation* section.......... 20

5 Device Comparison

表 5-1. Device Comparison

DEVICE	DEVICE TYPE	FEATURES	OUTPUT SWING	PACKAGE	BODY SIZE
LMK1D2108	Dual 1:8	Global output enable and swing control through pin control	350 mV	VQFN (48)	7.00 mm × 7.00 mm
			500 mV		
LMK1D2106	Dual 1:6	Global output enable and swing control through pin control	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D2104	Dual 1:4	Global output enable and swing control through pin control	350 mV	VQFN (28)	5.00 mm × 5.00 mm
			500 mV		
LMK1D2102	Dual 1:2	Global output enable and swing control through pin control	350 mV	VQFN (16)	3.00 mm × 3.00 mm
			500 mV		
LMK1D1216	2:16	Global output enable control through pin control	350 mV	VQFN (48)	7.00 mm × 7.00 mm
			500 mV		
LMK1D1212	2:12	Global output enable control through pin control	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208P	2:8	Individual output enable control through pin control	350 mV	VQGN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208I	2:8	Individual output enable control through I^2C	350 mV	VQFN (40)	6.00 mm × 6.00 mm
			500 mV		
LMK1D1208	2:8	Global output enable control through pin control	350 mV	VQFN (28)	5.00 mm × 5.00 mm
LMK1D1204P	2:4	Individual output enable control through pin control	350 mV	VQGN (28)	5.00 mm × 5.00 mm
LMK1D1204	2:4	Global output enable control through pin control	350 mV	VQFN (16)	3.00 mm × 3.00 mm

6 Pin Configuration and Functions

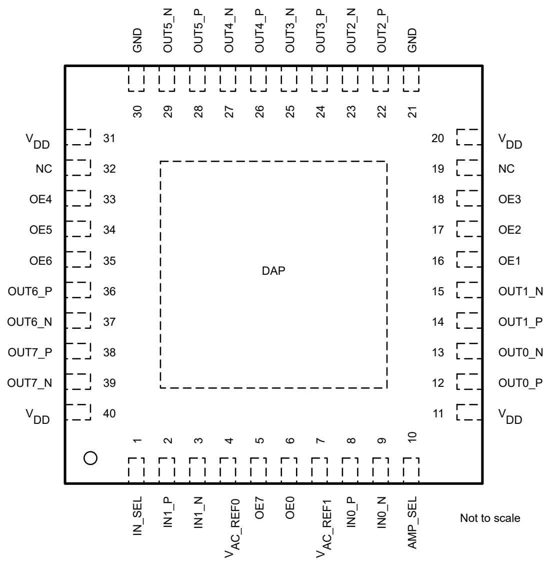


図 6-1. LMK1D1208P: RHA Package 40-Pin VQFN Top View

表 6-1. Pin Functions

NAME	NO.	TYPE[1]	DESCRIPTION
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT			
IN0_P	8	I	Primary: Differential input pair or single-ended input
IN0_N	9		
IN1_P	2	I	Secondary: Differential input pair or single-ended input. Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N.
IN1_N	3		
INPUT SELECT			
IN_SEL	1	I	Input selection with an internal 500-kΩ pullup and 320-kΩ pulldown, selects input port. See 表 9-2.
AMPLITUDE SELECT			
AMP_SEL	10	I	Output amplitude swing select with an internal 500-kΩ pullup and 320-kΩ pulldown. See 表 9-4.
OUTPUT ENABLE			
OE0	6	I	Output Enable for channel 0 HIGH (default): Enable output channel 0 LOW: Disable output channel 0 in Hi-Z state
OE1	16	I	Output Enable for channel 1 HIGH (default): Enable output channel 1 LOW: Disable output channel 1 in Hi-Z state
OE2	17	I	Output Enable for channel 2 HIGH (default): Enable output channel 2 LOW: Disable output channel 2 in Hi-Z state
OE3	18	I	Output Enable for channel 3 HIGH (default): Enable output channel 3 LOW: Disable output channel 3 in Hi-Z state
OE4	33	I	Output Enable for channel 4 HIGH (default): Enable output channel 4 LOW: Disable output channel 4 in Hi-Z state

表 6-1. Pin Functions (continued)

NAME	NO.	TYPE[1]	DESCRIPTION
OE5	34	I	Output Enable for channel 5 HIGH (default): Enable output channel 5 LOW: Disable output channel 5 in Hi-Z state
OE6	35	I	Output Enable for channel 6 HIGH (default): Enable output channel 6 LOW: Disable output channel 6 in Hi-Z state
OE7	5	I	Output Enable for channel 7 HIGH (default): Enable output channel 7 LOW: Disable output channel 7 in Hi-Z state
BIAS VOLTAGE OUTPUT			
V_{AC_REF0}	4	O	Bias voltage output for capacitive-coupled inputs. If used, TI recommends using a 0.1-μF capacitor to GND on this pin.
V_{AC_REF1}	7		
DIFFERENTIAL CLOCK OUTPUT			
OUT0_P	12	O	Differential LVDS output pair number 0
OUT0_N	13		
OUT1_P	14	O	Differential LVDS output pair number 1
OUT1_N	15		
OUT2_P	22	O	Differential LVDS output pair number 2
OUT2_N	23		
OUT3_P	24	O	Differential LVDS output pair number 3
OUT3_N	25		
OUT4_P	26	O	Differential LVDS output pair number 4
OUT4_N	27		
OUT5_P	28	O	Differential LVDS output pair number 5
OUT5_N	29		
OUT6_P	36	O	Differential LVDS output pair number 6
OUT6_N	37		
OUT7_P	38	O	Differential LVDS output pair number 7
OUT7_N	39		
SUPPLY VOLTAGE			
V_{DD}	11, 20, 31, 40	P	Device power supply (1.8 V, 2.5 V, or 3.3 V)
GROUND			
GND	21, 30	G	Ground
MISC			
DAP	DAP	G	Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation.
NC	19, 32	—	No Connection. Leave floating.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	3.6	V
V_O	Output voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_J	Junction temperature		135	°C
T_{stg}	Storage temperature (2)	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device unpowered

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90 % of VDD)	0.1		20	ms
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		135	°C

7.4 Thermal Information

THERMAL METRIC[1]		LMK1D1208P	UNIT
		RHA (VQFN)	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_{STAT}	Core supply current, static (LMK1D1208P)	All outputs enabled and unterminated, f = 0 Hz		75		mA
IDD_{100M}	Core supply current (LMK1D1208P)	All outputs enabled, R_L = 100 Ω, f =100 MHz		87	110	mA
IN_SEL/AMP_SEL CONTROL INPUT CHARACTERISTICS (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
Vd_{I3}	Tri-state input	Open		0.4 × V_{CC}		V
V_{IH}	Input high voltage	Minimum input voltage for a logical "1" state in table 1	0.7 × V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Maximum input voltage for a logical "0" state in table 1	–0.3		0.3 × V_{CC}	V
I_{IH}	Input high current	V_{DD} can be 1.8V, 2.5V, or 3.3V with V_{IH} = V_{DD}			30	µA
I_{IL}	Input low current	V_{DD} can be 1.8V, 2.5V, or 3.3V with V_{IH} = V_{DD}	–30			µA
$R_{pull\text{-}up}$	Input pullup resistor			500		kΩ
$R_{pull\text{-}down}$	Input pulldown resistor			320		kΩ
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input	DC		250	MHz
$V_{IN\_S\text{-}E}$	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4		3.465	V
dVIN/dt	Input Slew Rate (20% to 80% of the amplitude)		0.05			V/ns
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{IH} = 3.465 V			60	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{IL} = 0 V	–30			µA
C_{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input			2	GHz
$V_{IN,DIFF(p\text{-}p)}$	Differential input voltage peak-to-peak {2 × ($V_{INP} - V_{INN}$)}	V_{ICM} = 1 V (V_{DD} = 1.8 V)	0.3		2.4	V_{PP}
		V_{ICM} = 1.25 V (V_{DD} = 2.5 V/3.3 V)	0.3		2.4	
V_{ICM}	Input common-mode voltage	$V_{IN,DIFF(P\text{-}P)}$ > 0.4 V (V_{DD} = 1.8 V/2.5 V/3.3 V)	0.25		2.3	V
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{INP} = 2.4 V, V_{INN} = 1.2 V			30	µA

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{INP} = 0 V, V_{INN} = 1.2 V	–30			µA
C_{IN_SE}	Input capacitance (Single-ended)	at 25°C		3.5		pF
LVDS DC OUTPUT CHARACTERISTICS						
|VOD|	Differential output voltage magnitude |V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	250	350	450	mV
|VOD|	Differential output voltage magnitude |V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	400	500	650	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
$V_{OC(SS)}$	Steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V)	1		1.2	V
		$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V)	1.1		1.375	
$V_{OC(SS)}$	Steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V), AMP_SEL = 1	0.8		1.05	V
		$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V), AMP_SEL = 1	0.9		1.15	
$\Delta_{VOC(SS)}$	Change in steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
$\Delta_{VOC(SS)}$	Change in steady-state, common-mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
LVDS AC OUTPUT CHARACTERISTICS						
V_{ring}	Output overshoot and undershoot	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, f_{OUT} = 491.52 MHz	–0.1		0.1	V_{OD}
V_{OS}	Output AC common-mode voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω		50	100	mV_{pp}
V_{OS}	Output AC common-mode voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1		75	150	mV_{pp}
I_{OS}	Short-circuit output current (differential)	V_{OUTP} = V_{OUTN}	–12		12	mA
$I_{OS(cm)}$	Short-circuit output current (common-mode)	V_{OUTP} = V_{OUTN} = 0	–24		24	mA
t_{PD}	Propagation delay	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (1)	0.3		0.575	ns
$t_{SK,\ O}$	Output skew	Skew between outputs with the same load conditions (12 and 16 channels) (2)			20	ps
$t_{SK,\ PP}$	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			200	ps
$t_{SK,\ P}$	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (4)	–20		20	ps
$t_{RJIT(ADD)}$	Random additive Jitter (rms)	f_{IN} = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12 kHz to 20 MHz, with output load R_{LOAD} = 100 Ω		45	60	fs, RMS

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise	Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R_{LOAD} = 100 Ω	PN_{1kHz}		–143		dBc/Hz
		PN_{10kHz}		–150		
		PN_{100kHz}		–157		
		PN_{1MHz}		–160		
		PN_{floor}		–164		
MUX_{ISO}	Mux Isolation	f_{IN} = 156.25 MHz. The difference in power level at f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_R/t_F	Output rise and fall time	20% to 80% with R_{LOAD} = 100 Ω			300	ps
t_R/t_F	Output rise and fall time	20% to 80% with RLOAD = 100 Ω (AMP_SEL= 1)			300	ps
$t_{en/disable}$	Output Enable and Disable Time	Time taken for outputs to go from disable state to enable state and vice versa. (3)			1	µs
I_{leakZ}	Output leakage current in High Z	Outputs are held in high Z mode with OUTP = OUTN (max applied external voltage is the lesser of VDD or 1.89V and minimum applied external voltage is 0V)			50	µA
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{LOAD} = 100 µA	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) V_{DD} = 2.5 V/ 3.3 V						
PSNR	Power Supply Noise Rejection ($f_{carrier}$ = 156.25 MHz)	10 kHz, 100 mVpp ripple injected on V_{DD}		–70		dBc
		1 MHz, 100 mVpp ripple injected on V_{DD}		–50		

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
(3) Applies to the dual bank family.
(4) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

7.6 Typical Characteristics

図 7-1 captures the variation of the LMK1D1208P current consumption with input frequency and supply voltage. 図 7-2 shows the variation of the differential output voltage (VOD) swept across frequency. It is important to note that 図 7-1 and 図 7-2 serve as a guidance to the users on what to expect for the range of operating frequency supported by LMK1D1208P. These graphs were plotted for a limited number of frequencies and load conditions, which may not represent the customer system.

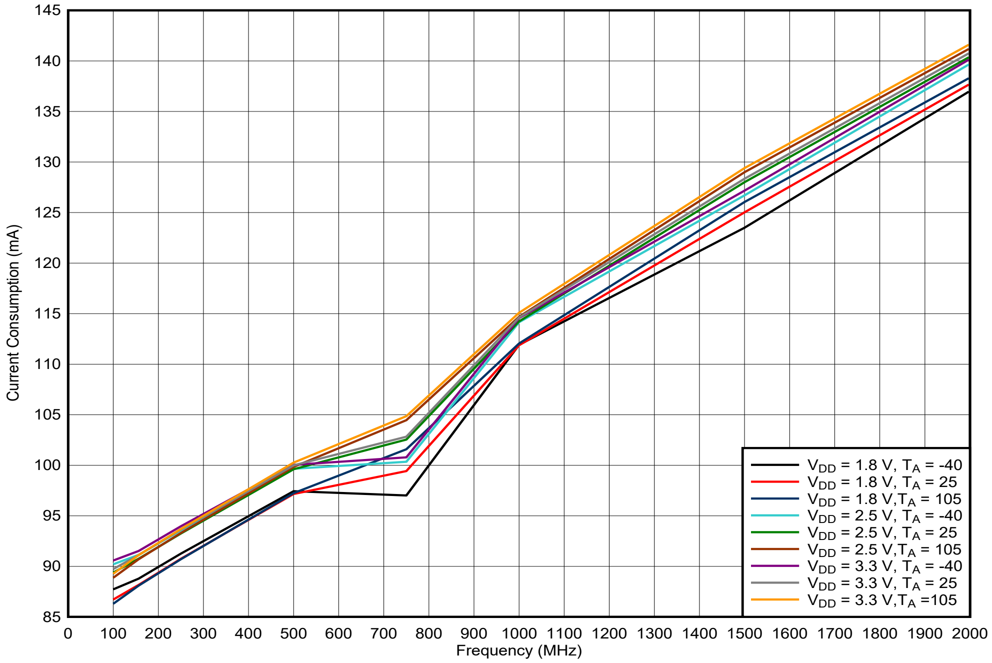


図 7-1. LMK1D1208P Current Consumption vs Frequency

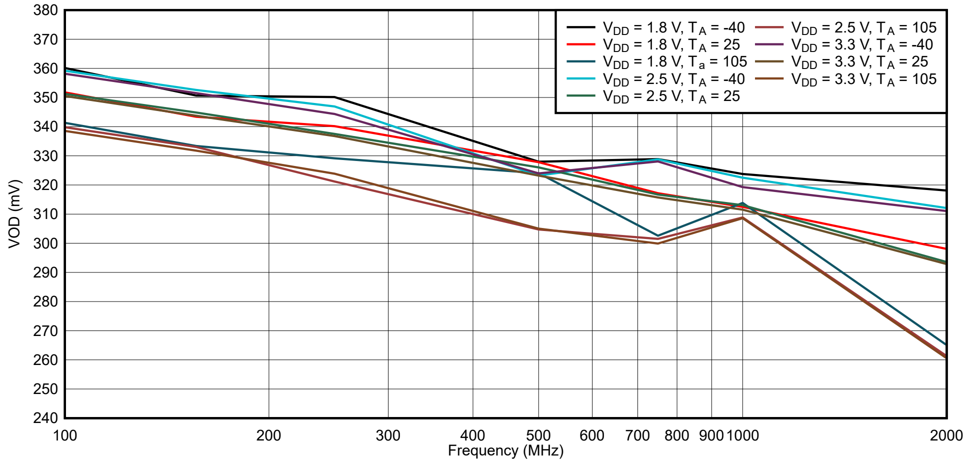


図 7-2. LMK1D1208P VOD vs Frequency

8 Parameter Measurement Information

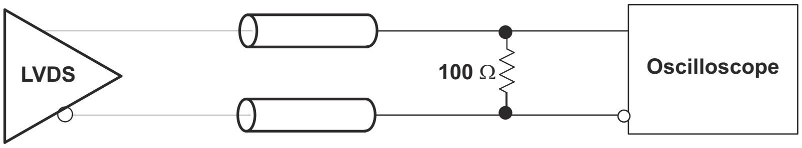


図 8-1. LVDS Output DC Configuration During Device Test

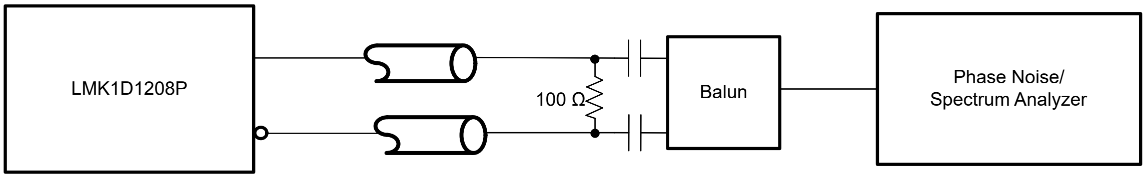


図 8-2. LVDS Output AC Configuration During Device Test

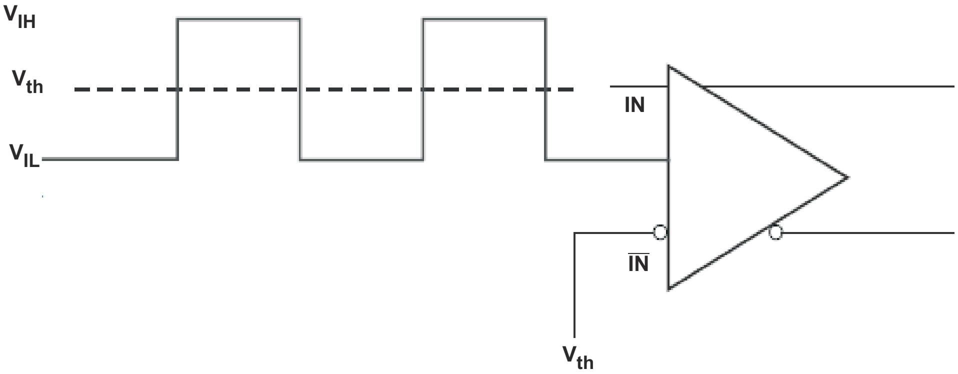


図 8-3. DC-Coupled LVCMOS Input During Device Test

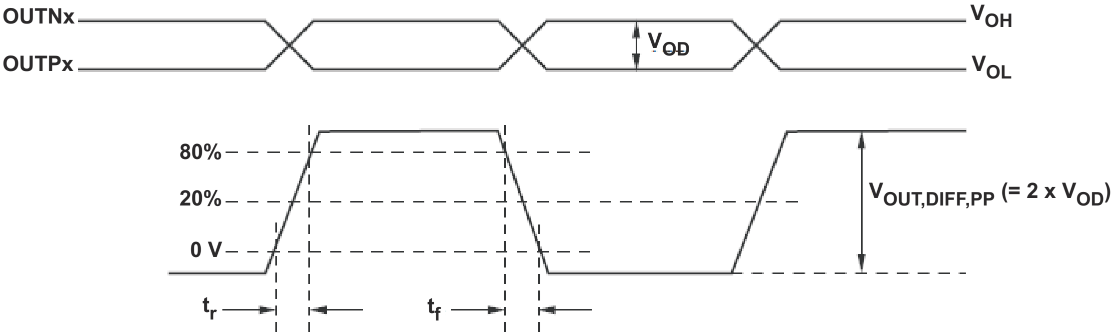
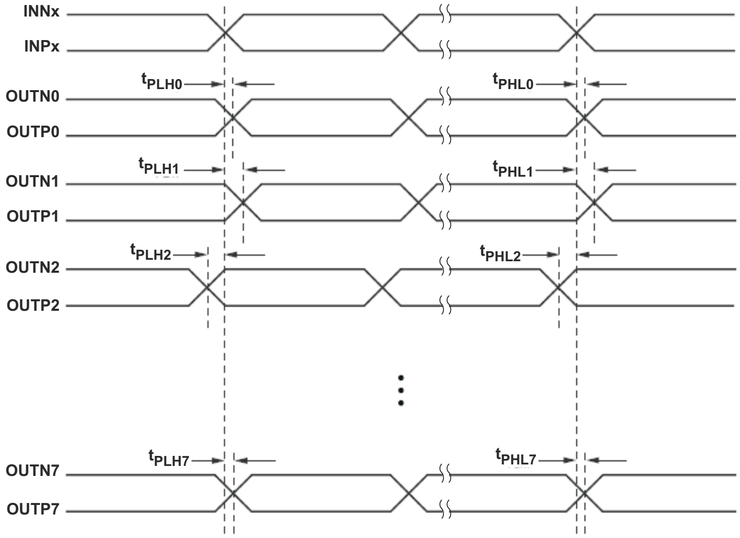


図 8-4. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..7)

B. Part to part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..7)

図 8-5. Output Skew and Part-to-Part Skew

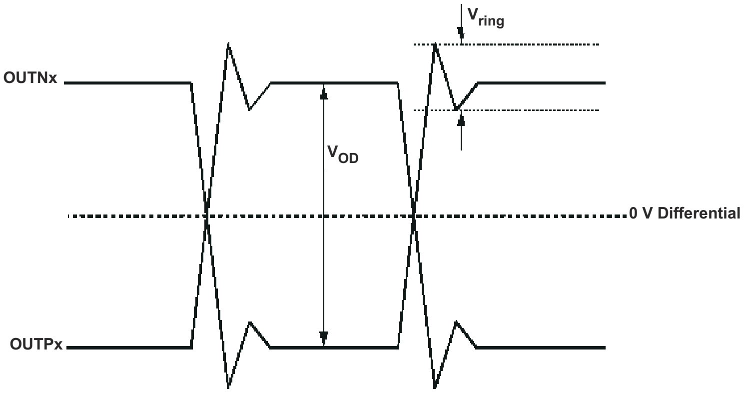


図 8-6. Output Overshoot and Undershoot

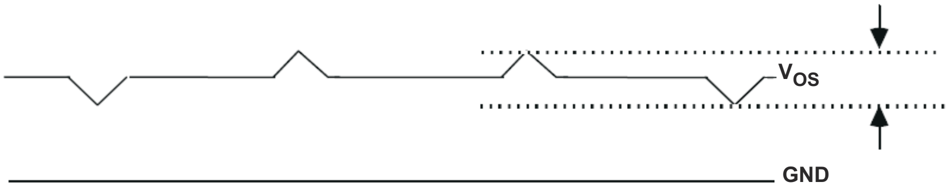


図 8-7. Output AC Common Mode

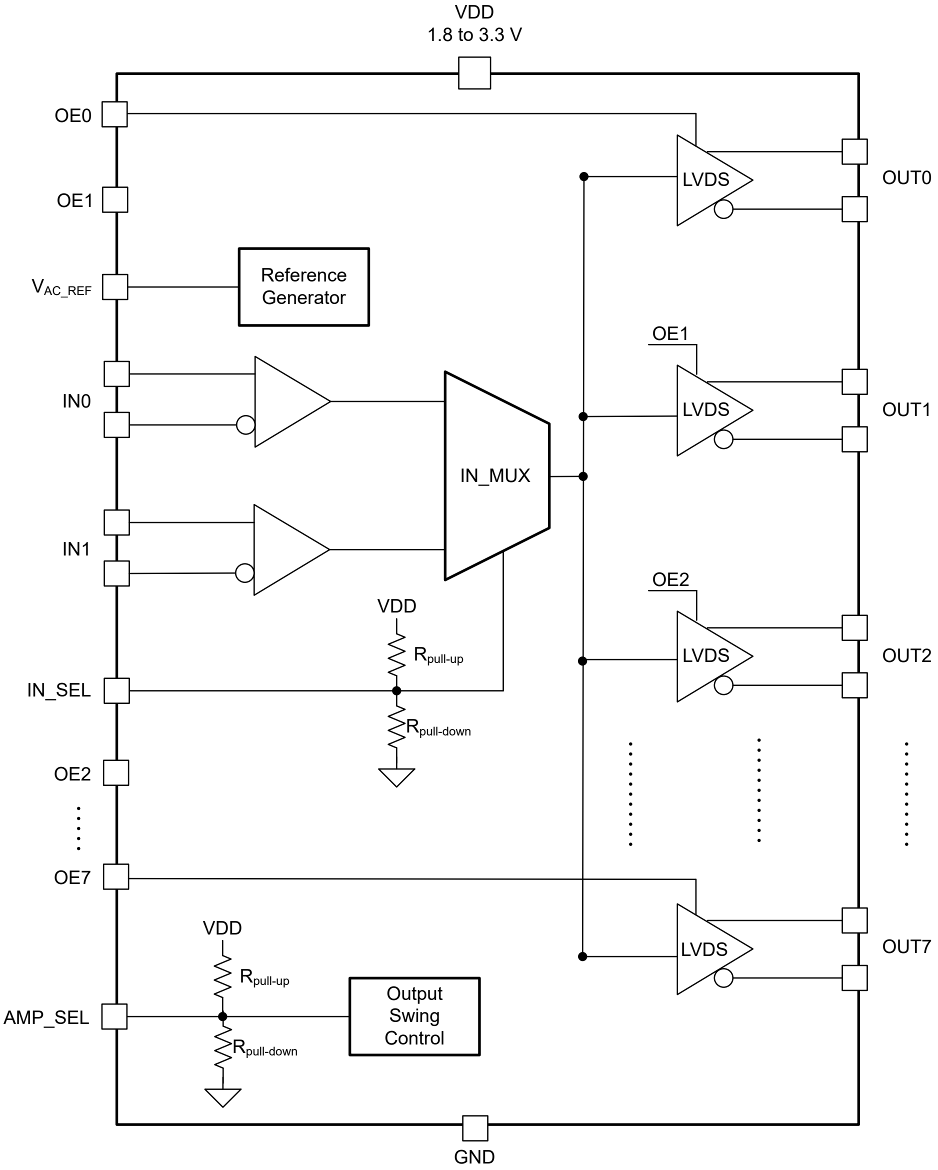
9 Detailed Description

9.1 Overview

The LMK1D1208P LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D1208P, AC coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

9.2 Functional Block Diagram



9.3 Feature Description

The LMK1D1208P is a low additive jitter LVDS fan-out buffer that can generate up to four copies of two selectable LVPECL, LVDS, HCSL, CML, or LVCMOS inputs. The LMK1D1208P can accept reference clock frequencies up to 2 GHz while providing low output skew.

表 9-1 lists the LMK1D1208P outputs divided into two banks.

表 9-1. Output Bank Mapping

BANK	CLOCK OUTPUTS
0	OUT0, OUT1, OUT2, OUT3
1	OUT4, OUT5, OUT6, OUT7

Apart from providing a very low additive jitter and low output skew, the LMK1D1208P has an input select pin (IN_SEL) and an output amplitude control pin (AMP_SEL).

9.3.1 Fail-Safe Input

The LMK1D120x family of devices is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to *Specifications* for more information on the maximum input supported by the device. The user should note that incorporating the fail-safe inputs also results in a slight increase in clock input pin capacitance. The device also incorporates an input hysteresis which prevents random oscillation in absence of an input signal. Furthermore, this feature allows the input pins to be left open.

9.4 Device Functional Modes

The two inputs of the LMK1D1208P are internally muxed together and can be selected through the control pin (see 表 9-2). Unused inputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D1208P to provide greater system flexibility.

表 9-2. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	IN0_P, IN0_N
1	IN1_P, IN1_N
Open	None (1)

(1) The input buffers are disabled and the state of the outputs are dependent on the state of OEx (see 表 9-3). If OEx = 0, the corresponding output will be disabled in Hi-Z state, whereas if OEx = 1 (default), the corresponding output will be logic low.

The outputs of the LMK1D1208P can be individually enabled or disabled using the OEx hardware pins (see 表 9-3). The disabled state of the outputs is Hi-Z (high impedance) as this reduces the power consumption and also prevents back-biasing of the devices connected to these outputs.

Unused outputs should be disabled to eliminate the need for a termination resistor. In the case of enabled unused outputs, TI recommends a 100-Ω termination for optimal performance.

表 9-3. Output Control

OEx	CLOCK OUTPUTS
0	OUTPx, OUTNx disabled in Hi-Z state
1 (default)	OUTPx, OUTNx enabled

The output amplitude of the banks of the LMK1D1208P can be selected through the amplitude selection pin (see 表 9-4). The higher output amplitude mode (boosted LVDS swing mode) can be used in applications which require higher amplitude either for better noise performance (higher slew rate) or if the receiver has swing requirements which the standard LVDS swing cannot meet.

表 9-4. Amplitude Selection

AMP_SEL	OUTPUT AMPLITUDE (mV)
0	Bank 0: boosted LVDS swing (500 mV) Bank 1: standard LVDS swing (350 mV)
OPEN	Bank 0: standard LVDS swing (350 mV) Bank 1: standard LVDS swing (350 mV)
1	Bank 0: boosted LVDS swing (500 mV) Bank 1: boosted LVDS swing (500 mV)

9.4.1 LVDS Output Termination

TI recommends that unused outputs are terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D1208P can be connected to LVDS receiver inputs with DC and AC coupling as shown in 図 9-1 and 図 9-2, respectively.

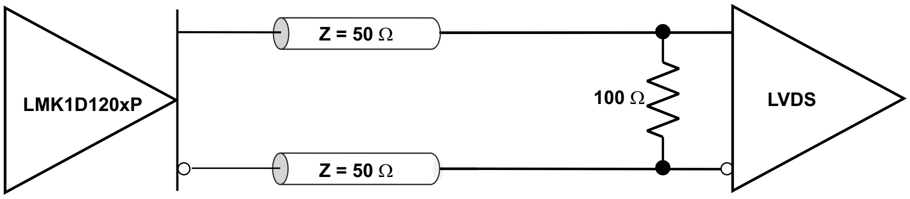


図 9-1. Output DC Termination

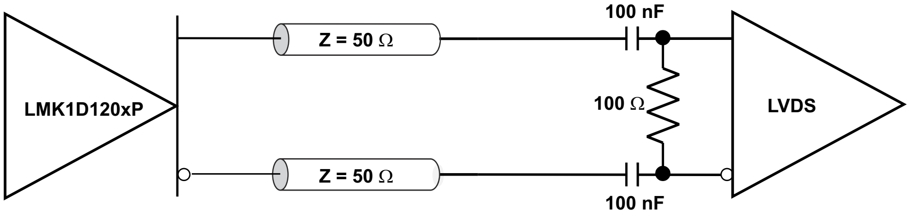


図 9-2. Output AC Termination (With the Receiver Internally Biased)

9.4.2 Input Termination

The LMK1D1208P inputs can be interfaced with LVDS, LVPECL, HCSL, or LVCMOS drivers.

LVDS drivers can be connected to LMK1D1208P inputs with DC and AC coupling as shown 図 9-3 and 図 9-4, respectively.

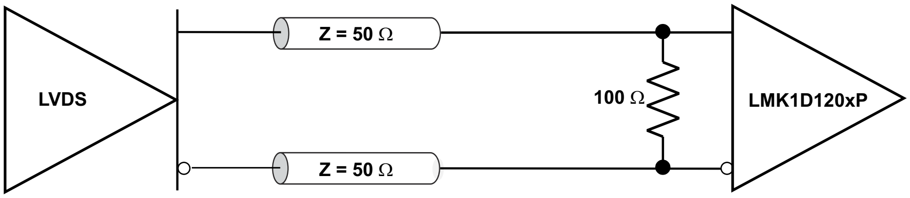


図 9-3. LVDS Clock Driver Connected to LMK1D1208P Input (DC-Coupled)

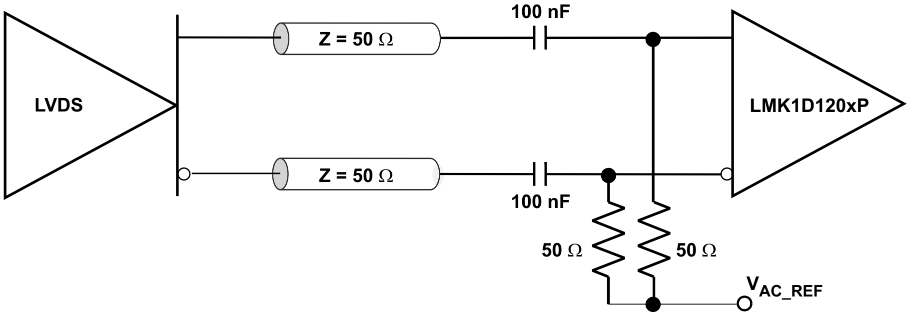


図 9-4. LVDS Clock Driver Connected to LMK1D1208P Input (AC-Coupled)

図 9-5 shows how to connect LVPECL inputs to the LMK1D1208P. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

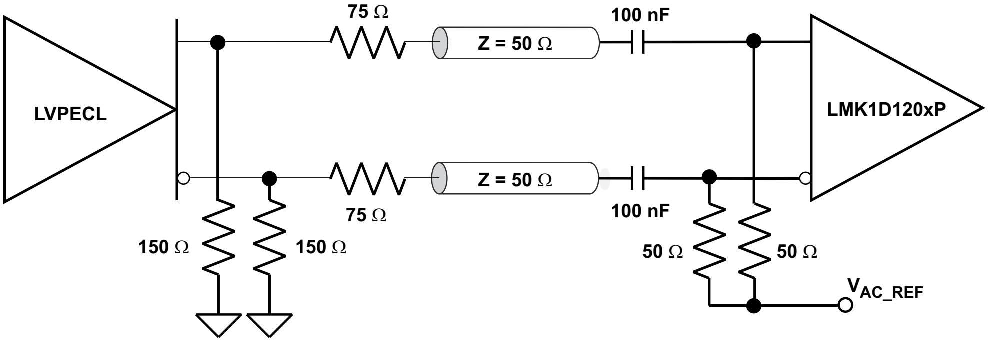


図 9-5. LVPECL Clock Driver Connected to LMK1D1208P Input

図 9-6 shows how to couple a LVCMOS clock input to the LMK1D1208P directly.

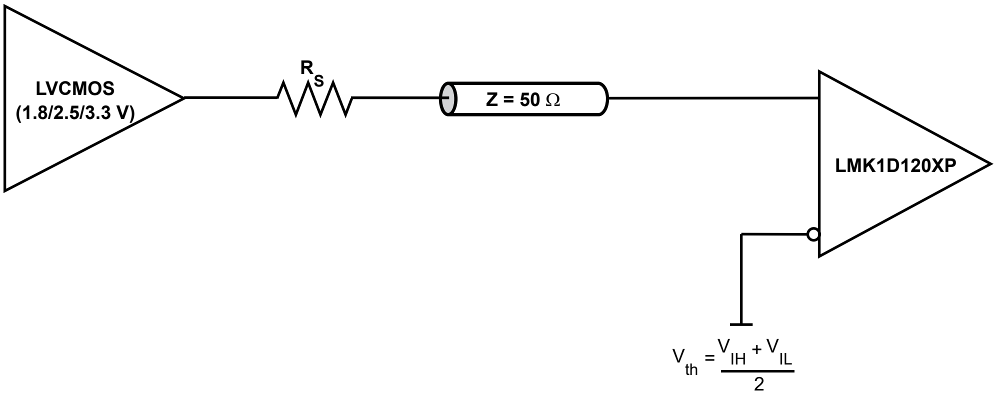


図 9-6. 1.8-V, 2.5-V, or 3.3-V LVCMOS Clock Driver Connected to LMK1D1208P Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK1D1208P is a low additive jitter universal to LVDS fan-out buffer with two selectable inputs, output amplitude selection, and pin-controlled output enables. The small package size, low output skew, low propagation delay and low additive jitter of this device is designed for applications that require high-performance clock distribution as well as for low-power and space-constraint applications.

10.2 Typical Application

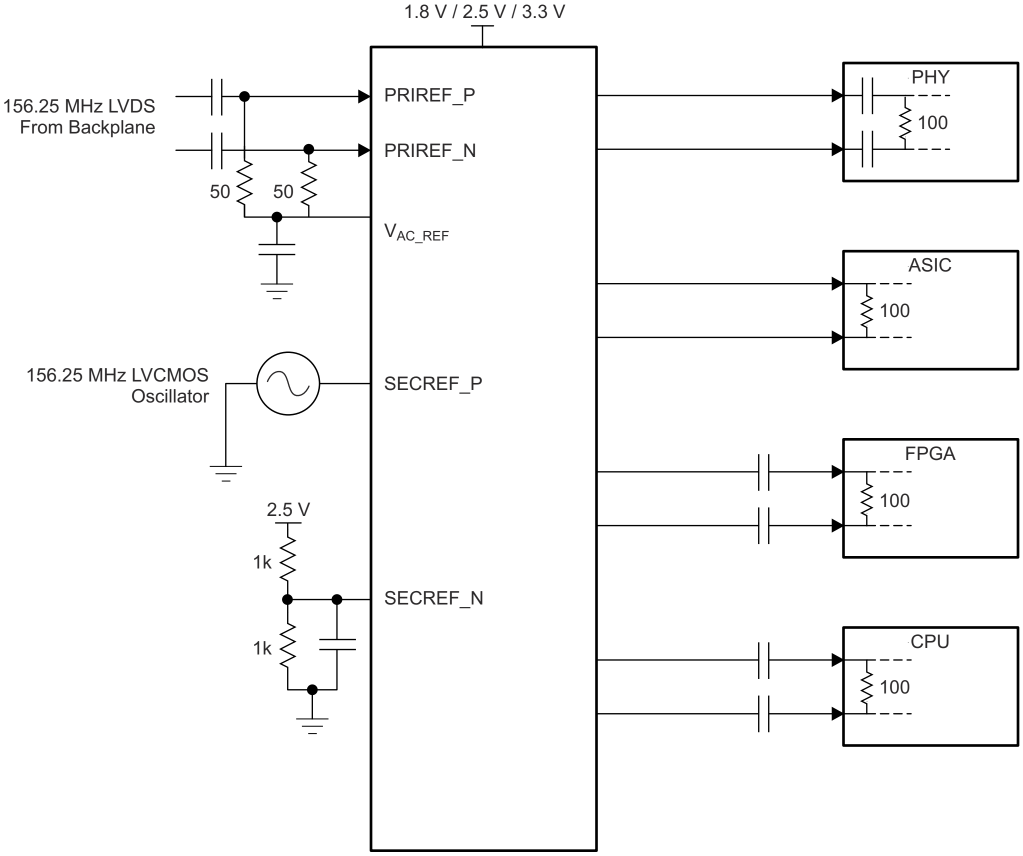


図 10-1. Fan-Out Buffer for Line Card Application

10.2.1 Design Requirements

The LMK1D1208P shown in 図 10-1 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz, LVCMOS, 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-μF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC coupling with an LVDS driver such as the LMK1D1208P. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D1208P. Again, no additional components are required.
- The FPGA requires external AC coupling, but has internal termination. 0.1-μF capacitors are placed to provide AC coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- The unused outputs of the LMK1D1208P can be disabled using the corresponding OEx pin. This results in a lower power consumption.

10.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

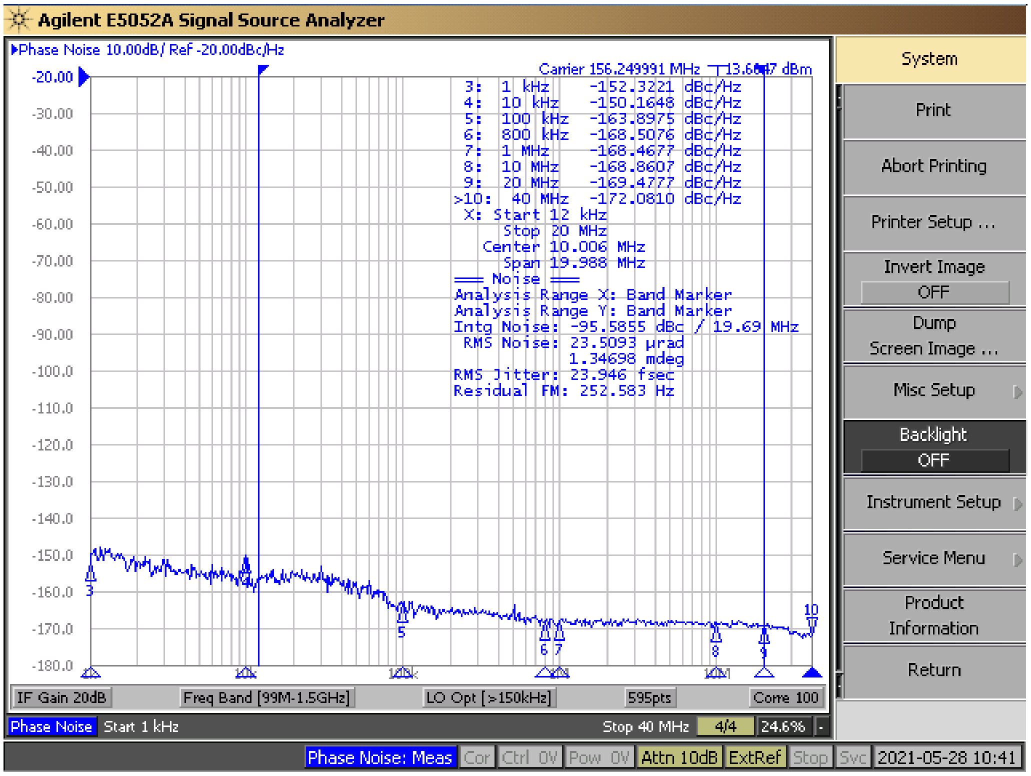
Unused outputs can be disabled using the corresponding OEx pin setting according to 表 9-3. Disabling the outputs also eliminates requirement of termination resistors.

In this example, the PHY, ASIC, FPGA and CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* user's guide (SCAU043).

10.2.3 Application Curves

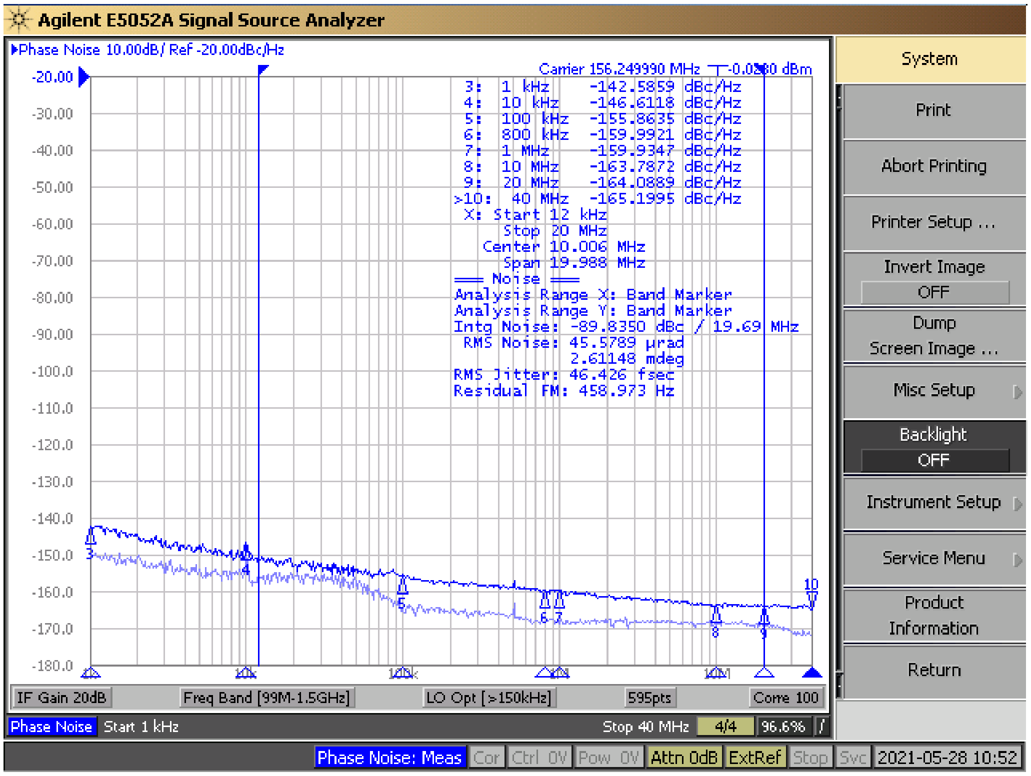
This section shows the low additive noise for the LMK1D1208P. The low noise 156.25-MHz source with 24-fs RMS jitter shown in 図 10-2 drives the LMK1D1208P, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (see 図 10-3). The resultant additive jitter is 39.7-fs RMS for this configuration.



```
Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 156.249991 MHz  13.6[illegible]7 dBm
   3:   1 kHz     -152.3221 dBc/Hz
   4:  10 kHz     -150.1648 dBc/Hz
   5: 100 kHz     -163.8975 dBc/Hz
   6: 800 kHz     -168.5076 dBc/Hz
   7:   1 MHz     -168.4677 dBc/Hz
   8:  10 MHz     -168.8607 dBc/Hz
   9:  20 MHz     -169.4777 dBc/Hz
 >10:  40 MHz     -172.0810 dBc/Hz
   X: Start 12 kHz
          Stop 20 MHz
        Center 10.006 MHz
          Span 19.988 MHz
 === Noise ===
 Analysis Range X: Band Marker
 Analysis Range Y: Band Marker
 Intg Noise: -95.5855 dBc / 19.69 MHz
  RMS Noise: 23.5093 µrad
             1.34698 mdeg
 RMS Jitter: 23.946 fsec
 Residual FM: 252.583 Hz
```

Note: Reference signal is a low-noise Rhode and Schwarz SMA100B

図 10-2. LMK1D1208P Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)



```
Carrier 156.249990 MHz   -0.0[illegible]0 dBm
  3:  1 kHz     -142.5859 dBc/Hz
  4:  10 kHz    -146.6118 dBc/Hz
  5:  100 kHz   -155.8635 dBc/Hz
  6:  800 kHz   -159.9921 dBc/Hz
  7:  1 MHz     -159.9347 dBc/Hz
  8:  10 MHz    -163.7872 dBc/Hz
  9:  20 MHz    -164.0889 dBc/Hz
>10:   40 MHz   -165.1995 dBc/Hz
  X: Start 12 kHz
         Stop 20 MHz
       Center 10.006 MHz
         Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -89.8350 dBc / 19.69 MHz
 RMS Noise: 45.5789 µrad
            2.61148 mdeg
RMS Jitter: 46.426 fsec
Residual FM: 458.973 Hz
```

```
IF Gain 20dB   Freq Band [99M-1.5GHz]   LO Opt [>150kHz]   595pts   Corre 100
Phase Noise  Start 1 kHz   Stop 40 MHz   4/4   96.6%
Phase Noise: Meas  Cor  Ctrl 0V  Pow 0V  Attn 0dB  ExtRef  Stop  Svc  2021-05-28 10:52
```

図 10-3. LMK1D1208P Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These ferrite beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

図 10-4 shows this recommended power-supply decoupling method.

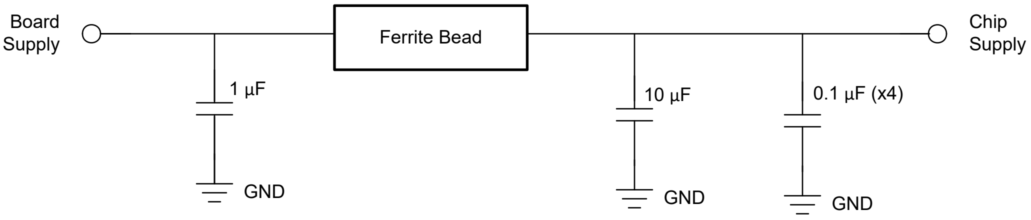


図 10-4. Power Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the PCB. To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. 図 10-5 and 図 10-6 show the recommended land and via patterns for the 40-pin LMK1D1208P device.

10.4.2 Layout Examples

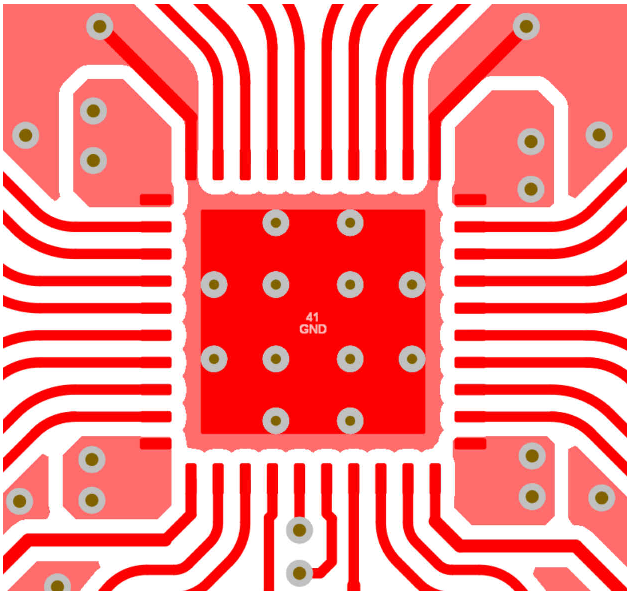


図 10-5. Recommended PCB Layout, Top Layer

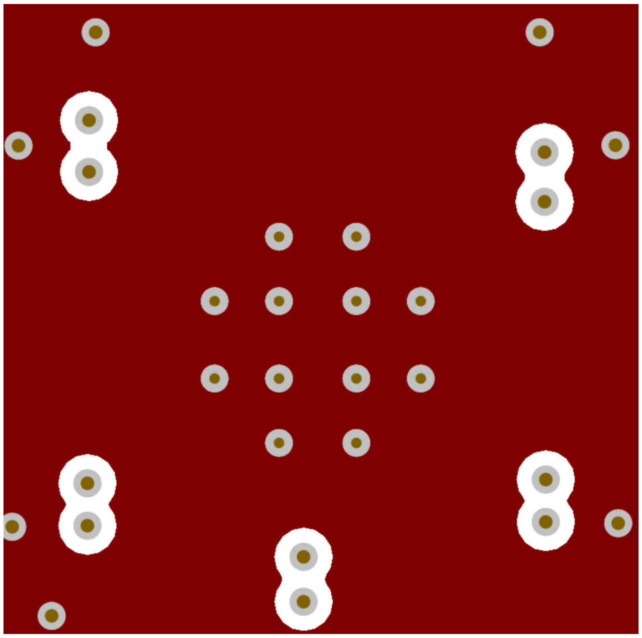


図 10-6. Recommended PCB Layout, GND Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* user's guide
- Texas Instruments, *Power Consumption of LVPECL and LVDS* Analog design journal
- Texas Instruments, *Using Thermal Calculation Tools for Analog Components* application report

11.2 サポート・リソース

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11.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1D1208PRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208P
LMK1D1208PRHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208P
LMK1D1208PRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208P
LMK1D1208PRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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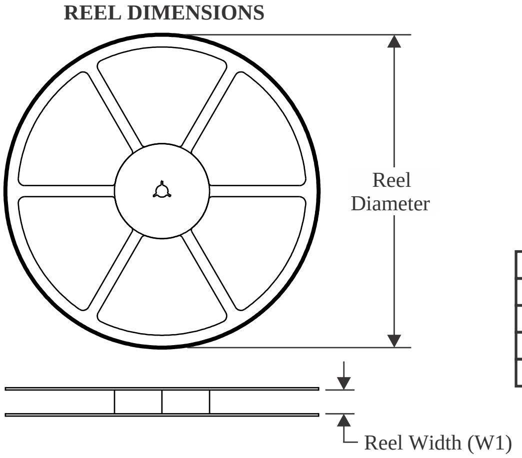
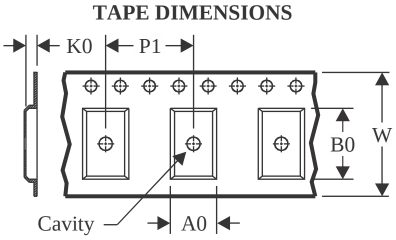
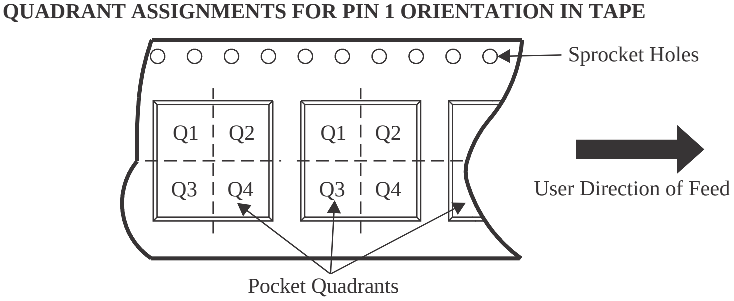
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





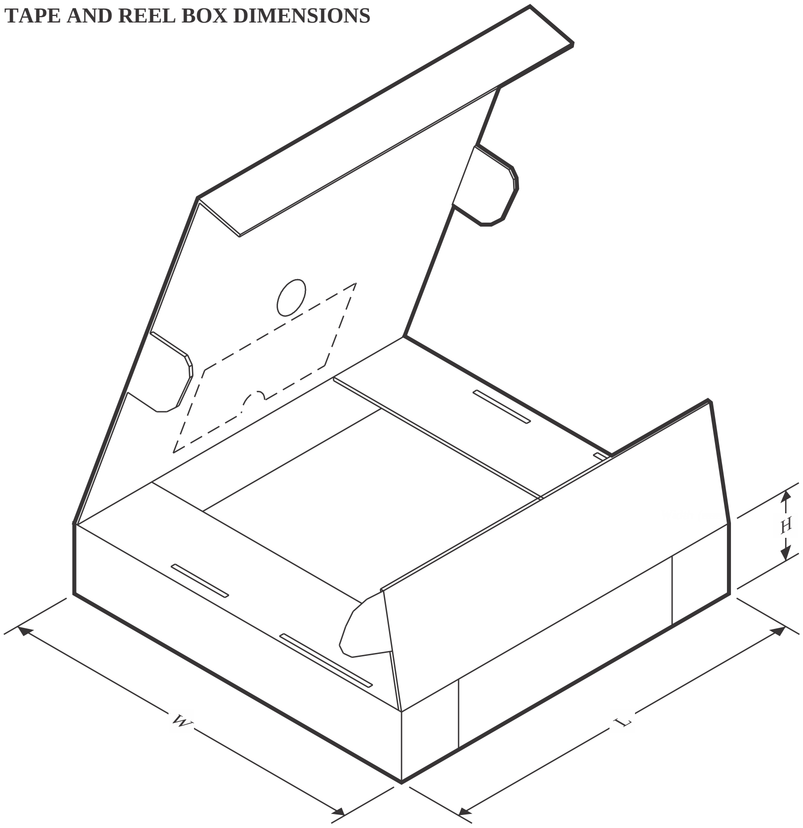
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1208PRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMK1D1208PRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1208PRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
LMK1D1208PRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

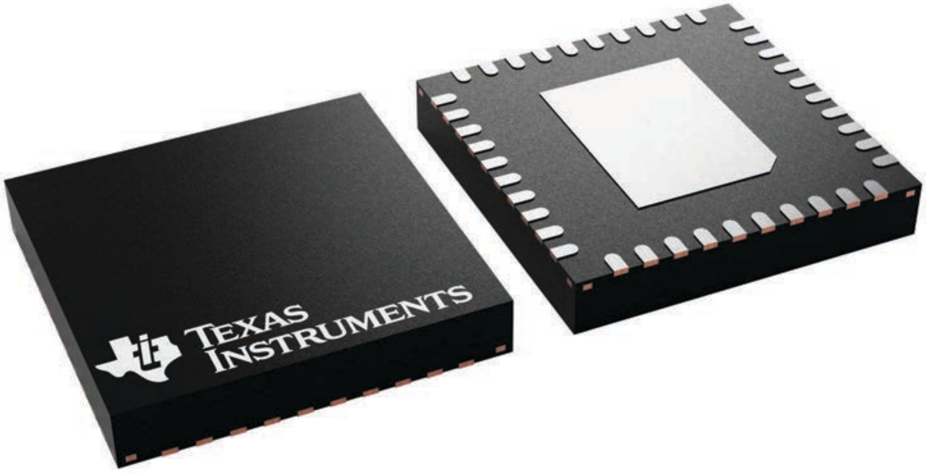
RHA 40

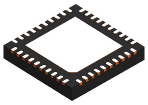
VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



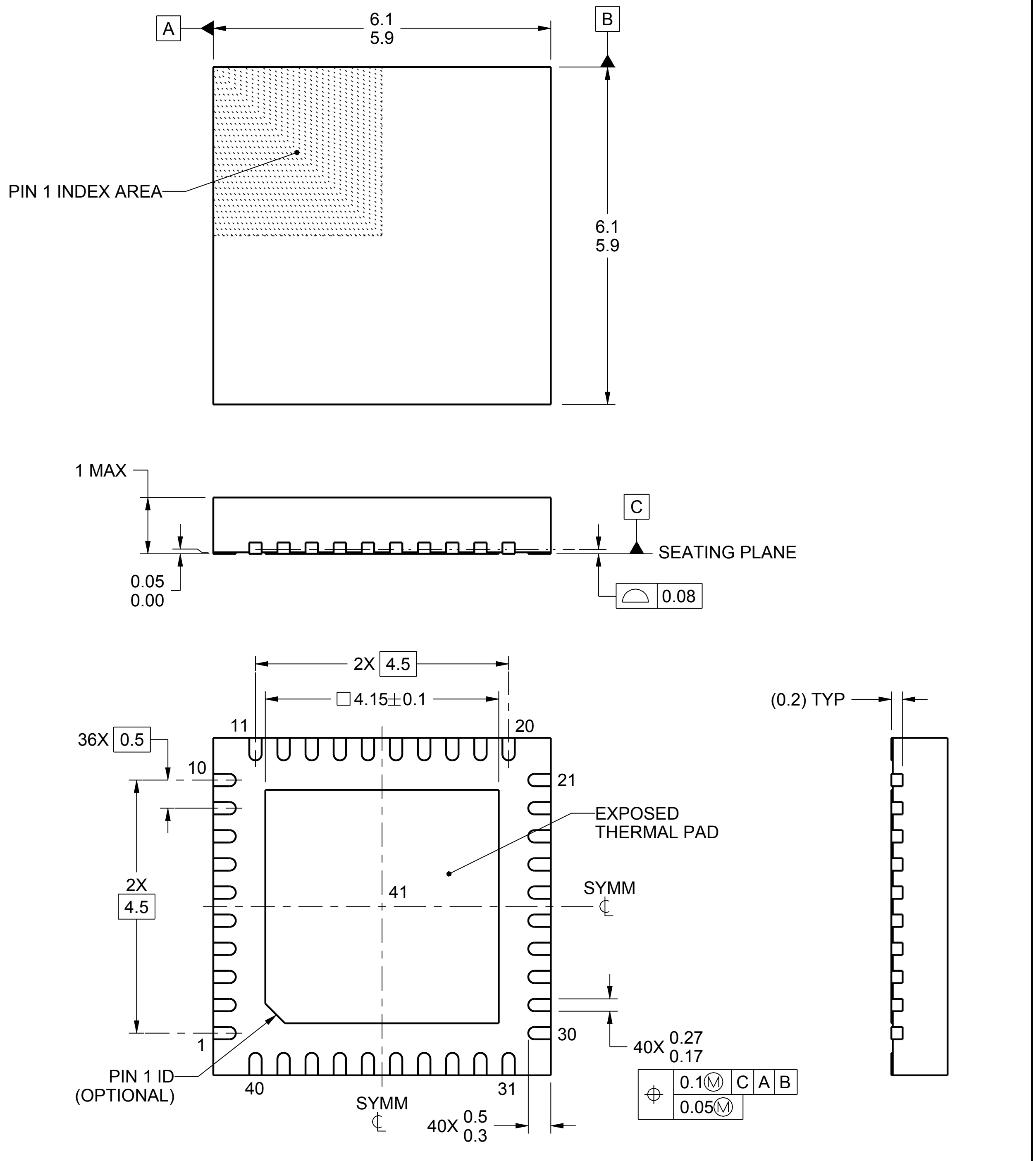


PACKAGE OUTLINE

RHA0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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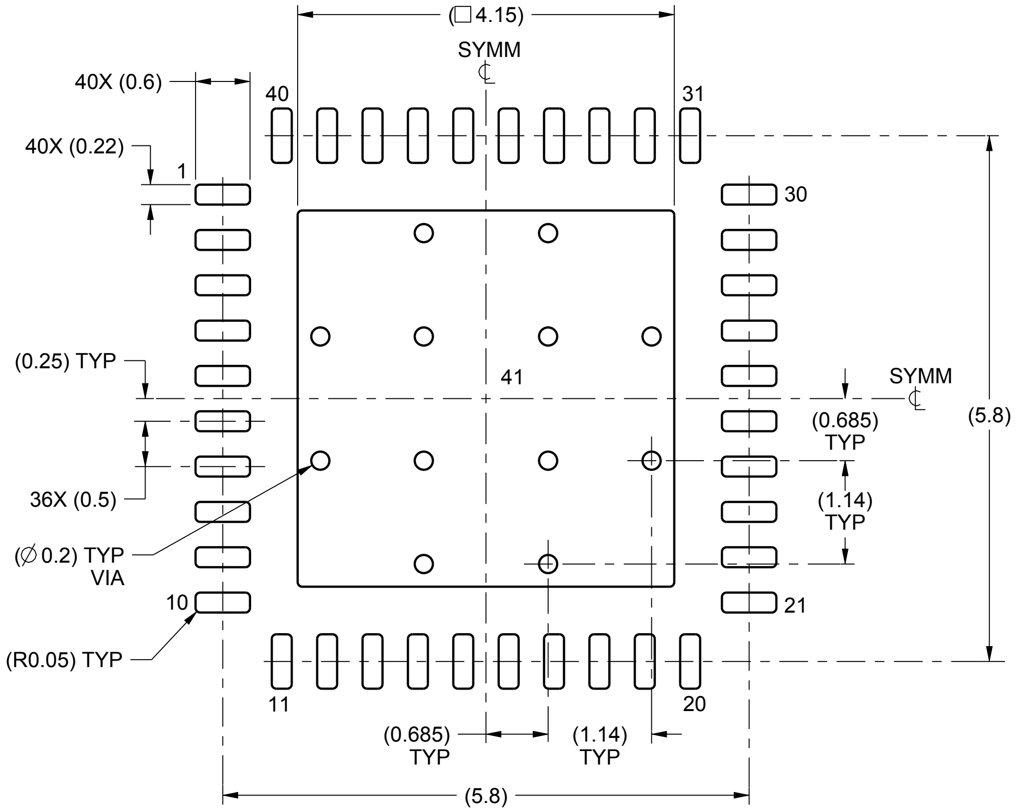
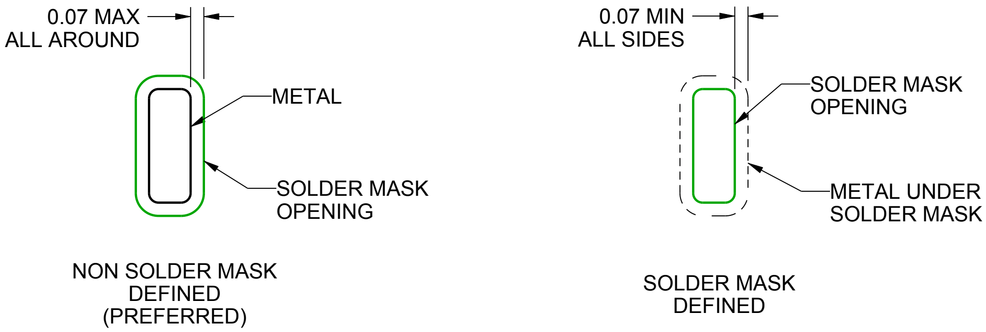
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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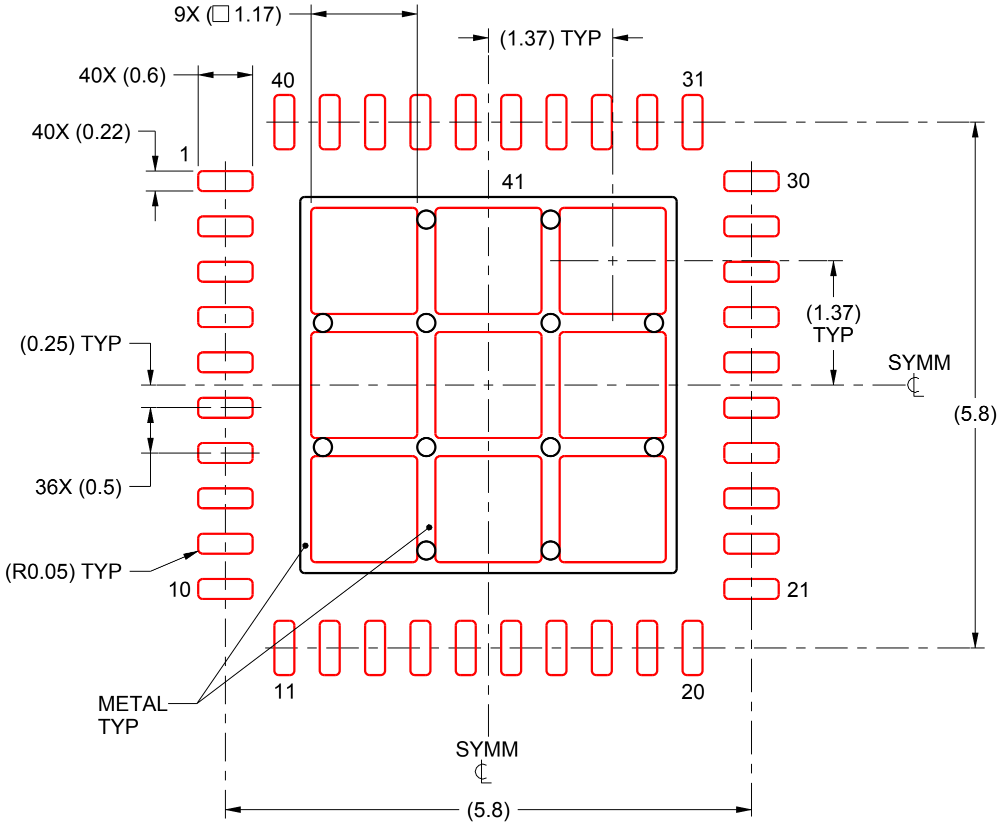
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265