LMK05318 2つの周波数領域に対応した超低ジッタ・ネットワーク・シンクロナイザ・クロック

1 特長

- デジタル位相ロック・ループ(DPLL)×1
  - ヒットレス・スイッチング：±50psの位相過渡応答
  - Fastlockによるプログラミング可能なループ帯域幅
  - 低コストのTCXO/OCXOを使用する標準準拠の同期およびホールドオーバー
- 業界をリードするジッタ性能を備えたアナログ位相同期ループ(APLL)×2
  - 312.5MHzで50fsのRMSジッタ(APLL1)
  - 155.52MHzで125fsのRMSジッタ(APLL2)
- 基準クロック入力×2
  - 優先度に基づく入力選択
  - 基準喪失時のデジタル・ホールドオーバー
- プログラマブル・ドライバによる8つのクロック出力
  - 最大6種類の出力周波数
  - AC-LVDS、AC-CML、AC-LVPECL、HCSL、および1.8VのLVCMOS出力フォーマット
- 起動時のカスタム・クロック用EEPROM/ROM
- 柔軟な構成オプション
  - 入力および出力で1Hz (1PPS)～800MHz
  - XO/TCXO/OCXO入力: 10～100MHz
  - 0.001ppb/ステップ未満のDCOモードにより高精度のクロック・ステアリングを実現（IEEE 1588 PTPスレーブ）
  - 高度なクロック監視およびステータス
  - I^2CまたはSPIインターフェイス
- PSNR: –83dBc（3.3V電源で50mVppのノイズ）
- 3.3V電源、1.8V、2.5V、または3.3V出力
- 工業用温度範囲: －40℃～＋85℃

2 アプリケーション

- SyncE (G.8262)、SONET/SDH (Stratum 3/3E、G.813、GR-1244、GR-253)、IEEE 1588 PTPスレーブ・クロック、または光伝送ネットワーク(G.709)
- 400Gライン・カード、イーサネット・スイッチおよびルーター用ファブリック・カード
- 無線基地局(BTS)、ワイヤレス・バックホール
- 試験/測定機器、医用画像処理
- 56G/112G PAM-4 PHY、ASIC、FPGA、SoC、プロセッサにおけるジッタ・クリーニング、ワンダ減衰、基準クロック生成

3 概要

LMK05318は高性能のネットワーク・シンクロナイザ・クロックであり、ジッタ・クリーニング、クロック生成、高度なクロック監視、優れたヒットレス・スイッチング性能により、通信インフラおよび産業機器の厳しいタイミング要件を満たすことができます。超低ジッタ・高PSNR (電源ノイズ除去性能)により、高速シリアル・リンクにおけるビット誤り率(BER)を低減します。

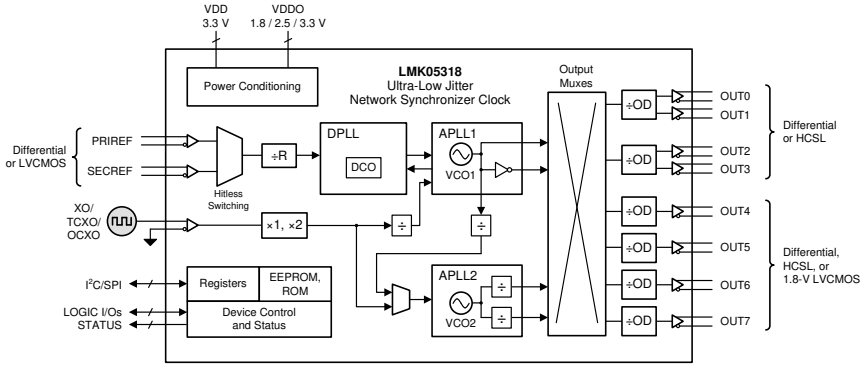
TI独自のBAW (Bulk Acoustic Wave) VCOテクノロジにより、XOおよび基準入力のジッタおよび周波数に関係なく、50fsのRMSジッタで出力クロックを生成できます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
LMK05318	VQFN（48）	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック概略図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

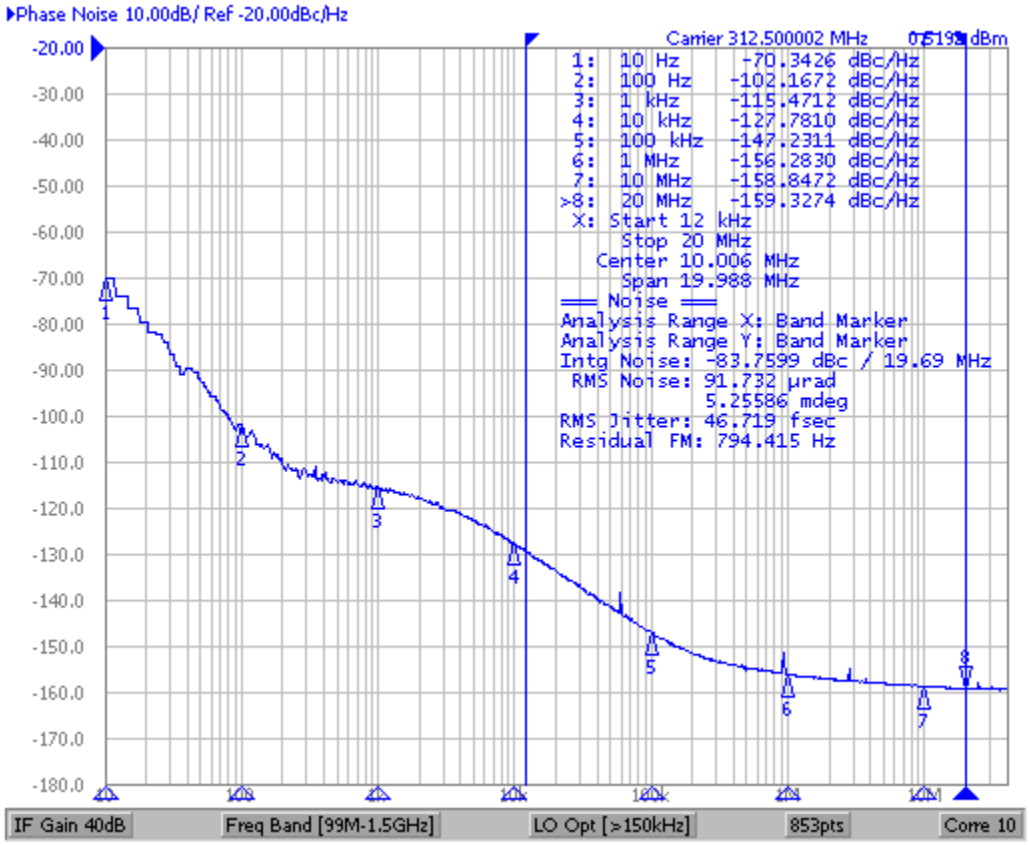
2018年6月発行のものから更新 **Page**

- デバイスのステータスを「事前情報」から「量産データ」に変更 ... 1

5 概要（続き）

DPLLはジッタ/ワンダ減衰用のプログラミング可能なループ帯域幅をサポートし、2つのAPLLはフラクショナル周波数変換をサポートしていることから、柔軟なクロック生成が実現します。DPLLでサポートする同期オプションには、位相キャンセレーションによるヒットレス・スイッチング、デジタル・ホールドオーバー、および0.001ppb未満の周波数ステップ・サイズにより高精度のクロック・ステアリング（IEEE 1588 PTPスレーブ）を実現するDCOモードがあります。DPLLは1PPS (pulse-per-second)の基準入力に位相ロックし、1つの出力でオプションのゼロ遅延モードをサポートできるため、プログラム可能なオフセットによって、決定性の入出力位相アライメントを実現します。高度な基準入力監視ブロックが、強力なクロック異常検出を実行し、基準喪失(LOR)時の出力クロックの乱れを最小限に抑えることができます。

一般的な低周波のTCXO/OCXOを使用して、同期標準に準拠したフリーラン/ホールドオーバー出力周波数安定性を確保できます。あるいは、フリーランまたはホールドオーバー時の周波数安定性やワンダが重視されない場合には、標準のXOを使用できます。I^2CまたはSPIインターフェイスによって完全にプログラミング可能であり、内蔵EEPROMまたはROMによる起動時のカスタム周波数設定にも対応しています。EEPROMは出荷時設定済みであり、必要に応じてインシステム・プログラミングも可能です。

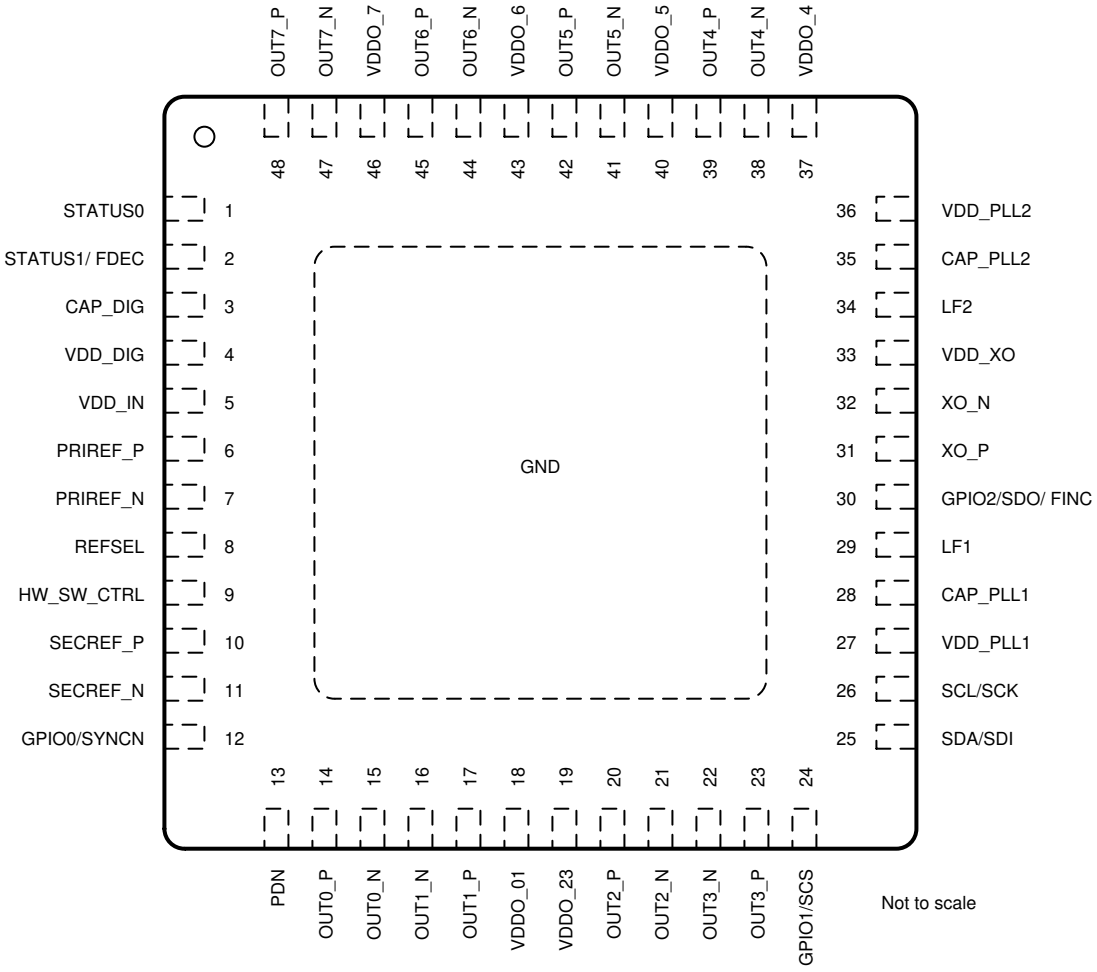


テスト条件については、Typical Characteristicsを参照してください。

図 1. 312.5MHzでの出力位相ノイズ(APLL1)、RMSジッタ50fs未満

6 Pin Configuration and Functions

RGZ Package
48-Pin QFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
POWER			
GND	PAD	G	**Ground / Thermal Pad.** The exposed pad must be connected to PCB ground for proper electrical and thermal performance. A 5×5 via pattern is recommended to connect the IC ground pad to the PCB ground layers.
VDD_IN	5	P	**Core Supply (3.3 V) for Primary and Secondary Reference Inputs.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_XO	33	P	**Core Supply (3.3 V) for XO Input.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_PLL1	27	P	**Core Supply (3.3 V) for PLL1, PLL2, and Digital Blocks.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_PLL2	36	P	
VDD_DIG	4	P	

(1) G = Ground, P = Power, I = Input, O = Output, I/O = Input or Output, A = Analog.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDDO_01	18	P	**Output Supply (1.8, 2.5, or 3.3 V) for Clock Outputs 0 to 7.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDDO_23	19	P	
VDDO_4	37	P	
VDDO_5	40	P	
VDDO_6	43	P	
VDDO_7	46	P	
CORE BLOCKS			
LF1	29	A	**External Loop Filter Capacitor for APLL1 and APLL2.** Place a nearby capacitor on each pin. For LF1, 0.47-µF is suggested for typical APLL1 loop bandwidths around 2.5 kHz. For LF2, 0.1-µF is suggested for typical APLL2 loop bandwidth around 500 kHz.
LF2	34	A	
CAP_PLL1	28	A	**External Bypass Capacitors for APLL1, APLL2, and Digital Blocks.** Place a nearby 10-µF bypass capacitor on each pin.
CAP_PLL2	35	A	
CAP_DIG	3	A	
INPUT BLOCKS			
PRIREF_P	6	I	**DPLL Primary and Secondary Reference Clock Inputs.** Each input pair can accept a differential or single-ended clock as a reference to the DPLL. Each pair has a programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock can be applied to the P input with the N input pulled down to ground. An unused input pair can be left floating.
PRIREF_N	7	I	
SECREF_P	10	I	
SECREF_N	11	I	
XO_P	31	I	**XO/TCXO/OCXO Input.** This input pair can accept a differential or single-ended clock signal from a low-jitter local oscillator as a reference to the APLLs. This input has a programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock (up to 2.5 V) can be applied to the P input with the N input pulled down to ground. A low-frequency TCXO or OCXO can be used to set the clock output frequency accuracy and stability during free-run and holdover modes. In DPLL mode, the XO frequency must have a non-integer relationship to the VCO1 frequency so APLL1 can operate in fractional mode (required for proper DPLL operation). In APLL-only mode, the XO frequency can have either an integer or non-integer relationship to the VCO1 frequency.
XO_N	32	I	
OUTPUT BLOCKS			
OUT0_P	14	O	**Clock Outputs 0 to 3 Bank.** Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL and HCSL. Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[0:3] bank is preferred for PLL1 clocks to minimize output crosstalk.
OUT0_N	15	O	
OUT1_P	17	O	
OUT1_N	16	O	
OUT2_P	20	O	
OUT2_N	21	O	
OUT3_P	23	O	
OUT3_N	22	O	
OUT4_P	39	O	**Clock Outputs 4 to 7 Bank.** Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL, HCSL, or 1.8-V LVCMOS clocks (one or two per pair). Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[4:7] bank is preferred for PLL2 clocks to minimize output crosstalk. When PLL2 is not used, the OUT[4:7] bank can be used for PLL1 clocks without risk of cross-coupling from PLL2.
OUT4_N	38	O	
OUT5_P	42	O	
OUT5_N	41	O	
OUT6_P	45	O	
OUT6_N	44	O	
OUT7_P	48	O	
OUT7_N	47	O	

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LOGIC CONTROL / STATUS (2)(3)			
HW_SW_CTRL	9	I	**Device Start-Up Mode Select** (3-level, 1.8-V compatible). This input selects the device start-up mode that determines the memory page used to initialize the registers, serial interface, and logic pin functions. The input level is sampled only at device power-on reset (POR). See Table 1 for start-up mode descriptions and logic pin functions.
PDN	13	I	**Device Power-Down** (active low). When PDN is pulled low, the device is in hard-reset and all blocks including the serial interface are powered down. When PDN is pulled high, the device is started according to device mode selected by HW_SW_CTRL and begins normal operation with all internal circuits reset to their initial state.
SDA/SDI	25	I/O	**I^2C Serial Data I/O (SDA) or SPI Serial Data Input (SDI).** See Table 1. When HW_SW_CTRL is 0 or 1, the serial interface is I^2C. SDA and SCL pins (open drain) require external I^2C pullup resistors. The default 7-bit I^2C address is 11001xxb, where the MSB bits (11001b) are initialized from on-chip EEPROM and the LSB bits (xxb) are determined by the logic input pins. When HW_SW_CTRL is 0, the LSBs are determined by the GPIO1 input state (3-level) during POR. When HW_SW_CTRL is 1, the LSBs are fixed to 00b. When HW_SW_CTRL is Float, the serial interface is SPI (4-wire, Mode 0) using the SDI, SCK, SCS, and SDO pins.
SCL/SCK	26	I	**I^2C Serial Clock Input (SCL) or SPI Serial Clock Input (SCK).** See Table 1.
GPIO0/SYNCN	12	I	**Multifunction Inputs or Outputs.** See Table 1.
GPIO1/SCS	24	I	
GPIO2/SDO/ FINC	30	I/O	
STATUS0	1	I/O	**Status Outputs 0 and 1.** Each output has programmable status signal selection, driver type (3.3-V LVCMOS or open-drain), and status polarity. Open-drain requires an external pullup resistor. Leave pin floating if unused. In I^2C mode, the STATUS1/FDEC pin can function as a DCO mode control input pin. See Table 1.
STATUS1/ FDEC	2	I/O	
REFSEL	8	I	**Manual DPLL Reference Clock Input Selection.** (3-level, 1.8-V compatible). REFSEL = 0 (PRIREF), 1 (SECREF), or Float or V_{IM} (Auto Select). This control pin must be enabled by register default or programming. Leave pin floating if unused.

(2) Internal resistors: PDN pin has 200-kΩ pullup to VDD_IN. HW_SW_CTRL, GPIO, REFSEL, and STATUS pins each have a 150-kΩ bias to V_{IM} (approximately 0.8 V) when PDN = 0 or 400-kΩ pulldown when PDN = 1.
(3) Unless otherwise noted: Logic inputs are 2-level, 1.8-V compatible inputs. Logic outputs are 3.3-V LVCMOS levels.

6.1 Device Start-Up Modes

The HW_SW_CTRL input pin selects the device start-up mode that determines the memory page (EEPROM or ROM) used to initialize the registers, the serial interface, and the logic pin functions at power-on reset. The initial register settings determine the device's frequency configuration on start-up. After start-up, the device registers can be accessed through the serial interface for device monitoring and programming, and the logic pins will function as defined by the selected mode.

Table 1. Device Start-Up Modes

HW_SW_CTRL INPUT LEVEL(1)	START-UP MODE	MODE DESCRIPTION
0	EEPROM + I^2C (Soft pin mode)	Registers are initialized from EEPROM, and I^2C interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: I^2C Data, I^2C Clock (open drain) • **GPIO0/SYNCN**: Output SYNC Input (active low). Pull up externally if not used. • **GPIO1/SCS**(1): I^2C Address LSB Select (Low = 00b, Float = 01b, High = 10b) • **GPIO2/SDO/FINC**(2): DPLL DCO Frequency Increment (active high) • **STATUS1/FDEC**(2): DPLL DCO Frequency Decrement (active high), or Status output
Float (V_{IM})	EEPROM + SPI (Soft pin mode)	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: SPI Data In (SDI), SPI Clock (SCK) • **GPIO0/SYNCN**: Output SYNC Input (active low). Pull up externally if not used. • **GPIO1/SCS**: SPI Chip Select (SCS) • **GPIO2/SDO/FINC**: SPI Data Out (SDO)
1	ROM + I^2C (Hard pin mode)	Registers are initialized from the ROM page selected by GPIO pins, and I^2C interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: I^2C Data, I^2C Clock (open drain) • **GPIO[2:0]** (1): ROM Page Select Inputs (000b to 111b) during POR. • After POR, GPIO2/SDO/FINC and STATUS1/FDEC pins can function the same as for HW_SW_CTRL = 0.

(1) The input levels on these pins are sampled only during POR.
(2) FINC and FDEC pins are only available when DCO mode and GPIO pin control are enabled by registers.

NOTE

To ensure proper start-up into EEPROM + SPI Mode, the HW_SW_CTRL, STATUS0, and STATUS1 pins must all be floating or biased to V_{IM} (0.8-V typical) before the PDN pin is pulled high. These three pins momentarily operate as 3-level inputs and get sampled at the low-to-high transition of PDN to determine the device start-up mode during POR. If any of these pins are connected to a system host (MCU or FPGA), TI recommends using external biasing resistors on each pin (10-kΩ pullup to 3.3 V with 3.3-kΩ pulldown to GND) to set the inputs to V_{IM} during POR. After power-up, the STATUS pins can operate as LVCMOS outputs to overdrive the external resistor bias for normal status operation.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD(2)	Core supply voltages	-0.3	3.6	V
VDDO(3)	Output supply voltages	-0.3	3.6	V
V_{IN}	Input voltage range for clock and logic inputs	-0.3	VDD+0.3	V
V_{OUT_LOGIC}	Output voltage range for logic outputs	-0.3	VDD+0.3	V
V_{OUT}	Output voltage range for clock outputs	-0.3	VDDO+0.3	V
T_J	Junction temperature		150	°C
Tstg	Storage temperture range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before the PDN is pulled high to trigger the internal power-on reset (POR).
(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	Core supply voltages	3.135	3.3	3.465	V
VDDO_x(2)	Output supply voltage for AC-LVDS/CML/LVPECL or HCSL driver	1.71	1.8, 2.5, 3.3	3.465	V
VDDO_x(2)	Output supply voltage for 1.8-V LVCMOS driver(3)	1.71	1.8	1.89	V
V_{IN}	Input voltage range for clock and logic inputs	0		3.465	V
T_J	Junction temperature			135	°C
t_{VDD}	Power supply ramp time(4)	0.01		100	ms
n_{EEcyc}	EEPROM program cycles(5)			100	cycles

(1) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).
(2) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.
(3) The LVCMOS driver supports full rail-to-rail swing when VDDO_x is 1.8 V ±5%. When VDDO_x is 2.5 V or 3.3 V, the LVCMOS driver will not fully swing to the positive rail due to the dropout voltage of the output channel's internal LDO regulator.
(4) Time for VDD to ramp monotonically above 2.7 V for proper internal power-on reset. For slower or non-monotonic VDD ramp, hold PDN low until after VDD voltages are valid.
(5) n_{EEcyc} specifies the maximum EEPROM program cycles allowed for customer programming. The initial count of factory-programmed cycles is non-zero due to production tests, but factory-programmed cycles are excluded from the n_{EEcyc} limit. The total number of EEPROM program cycles can be read from the 8-bit NVM count status register (NVMCNT), which automatically increments by 1 on each successful programming cycle. TI does not ensure EEPROM endurance if the n_{EEcyc} limit is exceeded by the customer.

7.4 Thermal Information: 4-Layer JEDEC Standard PCB

THERMAL METRIC(1) (2) (3)		LMK05318 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal information is based on a 4-layer JEDEC standard board with 25 thermal vias (5 x 5 pattern, 0.3 mm holes).
(3) Ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of Ψ_{JB} is defined by JESD51-6.

7.5 Thermal Information: 10-Layer Custom PCB

THERMAL METRIC(1) (2) (3)		LMK05318 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	9.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal information is based on a 10-layer 200 mm x 250 mm x 1.6 mm board with 25 thermal vias (5 x 5 pattern, 0.3 mm holes).
(3) Ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of Ψ_{JB} is defined by JESD51-6.

7.6 Electrical Characteristics

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_DIG	Core Current Consumption (VDD_DIG)			18		mA
IDD_IN	Core Current Consumption (VDD_IN)			38		mA
IDD_PLL1	Core Current Consumption (VDD_PLL1)	DPLL and APLL1 enabled		110		mA
IDD_XO	Core Current Consumption (VDD_XO)			20		mA
IDD_PLL2	Core Current Consumption (VDD_PLL2)	APLL2 disabled		20		mA
		APLL2 enabled		120		mA

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDDO_x	Output Current Consumption, per channel(1) (VDDO_x)	Output mux and divider enabled, excludes driver(s) Divider value = 2 to 6		50		mA
		Output mux and divider enabled, excludes driver(s) Divider value > 6		70		mA
		AC-LVDS		11		mA
		AC-CML		14		mA
		AC-LVPECL		16		mA
		HCSL, 50-Ω load to GND		25		mA
		1.8-V LVCMOS (x2), 100 MHz		6		mA
IDD_{PDN}	Total Current Consumption (all VDD and VDDO pins, 3.3 V)	Device powered-down (PDN pin held low)		56		mA
XO INPUT CHARACTERISTICS (XO)						
f_{IN}	Input frequency range		10		100	MHz
V_{IN-SE}	Single-ended input voltage swing	LVCMOS input, DC-coupled to XO_P	1		2.6	Vpp
$V_{IN-DIFF}$	Differential input voltage swing(2)	Differential input	0.4		2	Vpp
V_{ID}	Differential input voltage swing(2)	Differential input	0.2		1	|V|
dV/dt	Input slew rate(3)		0.2	0.5		V/ns
IDC	Input duty cycle		40		60	%
I_{IN}	Input leakage	50-Ω and 100-Ω internal terminations disabled	-350		350	µA
REFERENCE INPUT CHARACTERISTICS (PRIREF, SECREF)						
f_{IN}	Input frequency range	Differential input(4)	5		800	MHz
f_{IN}	Input frequency range	LVCMOS input	1E-6		250	MHz
V_{IN-SE}	Single-ended input voltage swing	LVCMOS input, DC-coupled to xREF_P	1			Vpp
$V_{IN-DIFF}$	Differential input voltage swing(2)	Differential input	0.4		2	Vpp
V_{ID}	Differential input voltage swing(2)	Differential input	0.2		1	V
dV/dt	Input slew rate(3)		0.2	0.5		V/ns
I_{IN}	Input leakage	50-Ω and 100-Ω internal terminations disabled	-350		350	µA
VCO CHARACTERISTICS						
f_{VCO1}	VCO1 Frequency Range		2499.875	2500	2500.125	MHz
f_{VCO2}	VCO2 Frequency Range		5500		6250	MHz

(1) IDDO_x current for an operating output is the sum of mux, divider and an output format.
(2) Minimum limit applies for the minimum setting of the differential input amplitude monitor (xREF_LVL_SEL = 0).
(3) In order to meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
(4) For a differential input clock below 5 MHz, TI recommends to disable the differential input amplitude monitor and enable at least one other monitor (frequency, window detectors) to validate the input clock. Otherwise, consider using an LVCMOS clock for an input below 5 MHz.

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
APLL CHARACTERISTICS						
f_{PD1}	APLL1 Phase Detector Frequency		1		50	MHz
f_{PD2}	APLL2 Phase Detector Frequency		10		150	MHz
AC-LVDS OUTPUT CHARACTERISTICS (OUTx)						
f_{OUT}	Output frequency(5)				800	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})	f_{OUT} ≥ 25 MHz; TYP at 156.25 MHz	250	350	450	mV
$V_{OUT-DIFF}$	Differential output voltage swing, peak-to-peak			2×V_{OD}		Vpp
V_{OS}	Output common mode		100		430	mV
t_{SK}	Output-to-output skew	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(6)	20% to 80%, < 300 MHz		225	350	ps
		± 100 mV around center point, ≥ 300 MHz		85	250	ps
PN_{FLOOR}	Output phase noise floor	f_{OUT} = 156.25 MHz; f_{OFFSET} > 10 MHz		-160		dBc/Hz
ODC	Output duty cycle(7)		45		55	%
AC-CML OUTPUT CHARACTERISTICS (OUTx)						
f_{OUT}	Output frequency(5)				800	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})	TYP at f_{OUT} = 156.25 MHz	400	600	800	mV
$V_{OUT-DIFF}$	Differential output voltage swing, peak-to-peak			2×V_{OD}		Vpp
V_{OS}	Output common mode		150		550	mV
t_{SK}	Output-to-output skew	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(6)	20% to 80%, < 300 MHz		225	300	ps
		± 100 mV around center point, ≥ 300 MHz		50	150	ps
PN_{FLOOR}	Output phase noise floor	f_{OUT} = 156.25 MHz; f_{OFFSET} > 10 MHz		-160		dBc/Hz
ODC	Output duty cycle(7)		45		55	%
AC-LVPECL OUTPUT CHARACTERISTICS (OUTx)						
f_{OUT}	Output frequency(5)				800	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})	TYP at f_{OUT} = 156.25 MHz	500	800	1000	mV
$V_{OUT-DIFF}$	Differential output voltage swing, peak-to-peak			2×V_{OD}		Vpp
V_{OS}	Output common mode		300		700	mV
t_{SK}	Output-to-output skew	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(6)	20% to 80%, < 300 MHz		200	300	ps
		± 100 mV around center point, ≥ 300 MHz		35	100	ps
PN_{FLOOR}	Output phase noise floor	f_{OUT} = 156.25 MHz; f_{OFFSET} > 10 MHz		-162		dBc/Hz
ODC	Output duty cycle(7)		45		55	%

(5) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min specification.
(6) Measured on the differential output waveform (OUTx_P - OUTx_N).
(7) Parameter is specified for PLL outputs divided from either VCO domain.

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HCSL OUTPUT CHARACTERISTICS (OUTx)						
f_{OUT}	Output frequency (5)				400	MHz
V_{OH}	Output high voltage		600		880	mV
V_{OL}	Output low voltage		-150		150	mV
t_{SK}	Output-to-output skew	Same post divider, output divide values, and output type			100	ps
dV/dt	Output slew rate (6)	± 150 mV around center point	1		4	V/ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	100 MHz		-160		dBc/Hz
ODC	Output duty cycle (7)		45		55	%
1.8-V LVCMOS OUTPUT CHARACTERISTICS (OUT[4:7])						
f_{OUT}	Output frequency		1E-6		200	MHz
V_{OH}	Output high voltage	I_{OH} = 1 mA	1.2			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.4	V
I_{OH}	Output high current			-23		mA
I_{OL}	Output low current			20		mA
t_R/t_F	Output rise/fall time	20% to 80%		250		ps
t_{SK}	Output-to-output skew	Same post divider, output divide values, and output type			100	ps
t_{SK}	Output-to-output skew	Same post divider, output divide values, LVCMOS-to-DIFF			1.5	ns
PN_{FLOOR}	Output phase noise floor	f_{OUT} = 66.66 MHz; f_{OFFSET} > 10 MHz		-160		dBc/Hz
ODC	Output duty cycle (7)		45		55	%
R_{OUT}	Output impedance			50		Ω
3-LEVEL LOGIC INPUT CHARACTERISTICS (HW_SW_CTRL, GPIO1, REFSEL, STATUS[1:0])						
V_{IH}	Input high voltage		1.4			V
V_{IM}	Input mid voltage	Input floating with internal bias and PDN pulled low	0.7		0.9	V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	-40		40	µA
I_{IL}	Input low current	V_{IL} = GND	-40		40	µA
2-LEVEL LOGIC INPUT CHARACTERISTICS (PDN, GPIO[2:0], SDI, SCK, SCS)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	-40		40	µA
I_{IL}	Input low current	V_{IL} = GND	-40		40	µA
SR	Input Slew Rate		0.5			V/ns

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC OUTPUT CHARACTERISTICS (STATUS[1:0], SDO)						
V_{OH}	Output high voltage	I_{OH} = 1 mA	1.2			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.6	V
t_R/t_F	Output rise/fall time	20% to 80%, LVCMOS mode, 1 kΩ to GND		500		ps
SPI TIMING REQUIREMENTS (SDI, SCK, SCS, SDO)						
f_{SCK}	SPI clock rate				20	MHz
	SPI clock rate; NVM write				5	MHz
t_1	SCS to SCK setup time		10			ns
t_2	SDI to SCK setup time		10			ns
t_3	SDI to SCK hold time		10			ns
t_4	SCK high time		25			ns
t_5	SCK low time		25			ns
t_6	SCK to SDO valid read-back data				20	ns
t_7	SCS pulse width		20			ns
t_8	SDI to SCK hold time		10			ns
I^2C-COMPATIBLE INTERFACE CHARACTERISTICS (SDA, SCL)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.5	V
I_{IH}	Input leakage		-15		15	µA
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.3	V
f_{SCL}	I^2C clock rate	Standard			100	kHz
		Fast mode			400	
$t_{SU(START)}$	START condition setup time	SCL high before SDA low	0.6			µs
$t_{H(START)}$	START condition hold time	SCL low after SDA low	0.6			µs
$t_{W(SCLH)}$	SCL pulse width high		0.6			µs
$t_{W(SCLL)}$	SCL pulse width low		1.3			µs
$t_{SU(SDA)}$	SDA setup time		100			ns
$t_{H(SDA)}$	SDA hold time	SDA valid after SCL low	0		0.9	µs
$t_{R(IN)}$	SDA/SCL input rise time				300	ns
$t_{F(IN)}$	SDA/SCL input fall time				300	ns
$t_{F(OUT)}$	SDA output fall time	C_{BUS} ≤ 400 pF			300	ns
$t_{SU(STOP)}$	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY NOISE REJECTION (PSNR) / CROSSTALK SPURS						
PSNR	Spur induced by power supply noise (V_N = 50 mVpp) (8) (9)	V_{DD} = 3.3 V, V_{DDO_x} = 3.3 V, 156.25 MHz, AC-DIFF output		–83		dBc
		V_{DD} = 3.3 V, V_{DDO_x} = 3.3 V, 156.25 MHz, HCSL output		–78		dBc
PSNR	Spur induced by power supply noise (V_N = 25 mVpp)(8) (9)	V_{DD} = 3.3 V, V_{DDO_x} = 1.8 V, 156.25 MHz, AC-DIFF output		–63		dBc
		V_{DD} = 3.3 V, V_{DDO_x} = 1.8 V, 156.25 MHz, HCSL output		–58		dBc
		V_{DD} = 3.3 V, V_{DDO_x} = 1.8 V, 156.25 MHz, LVCMOS output		–45		dBc
$SPUR_{XTALK}$	Spur level due to output-to-output crosstalk (adjacent channels)(9)	f_{OUTx} = 156.25 MHz, f_{OUTy} = 155.52 MHz, AC-LVPECL		–75		dBc
SPUR	Highest spur level within 12 kHz to 40 MHz band (excludes output crosstalk and integer-boundary spurs)(9)	f_{VCO1} = 2500 MHz, f_{VCO2} = 6065.28 MHz, f_{OUTx} = 156.25 MHz, f_{OUTy} = 155.52 MHz, AC-LVPECL		–80		dBc
PLL CLOCK OUTPUT PERFORMANCE CHARACTERISTICS						
RJ	RMS Phase Jitter (12 kHz to 20 MHz), including spurs(10)	312.5 MHz AC-DIFF output from APLL1, f_{XO} = 48.0048 MHz, f_{PD1} = f_{XO}/2, f_{VCO1} = 2.5 GHz		50	100	fs RMS
RJ	RMS Phase Jitter (12 kHz to 20 MHz), including spurs(10)	156.25 MHz AC-DIFF output from APLL1, f_{XO} = 48.0048 MHz, f_{PD1} = f_{XO}/2, f_{VCO1} = 2.5 GHz		60	100	fs RMS
RJ	RMS Phase Jitter (12 kHz to 20 MHz), including spurs(10)	153.6 MHz AC-DIFF output from APLL2, f_{XO} = 48.0048 MHz, f_{PD1} = f_{XO}/2, f_{VCO1} = 2.5 GHz, f_{PD2} = f_{VCO1}/18, f_{VCO2} = 5.5296 GHz		125	250	fs RMS
RJ	RMS Phase Jitter (12 kHz to 20 MHz), including spurs(10)	155.52 MHz AC-DIFF output from APLL2, f_{XO} = 48.0048 MHz, f_{PD1} = f_{XO}/2, f_{VCO1} = 2.5 GHz, f_{PD2} = f_{VCO1}/18, f_{VCO2} = 5.59872 GHz		125	250	fs RMS
BW	DPLL bandwidth range(11)	Programmed bandwidth setting	0.01		4000	Hz
J_{PK}	DPLL closed-loop jitter peaking(12)	f_{REF} = 25 MHz, f_{OUT} = 10 MHz, DPLL BW = 0.1 Hz or 10 Hz		0.1		dB
J_{TOL}	Jitter tolerance	Jitter modulation = 10 Hz, 25.78125 Gbps		6455		UI p-p
$t_{HITLESS}$	Phase hit between two reference inputs with 0 ppm error	Valid for a single switchover event between two clock inputs at the same frequency		± 50		ps
$f_{HITLESS}$	Frequency transient during hitless switch	Valid for a single switchover event between two clock inputs at the same frequency		± 10		ppb

(8) PSNR is the single-sideband spur level (in dBc) measured when sinusoidal noise with ampitude V_N and frequency f_N (between 100 kHz and 1 MHz) is injected onto VDD and VDDO_x pins.
(9) DJ_{SPUR} (ps pk-pk) = [2 × $10^{(dBc/20)}$ / (π × f_{OUT}) × 1E6], where dBc is the PSNR or SPUR level (in dBc) and f_{OUT} is the output frequency (in MHz).
(10) Excluding output coupling spurs
(11) Actual loop bandwidth may be lower. The valid loop bandwidth range may be constrained by the DPLL TDC frequency used in a given configuration.
(12) DPLL closed-loop jitter peaking of 0.1 dB or less is based on the DPLL bandwidth setting configured by the TICS Pro software tool.

7.7 Timing Diagrams

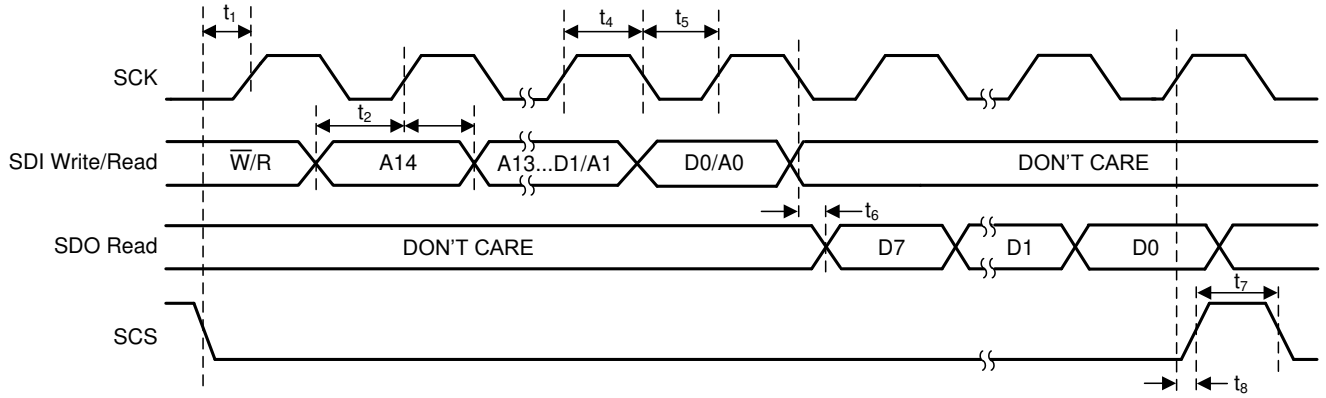


図 2. SPI Timing Parameters

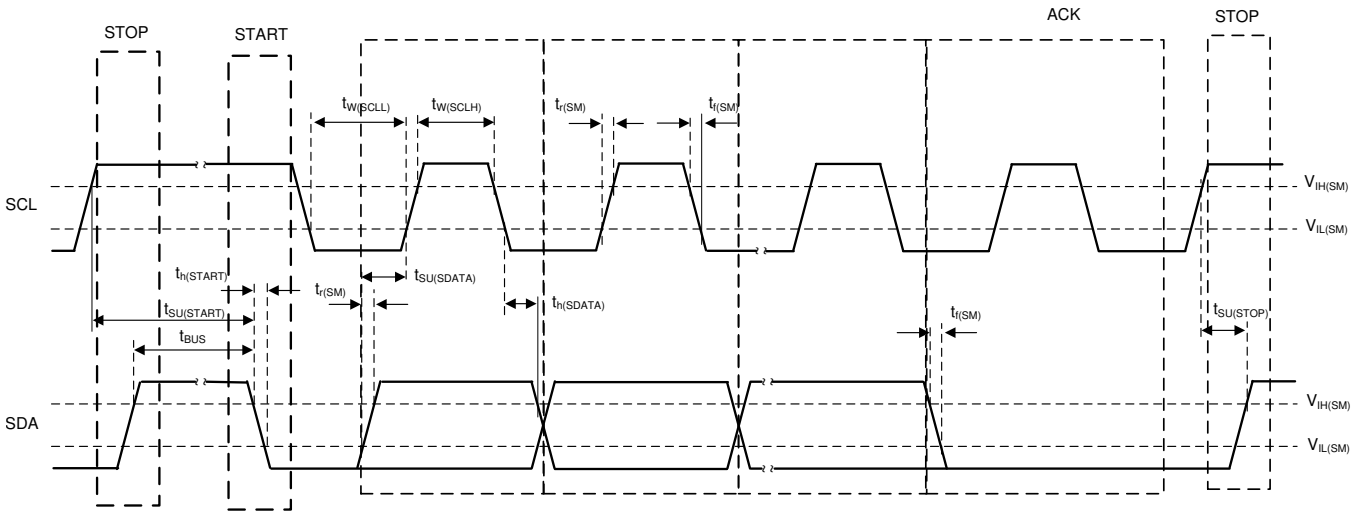


図 3. I²C Timing Diagram

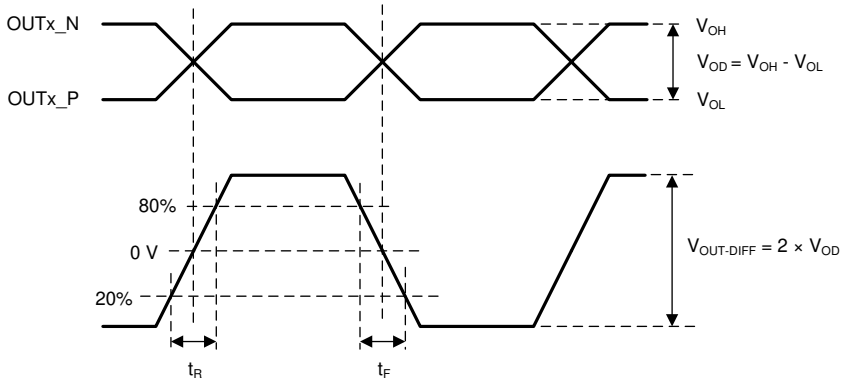


図 4. Differential Output Voltage and Rise/Fall Time

Timing Diagrams (continued)

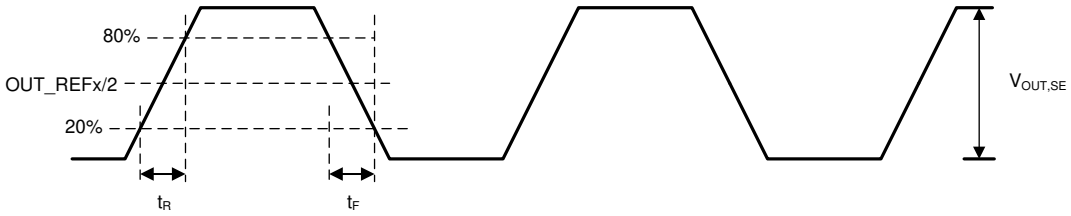


図 5. Single-Ended Output Voltage and Rise/Fall Time

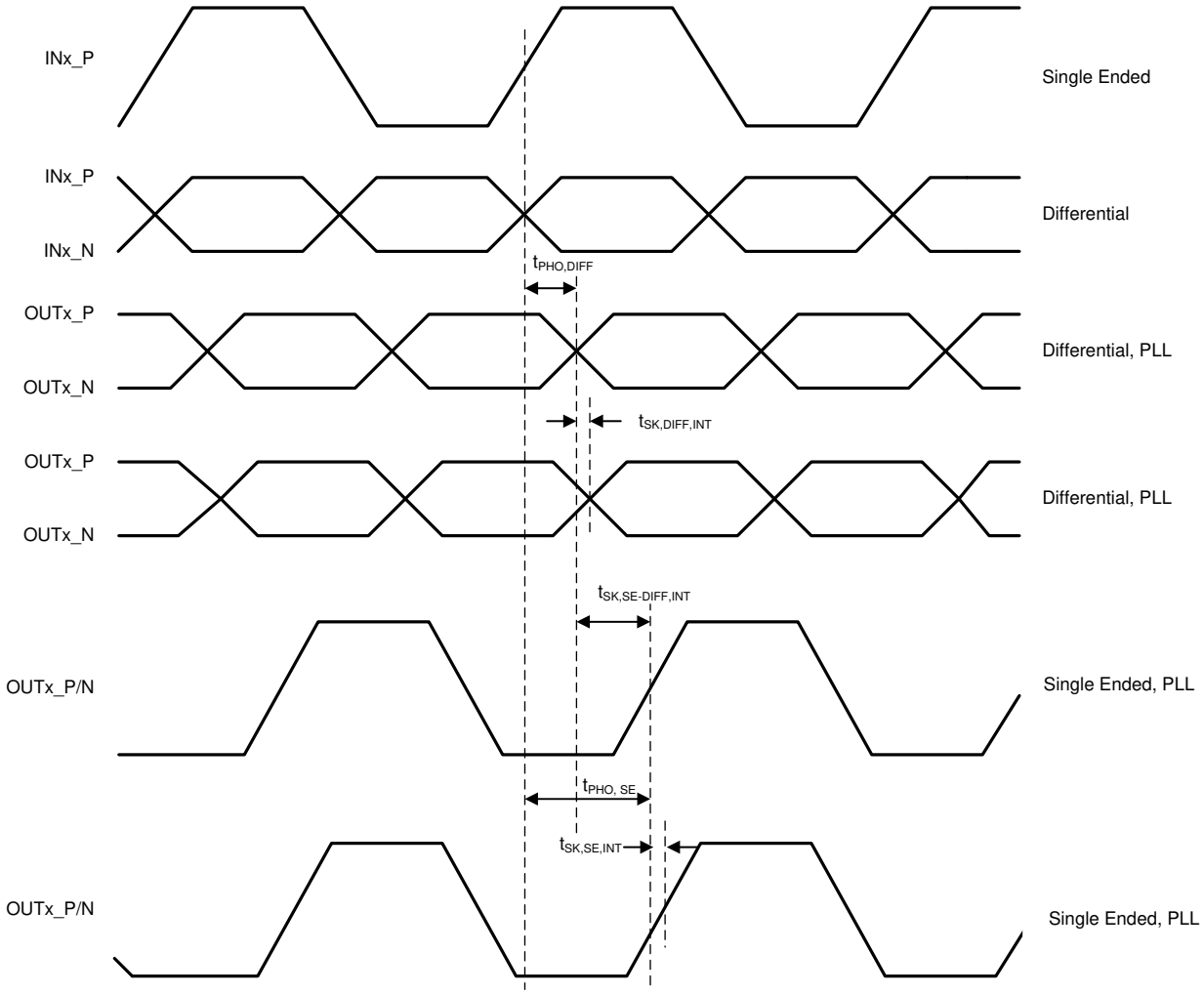


図 6. Differential and Single-Ended Output Skew and Phase Offset

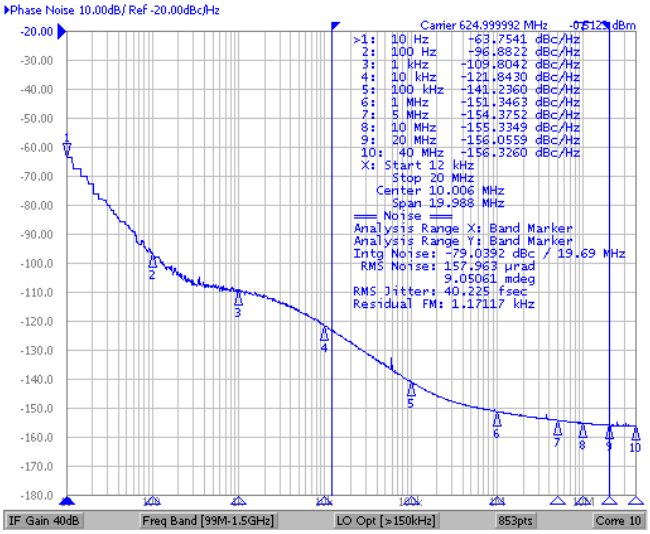
7.8 Typical Characteristics

Unless otherwise noted: VDD = 3.3 V, VDDO = 1.8 V, T_A = 25 °C, AC-LVPECL output measured.

DPLL: f_{REF} = 25 MHz, f_{TDC} = 25 MHz, BW_{DPLL} = 10 Hz, DPLL locked to reference.

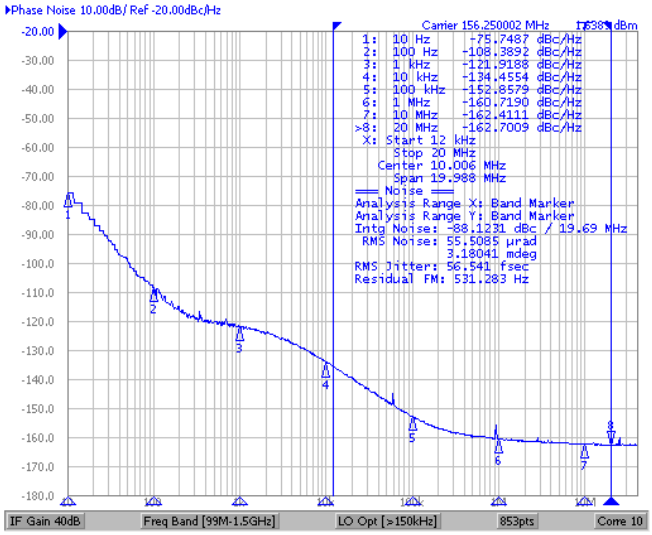
APLL1: f_{XO} = 48.0048 MHz, f_{PD1} = 24.0024 MHz (f_{XO}÷2), f_{VCO1} = 2500 MHz, BW_{APLL1} = 2.5 kHz, DPLL mode.

APLL2: f_{PD2} = 138.$\overline{8}$ MHz (f_{VCO1}÷18), BW_{APLL2} = 500 kHz, Cascaded APLL2 mode for 図 11 and 図 12.



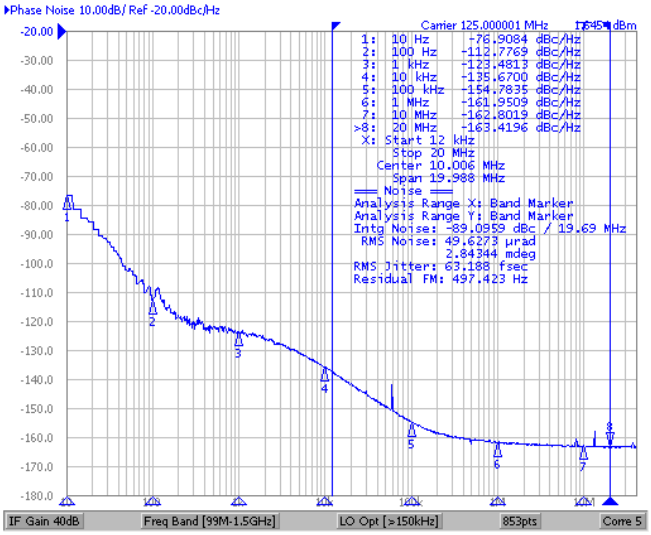
Jitter = 40 fs RMS (12 kHz to 20 MHz)
DPLL Mode (APLL2 Disabled)

図 7. 625-MHz Output Phase Noise (APLL1)



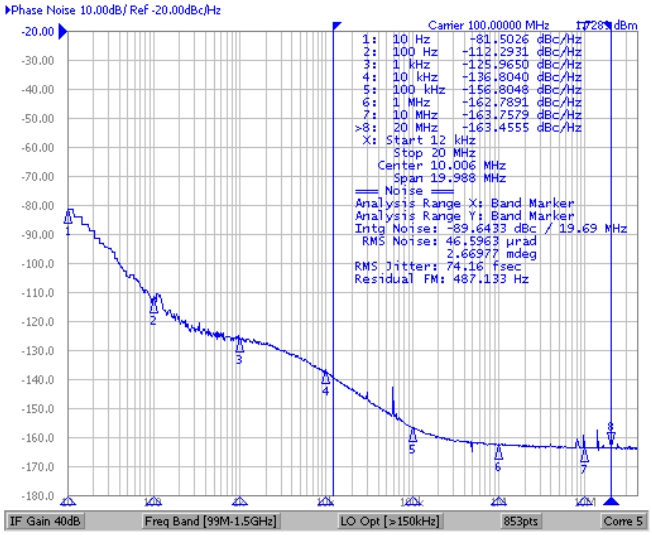
Jitter = 56 fs RMS (12 kHz to 20 MHz)
DPLL Mode (APLL2 Disabled)

図 8. 156.25-MHz Output Phase Noise (APLL1)



Jitter = 63 fs RMS (12 kHz to 20 MHz)
DPLL Mode (APLL2 Disabled)

図 9. 125-MHz Output Phase Noise (APLL1)

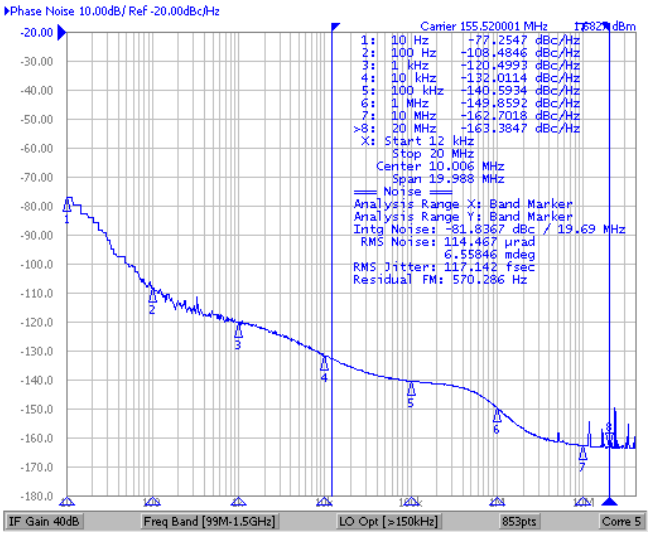


Jitter = 74 fs RMS (12 kHz to 20 MHz)
DPLL Mode (APLL2 Disabled)

図 10. 100-MHz Output Phase Noise (APLL1)

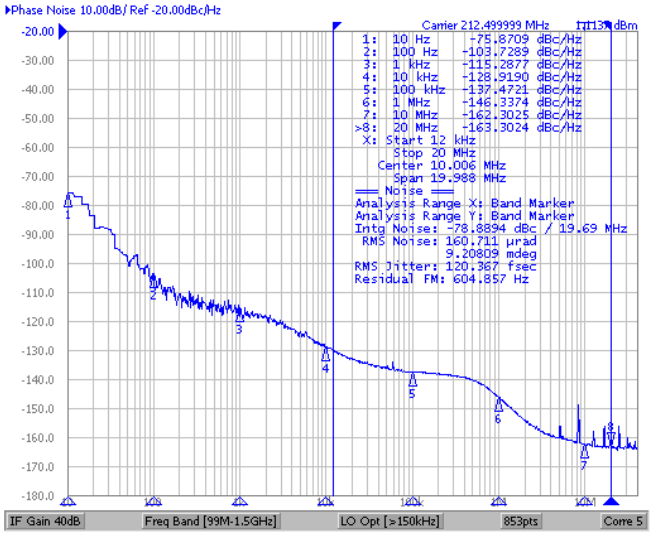
Typical Characteristics (continued)

APLL2: f_{PD2} = 138.$\overline{8}$ MHz (f_{VCO1}÷18), BW_{APLL2} = 500 kHz, Cascaded APLL2 mode for 図 11 and 図 12.



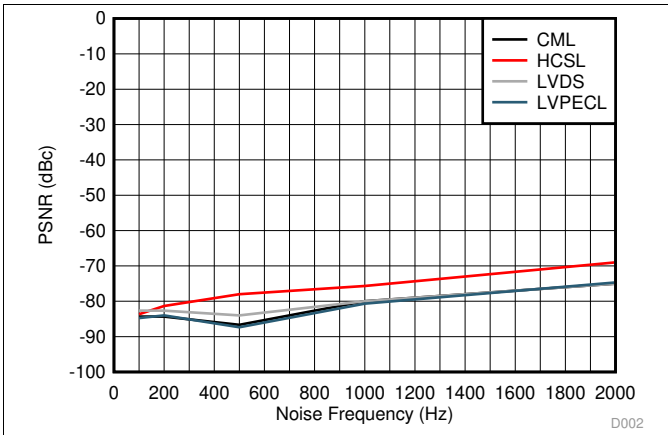
Jitter = 117 fs RMS (12 kHz to 20 MHz)
DPLL Mode With Cascaded APLL2
f_{VCO2} = 5598.72 MHz

図 11. 155.52-MHz Output Phase Noise (APLL2)



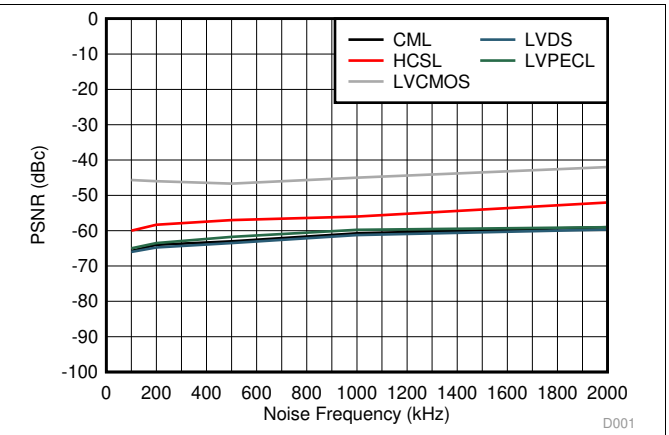
Jitter = 120 fs RMS (12 kHz to 20 MHz)
DPLL Mode With Cascaded APLL2
f_{VCO2} = 5737.5 MHz

図 12. 212.5-MHz Output Phase Noise (APLL2)



50-mVpp noise injected onto supplies (VDD = 3.3 V, VDDO = 3.3 V)

図 13. PSNR vs. Noise Frequency (50 mVpp) For 156.25-MHz Output



25-mVpp noise injected onto supplies (VDD = 3.3 V, VDDO = 1.8 V)

図 14. PSNR vs. Noise Frequency (25 mVpp) For 156.25-MHz Output (1)

(1) DJ_{SPUR} (ps pk-pk) = 2 × $10^{(dBc/20)}$ / (π × f_{OUT}) × 1E6, where dBc is the PSNR spur level (in dBc) and f_{OUT} is the output frequency (in MHz).

8 Parameter Measurement Information

8.1 Output Clock Test Configurations

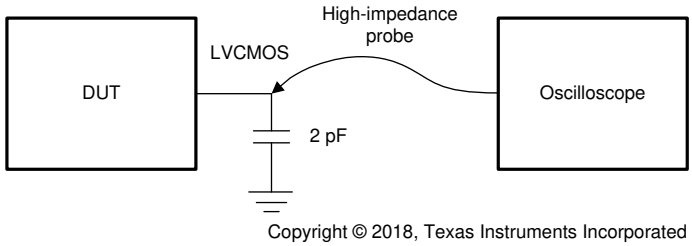


図 15. LVCMOS Output Test Configuration

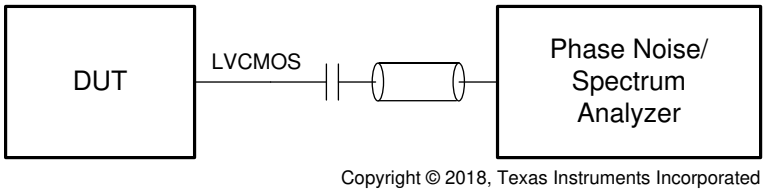


図 16. LVCMOS Output Phase Noise Test Configuration

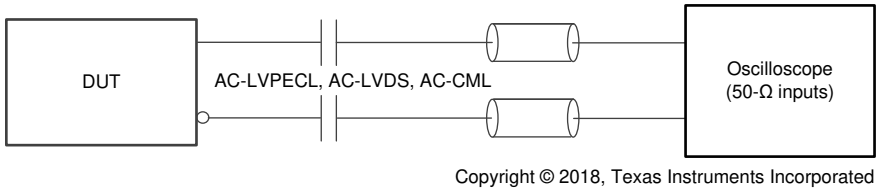


図 17. AC-LVPECL, AC-LVDS, AC-CML Output AC Test Configuration

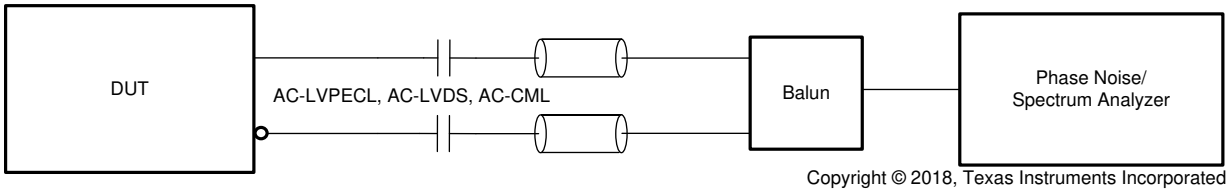


図 18. AC-LVPECL, AC-LVDS, AC-CML Output Phase Noise Test Configuration

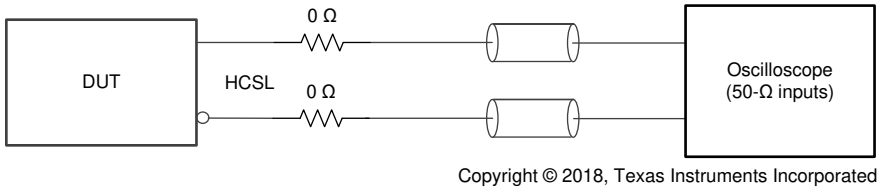


図 19. HCSL Output Test Configuration

Output Clock Test Configurations (continued)

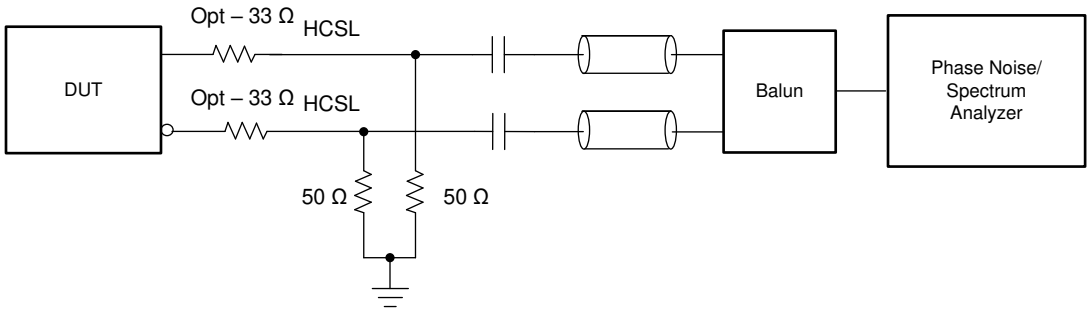
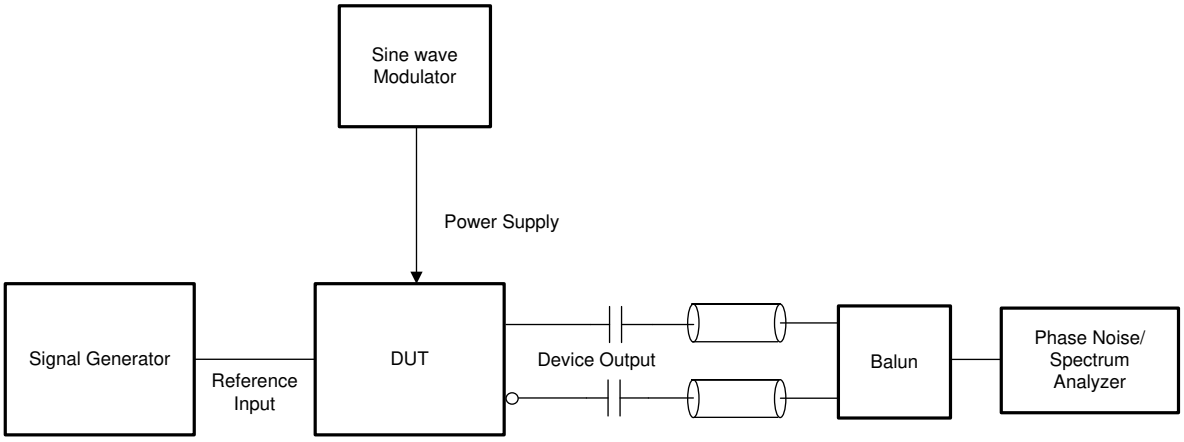


図 20. HCSL Output Phase Noise Test Configuration



Single-sideband spur level measured in dBc with a known noise amplitude and frequency injected onto the device power supply.

図 21. Power Supply Noise Rejection (PSNR) Test Configuration

9 Detailed Description

9.1 Overview

The LMK05318 has two reference inputs, one digital PLL (DPLL), two analog PLLs (APLLs) with integrated VCOs, and eight output clocks. with RMS phase jitter of 50-fs typical from APLL1 and 125-fs typical from APLL2. APLL1 uses an ultra-high performance BAW VCO (VCO1) with a very high quality factor, and thus has no dependency on the phase noise or frequency of the external oscillator (XO) input clock. This minimizes the overall solution cost and allows the use of an off-the-shelf XO, TCXO, or OCXO selected to meet the free-run and holdover frequency stability requirements of the application. APLL1 is cascaded with the DPLL, allowing the APLL1 domain to be locked to the DPLL reference input for synchronous clock generation. APLL2 can be used to generate unrelated clock frequencies either locked to the APLL1 domain or the free-running XO input.

The DPLL reference input mux supports automatic input selection or manual input selection through software or pin control. The device provides hitless switching with proprietary phase cancellation for superior phase transient performance (±50 ps typical). The reference clock input monitoring block monitors the clock inputs and will perform a hitless switchover or holdover when a loss of reference (LOR) is detected. A LOR condition can be detected upon any violation of the threshold limits set for the input monitors, which include amplitude, frequency, missing pulse, runt pulse, and 1-PPS (pulse-per-second) detectors. The threshold limits for each input detector can be set and enabled per clock input. The tuning word history monitor feature allows the initial output frequency accuracy upon entry into holdover to be determined by the historical average frequency when locked, minimizing the frequency and phase disturbance during a LOR condition.

The device has eight outputs with programmable drivers, allowing up to eight differential clocks, or a combination of differential clocks and up to four 1.8-V LVCMOS pairs (two outputs per pair). The output clocks can be selected from either APLL/VCO domain through the output muxes. The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. A 1-PPS output can be supported on Output 7 (OUT7). If needed, the user can enable the zero-delay mode (ZDM) synchronization to achieve deterministic phase alignment between an APLL1 clock on OUT7 and the selected reference input.

To support IEEE 1588 PTP slave clock or other clock steering applications, the DPLL also supports DCO mode with less than 0.001-ppb (part per billion) frequency resolution for precise frequency and phase adjustment through external software or pin control.

The device is fully programmable through I^2C or SPI and supports custom start-up frequency configuration with the internal EEPROM, which is factory pre-programmed and in-system programmable if needed. Internal LDO regulators provide excellent PSNR to reduce the cost and complexity of the power delivery network. The clock input and PLL monitoring status can be observed through the status pins and interrupt registers for full diagnostic capability.

9.1.1 ITU-T G.8262 (SyncE) Standards Compliance

The LMK05318 meets the applicable requirements of the ITU-T G.8262 (SyncE) standard. See the Application Report, *ITU-T G.8262 Compliance Test Result for the LMK05318* (SNAA316).

9.2 Functional Block Diagram

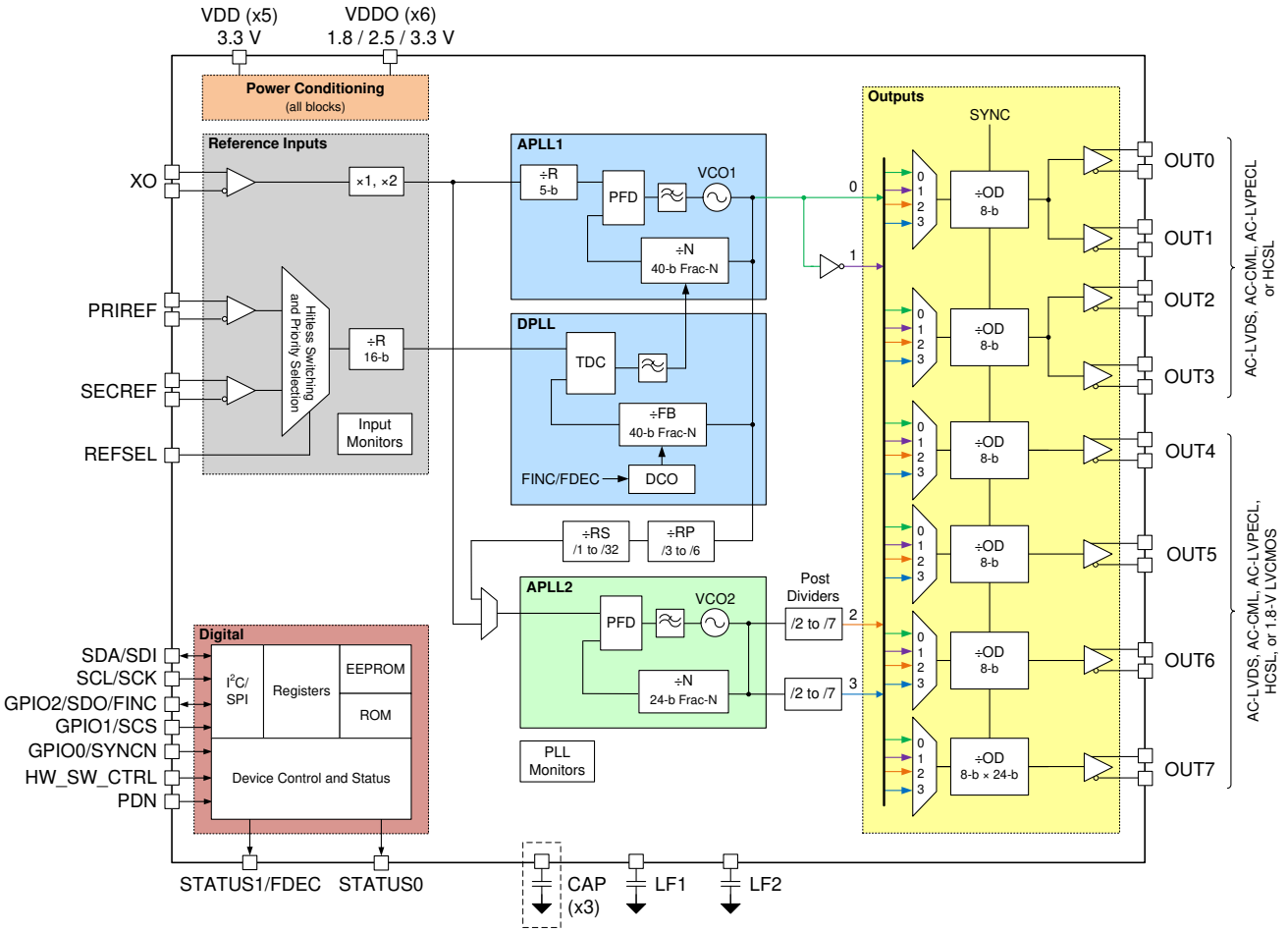


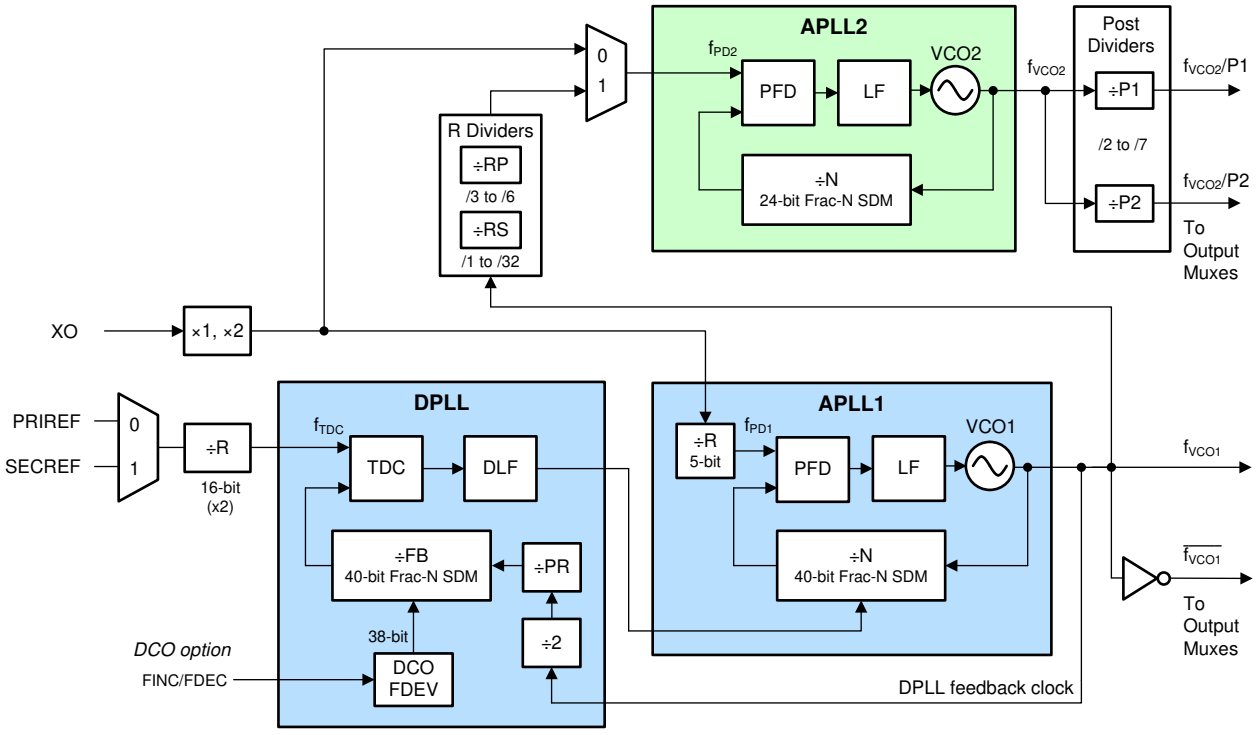
図 22. Top-Level Device Block Diagram

Functional Block Diagram (continued)

9.2.1 PLL Architecture Overview

図 23 shows the PLL architecture implemented in the LMK05318. The primary "PLL1" channel consists of a digital PLL (DPLL) and analog PLL (APLL1) with integrated BAW VCO (VCO1) capable of generating clocks with RMS phase jitter of 50-fs typical. A secondary APLL (APLL2) with integrated LC VCO (VCO2) can be used as an additional clock generation domain with RMS phase jitter of 125-fs typical.

The DPLL is comprised of a time-to-digital converter (TDC), digital loop filter (DLF), and 40-bit fractional feedback (FB) divider with sigma-delta-modulator (SDM). The APLLs are comprised of a reference (R) divider, phase-frequency detector (PFD), loop filter (LF), fractional feedback (N) divider with SDM, and VCO. APLL2 has a reference selection mux that allows APLL2 to be either locked to APLL1's VCO domain (Cascaded APLL2) or locked to the XO input (Non-Cascaded APLL2). Otherwise, APLL2 can be disabled (powered-down) if this clock domain is not needed. APLL1's VCO feeds the output clock distribution blocks directly, whereas APLL2's VCO drives the clock distribution blocks through its VCO post-dividers.



(1) DCO frequency adjustments can be software or pin controlled.

図 23. PLL Architecture

The following sections describe the basic principle of operation for DPLL mode and APLL-only mode. See PLL Operating Modes for more details on the PLL modes of operation including holdover.

9.2.2 DPLL Mode

In DPLL mode, the external XO input source determines the free-run and holdover frequency stability and accuracy of the output clocks. The BAW VCO1 determines the APLL1 output clock phase noise and jitter performance over the 12-kHz to 20-MHz integration band, regardless of the frequency and jitter of the XO input. This allows the use a cost-effective, low-frequency TCXO or OCXO as the external XO input to support standards-compliant frequency stability and low loop bandwidth (≤10 Hz) required in synchronization applications like SyncE and IEEE 1588.

Functional Block Diagram (continued)

The principle of operation for DPLL mode after power-on reset and initialization is as follows. If APLL2 is in cascaded mode as shown in 図 24, VCO1 is held at its nominal center frequency of 2.5 GHz while APLL2 locks. Then APLL1 locks the VCO1 frequency to the external XO input and operates in free-run mode. Once a valid DPLL reference input is detected, the DPLL begins lock acquisition. The DPLL TDC compares the phase of the selected reference input clock and the FB divider clock (from VCO1) and generates a digital correction word corresponding to the phase error. The correction word is filtered by the DLF, and the DLF output controls the APLL1 N divider SDM to pull the VCO1 frequency into lock with the reference input. VCO2 will track the VCO1 domain during DPLL lock acquisition and locked modes, allowing APLL2's clock domain to be synchronized to the DPLL reference input. Cascading APLL2 provides a high-frequency, ultra-low-jitter reference clock from VCO1 to minimize the APLL2 in-band phase noise/jitter impact that would otherwise occur if the APLL2's reference is from a XO/TCXO/OCXO with low frequency and/or high phase noise floor.

If APLL2 is not cascaded as shown in 図 25, VCO2 will lock to the XO input after initialization and operate independently of the DPLL/APLL1 domain.

When all reference inputs to the DPLL are lost, the PLLs will enter holdover mode and track the stability and accuracy of the external XO source.

If DCO mode is enabled on the DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the DPLL's FB divider SDM, where the frequency adjustment effectively propagates through the APLL1 domain (and APLL2 domain if cascaded) to the output clocks.

The programmed DPLL loop bandwidth (BW_{DPLL}) should be lower than all of the following:

1. 1/100th of the DPLL TDC rate
2. the APLL1 loop bandwidth (1 to 10 kHz typical)
3. the maximum DPLL bandwidth setting of 4 kHz.

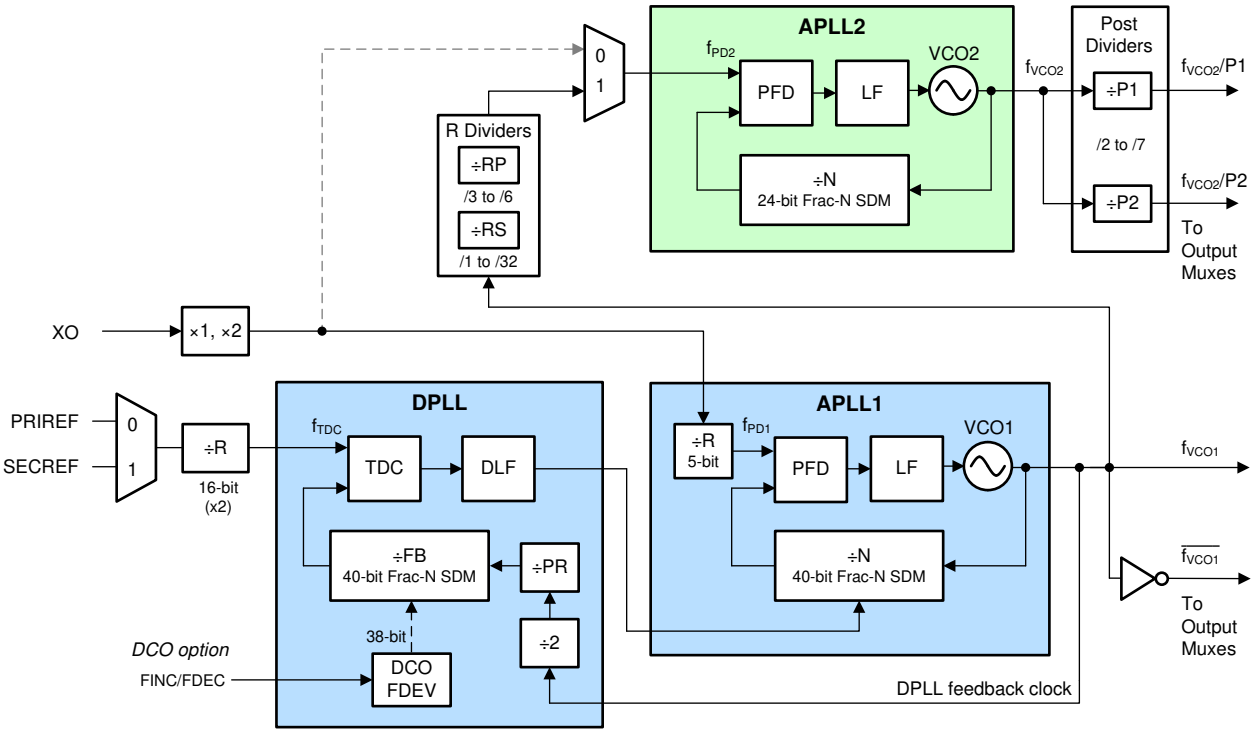


図 24. DPLL Mode With Cascaded APLL2

Functional Block Diagram (continued)

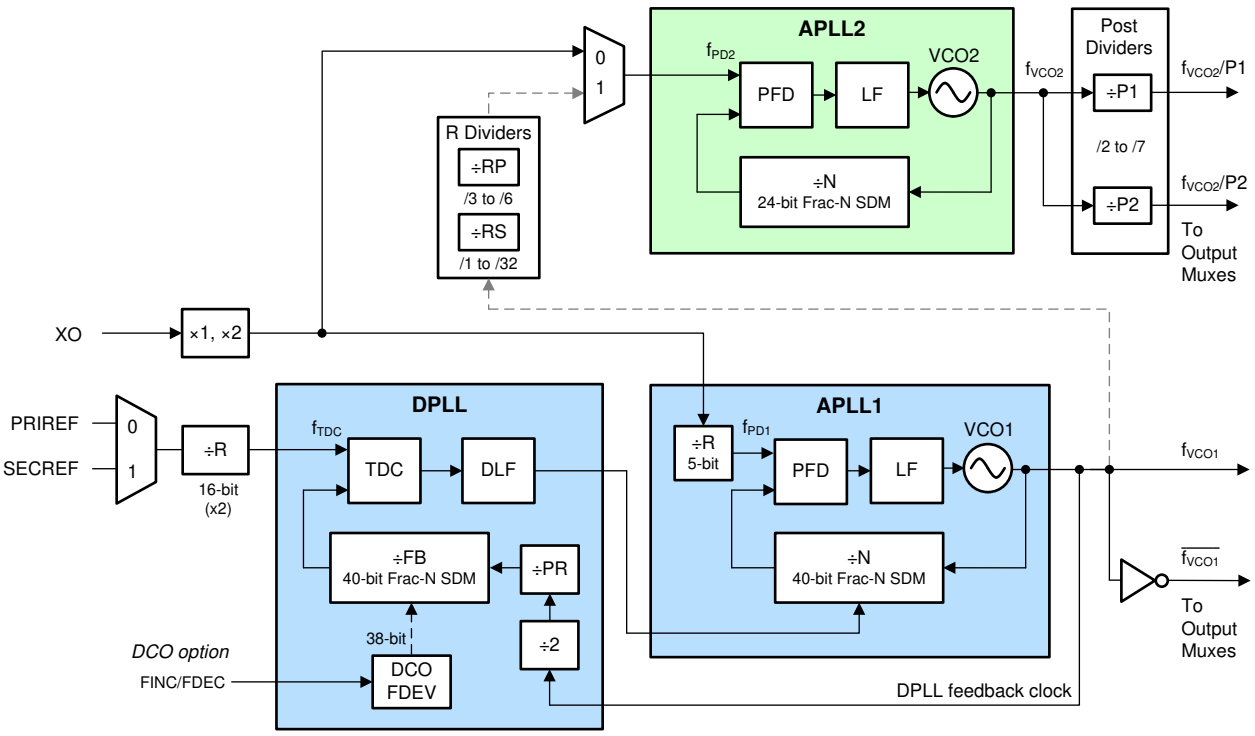


図 25. DPLL Mode With Non-Cascaded APLL2

Functional Block Diagram (continued)

9.2.3 APLL-Only Mode

In APLL-only mode, the external XO input source determines the free-run frequency stability and accuracy of the output clocks. The BAW VCO1 determines the APLL1 output clock phase noise and jitter performance over the 12-kHz to 20-MHz integration band, regardless of the frequency and jitter of the XO input.

The principle of operation for APLL-only mode after power-on reset and initialization is as follows. If APLL2 is in cascaded mode as shown in 図 26, VCO1 is held at its nominal center frequency of 2.5 GHz while APLL2 locks. Then APLL1 locks the VCO1 frequency to the external XO input and operates in free-run mode. The DPLL blocks are not used and do not affect the APLLs. VCO2 will track the VCO1 domain. Cascading APLL2 provides a high-frequency, ultra-low-jitter reference clock from VCO1 to minimize the APLL2 in-band phase noise/jitter impact that would occur otherwise if the APLL2's reference is from a XO/TCXO/OCXO with low frequency, high phase noise floor, or both.

If APLL2 is not cascaded as shown in 図 25, VCO2 will lock to the XO input after initialization and operate independent of the DPLL/APLL1 domain.

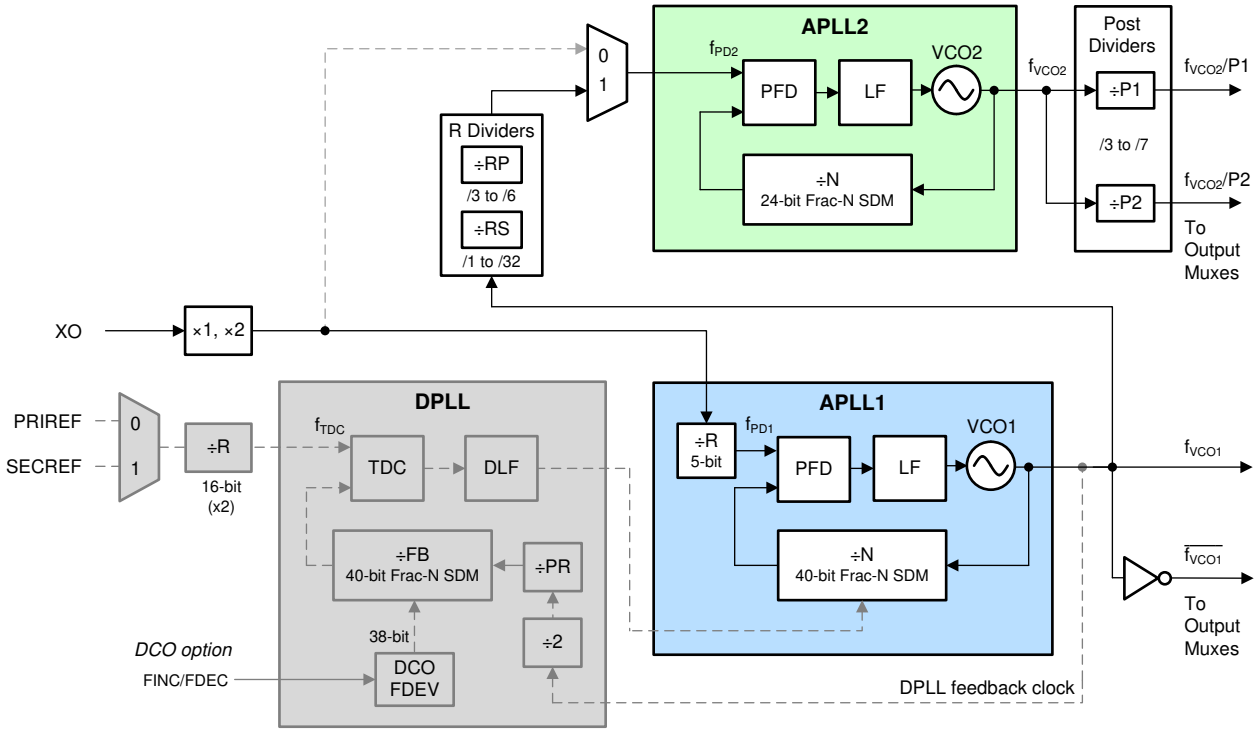


図 26. APLL-Only Mode With Cascaded APLL2

9.3 Feature Description

The following sections describe the features and functional blocks of the LMK05318.

9.3.1 Oscillator Input (XO_P/N)

The XO input is the reference clock for the fractional-N APLLs. The XO input determines the output frequency accuracy and stability in free-run or holdover modes.

For DPLL mode, the XO frequency must have a **non-integer relationship** with the VCO1 frequency so APLL1 can operate in fractional mode. For APLL-only mode, the XO frequency can have an integer or fractional relationship with the VCO1 and/or VCO2 frequencies.

Feature Description (continued)

In DPLL mode applications, such as SyncE and IEEE 1588, the XO input can be driven by a low-frequency TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability required by the applicable synchronization standard. TCXO and OCXO frequencies of 12.8, 19.2, 19.44, 24, 24.576, and 30.72 MHz are commonly available and cost-effective options that allow the APLL1 to operate in fractional mode for a VCO1 frequency of 2.5 GHz.

An XO/TCXO/OCXO source with low frequency or high phase jitter/noise floor will have no impact on the output jitter performance because the BAW VCO determines the jitter and phase noise over the 12-kHz to 20-MHz integration bandwidth.

The XO input buffer has programmable input on-chip termination and AC-coupled input biasing configurations as shown in 図 27. The buffered XO path also drives the input monitoring blocks.

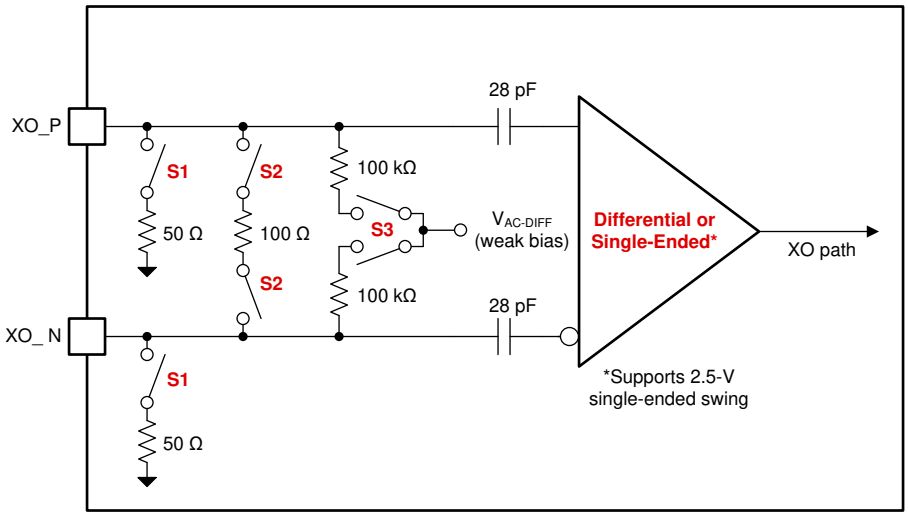


図 27. XO Input Buffer

表 2 lists the typical XO input buffer configurations for common clock interface types.

表 2. XO Input Buffer Modes

XO_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS	
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)
0h	LVDS, CML, LVPECL (DC-coupled)	OFF	OFF
1h	LVDS, CML, LVPECL (AC-coupled)	OFF	ON (1.3 V)
3h	LVDS, CML, LVPECL (AC-coupled, internal 100-Ω)	100 Ω	ON (1.3 V)
4h	HCSL (DC-coupled, internal 50-Ω)	50 Ω	OFF
8h	LVCMOS (DC-coupled)	OFF	OFF
Ch	Single-ended (DC-coupled, internal 50-Ω)	50 Ω	OFF

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.

9.3.2 Reference Inputs (PRIREF_P/N and SECREF_P/N)

The reference inputs (PRIREF and SECREF) can accept differential or single-ended clocks. Each input has programmable input type, termination, and AC-coupled input biasing configurations as shown in 図 28. Each input buffer drives the reference input mux of the DPLL block. The DPLL input mux can select from any of the reference inputs. The DPLL can switch between inputs with different frequencies provided they can be divided-down to a common frequency by DPLL R dividers. The reference input paths also drive the various detector blocks for reference input monitoring and validation.

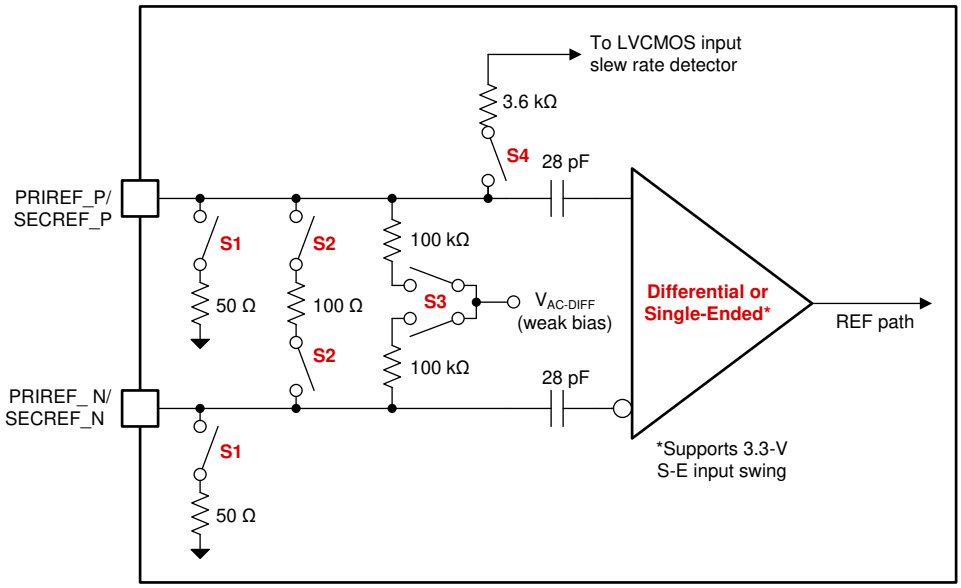


図 28. Reference Input Buffer

表 3 lists the reference input buffer configurations for common clock interface types.

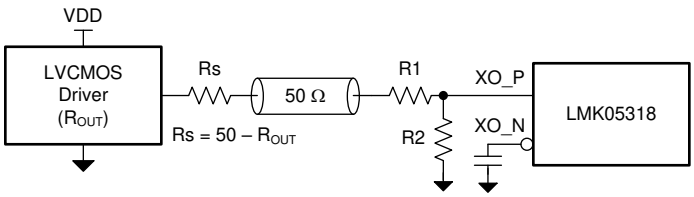
表 3. Reference Input Buffer Modes

REFx_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS		
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)	LVCMOS SLEW RATE DETECT (S4)(3)
0h	LVDS, CML, LVPECL (DC-coupled)	OFF	OFF	OFF
1h	LVDS, CML, LVPECL (AC-coupled)	OFF	ON (1.3 V)	OFF
3h	LVDS, CML, LVPECL (AC-coupled, internal 100-Ω)	100 Ω	ON (1.3 V)	OFF
4h	HCSL (DC-coupled, internal 50-Ω)	50 Ω	OFF	OFF
8h	LVCMOS (DC-coupled)	OFF	OFF	ON
Ch	Single-ended (DC-coupled, internal 50-Ω)	50 Ω	OFF	ON

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.
(3) S4: OFF = Differential input amplitude detector is used for all input types except LVCMOS or Single-ended.

9.3.3 Clock Input Interfacing and Termination

図 29 through 図 35 show the recommended input interfacing and termination circuits. Unused clock inputs can be left floating or pulled down.



VDD	R1 (Ω)	R2 (Ω)
3.3 V	125	375
2.5 V	0	open
1.8 V	0	open

図 29. Single-Ended LVCMOS to XO Input (XO_P)

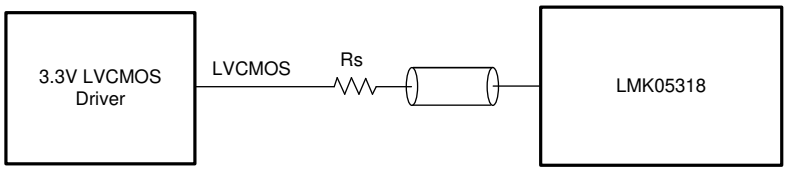


図 30. Single-Ended LVCMOS (1.8, 2.5, 3.3 V) to Reference (PRIREF_P/SECREF_P)

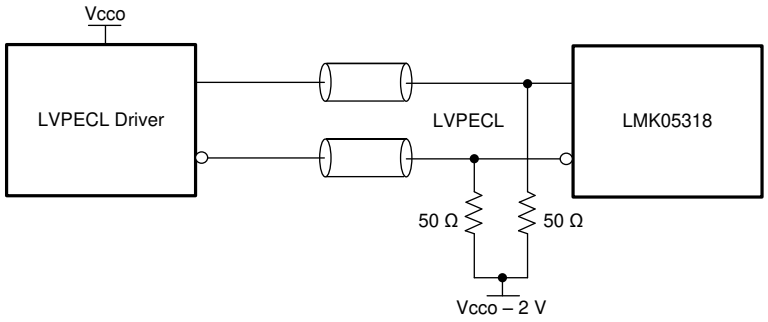


図 31. DC-Coupled LVPECL to Reference (PRIREF_P/SECREF_P) or XO Inputs

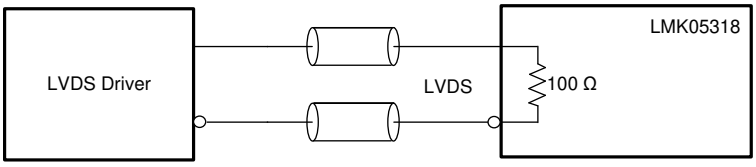


図 32. DC-Coupled LVDS to Reference (PRIREF/SECREF) or XO Inputs

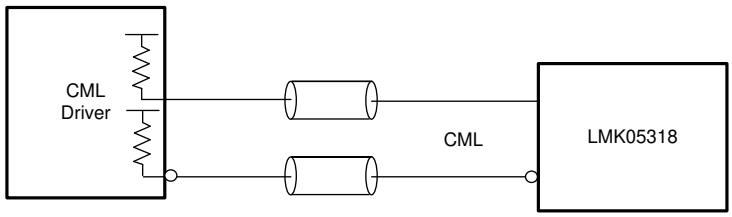


図 33. DC-Coupled CML (Source Terminated) to Reference (PRIREF/SECREF) or XO Inputs

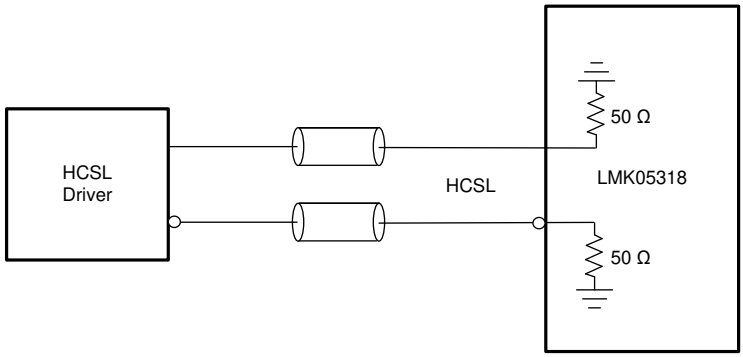


図 34. HCSL (Load Terminated) to Reference (PRIREF/SECREF) or XO Inputs

Driver	R_B (Ω)
LVDS	open
CML*	open
3.3-V LVPECL	150
2.5-V LVPECL	82
HCSL	50

*CML driver has 50-Ω pull-up

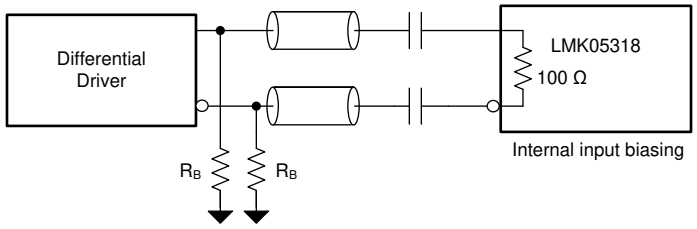


図 35. AC-Coupled Differential to Reference (PRIREF/SECREF) or XO Inputs

9.3.4 Reference Input Mux Selection

For the DPLL block, the reference input mux selection can be done automatically using an internal state machine with a configurable input priority scheme, or manually through software register control or hardware pin control. The input mux can select from PRIREF or SECREF. The priority for all inputs can be assigned through registers. The priority ranges from 0 to 2, where 0 = ignore (never select), 1 = first priority, and 2 = second priority. When both inputs are configured with the same priority setting, PRIREF will be given first priority. The selected input can be monitored through the status pins or register.

9.3.4.1 Automatic Input Selection

There are two automatic input selection modes that can be set by register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL will automatically switch over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input because valid, the DPLL will not switch-over until the currently selected input becomes invalid.

9.3.4.2 Manual Input Selection

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (see 表 4) or hardware pin control (see 表 5).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.

表 4. Manual Input Selection by Register Bits

DPLL_REF_MAN_REG_SEL BIT	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
0	0	PRIREF
1	0	SECREF

表 5. Manual Input Selection by Hardware Pins

REFSEL PIN	DPLL_REF_MAN_SEL BIT	SELECTED INPUT
0	1	PRIREF
Float (V_{IM})	1	Auto Select
1	1	SECREF

The reference input selection flowchart is shown in 図 36.

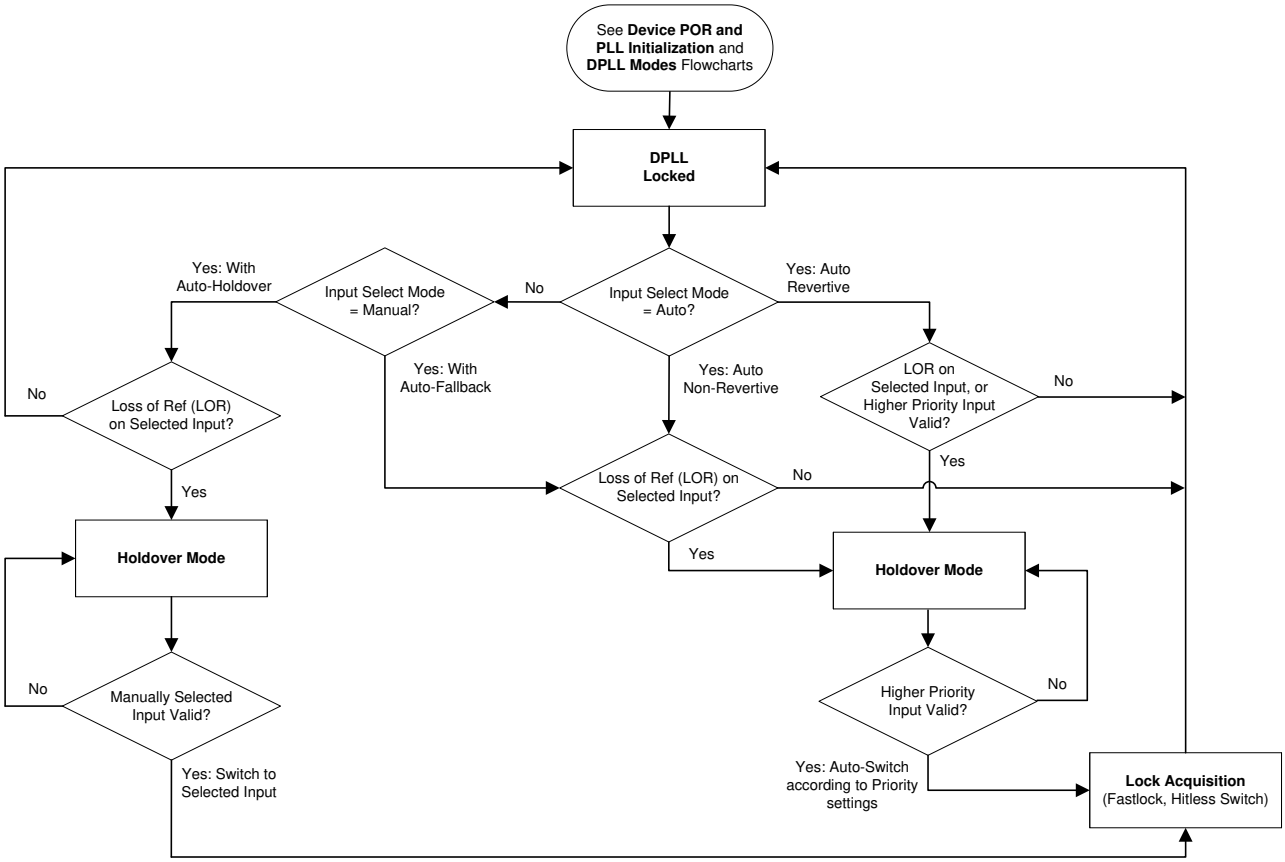


図 36. Reference Input Selection Flowchart

9.3.5 Hitless Switching

The DPLL supports hitless switching through TI's proprietary phase cancellation scheme. When hitless switching is enabled, it will prevent a phase transient (phase hit) from propagating to the outputs when the two switched inputs have a fixed phase offset and are frequency-locked. The inputs are frequency-locked when they have same exact frequency (0-ppm offset), or have frequencies that are integer-related and can each be divided to a common frequency by integers. When hitless switching is disabled, a phase hit equal to the phase offset between the two inputs will be propagated to the output at a rate determined by the DPLL fastlock bandwidth. The hitless switching specifications ($t_{HITLESS}$ and $f_{HITLESS}$) are valid for reference inputs with no wander. In the case where two inputs are switched but are not frequency-locked, the output smoothly transitions to the new frequency with reduced transient.

9.3.5.1 Hitless Switching With 1-PPS Inputs

Hitless switching between 1-PPS inputs is supported when zero-delay mode (ZDM) synchronization is disabled, but the switchover event should only occur after the DPLL has acquired lock. If a switchover occurs before the DPLL has locked initially, the switchover will not be hitless and the DPLL will take an indeterminate amount of time to lock. In this case, a soft-reset should be issued for the DPLL to lock to the selected input. In an application, the system host can monitor the DPLL lock status through a STATUS pin or bit to determine when the DPLL has locked before allowing a switchover between 1-PPS inputs. The DPLL lock time is governed by the DPLL bandwidth (typically 10 mHz for a 1-PPS input).

Hitless switching between 1-PPS inputs is not supported when ZDM synchronization is enabled.

9.3.6 Gapped Clock Support on Reference Inputs

The DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping severely increases the jitter of a clock, so the DPLL provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. The gapped clock width cannot be longer than the reference clock period after the R divider ($R_{PRI/SECREF}$ / $f_{PRI/SECREF}$). The reference input monitors should be configured to avoid any flags due to the worst-case clock gapping scenario to achieve and maintain lock. Reference switchover between two gapped clock inputs may violate the hitless switching specification if the switch occurs during a gap in either input clock.

9.3.7 Input Clock and PLL Monitoring, Status, and Interrupts

The following section describes the input clock and PLL monitoring, status, and interrupt features.

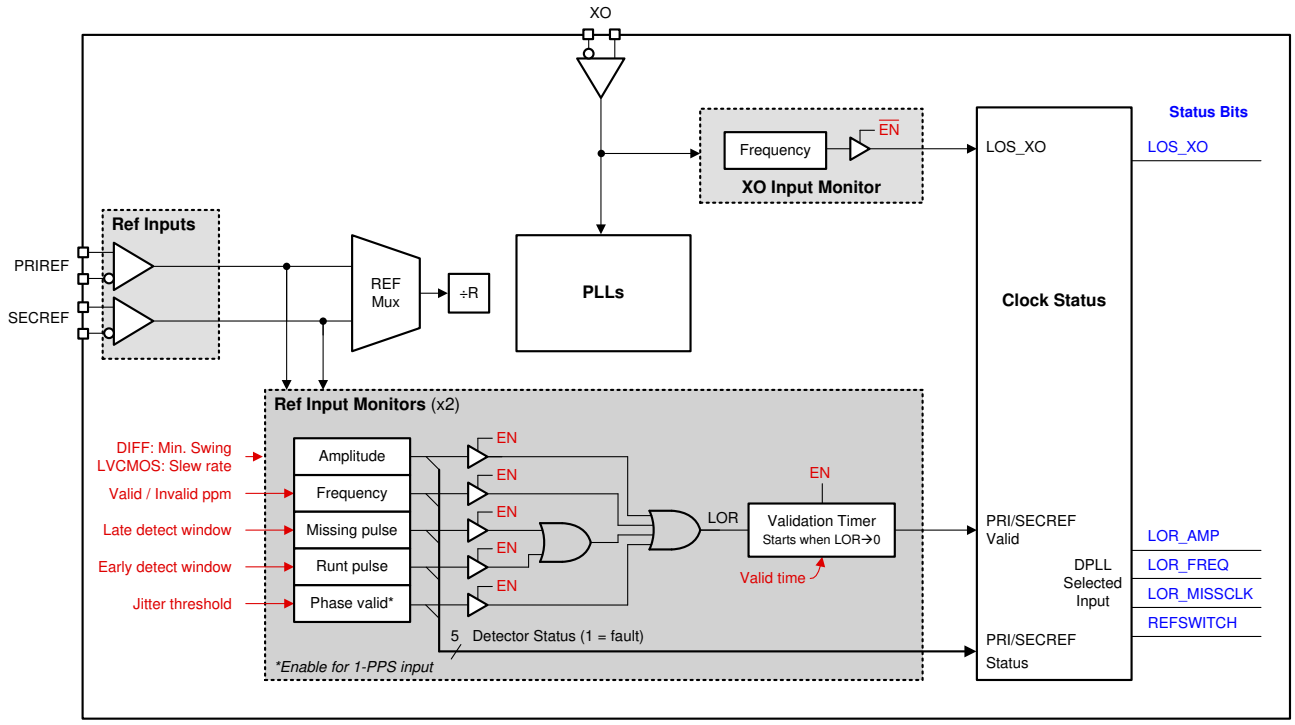


図 37. Clock Monitors for Reference and XO Inputs

9.3.7.1 XO Input Monitoring

The XO input has a coarse frequency monitor to help qualify the input before it is used to lock the APLLs.

The XO frequency detector clears its LOS_XO flag when the input frequency is detected within the supported range of 10 MHz to 100 MHz. The XO frequency monitor uses a RC-based detector and cannot precisely detect if the XO input clock has sufficient frequency stability to ensure successful VCO calibration during the PLL start-up when the external XO clock has a slow or delayed start-up behavior. See *Slow or Delayed XO Start-Up* for more information.

The XO frequency detector can be bypassed by setting the XO_FDET_BYP bit (shown as $\overline{EN}$ in 図 37) so that the XO input is always considered valid by the PLL control state machine. The user can observe the LOS_XO status flag through the status pins and status bit.

9.3.7.2 Reference Input Monitoring

Each DPLL reference clock input is independently monitored for input validation before it is qualified and available for selection by the DPLL. The reference monitoring blocks include amplitude, frequency, missing pulse, and runt pulse monitors. For a 1-PPS input, the phase valid monitor and LVCMOS input amplitude monitor are supported, while the differential input amplitude, frequency, missing pulse, and runt pulse monitors are not supported and must be disabled. A validation timer sets the minimum time for all enabled reference monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all reference monitors and validation timers are programmable per input. The reference monitors and validation timers are optional to enable, but are critical to achieve reliable DPLL lock and optimal transient performance during holdover or switchover events, and are also used to avoid selection of an unreliable or intermittent clock input. If a given detector is not enabled, it will not set a flag and will be ignored. The status flag of any enabled detector can be observed through the status pins for any reference input (selected or not selected). The status flags of the enabled detectors can also be read through the status bits for the selected input of the DPLL.

9.3.7.2.1 Reference Validation Timer

The validation timer sets the amount of time for each reference to be clear of flags from all enabled input monitors before the timer is qualified and valid for selection. The validation timer and enable settings are programmable.

9.3.7.2.2 Amplitude Monitor

The reference amplitude detector determines if the input meets the amplitude-related threshold depending on the input buffer configuration. For differential input mode, the amplitude detector clears its LOR_AMP flag when the differential input voltage swing (peak-to-peak) is greater than the minimum threshold selected by the registers (400, 500, or 600 mVpp nominal). For LVCMOS input mode, the input slew rate detector clears its LOR_AMP flag when its slew rate is faster than 0.2 V/ns on the clock edge selected by the registers (rising edge, falling edge, or both edges). If either the differential or LVCMOS input clock does not meet the specified thresholds, the amplitude detector will set the LOR_AMP flag and disqualify the input.

If the input frequency is below 5 MHz, the differential input detector may signal a false flag. In this case, the amplitude detector should be disabled and at least one other input monitor (frequency, window, or 1-PPS phase valid detector) should be enabled to validate the input clock. The LVCMOS input detector can be used for low-frequency clocks down to 1 Hz or 1 PPS.

9.3.7.2.3 Frequency Monitoring

The precision frequency detector measures the frequency offset or error (in ppm) of all input clocks relative to the XO input's frequency accuracy, which is considered as the "0-ppm reference clock" for frequency comparison. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor will clear the LOR_FREQ flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, the monitor will set the LOR_FREQ flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the LOR_FREQ flag from toggling when the input frequency offset is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the flag, which allow more time for the input frequency to settle, and can also provide better measurement resolution for an input with high drift or wander. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

9.3.7.2.4 Missing Pulse Monitor (Late Detect)

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold (T_{LATE}). When an input pulse arrives before T_{LATE}, the pulse is considered valid and the missing pulse flag will be cleared. When an input pulse does not arrive before T_{LATE} (due to a missing or late pulse), the flag will be set immediately to disqualify the input.

Typically, T_{LATE} should be set higher than the input's longest clock period (including cycle-to-cycle jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The missing pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO1}/12$ and should be disabled when outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block for each reference input. The status flags for both these monitors are combined by logic-OR gate and can be observed through status pin. The window detector flag for the selected DPLL input can also be observed through the corresponding MISSCLK status bit.

9.3.7.2.5 Runt Pulse Monitor (Early Detect)

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold (T_{EARLY}). When an input pulse arrives after T_{EARLY}, the pulse is considered valid and the runt pulse flag will be cleared. When an early or runt input pulse arrives before T_{EARLY}, the monitor will set the flag immediately to disqualify the input.

Typically, T_{EARLY} should be set lower than the input's shortest clock period (including cycle-to-cycle jitter). The early pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The early pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO1}/12$ and should be disabled when outside of this range.

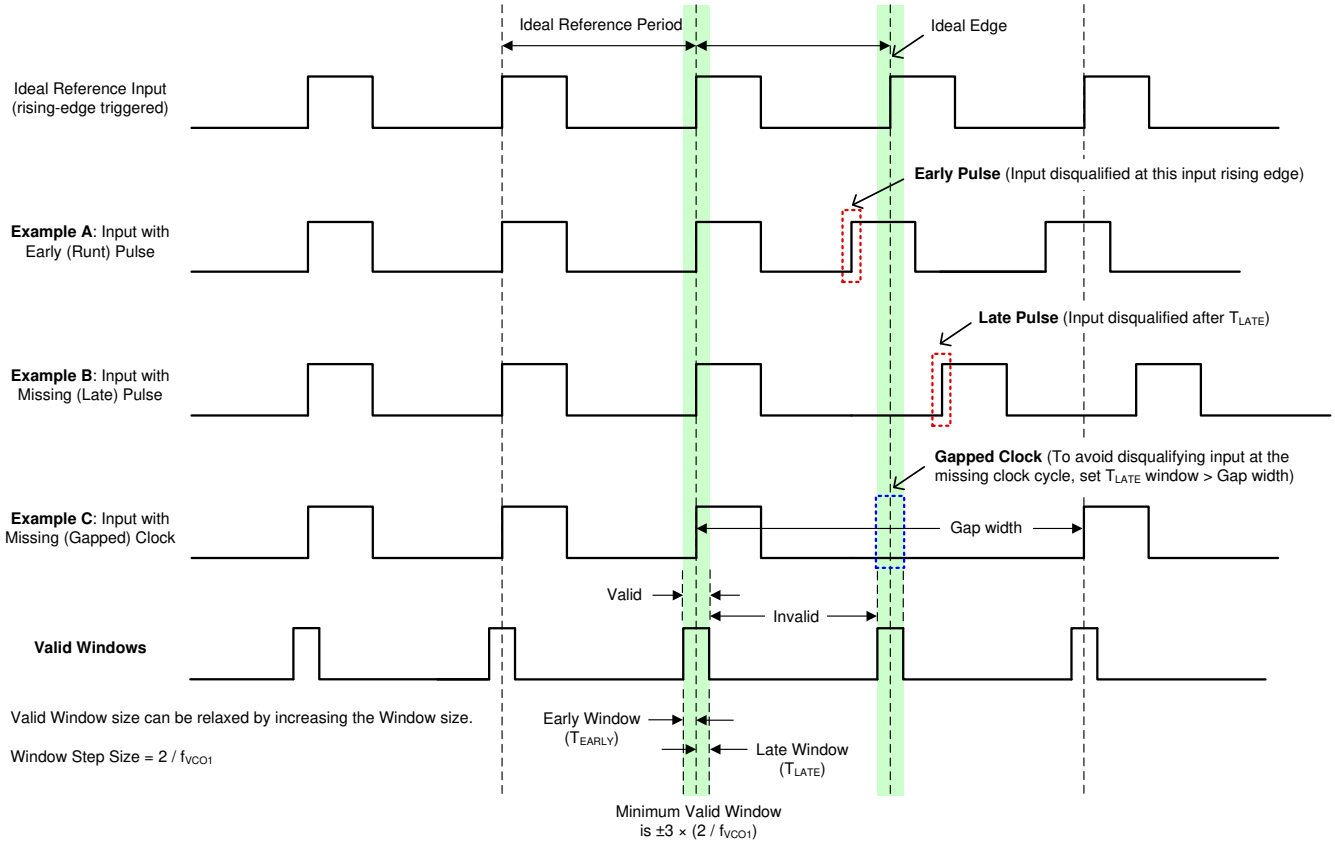


図 38. Early and Late Window Detector Examples

9.3.7.2.6 Phase Valid Monitor for 1-PPS Inputs

The phase valid monitor is designed specifically for 1-PPS input validation because the frequency and window detectors do not support this mode. The phase valid monitor uses a window detector to validate 1-PPS input pulses that arrive within the nominal clock period (T_{IN}) plus a programmable jitter threshold (T_{JIT}). When the input pulse arrives within the counter window (T_V), the pulse is considered valid and the phase valid flag will be cleared. When the input pulse does not arrive before T_V (due to a missing or late pulse), the flag will be set immediately to disqualify the input. T_{JIT} should be set higher than the worst-case input cycle-to-cycle jitter.

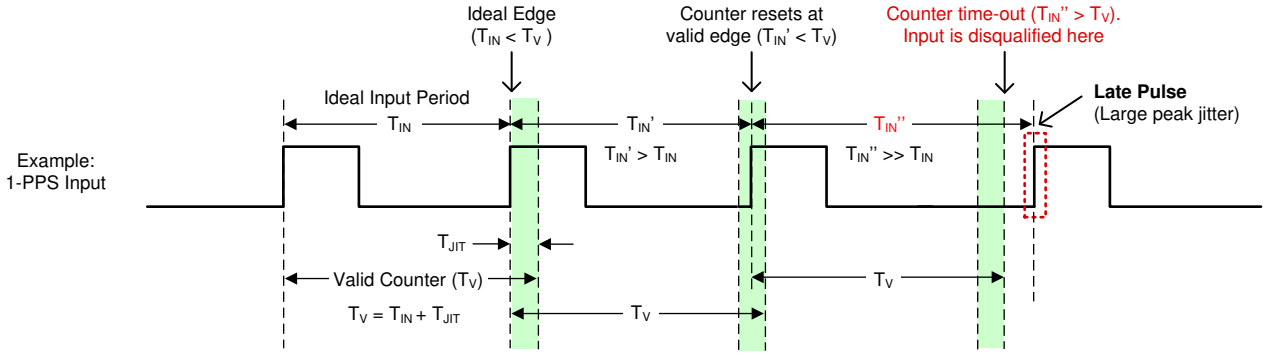


図 39. 1-PPS Input Window Detector Example

9.3.7.3 PLL Lock Detectors

The loss-of-lock (LOL) status is available for each APLL and the DPLL. The APLLs are monitored for loss-of-frequency lock only. The DPLL is monitored for both loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL). The DPLL lock threshold and loss-of-lock threshold are programmable for both LOPF and LOFL detectors.

The DPLL frequency lock detector will clear its LOFL flag when the DPLL's frequency error relative the selected reference input is less than the lock ppm threshold. Otherwise, it will set the LOFL flag when the DPLL's frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency lock detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the LOFL flag. Higher averaging may be useful when locking to an input with high wander or when the DPLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

The DPLL phase lock detector will clear its LOPL flag when the phase error of the DPLL is less than the phase lock threshold. Otherwise, the lock detector will set the LOPL flag when the phase error is greater than the phase unlock threshold.

Users can observe the APLL and DPLL lock detector flags through the status pins and the status bits.

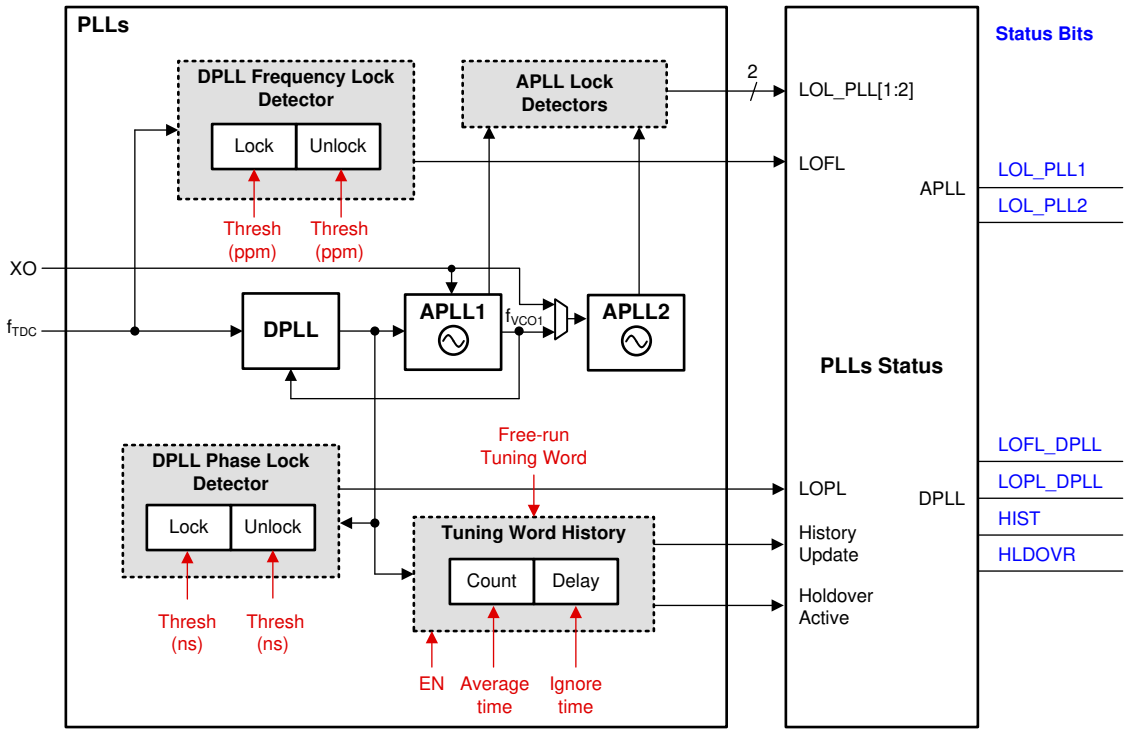


図 40. PLL Lock Detectors and History Monitor

9.3.7.4 Tuning Word History

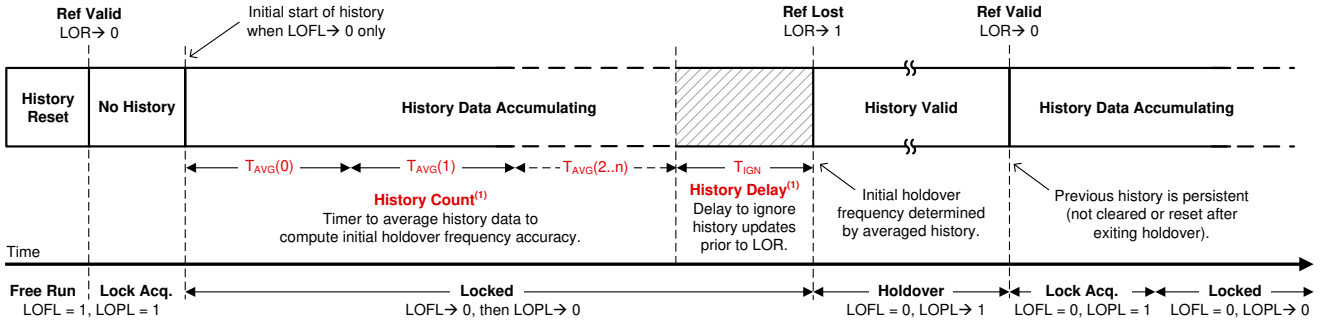
The DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

a. Locked Mode: From the output of the digital loop filter when locked
b. Holdover Mode: From the final output of the history monitor
c. Free Run Mode: From the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, it effectively averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time (T_{AVG}). Once the input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer T_{AVG} time will produce a more accurate initial holdover frequency. The stability of the 0-ppm reference clock (XO input) determines the long-term stability and accuracy of the holdover output frequency.

There is also a separate programmable delay timer (T_{IGN}) that can be set to ignore the history data that is corrupted just prior to entry into holdover. The history data could be corrupted if a tuning word update occurs while the input clock is failing and before it is detected by the input monitors. Both T_{AVG} and T_{IGN} times are programmable through the HISTCNT and HISTDLY register bits, respectively, and are related to the TDC rate.

The tuning word history is initially cleared after a device hard reset or soft reset. After the DPLL locks to a new reference, the history monitor waits for the first T_{AVG} timer to expire before storing the first tuning word value and begins to accumulate history. The history monitor will not clear the previous history value during reference switchover or holdover exit. The history can be manually cleared or reset by toggling the history enable bit (HIST_EN = 1 → 0 → 1), if needed.



(1) History count and delay windows are programmable.

図 41. Tuning Word History Windows

If the T_{AVG} period is set very long (minutes or hours) to obtain a more precise historical average frequency, it is possible for a switchover or holdover event to occur before the first tuning word is stored and available for use. To overcome this, there is an intermediate history update option (HIST_INTMD). If the history is reset, then the intermediate average can be updated at intervals of $T_{AVG}/2^K$, where K = HIST_INTMD to 0, *during the first T_{AVG} period only*. If HIST_INTMD = 0, there is no intermediate update and the first average is stored after the first T_{AVG} period. However, if HIST_INTMD = 4, then four intermediate averages are taken at $T_{AVG}/16$, $T_{AVG}/8$, $T_{AVG}/4$, and $T_{AVG}/2$, as well as at T_{AVG}. After the first T_{AVG} period, all subsequent history updates occur at the T_{AVG} period.

When no tuning word history exists, the free-run tuning word value (TUNING_FREE_RUN) determines the initial holdover output frequency accuracy.

9.3.7.5 Status Outputs

The STATUS0 and STATUS1 pins can be configured to output various status signals and interrupt flag for device diagnostic and debug purposes. The status signal, output driver type, and output polarity settings are programmable. The status signals available at these pins are listed in 表 6. When the status signal is asserted, the status output will be driven high (active high) assuming the output polarity is not inverted (or active low).

表 6. Status Pin Signals Available per Device Block

DEVICE BLOCK MONITORED	STATUS SIGNAL (ACTIVE HIGH)
XO	XO Loss of Signal (LOS)
APLL1 and APLL2	APLLx Lock Detected ($\overline{\text{LOL}}$)
	APLLx VCO Calibration Active
	APLLx N Divider, div-by-2
	APLLx Digital Lock Detect (DLD)
	APLL2 R Divider, div-by-2
EEPROM	EEPROM Active
All Inputs and PLLs	Interrupt (INTR)
PRIREF and SECREF	PRIREF/SECREF Monitor Divider Output, div-by-2
	PRIREF/SECREF Amplitude Monitor Fault
	PRIREF/SECREF Frequency Monitor Fault
	PRIREF/SECREF Missing or Early Pulse Monitor Fault
	PRIREF/SECREF Validation Timer Active
	PRIREF/SECREF Phase Validation Monitor Fault
DPLL	DPLL R Divider, div-by-2
	DPLL FB Divider, div-by-2
	DPLL Phase Lock Detected ($\overline{\text{LOPL}}$)
	DPLL PRIREF/SECREF Selected
	DPLL Holdover Active
	DPLL Reference Switchover Event
	DPLL Tuning History Update
	DPLL FastLock Active
	DPLL Loss of Lock (LOFL)

9.3.7.6 Interrupt

Any of the two status pins can be configured as a device interrupt output pin. The interrupt logic configuration is set through registers. When the interrupt logic is enabled, the interrupt output can be triggered from any combination of interrupt status indicators, including LOS for the XO, LOR for the selected DPLL input, LOL for each APLL and the DPLL, and holdover and switchover events for the DPLL. When the interrupt polarity is set high, a rising edge on the live status bit will assert its interrupt flag (sticky bit). Otherwise, when the polarity is set low, a falling edge on the live status bit will assert its interrupt flag. Any individual interrupt flag can be masked so it does not trigger the interrupt output. The unmasked interrupt flags are combined by the AND/OR gate to generate the interrupt output, which can be selected on either status pin.

When a system host detects an interrupt from the LMK05318, the host can read the interrupt flag or "sticky" registers to identify which bits were asserted to resolve the fault conditions in the system. After the system faults have been resolved, the host can clear the interrupt output by writing zeros to the sticky bits that were asserted.

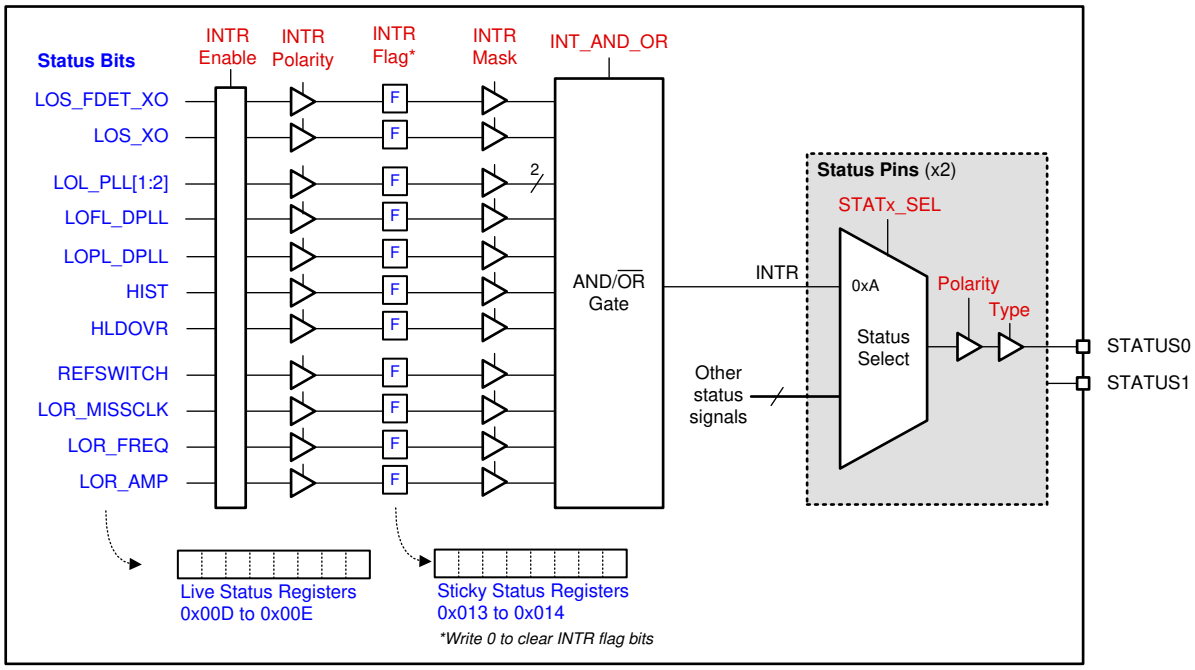


図 42. Status and Interrupt

9.3.8 PLL Relationships

図 43 shows the PLL architecture implemented in the LMK05318. The PLLs can be configured in the different PLL modes described in *PLL Architecture Overview*.

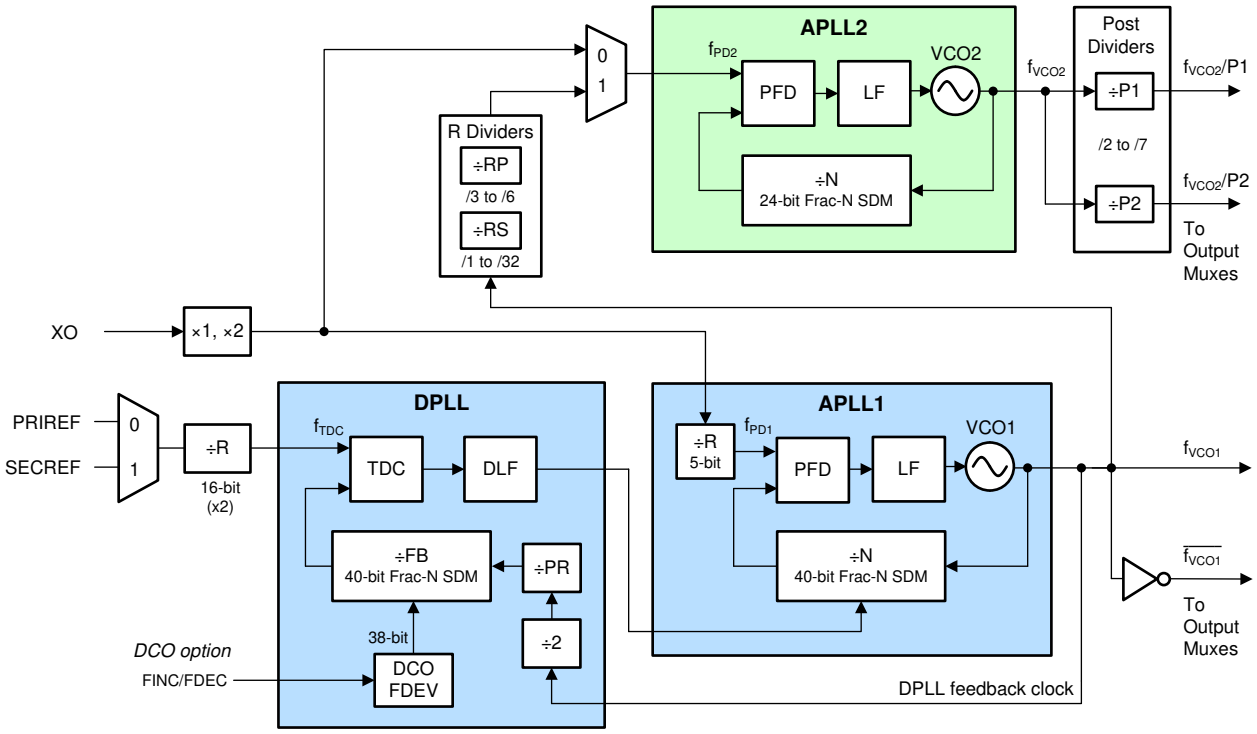


図 43. PLL Architecture

9.3.8.1 PLL Frequency Relationships

The following equations provide the PLL frequency relationships required to achieve closed-loop operation according to the selected PLL mode. The TICS Pro programming software can be used to generate valid divider settings based on the desired frequency plan configuration and PLL mode.

- To operate APLL1 in Free-run mode (locked to the XO input), the conditions in 式 1 and 式 2 must be met.
- To operate APLL1 in DPLL mode, the conditions in 式 1, 式 2, 式 3, and 式 4 must be met.
- To operate APLL2 in Cascaded mode, the conditions in 式 1, 式 2, 式 5, and 式 7 must be met.
- To operate APLL2 in Non-cascaded mode, the conditions in 式 6 and 式 7 must be met.

Note that any divider in the following equations refer to the actual divide value (or range) and not its programmable register value.

式 1 and 式 2 relate to APLL1:

$$f_{PD1} = f_{XO} \times D_{XO} / R_{XO} \quad (1)$$

where

- f_{PD1} = APLL1 phase detector frequency
- f_{XO}: XO input frequency
- D_{XO}: XO input doubler (1 = disabled, 2 = enabled)
- R_{XO}: APLL1 XO Input R divider value (1 to 32)

$f_{VCO1} = f_{PD1} \times (INT_{APLL1} + NUM_{APLL1} / DEN_{APLL1})$

where

- f_{VCO1}: VCO1 frequency
- INT_{APLL1}: APLL1 N divider integer value (12 bits, 1 to $2^{12} – 1$)
- NUM_{APLL1}: APLL1 N divider numerator value (40 bits, 0 to $2^{40} – 1$)
- DEN_{APLL1}: APLL1 N divider denominator value (fixed, 2^{40})
  - $0.125 < NUM_{APLL1} / DEN_{APLL1} < 0.875$ (In DPLL Mode) (2)

式 3 and 式 4 relate to the DPLL:

$f_{TDC} = f_{PRIREF} / R_{PRIREF} = f_{SECREF} / R_{SECREF}$

where

- f_{TDC}: DPLL TDC input frequency (see 式 3)
- f_{PRIREF} or f_{SECREF}: PRIREF or SECREF input frequency
- R_{PRIREF} or R_{SECREF}: PRIREF or SECREF R divider value (16 bits, 1 to $2^{16} – 1$) (3)

$f_{VCO1} = f_{TDC} \times 2 \times PR_{DPLL} \times (INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL})$

where

- PR_{DPLL}: DPLL prescaler divider value (2 to 17)
- INT_{DPLL}: DPLL FB divider integer value (30 bits, 1 to $2^{30} – 1$)
- NUM_{DPLL}: DPLL FB divider numerator value (40 bits, 0 to $2^{40} – 1$)
- DEN_{DPLL}: DPLL FB divider denominator value (40 bits, 1 to 2^{40}) (4)

式 5, 式 6, and 式 7 relate to APLL2:

Cascaded APLL2: $f_{PD2} = f_{VCO1} / (R_{APLL2\_PRE} \times R_{APLL2\_SEC})$

where

- f_{PD2}: APLL2 phase detector frequency
- R_{APLL2_PRE}: Cascaded APLL2 Pre R divider value (3 to 6)
- R_{APLL2_SEC}: Cascaded APLL2 Secondary R divider value (1 to 32) (5)

Non-Cascaded APLL2: $f_{PD2} = f_{XO} \times D_{XO}$ (6)

$f_{VCO2} = f_{PD2} \times (INT_{APLL2} + NUM_{APLL2} / DEN_{APLL2})$

where

- f_{VCO2}: VCO2 frequency
- INT_{APLL2}: APLL2 N divider integer value (9 bits, 1 to $2^{9} – 1$)
- NUM_{APLL2}: APLL2 N divider numerator value (24 bits, 0 to $2^{24} – 1$)
- DEN_{APLL2}: APLL2 N divider denominator value (fixed, 2^{24}) (7)

式 8, 式 9, 式 10, and 式 11 relate to the output frequency, which depends on the selected APLL clock source and output divider value:

APLL1 selected: $f_{CHxMUX} = f_{VCO1}$ (8)

APLL2 selected: $f_{CHxMUX} = f_{VCO2} / Pn_{APLL2}$ (9)

OUT[0:6]: $f_{OUTx} = f_{CHxMUX} / OD_{OUTx}$ (10)

OUT7: $f_{OUT7} = f_{CH7MUX} / (OD_{OUT7} \times OD2)$

where

- f_{CHxMUX}: Output mux source frequency (APLL1 or APLL2 post-divider clock)
- Pn_{APLL2}: APLL2 primary "P1" or secondary "P2" post-divide value (2 to 7)
- f_{OUTx}: Output clock frequency (x = 0 to 7)
- OD_{OUTx}: OUTx output divider value (8 bits, 1 to 2^{8})
- OD2: OUT7 secondary output divider value (24 bits, 1 to 2^{24})
  - If OD2 > 1, then $OD_{OUT7} \geq 6$ (11)

9.3.8.2 Analog PLLs (APLL1, APLL2)

APLL1 has a 40-bit fractional-N divider and APLL2 has a 24-bit fractional-N divider to support high-resolution frequency synthesis and very low phase noise and jitter. APLL1 has the ability to tune its VCO1 frequency through sigma-delta modulator (SDM) control in DPLL mode. APLL2 has the ability to lock its VCO2 frequency to the VCO1 frequency.

In free-run mode, APLL1 uses the XO input as an initial reference clock to VCO1. APLL1's PFD compares the fractional-N divided clock with its reference clock and generates a control signal. The control signal is filtered by the APLL1 loop filter to generate VCO1's control voltage to set its output frequency. The SDM modulates the N divider ratio to get the desired fractional ratio between the PFD input and the VCO output. APLL2 operates similar to APLL1, but the user can select APLL2's reference from either the VCO1 clock or XO clock.

In DPLL mode, the APLL1 fractional SDM is controlled by the DPLL loop to pull the VCO1 frequency into lock with the DPLL reference input. If APLL2 derives its reference from VCO1, then VCO2 will be effectively locked to the DPLL reference input, assuming there is no synthesis error introduced by the fractional N divide ratio of APLL2.

9.3.8.3 APLL Reference Paths

9.3.8.3.1 APLL XO Doubler

The APLL XO doubler can be enabled to double the PFD frequency up to 50 MHz for APLL1 and up to 150 MHz for APLL2 in Non-Cascaded mode. Enabling the XO doubler adds minimal noise and can be useful to increase the PFD frequency to optimize phase noise, jitter, and fractional spurs. The flat portion of the APLL phase noise can improve when the PFD frequency is increased.

9.3.8.3.2 APLL1 XO Reference (R) Divider

APLL1 has a 5-b XO R divider that can be used to meet the maximum APLL1 PFD frequency specification. It can also be used to ensure the APLL1 fractional-N divide ratio (NUM/DEN) is between 0.125 to 0.875, which is recommended to support the DPLL frequency tuning range. Otherwise, the XO R divider can be bypassed (divide by 1).

9.3.8.3.3 APLL2 Reference (R) Dividers

APLL2 has a cascaded primary R divider (÷3 to ÷6) and secondary R divider (÷1 to ÷32) to divide-down the VCO1 clock to meet the maximum APLL2 PFD frequency specification in Cascaded APLL2 mode. The dividers can also be used to operate APLL2 in integer mode or avoid near-integer spurs in fractional mode.

9.3.8.4 APLL Phase Frequency Detector (PFD) and Charge Pump

The APLL1 PFD frequency can operate up to 50 MHz and can be computed by 式 1. APLL1 has programmable charge pump settings from 0 to 1500 µA in 100-µA steps. Best performance from APLL1 is achieved with a charge pump currents of 800 µA or higher.

The APLL2 PFD frequency can operate up to 150 MHz and can be computed by 式 5 in Cascaded mode or 式 6 in Non-cascaded mode. APLL2 has programmable charge pump settings of 1.6, 3.2, 4.8, or 6.4 mA.

9.3.8.5 APLL Feedback Divider Paths

The VCO output of each APLL is fed back to its PFD block through the fractional feedback (N) divider. The VCO1 output is also fed back to the DPLL feedback path in DPLL mode.

9.3.8.5.1 APLL1 N Divider With SDM

The APLL1 fractional N divider includes a 12-b integer portion (INT), a 40-b numerator portion (NUM), a fixed 40-b denominator portion (DEN), and a sigma-delta modulator. The INT and NUM are programmable, while the denominator is fixed to 2^{40} for very high frequency resolution on the VCO1 clock. The total APLL1 N divider value is: $N = INT + NUM / 2^{40}$.

In APLL free-run mode, the PFD frequency and total N divider for APLL1 determine the VCO1 frequency, which can be computed by 式 2.

9.3.8.5.2 APLL2 N Divider With SDM

The APLL2 fractional N divider includes a 9-b integer portion (INT), a 24-b numerator portion (NUM), a fixed 24-b denominator portion (DEN), and a sigma-delta modulator. The INT and NUM are programmable, while the denominator is fixed to 2^{24} for high frequency resolution on the VCO2 clock. The total APLL2 N divider value is: N = INT + NUM / 2^{24}.

The PFD frequency and total N divider for APLL2 determine the VCO2 frequency, which can be computed by 式 7.

9.3.8.6 APLL Loop Filters (LF1, LF2)

APLL1 supports a programmable loop bandwidth from 100 Hz to 10 kHz (typical range), and APLL2 supports a programmable loop bandwidth from 100 kHz to 1 MHz (typical range). The loop filter components can be programmed to optimize the APLL bandwidth depending on the reference input frequency and phase noise. The LF1 and LF2 pins each require an external "C2" capacitor to ground. See the suggested values for the LF1 and LF2 capacitors in the *Pin Configuration and Functions* section.

図 44 shows the APLL loop filter structure between the PFD/charge pump output and VCO control input.

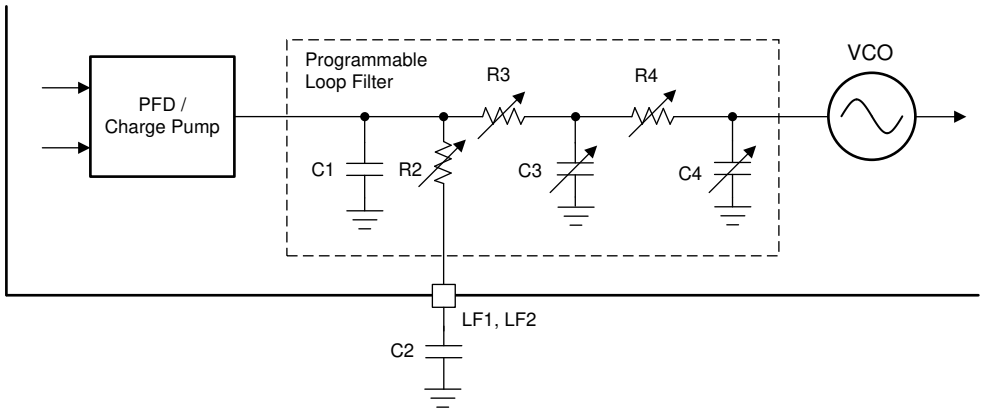


図 44. Loop Filter Structure of Each APLL

9.3.8.7 APLL Voltage Controlled Oscillators (VCO1, VCO2)

Each APLL contains a fully-integrated VCO, which takes the voltage from its loop filter and converts this into a frequency. VCO1 uses proprietary BAW resonator technology with a very high quality factor to deliver the lowest phase jitter and has a tuning range of 2.5 GHz ± 50 ppm. VCO2 uses a high-performance LC VCO with a wider tuning range of 5.5 to 6.25 GHz to cover a additional unrelated clock frequencies, if needed.

9.3.8.7.1 VCO Calibration

Each APLL VCO must be calibrated to ensure that the PLL can achieve lock and deliver optimal phase noise performance. VCO calibration establishes an optimal operating point within the VCO tuning range. VCO calibration is executed automatically during initial PLL start-up after device power-on, hard-reset, or soft-reset once the XO input is detected by its input monitor. To ensure successful calibration and APLL lock, it is critical for the XO clock to be stable in amplitude and frequency before the start of calibration; otherwise, the calibration can fail and prevent PLL lock and output clock start-up. Before VCO calibration and APLL lock, the output drivers are typically held in the mute state (configurable per output) to prevent spurious output clocks.

A VCO calibration can be triggered manually for a single APLL by toggling a PLL power-down cycle (PLLx_PDN bit = 1 → 0) through host programming. This may be needed after the APLL N divider value (VCO frequency) is changed dynamically through programming.

9.3.8.8 APLL VCO Clock Distribution Paths (P1, P2)

APLL1 has no VCO post-dividers. The primary VCO1 clock (P1) and a secondary VCO1 inverted clock (P2) are distributed to all output channel muxes. The inverted clock is optional, but it can help to reduce spurious in some cases.

APLL2 has two VCO2 post-dividers to provide more flexible clock frequency planning. The primary VCO2 post-divider clock (P1) and secondary post-divider clock (P2) are distributed to all output channel muxes. Both VCO2 post-dividers support independently programmable dividers (÷2 to ÷7). Note that output SYNC is not supported between output channels selecting a VCO2 post-divider of 2.

A PLL2 or device soft-reset is recommended after changing the APLL2 post-divider value to initialize it for deterministic divider operation.

9.3.8.9 DPLL Reference (R) Divider Paths

Each reference input clock (PRIREF and SECREF) has its own 16-b reference divider to the DPLL TDC block. The R divider output of the selected reference sets the TDC input frequency. To support hitless switching between inputs with different frequencies, the R dividers can be used to divide the clocks to a single common frequency to the DPLL TDC input.

9.3.8.10 DPLL Time-to-Digital Converter (TDC)

The TDC input compares the phase of the R divider clock of the selected reference input and the DPLL feedback divider clock from VCO1. The TDC output generates a digital correction word corresponding to the phase error which is processed by the DPLL loop filter.

The DPLL TDC input frequency (f_{TDC}) can operate up to 26 MHz and can be computed by 式 3.

9.3.8.11 DPLL Loop Filter (DLF)

The DPLL supports a programmable loop bandwidth from 10 mHz to 4 kHz and can achieve jitter peaking below 0.1 dB (typical). The low-pass jitter transfer characteristic of the DPLL attenuates its reference input noise with up to 60-dB/decade roll-off above the loop bandwidth.

The DPLL loop filter output controls the fractional SDM of APLL1 to steer the VCO1 frequency into lock with the selected DPLL reference input.

9.3.8.12 DPLL Feedback (FB) Divider Path

The DPLL feedback path has a fixed prescaler (÷2), programmable prescaler (÷2 to ÷17), and a fractional feedback (FB) divider. The programmable DPLL FB divider includes a 30-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total DPLL FB divider value is: FB_{DPLL} = INT + NUM / DEN.

In DPLL mode, the TDC frequency and total DPLL feedback divider and prescalers determine the VCO1 frequency, which can be computed by 式 4.

9.3.9 Output Clock Distribution

The output clock distribution blocks shown in 図 45 include six output muxes, six output dividers, and eight programmable output drivers. The output dividers support output synchronization (SYNC) to allow phase synchronization between two or more output channels. Also, the OUT7 channel has an optional zero-delay mode (ZDM) synchronization feature to support deterministic input-to-output phase alignment (typically for 1-PPS clocks) with programmable offset.

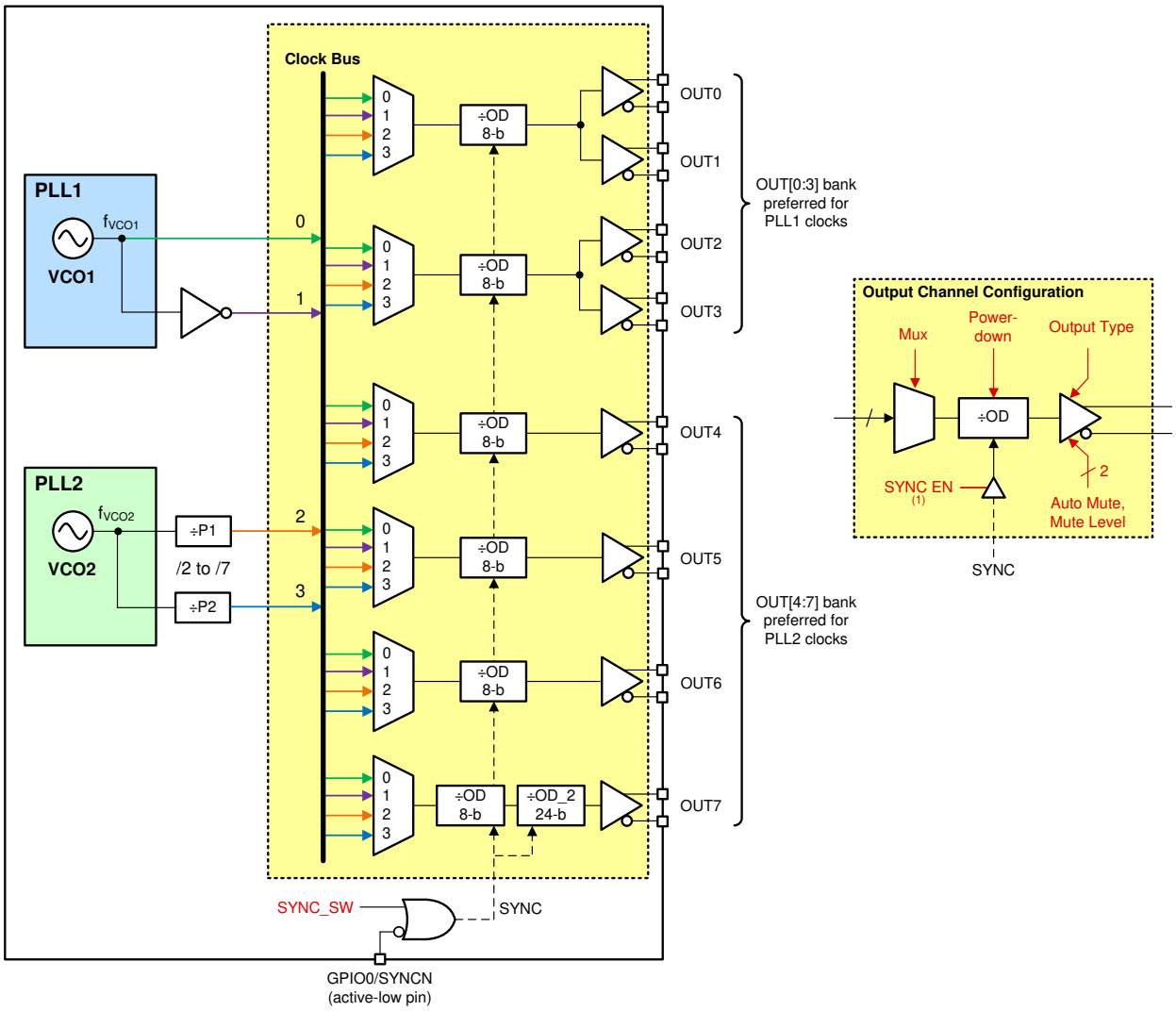


図 45. Output Clock Distribution

9.3.10 Output Channel Muxes

Each of the six output channels has as output mux. Each output mux for the OUT0 to OUT7 channels can individually select between the PLL1 VCO clocks (normal or inverted) and PLL2 VCO post-divider clocks.

9.3.11 Output Dividers (OD)

Each of the six output channels has an output divider after the output mux. The OUT[0:1] channel has a single output divider that is similar to the OUT[2:3] channel output divider. Each OUT[4:7] channel has an individual output divider. The output divider is used to generate the final clock output frequency from the source selected by the output mux.

Each OUT[0:6] channel has an 8-bit divider (OD) that can support output frequencies from 10 to 800 MHz (or up to the maximum frequency supported by the configured output driver type). It is possible to configure the PLL post-divider and output divider to achieve higher clock frequencies, but the output swing of the driver may fall out of specification.

The OUT7 channel has cascaded 8-bit (OD) and 24-bit (OD2) output dividers to support output frequencies from 1 Hz (1 PPS) to 800 MHz. The total OUT7 divide value is the product of the cascaded divider values (OD × OD2).

Each output divider is powered from the same VDDO_x supply used for the clock output drivers. The output divider can be powered down if not used to save power. For either OUT[0:1] or OUT[2:3] channel, the output divider is automatically powered down when both output drivers are disabled. For any OUT[4:7] channel, the output divider is automatically powered down when its output driver is disabled.

9.3.12 Clock Outputs (OUTx_P/N)

Each clock output can be individually configured as a differential driver (AC-LVDS/CML/LVPECL), HCSL driver, or 1.8-V LVCMOS drivers (two per pair). Otherwise, it can be disabled if not used to save power.

Each output channel has its own internal LDO regulator to provide excellent PSNR and minimize jitter and spurs induced by supply noise. The OUT[0:1] channel (mux, divider, and drivers) are powered through a single output supply pin (VDDO_01), and similarly for the OUT[2:3] channel (VDDO_23). Each OUT[4:7] channel have their own output supply pin (VDDO[4:7]). Each output supply can be separately powered by 1.8 V, 2.5 V, or 3.3 V for a differential or HCSL output, or 1.8 V for an LVCMOS output.

For differential and HCSL driver modes, the output clock specifications (such as output swing, phase noise, and jitter) are not sensitive to the VDDO_x voltage because of the channel's internal LDO regulator. When an output channel is left unpowered, the channel's output(s) will not generate any clocks.

表 7. Output Driver Modes

OUTx_FMT	OUTPUT FORMAT(1)
00h	Disabled (powered-down)
10h	AC-LVDS
14h	AC-CML
18h	AC-LVPECL
2Ch	HCSL (External 50-Ω to GND)
2Dh	HCSL (Internal 50-Ω to GND)
30h	LVCMOS (HiZ / HiZ)
32h	LVCMOS (HiZ / –)
33h	LVCMOS (HiZ / +)
35h	LVCMOS (Low / Low)
38h	LVCMOS (– / HiZ)
3Ah	LVCMOS (– / –)
3Bh	LVCMOS (– / +)
3Ch	LVCMOS (+ / HiZ)
3Eh	LVCMOS (+ / –)
3Fh	LVCMOS (+ / +)

(1) LVCMOS modes are only available on OUT[4:7].

9.3.12.1 AC-Differential Output (AC-DIFF)

The programmable differential output driver uses a switched-current mode type shown in 図 46. A tail current of 4, 6, or 8 mA (nominal) can be programmed to achieve V_{OD} swing compatible with AC-coupled LVDS, CML, or LVPECL receivers, respectively, across a 100-Ω differential termination. The differential output driver is ground-referenced (similar to an HCSL driver), meaning the differential output has a low common-mode voltage (V_{OS}).

The differential driver has internal biasing, so external pullup or pulldown resistors should not be applied. The differential output should be interfaced through external AC-coupling to a differential receiver with proper input termination and biasing.

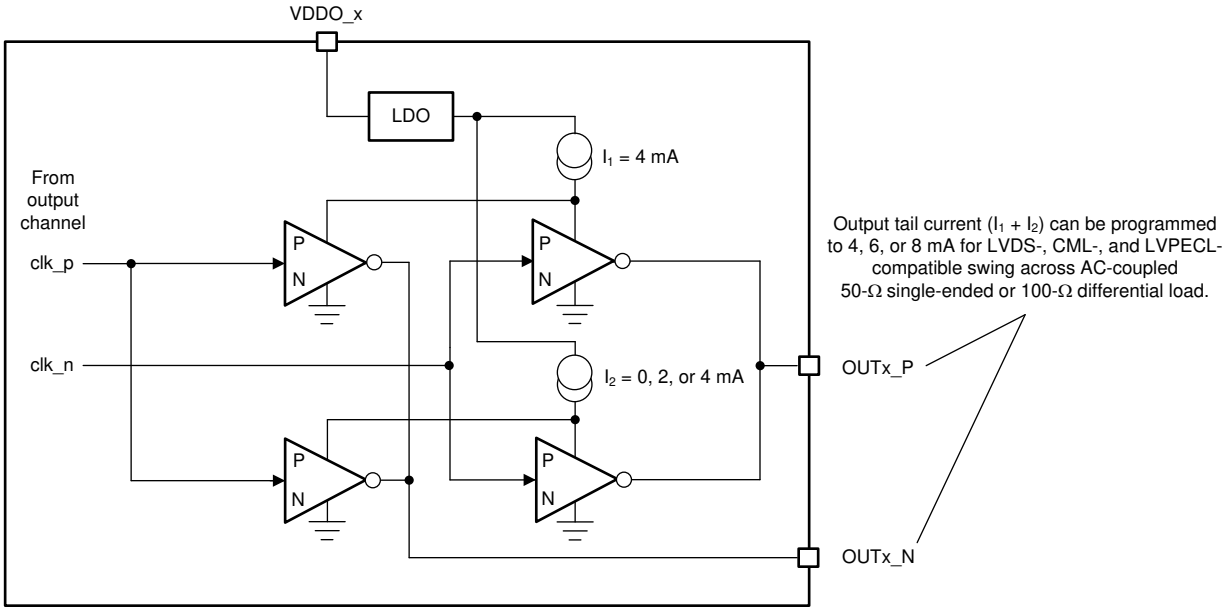


図 46. AC-LVDS/CML/LVPECL Output Driver Structure

9.3.12.2 HCSL Output

The HCSL output is an open-drain differential driver that can be DC-coupled to an HCSL receiver. The HCSL output has programmable internal 50-Ω termination to ground which can be enabled if the receiver side does not provide termination. If the internal termination is disabled, external 50-Ω to ground (on P and N) is required at either the driver side (source terminated) or the receiver side (load terminated).

9.3.12.3 1.8-V LVCMOS Output

The LVCMOS driver has two outputs per pair. Each output on P and N can be configured for normal polarity, inverted polarity, or disabled as HiZ or static low level. The LVCMOS output high level (V_{OH}) is determined by the VDDO_x voltage of 1.8 V for rail-to-rail LVCMOS output voltage swing. If a VDDO_x voltage of 2.5 V or 3.3 V is applied to the LVCMOS driver, the output V_{OH} level not will not swing to the VDDO_x rail due to the channel's internal LDO regulator.

Because an LVCMOS output clock is an unbalanced signal with large voltage swing, it can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks. If an LVCMOS clock is required from an output pair, configure the pair with both outputs enabled but with opposite polarity (+/– or –/+) and leave the unused output floating with no trace connected.

9.3.12.4 Output Auto-Mute During LOL

Each output driver can automatically mute or squelch its clock when the selected output mux clock source is invalid, as configured by its CHx_MUTE bit. The source can be invalid based on the LOL status of each PLL by configuring the APLL and DPLL mute control bits (MUTE_APLLx_LOCK, MUTE_DPLL_LOCK, MUTE_DPLL_PHLOCK). The mute level can be configured per output channel by its CHx_MUTE_LVL bits, where the mute level depends on the configured output driver type (Differential/HCSL or LVCMOS). The mute level for a differential or HCSL driver can be set to output common mode, differential high, or differential low levels. The mute level for an LVCMOS driver pair can be set to output low level for each of its outputs (P and N) independently. When auto-mute is disabled or bypassed (CHx_MUTE = 0 and CHx_MUTE_LVL = 0), the output clock can have incorrect frequency or be unstable before and during the VCO calibration. For this reason, the mute bypass mode should only be used for diagnostic or debug purposes.

9.3.13 Glitchless Output Clock Start-Up

When APLL auto-mute is enabled, the outputs will start up in synchronous fashion without clock glitches once APLL lock is achieved after any the following events: device power-on, exiting hard-reset, exiting soft-reset, or deasserting output SYNC (when SYNC_MUTE = 1).

9.3.14 Clock Output Interfacing and Termination

図 47 to 図 51 show the recommended output interfacing and termination circuits. Unused clock outputs can be left floating and powered down by programming.

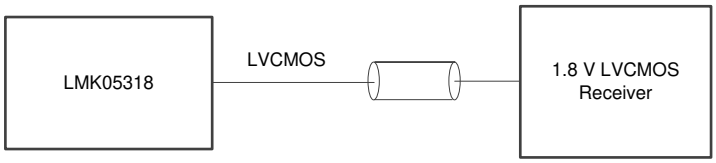


図 47. 1.8-V LVCMOS Output to 1.8-V LVCMOS Receiver

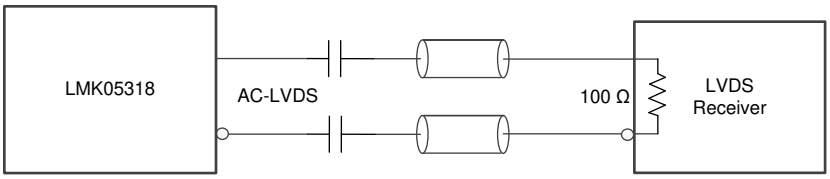


図 48. AC-LVDS Output to LVDS Receiver With Internal Termination/Biasing

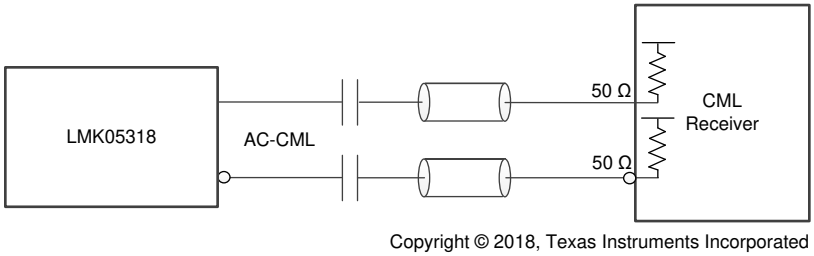


図 49. AC-CML Output to CML Receiver With Internal Termination/Biasing

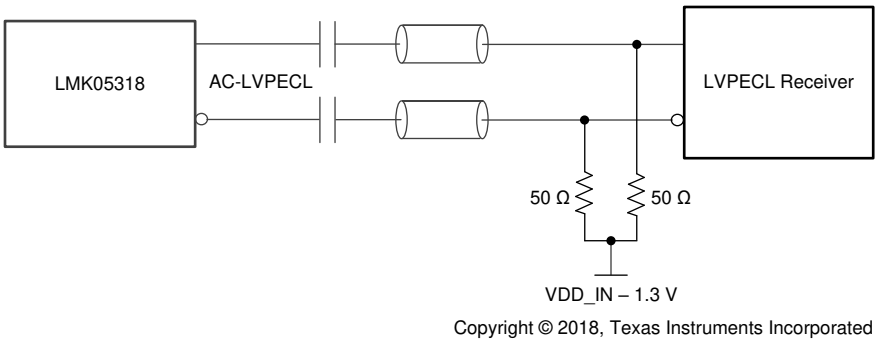
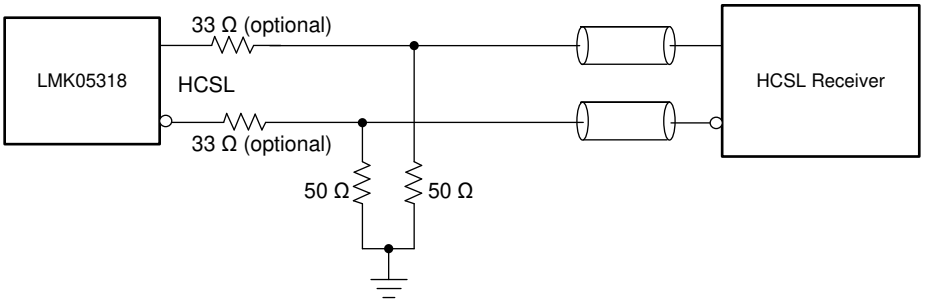


図 50. AC-LVPECL Output to LVPECL Receiver With External Termination/Biasing



If HCSL Internal Termination (50-Ω to GND) is enabled, short 33-Ω and remove 50-Ω external resistors.

図 51. HCSL Output to HCSL Receiver With External Source Termination

9.3.15 Output Synchronization (SYNC)

Output SYNC can be used to phase-align two or more output clocks with a common rising edge by allowing the output dividers to exit reset on the same PLL output clock cycle. Any output dividers selecting the same PLL output can be synchronized together as a SYNC group by triggering a SYNC event through the hardware pin or software bit.

The following requirements must be met to establish a SYNC group for two or more output channels:

- Output dividers have their respective sync enable bit set (CHx_SYNC_EN = 1).
- Output dividers have their output mux selecting the same PLL output.
- The PLL (post-divider) output has its sync enable bit set (for example, PLL1_P1_SYNC_EN = 1).

A SYNC event can be asserted by the hardware GPIO0/SYNCN pin (active low) or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers held are reset and clock outputs are muted. When SYNC is deasserted, the outputs will start with their initial clock phases synchronized or aligned. SYNC can also be used to mute any SYNC-enabled outputs to prevent output clocks from being distributed to downstream devices until they are configured and ready to accept the incoming clock.

Output channels with their sync disabled (CHx_SYNC_EN bit = 0) will not be affected by a SYNC event and will continue normal output operation as configured. Also, VCO and PLL post-divider clocks do not stop running during the SYNC so they can continue to source output channels that do not require synchronization. Output dividers with divide-by-1 (divider bypass mode) are not gated during the SYNC event.

表 8. Output Synchronization

GPIO0/SYNCN PIN	SYNC_SW BIT	OUTPUT DIVIDER AND DRIVER STATE
0	1	Output driver(s) muted and output divider(s) reset
0→1	1→0	Outputs in a SYNC group are unmuted with their initial clock phases aligned
1	0	Normal output driver/divider operation as configured

注

Output SYNC is not supported (output-to-output skew specifications is not ensured) between output channels selecting a PLL2 output (P1 or P2) with VCO2 post-divider of 2.

9.3.16 Zero-Delay Mode (ZDM) Synchronization for 1-PPS Input and Output

Zero-delay mode synchronization can be enabled to achieve *zero* phase delay between the selected DPLL reference input clock and the OUT7 clock as shown in 図 52. This is primarily used to achieve deterministic phase relationship between a 1-PPS input and 1-PPS output. This feature can be configured through registers by enabling ZDM (DPLL_ZDM_SYNC_EN bit = 1) and enabling OUT7 divider synchronization (CH7_SYNC_EN bit = 1). The OUT7 clock must be derived from the DPLL and APLL1 VCO domain (f_{VCO1}).

When the DPLL is not locked and the DPLL reference input is invalid, the OUT7 clock is held in mute state (no clock). Once the reference input is validated and selected, the OUT7 channel divider is reset or *SYNCed* using the DPLL reference input clock edge to achieve a deterministic phase relationship between the reference input and OUT7 clock. OUT7 is not affected by normal output SYNC events, and OUT[0:6] are not be affected by a ZDM SYNC event. The input-to-output phase offset can be adjusted through the DPLL phase offset register control (DPLL_REF_SYNC_PH_OFFSET bits). If the DPLL phase offset is programmed on-the-fly with 1-PPS input, it can take a long time to adjust due to the narrow DPLL bandwidth (10 mHz typical).

Hitless switching between 1-PPS inputs is not supported when ZDM is enabled. If a switchover event between 1-PPS inputs occurs when ZDM is enabled, a soft-reset should be issued for the DPLL to relock and realign the 1-PPS output to the selected input.

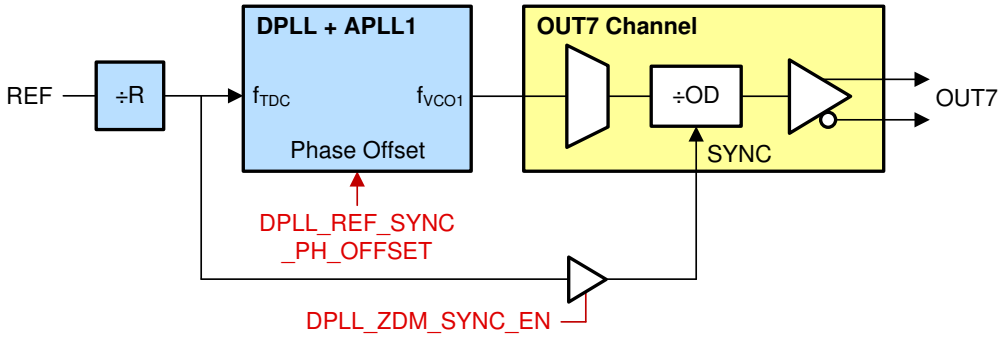


図 52. DPLL ZDM Synchronization Between Reference Input and OUT7

9.4 Device Functional Modes

9.4.1 Device Start-Up Modes

The LMK05318 can start up in one of three device modes depending on the 3-level input level sampled on the HW_SW_CTRL pin during power-on reset (POR):

- **HW_SW_CTRL = 0:** EEPROM + I^2C Mode (Soft pin mode)
- **HW_SW_CTRL = Float (V_{IM}):** EEPROM + SPI Mode (Soft pin mode)
- **HW_SW_CTRL = 1:** ROM + I^2C Mode (Hard pin mode)

The device start-up mode determines:

- The memory bank (EEPROM or ROM) used to initialize the register settings that sets the frequency configuration.
- The serial interface (I^2C or SPI) used for register access.
- The logic pin functionality for device control and status.

After start-up, the I^2C or SPI interface is enabled for register access to monitor the device status and control (or reconfigure) the device if needed. The register map configurations are the same for I^2C and SPI.

Table 1 summarizes the device start-up mode and corresponding logic pin functionality.

図 53 shows the device power-on reset configuration sequence.

Device Functional Modes (continued)

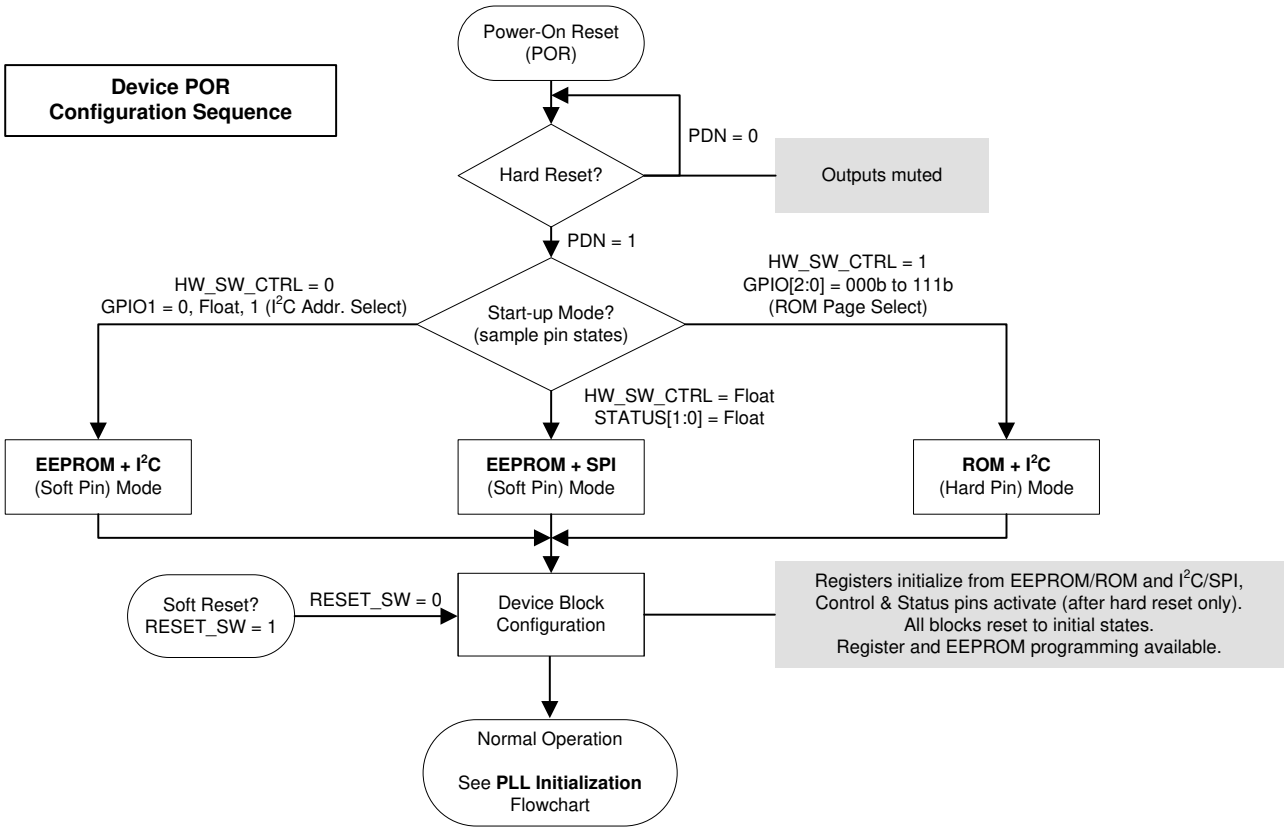


図 53. Device POR Configuration Sequence

9.4.1.1 EEPROM Mode

In EEPROM mode, the frequency configuration of the device is loaded to the registers from the non-volatile EEPROM. The factory default start-up configuration for EEPROM mode is summarized in EEPROM Start-Up Mode Default Configuration. If a different custom start-up configuration is needed, a different EEPROM image can be programmed in-system through the serial interface. The EEPROM supports up to 100 programming cycles to facilitate clock reconfiguration for system-level prototyping, debug, and optimization.

The EEPROM image can store a single frequency configuration (one register page). Upon request, a factory pre-programmed device with a custom EEPROM image could be assigned by TI with a unique orderable part number (OPN).

TI suggests to use the EEPROM mode when either of the following is true:

- A single custom start-up frequency configuration is required from a single OPN.
- A host device is available to program the registers (and EEPROM if needed) with a new configuration after power-up through I^2C or SPI. SPI is not supported in ROM mode.

9.4.1.2 ROM Mode

In ROM mode, the frequency configuration of the device is loaded to the registers from one of eight register pages in ROM selected by the GPIO[2:0] control pins. All register pages in the ROM image can be factory-set in hardware (mask ROM) and are not software programmable. Only the I^2C interface is available for register access after start-up in ROM mode.

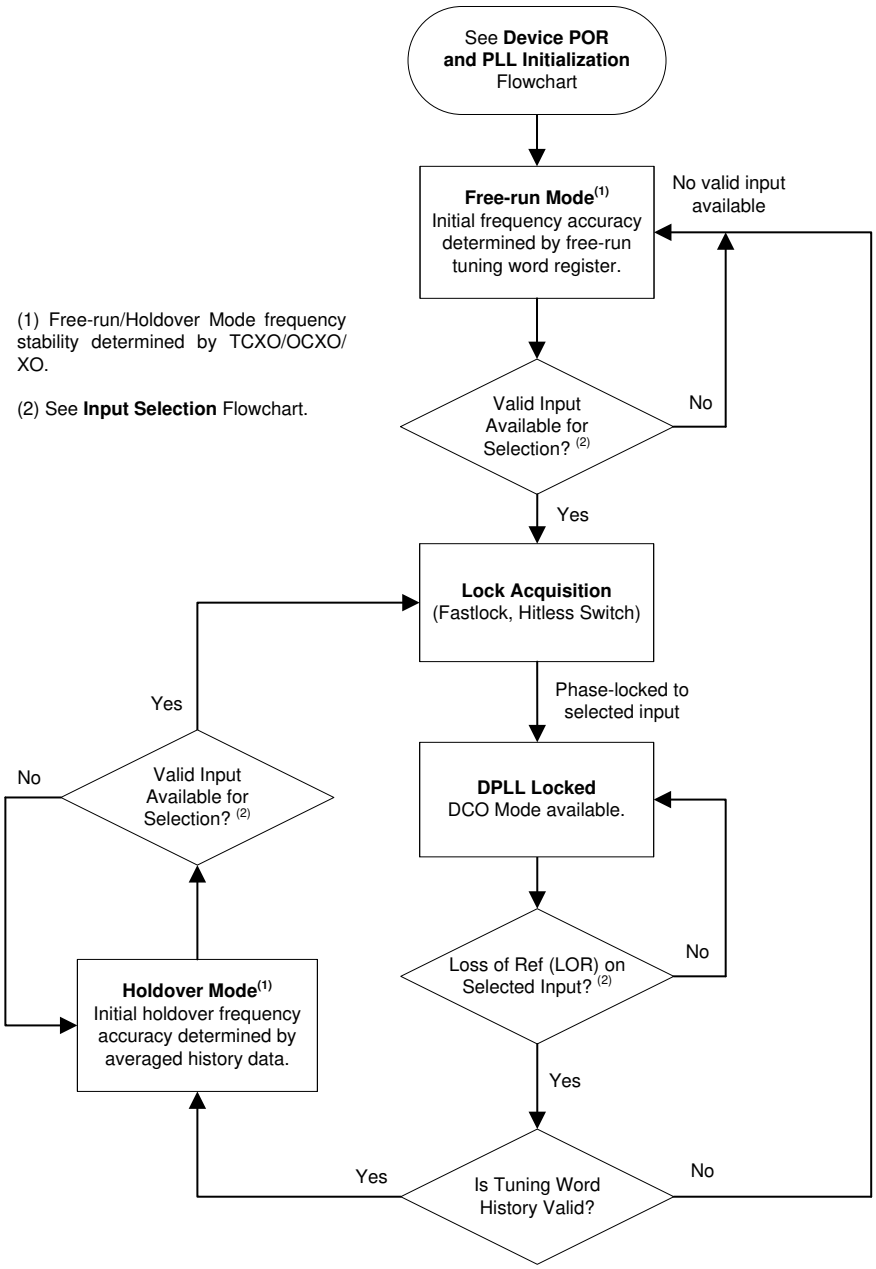
The factory ROM image have default register pages intended for TI internal use, but ROM pages may be allocated for future custom frequency configurations upon request.

Device Functional Modes (continued)

A benefit of ROM mode over EEPROM mode is that a custom ROM image can support up to eight different pin-selectable frequency configurations from a single OPN. Upon request, a factory preset device with a custom ROM image could be assigned by TI with a unique OPN.

9.4.2 PLL Operating Modes

The following sections describe the PLL modes of operation shown in 図 54.



(1) Assumes DPLL_HLDOVR_MODE bit is 0 to enter free-run mode if history is not valid.

図 54. PLL Operating Mode

Device Functional Modes (continued)

9.4.2.1 Free-Run Mode

After device POR configuration and initialization, APLL1 will automatically lock to the XO clock once it is detected by its input monitor. Then, APLL2 will acquire lock to either VCO1 or XO frequency as selected. The output clock frequency accuracy and stability in free-run mode are equal to that of the XO input. The reference inputs remain invalid (unqualified) during free-run mode.

9.4.2.2 Lock Acquisition

The DPLL constantly monitors its reference inputs for a valid input clock. When at least one valid input clock is detected, the PLL1 channel will exit free-run mode or holdover mode and initiate lock acquisition through the DPLL. The device supports the Fastlock feature where the DPLL temporarily engages a wider loop bandwidth to reduce the lock time. Once the lock acquisition is done, the loop bandwidth is set to its normal configured loop bandwidth setting (BW_{DPLL}).

9.4.2.3 Locked Mode

Once locked, the APLL1 output clocks are frequency and phase locked to the selected DPLL input clock. While the DPLL is locked, the APLL1 output clocks will not be affected by frequency drift on the XO input. The DPLL has a programmable frequency lock detector and phase lock detectors to indicate loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL) status flags, which can be observed through the status pins or status bits. Once frequency lock is detected (LOFL → 0), the tuning word history monitor (if enabled) will begin to accumulate historical averaging data used to determine the initial output frequency accuracy upon entry into holdover mode.

9.4.2.4 Holdover Mode

When a loss-of-reference (LOR) condition is detected and no valid input is available, the PLL1 channel enters holdover mode. If the tuning word history is valid, the initial output frequency accuracy upon entry into holdover will be pulled to the computed average frequency accuracy just prior to the loss of reference. If history is not valid (no history exists) and the DPLL_HLDOVR_MODE bit is 0, the holdover frequency accuracy will be determined by the free-run tuning word register (user programmable). Otherwise, if history is not valid and DPLL_HLDOVR_MODE is 1, the DPLL will hold its last digital loop filter output control value (which is not tuning word history).

If history is valid, the initial holdover frequency accuracy depends on the DPLL loop bandwidth and the elapsed time used for historical averaging. See *Tuning Word History*. In general, the longer the historical average time, the more accurate the initial holdover frequency assuming the 0-ppm reference clock (XO input) is drift-free. The stability of the XO reference clock determines the long-term stability and accuracy of the holdover output frequency. Upon entry into holdover, the LOPL flag will be asserted (LOPL → 1). The LOFL flag will not be asserted, however, as long as the holdover frequency accuracy does not drift beyond of the programmed loss-of-frequency-lock threshold. When a valid input becomes available for selection, the PLL1 channel will exit holdover mode and automatically phase lock with the new input clock without any output glitches.

9.4.3 PLL Start-Up Sequence

図 55 shows the general sequence for PLL start-up after device configuration. This sequence is also applicable after a device soft-reset or individual PLL soft-reset. To ensure proper VCO calibration, it is critical for the external XO clock to be stable in amplitude and frequency prior to the start of VCO calibration. Otherwise, the VCO calibration can fail and prevent start-up of the PLL and its output clocks.

Device Functional Modes (continued)

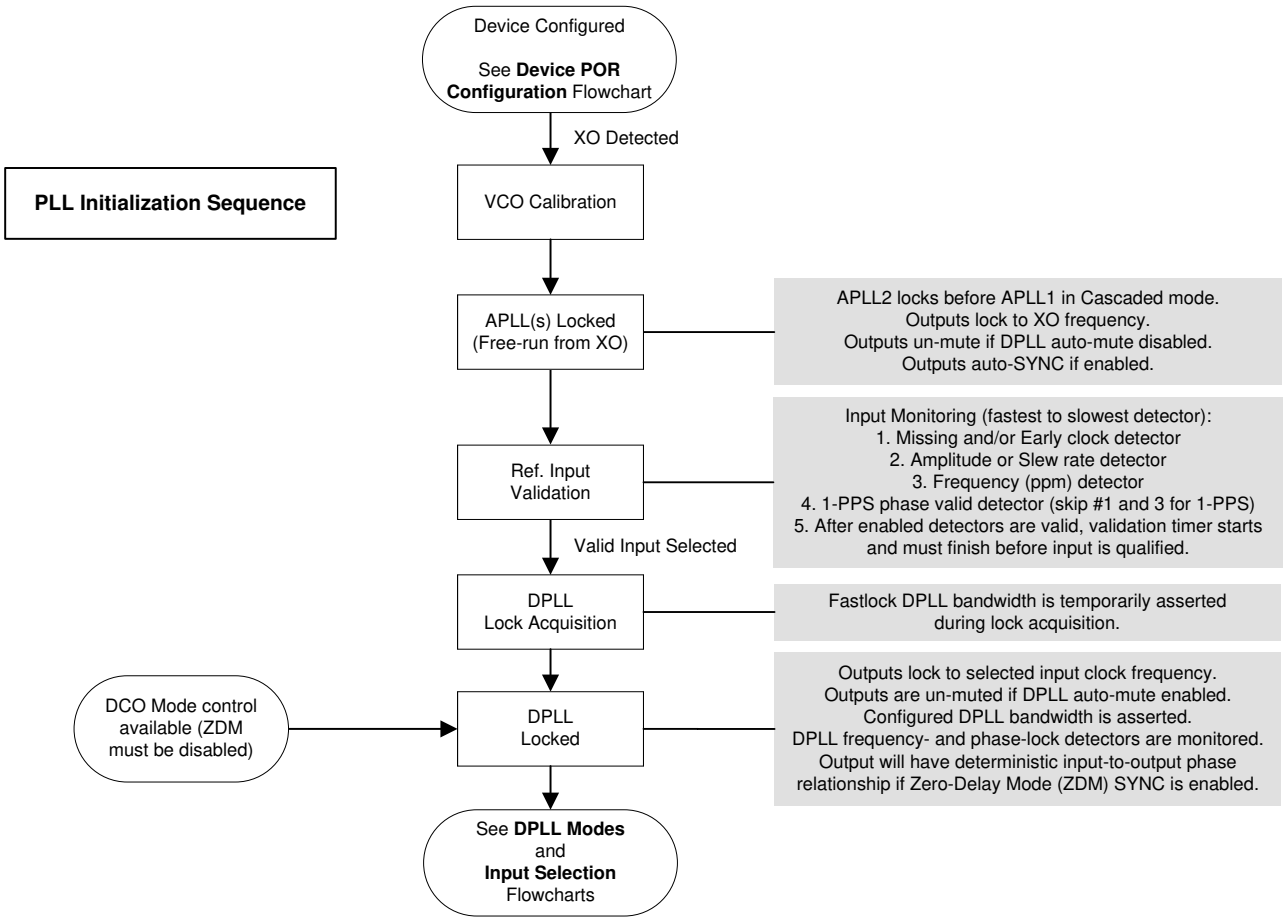


図 55. PLL Start-Up Sequence

9.4.4 Digitally-Controlled Oscillator (DCO) Mode

To support the IEEE 1588 slave clock and other clock steering applications, the DPLL supports DCO mode to allow precise output clock frequency adjustment of less than 0.001 ppb/step. DCO mode can be enabled (DPLL_FDEV_EN = 1) when the DPLL is locked.

The DCO frequency step size can be programmed through a 38-bit frequency deviation word register (DPLL_FDEV bits). The DPLL_FDEV value is an offset added to or subtracted from the current numerator value of the DPLL fractional feedback divider and determines the DCO frequency offset at the VCO output.

The DCO frequency increment (FINC) or frequency decrement (FDEC) updates can be controlled through software control or pin control in I^2C mode. DCO updates through software control are always available through I^2C or SPI by writing to the DPLL_FDEV_REG_UPDATE register bit. Writing a 0 will increment the DCO frequency by the programmed step size, and writing a 1 will decrement it by the step size. SPI can achieve faster DCO update rates than to I^2C because the SPI has faster register transfer.

When pin control mode is enabled (GPIO_FDEV_EN = 1) in I^2C mode, the GPIO2/SDO/FINC pin will function as the FINC input and the STATUS1/FDEC pin will function as the FDEC input (STATUS1 output will be disabled). A positive pulse on the FINC pin or FDEC pin will apply a corresponding DCO update to the DPLL. The minimum positive pulse width applied to the FINC or FDEC pins should be greater than 100 ns to be captured by the internal sampling clock. The DCO update rate should be limited to less than 1 MHz when using pin control.

Device Functional Modes (continued)

When DCO mode is disabled (DPLL_FDEV_EN = 0), the DCO frequency offset will be cleared and the VCO output frequency will be determined by the original numerator value of the DPLL fractional feedback divider.

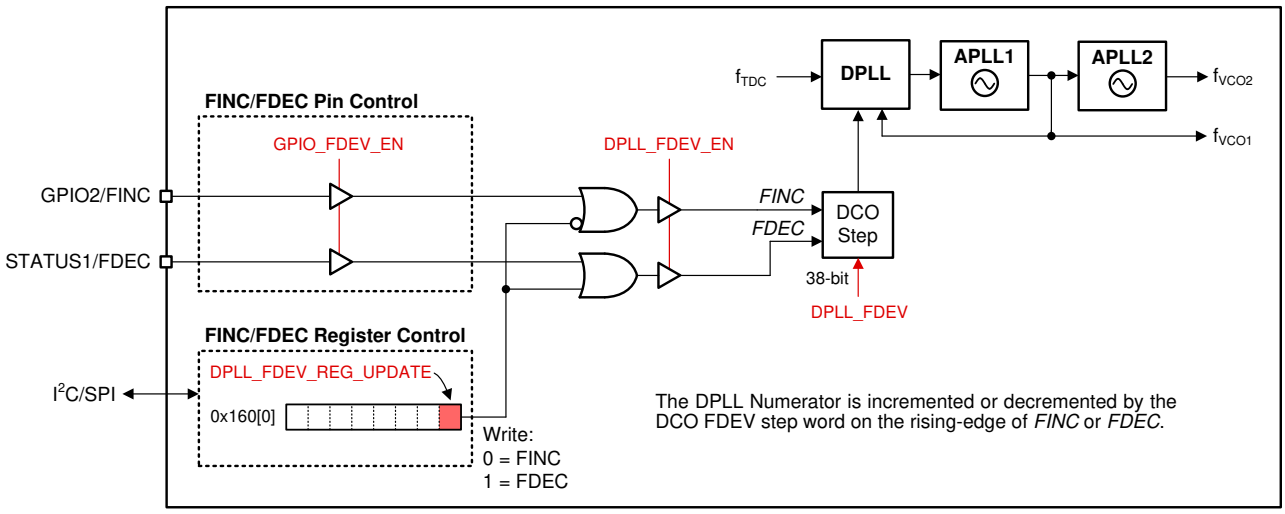


図 56. DCO Mode Control Options

9.4.4.1 DCO Frequency Step Size

式 12 shows the formula to compute the DPLL_FDEV register value required to meet the specified DCO frequency step size in ppb (part-per-billion) when DCO mode is enabled for the DPLL.

$$DPLL\_FDEV = (Reqd\_ppb / 10^9) \times DEN_{DPLL} \times f_{VCO1} / (2 \times PR_{DPLL}) / (f_{REF} / R_{REF}) \quad (12)$$

where

- DPLL_FDEV: Frequency deviation value (0 to 2^{38}- 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- DEN_{DPLL}: DPLL FB divider denominator value (1 to 2^{40})
- f_{VCO1}: VCO1 frequency
- PR: DPLL feedback prescaler divide value (2 to 17)
- f_{REF}: PRIREF or SECREF input frequency
- Rx: PRIREF or SECREF input divide value (1 to 2^{16}- 1)

9.4.4.2 DCO Direct-Write Mode

An alternate method to update the DCO frequency is to take the current numerator value (DPLL_REF_NUM) of the DPLL fractional feedback divider, compute the adjusted numerator value by adding or subtracting the DPLL_FDEV step value computed above, and write the adjusted numerator value through I^2C or SPI.

9.4.5 Zero-Delay Mode Synchronization

The DPLL supports a zero-delay mode (ZDM) synchronization option to achieve a known and deterministic phase relationship between the selected DPLL reference input and the OUT7 clock. This is primarily intended to achieve phase alignment between a 1-PPS input and 1-PPS output. See *Zero-Delay Mode (ZDM) Synchronization for 1-PPS Input and Output*.

9.5 Programming

9.5.1 Interface and Control

A system host device (MCU or FPGA) can use either I^2C or SPI to access the register, SRAM, and EEPROM maps. The register and EEPROM map configurations are the same for I^2C and SPI. The device can be initialized, controlled, and monitored through register access during normal operation (when PDN is deasserted). Some device features can also be controlled and monitored through the external logic control and status pins.

In the absence of a host, the LMK05318 can self-start from its on-chip EEPROM or ROM page depending on the state of HW_SW_CTRL pin. The EEPROM or ROM page is used to initialize the registers upon device POR. A custom EEPROM configuration can be programmed in-system through the register interface by either I^2C or SPI. The ROM configurations are fixed in hardware and cannot be modified.

図 57 shows the device control pin, register, and memory interfaces. The arrows refer to the control interface directions between the different blocks.

The register map has 435 data bytes. Some registers,such as status registers and internal test/diagnostic registers (above R352), do not need to be written during device initialization.

The SRAM/EEPROM map has one register page with 256 data bytes. The SRAM/EEPROM map has fewer bytes because not all bit fields are mapped from the register space. To program the EEPROM, it is necessary to write the register contents to SRAM (internal register commit or direct write), then Program EEPROM with the register contents from SRAM.

The ROM map has eight register pages with 249 data bytes per page. The ROM contents are fixed in hardware and cannot be modified.

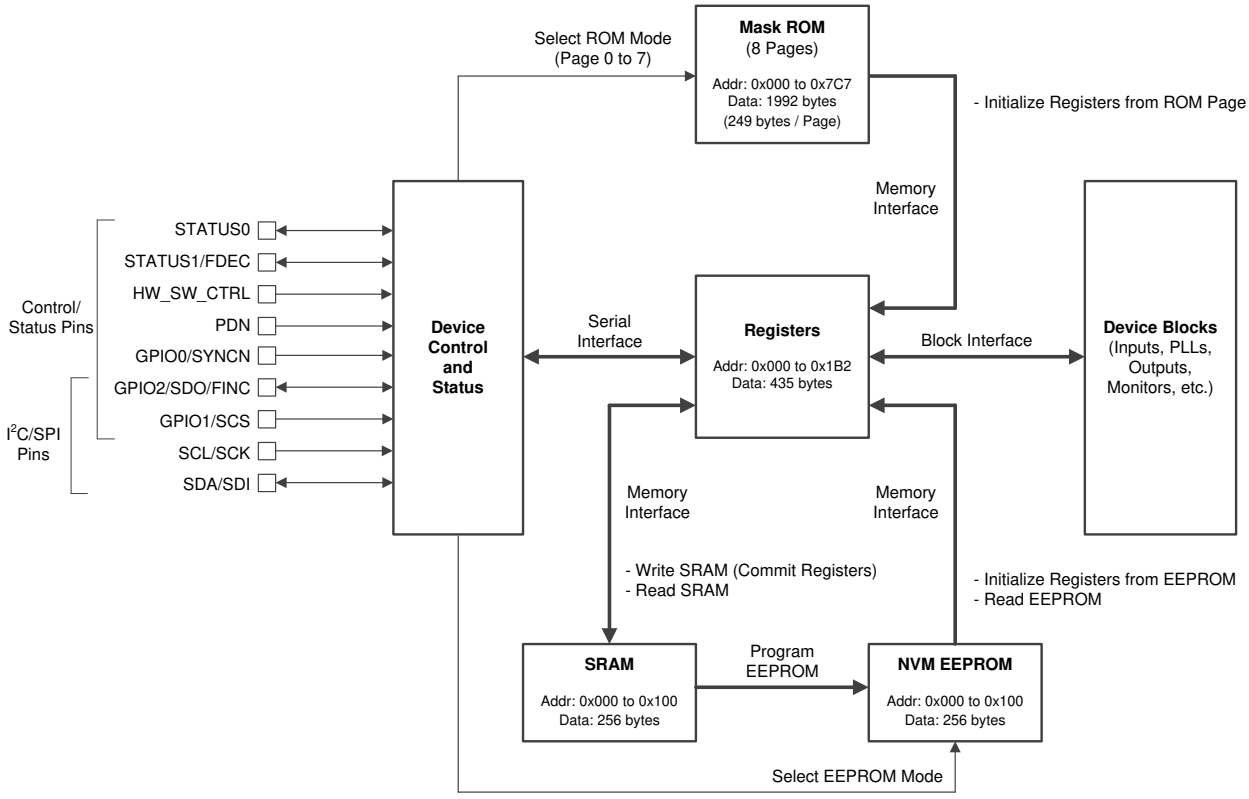


図 57. Device Control, Register, and Memory Interfaces

Programming (continued)

9.5.2 I²C Serial Interface

When started in I²C mode (HW_SW_CTRL = 0 or 1), the LMK05318 operates as an I²C slave and supports bus rates of 100 kHz (standard mode) and 400 kHz (fast mode). Slower bus rates can work as long as the other I²C specifications are met.

In EEPROM mode, the LMK05318 can support up to four different I²C addresses depending on the GPIO1 pins. The 7-bit I²C address is 11001xxb, where the two LSBs are determined by the GPIO1 input levels sampled at device POR and the five MSBs (11001b) are initialized from the EEPROM. In ROM mode, the two LSBs are fixed to 00b, while the five MSB (11001b) are initialized from the EEPROM.

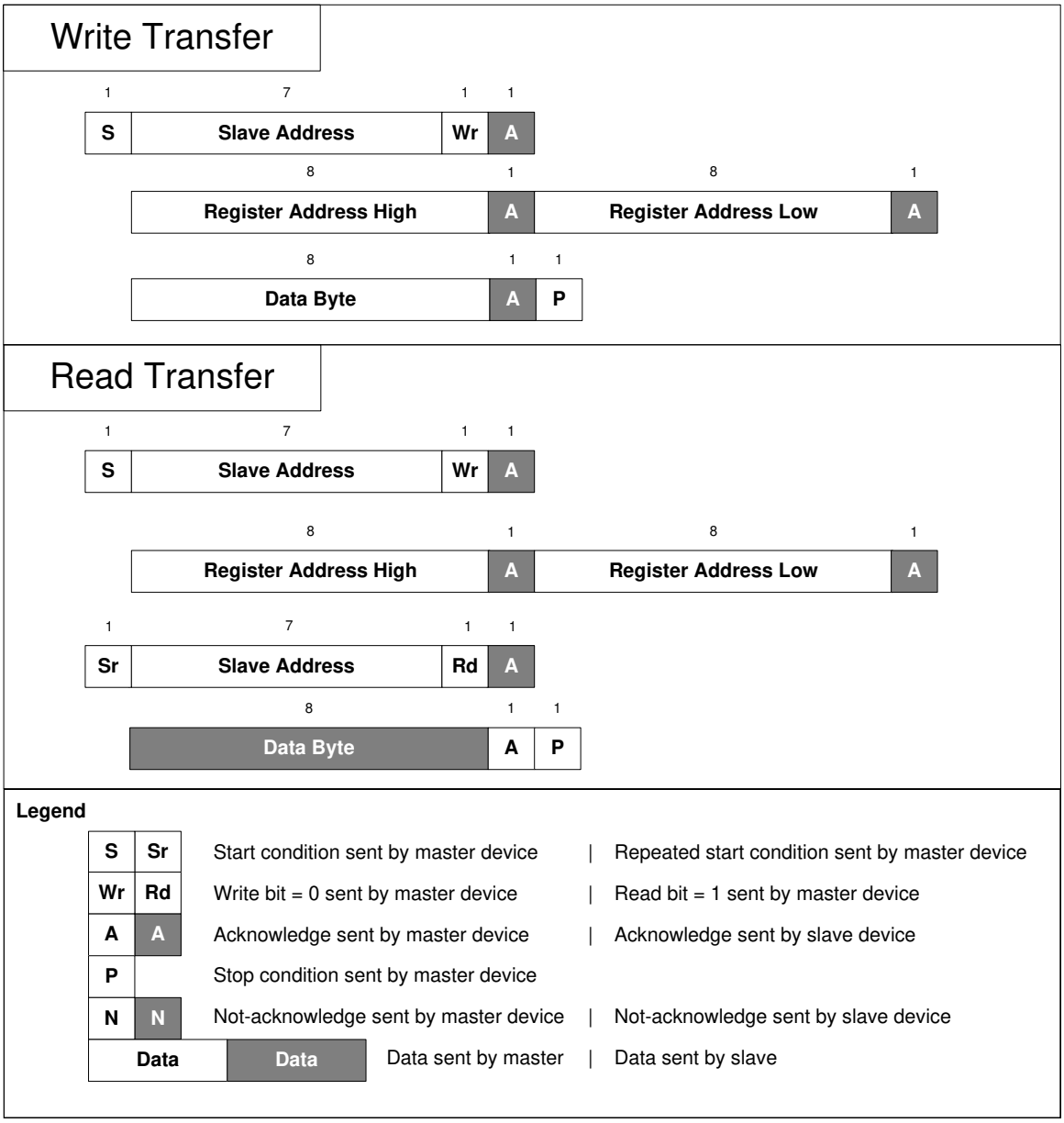


図 58. I²C Byte Write and Read Transfers

Programming (continued)

9.5.2.1 I²C Block Register Transfers

The device supports I²C block write and block read register transfers as shown in 図 59.

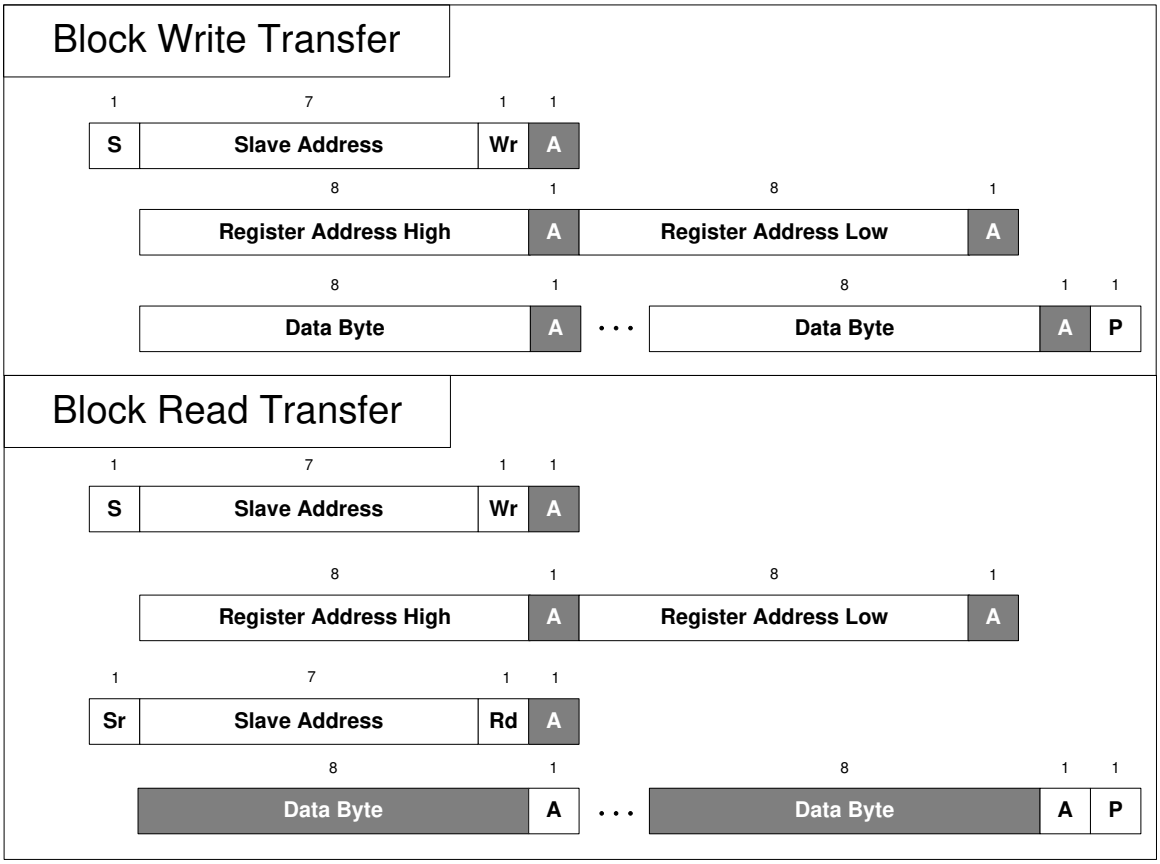


図 59. I²C Block Register Transfers

9.5.3 SPI Serial Interface

When started in SPI mode (HW_SW_CTRL = Float or V_{IM}), the device uses a 4-wire SPI interface with SDI, SCK, SDO, and SCS signals. The host device must present data to the device MSB first. A message includes a transfer direction bit (W/R), a 15-bit address field (A14 to A0), and a 8-bit data field (D7 to D0) as shown in 図 60. The W/R bit is 0 for a SPI write and 1 for a SPI read.

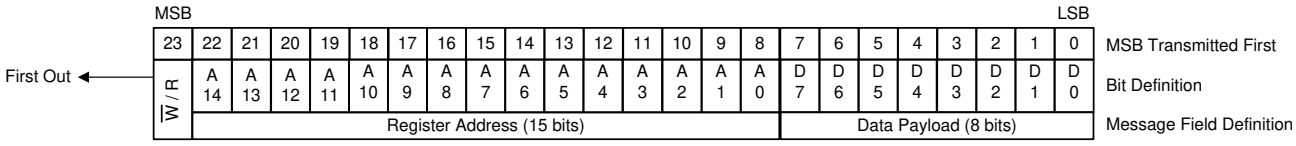


図 60. SPI Message Format

A message frame is initiated by asserting SCS low. The frame ends when SCS is deasserted high. The first bit transferred is the W/R bit. The next 15 bits are the register address, and the remaining eight bits are data. On write transfers, data is committed in bytes as the final data bit (D0) is clocked in on the rising edge of SCK. If the write access is not an even multiple of eight clocks, the trailing data bits are not committed. On read transfers, data bits are clocked out from the SDO pin on the falling edges of SCK.

Programming (continued)

9.5.3.1 SPI Block Register Transfer

The device supports a SPI block write and block read transfers. A SPI block transfer is exactly (2 + N) bytes long, where N is the number of data bytes to write or read. The host device (SPI master) is only required to specify the lowest address of the sequence of addresses to be accessed. The device will automatically increment the internal register address pointer if the SCS pin remains low after the host finishes the initial 24-bit transmission sequence. Each transfer of eight bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

9.5.4 Register Map and EEPROM Map Generation

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user-selected clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register map data (hex format) or SRAM/EEPROM map data can be exported to enable host programming of the LMK05318 on start-up.

If desired, customers may send their TICS Pro setup file (.tcs) to TI to review and optimize the configuration settings or to support factory pre-programmed samples.

9.5.5 General Register Programming Sequence

For applications that use a system host to program the initial LMK05318 configuration after start-up, this general procedure can be followed from the register map data generated and exported from TICS Pro:

1. Apply power to the device to start in I^2C or SPI mode. The PDN pin must be pulled high or driven high.
2. Write the register settings from lower to higher addresses (R0 to R352) while applying the following register mask (do not modify mask bits = 1):
   - Mask R12 = A7h (Device reset/control register)
   - Mask R157 = FFh (NVM control bits register)
   - Mask R164 = FFh (NVM unlock bits register)
   - Mask R353 to R435 = FFh (Internal test/diagostic registers should not be written)
3. Write 1b to R12[7] to assert device soft-reset. This does not reset the register values.
4. Write 0b to R12[7] to exit soft-reset and begin the PLL start-up sequence.
5. See *EEPROM Programming Using Method #1 (Register Commit)* to store the active configuration to the EEPROM to enable auto-startup on the next power cycle.

9.5.6 EEPROM Programming Flow

Before the EEPROM can be programmed, it is necessary to program the desired configuration to the SRAM through the memory control registers. The register data can be written to the SRAM by transferring the active register configuration internally using Method #1, or by direct writes to the SRAM using Method #2.

- **Method #1** (Register Commit) requires the active registers be first programmed to the desired configuration, but does not require knowledge of the SRAM/EEPROM map.
- **Method #2** (Direct Writes) bypasses any writes to the active registers, allowing the device to continue normal operation without disruption while the SRAM/EEPROM are programmed.

The programming flow for the two methods are different and described as follows.

9.5.6.1 EEPROM Programming Using Method #1 (Register Commit)

This sequence can be followed to program the SRAM and EEPROM using the active register configuration.

1. Program the desired configuration to the active registers (see *General Register Programming Sequence*). This requires the register settings in the register map format.
2. *Write SRAM Using Register Commit*.
3. *Program EEPROM*.

Programming (continued)

9.5.6.1.1 Write SRAM Using Register Commit

The SRAM array is volatile shadow memory mapped to a subset of the active configuration registers and is used to program the EEPROM.

Once the active registers have been programmed, the data can be internally committed to the SRAM with a single register transaction:

1. Write 40h to R157 (REGCOMMIT bit, self-clearing). This commits the current register data to the SRAM internally.
2. (optional) Program any of the user-programmable fields to SRAM. See *User-Programmable Fields In EEPROM*. This step should not precede the prior step.

9.5.6.1.2 Program EEPROM

The EEPROM array is non-volatile memory mapped directly from the SRAM array.

After the register settings have been written to the SRAM (by either Method #1 or #2), the EEPROM can be programmed through the following sequence:

1. Write EAh to R164 (NVMUNLK). This unlocks the EEPROM to allow programming.
2. Write 03h to R157 (NVM_ERASE_PROG bits). This programs the EEPROM from the entire contents of the SRAM. The total erase/program cycle takes about 230 ms.
   - **NOTE**: Steps 1 and 2 must be atomic writes without any other register transactions in-between.
3. (optional) Read or poll R157[2] (NVMBUSY bit). When this bit cleared, the EEPROM programming is done.
4. (optional) Write 00h to R164. This locks the EEPROM to protect against inadvertent programming.

On the next power-up or hard-reset, the device can self-start in EEPROM mode from the newly programmed configuration. Also, the NVMCNT register value will be incremented by 1 after power-up or hard-reset to reflect total number of EEPROM programming cycles completed successfully.

9.5.6.2 EEPROM Programming Using Method #2 (Direct Writes)

This sequence can be followed to program the EEPROM by writing the SRAM directly to avoid disruption to the current device operation. This requires the register settings in the SRAM/EEPROM map format.

1. *Write SRAM Using Direct Writes*.
2. *Program EEPROM*.

9.5.6.2.1 Write SRAM Using Direct Writes

This SRAM direct write method can be used if it is required to store a different device configuration to EEPROM without disrupting the current operational state of the device. This method requires that the SRAM/EEPROM map data is already generated, which can be exported by TICS Pro.

The SRAM can be directly written *without modifying the active configuration registers* through the following sequence:

1. Write the most significant five bits of the SRAM address to R159 (MEMADR byte 1) and write the least significant eight bits of the SRAM address to R160 (MEMADR byte 0).
2. Write the SRAM data byte to R162 (RAMDAT byte) for the address specified in the previous step in the same register transaction.
   - Any additional write (or read) transfers in same transaction will cause the SRAM address pointer to be auto-incremented and a subsequent write (or read) will take place at the next SRAM address.
   - Byte or Block write transfers to R162 can be used to write the entire SRAM map sequentially from Byte 0 to 252.
     - Bytes 253 to 255 must not be modified or overwritten and shall be reserved for TI internal use only.
   - Alternatively, it is valid to write R159 and R160 to set the memory address pointer explicitly before each write to R162.
   - Access to the SRAM will terminate at the end of current write transaction.
   - Note that reading the RAMDAT register will also cause the memory address pointer to be auto-incremented.

Programming (continued)

9.5.6.2.2 User-Programmable Fields In EEPROM

表 9 summarizes the address of several user-programmable bytes in EEPROM. These bytes can be written using the SRAM direct write method prior to programming the EEPROM. It is optional to modify these bytes from their factory default settings.

表 9. User-Programmable Fields

ADDRESS BYTE # (DECIMAL)	FIELD NAME	DESCRIPTION
5	SLAVEADR[7:0]	**I^2C Slave Address MSB Bits [7:3].** Bits [7:3] can be written to set the five MSBs of the 7-bit slave address. Bits [2:0] should be written with zeros. The two LSBs of the 7-bit address are determined by the control pins on device start-up. Default SLAVEADR[7:0] value = C8h (corresponds to 7-bit address of 64h). After the EEPROM is programmed and a subsequent POR cycle, the SLAVEADR value stored in EEPROM can be read from R10.
11	EEREV[7:0]	**EEPROM Image Revision.** This byte can be written to set the EEPROM image revision number or any customer-specific data for part traceability. After the EEPROM is programmed and a subsequent POR cycle, the EEREV value stored in EEPROM can be read from R11.
249	NVM_SPARE_BY0[7:0]	**NVM Spare Bytes.** These four bytes can be written with any customer-specific data for part traceability. After the EEPROM is programmed, these bytes can be read directly from EEPROM (see *Read EEPROM*).
250	NVM_SPARE_BY1[7:0]	
251	NVM_SPARE_BY2[7:0]	
252	NVM_SPARE_BY3[7:0]	

9.5.7 Read SRAM

The contents of the SRAM can be read back, one word at a time, starting with that of the requested address through the following sequence. This sequence can be used to verify the contents of the SRAM before it is transferred to the EEPROM during an EEPROM program cycle.

1. Write the most significant five bits of the SRAM address to R159 (MEMADR byte 1) and write the least significant eight bits of the SRAM address to R160 (MEMADR byte 0).
2. Read R162 (RAMDAT byte) to fetch the SRAM data byte from the address specified in the previous step in the same register transaction.
   - Any additional read transfers that are part of the same transaction will cause the SRAM address to auto-increment and a subsequent read will take place at the next SRAM address.
   - Byte or Block read transfers from R162 can be used to read the entire SRAM map sequentially from Byte 0 to 252.
   - Access to SRAM will terminate at the end of current register transaction.

9.5.8 Read EEPROM

The contents of the EEPROM can be read back, one word at a time, starting with that of the requested address through the following sequence. This sequence can be used to verify the EEPROM contents after the last successful program cycle.

1. Write the most significant five bit of the EEPROM address in R159 (MEMADR byte 1) and write the least significant eight bits of the EEPROM address in R160 (MEMADR byte 0).
2. Read R161 (NVMDAT byte) to fetch the EEPROM data byte from the address specified in the previous step in the same register transaction.
   - Any additional read transfer that is part of the same transaction will cause the EEPROM address pointer to be auto-incremented and a subsequent read will take place of the next address.
   - Byte or Block read transfers from R161 can be used to read the entire EEPROM map sequentially from Byte 0 to 252.
   - Access to EEPROM will terminate at the end of current register transaction.

9.5.9 EEPROM Start-Up Mode Default Configuration

The generic LMK05318 device is factory pre-programmed with the EEPROM default configuration in 表 10. A different start-up configuration can be stored to the EEPROM through in-system programming.

表 10. LMK05318 EEPROM Start-Up Default Configuration

SYSTEM CLOCK	FREQUENCY (MHz)	INPUT TYPE	XO DOUBLER
XO	48.0048	AC-DIFF(ext. term)	Disabled
CLOCK INPUTS	**FREQUENCY (MHz)**	**INPUT TYPE**	**AUTO PRIORITY**
PRIREF	25	AC-DIFF(ext. term)	1st
SECREF	25	AC-DIFF(ext. term)	2nd
INPUT SELECTION	**INPUT SELECT MODE**	**MANUAL SELECTION MODE**	**MANUAL REGISTER SELECTION**
DPLL	Manual with Auto-Fallback	Pin Select	PRIREF
CLOCK OUTPUTS	**FREQUENCY (MHz)**	**OUTPUT MUX**	**OUTPUT TYPE**
OUT0	156.25	PLL 1	Disabled
OUT1	156.25	PLL 1	Disabled
OUT2	156.25	PLL 1	AC-LVPECL
OUT3	156.25	PLL 1	AC-LVPECL
OUT4	156.25	PLL 1	Disabled
OUT5	156.25	PLL 1	Disabled
OUT6	25	PLL 1	AC-LVPECL
OUT7	100	PLL 1	HCSL (ext. 50-Ω term.)
PLL CONFIGURATION	**PLL MODE**	**LOOP BW (Hz)**	**TDC or PFD RATE (MHz)**
DPLL	DPLL Mode	100	25
APLL1	DPLL Mode	1000	24.0048
APLL2	Disabled	–	–
REF INPUT MONITORS (1)	**VALIDATION TIMER (s)**	**FREQ DET VALID (ppm)**	**FREQ DET INVALID (ppm)**
PRIREF	0.1	-	-
SECREF	0.1	-	-
REF INPUT MONITORS (2)	**EARLY DETECT WINDOW (ns)**	**LATE DETECT WINDOW (ns)**	**1-PPS JITTER THRESHOLD (µs)**
PRIREF	33.6	46.4	–
SECREF	33.6	46.4	–
FREQUENCY LOCK DETECT	**LOCK (ppm)**	**UNLOCK (ppm)**	**ACCURACY (ppm)**
DPLL	1	10	1
DCO MODE	**DCO CONTROL**	**STEP SIZE (ppb)**	**FINC/FDEC MODE**
DPLL	DCO Disabled	–	Register bit
ZERO-DELAY MODE	**DPLL ZDM SYNC**	**PHASE OFFSET (ns)**	
REF-to-OUT7	ZDM Disabled	–	
STATUS PINS	**SIGNAL**	**TYPE**	**POLARITY**
STATUS0	DPLL Loss of Frequency Lock	3.3-V LVCMOS	Active High
STATUS1	DPLL Holdover Active	3.3-V LVCMOS	Active High

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Device Start-Up Sequence

The device start-up sequence is shown in 図 61.

Application Information (continued)

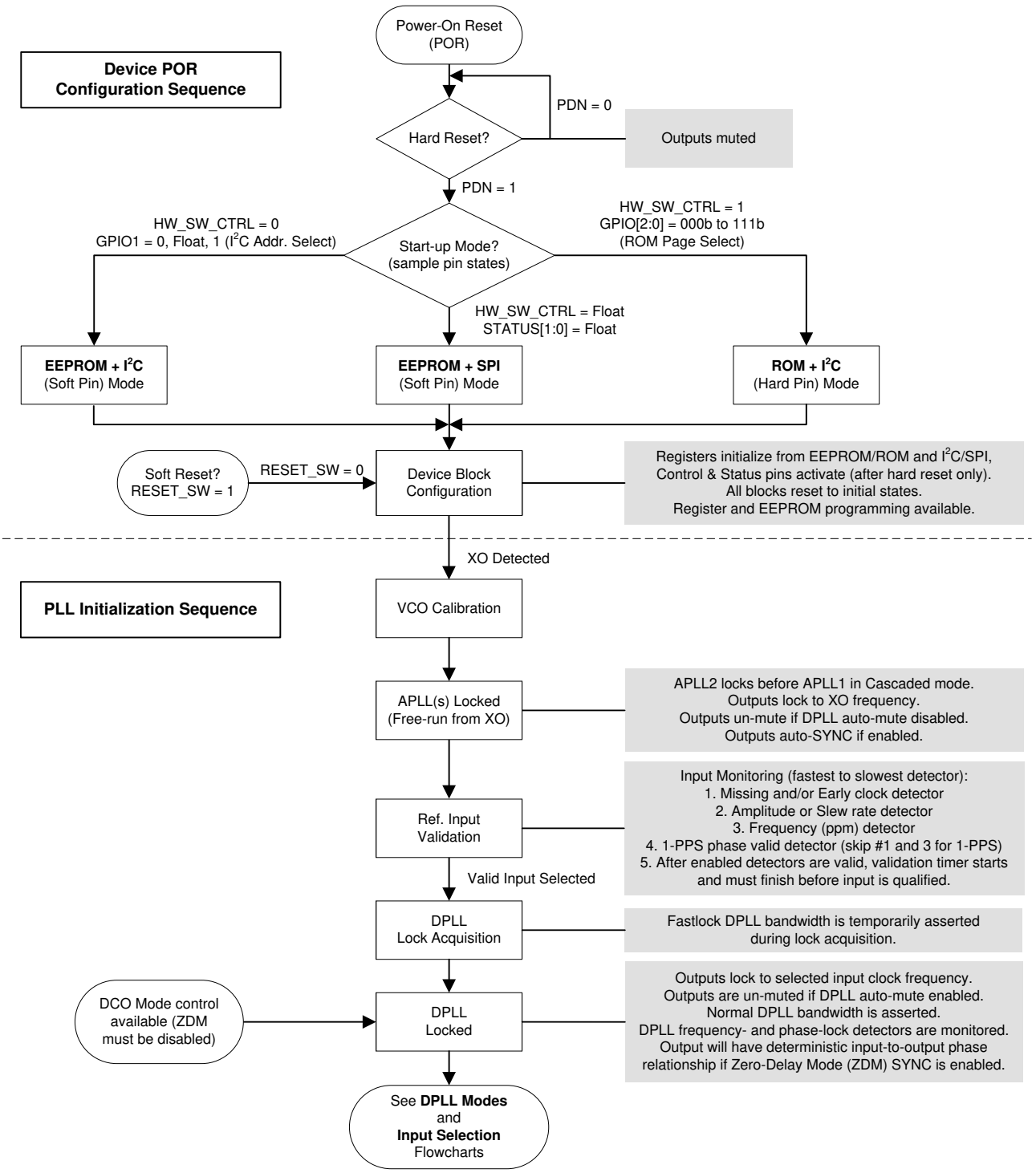


図 61. Device Start-Up Sequence

Application Information (continued)

10.1.2 Power Down (PDN) Pin

The PDN pin (active low) can be used for device power down and used to initialize the POR sequence. When PDN is pulled low, the entire device is powered down and the serial interface is disabled. When PDN is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in 図 61. If the PDN pin is toggled to issue a momentary hard-reset, the negative pulse applied to the PDN pin should be greater than 200 ns to be captured by the internal digital system clock.

表 11. PDN Control

PDN PIN STATE	DEVICE OPERATION
0	Device is disabled
1	Normal operation

10.1.3 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

10.1.3.1 Mixing Supplies

The LMK05318 incorporates flexible power supply architecture. While all VDD core supplies should be powered by the same 3.3-V rail, the individual output supplies can be powered from separate 1.8-V, 2.5-V, or 3.3-V rails. This can allow all VDDO output supplies to operate at 1.8 V to minimize power consumption.

10.1.3.2 Power-On Reset (POR) Circuit

The LMK05318 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All VDD core supplies have ramped above 2.72 V
- PDN pin has ramped above 1.2 V (minimum V_{IH})

10.1.3.3 Powering Up From a Single-Supply Rail

As long as all VDD core supplies are driven by the same 3.3-V supply rail that ramp in a monotonic manner from 0 V to 3.135 V, irrespective of the ramp time, then there is no requirement to add a capacitor on the PDN pin to externally delay the device power-up sequence. As shown in 図 62, the PDN pin can be left floating or otherwise driven by a system host to meet the clock sequencing requirements in the system.

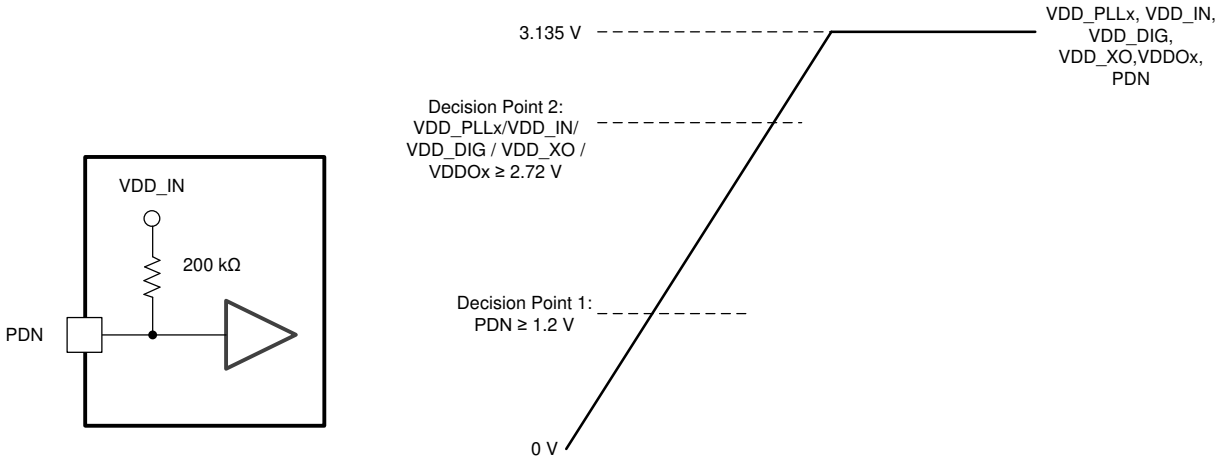


図 62. Recommendation for Power Up From a Single-Supply Rail

10.1.3.4 Power Up From Split-Supply Rails

If some VDD core supplies are driven from different supply rails, TI recommends to start the PLL calibration after all of the core supplies have ramped above 3.135 V. This can be realized by delaying the PDN low-to-high transition. The PDN input incorporates a 200-kΩ resistor to VDD_IN and as shown in 図 63, a capacitor from the PDN pin to GND can be used to form an R-C time constant with the internal pullup resistor. This R-C time constant can be designed to delay the low-to-high transition of PDN until all the core supplies have ramped above 3.135 V.

Alternatively, the PDN pin can be driven high by a system host or power management device to delay the device power-up sequence until all VDD supplies have ramped.

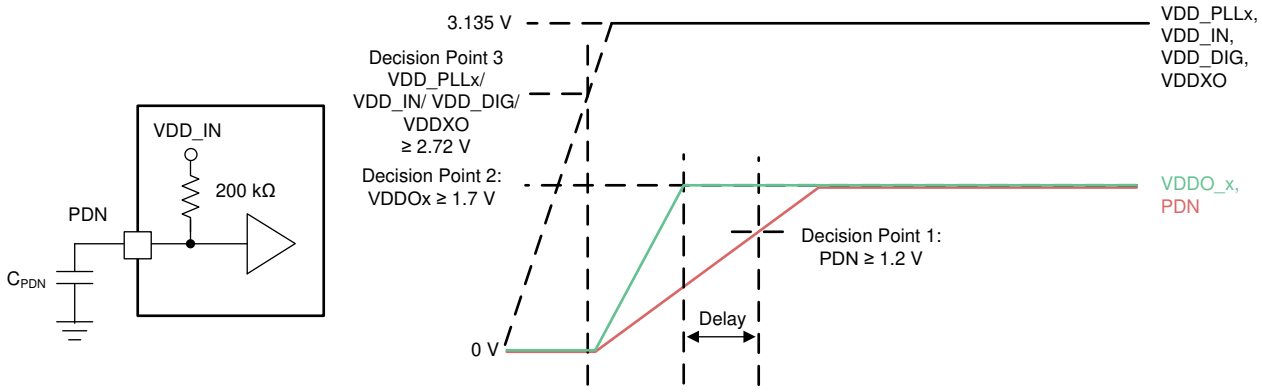


図 63. Recommendation for Power Up From Split-Supply Rails

10.1.3.5 Non-Monotonic or Slow Power-Up Supply Ramp

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0 V to 3.135 V of over 100 ms, TI recommends to delay the VCO calibration until after all of the core supplies have ramped above 3.135 V. This could be achieved by delaying the PDN low-to-high transition with one of the methods described in *Power Up From Split-Supply Rails*.

If any core supply cannot ramp above 3.135 V before the PDN low-to-high transition, it is acceptable to issue a device soft-reset after all core supplies have ramped to manually trigger the VCO calibration and PLL start-up sequence.

10.1.4 Slow or Delayed XO Start-Up

Because the external XO clock input is used as the reference input for the VCO calibration, the XO input amplitude and frequency must be stable before the start of VCO calibration to ensure successful PLL lock and output start-up. If the XO clock is not stable prior to VCO calibration, the VCO calibration can fail and prevent PLL lock and output clock start-up.

If the XO clock has a slow start-up time or has glitches on power-up (due to a slow or non-monotonic power supply ramp, for example), TI recommends to delay the start of VCO calibration until after the XO is stable. This could be achieved by delaying the PDN low-to-high transition until after the XO clock has stabilized using one of the methods described in *Power Up From Split-Supply Rails*. It is also possible to issue a device soft-reset after the XO clock has stabilized to manually trigger the VCO calibration and PLL start-up sequence.

10.2 Typical Application

図 64 shows a reference schematic to help implement the LMK05318 and its peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS, AC-coupled differential, and HCSL clock interfacing examples are shown for the clock input and output pins. An external LVCMOS oscillator drives an AC-coupled voltage divider network as an example to interface the 3.3-V LVCMOS output to meet the input voltage swing specified for the XO input. The required external capacitors are placed close to the LMK05318 and are shown with the suggested values. External pullup and pulldown resistor options at the logic I/O pins set the default input states. The I^2C or SPI pins and other logic I/O pins can be connected to a host device (not shown) to program and control the LMK05318 and monitor its status. This example assumes the device will start up from EEPROM mode with an I^2C interface (HW_SW_CTRL = 0).

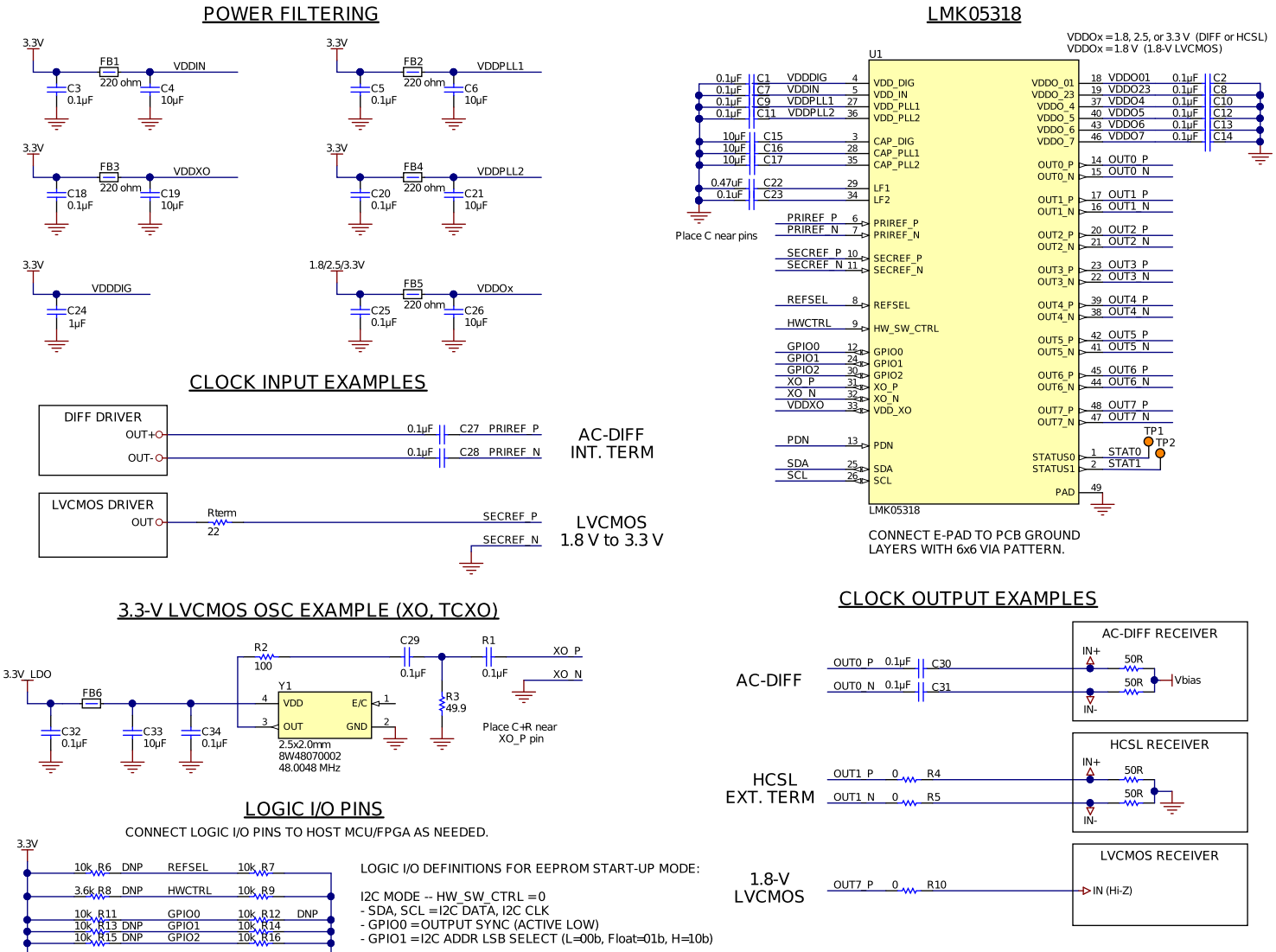


図 64. LMK05318 Reference Schematic Example

10.2.1 Design Requirements

In a typical application, consider the following design requirements or parameters to implement the overall clock solution:

1. Device initial configuration. The device should be configured as either host programmed (MCU or FPGA) or factory pre-programmed.
2. Device start-up mode and serial interface. Typically, this will be EEPROM + I^2C or SPI mode.
3. XO frequency, signal type, and frequency accuracy and stability. Consider a high-stability TCXO or OCXO for the XO input if any of the following is required:
   – Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
   – Lowest possible close-in phase noise at offsets ≤ 100 Hz
   – Narrow DPLL bandwidth ≤ 10 Hz
4. For the DPLL/APLL1 domain, determine the following:
   – Input clocks: frequency, buffer mode, priority, and input selection mode
   – Output clocks: frequency, buffer mode
   – DPLL loop bandwidth and maximum TDC frequency
   – If the DCO Mode or Zero-Delay Mode is required
5. For the APLL2 domain, determine the following:
   – APLL2 reference: VCO1 for synchronous clocking with Cascaded APLL2, or XO for asynchronous clocking with Non-cascaded APLL2
   – Output clocks: frequency, buffer mode
6. Input clock and PLL monitoring options
7. Status outputs and interrupt flag
8. Power supply rails

10.2.2 Detailed Design Procedure

In a typical application, TI recommends the following steps:

1. Use the LMK05318 GUI in the TICS Pro programming software for a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (in hex format) to enable host programming or factory pre-programming.
   – If using a generic (non-custom) device, a host device can program the register settings through the serial interface after power-up and issue a soft-reset (by RESET_SW bit) to start the device. The host can also store the settings to the EEPROM to allow automatic start-up with these register settings on subsequent power-on reset cycles.
   – Alternatively, a LMK05318 setup file for TICS Pro (.tcs) can be sent to TI to support factory pre-programmed samples.
2. Tie the HW_SW_CTRL pin to ground to select EEPROM+I^2C mode, or bias the pin to V_{IM} through the weak internal resistors or external resistors to select EEPROM+SPI mode. Determine the logic I/O pin assignments for control and status functions. See *Device Start-Up Modes*.
   – Connect I^2C/SPI and logic I/O pins (1.8-V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select an XO frequency by following *Oscillator Input (XO_P/N)*.
   – Choose an XO with target phase jitter performance that meets the frequency stability and accuracy requirements required for the output clocks during free-run or holdover.
   – For a 3.3-V LVCMOS driver, follow the OSC clock interface example in 図 64. Power the OSC from a low-noise LDO regulator or optimize its power filtering to avoid supply noise-induced jitter on the XO clock.
   – **TICS Pro:** Configure the XO input buffer mode to match the XO driver interface requirements. See 表 2.

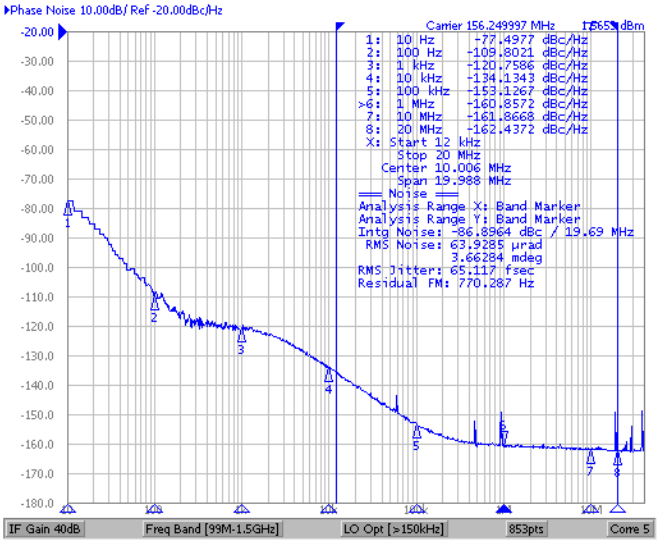
4. Wire the clock I/O for each PLL domain in the schematic and use TICS Pro to configure the device settings as follows:
   - Reference inputs: Follow the LVCMOS or differential clock input interface examples in 図 64 or *Clock Input Interfacing and Termination*.
     - **TICS Pro:** For DPLL mode, configure the reference input buffer modes to match the reference clock driver interface requirements. See 表 3.
     - LVCMOS clock input should be used for input frequencies below 5 MHz when amplitude monitoring is enabled.
   - **TICS Pro:** For DPLL mode, configure the DPLL input selection modes and input priorities. See *Reference Input Mux Selection*.
   - **TICS Pro:** If APLL2 is used, configure the APLL2 reference for VCO1 domain (Cascaded APLL2) or XO clock (Non-cascaded APLL2).
   - **TICS Pro:** Configure each output with the required clock frequency and PLL domain. TICS Pro can calculate the VCO frequencies and divider settings for the PLL and outputs. Consider the following output clock assignment guidelines to minimize crosstalk and spurs:
     - OUT[0:3] bank is preferred for PLL1 clocks.
     - OUT[4:7] bank is preferred for PLL2 clocks.
     - Group identical output frequencies (or harmonic frequencies) on adjacent channels, and use the output pairs with a single divider (OUT0/1 or OUT2/3) when possible to minimize power.
     - Separate clock outputs when the difference of the two frequencies, $|f_{OUTx} – f_{OUTy}|$, falls within the jitter integration bandwidth (12 kHz to 20 MHz, for example). Any outputs that are potential aggressors should be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation.
     - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If an LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace.
     - If not all outputs pairs are used in the application, consider connecting an unused output to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP ports).
   - **TICS Pro:** Configure the output drivers.
     - Configure the output driver modes to match the receiver clock input interface requirements. See 表 7.
     - Configure any output SYNC groups that need their output phases synchronized. See *Output Synchronization (SYNC)*.
     - Configure the output auto-mute modes, output mute levels, and APLL and DPLL mute options. See *Output Auto-Mute During LOL*.
   - Clock output Interfacing: Follow the single-ended or differential clock output interface examples in 図 64 or *Clock Output Interfacing and Termination*.
     - Differential outputs should be AC-coupled and terminated and biased at the receiver inputs.
     - HCSL outputs should have 50-Ω termination to GND (at source or load side) unless the internal source termination is enabled by programming.
     - LVCMOS outputs have internal source termination to drive 50-Ω traces directly. LVCMOS V_{OH} level is determined by VDDO voltage (1.8 V).
   - **TICS Pro:** Configure the DPLL loop bandwidth.
     - Below the loop bandwidth, the reference noise is added to the TDC noise floor and the XO/TCXO/OCXO noise. Above the loop bandwidth, the reference noise will be attenuated with roll-off up to 60 dB/decade. The optimal bandwidth depends on the relative phase noise between the reference input and the XO. APLL1's loop bandwidth can be configured to provide additional attenuation of the reference input, TDC, and XO phase noise above APLL1's bandwidth (typically around 1 kHz).
   - **TICS Pro:** Configure the maximum TDC frequency to optimize the DPLL TDC noise contribution for the desired use case.
     - *Wired*: The maximum TDC rate is preset to 400 kHz. This supports SyncE and other use cases using a narrow loop bandwidth (≤10 Hz) with a TCXO/OCXO/XO to set the frequency stability and wander performance.

  - *Wireless*: The maximum TDC rate is preset to 26 MHz for lowest in-band TDC noise contribution. This supports wireless and other use cases where close-in phase noise is critical.
  - *Custom*: The maximum TDC rate can be specified for any value up to 26 MHz.
- **TICS Pro:** If clock steering is needed (such as for IEEE 1588 PTP), enable DCO mode for the DPLL loop and enter the frequency step size (in ppb). The FDEV step register will be computed according to *DCO Frequency Step Size*. Enable the FINC/FDEC pin control on the GPIO pins if needed.
- **TICS Pro:** If deterministic input-to-output clock phase is needed for 1-PPS input and 1-PPS output (on OUT7), enable the ZDM and OUT7 divider synchronization features. See *Zero-Delay Mode (ZDM) Synchronization for 1-PPS Input and Output*.

5. **TICS Pro:** Configure the reference input monitoring options for each reference input. Disable the monitor when not required or when the input operates beyond the monitor's supported frequency range. See *Reference Input Monitoring*.
   - *Amplitude monitor*: Set the LVCMOS detected slew rate edge or the differential input amplitude threshold to monitor input signal quality. Disable the monitor for a differential input below 5 MHz or else use an LVCMOS input clock.
   - *Frequency monitor*: Set the valid and invalid thresholds (in ppm).
   - *Missing pulse monitor*: Set the late window threshold (T_{LATE}) to allow for the longest expected input clock period, including worst-case cycle-to-cycle jitter. For a gapped clock input, set T_{LATE} based on the number of allowable missing clock pulses.
   - *Runt pulse monitor*: Set the early window threshold (T_{EARLY}) to allow for the shortest expected input clock period, including worst-case cycle-to-cycle jitter.
   - *1-PPS Phase validation monitor*: Set the phase validation jitter threshold, including worst-case input cycle-to-cycle jitter.
   - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
6. **TICS Pro:** Configure the DPLL lock detect and tuning word history monitoring options for each channel. See *PLL Lock Detectors* and *Tuning Word History*.
   - *DPLL tuning word history*: Set the history count/averaging time (T_{AVG}), history delay/ignore time (T_{IGN}), and intermediate averaging option.
   - *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.
7. **TICS Pro:** Configure each status output pin and interrupt flag as needed. See *Status Outputs* and *Interrupt*.
   - Select the desired status signal selection, status polarity, and driver mode (3.3-V LVCMOS or open-drain). Open-drain requires an external pullup resistor.
   - If the Interrupt is enabled and selected as a status output, configure the flag polarity and the mask bits for any interrupt source, and the combinational AND/OR gate as needed.
8. Consider the following guidelines for designing the power supply:
   - Outputs with identical frequency or integer-related (harmonic) frequencies can share a common filtered power supply.
     - Example: 156.25-MHz and 312.5-MHz outputs on OUT[0:1] and OUT[2:3] can share a filtered VDDO supply (Group 1), while 100-MHz, 50-MHz, and 25-MHz outputs on OUT[4:7] can share a separate VDDO supply (Group 2).
   - For lowest power, AC-DIFF or HCSL outputs can be powered from a 1.8-V supply with no degradation in output swing or phase noise (compared to 2.5 V or 3.3 V).
   - 1.8-V LVCMOS outputs should be powered from a 1.8-V supply.
   - See *Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains*.

10.2.3 Application Curves

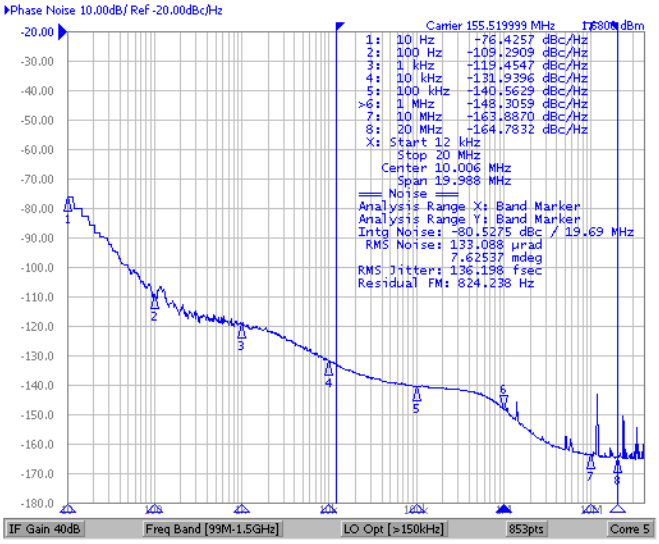
Unless otherwise noted, test conditions are the same as in *Typical Characteristics*. 156.25-MHz output (APLL1) on OUT3 and 155.52 MHz output (APLL2) on OUT4 running simultaneously to demonstrate minimal coupling between the PLL domains and minimal degradation in phase noise and jitter. Device operating in DPLL Mode with Cascaded APLL2. AC-LVPECL outputs measured.



Jitter = 65 fs RMS (12 kHz to 20 MHz)

f_{VCO1} = 2500 MHz (VCO1 inverted)

図 65. 156.25-MHz Output Phase Noise (OUT3) With 155.52-MHz Output Enabled (OUT4)



Jitter = 136 fs RMS (12 kHz to 20 MHz)

f_{VCO2} = 6065.28 MHz (VCO2 post-divider = 3)

図 66. 155.52-MHz Output Phase Noise (OUT4) With 156.25-MHz Output Enabled (OUT3)

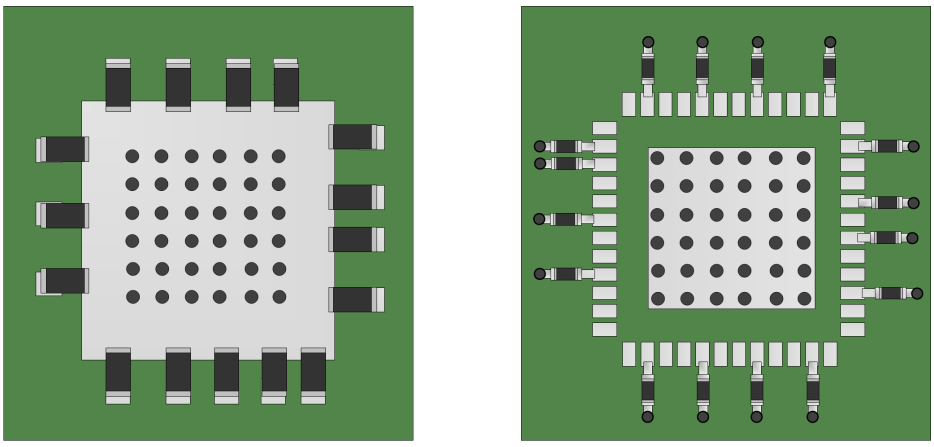
10.3 Do's and Don'ts

- Power all the VDD pins with proper supply decoupling and bypassing connect as shown in 図 64.
- Power down unused blocks through registers to minimize power consumption.
- Use proper source or load terminations to match the impedance of input and output clock traces for any active signals to/from the device.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- For EEPROM+SPI Mode: Leave HW_SW_CTRL and STATUS[1:0] pins floating during POR to ensure proper start-up. These pins has internal biasing to V_{IM} internally.
  - If HW_SW_CTRL or either STATUS pin is connected to a system host (MCU or FPGA), the host device must be configured with high-impedance input (no pullup or pulldown resistors) to avoid conflict with the internal bias to V_{IM}. If needed, external biasing resistors (10-kΩ pullup to 3.3 V and 3.3-kΩ pulldown) can be connected on each STATUS pin to bias the inputs to V_{IM} during POR.
- Consider routing each STATUS pin to a test point or high-impedance input of a host device to monitor device status outputs.
- Consider using a LDO regulator to power the external XO/TCXO/OCXO source.
  - High jitter and spurious on the oscillator clock are often caused by high spectral noise and ripple on its power supply.
- Include dedicated header to access the I^2C or SPI interface of the device, as well as a header pin for ground.
  - This can enabled off-board programming for device bring-up, prototyping, and diagnostics using the TI USB2ANY interface and TICS Pro software tools.

11 Power Supply Recommendations

11.1 Power Supply Bypassing

図 67 shows two general placements of power supply bypass capacitors on either the back side or the component side of the PCB. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component side and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.



(**Does not** indicate actual location of the LMK05318 supply pins)

図 67. Generalized Placement of Power Supply Bypass Capacitors

11.2 Device Current and Power Consumption

The device power consumption is dependent on the actual configuration programmed to the device. The individual supply pin current consumption values in *Electrical Characteristics* can be used to estimate device power consumption and power supply dimensioning.

11.2.1 Current Consumption Calculations

Core supply currents:

$$IDD\_CORE = IDD\_DIG + IDD\_IN + IDD\_XO + IDD\_PLL1 + IDD\_PLL2 \quad (13)$$

OUT[0:1] or OUT[2:3] channel supply current:

$$IDDO\_XY = IDDO\_XY_{DIVIDER} + IDDO\_X_{DRIVER} + IDDO\_Y_{DRIVER} \quad (14)$$

OUT[4:7] channel supply current:

$$IDDO\_X = IDDO\_X_{DIVIDER} + IDDO\_X_{DRIVER} \quad (15)$$

When an output channel's divider and drivers are disabled, its IDDO_x equals approximately 0 mA.

11.2.2 Power Consumption Calculations

Core power consumption:

$$P_{CORE} = IDD\_CORE \times VDD \quad (16)$$

Output power consumption:

$$P_{OUT} = (IDDO\_01 \times VDDO\_01) + (IDDO\_23 \times VDDO\_23) + ... + (IDDO\_7 \times VDDO\_7) \quad (17)$$

Total device power consumption:

$$P_{TOTAL} = P_{CORE} + P_{OUT} \quad (18)$$

11.2.3 Example

Estimate the current and power consumption for the following device configuration:

- VDD = 3.3 V and VDDO_x = 1.8 V
- DPLL/APLL1 mode with Cascaded APLL2
- XO: 48 MHz, PRIREF and SECREF: 25 MHz
- OUT[0:1]: 156.25 MHz AC-LVPECL (x2), PLL1
- OUT[2:3]: 156.25 MHz AC-CML (x2), PLL1
- OUT4: 133.33 MHz AC-LVDS, PLL2
- OUT5: Disabled
- OUT6: 100 MHz HCSL, PLL1
- OUT7: 25 MHz LVCMOS (x2), PLL1

From 式 13: IDD_CORE = 18 + 38 + 20 + 110 + 120 = 306 mA

From 式 14 and 式 15:

- IDDO_01 = 70 + 16 + 16 = 102 mA
- IDDO_23 = 70 + 14 + 14 = 98 mA
- IDDO_4 = 70 + 10 = 80 mA
- IDDO_5 = 0 mA
- IDDO_6 = 70 + 25 = 95 mA
- IDDO_7 = 70 + 6 = 76 mA

From 式 16: P_{CORE} = 306 mA × 3.3 V = 1.01 W

From 式 17: P_{OUT} = (102 + 98 + 80 + 95 + 76) mA × 1.8 V = 0.812 W

From 式 18: P_{TOTAL} = 1.01 W + 0.812 W = 1.822 W

12 Layout

12.1 Layout Guidelines

- Isolate input, XO/OCXO/TCXO and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO/OCXO/TCXO placement and layout in terms of the supply/ground noise and thermal gradients from nearby circuitry (for example, power supplies, FPGA, ASIC) as well as system-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillator.
- Avoid impedance discontinuities on controlled-impedance 50-Ω single-ended (or 100-Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the IC, or directly below the IC pins on the opposite side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- Use multiple vias to connect wide supply traces to the respective power islands or planes if possible.
- Use at least a 5×5 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.
- See the Land Pattern Example, Solder Mask Details, and Solder Paste Example in the *メカニカル、パッケージ、および注文情報*.

12.2 Layout Example

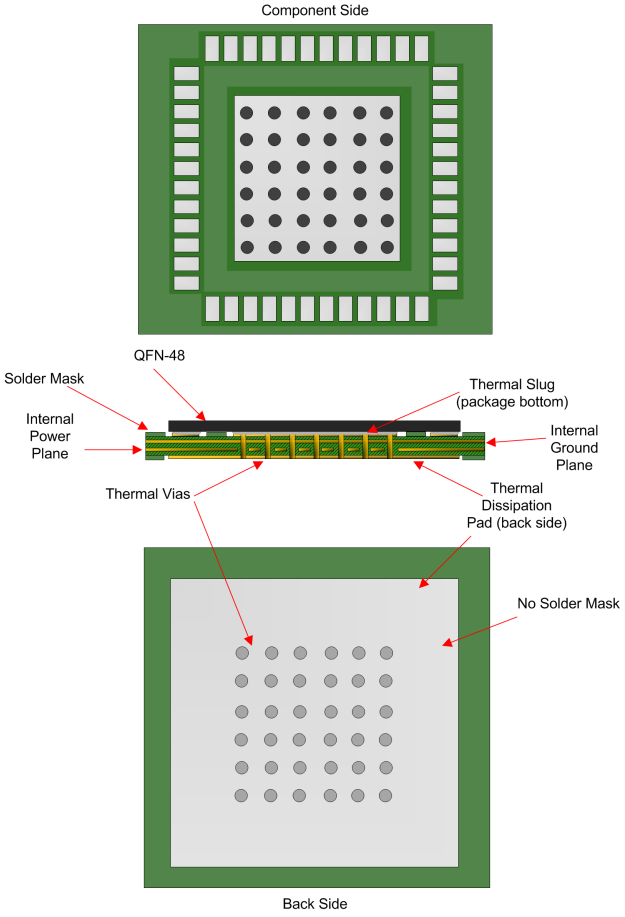


図 68. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended)

12.3 Thermal Reliability

The LMK05318 is a high-performance device. To ensure good electrical and thermal performance, TI recommends to design a thermally-enhanced interface between the IC ground/thermal pad and the PCB ground using at least a 5×5 through-hole via pattern connected to multiple PCB ground layers as shown in 図 68.

12.3.1 Support for PCB Temperature up to 105°C

The device can maintain a safe junction temperature below the recommended maximum value of 125°C even when operated on a PCB with a maximum board temperature (T_{PCB}) of 105 °C. This can shown by the following example calculation, which assumes the total device power (P_{TOTAL}) computed with all blocks enabled using the typical current consumption from the *Electrical Characteristics* (VDD = 3.3 V, VDDO = 1.8 V) and the thermal data in *Thermal Information: 10-Layer Custom PCB* with no airflow.

$$T_J = T_{PCB} + (\Psi_{JB} \times P_{TOTAL}) = \mathbf{113.8\ °C} \quad (19)$$

where

- T_{PCB} = 105 °C
- Ψ_{JB} = 4.4 °C/W
- $P_{TOTAL} = P_{CORE} + P_{OUTPUT}$ = 2.0 W
  - P_{CORE} = (18 + 38 + 20 + 110 + 120) mA × 3.3 V = 1.01 W
    - DPLL, APLL1, APLL2, and all Inputs enabled
  - P_{OUTPUT} = (102 + 102 + 86 + 86 + 86 + 86) mA × 1.8 V = 0.986 W
    - All output channels enabled with output divider values > 6 and AC-LVPECL output types

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 TICS Pro

TICS　Proは、EVMプログラミングおよびレジスタ・マップ生成用オフライン・ソフトウェア・ツールであり、個々の用途に合わせてデバイス構成をプログラミングできます。TICS Proについては、www.ti.com/tool/TICSPRO-SWを参照してください。

13.1.2 関連資料

以下を参照してください。

- *『LMK05318のITU-T G.8262準拠テスト結果』*(SNAA316)
- *『LMK05318でサポートされる同期モード』*(SNAA324)
- *『LMK05318での高速56G PAM-4シリアル・リンクのクロッキング』*(SNAA325)
- *『LMK05318EVMユーザー・ガイド』*(SNAU236)

13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.4 商標

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13.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

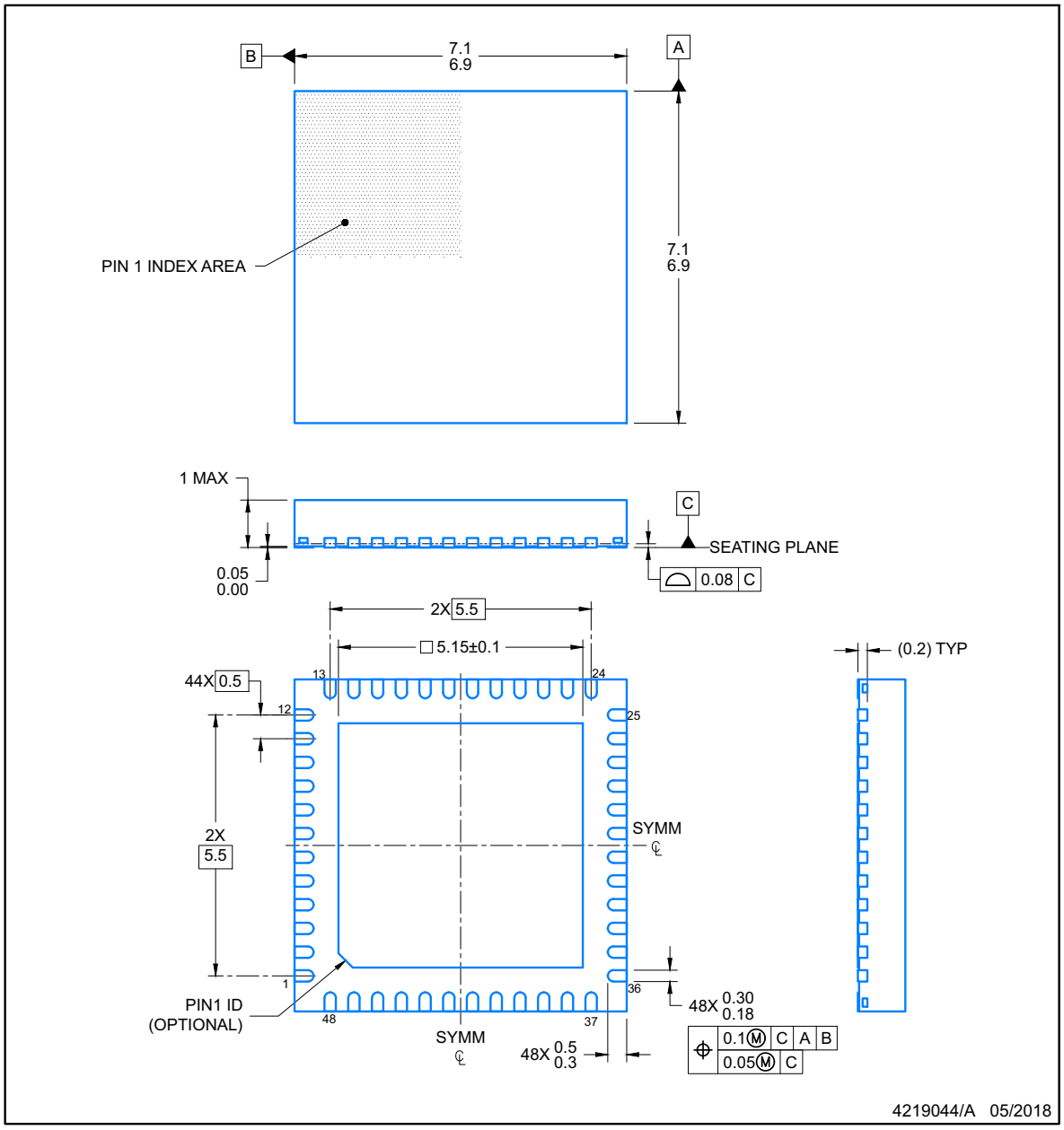
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OUTLINE

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



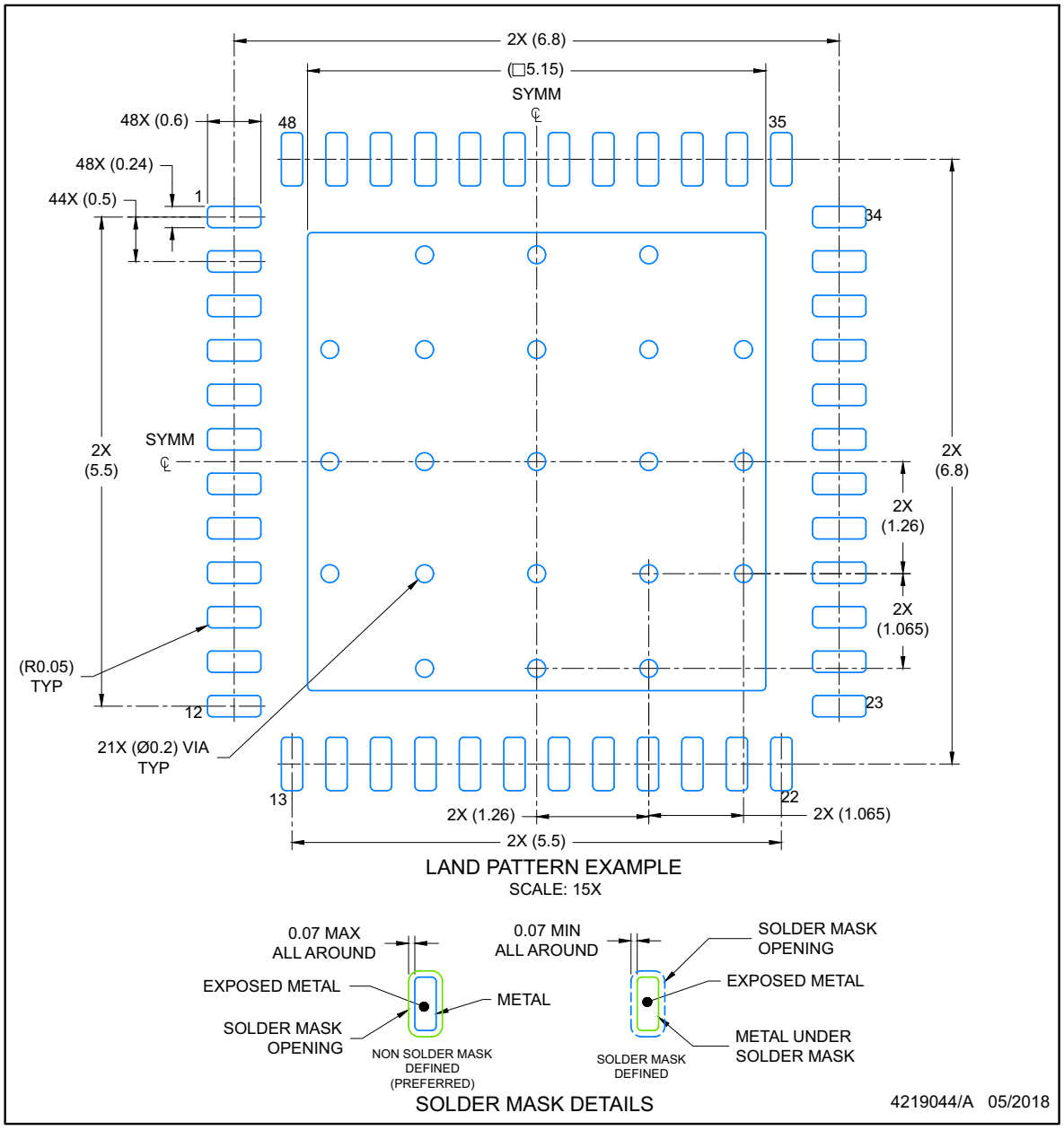
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048A — **VQFN - 1 mm max height**

PLASTIC QUADFLAT PACK- NO LEAD



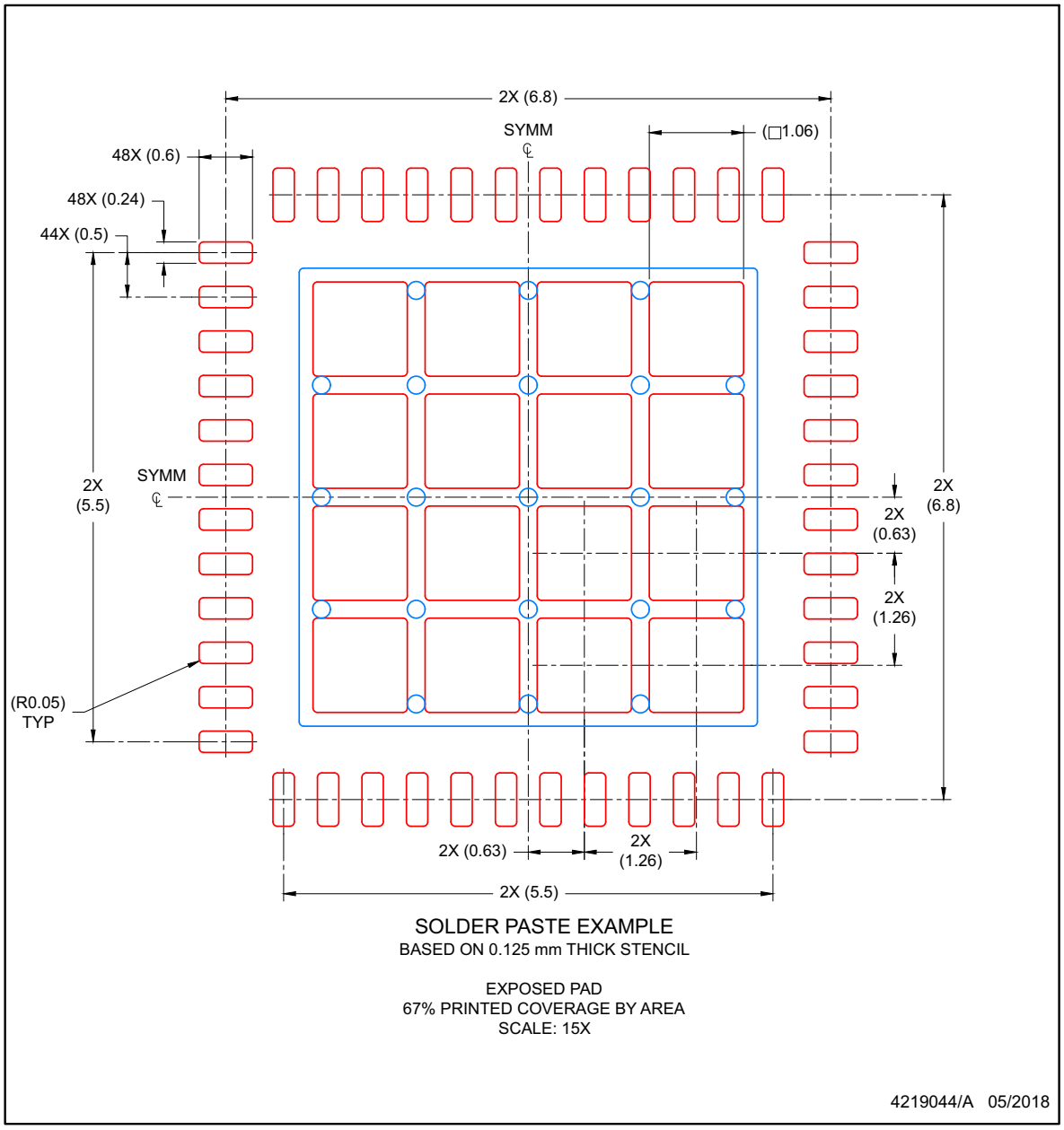
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048A — **VQFN - 1 mm max height**

PLASTIC QUADFLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK05318RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK05318RGZRG4	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZRG4.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZRG4.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK05318RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	K05318A3 2500
LMK05318RGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

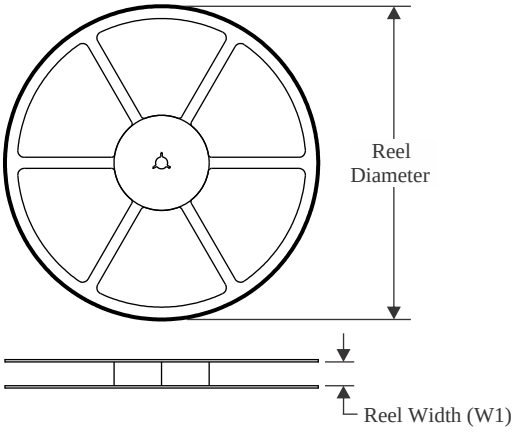
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

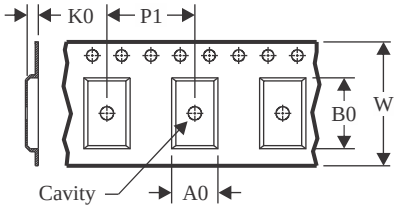
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

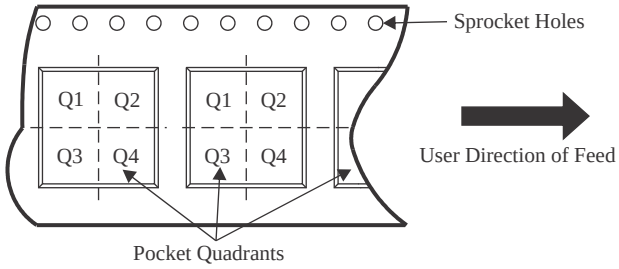


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

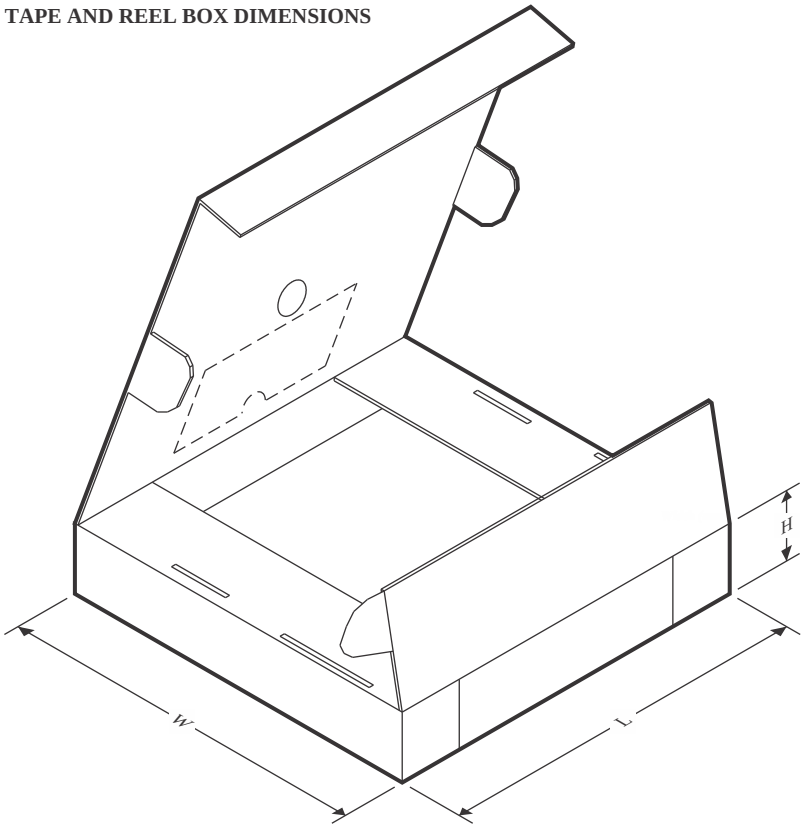
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK05318RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
LMK05318RGZRG4	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
LMK05318RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK05318RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
LMK05318RGZRG4	VQFN	RGZ	48	2500	367.0	367.0	38.0
LMK05318RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

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