

🕳 Order

Now





参考資料

LMK04832

JAJSFI6C - FEBRURAY 2017 - REVISED MAY 2018

LMK04832 超低ノイズ、JESD204B準拠 クロック・ジッタ・クリーナ、デュアル・ループPLL内蔵

Technical

Documents

1 特長

- 最大クロック出力周波数: 3255MHz
- マルチモード: デュアルPLL、シングルPLL、クロック分配
- 超低ノイズ(2500MHz時):
 - 54fs RMSジッタ(12kHz~20MHz)
 - 64fs RMSジッタ(100Hz~20MHz)
 - -157.6dBc/Hzのノイズ・フロア
- 超低ノイズ(3200MHz時):
 - 61fs RMSジッタ(12kHz~20MHz)
 - 67fs RMSジッタ(100Hz~100MHz)
 - −156.5dBc/Hzのノイズ・フロア
- PLL2
 - PLL FOM: -230dBc/Hz
 - PLL 1/f: -128dBc/Hz
 - 位相検出速度: 最高320MHz
 - 2つの内蔵VCO: 2440~2580MHz
 および2945~3255MHz
- 最大14個の差動デバイス・クロック
 - CML、LVPECL、LCPECL、HSDS、LVDS、 2xLVCMOSプログラマブル出力
- ・ 最大1個のバッファ付きVCXO/XO出力
 - LVPECL、LVDS、2xLVCMOSプログラマブル
- 1-1023のCLKout分周器
- 1-8191のSYSREF分周器
- SYSREFクロックの25psステップ・アナログ遅延
- デバイス・クロックおよびSYSREFのデジタル遅 延および動的デジタル遅延
- PLL1によるホールドオーバー・モード
- PLL1またはPLL2による0遅延
- 105℃のPCB温度に対応(サーマル・パッドで測定)

2 アプリケーション

- 試験/測定機器
- レーダー
- マイクロ波バックホール
- データ・コンバータのクロック供給

3 概要

🥭 Tools &

Software

LMK04832は、超高性能でJEDEC JESD204Bに準拠したクロック・コンディショナーで、LMK0482xファミリの製品とピン互換性があります。

Support &

Community

22

PLL2からの14のクロック出力を構成して、7つの JESD204Bコンバータ、あるいはデバイス・クロックおよび SYSREFクロックを使用するその他のロジック・デバイスを 駆動できます。DCおよびAC結合によりSYSREFを生成 することが可能です。JESD204Bアプリケーションに限ら ず、従来のクロッキング・システム向けに14の出力をそれ ぞれ高性能出力として個別に構成できます。

LMK04832は、SYSREFの生成またはリクロッキングの有 無にかかわらず、デュアルPLL、シングルPLL、またはク ロック分配モードで動作するように構成できます。PLL2 は内蔵VCOでも外付けVCOでも動作します。

高性能である上に、電力と性能のトレードオフ、デュアル VCO、動的デジタル遅延、ホールドオーバーといった機 能を備えたLMK04832は、柔軟性の高い高性能クロック・ ツリー・ソリューションとして最適です。

製品情報(1)

型番	説明	本体サイズ(公称)
LMK04832NKDT LMK04832NKDR	WQFN (64)	9.00mm×9.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末 尾にある注文情報を参照してください。
- (2) T=テープ、R=リール

概略回路図





LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



1	特長	
2	アプ	リケーション1
3	概要	Ę1
4	改訂	宿歴2
5	Pin	Configuration and Functions
6	Spe	cifications
	6.1	Absolute Maximum Ratings 5
	6.2	ESD Ratings
	6.3	Recommended Operating Conditions 6
	6.4	Thermal Information 6
	6.5	Electrical Characteristics 6
	6.6	Timing Requirements 17
	6.7	Timing Diagram 17
	6.8	Typical Characteristics – Clock Output AC
		Characteristics 18
7	Para	ameter Measurement Information 20
	7.1	Charge Pump Current Specification Definitions 20
	7.2	Differential Voltage Measurement Terminology 21
8	Deta	ailed Description 22
	8.1	Overview 22
	8.2	Functional Block Diagram 26

	8.3	Feature Description	29
	8.4	Device Functional Modes	41
	8.5	Programming	44
	8.6	Register Maps	45
9	Appl	ication and Implementation	90
	9.1	Application Information	90
	9.2	Typical Application	93
	9.3	Do's and Don'ts	97
10	Pow	er Supply Recommendations	97
	10.1	Current Consumption	97
11	Layo	out	98
	11.1	Layout Guidelines	98
	11.2	Layout Example	98
12	デバ	イスおよびドキュメントのサポート	100
	12.1	デバイス・サポート	100
	12.2	コミュニティ・リソース	100
	12.3	商標	100
	12.4	静電気放電に関する注意事項	100
	12.5	Glossary	100
13	メカニ	ニカル、パッケージ、および注文情報	100

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (January 2018) から Revision C に変更	Page
 デバイスの状態を「事前情報」から「量産データ」に変更 	1
Revision A (August 2017) から Revision B に変更	Page
 特長のジッタ、ノイズ・フロア、PLL性能VCO範囲を更新 	1
Updated the Electrical Characteristics table	5
Updated the Detailed Description section	22
2017年2月発行のものから更新	Page



www.tij.co.jp



5 Pin Configuration and Functions



Pin Functions

PIN		1/0	TYPE	DESCRIPTION(1)		
NO.	NAME	1/0	TTPE	DESCRIPTION		
1	CLKout0	0	Drogrommable	Clock output 0. For JESD204B systems suggest Device Clock.		
2	CLKout0*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, or LVDS.		
3	CLKout1	0	Drogrommable	Clock output 1. For JESD204B systems suggest SYSREF Clock.		
4	CLKout1*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		
5	RESET/GPO	Ι	CMOS	Device reset input or GPO		
6	SYNC/SYSREF_ REQ	I	CMOS	Synchronization input or SYSREF_REQ for requesting continuous SYSREF.		
7						
8	NC	—	—	Do not connect.		
9						
10	Vcc1_VCO		PWR	Power supply for VCO and clock distribution.		
11	LDObyp1		ANLG	LDO Bypass, bypassed to ground with 10-µF capacitor.		
12	LDObyp2		ANLG	LDO Bypass, bypassed to ground with a 0.1-µF capacitor.		
13	CLKout3	0	Drogrommobio	Clock output 3. For JESD204B systems suggest SYSREF Clock.		
14	CLKout3*	0	Fiogrammable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		

(1) See Pin Connection Recommendations for recommended connections.

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018 TEXAS INSTRUMENTS

www.ti.com

Pin Functions (continued)

	PIN					
NO.	NAME	1/0	TYPE	DESCRIPTION		
15	CLKout2	_		Clock output 2. For JESD204B systems suggest Device Clock.		
16	CLKout2*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, or LVDS.		
17	Vcc2_CG1		PWR	Power supply for clock outputs 2 and 3.		
18	CS*	I	CMOS	Chip Select		
19	SCK	I	CMOS	SPI Clock		
20	SDIO	I/O	CMOS	SPI Data		
21	Vcc3_SYSREF		PWR	Power supply for SYSREF divider and SYNC.		
22	CLKout5	0	Brogrommobio	Clock output 5. For JESD204B systems suggest SYSREF Clock.		
23	CLKout5*	0	Fiogrammable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		
24	CLKout4	~	Due average also	Clock output 4. For JESD204B systems suggest Device Clock.		
25	CLKout4*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, or LVDS.		
26	Vcc4_CG2		PWR	Power supply for clock outputs 4, 5, 6 and 7.		
27	CLKout6	~	Due average also	Clock output 6. For JESD204B systems suggest Device Clock.		
28	CLKout6*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, or LVDS.		
29	CLKout7	~	Due average also	Clock output 7. For JESD204B systems suggest SYSREF Clock.		
30	CLKout7*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		
31	Status_LD1	I/O	Programmable	Programmable status pin.		
32	CPout1	0	ANLG	Charge pump 1 output.		
33	Vcc5_DIG		PWR	Power supply for the digital circuitry.		
CLKin1				Reference Clock Input Port 1 for PLL1.		
34	FBCLKin	Ι	ANLG	Feedback input for external clock feedback input (0-delay mode).		
	Fin1			External VCO Input or clock distribution input.		
	CLKin1* Reference Clock Input Port 1 for P		Reference Clock Input Port 1 for PLL1.			
35	FBCLKin*	I	ANLG	Feedback input for external clock feedback input (0-delay mode).		
	Fin1*			External VCO Input or clock distribution input.		
36	Vcc6_PLL1		PWR	Power supply for PLL1, charge pump 1, holdover DAC		
37	CLKin0			Pafaranaa Claak Input Dart 0 far DI 1		
38	CLKin0*	I	ANLO			
39	Vcc7_OSCout		PWR	Power supply for OSCout port.		
10	OSCout	1/0	Drogrommable	Buffered output of OSCin port.		
40	CLKin2	1/0	Programmable	Reference Clock Input Port 2 for PLL1.		
11	OSCout*	1/0	Drogrommable	Buffered output of OSCin port.		
41	CLKin2*	1/0	Flogrammable	Reference Clock Input Port 2 for PLL1.		
42	Vcc8_OSCin		PWR	Power supply for OSCin		
43	OSCin			Feedback to DLL1 and reference input to DLL2. AC sounded		
44	OSCin*	1	ANLG	reeuback to FLLT and reference input to FLLZ. AC-coupled.		
45	Vcc9_CP2		PWR	Power supply for PLL2 Charge Pump.		
46	CPout2	0	ANLG	Charge pump 2 output.		
47	Vcc10_PLL2		PWR	Power supply for PLL2.		
48	Status_LD2	I/O	Programmable	Programmable status pin.		
49	CLKout9	~	Drogromershi	Clock output 9. For JESD204B systems suggest SYSREF Clock.		
50	CLKout9*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		
51	CLKout8	0	Drogrommable	Clock output 8. For JESD204B systems suggest Device Clock.		
52	CLKout8*	0	Fiogrammable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.		
53	Vcc11_CG3		PWR	Power supply for clock outputs 8, 9, 10, and 11.		



Pin Functions (continued)

PIN		1/0	TYPE		
NO.	NAME	1/0	TIPE	DESCRIPTION	
54	CLKout10	0	Brogrommobio	Clock output 10. For JESD204B systems suggest Device Clock.	
55	CLKout10*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.	
56	CLKout11	0	Brogrommobio	Clock output 11. For JESD204B systems suggest SYSREF Clock.	
57	CLKout11*	0	Flogrammable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.	
58	CLKin_SEL0	I/O	Programmable	e Programmable status pin.	
59	CLKin_SEL1	I/O	Programmable	Programmable status pin.	
60	CLKout13	0	Brogrommobio	Clock output 13. For JESD204B systems suggest SYSREF Clock.	
61	CLKout13*	0	Flogrammable	Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.	
62	CLKout12	0	Drammakla	Clock output 12. For JESD204B systems suggest Device Clock.	
63	CLKout12*	0	Programmable	Programmable formats: CML, LVPECL, LCPECL, or LVDS.	
64	Vcc12_CG0		PWR	Power supply for clock outputs 0, 1, 12, and 13.	
DAP	DAP		GND	DIE ATTACH PAD, connect to GND.	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	-0.3	3.6	V
V _{IN}	Input voltage	-0.3	(V _{CC} +0.3)	V
TL	Lead temperature (solder 4 seconds)		260	°C
TJ	Junction temperature		150	°C
I _{IN}	Differential input current (CLKinX/X*, OSCin/OSCin*)		±5	mA
MSL	Moisture sensitivity level		3	
T _{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Never to exceed 3.6 V

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	
	Electrostatic discharge	Machine Model (MM)	±150	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±250	

 JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

JAJSFI6C - FEBRURAY 2017 - REVISED MAY 2018

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
TJ	Junction Temperature			125	°C
T _A	Ambient Temperature	-40	25	85	°C
T _{PCB}	PCB Temperature (measured at thermal pad)			105	°C
V _{CC}	Supply Voltage	3.15	3.3	3.45	V

6.4 Thermal Information

		LMK04832		
	THERMAL METRIC ⁽¹⁾	NKD (WQFN)	UNIT	
		64 PINS		
R _{0JA}	Junction-to-ambient thermal resistance ⁽²⁾	24.3	°C/W	
R _{0JC(top)}	Junction-to-case (top) thermal resistance ⁽³⁾	6.1	°C/W	
R _{0JB}	Junction-to-board thermal resistance ⁽⁴⁾	3.5	°C/W	
Ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.1	°C/W	
Ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	3.5	°C/W	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	0.7	°C/W	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R Θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R\Theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
CURRENT CONSUMPTION ⁽¹⁾								
I _{CC_PD}	Power Down Supply Current			1.5	3	mA		
I _{CC_JESD204B_ALL}	Supply Current for JESD204B use case during JESD204B synchronization VCO = 2949.12 MHz Dual Loop ⁽²⁾	4 CML 32 mA clocks in bypass 3 LVDS clock /12 4 SYSREF as LCPECL 3 SYSREF as LVDS		930	1120	mA		
ICC_JESD204B_LOW	Supply Current for JESD204B use case during JESD204B steady state while holding SYSREF as low in DC coupled configuration. ⁽²⁾	4 CML 32 mA clocks in bypass 3 LVDS clock /12 4 SYSREF as LCPECL (low state) 3 SYSREF as LVDS (low state)		780	940	mA		
ICC_JESD204B_VCM	Supply Current for JESD204B use case during JESD204B steady state while setting SYSREF outputs as Vcm. ⁽²⁾	4 CML 32 mA clocks in bypass 3 LVDS clock /12 7 SYSREF outputs powered down		675	810	mA		

(1) Use the TICS Pro tool to calculate Icc for a specific configuration.

(2) LCPECL clocks have 120 Ω emitter resistors. OSCout LVPECL clock uses 240 Ω ohm emitter resistors. Other settings include CLKoutX_Y_IDL = 0, CLKoutX_Y_ODL = 0, DCLKX_Y_DCC = 0. SCLK_X_Y_ADLY_EN = 0.

Copyright © 2017-2018, Texas Instruments Incorporated



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

PARAMETER TEST CONDITIONS		TEST CONDITIONS	MIN	TYP MAX	
CLKin0/0*, CLKir	n1/1*, and CLKin2/2* INPUT CLOCK SP	ECIFICATIONS			
f _{CLKinX_LOS}	Clock Input LOS (CLKin0/1/2)	LOS_EN = 1	0.001	25	MHz
f _{CLKin0_PLL1_MOS}	Clock Input Frequency for PLL1	CLKin0_OUT_MUX = 2 (PLL1)			MHz
f _{CLKin1_PLL1_MOS}	Reference (CLKin0/1/2)	CLKin1_OUT_MUX = 2 (PLL1)	0.001	25	MHz
f _{CLKin2_PLL1_MOS}	CLKinX_TYPE = 1 (MOS)	OSCout_FMT = 0 (Power down)			MHz
f _{CLKin0_PLL1}	Clock Input Frequency for PLL1	CLKin0_OUT_MUX = 2 (PLL1)			
f _{CLKin1_PLL1}	Reference (CLKin0/1/2)	CLKin1_OUT_MUX = 2 (PLL1)	0.001	75) MHz
f _{CLKin2_PLL1}	CLKinX_TYPE = 0 (Bipolar)	OSCout_FMT = 0 (Power down)			
f _{CLKin0_PLL2}		CLKin0_OUT_MUX = 2 (PLL1) PLL2R_CLK_MUX = 1 (PLL1 CLKinX)			
f _{CLKin1_PLL2}	Clock Input Frequency for PLL2 Reference (CLKin0/1/2)	CLKin1_OUT_MUX = 2 (PLL1) PLL2R_CLK_MUX = 1 (PLL1 CLKinX)	500		MHz
f _{CLKin2_PLL2}		OSCout_FMT = 0 (Power down) PLL2R_CLK_MUX = 1 (PLL1 CLKinX)			
f _{CLKin1_FB}	Clock Input Frequency for 0-delay with external feedback (CLKin1)	CLKin1_OUT_MUX = 1 (FB Mux) CLKin1_TYPE = 0 (Bipolar)	0.001	75	MHz
f _{CLKin1_Fin}	Clock Input Frequency for external VCO or distribution mode (CLKin1)	CLKin1_OUT_MUX = 0 (Fin) CLKin1_TYPE = 0 (Bipolar)	0.001	325	MHz
SLEW _{CLKin}	Clock Input Slew Rate ⁽³⁾	20% to 80%	0.15	0.5	V/ns
V _{ID} CLKin_AC	Differential Clash Innut Valtage (4)		0.125	1.5	5 V
V _{SS} CLKin_AC	Differential Clock Input Voltage	AC-coupled	0.25	3.	1 Vpp
V _{CLKin}	Clock Input Single-ended Input Voltage	AC-coupled to CLKinX; CLKinX* AC-coupled to Ground CLKinX_TYPE = 0 (Bipolar)	0.5	2.	4 Vpp
	DC offset voltage between	Each pin AC-coupled, CLKin0/1/2 CLKinX_TYPE = 0 (Bipolar)		0	mV
V _{CLKinX-offset}	CLKinX/CLKinX [*] (CLKinX [*] - CLKinX)	Each pin AC-coupled, CLKin0/1 CLKinX_TYPE = 1 (MOS)		55	mV
	DC offset voltage between CLKin2/CLKin2* (CLKin2* - CLKin2)	Each pin AC-coupled CLKinX_TYPE = 1 (MOS)		20	mV
V _{CLKin} V _{IH}	High Input Voltage	DC-coupled to CLKinX;	2	Vc	c V
V _{CLKin} V _{IL}	Low Input Voltage	CLKinX* AC-coupled to Ground CLKinX_TYPE = 1 (MOS)	0	0	4 V

(3) In order to meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.

(4) See Differential Voltage Measurement Terminology for definition of V_{ID} and V_{OD} voltages.



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ °C} < \text{T}_{A} < 85 \text{ °C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}, \text{T}_{A} = 25 \text{ °C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT	
PLL1 SPECIFICAT	IONS					
f _{PD1}	PLL1 Phase Detector Frequency			40	MHz	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 0	50			
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 1	150			
	PLL1 Charge Pump Source	V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 2	250			
ICPout1SOURCE	Current ⁽⁵⁾				μΑ	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 14	1450		1	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 15	1550		Ī	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 0	-50			
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 1	-150			
	DI L 1 Charge Dump Sink Current ⁽⁵⁾	V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 2	-250			
ICPout15IINK	PLET Charge Pump Sink Current				μΑ	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 14	-1450		Ī	
		V _{CPout1} = Vcc/2, PLL1_CP_GAIN = 15	-1550			
I _{CPout1} %MIS	Charge Pump Sink / Source Mismatch	$V_{CPout1} = Vcc/2, T_A = 25 \ ^{\circ}C$	1%	10%		
I _{CPout1} %V _{TUNE}	Magnitude of Charge Pump Current Variation vs. Charge Pump Voltage	$0.5 \text{ V} < \text{V}_{\text{CPout1}} < \text{V}_{\text{CC}} - 0.5 \text{ V} \text{ T}_{\text{A}} = 25 ^{\circ}\text{C}$	4%			
I _{CPout1} %TEMP	Charge Pump Current vs. Temperature Variation		4%			
I _{CPout1} TRI	Charge Pump TRI-STATE Leakage Current	0.5 V < V _{CPout1} < V _{CC} - 0.5 V		5	nA	
	PLL 1/f Noise at 10 kHz offset	PLL1_CP_GAIN = 50 µA	-113			
PN10 kHz ⁽⁶⁾	Normalized to 1 GHz Output	PLL1_CP_GAIN = 450 μA	-117		dBc/	
	Frequency	PLL1_CP_GAIN = 1550 μA	-119		112	
		PLL1_CP_GAIN = 50 µA	-217			
PN1 Hz ⁽⁷⁾	Normalized Phase Noise	PLL1_CP_GAIN = 450 µA	-224		dBc/	
		PLL1_CP_GAIN = 1550 μA	-225		112	

(5) This parameter is programmable

(6) A specification in modeling PLL in-band phase noise is the 1/f flicker noise, L_{PLL_flicker}(f), which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10 kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10 kHz = L_{PLL_flicker}(10 kHz) - 20 log(Fout / 1 GHz), where LPLL_flicker(f) is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure L_{PLL_flicker}(f) it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). L_{PLL_flicker}(f) can be masked by the reference oscillator performance if a low-power or noisy source is used. The total PLL in-band phase noise performance is the sum of L_{PLL_flicker}(f) and L_{PLL_flick}(f).

(7) A specification modeling PLL in-band phase noise. The normalized phase noise contribution of the PLL, L_{PLL_flat}(f), is defined as: PN1 HZ = L_{PLL_flat}(f) - 20 log(N) - 10 log(f_{PDX}). L_{PLL_flat}(f) is the single side band phase noise measured at an offset frequency, f, in a 1 Hz bandwidth and f_{PDX} is the phase detector frequency of the synthesizer. L_{PLL_flat}(f) contributes to the total noise, L(f).



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCin INPUT CL	OCK SPECIFICATIONS					
f _{OSCin}	PLL2 Reference Input				500	MHz
SLEW _{OSCin}	PLL2 Reference Clock minimum slew rate on OSCin ⁽³⁾	20% to 80%	0.15	0.5		V/ns
V _{OSCin}	Input Voltage for OSCin or OSCin*	AC coupled; Single-ended (Unused pin AC-coupled to GND)	0.2		2.4	Vpp
V _{ID} OSCin			0.2		1.55	V
V _{SS} OSCin	Differential voltage swing (*)	AC-coupled	0.4		3.1	Vpp
V _{OSCin-offset}	DC offset voltage between OSCin/OSCin* (OSCinX* - OSCinX)	Each pin AC-coupled		20		mV
f _{doubler_max}	Doubler input frequency	EN_PLL2_REF_2X = 1 ⁽⁸⁾ ; OSCin Duty Cycle 40% to 60%			320	MHz
PLL2 SPECIFICA	TIONS					
f _{PD2}	Phase Detector Frequency				320	MHz
	PLL2 Charge Pump Source	$V_{CPout2} = V_{CC}/2$, PLL2_CP_GAIN = 2		1600		114
CPout2 SOURCE	Current ⁽⁵⁾	$V_{CPout2} = V_{CC}/2$, PLL2_CP_GAIN = 3		3200		μΑ
1	PLL 2 Charge Pump Sink Current ⁽⁵⁾	$V_{CPout2} = V_{CC}/2$, PLL2_CP_GAIN = 2		-1600		
CPout2 SINK		$V_{CPout2} = V_{CC}/2$, PLL2_CP_GAIN = 3		-3200		μΑ
I _{CPout2%MIS}	Charge Pump Sink / Source Mismatch	$V_{CPout2} = Vcc/2, T_A = 25 \ ^{\circ}C$		1%	10%	
I _{CPout2%VTUNE}	Magnitude of Charge Pump Current Variation vs. Charge Pump Voltage	0.5 V < V _{CPout2} < VCC - 0.5 V T _A = 25 °C		4%		
I _{CPout2%TEMP}	Charge Pump Current vs. Temperature Variation			4%		
I _{CPout2 TRI}	Charge Pump TRI-STATE Leakage Current	0.5 V < V _{CPout2} < V _{CC} - 0.5 V			10	nA
PN10 kHz ⁽⁶⁾	PLL 1/f Noise at 10 kHz offset. Normalized to 1 GHz Output Frequency	PLL2_CP_GAIN = 3200 µA		-128		dBc/ Hz
PN1 Hz ⁽⁷⁾	Normalized Phase Noise Contribution	PLL2_CP_GAIN = 3200 μA		-230		dBc/ Hz

(8) The EN_PLL2_REF_2X bit enables/disables a frequency doubler mode for the PLL2 OSCin path.



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST C	ONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL V	CO SPECIFICATIONS						
		VCO0		2440		2580	
T _{VCO}	LMK04832 VCO Tuning Range	VCO1		2945		3255	WHZ
		1/000	2440 MHz		-11.8		
14		VC00	2580 MHz		-14.5		MHz/
r _{VCO}	LIVIK04832 viune Tuning Sensitivity	VC01	2945 MHz		-22.9		V
		VCOT	3255 MHz		-31.4		
ATCL	Allowable Temperature Drift for Continuous Lock ⁽⁹⁾	After programming to output configuration assure continuous l	for lock, no changes to a are permitted to ock			125	°C
			1 kHz		-55		
		10 kHz		-86.3			
		VCO0 at 100 2440 MHz 800	100 kHz		-115.2		dBc/ Hz
			800 kHz		-136.3		
			1 MHz		-137.6		
			1 kHz		-53.3		dBc/ Hz
		1/000 at	10 kHz		-85		
		2580 MHz	100 kHz		-114.3		
		2000	800 kHz		-135.3		
l (f)	Open-loop phase poise		1 MHz		-136.9		
	Open-loop pliase hoise		1 kHz		-49.2		
		1/001 at	10 kHz		-81.1		
		2945 MHz	100 kHz		-111.1		dBc/ Hz
			800 kHz		-133.8		
			1 MHz		-135.9		
			1 kHz		-46.6		
			10 kHz		-78.9		
		3250 MHz	100 kHz		-108.9		dBc/ Hz
			800 kHz		-131.7		
			1 MHz		-133.3		

(9) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the 0x168 register was last programmed with PLL2_FCAL_DIS = 0, and still have the part stay in lock. The action of programming the 0x168 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the appropriate register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of – 40 °C to 85 °C without violating specifications.



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST C	ONDITIONS	MIN TYP	MAX	UNIT
CLOCK OUTP	UT NOISE FLOOR					
L(f) _{CLKout}		LVDS	CLKoutX_Y_ODL=1	-159.5		
L(f) _{CLKout}		HSDS 6 mA	CLKoutX_Y_ODL=1	-161.5		
L(f) _{CLKout}		HSDS 8 mA	CLKoutX_Y_ODL=1	-162.5		
L(f) _{CLKout}		LCPECL	CLKoutX_Y_ODL=1	-162.5		
L(f) _{CLKout}		LVPECL 1.6 Vpp	CLKoutX_Y_ODL=1	-162		
L(f) _{CLKout}		LVPECL 2 Vpp	CLKoutX_Y_ODL=1	-163		
L(f) _{CLKout}	245.76 MHz Noise Floor 20 MHz Offset	CML 16 mA, odd CLKoutY DC bias: 50 Ω to Vcc	CLKoutX_Y_ODL=1	-162.5		dBc/ Hz
L(f) _{CLKout}		CML 24 mA, odd CLKoutY DC bias: 50 Ω to Vcc	CLKoutX_Y_ODL=1	-162.5		
L(f) _{CLKout}		CML 32 mA, odd CLKoutY DC bias: 50 Ω to Vcc	CLKoutX_Y_ODL=1	-163		
L(f) _{CLKout}		LVCMOS	CLKoutX_Y_ODL=1	-160		
L(f) _{CLKout}		CML 16 mA, even CLKoutX DC bias: 68 nH to 20 Ω to Vcc	CLKoutX_Y_IDL=1	-155.5		
L(f) _{CLKout}	3.2 GHz Noise Floor 20 MHz Offset	CML 24 mA, even CLKoutX DC bias: 68 nH to 20 Ω to Vcc	CLKoutX_Y_IDL=1	-156		dBc/ Hz
L(f) _{CLKout}		CML 32 mA, even CLKoutX DC bias: 68 nH to 20Ω to Vcc	CLKoutX_Y_IDL=1	-156.5		
CLKout CLOS	ED LOOP PHASE NOISE SPECIFICATIO	ONS				
		Offset = 1 kHz		-125		
1 (f)	VCO0 SSB Phase Noise 245.76	Offset = 10 kHz		-134		dBc/
L([†])CLKout	Doubler disabled	Offset = 100 kHz		-137		Hz
		Offset = 1 MHz		-154]	
		Offset = 1 kHz		-125		
1 (f)	VCO1 SSB Phase Noise 245.76	Offset = 10 kHz		-135		dBc/
└UCLKout	Doubler disabled	Offset = 100 kHz		-137		Hz
		Offset = 1 MHz		-151		

(10) Dual Loop, OSCin reference is a 122.88 MHz Crystek 603281 VCXO. Data collected using a MACOM H-183-4 Hybrid Junction for differential to single ended conversion. PLL2_CP = 3.2 mA. PLL2 Loop filter is C1i = 60 pF, C1 (external) = 4.7 pF, R2 = 820 Ω (external), C2 = 3.9 nF (external), R3 = 2.4 kΩ, C3 = 50 pF, R4 = 200 Ω, C4 = 10 pF. PLL1_CP = 450 µA with a narrow loop bandwidth. CLKoutX_Y_IDL = 0, CLKoutX_Y_ODL = 1. Even CLKout with LVPECL20 format using 120-Ω to GND.



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ °C} < \text{T}_{A} < 85 \text{ °C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}, \text{T}_{A} = 25 \text{ °C}$, at the *Recommended Operating Conditions* are not assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLKout CLOSE	D LOOP JITTER SPECIFICATIONS					1
	VCO0, f _{CLKout} = 2500 MHz ⁽¹¹⁾	PDF = 312.5 MHz BW = 12 kHz to 20 MHz		54		fs rms
J _{CLKout}	Integrated RMS Jitter	PDF = 312.5 MHz BW = 100 Hz to 100 MHz		64		fs rms
	VCO1, f _{CLKout} = 3200 MHz ⁽¹¹⁾	PDF = 320 MHz BW = 12 kHz to 20 MHz		61		fs rms
	Integrated RMS Jitter	PDF = 320 MHz BW = 100 Hz to 100 MHz		67		fs rms
	VCO0, f _{CLKout} = 2457.6 MHz Integrated RMS Jitter ⁽¹⁰⁾	PDF = 245.76 MHz (Doubler enabled) BW = 12 kHz to 20 MHz		55		fs rms
	VCO0, f _{CLKout} = 2457.6 MHz Integrated RMS Jitter ⁽¹⁰⁾	PDF = 122.88 MHz BW = 12 kHz to 20 MHz		70		fs rms
JCLKout	VCO1, f _{CLKout} = 2949.12 MHz Integrated RMS Jitter ⁽¹⁰⁾	PDF = 245.76 (Doubler enabled) BW = 12 kHz to 20 MHz		60		fs rms
	VCO1, f _{CLKout} = 2949.12 MHz Integrated RMS Jitter ⁽¹⁰⁾	PDF = 122.88 MHz BW = 12 kHz to 20 MHz		75		fs rms
DEFAULT POWE	ER on RESET CLOCK OUTPUT FREQU	ENCY	•			
f _{OSCout}	OSCout default frequency ⁽¹²⁾				500	MHz
CLOCK SKEW ⁽¹⁾	3)					
T _{SKEW}	Maximum skew CLKoutX to CLKoutX F_{CLK} = 1.6 GHz, R_L = 100 Ω AC-coupled	Any even CLKoutX, same format ⁽¹⁴⁾ Device Clock DCLKX_Y_BYP = 1		60		ps
T _{skew}	Maximum skew for CLKoutX to CLKoutX or CLKoutY to CLKoutY F _{CLK} = 250 MHz, R_L = 100 Ω AC-coupled	Even to even or odd to odd clock, same format ⁽¹⁵⁾ Device clock DCLKX_Y_BYP = 0 DCLKX_Y_DIV = 12		60		ps
T _{skew}	Maximum skew for any CLKoutX or Y to any CLKoutX or Y F_{CLK} = 250 MHz, R_L = 100 Ω AC-coupled	Any output, same format ⁽¹⁵⁾ Device clock DCLKX_Y_BYP = 0 DCLKX_Y_DIV = 12		100		ps
T _{skew}	Delay from CLKoutX to CLKoutY in same pair $F_{CLK} = 250 \text{ MHz}, R_L = 100 \Omega \text{ AC-coupled}$	Same pair of device clocks, same format ⁽¹⁵⁾		35		ps

(11) Single Loop, OSCin reference is R&S SMA100B Signal Generator with option SMAB-B711 through Prodyn BIB-100G Balun to OSCin. Data collected using a MACOM H-183-4 Hybrid Junction for differential to single ended conversion. PLL2 Loop filter is C1 = 60 pF, R2 = 470 Ω (external), C2 = 150 nF (external), R3 = 2.4 kΩ, C3 = 50 pF, R4 = 200 Ω, C4 = 10 pF, PLL2_CP = 3.2 mA. CLKoutX_Y_IDL = 1, CLKoutX_Y_ODL = 0; Even CLKout with CML 32 mA format using DC bias 68-nH to 20-Ω to Vcc.

(12) OSCout will oscillate at start-up at the frequency of the VCXO attached to OSCin port.

(13) Equal loading and identical clock configuration on each clock input and/or output is required for skew, setup, and hold specifications to be valid.

(14) Valid for CML 32 mA, CML 24 mA, CML 16 mA. CML DC bias is 50 ohms to Vcc or 68 nH to 20 Ω to Vcc.

(15) Valid for HSDS 8 mA, HSDS 6 mA, LVDS. LVPECL20, LVPECL16, LCPECL with 120 Ω emitter resistor to ground.



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CO	TEST CONDITIONS		TYP	MAX	UNIT
CML 32 mA	CLOCK OUTPUTS (CLKoutX/Y)						
T _R / T _F	20% to 80% Output Rise/Fall	R_L = AC-coupled 100 Odd CLKoutY, CLKo DC Bias, 50 ohm to 1	R_L = AC-coupled 100 Ω, 250 MHz Odd CLKoutY, CLKoutX_Y_ODL = 1 DC Bias, 50 ohm to Vcc		135		ps
V _{OH}	Output High Voltage		T = 25 °C, DC measurement Termination 50-Ω pull up to Vcc		Vcc		
V _{OL}	Output Low Voltage	T = 25 °C, DC measurements Termination 50-Ω pu			Vcc - 1.66		V
V _{OD}	Differential Output Voltage				1660		mV
	$ \begin{array}{c} DC \text{ bias is } 50 \ \Omega \text{ pull} \\ up \text{ to } Vcc \\ R_L = AC\text{-coupled} \\ 100 \ \Omega \end{array} $		250 MHz ⁽¹⁶⁾		1070		
V _{OD}	Differential Output Voltage	DC higg is 68 all to	2.5 GHz ⁽¹⁷⁾		765		mV
		$20-\Omega$ to Vcc	2.5 GHz ⁽¹⁸⁾		550		
		$R_L = AC$ -coupled	3.2 GHz ⁽¹⁷⁾		610		UNIT ps V ImVI ps V ImVI ImVI
		100 Ω	3.2 GHz ⁽¹⁸⁾		385		
CML 24 mA	CLOCK OUTPUTS (CLKoutX/Y)						
T _R / T _F	20% to 80% Output Rise/Fall	R_L = AC-coupled 100 Odd CLKoutY, CLKo DC Bias, 50 ohm to	R_L = AC-coupled 100 Ω, 250 MHz Odd CLKoutY, CLKoutX_Y_ODL = 1 DC Bias. 50 obm to Vcc		125		ps
V _{OH}	Output High Voltage				Vcc		
V _{OL}	Output Low Voltage	T = 25 °C, DC meas Termination 50- Ω pu	urement II up to Vcc		Vcc - 1.26		V
V _{OD}	Differential Output Voltage				1260		mV
		DC bias is $50-\Omega$ pull up to Vcc $R_L = AC$ -coupled 100 Ω	250 MHz ⁽¹⁶⁾		815		
V _{OD}	V _{OD} Differential Output Voltage	DC bios is 68 styles	2.5 GHz ⁽¹⁷⁾		595		mV
		$20-\Omega$ to Vcc	2.5 GHz ⁽¹⁸⁾		445		1
		$R_L = AC$ -coupled	3.2 GHz ⁽¹⁷⁾		480		
		100 Ω	3.2 GHz ⁽¹⁸⁾		330		

(16) For even and odd outputs CLKoutX_Y_IDL=0. For even outputs CLKoutX_Y_ODL=X and for odd CLKoutX_Y_ODL=1.
(17) Even clock outputs (CLKoutX). CLKoutX_Y_IDL=1, CLKoutX_Y_ODL=X.
(18) Odd clock outputs (CLKoutY). CLKoutX_Y_IDL=X, CLKoutX_Y_ODL=1



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CO	NDITIONS	MIN TYP	MAX	UNIT
CML 16 mA CLO	CK OUTPUTS (CLKoutX/Y)					
T _R / T _F	20% to 80% Output Rise/Fall	R _L = AC-coupled 100 Odd CLKoutY, CLKo DC Bias, 50 ohm to V	0 Ω, 250 MHz utX_Y_ODL = 1 Vcc	120		ps
V _{OH}	Output High Voltage			Vcc		
V _{OL}	Output Low Voltage	T = 25 °C, DC mease Termination is 50-Ω	urement pull up to Vcc	Vcc - 0.84		V
V _{OD}	Differential Output Voltage	_		840		mV
V _{OD}		DC bias is $50-\Omega$ pull up to Vcc $R_L = AC$ -coupled 100Ω	DC bias is $50 \cdot \Omega$ pull up to Vcc $R_L = AC$ -coupled $100 \ \Omega$ $250 \text{ MHz}^{(16)}$ $250 \text{ C}^{(17)}$			
V _{OD}	Differential Output Voltage	DC bias is 68 pH to	2.5 GHz ⁽¹⁷⁾	400		mV
V _{OD}		$20-\Omega$ to Vcc	2.5 GHz ⁽¹⁸⁾	325		
V _{OD}		$R_L = AC$ -coupled	3.2 GHz ⁽¹⁷⁾	325		
V _{OD}		100 Ω	3.2 GHz ⁽¹⁸⁾	250		
LVPECL CLOCK	OUTPUT (CLKoutX/Y, OSCout)					
T _R / T _F	20% to 80% Output Rise/Fall	$R_L = AC$ -coupled 100) Ω, 250 MHz	140		ps
LVPECL 2000 mV	pp CLOCK OUTPUTS (CLKoutX/Y, OS	SCout)				
V _{OH}	Output High Voltage			V _{CC} - 1		V
V _{OL}	Output Low Voltage	DC Measurement	o Vcc - 2 0 V	V _{CC} - 2		V
V _{OD}	Output Voltage ⁽⁴⁾			1000		mV
			250 MHz ⁽¹⁹⁾	925		
	$Em = 120 \Omega$ to	2.5 GHz ⁽²⁰⁾	585			
V _{OD}	Differential Output Voltage	ground Termination = AC-	2.5 GHz ⁽²¹⁾	545		mV
		coupled 100 Ω	3.2 GHz ⁽²⁰⁾	415		
			3.2 GHz ⁽²¹⁾	370		L
LVPECL 1600 mV	pp CLOCK OUTPUTS (CLKoutX/Y, OS	SCout)		Γ		
V _{OH}	Output High Voltage	_		V _{CC} - 1		V
V _{OL}	Output Low Voltage	DC Measurement Termination = $50-\Omega$ t	o V _{CC} - 2.0 V	V _{CC} - 1.8		V
V _{OD}	Output Voltage ⁽⁴⁾			800		mV
			250 MHz ⁽¹⁹⁾	760		
		$Em = 120 \Omega$ to	2.5 GHz ⁽²⁰⁾	510		
V _{OD}	Differential Output Voltage	Termination = AC-	2.5 GHz ⁽²¹⁾	480		mV
		coupled 100 Ω	3.2 GHz ⁽²⁰⁾	370		
			3.2 GHz ⁽²¹⁾	340		
LCPECL CLOCK	OUTPUT (CLKoutX/Y, OSCout)	I		Γ		
T _R / T _F	20% to 80% Output Rise/Fall	$R_L = AC$ -coupled 100 DC bias = 120 Ω to 0) Ω GND	135		ps
V _{OH}	Output High Voltage			1.6		V
V _{OL}	Output Low Voltage	Termination = 50-0 t	o 0.5 V	0.6		V
V _{OD}	Output Voltage ⁽⁴⁾			1000		mV
HSDS 8 mA CLO	CK OUTPUTS (CLKoutX/Y)					
T _R / T _F	20% to 80% Output Rise/Fall	R_{L} = 100 Ω, 250 MH	Z	170		ps

(19) CLKoutX_Y_IDL=X and CLKoutX_Y_ODL=X.
(20) Even clock outputs (CLKoutX). CLKoutX_Y_IDL=X, CLKoutX_Y_ODL=1.
(21) Odd clock outputs (CLKoutY). CLKoutX_Y_IDL=X, CLKoutX_Y_ODL=1



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	Output High Voltage			V _{CC} - 0.95		V
V _{OL}	Output Low Voltage	DC Measurement		V _{CC} - 1.7		V
V _{OD}	Output Voltage ⁽⁴⁾	Termination = 50-22 to v_{CC} - 1.64 v		750		mV
ΔV_{OD}	Change in Magnitude of V _{OD} for complementary output states		-115		115	mV
HSDS 6 mA CLOC	K OUTPUTS (CLKoutX/Y)					
T _R / T _F	20% to 80% Output Rise	R _L = 100 Ω, 250 MHz		170		ps
V _{OH}	Output High Voltage			V _{CC} - 0.9		V
V _{OL}	Output Low Voltage	DC Measurement Termination = 50-Ω to V _{CC} - 1.42 V		V _{CC} - 1.5		V
V _{OD}	Output Voltage ⁽⁴⁾	Termination = 50- Ω to V _{CC} - 1.42 V		600		mV
ΔV_{OD}	Change in Magnitude of V _{OD} for complementary output states		-80		80	mV
LVDS CLOCK OUT	FPUTS (CLKoutX/Y, OSCout)	•				
T _R / T _F	20% to 80% Output Rise	R _L = 100 Ω, 250 MHz		175		ps
V _{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	Change in Magnitude of V _{OD} for complementary output states	T = 25 °C, DC measurement	-60		60	mV
V _{OS}	Output Offset Voltage	AC-coupled to receiver input $R_1 = 100-\Omega$ differential termination	1.125	1.25	1.375	V
ΔV_{OS}	Change in V _{OS} for complementary output states	···-			35	mV
I _{SA} I _{SB}	Output short circuit current - single- ended	Single-ended output shorted to GND T = 25 °C	-24		24	mA



Electrical Characteristics (continued)

 $(3.15 \text{ V} < \text{V}_{CC} < 3.45 \text{ V}, -40 \text{ }^{\circ}\text{C} < \text{T}_{A} < 85 \text{ }^{\circ}\text{C}$. Typical values at $\text{V}_{CC} = 3.3 \text{ V}$, $\text{T}_{A} = 25 \text{ }^{\circ}\text{C}$, at the *Recommended Operating Conditions* are not assured.)

	PARAMETER	TEST CONDITIONS	MIN	TYP MA	X	UNIT
LVCMOS CLC	OCK OUTPUTS (CLKout8/10/Y, OSCout)	"				
f _{CLKout}	Maximum Frequency	5 pF Load	250			MHz
V _{OH}	Output High Voltage	1 mA Load	Vcc - 0.1			V
V _{OL}	Output Low Voltage	1 mA Load		(.1	V
I _{OH}	Output High Current (Source)	$V_{CC} = 3.3 \text{ V}, V_{O} = 1.65 \text{ V}$		-28		mA
I _{OL}	Output Low Current (Sink)	$V_{CC} = 3.3 \text{ V}, V_{O} = 1.65 \text{ V}$		28		mA
DUTY _{CLK}	Output Duty Cycle ⁽²²⁾ (23)	$V_{CC}/2$ to $V_{CC}/2$, F_{CLK} = 100 MHz, T = 25°C		50		%
DIGITAL OUT	PUTS (CLKin_SELX, Status_LDX, and RE	SET/GPO)				
V _{OH}	High-Level Output Voltage	I _{OH} = -500 μA CLKin_SELX_TYPE = 3 or 4 Status_LDX_TYPE = 3 or 4 RESET_TYPE = 3 or 4	V _{CC} - 0.4			V
V _{OL}	Low-Level Output Voltage	$I_{OL} = 500 \ \mu A$ CLKin_SELX_TYPE = 3, 4, or 6 Status_LDX_TYPE = 3, 4, or 6 RESET_TYPE = 3, 4, or 6		C	.4	V
DIGITAL OUT	PUTS (SDIO)					
V _{OH}	High-Level Output Voltage	I _{OH} = -500 μA; During SPI read. SDIO_RDBK_TYPE = 0	V _{CC} - 0.4			V
V _{OL}	Low-Level Output Voltage	I _{OL} = 500 μA; During SPI read. SDIO_RDBK_TYPE = 0 or 1		C	.4	V
DIGITAL INPU	ITS (CLKinX_SEL, RESET/GPO, SYNC, S	CK, SDIO, and CS*)				
VIH	High-Level Input Voltage		1.2			V
VIL	Low-Level Input Voltage			C	.5	V
DIGITAL INPU	IT (CLKinX_SEL)					
		CLKin_SELX_TYPE = 0 (High Impedance)	-5		5	
I _{IH}	High-Level Input Current $V_{IH} = V_{CC}$	CLKin_SELX_TYPE = 1 (Pull up)	-5		5	μA
		CLKin_SELX_TYPE = 2 (Pull-down)	10		30	
		CLKin_SELX_TYPE = 0 (High Impedance)	-5		5	
I _{IL}	Low-Level Input Current $V_{IL} = 0 V$	CLKin_SELX_TYPE = 1 (Pull up)	-40		-5	μA
		CLKin_SELX_TYPE = 2 (Pull-down)	-5		5	
DIGITAL INPU	IT (RESET/GPO)					
IIH	High-Level Input Current $V_{IH} = V_{CC}$	RESET_TYPE = 2 (Pull-down)	10		30	μA
		RESET_TYPE = 0 (High Impedance)	-5		5	
I _{IL}	Low-Level Input Current $V_{IL} = 0 V$	RESET_TYPE = 1 (Pull up)	-40		-5	μA
		RESET_TYPE = 2 (Pull-down)	-5		5	
DIGITAL INPU	IT (SYNC)					
I _{IH}	High-Level Input Current	V _{IH} = V _{CC}			25	μA
IIL	Low-Level Input Current	V _{IL} = 0 V	-5		5	μA
DIGITAL INPU	ITS (SCK, SDIO, CS*)					
I _{IH}	High-Level Input Current	V _{IH} = V _{CC}	-5		5	μA
IIL	Low-Level Input Current	$V_{IL} = 0 V$	-5		5	μA

(22) For OSCout when driven by OSCin, assumes OSCin has 50% input duty cycle.
(23) For any device clock with an odd divide value, assumes selected clock output has DCLKX_Y_DCC = 1 to enable duty cycle correction.

6.6 Timing Requirements

	DIGITAL INPUT TIMING	MIN	NOM MAX	UNIT
td _S	Setup time for SDI edge to SCLK rising edge	20		ns
td _H	Hold time for SDI edge to SCLK rising edge	10		ns
t _{SCLK}	Period of SCLK	200 ⁽¹⁾		ns
t _{HIGH}	High width of SCLK	60		ns
t _{LOW}	Low width of SCLK	60		ns
tc _S	Setup time for CS* falling edge to SCLK rising edge	20		ns
tc _H	Hold time for CS* rising edge from SCLK rising edge	20		ns
td _V	SCLK falling edge to valid read back data		60	ns

(1) 5 MHz

6.7 Timing Diagram

Register programming information on the SDIO pin is clocked into a shift register on each rising edge of the SCK signal. On the rising edge of the CS* signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/µs is recommended for these signals. After programming is complete the CS* signal should be returned to a high state. If the SCK or SDIO lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

4-cwire mode read back has same timing as SDIO pin.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.



図 1. SPI Timing Diagram





6.8 Typical Characteristics – Clock Output AC Characteristics

Jitter from 100 Hz to 100 MHz = 63.6 fs rms.

Output is CLKout4 as CML 32 mA with 68-nH to $20-\Omega$ DC bias.

Other settings are CLKout4_5_IDL = 1 and CLKout4_5_BYP = 1.

PLL2 Loop Filter R2 = 470 Ω , C2 = 150 nF, Charge Pump = 3200 μ A.

Reference is R&S SMA100B Signal Generator with option SMAB - B711 through Prodyn BIB-100G Balun to OSCin.

図 2. PLL2 with VCO1 Performance at 2500 MHz With 312.5-MHz OSCin/Phase Detector Frequency





Typical Characteristics – Clock Output AC Characteristics (continued)

Jitter from 100 Hz to 100 MHz = 67 fs rms.

Output is CLKout4 as CML 32 mA with 68-nH to $20-\Omega$ DC bias.

Other settings are CLKout4_5_IDL = 1 and CLKout4_5_BYP = 1.

PLL2 Loop Filter R2 = 470 Ω , C2 = 150 nF, Charge Pump = 3200 μ A.

Reference is R&S SMA100B Signal Generator with option SMAB - B711 through Prodyn BIB-100G Balun to OSCin.

図 3. PLL2 with VCO1 Performance at 3200 MHz With 320-MHz OSCin/Phase Detector Frequency



7 Parameter Measurement Information

7.1 Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at V_{CPout} = V_{CC} - ΔV

I2 = Charge Pump Sink Current at V_{CPout} = V_{CC}/2

- I3 = Charge Pump Sink Current at V_{CPout} = ΔV
- I4 = Charge Pump Source Current at V_{CPout} = V_{CC} Δ V

I5 = Charge Pump Source Current at $V_{CPout} = V_{CC}/2$

I6 = Charge Pump Source Current at $V_{CPout} = \Delta V$

 ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

7.1.1 Charge Pump Output Current Magnitude Variation vs Charge Pump Output Voltage

$$I_{CPout} Vs V_{CPout} = \frac{||1| - ||3|}{||1| + ||3|} \times 100\%$$
$$= \frac{||4| - ||6|}{||4| + ||6|} \times 100\%$$

7.1.2 Charge Pump Sink Current vs Charge Pump Output Source Current Mismatch

$$I_{CPout}$$
 Sink Vs I_{CPout} Source = $\frac{|12| - |15|}{|12| + |15|} \times 100\%$

7.1.3 Charge Pump Output Current Magnitude Variation vs Ambient Temperature

$$I_{CPout} Vs T_{A} = \frac{|I_{2}||_{T_{A}} - |I_{2}||_{T_{A}} = 25^{\circ}C}{|I_{2}||_{T_{A}} = 25^{\circ}C} \times 100\%$$
$$= \frac{|I_{5}||_{T_{A}} - |I_{5}||_{T_{A}} = 25^{\circ}C}{|I_{5}||_{T_{A}} = 25^{\circ}C} \times 100\%$$



7.2 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

 \bowtie 4 illustrates the two different definitions side-by-side for inputs and \bowtie 5 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

 V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).



Refer to application note AN-912 Common Data Transmission Parameters and their Definitions (SNLA036) for more information.



8 Detailed Description

8.1 Overview

The LMK04832 device is very flexible to meet many application requirements. Use cases include dual loop, dual loop 0-delay nested, dual loop 0-delay cascaded, single loop, single loop 0-delay, and clock distribution.

The device may be used in JESD204B systems by providing a device clock and SYSREF to target devices, however traditional (non-JESD204B) systems are possible by programming pairs of outputs to share the clock divider or any mix of JESD204B and traditional.

8.1.1 Differences to LMK0482x

The LMK04832 is pin-to-pin compatible with LMK0482x. The LMK04832 can be substituted directly into an existing LMK0482x hardware design. However, if a CML output is to be used on LMK04832, then $50-\Omega$ pullups to V_{CC} are required. For higher amplitude on high frequency CML outputs, use 68 nH on each output pin to a common to 20 ohms to Vcc. The LMK04832 does support LVPECL20 and LVPECL16 modes, but best performance is achieved with CML outputs in bypass mode. Division of up to 1023 is supported by DCLKx_DIV and each output clock can be a DEVCLK or a SYSREF. In addition, some programming updates are required from LMK04828 to LMK04832, particularly for controlling the clock output groups.

8.1.2 Jitter Cleaning

The dual loop PLL architecture of the LMK04832 provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 typically uses a narrow loop bandwidth (typically 10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This cleaned reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (typically 50 kHz to 200 kHz). The loop bandwidth for PLL2 is chosen to take advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO.

Ultra-low jitter is achieved by allowing the phase noise of the external VCXO to dominate the final output phase noise at low offset frequencies and the phase noise of the internal VCO to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

8.1.3 JEDEC JESD204B Support

The LMK04832 provides support for JEDEC JESD204B. The LMK04832 clocks up to 7 JESD204B targets using 7 device clocks and 7 SYSREF clocks.

The LMK04832 allows every clock output to be configured as a device clock or SYSREF clock.

8.1.4 Clock Inputs

注 CLKin1 can be used as a reference for dual loop, single loop, or clock distribution mode, providing flexibility configuring the device for different operation modes from one clock input..

8.1.4.1 Three Redundant PLL1 Reference Inputs

The LMK04832 has up to three reference clock inputs for PLL1. They are CLKin0, CLKin1, and CLKin2. Automatic or manual switching can occur between the inputs.

CLKin0, CLKin1, and CLKin2 each have their own PLL1 R dividers allowing clock switching references of different frequencies.



Overview (continued)

CLKin1 is shared for use as an external 0-delay feedback (FBCLKin), or for use with an external VCO (Fin).

CLKin2 is shared for use as OSCout. To use CLKin2 as an input power down OSCout, see VCO_MUX, OSCout MUX, OSCout FMT.

Fast manual switching between reference clocks and holdover is possible with external pins CLKin_SEL0 and CLKin_SEL1.

8.1.4.2 PLL2 Reference Inputs

In dual loop configurations, the PLL2 reference is from OSCin. However, in single PLL2 loop operation, it is also possible to use any of the three CLKins of PLL1 as a reference to PLL2.

8.1.4.3 Clock Distribution Reference Input

For clock distribution mode, a reference signal is applied to the Fin1 pins for clock distribution. CLKin0 can be used to distribute a SYSREF signal through the device. In this use case, CLKin0 is re-clocked by CLKin1.

8.1.5 VCXO Buffered Output

The LMK04832 provides OSCout, which by power-on default is a buffered copy of the PLL1 feedback and PLL2 reference input at OSCin. This reference input is typically a low noise VCXO or XO. This output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the LMK04832 is programmed.

The OSCout buffer output type is programmable to LVDS, LVPECL, or LVCMOS.

The VCXO buffered output can be synchronized to the VCO clock distribution outputs by using Cascaded 0-Delay Mode.

8.1.6 Frequency Holdover

The LMK04832 supports holdover operation to keep the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established.

8.1.7 Internal VCOs

The LMK04832 has two internal VCOs. The output of the selected VCO is routed to the Clock Distribution Path. This same selection is also fed back to the PLL2 phase detector through a prescaler and N-divider.

8.1.8 External VCO Mode

The Fin1 input allows an external VCO to be used with PLL2 of the LMK04832. Using Fin1 input for external VCO prevents use of CLKin1 for other purposes.

8.1.9 Clock Distribution

The LMK04832 features a total of 14 PLL2 clock outputs driven from the internal or external VCO.

All clock outputs have programmable output types. They can be programmed to CML, LVPECL, LVDS, HSDS, or LCPECL. All odd clock outputs plus CLKout8 and CLKout10 may be programmed to LVCMOS.

If OSCout is included in the total number of clock outputs the LMK04832 is able to distribute up to 15 differential clocks. OSCout may be a buffered version of OSCin, DCLKout6, DCLKout8, or SYSREF. Its output format is programmable to LVDS, LVPECL, or LVCMOS.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

8.1.9.1 Clock Divider

The LMK04832 has 7 clock dividers. In a traditional clocking system each divider can drive two outputs. The divider range is 1 to 1023. Duty cycle correction may be enabled for the output. When the divider is used even clocks may not output CML.

Copyright © 2017–2018, Texas Instruments Incorporated



Overview (continued)

In a JESD204B system, one clock output is a device clock driven from the clock divider and the other paired clock is from the SYSREF divider. For connectivity flexibility, either the even or odd clock output may be driven by the clock divider or be the SYSREF output.

8.1.9.2 High Performance Divider Bypass Mode

Even clock outputs (CLKoutX) of the LMK04832 may bypass the clock divider to achieve the best possible noise floor and output swing. In this mode, the only usable output format is CML.

8.1.9.3 SYSREF Clock Divider

The SYSREF divider supports a divide range of 8 to 8191 (even and odd). There is no duty cycle correction for the SYSREF divider. The SYSREF output may be routed to all clock outputs.

8.1.9.4 Device Clock Delay

The device clocks support digital delay for phase adjustment of the clock outputs.

The digital delay allows outputs to be delayed from 8 to 1023 VCO cycles. The delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

The digital delay value takes effect on the clock output phase after a SYNC event.

8.1.9.5 Dynamic Digital Delay

The device clock dividers support a dynamic digital delay feature which allows the clock to be delayed by one full device clock cycle. With a single programming, an adjustment of up to 255 one cycle delays may occur. When making a multi-step adjustment, the adjustments are periodically applied to reduce impact to the clock.

Dynamic phase adjustments of half a clock distribution cycle are possible by half step.

The SYSREF digital delay value is reused for dynamic digital delay. To achieve a one cycle delay program the SYSREF digital delay value to one greater than half the SYSREF divide value.

8.1.9.6 SYSREF Delay: Global and Local

The SYSREF divider includes a digital delay block which allows a global phase shift with respect to the device clocks.

Each clock output pair includes a local SYSREF analog and digital delay for unique phase adjustment of each SYSREF clock.

The local analog delay allows for approximately 21-ps steps. Turning-on analog delay adds an additional 124ps of delay in the clock path. The digital delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

The local digital delay and half step allows a SYSREF output to be delayed from 1.5 to 11 clock distribution path cycles.

8.1.9.7 Programmable Output Formats

All LMK04832 clock outputs can be programmed to an LVDS, HSDS, LVPECL, or LCPECL output type. Odd clock outputs in addition to CLKout8 and CLKout10 may also be programmed to LVCMOS. All odd clock outputs can also be programmed to CML. When in bypass mode the even clock output may only be CML.

The OSCout can be programmed to an LVDS, LVPECL, or LVCMOS output type.

Any HSDS output type can be programmed to 6-mA or 8-mA amplitude levels.

Any LVPECL output type can be programmed to 1600-mVpp or 2000-mVpp amplitude levels. The 2000-mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000-mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

LCPECL allows for DC-coupling SYSREF to low voltage JESD204B targets.



Overview (continued)

8.1.9.8 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay.

The SYNC event must occur for digital delay values to take effect.

8.1.10 0-Delay

The LMK04832 supports two types of 0-delay.

- 1. Cascaded 0-delay
- 2. Nested 0-delay

Cascaded 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL2 input clock (OSCin) to the phase of a clock selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKout6, CLKout8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKin port. The FB_MUX selects the feedback source. Because OSCin has a fixed deterministic phase relationship to the feedback clock, OSCout will also have a fixed deterministic phase relationship to the feedback clock (CLKinX) also has a fixed deterministic phase relationship to PLL2 input clock (OSCin); this results in a fixed deterministic phase relationship between all clocks from CLKinX to the clock outputs.

Nested 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL1 input clock (CLKinX) to the phase of a clock selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKout6, CLKout8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKin port. The FB_MUX selects the feedback source.

Without using 0-delay mode, there will be n possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

8.1.11 Status Pins

The LMK04832 provides status pins which can be monitored for feedback or in some cases used for input depending upon device programming. For example:

- The CLKin_SEL0 pin may indicate the LOS (loss-of-signal) for CLKin0.
- The CLKin_SEL1 pin may be an input for selecting the active clock input.
- The Status_LD1 pin may indicate if the device is locked.
- The Status_LD2 pin may indicate if PLL2 is locked.

The status pins can be programmed to a variety of other outputs including PLL divider outputs, combined PLL lock detect signals, PLL1 Vtune railing, readback, and so forth. Refer to the *Register Maps* section of this data sheet for more information.



JAJSFI6C-FEBRURAY 2017-REVISED MAY 2018

www.tij.co.jp

8.2 Functional Block Diagram

☑ 6 illustrates the high level LMK04832 block diagram.



図 6. High Level LMK04832 Block Diagram



Functional Block Diagram (continued)



Copyright $\ensuremath{\mathbb{C}}$ 2017, Texas Instruments Incorporated

図 7. Device and SYSREF Clock Output Block

TEXAS INSTRUMENTS

www.tij.co.jp

Functional Block Diagram (continued)



Copyright © 2017, Texas Instruments Incorporated





8.3 Feature Description

8.3.1 Synchronizing PLL R Dividers

In some cases, it is necessary to synchronize PLL R dividers to enable determinism of clocks outputs to inputs. This typically is required when the fraction Total PLL N divide / Total PLL R divide does not reduce to N / 1

8.3.1.1 PLL1 R Divider Synchronization

It is possible to use the CLKin0 or SYNC pin to synchronize the PLL1 R divider. In either case, the PLL1 R divider is armed for reset, then the rising sync edge arrives from either SYNC pin or CLKin0. After the PLL1 R divider is armed, PLL1 is unlocked until the synchronization edge arrives and allows the divider to operate and the PLL to lock. The procedure to synchronize PLL1 R is as follows:

- 1. Setup device for synchronizing PLL1 R:
 - PLL1R_SYNC_EN = 0x1
 - PLL1R_SYNC_SRC = 0x1 (SYNC pin) or 0x2 (CLKin0)
 - CLKin0_DEMUX = 0x2 (PLL1)
 - $CLKin1_DEMUX = 0x2$ (PLL1)
 - CLKin0_TYPE = 0x1 (MOS) for DC-coupled or CLKin0_TYPE = 0x0 (Bipolar) for AC-coupled
- 2. Arm PLL1 R divider for synchronization
 - PLL1R_RST = 1, then 0.
 - PLL1 is unlocked.
- 3. Send rising edge on SYNC pin or CLKin0.
 - PLL1 R divider is released from reset and PLL1 relocks.

It is necessary to meet a setup and hold time when CLKin0 or SYNC pin goes high to ensure deterministic reset of the PLL1 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL1 R synchronization.

8.3.1.2 PLL2 R Divider Synchronization

The SYNC pin must be used to synchronized the PLL2 R divider. When PLL2R_SYNC_EN = 1, as long as the SYNC pin is held high, the PLL2 R divider is held in reset. When the SYNC pin is returned low, the divider is allowed to continue dividing. While PLL2R_SYNC_EN = 1 and SYNC pin is high PLL2 is unlocked.

It is necessary to meet a setup and hold time when SYNC pin goes low to ensure deterministic reset of the PLL2 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL2 R synchronization.



Feature Description (continued)

8.3.2 SYNC/SYSREF

The SYNC and SYSREF signals share the same SYNC/SYSREF Clock Distribution path. To properly use SYNC and/or SYSREF for JESD204B it is important to understand the SYNC/SYSREF system. Z 7 illustrates the detailed diagram of a clock output block with SYNC circuitry included. Z 8 illustrates the interconnects and highlights some important registers used in controlling the device for SYNC/SYSREF purposes.

To reset or synchronize a divider, the following conditions must be met:

- 1. SYNC_EN must be set. This ensures proper operation of the SYNC circuitry.
- 2. SYSREF_MUX and SYNC_MODE must be set to a proper combination to provide a valid SYNC/SYSREF signal.
 - If SYSREF block is being used, the SYSREF_PD bit must be clear.
 - If the SYSREF Pulser is being used, the SYSREF_PLSR_PD bit must be clear.
 - For each CLKoutX or CLKoutY being used for SYSREF, the respective SCLKX_Y_PD bit must be cleared.
- DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits must be clear to power up the digital delay circuitry used during SYNC to cause deterministic phase between the device clock dividers and the global SYSREF divider.
- The SYNC_DISX bit must be clear to allow SYNC/SYSREF signal to divider circuit. The SYSREF_MUX
 register selects the SYNC source which resets the SYSREF/CLKoutX dividers provided the corresponding
 SYNC_DISX bit is clear.
- 5. Other bits which impact the operation of SYNC such as SYNC_1SHOT_EN may be set as desired.
- 6. After these dividers are synchronized, the DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits may be set to save current. Clearing them to power up may disrupt the output clock phase.

	ssible combinations	1 illustrates the some	ns of SYSREF MUX	and SYNC MOD
--	---------------------	------------------------	------------------	--------------

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
SYNC Disabled	0	0	CLKin0_DEMUX ≠ 0	No SYNC will occur.
Pin or SPI SYNC	1	0	CLKin0_DEMUX ≠ 0	Basic SYNC functionality, SYNC pin polarity is selected by SYNC_POL. To achieve SYNC through SPI, toggle the SYNC_POL bit.
Differential input SYNC	х	0 or 1	CLKin0_DEMUX = 0	Differential CLKin0 now operates as SYNC input.
JESD204B Pulser on pin transition.	2	2	SYSREF_PULSE_CNT sets pulse count	Produce SYSREF_PULSE_CNT programmed number of pulses on pin transition. SYNC_POL can be used to cause SYNC through SPI.
JESD204B Pulser on SPI programming.	3	2	SYSREF_PULSE_CNT sets pulse count	Programming SYSREF_PULSE_CNT register starts sending the number of pulses.
Re-clocked SYNC	1	1	SYSREF operational, SYSREF Divider as required for training frame size.	Allows precise SYNC for n-bit frame training patterns for non-JESD converters such as LM97600.
External SYSREF request	0	2	SYSREF_REQ_EN = 1 Pulser powered up	When SYNC pin is asserted, continuous SYSERF pulses occur. Turning on and off of the pulses is synchronized to prevent runt pulses from occurring on SYSREF.
Continuous SYSREF	Х	3	SYSREF_PD = 0 SYSREF_DDLY_PD = 0 SYSREF_PLSR_PD = 1 (1)	Continuous SYSREF signal.

表 1. Some Possible SYNC Configurations

(1) SCLKX_Y_PD = 0 as required per SYSREF output. This applies to any SYNC or SYSREF output on SCLKX_Y when SCLKX_Y_MUX = 1 (SYSREF output)



Feature Description (continued)

			J	
NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
Re-clocked SYSREF distribution	0	0	SYSREF_DDLY_PD = 1 SYSREF_PLSR_PD = 1 SYSREF_PD = 1.	Fan-out of CLKin0 reclocked to the clock distribution path.

表 1. Some Possible SYNC Configurations (continued)

注

Because the SYNC/SYSREF signal is reclocked by the Clock Distribution Path, an active clock must be present on the Clock Distribution Path (either from VCO or CLKin1/Fin pins in distribution mode) for SYNC to take effect.

	•	
-	±	
	т.	

Any device clock divider or the SYSREF divider which does not have the SYNC_DISX bit or SYNC_DISSYSREF bit set will reset while SYNC/SYSREF Distribution Path is high. This is especially important for the SYSREF divider which has the ability to reset itself if the SYNC_DISSYSREF = 0! **Be sure to set SYNC_DISX/SYNC_DISSYSREF bits as required.**

~ ~
Υ
·+-
<u> </u>

While using Divide-by-2 or Divide-by-3 for DCLK_X_Y_DIV, SYNC procedure requires to first program Divide-by-4 and then back to Divide-by-2 or Divide-by-3 before doing SYNC.

8.3.3 JEDEC JESD204B

8.3.3.1 How to Enable SYSREF

表 2 summarizes the bits needed to make SYSREF functionality operational.

表	2.	SY	'SR	EF	Bits
---	----	----	-----	----	------

REGIS TER	FIELD	VALUE	DESCRIPTION
0x140	SYSREF_PD	0	Must be clear, power-up SYSREF circuitry including the SYSREF divider.
0x140	SYSREF_DDLY_ PD	0	Must be clear to power-up digital delay circuitry. Must be powered up during initial SYNC to ensure deterministic timing to other clock dividers.
0x143	SYNC_EN	1	Must be set, enable SYNC.
0x143	SYSREF_CLR	1 → 0	Do not hold local SYSREF DDLY block in reset except at start. Anytime SYSREF_PD = 1 because of user programming or device RESET, it is necessary to set SYSREF_CLR for 15 VCO clock cycles to clear the local SYSREF digital delay. Once cleared, SYSREF_CLR must be cleared to allow SYSREF to operate.

Enabling JESD204B operation involves synchronizing all the clock dividers with the SYSREF divider, then configuring the actual SYSREF functionality.

8.3.3.1.1 Setup of SYSREF Example

The following procedure is a programming example for a system which is to operate with a 3000-MHz VCO frequency. Use CLKout0 and CLKout2 to drive converters at 1500 MHz. Use CLKout4 to drive an FPGA at 150 MHz. Synchronize the converters and FPGA using a two SYSREF pulses at 10 MHz.

- 1. Program registers 0x000 to 0x555 (refer to *Recommended Programming Sequence*). Key to prepare for SYSREF operations:
 - a. Prepare for manual SYNC: SYNC_POL = 0, SYNC_MODE = 1, SYSREF_MUX = 0
 - b. Setup output dividers as per example: DCLK0_1_DIV and DCLK2_3_DIV = 2 for frequency of 1500 MHz. DCLK4_5_DIV = 20 for frequency of 150 MHz.

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



www.tij.co.jp

- c. Setup output dividers as per example: SYSREF_DIV = 300 for 10 MHz SYSREF
- d. Setup SYSREF: SYSREF_PD = 0, SYSREF_DDLY_PD = 0, DCLK0_1_DDLY_PD = 0, DCLK2_3_DDLY_PD = 0, DCLK4_5_DDLY_PD = 0, SYNC_EN = 1, SYSREF_PLSR_PD = 0, SYSREF_PULSE_CNT = 1 (2 pulses). SCLK0_1_PD = 0, SCLK2_3_PD = 0, SCLK4_5_PD = 0
- e. Clear Local SYSREF DDLY: SYSREF_CLR = 1.
- 2. Establish deterministic phase relationships between SYSREF and Device Clock for JESD204B:
 - a. Set device clock and SYSREF divider digital delays: DCLK0_1_DDLY, DCLK2_3_DDLY, DCLK4_5_DDLY, and SYSREF_DDLY.
 - b. Set device clock digital delay half steps: DCLK0_1_HS, DCLK2_3_HS, DCLK4_5_HS.
 - c. Set SYSREF clock digital delay as required to achieve known phase relationships: SCLK0_1_DDLY, SCLK2_3_DDLY, and SCLK4_5_DDLY. If half step adjustments are required SCLK0_1_HS, SCLK2_3_HS, and SCLK4_5_HS.
 - d. To allow SYNC to affect dividers: SYNC_DIS0 = 0, SYNC_DIS2 = 0, SYNC_DIS4 = 0, SYNC_DISSYSREF = 0
 - e. Perform SYNC by toggling SYNC_POL = 1 then SYNC_POL = 0.
- 3. Now that dividers are synchronized, **disable SYNC from resetting these dividers.** It is not desired for SYSREF to reset it's own divider or the dividers of the output clocks.
 - a. Prevent SYNC (SYSREF) from affecting dividers: SYNC_DIS0 = 1, SYNC_DIS2 = 1, SYNC_DIS4 = 1, SYNC_DISSYSREF = 1.
- 4. Release reset of local SYSREF digital delay.
 - a. SYSREF_CLR = 0. Note this bit needs to be set for only 15 clock distribution path clocks after SYSREF_PD = 0.

5. Set SYSREF operation.

- a. Allow pin SYNC event to start pulser: SYNC_MODE = 2.
- b. Select pulser as SYSREF signal: SYSREF_MUX = 2.
- 6. **Complete!** Now asserting the SYNC pin, or toggling SYNC_POL will result in a series of 2 SYSREF pulses.

8.3.3.1.2 SYSREF_CLR

The local digital delay of the SCLKX_Y_DDLY is implemented as a shift buffer. To ensure no unwanted pulses occur at this SYSREF output at start-up, when using SYSREF, requires clearing the buffers by setting SYSREF_CLR = 1 for 15 VCO clock cycles. After a reset, this bit is set, so it must be cleared before SYSREF output is used.

If the SYSREF pulser is used. It is also required to set SYSREF_CLR = 1 for 15 VCO clock cycles after the SYSREF pulser is powered up.

8.3.3.2 SYSREF Modes

8.3.3.2.1 SYSREF Pulser

This mode allows for the output of 1, 2, 4, or 8 SYSREF pulses for every SYNC pin event or SPI programming. This implements the gapped periodic functionality of the JEDEC JESD204B specification.

When in SYSREF Pulser mode, programming the field SYSREF_PULSE_CNT in register 0x13E will result in the pulser sending the programmed number of pulses.

8.3.3.2.2 Continuous SYSREF

This mode allows for continuous output of the SYSREF clock.

注

Continuous operation of SYSREF is not recommended due to crosstalk from the SYSREF clock to device clock. JESD204B is designed to operate with a single burst of pulses to initialize the system at start-up, after which it is theoretically not required to send another SYSREF because the system will continue to operate with deterministic phases.



8.3.3.2.3 SYSREF Request

This mode allows an external source to synchronously turn on or off a continuous stream of SYSREF pulses using the SYNC/SYSREF_REQ pin.

Setup the mode by programming SYSREF_REQ_EN = 1 and SYSREF_MUX = 2 (Pulser). The pulser does not need to be powered for this mode of operation.

When the SYSREF_REQ pin is asserted, the SYSREF_MUX will synchronously be set to continuous mode providing continuous pulses at the SYSREF frequency until the SYSREF_REQ pin is unasserted and the final SYSREF pulse will complete sending synchronously.

8.3.4 Digital Delay

Digital (coarse) delay allows a group of outputs to be delayed by 8 to 1023 clock distribution path cycles. The delay step can be as small as half the period of the clock distribution path cycle by using the DCLKX_Y_HS bit. There are two different ways to use the digital delay:

- 1. Fixed digital delay
- 2. Dynamic digital delay

In both delay modes, the regular clock divider is substituted with an alternative divide value.

8.3.4.1 Fixed Digital Delay

Fixed digital delay value takes effect on the clock outputs after a SYNC event. As such, the outputs will be LOW for a while during the SYNC event. Applications that cannot accept clock breakup when adjusting digital delay during application run time should use dynamic digital delay to adjust phase.

8.3.4.1.1 Fixed Digital Delay Example

Assuming the device already has the following initial configurations, and the application should delay CLKout2 by one VCO cycle compared to CLKout0.

- VCO frequency = 2949.12 MHz
- CLKout0 = 368.64 MHz (DCLK0_1_DIV = 8, CLKout0_SRC_MUX = 0 (Device Clock))
- CLKout2 = 368.64 MHz (DCLK2_3_DIV = 8, CLKout2_SRC_MUX = 0 (Device Clock))

The following steps should be followed

- 1. Set DCLK0_1_DDLY = 8 and DCLK2_3_DDLY = 9. Static delay for each clock.
- 2. Set DCLK0_1_DDLY_PD = 0 and DCLK2_3_DDLY_PD = 0. Power up the digital delay circuit.
- 3. Set SYNC_DIS0 = 0 and SYNC_DIS2 = 0. Allow the outputs to be synchronized.
- 4. Perform SYNC by asserting, then unasserting SYNC. Either by using SYNC_POL bit or the SYNC pin.
- 5. Now that the SYNC is complete, to save power it is allowable to power down DCLK0_1_DDLY_PD = 1 and/or DCLK2_3_DDLY_PD = 1.
- 6. Set SYNC_DIS0 = 1 and SYNC_DIS2 = 1. Prevent the output from being synchronized, very important for steady-state operation when using JESD204B.



LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



8.3.4.2 Dynamic Digital Delay

Dynamic digital delay allows the phase of clocks to be changed with respect to each other with little impact to the clock signal.

For the device clock dividers this is accomplished by substituting the regular clock divider with an alternate divide value of one larger than the regular divider for one cycle. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT field for all outputs with DDLYdX_EN = 1.

For the SYSREF divider an alternate divide value will be substituted for the regular divide value. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT if DDLYd_SYSREF_EN = 1. To achieve one cycle delay as is done for the device clock dividers, set the SYSREF_DDLY value to one greater than SYSREF_DIV+SYSREF_DIV/2. For example, for a SYSREF divider of 100, to achieve 1 cycle delay, SYSREF_DIV = 100 + 50 + 1 = 151.

While using the Dynamic Digital Delay feature, CLKin_OVERRIDE must be set to 0.

- By programming a larger alternate divider (delay) value, the phase of the adjusted outputs are delayed with respect to the other clocks.
- By programming a smaller alternate divider (delay) value, the phase of the adjusted outputs are advanced with respect to the other clocks.

8.3.4.3 Single and Multiple Dynamic Digital Delay Example

In this example, two separate adjustments are made to the device clocks. In the first adjustment, a single delay of 1 VCO cycle occurs between CLKout2 and CLKout0. In the second adjustment, two delays of 1 VCO cycle occur between CLKout2 and CLKout0. At this point in the example, CLKout2 is delayed 3 VCO cycles behind CLKout0.

Assuming the device already has the following initial configurations:

- VCO frequency: 2949.12 MHz
- CLKout0 = 368.64 MHz, DCLK0_1_DIV = 8
- CLKout2 = 368.64 MHz, DCLK2_3_DIV = 8

The following steps illustrate the example above:

- 1. Set DCLK2_3_DDLY = 4. First part of delay for CLKout2.
- 2. Set DCLK2_3_DDLY_PD = 0. Enable the digital delay for CLKout2.
- 3. Set DDLYd0_EN = 0 and DDLYd2_EN = 1. Enable dynamic digital delay for CLKout2 but not CLKout0.
- 4. Set DDLYd_STEP_CNT = 1. This begins the **first adjustment.**

Before step 4, CLKout2 clock edge is aligned with CLKout0.

After step 4, CLKout2 counts nine clock distribution path cycles to the next rising edge, one greater than the divider value, effectively delaying CLKout2 by one VCO cycle with respect to CLKout0. This is the first adjustment.

5. Set DDLYd_STEP_CNT = 2. This begins the **second adjustment.**

Before step 5, CLKout2 clock edge was delayed 1 clock distribution path cycle from DCLKout0.

After step 5, CLKout2 counts nine clock distribution path cycles twice, each time one greater than the divide value, effectively delaying CLKout2 by two clock distribution path cycles with respect to CLKout0. This is the second adjustment.



図 10. Single and Multiple Adjustment Dynamic Digital Delay Example

8.3.5 SYSREF to Device Clock Alignment

To ensure proper JESD204B operation, the timing relationship between the SYSREF and the Device clock must be adjusted for optimum setup and hold time as shown in 2 11. The global SYSREF digital delay (SYSREF DDLY), local SYSREF digital delay (SCLKX Y DDLY), local SYSREF half step (SCLKX Y HS), and local SYSREF analog delay (SCLKX_Y_ADLY, SCLK2_3_ADLY_EN) can be adjusted to provide the required setup and hold time between SYSREF and Device Clock. It is also possible to adjust the device clock digital delay (DCLKX Y DDLY) and half step (DCLK0 1 HS, DCLK0 1 DCC) to adjust phase with respect to SYSREF.



図 11. SYSREF to Device Clock Timing alignment

Depending on the DCLKout_X path settings, local SCLK_X_Y_DDLY might need adjustment factor. Following equation can be used to calculate the required Digital Delay Values to align SYSREF to the corresponding DCLKout:

SYSREF_DDLY = DCLKX_Y_DDLY - 1 + DCLK_DIV_ADJUST + DCLK_HS_ADJUST - SCLK_X_Y_DDLY (1)

SYSREF DDLY > 7; SCLK X Y DDLY > 1.

DCLKX_Y_DIV	DCLK_DIV_ADJUST
>6	0
6	-1

表 3. DCLK_DIV_ADJUST





LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018 TEXAS INSTRUMENTS

www.tij.co.jp

表 3. DCLK_DIV_ADJUST (continued)

DCLKX_Y_DIV	DCLK_DIV_ADJUST
5	3
4	0
3 (1)	-2
2 (1)	-2

(1) Refer to the SYNC requirement SYNC/SYSREF

表 4. DCLK_HS_ADJUST

DCLK & HS	DCLK_HS_ADJUST
0	0
1	1

For example, DCLKX_Y_DIV = 32, DCLKX_Y_DDLY = 10, DCC&HS = 1;

SYSREF_DDLY=10 - 1 + 0 + 1 - 2 = 8


8.3.6 Input Clock Switching

Manual, pin select, and automatic are three different kinds clock input switching modes can be selected according to the combination of bits as illustrated in 🛛 12.



図 12. CLKinX Input Reference

The following sections provide information about how the active input clock is selected and what causes a switching event in the various clock input selection modes.

8.3.6.1 Input Clock Switching - Manual Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 0, the active CLKin is selected by CLKin_SEL_MANUAL. Programming a value of 0, 1, or 2 to CLKin_SEL_MANUAL causes CLKin0, CLKin1, or CLKin2, respectively, to be the selected active input clock. In this mode, the EN_CLKinX bits are overriden such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0.

If holdover is entered in this mode by setting CLKin_SEL_MANUAL = 3, then the device will re-lock to the selected CLKin upon holdover exit.

8.3.6.2 Input Clock Switching - Pin Select Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the active CLKin is selected by the CLKin_SEL# and Status_LD1 pins.

Configuring Pin Select Mode

The CLKin_SEL0_TYPE must be programmed to an input value for the CLKin_SEL0 pin to function as an input for pin select mode.

The CLKin_SEL1_TYPE must be programmed to an input value for the CLKin_SEL1 pin to function as an input for pin select mode.

The polarity of the clock input select pins can be inverted with the CLKin_SEL_PIN_POL bit.

The pin select mode overrides the EN_CLKinX bits such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0. To switch as fast as possible, keep the clock input buffers enabled (EN_CLKinX = 1) that could be switched to.

Copyright © 2017-2018, Texas Instruments Incorporated

TEXAS INSTRUMENTS

8.3.6.3 Input Clock Switching - Automatic Mode

When CLKin_SEL_AUTO_EN = 1, LOS_EN = 1, and HOLDOVER_EXIT_MODE = 0 (Exit based on LOS), the active clock is selected in priority order with CLKin0 being the highest priority, CLKin1 second, and CLKin2 third.

For a clock input to be eligible to be switched to, it must be enabled using EN_CLKinX. The LOS_TIMEOUT should also be set to a frequency below the input frequency.

To ensure LOS is valid for AC-coupled inputs, the MOS mode must be set for the CLKin and no termination is allowed to be between the pins unless DC blocked, for example, no $100-\Omega$ termination across CLKin0 and CLKin0* pins on IC side of AC-coupling capacitors.

8.3.7 Digital Lock Detect

Both PLL1 and PLL2 support digital lock detect. Digital lock detect compares the phase between the reference path (R) and the feedback path (N) of the PLL. When the time error, which is phase error, between the two signals is less than a specified window size (ϵ) a lock detect count increments. When the lock detect count reaches a user specified value, PLL1_DLD_CNT or PLL2_DLD_CNT, lock detect is asserted true. Once digital lock detect to be asserted false. This is illustrated in 🛛 13.



図 13. Digital Lock Detect Flowchart

This incremental lock detect count feature functions as a digital filter to ensure that lock detect is not asserted for only a brief time when the phases of R and N are within the specified tolerance for only a brief time during initial phase lock.

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect signal can be monitored on the Status_LD1 or Status_LD2 pin. The pin may be programmed to output the status of lock detect for PLL1, PLL2, or both PLL1 and PLL2.

8.3.7.1 Calculating Digital Lock Detect Frequency Accuracy

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect feature can also be used with holdover to automatically exit holdover mode. See *Exiting Holdover* for more info.



8.3.8 Holdover

Holdover mode causes PLL2 to stay locked on frequency with minimal frequency drift when an input clock reference to PLL1 becomes invalid. While in holdover mode, the PLL1 charge pump is TRI-STATED and a fixed tuning voltage is set on CPout1 to operate PLL1 in open loop.

8.3.8.1 Enable Holdover

Program HOLDOVER_EN = 1 to enable holdover mode.

Holdover mode can be configured to set the CPout1 voltage upon holdover entry to a fixed user defined voltage $(EN_MAN_DAC = 1)$ or a tracked voltage $(EN_MAN_DAC = 0)$.

8.3.8.1.1 Fixed (Manual) CPout1 Holdover Mode

By programming MAN_DAC_EN = 1, then the MAN_DAC value will be set on the CPout1 pin during holdover.

The user can optionally enable CPout1 voltage tracking (TRACK_EN = 1), read back the tracked DAC value, then re-program MAN_DAC value to a user desired value based on information from previous DAC read backs. This allows the most user control over the holdover CPout1 voltage, but also requires more user intervention.

8.3.8.1.2 Tracked CPout1 Holdover Mode

By programming MAN_DAC_EN = 0 and TRACK_EN = 1, the tracked voltage of CPout1 is set on the CPout1 pin during holdover. When the DAC has acquired the current CPout1 voltage, the *DAC_Locked* signal is set which may be observed on Status_LD1 or Status_LD2 pins by programming PLL1_LD_MUX or PLL2_LD_MUX, respectively.

Updates to the DAC value for the Tracked CPout1 sub-mode occurs at the rate of the PLL1 phase detector frequency divided by (DAC_CLK_MULT × DAC_CLK_CNTR).

The DAC update rate should be programmed for \leq 100 kHz to ensure DAC holdover accuracy.

The ability to program slow DAC update rates, for example one DAC update per 4.08 seconds when using 1024kHz PLL1 phase detector frequency with DAC_CLK_MULT = 16,384 and DAC_CLK_CNTR = 255, allows the device to *look-back* and set CPout1 at a previous *good* CPout1 tuning voltage values before the event which caused holdover to occur.

The current voltage of DAC value can be read back using RB_DAC_VALUE, see RB_DAC_VALUE.

8.3.8.2 During Holdover

PLL1 is run in open-loop mode.

- PLL1 charge pump is set to TRI-STATE.
- PLL1 DLD is unasserted.
- The HOLDOVER status is asserted
- During holdover, if PLL2 was locked prior to entry of holdover mode, PLL2 DLD continues to be asserted.
- CPout1 voltage is set to:
 - a voltage set in the MAN_DAC register (MAN_DAC_EN = 1).
 - a voltage determined to be the last valid CPout1 voltage (MAN_DAC_EN = 0).
- PLL1 attempts to lock with the active clock input.

The HOLDOVER status signal can be monitored on the Status_LD1 or Status_LD2 pin by programming the PLL1_DLD_MUX or PLL2_DLD_MUX register to *Holdover Status*.

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018

(2)

(3)

8.3.8.3 Exiting Holdover

Holdover mode can be exited in one of two ways.

- Manually, by programming the device from the host.
- Automatically, when the LOS signal unasserts for a clock that provides a valid input to PLL1.

8.3.8.4 Holdover Frequency Accuracy and DAC Performance

When in holdover mode, PLL1 runs in open loop and the DAC sets the CPout1 voltage. If *fixed CPout1* mode is used, then the output of the DAC is dependent upon the MAN_DAC register. If *tracked CPout1* mode is used, then the output of the DAC is approximately the same voltage at the CPout1 pin before holdover mode was entered. When using Tracked mode and MAN_DAC_EN = 1, the DAC value during holdover is loaded with the programmed value in MAN_DAC and not the tracked value.

When in Tracked CPout1 mode, the DAC has a worst-case tracking error of ± 2 LSBs once PLL1 tuning voltage is acquired. The step size is approximately 3.2 mV, therefore the VCXO frequency error during holdover mode caused by the DAC tracking accuracy is ± 6.4 mV × Kv, where Kv is the tuning sensitivity of the VCXO in use. Therefore, the accuracy of the system when in holdover mode in ppm is:

Holdover accuracy (ppm) = $\frac{\pm 6.4 \text{ mV} \times \text{Kv} \times 1e6}{\text{VCXO Frequency}}$

As an example, consider a system with a 19.2-MHz clock input, a 153.6-MHz VCXO with a Kv of 17 kHz/V. The accuracy of the system in holdover in ppm is:

±0.71 ppm = ±6.4 mV × 17 kHz/V × 1e6 / 153.6 MHz

It is important to account for this frequency error when determining the allowable frequency error window to cause holdover mode to exit.

8.3.9 PLL2 Loop Filter

PLL2 has an integrated loop filter of C1i = 60 pF, R3 = 2400 Ω , C3 = 50 pF, R4 = 200 Ω and C4 = 10 pF as shown in 🛛 14. Loop filter components C1, C2, and R2 can be solved using TI software. See $\overline{\tau}/(\tau R \cdot t)$ for more information.

LMK04832

CPout2

 \ge R2

C1



R3

C1i

R4

vco





8.4 Device Functional Modes

8

The following section describes the settings to enable various modes of operation for the LMK04832.

The LMK04832 is a flexible device that can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

8.4.1 DUAL PLL

8.4.1.1 Dual Loop

☑ 15 illustrates the typical use case of the LMK04832 in dual loop mode. In dual loop mode, the reference to PLL1 is from CLKin0, CLKin1, or CLKin2. An external VCXO is used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO by using a narrow loop bandwidth. The VCXO may be buffered through the OSCout port. The VCXO is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to seven divide/delay blocks which drive up to 14 clock outputs.

Hitless switching and holdover functionality are optionally available when the input reference clock is lost. Holdover works by forcing a DAC voltage to the tuning voltage of the VCXO.

It is also possible to use an external VCO in place of PLL2's internal VCO. In this case one less CLKin is available as a reference as CLKin1 is used for external Fin input.



図 15. Simplified Functional Block Diagram for Dual Loop Mode

8.4.1.2 Dual Loop With Cascaded 0-Delay

☑ 16 illustrates the use case of cascaded 0-delay dual loop mode. This configuration differs from dual loop mode ☑ 15 in that the feedback for PLL2 is driven by a clock output instead of the VCO output directly.

It is also possible to use an external VCO in place of the internal VCO of the PLL2, but one less CLKin is available as a reference and the external 0-delay feedback is not available.

LMK04832

JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



Device Functional Modes (continued)





8.4.1.3 Dual Loop With Nested 0-Delay

☑ 17 illustrates the use case of nested 0-delay dual loop mode. This configuration is similar to the dual PLL in ☑ 15 except that the feedback to the first PLL is driven by a clock output. The PLL2 reference OSCin is not deterministic to the CLKin or feedback clock.



図 17. Simplified Functional Block Diagram for Nested 0-Delay Dual Loop Mode



Device Functional Modes (continued)

8.4.2 Single PLL

8.4.2.1 PLL2 Single Loop

☑ 18 illustrates the use case of PLL2 single loop mode. When used with a high-frequency clean reference performance as good as dual loop mode may be achieved. Traditionally the OSCin is used as a reference to PLL2, but it is also possible to use CLKinX as a reference to PLL2.





8.4.2.2 PLL2 With External VCO

Adding an external VCO is possible using the CLKin1/Fin input port. The input may be single-ended or differential. At high frequency the input impedance to Fin is low, a resistive pad is recommended for matching.



2 19. Simplified Functional Block Diagram for Single Loop Mode With External VCO



Device Functional Modes (continued)

8.4.3 Distribution Mode

20 illustrates the use case of distribution mode. As in all the other use cases, OSCin to OSCout can be used as a buffer to OSCin or from clock distribution path via CLKout6, CLKout8, or the SYSREF divider.

At high frequency, the input impedance to Fin is low and a resistive pad is recommended for matching.



20. Simplified Functional Block Diagram for Distribution Mode

8.5 Programming

The LMK04832 device is programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 15-bit address field (A14 to A0) and a 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes *high* to latch the contents into the shift register. It is recommended to program registers in numeric order (for example, 0x000 to 0x555 with exceptions noted in the *Recommended Programming Sequence*). Each register consists of one or more fields which control the device functionality. See the *Electrical Characteristics* section and \mathbb{Z} 1 for timing details.

8.5.1 Recommended Programming Sequence

Registers are generally programmed in numeric order with 0x000 being the first and 0x555 being the last register programmed. The recommended programming sequence from POR involves:

- 1. Program register 0x000 with RESET = 1.
- 2. Program defined registers from 0x000 to 0x165.
- 3. If PLL2 is used, program 0x173 with PLL2_PD and PLL2_PRE_PD clear to allow PLL2 to lock after PLL2_N is programmed.
- 4. Continue programming defined registers from 0x166 to 0x555.

注

When using the internal VCO, PLL2_N registers 0x166, 0x167, and 0x168 must be programmed after other PLL2 dividers are programed to ensure proper VCO frequency calibration. This is also true for PLL2_N_CAL registers 0x163, 0x164, 0x165 when PLL2_NCLK_MUX = 1. So if any divider such as PLL2_R is altered to change the VCO frequency, the VCO calibration must be run again by programming PLL2_N.

Power up PLL2 by setting PLL2_PRE_PD = 0 and PLL2_PD = 0 in register 0x173 before programming PLL2_N.



8.6 Register Maps

8.6.1 Register Map for Device Programming

 $\frac{1}{5}$ provides the register map for device programming. Any register can be read from the same data address it is written to.

ADDRESS [14:0]		DATA[7:0]						
23:8	7	6	5	4	3	2	1	0
0x000	RESET	0	0	SPI_3WIRE _DIS	0	0	0	0
0x002	0	0	0	0	0	0	0	POWER DOWN
0x003				ID_DEVI	CE_TYPE			
0x004				ID_PRC	DD[15:8]			
0x005				ID_PR	OD[7:0]			
0x006		ID_MASKREV						
0x00C	ID_VNDR[15:8]							
0x00D				ID_VN	DR[7:0]			
0x100				DCLK0_1	_DIV[7:0]			
0x101				DCLK0_1_	_DDLY[7:0]			
0x102	CLKout0_1_PD	CLKout0_1_OD L	CLKout0_1_IDL	DCLK0_1_DDL Y_PD	DCLK0_1_	_DDLY[9:8]	DCLK0_1	_DIV[9:8]
0x103	0	1	CLKout0_SRC_ MUX	DCLK0_1_PD	DCLK0_1_BYP	DCLK0_1_DCC	DCLK0_1_POL	DCLK0_1_HS
0x104	0	0	CLKout1_SRC_ MUX	SCLK0_1_PD	SCLK0_1_I	DIS_MODE	SCLK0_1_POL	SCLK0_1_HS
0x105	0 0 SCLK0_1_ADL Y_EN SCLK0_1_ADLY							
0x106	0	0 0 0 0 SCLK0_1_DDLY						
0x107	CLKout1_FMT CLKout0_FMT							
0x108				DCLK2_3	3_DIV[7:0]			
0x109		I	I	DCLK2_3_	_DDLY[7:0]		I	
0x10A	CLKout2_3_PD	CLKout2_3_OD L	CLKout2_3_IDL	DCLK2_3_DDL Y_PD	DCLK2_3_	_DDLY[9:8]	DCLK2_3	_DIV[9:8]
0x10B	0	1	CLKout2_SRC_ MUX	DCLK2_3_PD	DCLK2_3_BYP	DCLK2_3_DCC	DCLK2_3_POL	DCLK2_3_HS
0x10C	0	0	CLKout3_SRC_ MUX	SCLK2_3_PD	SCLK2_3_I	DIS_MODE	SCLK2_3_POL	SCLK2_3_HS
0x10D	0	0	SCLK2_3_ADL Y_EN		-	SCLK2_3_ADLY		
0x10E	0	0	0	0		SCLK2_	3_DDLY	
0x10F		CLKout	t3_FMT			CLKou	t2_FMT	
0x110				DCLK4_5	5_DIV[7:0]			
0x111				DCLK4_5_	_DDLY[7:0]			
0x112	CLKout4_5_PD	CLKout4_5_OD L	CLKout4_5_IDL	DCLK4_5_DDL Y_PD	DCLK4_5_	_DDLY[9:8]	DCLK4_5	_DIV[9:8]
0x113	0	1	CLKout4_SRC_ MUX	DCLK4_5_PD	DCLK4_5_BYP	DCLK4_5_DCC	DCLK4_5_POL	DCLK4_5_HS
0x114	0	0	CLKout5_SRC_ MUX	SCLK4_5_PD	SCLK4_5_I	DIS_MODE	SCLK4_5_POL	SCLK4_5_HS
0x115	0	0 0 SCLK4_5_ADL Y_EN SCLK4_5_ADLY						
0x116	0	0	0	0		SCLK4_	5_DDLY	
0x117		CLKout	t5_FMT			CLKou	t4_FMT	
0x118				DCLK6_7	_DIV[7:0]			
0x119		DCLK6_7_DDLY[7:0]						

表 5. LMK04832 Register Map

Copyright © 2017–2018, Texas Instruments Incorporated



Register Maps (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x11A	CLKout6_7_PD	CLKout6_7_OD L	CLKout6_7_IDL	DCLK6_7_DDL Y_PD	DCLK6_7_	_DDLY[9:8]	DCLK6_7	_DIV[9:8]
0x11B	0	1	CLKout6_SRC_ MUX	DCLK6_7_PD	DCLK6_7_BYP	DCLK6_7_DCC	DCLK6_7_POL	DCLK6_7_HS
0x11C	0	0	CLKout7_SRC_ MUX	SCLK6_7_PD	SCLK6_7_	DIS_MODE	SCLK6_7_POL	SCLK6_7_HS
0x11D	0	0	SCLK6_7_ADL Y_EN			SCLK6_7_ADLY		
0x11E	0	0	0	0		SCLK6_	7_DDLY	
0x11F		CLKout	t7_FMT			CLKout	t6_FMT	
0x120				DCLK8_9	9_DIV[7:0]			
0x121		1	1	DCLK8_9	_DDLY[7:0]		1	
0x122	CLKout8_9_PD	CLKout8_9_OD L	CLKout8_9_IDL	DCLK8_9_DDL Y_PD	DCLK8_9_	_DDLY[9:8]	DCLK8_9	9_DIV[9:8]
0x123	0	1	CLKout8_SRC_ MUX	DCLK8_9_PD	DCLK8_9_BYP	DCLK8_9_DCC	DCLK8_9_POL	DCLK8_9_HS
0x124	0	0	CLKout9_SRC_ MUX	SCLK8_9_PD	SCLK8_9_	DIS_MODE	SCLK8_9_POL	SCLK8_9_HS
0x125	0	0	SCLK8_9_ADL Y_EN			SCLK8_9_ADLY		
0x126	0	0	0	0		SCLK8_	9_DDLY	
0x127	CLKout9_FMT CLKout8_FMT							
0x128				DCLK10_1	1_DIV[7:0]			
0x129		1	1	DCLK10_1	1_DDLY[7:0]		1	
0x12A	CLKout10_11_P D	CLKout10_11_ ODL	CLKout10_11_I DL	DCLK10_11_D DLY_PD	DCLK10_11	_DDLY[9:8]	DCLK10_1	1_DIV[9:8]
0x12B	0	1	CLKout10_SRC _MUX	DCLK10_11_PD	DCLK10_11_BY P	DCLK10_11_D CC	DCLK10_11_P OL	DCLK10_11_HS
0x12C	0	0	CLKout11_SRC _MUX	SCLK10_11_PD	SCLK10_11	_DIS_MODE	SCLK10_11_P OL	SCLK10_11_HS
0x12D	0	0	SCLK10_11_AD LY_EN		;	SCLK10_11_ADLY	/	
0x12E	0	0	0	0		SCLK10_	11_DDLY	
0x12F		CLKout	11_FMT			CLKout	10_FMT	
0x130				DCLK12_1	I3_DIV[7:0]			
0x131				DCLK12_1	3_DDLY[7:0]		1	
0x132	CLKout12_13_P D	CLKout12_13_ ODL	CLKout12_13_I DL	DCLK12_13_D DLY_PD	DCLK12_13	3_DDLY[9:8]	DCLK12_1	3_DIV[9:8]
0x133	0	1	CLKout12_SRC _MUX	DCLK12_13_PD	DCLK12_13_BY P	DCLK12_13_D CC	DCLK12_13_P OL	DCLK12_13_HS
0x134	0	0	CLKout13_SRC _MUX	SCLK12_13_PD	SCLK12_13	_DIS_MODE	SCLK12_13_P OL	SCLK12_13_HS
0x135	0	0	SCLK12_13_AD LY_EN		;	SCLK12_13_ADLY	/	
0x136	0	0	0	0		SCLK12_	13_DDLY	
0x137		CLKout	13_FMT	1		CLKout	12_FMT	
0x138	0	VCO_	_MUX	OSCout_MUX		OSCou	ut_FMT	
0x139	0	0	0	SYSREF_REQ_ EN	SYNC_BYPASS	0	SYSRE	F_MUX
0x13A	0	0	0		:	SYSREF_DIV[12:8]	
0x13B		I	I	SYSREF	_DIV[7:0]			
0x13C	0	0	0		S	YSREF_DDLY[12:	8]	
0x13D				SYSREF_	DDLY[7:0]			
0x13E	0	0	0	0	0	SI	SREF_PULSE_C	NT



Register Maps (continued)

ADDRESS [14:0]		DATA[7:0]						
23:8	7	6	5	4	3	2	1	0
0x13F	PLL2_RCLK_ MUX	0	PLL2_NCLK_ MUX	PLL1_N	CLK_MUX	FB_	MUX	FB_MUX_EN
0x140	PLL1_PD	VCO_LDO_PD	VCO_PD	OSCin_PD	SYSREF_GBL_ PD	SYSREF_PD	SYSREF_DDLY _PD	SYSREF_PLSR _PD
0x141	DDLYd_ SYSREF_EN	DDLYd12_EN	DDLYd10_EN	DDLYd8_EN	DDLYd6_EN	DDLYd4_EN	DDLYd2_EN	DDLYd0_EN
0x142				DDLYd_S	TEP_CNT			
0x143	SYSREF_CLR	SYNC_1SHOT_ EN	SYNC_POL	SYNC_EN	SYNC_PLL2_ DLD	SYNC_PLL1_ DLD	SYNC_	MODE
0x144	SYNC_DISSYS REF	SYNC_DIS12	SYNC_DIS10	SYNC_DIS8	SYNC_DIS6	SYNC_DIS4	SYNC_DIS2	SYNC_DIS0
0x145	0	PLL1R_SYNC_ EN	PLL1R_S	YNC_SRC	PLL2R_SYNC_ EN	0	0	0
0x146	CLKin_SEL_PIN _EN	CLKin_SEL_PIN _POL	CLKin2_EN	CLKin1_EN	CLKin0_EN	CLKin2_TYPE	CLKin1_TYPE	CLKin0_TYPE
0x147	CLKin_SEL_ AUTO_ REVERT_EN	CLKin_SEL_ AUTO_EN	CLKin_SEL	MANUAL	CLKin1_	DEMUX	CLKin0_	DEMUX
0x148	0	0		CLKin_SEL0_MU	X	(CLKin_SEL0_TYPE	
0x149	0	SDIO_RDBK_ TYPE		CLKin_SEL1_MU	x	(CLKin_SEL1_TYPE	
0x14A	0	0		RESET_MUX			RESET_TYPE	
0x14B	LOS_TI	LOS_TIMEOUT LOS_EN TRACK_EN HOLDOVER_ FORCE MAN_DAC_EN MAN_DAC[S				AC[9:8]		
0x14C		MAN_DAC[7:0]						
0x14D	0	0 DAC_TRIP_LOW						
0x14E	DAC_CL	K_MULT			DAC_TR	IP_HIGH		
0x14F				DAC_CL	K_CNTR			
0x150	0	CLKin_OVERRI DE	HOLDOVER_ EXIT_MODE	HOLDOVER_ PLL1_DET	LOS_EXTERNA L_INPUT	HOLDOVER_ VTUNE_DET	CLKin_SWITCH _CP_TRI	HOLDOVER_ EN
0x151	0	0			HOLDOVER_E	DLD_CNT[13:8]		
0x152				HOLDOVER_	DLD_CNT[7:0]	D// 0 01		
0x153	0	0			CLKin0	_R[13:8]		
0x154	0	0		CLKIN	J_R[7:0]	D[12:0]		
0x155	0	0		CI Kin		_K[13:0]		
0x150	0	0		CLNII		R[13·8]		
0x157	0	0		CI Kin:	2 R[7:0]	_[[[10:0]		
0x159	0	0		02	PLL1	N[13:8]		
0x15A		-		PLL1				
0x15B	PLL1_W	ND_SIZE	PLL1_CP_TRI	PLL1_CP_POL		PLL1_C	P_GAIN	
0x15C	0	0			PLL1_DLD	_CNT[13:8]		
0x15D		PLL1_DLD_CNT[7:0]						
0x15E	0	0 0 HOLDOVER_EXIT_NADJ						
0x15F			PLL1_LD_MUX PLL1_LD_TYPE					
0x160	0	0	0	0		PLL	.2_R	
0x161				PLI	_2_R			
0x162		PLL2_P		0	OSCin	_FREQ	PLL2_XTAL_EN	PLL2_REF_2X_ EN
0x163	0	0	0	0	0	0	PLL2_N_0	CAL[17:16]
0x164				PLL2_N_	CAL[15:8]			
0x165	PLL2_N_CAL[7:0]							

表 5. LMK04832 Register Map (continued)



Register Maps (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x166	0	0	0	0	0	0	PLL2_N	J[17:16]
0x167				PLL2_	N[15:8]			
0x168				PLL2_	_N[7:0]			
0x169	0	PLL2_W	ND_SIZE	PLL2_C	P_GAIN	PLL2_CP_POL	PLL2_CP_TRI	PLL2_DLD_EN
0x16A	0	0			PLL2_DLD	_CNT[13:8]		
0x16B		PLL2_DLD_CNT[7:0]						
0x16C	0	0	0	0	0	0	0	0
0x173	0	PLL2_PRE_PD	PLL2_PD	0	0	0	0	0
0x177			PLL1R_RST					
0x182	0	0	0	0	0	0	CLR_PLL1_LD_ LOST	CLR_PLL2_LD_ LOST
0x183	0	0	0	0	RB_PLL1_DLD_ LOST	RB_PLL1_DLD	RB_PLL2_DLD_ LOST	RB_PLL2_DLD
0x184	RB_DAC_VALUE[9:8] RB_CLKin2_ SEL			RB_CLKin1_ SEL	RB_CLKin0_ SEL	RB_CLKin2_ LOS	RB_CLKin1_ LOS	RB_CLKin0_ LOS
0x185	RB_DAC_VALUE[7:0]							
0x188	0	х	RB_ HOLDOVER	х	RB_DAC_RAIL	RB_DAC_HIGH	RB_DAC_LOW	RB_DAC_ LOCKED
0x555				SPI_I				

表 5. LMK04832 Register Map (continued)



8.6.2 Device Register Descriptions

The following section details the fields of each register, the Power-On-Reset Defaults, and specific descriptions of each bit.

In some cases similar fields are located in multiple registers. In this case specific outputs may be designated as X or Y. In these cases, the X represents even numbers from 0 to 12 and the Y represents odd numbers from 1 to 13. In the case where X and Y are both used in a bit name, then Y = X + 1.

8.6.2.1 System Functions

8.6.2.1.1 RESET, SPI_3WIRE_DIS

This register contains the RESET function and the ability to turn off 3-wire SPI mode. To use a 4-wire SPI mode, selecting SPI Read back in one of the output MUX settings. For example CLKin0_SEL_MUX or RESET_MUX. It is possible to have 3-wire and 4-wire readback at the same time.

BIT	NAME	POR DEFAULT	DESCRIPTION
7	RESET	0	0: Normal operation 1: Reset (automatically cleared)
6:5	NA	0	Reserved
4	SPI_3WIRE_DIS	0	Disable 3-wire SPI mode. 0: 3 Wire Mode enabled 1: 3 Wire Mode disabled
3:0	NA	NA	Reserved

表 6. Register 0x000

8.6.2.1.2 POWERDOWN

This register contains the POWERDOWN function.

表 7. Register 0x002

BIT	NAME	POR DEFAULT	DESCRIPTION
7:1	NA	0	Reserved
0	POWERDOWN	0	0: Normal operation 1: Power down device.

8.6.2.1.3 ID_DEVICE_TYPE

This register contains the product device type. This is read only register.

表 8. Register 0x003

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_DEVICE_TYPE	6	PLL product device type.

8.6.2.1.4 ID_PROD

These registers contain the product identifier. This is a read only register.

表 9. ID_PROD Field Registers

MSB	LSB
0x004[7:0] / ID_PROD[15:8]	0x005[7:0] / ID_PROD[7:0]

表 10. Registers 0x004 and 0x005

REGISTER	BIT	FIELD NAME	POR DEFAULT	DESCRIPTION
0x004	7:0	ID_PROD[15:8]	209 (0xD1)	MSB of the product identifier.
0x005	7:0	ID_PROD[7:0]	99 (0x63)	LSB of the product identifier.

8.6.2.1.5 ID_MASKREV

This register contains the IC version identifier. This is a read only register.

表 11. Register 0x006

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_MASKREV	112 (0x70)	IC version identifier for LMK04832.

8.6.2.1.6 ID_VNDR

These registers contain the vendor identifier. This is a read only register.

表 12. ID_VNDR Field Registers

MSB	LSB
0x00C[7:0] / ID_VNDR[15:8]	0x00D[7:0] / ID_VNDR[7:0]

表 13. Registers 0x00C, 0x00D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION
0x00C	7:0	ID_VNDR[15:8]	81 (0x51)	MSB of the vendor identifier.
0x00D	7:0	ID_VNDR[7:0]	4 (0x04)	LSB of the vendor identifier.



8.6.2.2 (0x100 - 0x138) Device Clock and SYSREF Clock Output Controls

8.6.2.2.1 DCLKX_Y_DIV

The device clock divider can drive up to two outputs, an even (X) and an odd (Y) clock output. Divide is a 10 bit number and split across two registers.

MSB	LSB
0x0102[1:0] = DCLK0_1_DIV[9:8]	0x100[7:0] = DCLK0_1_DIV[7:0]
0x010A[1:0] = DCLK2_3_DIV[9:8]	0x108[7:0] = DCLK2_3_DIV[7:0]
0x0112[1:0] = DCLK4_5_DIV[9:8]	0x110[7:0] = DCLK4_5_DIV[7:0]
0x011A[1:0] = DCLK6_7_DIV[9:8]	0x118[7:0] = DCLK6_7_DIV[7:0]
0x0122[1:0] = DCLK8_9_DIV[9:8]	0x120[7:0] = DCLK8_9_DIV[7:0]
0x012A[1:0] = DCLK10_11_DIV[9:8]	0x128[7:0] = DCLK10_11_DIV[7:0]
0x0132[1:0] = DCLK12_13_DIV[9:8]	0x130[7:0] = DCLK12_13_DIV[7:0]

表 14. DCLKX_Y_DIV Field Registers

表 15. Registers 0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION	
0x102, 0x10A, 0x112,	1.0		$X_Y = 0_1 \rightarrow 2$ $X_Y = 2_3 \rightarrow 4$ $X_Y = 4 \ 5 \rightarrow 8$	DCLKX_Y_DIV sets the divide value for the clock output, the divide may be even or odd. Both even or odd divides output a 50% duty cycle clock if duty cycle correction (DCC) is enabled.		
0x11A, 0x122	1.0	DOEIX[1_DIV[0.0]		Field Value	Divider Value	
0x12A, 0x132				0 (0x00)	Reserved	
0x100,			$X_Y = 6_7 \rightarrow 8$ $X_Y = 8_9 \rightarrow 8$ $X = 10 11 \rightarrow 8$	1 (0x01)	1 ⁽¹⁾	
0x108, 0x110				2 (0x02)	2	
0x118,	7:0	7:0 DCLKX_Y_DIV[7:0] X_Y =	$X Y = 12 13 \rightarrow 2$			
0x120, 0x128 and				1022 (0x3FE)	1022	
0x120, and 0x130				1023 (0x3FF)	1023	

(1) Duty cycle correction must also be enabled, DCLKX_Y_DCC = 1.

8.6.2.2.2 DCLKX_Y_DDLY

This register controls the digital delay for the device clock outputs.

表 16. DCLKX_Y_DDLY Field Registers

MSB	LSB
0x0102[2:3] = DCLK0_1_DDLY[9:8]	0x101[7:0] = DCLK0_1_DDLY[7:0]
0x010A[2:3] = DCLK2_3_DDLY[9:8]	0x109[7:0] = DCLK2_3_DDLY[7:0]
0x0112[2:3] = DCLK4_5_DDLY[9:8]	0x111[7:0] = DCLK4_5_DDLY[7:0]
0x011A[2:3] = DCLK6_7_DDLY[9:8]	0x119[7:0] = DCLK6_7_DDLY[7:0]
0x0122[2:3] = DCLK8_9_DDLY[9:8]	0x121[7:0] = DCLK8_9_DDLY[7:0]
0x012A[2:3] = DCLK10_11_DDLY[9:8]	0x129[7:0] = DCLK10_11_DDLY[7:0]
0x0132[2:3] = DCLK12_13_DDLY[9:8]	0x131[7:0] = DCLK12_13_DDLY[7:0]

表 17. Registers 0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION
0x102,		:3 DCLKX_Y_DDLY[9:8]		Static digital delay which takes effe	ct after a SYNC.
0x10A, 0x112				Field Value	Delay Values
0x112, 0x11A,	2:3			0 (0x00)	Reserved
0x122,				1 (0x01)	Reserved
0.12A, 0.132		0 DCLKX_Y_DDLY[7:0]	10 (0x0A)		
0x101, 0x109.	7:0			7 (0x07)	Reserved
				8 (0x08)	8
0x111,				9 (0x09)	9
0x119, 0x121, 0x129, 0x131					
				1022 (0x3FE)	1022
				1023 (0x3FF)	1023

Depending on the DCLK divide value, there may be an adjustment in phase delay required. 表 18 illustrate the impact of different divide values on the final digital delay.

表 18. Digital Delay Adjustment based on Divide Values

Divide Value	Digital delay Adjustment
2, 3	-2 ⁽¹⁾
4, 7 to 1023	0
5	+3
6	+1

(1) Before SYNC, program divider to Divide-by-4, then back to Divide-by-2 or Divide-by-3 to ensure '-2' delay relationship.

For example, 表 19 illustrates a system with clock outputs having divide values /2,/4,/5 and /6 to share a common edge.

表 19. Digital Delay Adjustment Illustration

Divide Value	Programmed DDLY	Actual DDLY
2	13	11
4	11	11
5	8	11
6	10	11



8.6.2.2.3 CLKoutX_Y_PD, CLKoutX_Y_ODL, CLKoutX_Y_IDL, DCLKX_Y_DDLY_PD, DCLKX_Y_DDLY[9:8], DCLKX_Y_DIV[9:8]

BIT	NAME	POR DEFAULT	DESCRIPTION
7	CLKoutX_Y_PD	1	Power down the clock group defined by X and Y. 0: Enabled 1: Power down entire clock group including both CLKoutX and CLKoutY.
6	CLKoutX_Y_ODL	0	Sets output drive level for clocks. This has no impact for the even clock output in bypass mode. 0: Normal operation 1: Higher current consumption and lower noise floor.
5	CLKoutX_Y_IDL	0	Sets input drive level for clocks. 0: Normal operation 1: Higher current consumption and lower noise floor.
4	DCLKX_Y_DDLY_PD	0	Powerdown the device clock digital delay circuitry. 0: Enabled 1: Power down static digital delay for device clock divider.
3:2	DCLKX_Y_DDLY[9:8]	0	MSB of static digital delay, see DCLKX_Y_DDLY.
1:0	DCLKX_Y_DIV[9:8]	CLKX_Y_DIV[9:8] 0 MSB of device clock divide value, see 表 15.	

表 20. Registers 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

8.6.2.2.4 CLKoutX_SRC_MUX, CLKoutX_Y_PD, DCLKX_Y_BYP, DCLKX_Y_DCC, DCLKX_Y_POL, DCLKX_Y_HS

These registers control the analog delay properties for the device clocks.

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	NA	1	Reserved
5	CLKoutX_SRC_MUX 0 Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF 1: SYSREF		Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF
4	CLKoutX_Y_PD	0	Power down the clock group defined by X and Y. 0: Enabled 1: Power down enter clock group X_Y.
3	DCLKX_BYP	0	 Enable high performance bypass path for even clock outputs. 0: CLKoutX not in high performance bypass mode. CML is not valid for CLKoutX_FMT. 1: CLKoutX in high performance bypass mode. Only CML clock format is valid.
2	DCLKX_Y_DCC	0	Duty cycle correction for device clock divider. Required for half step. 0: No duty cycle correction. 1: Duty cycle correction enabled.
1	DCLKX_Y_POL	0	Invert polarity of device clock output. This also applies to CLKoutX in high performance bypass mode. Polarity invert is a method to get a half-step phase adjustment in high performance bypass mode or /1 divide value. 0: Normal polarity 1: Invert polarity
0	DCLKX_Y_HS	0	Sets the device clock half step value. Must be set to zero (0) for a divide of 1. No effect if DCLKX_Y_DCC = 0. 0: No phase adjustment 1: Adjust device clock phase -0.5 clock distribution path cycles.

表 21. Registers 0x103, 0x10B, 0x113, 0x11B, 0x123, 0x12B, 0x133



8.6.2.2.5 CLKoutY_SRC_MUX, SCLKX_Y_PD, SCLKX_Y_DIS_MODE, SCLKX_Y_POL, SCLKX_Y_HS

These registers set the half step for the device clock, the SYSREF output MUX, the SYSREF clock digital delay, and half step.

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	CLKoutY_SRC_MUX	0	Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF	
4	SCLKX_Y_PD	1	Power down the SYSREF clock output circuitry. 0: SYSREF enabled 1: Power down SYSREF path for clock pair.	
			Set disable mode for clock outputs contassert when SYSREF_GBL_PD = 1.	trolled by SYSREF. Some cases will
		0	Field Value	Disable Mode
	SCLKX_Y_DIS_MODE		0 (0x00)	Active in normal operation
3:2			1 (0x01)	If SYSREF_GBL_PD = 1, the output is a logic low, otherwise it is active.
			2 (0x02)	If SYSREF_GBL_PD = 1, the output is a nominal Vcm voltage for odd clock channels ⁽¹⁾ and low for even clocks. Otherwise outputs are active.
			3 (0x03)	Output is a nominal Vcm voltage ⁽¹⁾
1	SCLKX_Y_POL	0	Sets the polarity of clock on SCLKX_Y when SYSREF clock output is selected with CLKoutX_MUX or CLKoutY_MUX. 0: Normal 1: Inverted	
0	SCLKX_Y_HS	0	Sets the local SYSREF clock half step value. 0: No phase adjustment 1: Adjust device SYSREF phase -0.5 clock distribution path cycles.	

表 22. Registers 0x104, 0x10C, 0x114, 0x11C, 0x124, 0x12C, 0x134

(1) If LVPECL mode is used with emitter resistors to ground, the output Vcm will be approximately 0 V, each pin will be approximately 0 V. If CML mode is used with pullups to V_{CC} , the output V_{CM} will be approximately V_{CC} V, each pin will be approximately V_{CC} V.

8.6.2.2.6 SCLKX_Y_ADLY_EN, SCLKX_Y_ADLY

These registers set the analog delay parameters for the SYSREF outputs.

表 23. Registers 0x105, 0x10D, 0x115, 0x11D, 0x125, 0x12D, 0x135

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	SCLKX_Y _ADLY_EN	0	Enables analog delay for the SYSREF output. 0: Disabled 1: Enabled	
	SCLKX_Y _ADLY	SCLKX_Y 0 _ADLY 0	SYSREF analog delay in approximately 2 adds an additional 125 ps in propagation	21 ps steps. Selecting analog delay delay. Range is 125 ps to 608 ps.
			Field Value	Delay Value
			0 (0x0)	125 ps
			1 (0x1)	146 ps (+21 ps from 0x00)
4:0			2 (0x2)	167 ps (+42 ps from 0x00)
			3 (0x3)	188 ps (+63 ps from 0x00)
			14 (0xE)	587 ps (+462 ps from 0x00)
			15 (0xF)	608 ps (+483 ps from 0x00)

8.6.2.2.7 SCLKX_Y_DDLY

表 24. Registers 0x106, 0x10E, 0x116, 0x11E, 0x126, 0x12E, 0x136

BIT	NAME	POR DEFAULT	DESCRIPTION
7:4	NA	0	Reserved
3:0	SCLKX_Y_DDLY	0	Set digital delay value for SYSREF clock (minimum 8)



8.6.2.2.8 CLKoutY_FMT, CLKoutX_FMT

The difference in the tables is that some of the clock outputs have inverted CMOS polarity settings.

BIT	NAME	POR DEFAULT	T DESCRIPTION			
			Set CLKoutY clock format			
			Field Value	Outp	out Format	
			0 (0x00)	Po	werdown	
			1 (0x01)		LVDS	
7:4			2 (0x02)	HSDS 6 mA		
			3 (0x03)	HS	DS 8 mA	
			4 (0x04)	LVPE	CL 1600 mV	
			5 (0x05)	LVPE	CL 2000 mV	
		0	6 (0x06)	L	CPECL	
		0	7 (0x07)	CN	1L 16 mA	
			8 (0x08)	CN	1L 24 mA	
			9 (0x09)	CM	1L 32 mA	
			10 (0x0A)	CMC	DS (Off/Inv)	
			11 (0x0B)	CMOS	CMOS (Norm/Off)	
			12 (0x0C)	CMC	CMOS (Inv/Inv)	
			13 (0x0D)	CMOS	CMOS (Inv/Norm)	
			14 (0x0E)	CMOS	S (Norm/Inv)	
			15 (0x0F)	CMOS	(Norm/Norm)	
		0	Set CLKoutX clock format			
			Field Value	Output Format DCLKX_BYP = 0	Output Format DCLKX_BYP = 1	
			0 (0x00)	Powerdown	Reserved	
			1 (0x01)	LVDS	Reserved	
			2 (0x02)	HSDS 6 mA	Reserved	
			3 (0x03)	HSDS 8 mA	Reserved	
			4 (0x04)	LVPECL 1600 mV	Reserved	
			5 (0x05)	LVPECL 2000 mV	Reserved	
3:0	CLKoutX_FMT		6 (0x06)	LCPECL	Reserved	
			7 (0x07)	Reserved	CML 16 mA	
			8 (0x08)	Reserved	CML 24 mA	
			9 (0x09)	Reserved	CML 32 mA	
			10 (0x0A)	CMOS (Off/Inv) ⁽¹⁾	Reserved	
			11 (0x0B)	CMOS (Norm/Off) ⁽¹⁾	Reserved	
			12 (0x0C)	CMOS (Inv/Inv) ⁽¹⁾	Reserved	
			13 (0x0D)	CMOS (Inv/Norm) ⁽¹⁾	Reserved	
			14 (0x0E)	CMOS (Norm/Inv) ⁽¹⁾	Reserved	
			15 (0x0F)	CMOS (Norm/Norm) ⁽¹⁾	Reserved	

表 25. Registers 0x107 (CLKout0_1), 0x11F (CLKout6_7), 0x12F (CLKout10_11)

(1) Only valid for CLKout10.

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018 NSTRUMENTS www.tij.co.jp

Texas

表 26. Registers 0x10F (CLKout2_3), 0x117 (CLKout4_5), 0x127 (CLKout8_9), 0x137 (CLKout12_13)

BIT	NAME	POR DEFAULT	DESCRIPTION				
			Set CLKoutY clock format				
			Field Value	Outp	out Format		
			0 (0x00)	Powerdown			
			1 (0x01)		LVDS		
			2 (0x02)	HS	DS 6 mA		
7:4			3 (0x03)	HS	DS 8 mA		
			4 (0x04)	LVPE	CL 1600 mV		
			5 (0x05)	LVPE	CL 2000 mV		
		0	6 (0x06)	L	CPECL		
	CLKOUTY_FM1	0	7 (0x07)	CM	IL 16 mA		
			8 (0x08)	CM	IL 24 mA		
			9 (0x09)	CM	IL 32 mA		
			10 (0x0A)	CMOS	S (Off/Norm)		
			11 (0x0B)	CMC	IOS (Inv/Off)		
			12 (0x0C)	CMOS	/OS (Norm/Norm)		
			13 (0x0D)	CMOS	MOS (Norm/Inv)		
			14 (0x0E)	CMOS	S (Inv/Norm)		
			15 (0x0F)	CMC	OS (Inv/Inv)		
			Set CLKoutX clock format				
			Field Value	Output Format DCLKX_BYP = 0	Output Format DCLKX_BYP = 1		
		0	0 (0x00)	Powerdown	Reserved		
			1 (0x01)	LVDS	Reserved		
			2 (0x02)	HSDS 6 mA	Reserved		
			3 (0x03)	HSDS 8 mA	Reserved		
			4 (0x04)	LVPECL 1600 mV	Reserved		
			5 (0x05)	LVPECL 2000 mV	Reserved		
3:0	CLKoutX_FMT		6 (0x06)	LCPECL	Reserved		
			7 (0x07)	Reserved	CML 16 mA		
			8 (0x08)	Reserved	CML 24 mA		
			9 (0x09)	Reserved	CML 32 mA		
			10 (0x0A)	CMOS (Off/Norm) ⁽¹⁾	Reserved		
			11 (0x0B)	CMOS (Inv/Off) ⁽¹⁾	Reserved		
			12 (0x0C)	CMOS (Norm/Norm) ⁽¹⁾	Reserved		
			13 (0x0D)	CMOS (Norm/Inv) ⁽¹⁾	Reserved		
			14 (0x0E)	CMOS (Inv/Norm) ⁽¹⁾	Reserved		
			15 (0x0F)	CMOS (Inv/Inv) ⁽¹⁾	Reserved		

(1) Only valid for CLKout8.



8.6.2.3 SYSREF, SYNC, and Device Config

8.6.2.3.1 VCO_MUX, OSCout_MUX, OSCout_FMT

BIT	NAME	POR DEFAULT	DESCRIPTION		
7	NA	0	Reserved		
			Selects clock distribution path source from VCO0, VCO1, or CLKin (externa VCO)		
			Field Value	VCO Selected	
6:5	VCO_MUX	2	0 (0x00)	VCO 0	
			1 (0x01)	VCO 1	
			2 (0x02)	Fin1 / CLKin1 (external VCO)	
			3 (0x03)	Reserved	
4	OSCout_MUX	0	Select the source for OSCout: 0: Buffered OSCin 1: Feedback Mux		
			Selects the output format of OSCout. W used as CLKin2.	hen powered down, these pins may be	
			Field Value	OSCout Format	
			0 (0x00)	Power down (CLKin2)	
			1 (0x01)	LVDS	
			2 (0x02)	Reserved	
			3 (0x03)	Reserved	
			4 (0x04)	LVPECL 1600 mVpp	
			5 (0x05)	LVPECL 2000 mVpp	
3:0	OSCout_FM1	4	6 (0x06)	LVCMOS (Norm / Inv)	
			7 (0x07)	LVCMOS (Inv / Norm)	
			8 (0x08)	LVCMOS (Norm / Norm)	
			9 (0x09)	LVCMOS (Inv / Inv)	
			10 (0x0A)	LVCMOS (Off / Norm)	
			11 (0x0B)	LVCMOS (Off / Inv)	
			12 (0x0C)	LVCMOS (Norm / Off)	
			13 (0x0D)	LVCMOS (Inv / Off)	
			14 (0x0E)	LVCMOS (Off / Off)	

表 27. Register 0x138

TEXAS INSTRUMENTS

www.tij.co.jp

8.6.2.3.2 SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX

This register sets the source for the SYSREF outputs. Refer to 🛛 8 and SYNC/SYSREF.

BIT	NAME	POR DEFAULT	DESCR	DESCRIPTION		
7:6	NA	0	Reserved	Reserved		
5	NA	0	Reserved			
4	SYSREF_REQ_EN	0	Enables the SYNC/SYSREF_REQ pin to continuous pulses. When using this feat SYSREF_MUX = 2 (Pulser).	Enables the SYNC/SYSREF_REQ pin to force the SYSREF_MUX = 3 for continuous pulses. When using this feature enable pulser and set SYSREF_MUX = 2 (Pulser).		
3	SYNC_BYPASS	0	Bypass SYNC polarity invert and other circuitry. 0: Normal 1: SYNC signal is bypassed			
2	NA	0	Reserved	Reserved		
			Selects the SYSREF source.			
			Field Value	SYSREF Source		
1.0		SYSREF_MUX 0	0 (0x00)	Normal SYNC		
1.0	SYSKEF_MUX		1 (0x01)	Re-clocked		
			2 (0x02)	SYSREF Pulser		
			3 (0x03)	SYSREF Continuous		

表 28. Register 0x139



8.6.2.3.3 SYSREF_DIV

These registers set the value of the SYSREF output divider.

表 29. SYSREF_DIV[12:0]

MSB	LSB
0x13A[4:0] = SYSREF_DIV[12:8]	0x13B[7:0] = SYSREF_DIV[7:0]

表 30. Registers 0x13A and 0x13B

REGISTER	BIT	NAME	POR DEFAULT	DESCRIF	PTION
0x13A	7:5	NA	0	Reserved	
		SYSREF_DIV[12:8]	12	Divide value for the SYSREF out	puts.
0x13A	4.0			Field Value	Divide Value
	4.0			0 to 7 (0x00 to 0x07)	Reserved
				8 (0x08)	8
0x13B		SYSREF_DIV[7:0]	0	9 (0x09)	9
	7.0				
	7:0			8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

8.6.2.3.4 SYSREF_DDLY

These registers set the delay of the SYSREF digital delay value.

表 31. SYSREF Digital Delay Register Configuration, SYSREF_DDLY[12:0]

MSB	LSB
0x13C[4:0] / SYSREF_DDLY[12:8]	0x13D[7:0] / SYSREF_DDLY[7:0]

表 32. Registers 0X13C and 0X13D

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION
0x13C	7:5	NA	0	Reserved	
	4:0	SYSREF_DDLY[12:8]	0	Sets the value of the SYSREF of	digital delay.
				Field Value	Delay Value
0x13C				0x00 to 0x07	Reserved
				8 (0x08)	8
	7:0	SYSREF_DDLY[7:0]	8	9 (0x09)	9
0.42D					
0813D				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

LMK04832

JAJSFI6C-FEBRURAY 2017-REVISED MAY 2018



8.6.2.3.5 SYSREF_PULSE_CNT

This register sets the number of SYSREF pulses if SYSREF is not in continuous mode. See SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX for further description of SYSREF's outputs.

Programming the register causes the specified number of pulses to be output if "SYSREF Pulses" is selected by SYSREF_MUX and SYSREF functionality is powered up.

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:2	NA	0	Reserved		
			Sets the number of SYSREF pulses ge See SYSREF_REQ_EN, SYNC_BYPA on SYSREF modes.	nerated when not in continuous mode. SS, SYSREF_MUX for more information	
	SYSREF_PULSE_CNT	SYSREF_PULSE_CNT 3	Field Value	Number of Pulses	
1:0			0 (0x00)	1 pulse	
			1 (0x01)	2 pulses	
			2 (0x02)	4 pulses	
			3 (0x03)	8 pulses	

表 33. Register 0x13E

8.6.2.3.6 PLL2_RCLK_MUX, PLL2_NCLK_MUX, PLL1_NCLK_MUX, FB_MUX, FB_MUX_EN

This register controls the feedback feature.

表 34. Register 0x13F

BIT	NAME	POR DEFAULT	DESCRIP	TION	
7	PLL2_RCLK_MUX	0	Selects the source for PLL2 reference. 0: OSCin 1: Currently selected CLKin.		
6	NA	0	Reserved		
5	PLL2_NCLK_MUX	0	Selects the input to the PLL2 N Divider 0: PLL2 Prescaler 1: Feedback Mux		
4:3	PLL1_NCLK_MUX	0	Selects the input to the PLL1 N Divider. 0: OSCin 1: Feedback Mux 2: PLL2 Prescaler		
		FB MUX 0	When in 0-delay mode, the feedback mux back into the PLL1 N Divider.	selects the clock output to be fed	
			Field Value	Source	
2:1	FB_MUX		0 (0x00)	CLKout6	
			1 (0x01)	CLKout8	
		FB_MUX_EN 0	2 (0x02)	SYSREF Divider	
			3 (0x03)	External	
0	FB_MUX_EN		When using 0-delay, FB_MUX_EN must b mux. 0: Feedback mux powered down 1: Feedback mux enabled	e set to 1 power up the feedback	



8.6.2.3.7 PLL1_PD, VCO_LDO_PD, VCO_PD, OSCin_PD, SYSREF_GBL_PD, SYSREF_PD, SYSREF_DDLY_PD, SYSREF_PLSR_PD

This register contains power down controls for OSCin and SYSREF functions.

BIT	NAME	POR DEFAULT	DESCRIPTION
7	PLL1_PD	1	Power down PLL1 0: Normal operation 1: Power down
6	VCO_LDO_PD	1	Power down VCO_LDO 0: Normal operation 1: Power down
5	VCO_PD	1	Power down VCO 0: Normal operation 1: Power down
4	OSCin_PD	0	Power down the OSCin port. 0: Normal operation 1: Power down
3	SYSREF_GBL_PD	0	Power down individual SYSREF outputs depending on the setting of SCLKX_Y_DIS_MODE for each SYSREF output. SYSREF_GBL_PD allows many SYSREF outputs to be controlled through a single bit. 0: Normal operation 1: Activate Power down Mode
2	SYSREF_PD	0	Power down the SYSREF circuitry and divider. If powered down, SYSREF output mode cannot be used. SYNC cannot be provided either. 0: SYSREF can be used as programmed by individual SYSREF output registers. 1: Power down
1	SYSREF_DDLY_PD	0	Power down the SYSREF digital delay circuitry. 0: Normal operation, SYSREF digital delay may be used. Must be powered up during SYNC for deterministic phase relationship with other clocks. 1: Power down
0	SYSREF_PLSR_PD	0	Powerdown the SYSREF pulse generator. 0: Normal operation 1: Powerdown

表 35. Register 0x140

8.6.2.3.8 DDLYdSYSREF_EN, DDLYdX_EN

This register enables dynamic digital delay for enabled device clocks and SYSREF when DDLYd_STEP_CNT is programmed.

BIT	NAME	POR DEFAULT	DESCR	IPTION		
7	DDLYd _SYSREF_EN	0	Enables dynamic digital delay on SYSREF outputs			
6	DDLYd12_EN	0	Enables dynamic digital delay on DCLKout12			
5	DDLYd10_EN	0	Enables dynamic digital delay on DCLKout10			
4	DDLYd8_EN	0	Enables dynamic digital delay on DCLKout8	0: Disabled		
3	DDLYd6_EN	0	Enables dynamic digital delay on DCLKout6	1: Enabled		
2	DDLYd4_EN	0	Enables dynamic digital delay on DCLKout4			
1	DDLYd2_EN	0	Enables dynamic digital delay on DCLKout2			
0	DDLYd0_EN	0	Enables dynamic digital delay on DCLKout0			

表 36. Register 0x141

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



8.6.2.3.9 DDLYd_STEP_CNT

This register sets the number of dynamic digital delay adjustments occur. Upon programming, the dynamic digital delay adjustment begins for each clock output with dynamic digital delay enabled. Dynamic digital delay can only be started by SPI.

Other registers must be set: SYNC_MODE = 3

BIT	NAME	POR DEFAULT	DESCRIPTION	
			Sets the number of dynamic digital dela	y adjustments that will occur.
			Field Value	Dynamic Digital Delay Adjustments
			0 (0x00)	No Adjust
			1 (0x01)	1 step
7:0	DDLYd_STEP_CNT	0	2 (0x02)	2 steps
			3 (0x03)	3 steps
			254 (0xFE)	254 steps
			255 (0xFF)	255 steps

表 37. Register 0x142



8.6.2.3.10 SYSREF_CLR, SYNC_1SHOT_EN, SYNC_POL, SYNC_EN, SYNC_PLL2_DLD, SYNC_PLL1_DLD, SYNC_MODE

This register sets general SYNC parameters such as polarization, and mode. Refer to $\boxtimes 8$ for block diagram. Refer to $\boxed{1}$ for using SYNC_MODE for specific SYNC use cases.

BIT	NAME	POR DEFAULT	DESC	RIPTION	
7	SYSREF_CLR	0	Except during SYSREF Setup Procedu always be programmed to 0. While this .	re (see SYNC/SYSREF), this bit should bit is set, extra current is used. Refer to	
6	SYNC_1SHOT_EN	0	SYNC one shot enables edge sensitive SYNC. 0: SYNC is level sensitive and outputs will be held in SYNC as long as SYNC is asserted. 1: SYNC is edge sensitive, outputs will be SYNCed on rising edge of SYNC. This results in the clock being held in SYNC for a minimum amount of time.		
5	SYNC_POL	0	Sets the polarity of the SYNC pin. 0: Normal 1: Inverted		
4	SYNC_EN	0	Enables the SYNC functionality. 0: Disabled 1: Enabled		
3	SYNC_PLL2_DLD	0	0: Off 1: Assert SYNC until PLL2 DLD = 1		
2	SYNC_PLL1_DLD	0	0: Off 1: Assert SYNC until PLL1 DLD = 1		
			Sets the method of generating a SYNC	ating a SYNC event.	
			Field Value	SYNC Generation	
			0 (0x00)	Prevent SYNC Pin, SYNC_PLL1_DLD flag, or SYNC_PLL2_DLD flag from generating a SYNC event.	
		SYNC_MODE 1	1 (0x01)	SYNC event generated from SYNC pin or if enabled the SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.	
1:0	SYNC_MODE		2 (0x02)	For use with pulser - SYNC/SYSREF pulses are generated by pulser block via SYNC Pin or if enabled SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.	
			3 (0x03)	For use with pulser - SYNC/SYSREF pulses are generated by pulser block when programming register 0x13E (SYSREF_PULSE_CNT) is written to (see).	

表 38. Register 0x143

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



www.tij.co.jp

8.6.2.3.11 SYNC_DISSYSREF, SYNC_DISX

SYNC_DISX will prevent a clock output from being synchronized or interrupted by a SYNC event or when outputting SYSREF.

BIT	NAME	POR DEFAULT	DESCRIPTION			
7	SYNC_DISSYSREF	0	Prevent the SYSREF clocks from becoming synchronized during a SYNC event. If SYNC_DISSYSREF is enabled it will continue to operate normally during a SYNC event.			
6	SYNC_DIS12	0				
5	SYNC_DIS10	0				
4	SYNC_DIS8	0	Prevent the device clock output from becoming synchronized during a SYNC			
3	SYNC_DIS6	0	event or SYSREF clock. If SYNC_DIS bit for a particular output is enabled then it will continue to operate normally during a SYNC event or SYSREF			
2	SYNC_DIS4	0	clock.			
1	SYNC_DIS2	0				
0	SYNC_DIS0	0				

表 39. Register 0x144

8.6.2.3.12 PLL1R_SYNC_EN, PLL1R_SYNC_SRC, PLL2R_SYNC_EN

These bits are used when synchronizing PLL1 and PLL2 R dividers. Refer to Synchronizing PLL R Dividers for more information.

表 40. Register 0x145	
----------------------	--

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6	PLL1R_SYNC_EN	0	Enable synchronization for PLL1 R divider 0: Not enabled 1: Enabled	
			Select the source for PLL1 R divider synchronization	
			Field Value	Definition
5:4 PLL1		0	0 (0x00)	Reserved
	PLLIK_STNC_SKC		1 (0x01)	SYNC Pin
			2 (0x02)	CLKin0
			3 (0x03)	Reserved
3	PLL2R_SYNC_EN	0	Enable synchronization for PLL2 R divider. Synchronization for PLL2 R always comes from the SYNC pin. 0: Not enabled 1: Enabled	
2:0	NA	0	Reserved	



8.6.2.4 (0x146 - 0x149) CLKin Control

8.6.2.4.1 CLKin_SEL_PIN_EN, CLKin_SEL_PIN_POL, CLKin2_EN, CLKin1_EN, CLKin0_EN, CLKin2_TYPE, CLKin1_TYPE, CLKin0_TYPE

This register has CLKin enable and type controls. See *Input Clock Switching* for more info on how clock input selection works.

BIT	NAME	POR DEFAULT	DESCF	RIPTION
7	CLKin_SEL_PIN_EN	0	Enables pin control according to 🛛 12.	
6	CLKin_SEL_PIN_POL	0	Inverts the CLKin polarity for use in pin select mode. 0: Active High 1: Active Low	
5	CLKin2_EN	0	Enable CLKin2 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
4	CLKin1_EN	1	Enable CLKin1 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
3	CLKin0_EN	1	Enable CLKin0 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
2	CLKin2_TYPE	0	There are two buffer types for CLKin0	
1	CLKin1_TYPE	0		1, and 2: bipolar and CMOS. Bipolar is
0	CLKin0_TYPE	0	0: Bipolar 1: MOS	like LVDS or LVPECL. CMOS is recommended for DC-coupled single ended inputs. When using bipolar, CLKinX and CLKinX* must be AC-coupled. When using CMOS, CLKinX and CLKinX* may be AC or DC-coupled if the input signal is differential. If the input signal is single-ended the used input may be either AC or DC-coupled and the unused input must AC grounded.

表 41. Register 0x146

8.6.2.4.2 CLKin_SEL_AUTO_REVERT_EN, CLKin_SEL_AUTO_EN, CLKin_SEL_MANUAL, CLKin1_DEMUX, CLKin0_DEMUX

表 42. Register 0x147

BIT	NAME	POR DEFAULT	DESCRIPTION		
7	CLKin_SEL_ AUTO_REVERT_EN	0	When in auto clock switching mode. If active clock is detected on higher priority clock, the clock input is immediately switched. Highest priority input is lowest numbered active clock input.		
6	CLKin_SEL_AUTO_EN	0	Enables pin control according to \boxtimes 12.		
			Selects the clock input when in manual	mode according to 🛛 12.	
			Field Value	Definition	
5:4	CLKin_SEL_MANUAL	MANUAL 1	0 (0x00)	CLKin0	
			1 (0x01)	CLKin1	
			2 (0x02)	CLKin2	
			3 (0x03)	Holdover	
			Selects where the output of the CLKin1	buffer is directed.	
			Field Value	CLKin1 Destination	
2.2		0	0 (0x00)	Fin	
3.2		U	1 (0x01)	Feedback Mux (0-delay mode)	
			2 (0x02)	PLL1	
			3 (0x03)	Off	

Copyright © 2017-2018, Texas Instruments Incorporated

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018 Texas Instruments

www.tij.co.jp

BIT	NAME	POR DEFAULT	DESCR	IPTION
			Selects where the output of the CLKin0	buffer is directed.
			Field Value	CLKin0 Destination
1.0		2	0 (0x00)	SYSREF Mux
1.0	CERIIO_DEMOX	3	1 (0x01)	Reserved
			2 (0x02)	PLL1
			3 (0x03)	Off

表 42. Register 0x147 (continued)

8.6.2.4.3 CLKin_SEL0_MUX, CLKin_SEL0_TYPE

This register has CLKin_SEL0 controls.

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:6	NA	0	Reserved		
			This set the output value CLKin_SEL0_TYPE is s	e of the CLKin_SEL0 pin. Thi et to an output mode	is register only applies if
			Field Value	Output	Format
			0 (0x00)	Logi	c Low
			1 (0x01)	CLKir	10 LOS
5:3	CLKin_SEL0_MUX	0	2 (0x02)	CLKin0	Selected
			3 (0x03)	DAC	Locked
			4 (0x04)	DAC	C Low
			5 (0x05)	DAC High	
			6 (0x06)	SPI Re	eadback
			7 (0x07)	Res	erved
			This sets the IO type of	the CLKin_SEL0 pin.	
			Field Value	Configuration	Function
			0 (0x00)	Input	Input mode, see Input
		2	1 (0x01)	Input with pullup resistor	Clock Switching - Pin
2:0	CLKin_SEL0_TYPE		2 (0x02)	Input with pulldown resistor	description of input mode.
			3 (0x03)	Output (push-pull)	
			4 (0x04)	Output inverted (push- pull)	Output modes; the CLKin_SEL0_MUX
			5 (0x05)	Reserved	outputs.
			6 (0x06)	Output (open-drain)	1 '

表 43. Register 0x148



8.6.2.4.4 SDIO_RDBK_TYPE, CLKin_SEL1_MUX, CLKin_SEL1_TYPE

This register has CLKin_SEL1 controls and register readback SDIO pin type.

表	44.	Re	gis	ter	0x1	49
			~			

BIT	NAME	POR DEFAULT	DESCRIPTION		
7	NA	0	Reserved		
6	SDIO_RDBK_TYPE	1	Sets the SDIO pin to open drain when during SPI readback in 3 wire mode. 0: Output, push-pull 1: Output, open drain.		
			This set the output value CLKin_SEL1_TYPE is set	of the CLKin_SEL1 pin. Thi to an output mode.	s register only applies if
			Field Value	Output	Format
			0 (0x00)	Logic	c Low
			1 (0x01)	CLKin	1 LOS
5:3	CLKin_SEL1_MUX	0	2 (0x02)	CLKin1	Selected
			3 (0x03)	DAC Locked	
			4 (0x04)	DAC	Clow
			5 (0x05)	DAC	High
			6 (0x06)	SPI Re	adback
			7 (0x07)	Rese	erved
			This sets the IO type of the	ne CLKin_SEL1 pin.	
			Field Value	Configuration	Function
		CLKin_SEL1_TYPE 2	0 (0x00)	Input	Input mode, see Input
			1 (0x01)	Input with pullup resistor	Clock Switching - Pin Select Mode for
2:0	CLKin_SEL1_TYPE		2 (0x02)	Input with pulldown resistor	description of input mode.
			3 (0x03)	Output (push-pull)	
			4 (0x04)	Output inverted (push- pull)	Output modes; see the CLKin_SEL1_MUX register for description of outputs.
			5 (0x05)	Reserved	
			6 (0x06)	Output (open-drain)	



8.6.2.5 RESET_MUX, RESET_TYPE

This register contains control of the RESET pin.

表。	45.	Register	0x14A
----	-----	----------	-------

BIT	NAME	POR DEFAULT	DESCRIPTION			
7:6	NA	0	Reserved			
	RESET_MUX	0	This sets the output value of the RESET pin. This register only applies if RESET_TYPE is set to an output mode.			
			Field Value	Output Format		
			0 (0x00)	Logic Low		
			1 (0x01)	Reserved		
5:3			2 (0x02)	CLKin2 Selected		
			3 (0x03)	DAC Locked		
			4 (0x04)	DAC Low		
			5 (0x05)	DAC High		
			6 (0x06)	SPI Readback		
	RESET_TYPE	2	This sets the IO type of the RESET pin.			
			Field Value	Configuration	Function	
			0 (0x00)	Input		
			1 (0x01)	Input with pullup resistor	Reset Mode Reset pin high = Reset	
2:0			2 (0x02)	Input with pulldown resistor		
			3 (0x03)	Output (push-pull)	Output modes; see the RESET_MUX register for description of outputs.	
			4 (0x04)	Output inverted (push- pull)		
			5 (0x05)	Reserved		
			6 (0x06)	Output (open-drain)		



8.6.2.6 (0x14B - 0x152) Holdover

8.6.2.6.1 LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8]

This register contains the holdover functions.

BIT	NAME	POR DEFAULT	DESCRIPTION		
	LOS_TIMEOUT	0	This controls the amount of time in which no activity on a CLKin forces a clock switch event.		
7:6			Field Value	Timeout	
			0 (0x00)	5 MHz typical	
			1 (0x01)	25 MHz typical	
			2 (0x02)	100 MHz typical	
			3 (0x03)	200 MHz typical	
5	LOS_EN	0	Enables the LOS (Loss-of-Signal) timeout control. Valid for MOS clock inputs. 0: Disabled 1: Enabled		
4	TRACK_EN	0	Enable the DAC to track the PLL1 tuning voltage, optionally for use in holdover mode. After device reset, tracking starts at DAC code = 512. Tracking can be used to monitor PLL1 voltage in any mode. 0: Disabled 1: Enabled, will only track when PLL1 is locked.		
3	HOLDOVER _FORCE	0	This bit forces holdover mode. When holdover mode is forced, if MAN_DAC_EN = 1, then the DAC will set the programmed MAN_DAC value. Otherwise the tracked DAC value will set the DAC voltage. 0: Disabled 1: Enabled.		
2	MAN_DAC_EN	1	This bit enables the manual DAC mode 0: Automatic 1: Manual		
1:0	MAN DAC[9:8]	2	See MAN_DAC for more information on	the MAN_DAC settings	

表 46. Register 0x14B

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018



www.tij.co.jp

8.6.2.6.2 MAN_DAC

These registers set the value of the DAC in holdover mode when used manually.

表 47. MAN_	DAC[9:0]
------------	----------

MSB				LSB			
0x14B[1:0]					0x14C[7:0]		
REGISTER	BIT	NAME	POR DEFAUL	OR DEFAULT DESCRIPTION		IPTION	
0x14B	7:2				See LOS_TIMEOUT, LOS_EN, HOLDOVER_FORCE, MAN_D/ information on these bits.	TRACK_EN, AC_EN, MAN_DAC[9:8] for	
		MAN_DAC[9:8]			Sets the value of the manual Damode.	AC when in manual DAC	
0x14B	1:0		2		Field Value	DAC Value	
					0 (0x00)	0	
					1 (0x01)	1	
	7:0	MAN_DAC[7:0]			2 (0x02)	2	
0.440			0				
UX 14C			0		1022 (0x3FE)	1022	
					1023 (0x3FF)	1023	

8.6.2.6.3 DAC_TRIP_LOW

This register contains the high value at which holdover mode is entered.

表 48. Register 0x14D

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:6	NA	0	Reserved		
			Voltage from GND at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.		
			Field Value	DAC Trip Value	
			0 (0x00)	1 x Vcc / 64	
			1 (0x01)	2 x Vcc / 64	
5:0	DAC_TRIP_LOW	0	2 (0x02)	3 x Vcc / 64	
			3 (0x03)	4 x Vcc / 64	
			61 (0x17)	62 x Vcc / 64	
			62 (0x18)	63 x Vcc / 64	
			63 (0x19)	64 x Vcc / 64	


8.6.2.6.4 DAC_CLK_MULT, DAC_TRIP_HIGH

This register contains the multiplier for the DAC clock counter and the low value at which holdover mode is entered.

BIT	NAME	POR DEFAULT	DESC	RIPTION	
			This is the multiplier for the DAC_CLK_CNTR which sets the rate at which the DAC value is tracked.		
			Field Value	DAC Multiplier Value	
7:6	DAC_CLK_MULT	0	0 (0x00)	4	
			1 (0x01)	64	
			2 (0x02)	1024	
			3 (0x03)	16384	
	DAC_TRIP_HIGH		Voltage from Vcc at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.		
			Field Value	DAC Trip Value	
			0 (0x00)	1 x Vcc / 64	
			1 (0x01)	2 x Vcc / 64	
5:0		0	2 (0x02)	3 x Vcc / 64	
			3 (0x03)	4 x Vcc / 64	
			61 (0x17)	62 x Vcc / 64	
			62 (0x18)	63 x Vcc / 64	
			63 (0x19)	64 x Vcc / 64	

表 49. Register 0x14E

8.6.2.6.5 DAC_CLK_CNTR

This register contains the value of the DAC when in tracked mode.

表 50. Register 0x14F

BIT	NAME	POR DEFAULT	DESCRIPTION		
		CNTR 127	This with DAC_CLK_MULT set the rate at which the DAC is updated. The update rate is = DAC_CLK_MULT * DAC_CLK_CNTR / PLL1 PDF		
			Field Value	DAC Value	
			0 (0x00)	0	
7:0	DAC_CLK_CNTR		1 (0x01)	1	
			2 (0x02)	2	
			3 (0x03)	3	
			253 (0xFD)	253	
			254 (0xFE)	254	
			255 (0xFF)	255	

8.6.2.6.6 CLKin_OVERRIDE, HOLDOVER_EXIT_MODE, HOLDOVER_PLL1_DET, LOS_EXTERNAL_INPUT, HOLDOVER_VTUNE_DET, CLKin_SWITCH_CP_TRI, HOLDOVER_EN

This register has controls for enabling clock in switch events.

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	CLKin _OVERRIDE	0	 When manual clock select is enabled, then CLKin_SEL_MANUAL = 0/1/2 selects a manual clock input. CLKin_OVERRIDE = 1 will force that clock input. CLKin_OVERRIDE = 1 is used with clock distribution mode for best performance. 0: Normal, no override. 1: Force select of only CLKin0/1/2 as specified by CLKin_SEL_MANUAL in manual mode. Dynamic digital delay will not operate.
5	HOLDOVER_ EXIT_MODE	0	 0: Exit based on LOS status. If clock is active by LOS, then begin exit. 1: Exit based on PLL1 DLD. When the PLL1 phase detector confirming valid clock.
4	HOLDOVER _PLL1_DET	0	This enables the HOLDOVER when PLL1 lock detect signal transitions from high to low. 0: PLL1 DLD does not cause a clock switch event 1: PLL1 DLD causes a clock switch event
3	LOS_EXTERNAL_INPUT	0	Use external signals for LOS status instead of internal LOS circuitry. CLKin_SEL0 pin is used for CLKin0 LOS, CLKin_SEL1 pin is used for CLKin1 LOS, and Status_LD1 is used for CLKin2 LOS. For any of these pins to be valid, the corresponding _TYPE register must be programmed as an input. 0: Disabled 1: Enabled
2	HOLDOVER_ VTUNE_DET	0	Enables the DAC Vtune rail detector. When the DAC achieves a specified Vtune, if this bit is enabled, the current clock input is considered invalid and an input clock switch event is generated. 0: Disabled 1: Enabled
1	CLKin_SWITCH_CP_TRI	0	Enable clock switching with tri-stated charge pump.0: Not enabled.1: PLL1 charge pump tri-states during clock switching.
0	HOLDOVER_EN	0	Sets whether holdover mode is active or not. 0: Disabled 1: Enabled

表 51. Register 0x150



8.6.2.6.7 HOLDOVER_DLD_CNT

表 52. HOLDOVER_DLD_CNT[13:0]

MSB	LSB
0x151[5:0] / HOLDOVER_DLD_CNT[13:8]	0x152[7:0] / HOLDOVER_DLD_CNT[7:0]

This register has the number of valid clocks of PLL1 PDF before holdover is exited.

表 53. Registers 0x151 and 0x152

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x151	7:6	NA	0	Reserved	
		HOLDOVER _DLD_CNT[13:8]	2	The number of valid clocks of F mode is exited.	PLL1 PDF before holdover
0x151	5:0			Field Value	Count Value
				0 (0x00)	0
				1 (0x01)	1
	7.0	7:0 HOLDOVER _DLD_CNT[7:0]	0	2 (0x02)	2
0.450					
0x152	7.0			16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

TEXAS INSTRUMENTS

www.tij.co.jp

8.6.2.7 (0x153 - 0x15F) PLL1 Configuration

8.6.2.7.1 CLKin0_R

表 54. CLKin0_R[13:0]

MSB	LSB
0x153[5:0] / CLKin0_R[13:8]	0x154[7:0] / CLKin0_R[7:0]

These registers contain the value of the CLKin0 divider.

表 55. Registers 0x153 and 0x154

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION	
0x153	7:6	NA	0	Reserved		
		CLKin0_R[13:8]	0	The value of PLL1 N counter w	hen CLKin0 is selected.	
0.450	5.0			Field Value	Divide Value	
00153	5:0			0 (0x00)	Reserved	
				1 (0x01)	1	
		7:0 CLKin0_R[7:0]	120	2 (0x02)	2	
0.454	7.0					
0X154	7:0			16382 (0x3FFE)	16382	
					16383 (0x3FFF)	16383

8.6.2.7.2 CLKin1_R

表 56. CLKin1_R[13:0]

MSB	LSB
0x155[5:0] / CLKin1_R[13:8]	0x156[7:0] / CLKin1_R[7:0]

These registers contain the value of the CLKin1 R divider.

表 57. Registers 0x155 and 0x156

REGISTER	BIT	NAME	POR DEFAULT	DESCR	RIPTION
0x155	7:6	NA	0	Reserved	
		CLKin1_R[13:8]	0	The value of PLL1 N counter w	hen CLKin1 is selected.
0,455	5.0			Field Value	Divide Value
02122	5.0			0 (0x00)	Reserved
				1 (0x01)	1
	7.0	0 CLKin1_R[7:0]	150	2 (0x02)	2
0.450					
02120	7:0			16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383



LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018

www.tij.co.jp

8.6.2.7.3 CLKin2_R

表 58. CLKin2_R[13:0]

MSB	LSB
0x157[5:0] / CLKin2_R[13:8]	0x158[7:0] / CLKin2_R[7:0]

表 59. Registers 0x157 and 0x158

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION
0x157	7:6	NA	0	Reserved	
		CLKin2_R[13:8]	0	The value of PLL1 N counter w	hen CLKin2 is selected.
0.457	5.0			Field Value	Divide Value
02157	5:0			0 (0x00)	Reserved
				1 (0x01)	1
		7:0 CLKin2_R[7:0]	150	2 (0x02)	2
0.450					
0x158	7:0			16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

8.6.2.7.4 PLL1_N

表 60. PLL1_N[13:0]

MSB	LSB
0x159[5:0] / PLL1_N[13:8]	0x15A[7:0] / PLL1_N[7:0]

These registers contain the N divider value for PLL1.

表 61. Registers 0x159 and 0x15A

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x159	7:6	NA	0	Reserved	
0x159 5:0				The value of PLL1 N counter.	
	5:0	PLL1_N[13:8]	0	Field Value	Divide Value
				0 (0x00)	Not Valid
				1 (0x01)	1
0x15A 7:				2 (0x02)	2
	7:0	7:0 PLL1_N[7:0]	120		
				4,095 (0xFFF)	4,095

TEXAS INSTRUMENTS

www.tij.co.jp

8.6.2.7.5 PLL1_WND_SIZE, PLL1_CP_TRI, PLL1_CP_POL, PLL1_CP_GAIN

This register controls the PLL1 phase detector.

BIT	NAME	POR DEFAULT	DESCRIPTION			
			PLL1_WND_SIZE sets the window size used for digital lock detect for PLL1. If the phase error between the reference and feedback of PLL1 is less than specified time, then the PLL1 lock counter increments.			
			Field Value	Definition		
7:6	PLL1_WND_SIZE	3	0 (0x00)	4 ns		
			1 (0x01)	9 ns		
			2 (0x02)	19 ns		
			3 (0x03)	43 ns		
5	PLL1_CP_TRI	0	This bit allows for the PLL1 charge pump output pin, CPout1, to be placed TRI-STATE. 0: PLL1 CPout1 is active 1: PLL1 CPout1 is at TRI-STATE			
4	PLL1_CP_POL	1	PLL1_CP_POL sets the charge pump polarity for PLL1. Many VCXOs use positive slope. A positive slope VCXO increases output frequency with increasing voltage. A negative slope VCXO decreases output frequency with increasing voltage. 0: Negative Slope VCO/VCXO 1: Positive Slope VCO/VCXO			
			This bit programs the PLL1 charge pum	p output current level.		
			Field Value	Gain		
			0 (0x00)	50 µA		
			1 (0x01)	150 µA		
3:0		1	2 (0x02)	250 μΑ		
	T LET_OF_OAIN	4	3 (0x03)	350 µA		
			4 (0x04)	450 µA		
			14 (0x0E)	1450 µA		
1			15 (0x0F)	1550 µA		

表 62. Register 0x15B



8.6.2.7.6 PLL1_DLD_CNT

表 63. PLL1_DLD_CNT[13:0]

MSB	LSB
0x15C[5:0] / PLL1_DLD_CNT[13:8]	0x15D[7:0] / PLL1_DLD_CNT[7:0]

This register contains the value of the PLL1 DLD counter.

表 64. Registers 0x15C and 0x15D

REGISTER	BIT	NAME	POR DEFAULT	DESCR	RIPTION
0x15C	7:6	NA	0	Reserved	
0x15C	5:0	PLL1_DLD _CNT[13:8]	32	The reference and feedback of window of phase error as specthis many phase detector cycle detect is asserted.	PLL1 must be within the ified by PLL1_WND_SIZE for s before PLL1 digital lock
	5.0			Field Value	Delay Value
				0 (0x00)	Reserved
				1 (0x01)	1
0x15D 7:0		7:0 PLL1_DLD _CNT[7:0]	0	2 (0x02)	2
	7:0			3 (0x03)	3
				16,382 (0x3FFE)	16,382
				16,383 (0x3FFF)	16,383

8.6.2.7.7 HOLDOVER_EXIT_NADJ

表 65. Register 0x15E

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	NA	0	Reserved
4:0	HOLDOVER_EXIT_NADJ	30	When holdover exists, PLL1 R counter and PLL1 N counter are reset. HOLDOVER_EXIT_NADJ is a 2s complement number which provides a relative timing offset between PLL1 R and PLL1 N divider.



8.6.2.7.8 PLL1_LD_MUX, PLL1_LD_TYPE

This register configures the PLL1 LD pin.

BIT	NAME		DESCRIPTION			
DII		FOR DEFAULT	This sate the output value of the Status			
			Field Value	MUX Value		
			0 (0x00)	Logic Low		
			1 (0x01)	PLL1 DLD		
			2 (0x02)	PLL2 DLD		
			3 (0x03)	PLL1 & PLL2 DLD		
			4 (0x04)	Holdover Status		
			5 (0x05)	DAC Locked		
			6 (0x06)	Reserved		
			7 (0x07)	SPI Readback		
7:3	PLL1_LD_MUX	1	8 (0x08)	DAC Rail		
			9 (0x09)	DAC Low		
			10 (0x0A)	DAC High		
			11 (0x0B)	PLL1_N		
			12 (0x0C)	PLL1_N/2		
			13 (0x0D)	PLL2_N		
			14 (0x0E)	PLL2_N/2		
			15 (0x0F)	PLL1_R		
			16 (0x10)	PLL1_R/2		
			17 (0x11)	PLL2_R ⁽¹⁾		
			18 (0x12)	PLL2_R/2 ⁽¹⁾		
			Sets the IO type of the Status_LD1 pin.			
			Field Value	ТҮРЕ		
			0 (0x00)	Input for External CLKin2 LOS		
			1 (0x01)	Input for External CLKin2 LOS (pullup)		
2:0	PLL1_LD_TYPE	_TYPE 6	2 (0x02)	Input for External CLKin2 LOS (pulldwn)		
			3 (0x03)	Output (push-pull)		
			4 (0x04)	Output inverted (push-pull)		
			5 (0x05)	Reserved		
			6 (0x06)	Output (open-drain)		

表 66. Register 0x15F

(1) Only valid when PLL2_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).



8.6.2.8 (0x160 - 0x16E) PLL2 Configuration

8.6.2.8.1 PLL2_R

表 67. PLL2_R[11:0]

MSB	LSB
0x160[3:0] / PLL2_R[11:8]	0x161[7:0] / PLL2_R[7:0]

This register contains the value of the PLL2 R divider.

表 68. Registers 0x160 and 0x161

REGISTER	BIT	NAME	POR DEFAULT	DESCR	RIPTION
0x160	7:4	NA	0	Reserved	
		PLL2_R[11:8]	0	Valid values for the PLL2 R div	ider.
0,460	2.0			Field Value	Divide Value
02160	3.0			0 (0x00)	Not Valid
				1 (0x01)	1
0x161		7:0 PLL2_R[7:0]	2	2 (0x02)	2
				3 (0x03)	3
	7:0				
				4,094 (0xFFE)	4,094
				4,095 (0xFFF)	4,095



8.6.2.8.2 PLL2_P, OSCin_FREQ, PLL2_REF_2X_EN

This register sets other PLL2 functions.

BIT	NAME	POR DEFAULT	DESCRIPTION		
			The PLL2 N Prescaler divides the output of the VCO as selected by Mode_MUX1 and is connected to the PLL2 N divider.		
			Field Value	Value	
			0 (0x00)	8	
			1 (0x01)	2	
7:5	PLL2_P	2	2 (0x02)	2	
			3 (0x03)	3	
			4 (0x04)	4	
			5 (0x05)	5	
			6 (0x06)	6	
			7 (0x07)	7	
			The frequency of the PLL2 reference inp (OSCin/OSCin* port) must be programm of the frequency calibration routine which frequency.	but to the PLL2 Phase Detector ed in order to support proper operation in locks the internal VCO to the target	
			Field Value	OSCin Frequency	
4.0		2	0 (0x00)	0 to 63 MHz	
4.2		3	1 (0x01)	>63 MHz to 127 MHz	
			2 (0x02)	>127 MHz to 255 MHz	
			3 (0x03)	Reserved	
			4 (0x04)	>255 MHz to 500 MHz	
			5 (0x05) to 7(0x07)	Reserved	
1	NA	0	Reserved		
0	PLL2_REF_2X_EN	PLL2_REF_2X_EN 1	Enabling the PLL2 reference frequency of detector frequencies on PLL2 than would VCXO frequency. Higher phase detector frequencies reduc the design of wider loop bandwidth filters 0: Doubler Disabled 1: Doubler Enabled	doubler allows for higher phase d normally be allowed with the given ces the PLL2 N values which makes s possible.	

表 69. Register 0x162



8.6.2.8.3 PLL2_N_CAL

PLL2_N_CAL[17:0]

PLL2 never uses 0-delay during frequency calibration. These registers contain the value of the PLL2 N divider used with PLL2 pre-scaler during calibration for cascaded 0-delay mode. Once calibration is complete, PLL2 will use PLL2_N value. Cascaded 0-delay mode occurs when PLL2_NCLK_MUX = 1.

表 70. PLL2_N_CAL[17:0]

MSB	—	LSB
0x163[1:0] / PLL2_N_CAL[17:16]	0x164[7:0] / PLL2_N_CAL[15:8]	0x165[7:0] / PLL2_N_CAL[7:0]

表 71. Registers 0x163, 0x164, and 0x165

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x163	7:2	NA	0	Reserved	
0,462	0.400 A.0 DIL		0	Field Value	Divide Value
0X163 1:0 PLL2_N_CAL[17:16	PLLZ_N_CAL[17:10]	0	0 (0x00)	Not Valid	
	7.0		0	1 (0x01)	1
UX 164	7.0	PLLZ_N_CAL[15:6]	0	2 (0x02)	2
0,465	7.0		10		
0x165	7.0	PLLZ_N_CAL[7:0]	12	262,143 (0x3FFFF)	262,143

8.6.2.8.4 PLL2_N

This register disables frequency calibration and sets the PLL2 N divider value. Programming register 0x168 starts a VCO calibration routine if PLL2_FCAL_DIS = 0.

表 72. PLL2_N[17:0]

MSB	—	LSB
0x166[1:0] / PLL2_N[17:16]	0x167[7:0] / PLL2_N[15:8]	0x168[7:0] / PLL2_N[7:0]

表 73. Registers 0x166, 0x167, and 0x168

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION
0x166	7:3	NA	0	Reserved	
0x166	1.0	PLL2_N[17:16]	0	Field Value	Divide Value
	1:0			0 (0x00)	Not Valid
0.407	0x167 7:0 PLL2_N[15:8]		0	1 (0x01)	1
02107		PLL2_N[15.6]		2 (0x02)	2
0x168	7.0	PLL2_N[7:0]	12		
	7.0			262,143 (0x3FFFF)	262,143

TEXAS INSTRUMENTS

www.tij.co.jp

8.6.2.8.5 PLL2_WND_SIZE, PLL2_CP_GAIN, PLL2_CP_POL, PLL2_CP_TRI

This register controls the PLL2 phase detector.

BIT	NAME	POR DEFAULT	DESCR	RIPTION
7	NA	0	Reserved	
			PLL2_WND_SIZE sets the window size the phase error between the reference specified time, then the PLL2 lock coun	used for digital lock detect for PLL2. If and feedback of PLL2 is less than ter increments.
6·5		2	Field Value	Maximum Phase Detector Frequency / Window Size
0.5	PLLZ_WIND_SIZE	2	0 (0x00)	Reserved
			1 (0x01)	320 MHz / 1 ns
			2 (0x02)	240 MHz / 1.8 ns
			3 (0x03)	160 MHz / 2.6 ns
			This bit programs the PLL2 charge pum also illustrates the impact of the PLL2 T PLL2_CP_GAIN.	p output current level. The table below RISTATE bit in conjunction with
		3	Field Value	Definition
4:3 PLL2_CP_GAIN	PLL2_CP_GAIN		0 (0x00)	Reserved
			1 (0x01)	Reserved
			2 (0x02)	1600 µA
			3 (0x03)	3200 µA
2	PLL2 CP POL	0	PLL2_CP_POL sets the charge pump p requires the negative charge pump pola positive slope. A positive slope VCO increases output negative slope VCO decreases output f	olarity for PLL2. The internal VCO arity to be selected. Many VCOs use frequency with increasing voltage. A requency with increasing voltage.
			Field Value	Description
			0	Negative Slope VCO/VCXO
			1	Positive Slope VCO/VCXO
1	PLL2_CP_TRI	0	PLL2_CP_TRI TRI-STATEs the output of the PLL2 charge pump. 0: Disabled 1: TRI-STATE	
0	PLL2_DLD_EN	0	PLL2 DLD circuitry is enabled when the to a lock detect status pin. PLL2_DLD_ circuitry without needing to provide PLL PLL2 DLD status to be read back using be used for other purposes. 0: PLL2 DLD circuitry is on only of PLL2 output from a Status_LD_MUX. 1: PLL2 DL D circuitry is forced on.	PLL2 DLD is used to provide an output EN allows enabling the PLL2 DLD 2 DLD to a status pin. This enables SPI while allowing the Status pins to 2 DLD or PLL1 + PLL2 DLD signal is

表 74. Register 0x169



8.6.2.8.6 PLL2_DLD_CNT

表 75. PLL2_DLD_CNT[13:0]

MSB	LSB
0x16A[5:0] / PLL2_DLD_CNT[13:8]	0x16B[7:0] / PLL2_DLD_CNT[7:0]

This register has the value of the PLL2 DLD counter.

表 76. Registers 0x16A and 0x16B

REGISTER	BIT	NAME	POR DEFAULT	DESCR	IPTION
0x16A	7	NA	0	Reserved	
0x16A	5:0	PLL2_DLD _CNT[13:8]	32	The reference and feedback of window of phase error as speci PLL2_DLD_CNT cycles before asserted.	PLL2 must be within the fied by PLL2_WND_SIZE for PLL2 digital lock detect is
				Field Value	Divide Value
				0 (0x00)	Not Valid
				1 (0x01)	1
	7:0	PLL2_DLD_CNT	0	2 (0x02)	2
				3 (0x03)	3
0x16B					
				16,382 (0x3FFE)	16,382
				16,383 (0x3FFF)	16,383

8.6.2.8.7 PLL2_LD_MUX, PLL2_LD_TYPE

This register sets the output value of the Status_LD2 pin.

BIT	NAME	POR DEFAULT	DESCRIPTION	
			This sets the output value of the Status_	LD2 pin.
			Field Value	MUX Value
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
7:3	PLL2_LD_MUX	0	8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N
			12 (0x0C)	PLL1_N/2
			13 (0x0D)	PLL2_N
			14 (0x0E)	PLL2_N/2
			15 (0x0F)	PLL1_R
			16 (0x10)	PLL1_R/2
			17 (0x11)	PLL2_R ⁽¹⁾
			18 (0x12)	PLL2_R/2 ⁽¹⁾
			Sets the IO type of the Status_LD2 pin.	
			Field Value	ТҮРЕ
			0 (0x00)	Reserved
			1 (0x01)	Reserved
2:0	PLL2_LD_TYPE	6	2 (0x02)	Reserved
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open drain)

表 77. Register 0x16E

(1) Only valid when PLL1_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

8.6.2.9 (0x16F - 0x555) Misc Registers

8.6.2.9.1 PLL2_PRE_PD, PLL2_PD

BIT	NAME	POR DEFAULT	DESCRIPTION			
7	N/A	0	Reserved			
6	PLL2_PRE_PD	1	Powerdown PLL2 prescaler 0: Normal Operation 1: Powerdown			
5	PLL2_PD	1	Powerdown PLL2 0: Normal Operation 1: Powerdown			
4:0	N/A	16	Reserved			

表 78. Register 0x173

8.6.2.9.2 PLL1R_RST

Refer to PLL1 R Divider Synchronization for more information on synchronizing PLL1 R divider.

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	NA	0	Reserved
5	PLL1R_RST	0	When set, PLL1 R divider will be held in reset. PLL1 will never lock with PLL1R_RST = 1. This bit is used in when synchronizing the PLL1 R divider. 0: PLL1 R divider normal operation. 1: PLL1 R divider held in reset.
4:0	NA	0	Reserved

表 79. Register 0x177

TEXAS INSTRUMENTS

www.tij.co.jp

8.6.2.9.3 CLR_PLL1_LD_LOST, CLR_PLL2_LD_LOST

表 80. Register 0x182

BIT	NAME	POR DEFAULT	DESCRIPTION
7:2	NA	0	Reserved
1	CLR_PLL1_LD_LOST	0	To reset RB_PLL1_LD_LOST, write CLR_PLL1_LD_LOST with 1 and then 0. 0: RB_PLL1_LD_LOST will be set on next falling PLL1 DLD edge. 1: RB_PLL1_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL1_LD_LOST to become set again.
0	CLR_PLL2_LD_LOST	0	To reset RB_PLL2_LD_LOST, write CLR_PLL2_LD_LOST with 1 and then 0. 0: RB_PLL2_LD_LOST will be set on next falling PLL2 DLD edge. 1: RB_PLL2_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL2_LD_LOST to become set again.

8.6.2.9.4 RB_PLL1_LD_LOST, RB_PLL1_LD, RB_PLL2_LD_LOST, RB_PLL2_LD

For PLL2 DLD read back to be valid, either PLL2 DLD or PLL1 + PLL2 DLD signal must be output from the status pins, or PLL2_DLD_EN bit must be set = 1.

BIT	NAME	POR DEFAULT	DESCRIPTION
7:4	N/A	0	Reserved
3	RB_PLL1_LD_LOST	0	This is set when PLL1 DLD edge falls. Does not set if cleared while PLL1 DLD is low.
2	RB_PLL1_LD	0	Read back 0: PLL1 DLD is low. Read back 1: PLL1 DLD is high.
1	RB_PLL2_LD_LOST	0	This is set when PLL2 DLD edge falls. Does not set if cleared while PLL2 DLD is low.
0	RB_PLL2_LD	0	PLL1_LD_MUX or PLL2_LD_MUX must select setting 2 (PLL2 DLD) for valid reading of this bit. Read back 0: PLL2 DLD is low. Read back 1: PLL2 DLD is high.

表 81. Register 0x183



8.6.2.9.5 RB_DAC_VALUE (MSB), RB_CLKinX_SEL, RB_CLKinX_LOS

This register provides read back access to CLKinX selection indicator and CLKinX LOS indicator. The 2 MSBs are shared with the RB_DAC_VALUE. See RB_DAC_VALUE section.

表 82. Register 0x184

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	RB_DAC_VALUE[9:8]		See RB_DAC_VALUE section.
5	RB_CLKin2_SEL		Read back 0: CLKin2 is not selected for input to PLL1. Read back 1: CLKin2 is selected for input to PLL1.
4	RB_CLKin1_SEL		Read back 0: CLKin1 is not selected for input to PLL1. Read back 1: CLKin1 is selected for input to PLL1.
3	RB_CLKin0_SEL		Read back 0: CLKin0 is not selected for input to PLL1. Read back 1: CLKin0 is selected for input to PLL1.
2	N/A		
1	RB_CLKin1_LOS		Read back 1: CLKin1 LOS is active. Read back 0: CLKin1 LOS is not active.
0	RB_CLKin0_LOS		Read back 1: CLKin0 LOS is active. Read back 0: CLKin0 LOS is not active.

8.6.2.9.6 RB_DAC_VALUE

Contains the value of the DAC for user readback.

表 83. RB_DAC_VALUE[9:0]

MSB	LSB
0x184 [7:6] / RB_DAC_VALUE[9:8]	0x185 [7:0] / RB_DAC_VALUE[7:0]

表 84. Registers 0x184 and 0x185

			-	
REGISTER	BIT	NAME	POR DEFAULT	
0x184	7:6	RB_DAC_ VALUE[9:8]	2	DAC value is 512 on power on reset, if PLL1 locks upon
0x185	7:0	RB_DAC_ VALUE[7:0]	0	power-up the DAC value will change.

8.6.2.9.7 RB_HOLDOVER

表 85. Register 0x188

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	N/A		Reserved
4	RB_HOLDOVER		Read back 0: Not in HOLDOVER. Read back 1: In HOLDOVER.
3:0	N/A		Reserved

8.6.2.9.8 SPI_LOCK

Prevents SPI registers from being written to, except for 0x555.

This register cannot be read back.

表 86. Register 0x555

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:0	SPI_LOCK	0	0: Registers unlocked. 1 to 255: Registers locked.		

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To assist customers in frequency planning and design of loop filters, Texas Instruments provides Clock Architect and PLLatinum Sim and on ti.com.

9.1.1 Digital Lock Detect Frequency Accuracy

The digital lock detect circuit is used to determine PLL1 locked, PLL2 locked, and holdover exit events. A window size and lock count register are programmed to set a ppm frequency accuracy of reference to feedback signals of the PLL for each event to occur. When a PLL digital lock event occurs, the digital lock detect of thePLL is asserted true. When the holdover exit event occurs, the device will exit holdover mode when HOLDOVER_EXIT_MODE = 1 (Exit based on DLD).

EVENT	PLL	WINDOW SIZE	LOCK COUNT		
PLL1 Locked	PLL1	PLL1_WND_SIZE	PLL1_DLD_CNT		
PLL2 Locked	PLL2	PLL2_WND_SIZE	PLL2_DLD_CNT		
Holdover exit	PLL1	PLL1_WND_SIZE	HOLDOVER_DLD_CNT		

表 87. Digital Lock Detect Related Fields

For a digital lock detect event to occur, there must be a *lock count* number of phase detector cycles of PLLX during which the time and phase error of the PLLX_R reference and PLLX_N feedback signal edges are within the user programmable *window size*. Because there must be at least one *lock count* phase detector event before a lock event occurs, a minimum digital lock event time can be calculated as *lock count* / f_{PDX} where X = 1 for PLL1 or 2 for PLL2.

By using ± 4 , values for a *lock count* and *window size* can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs:

 $ppm = \frac{1e6 \times PLLX_WND_SIZE \times f_{PDX}}{PLLX_DLD_CNT}$

(4)

The effect of the *lock count* value is that it shortens the effective lock window size by dividing the *window size* by *lock count*.

If at any time the PLLX_R reference and PLLX_N feedback signals are outside the time window set by *window size*, then the *lock count* value is reset to 0.

9.1.1.1 Minimum Lock Time Calculation Example

To calculate the minimum PLL2 *digital* lock time given a PLL2 phase detector frequency of 40 MHz and PLL2_DLD_CNT = 10,000. Then, the minimum lock time of PLL2 will be 10,000 / 40 MHz = 250μ s.



9.1.2 Driving CLKin AND OSCin Inputs

9.1.2.1 Driving CLKin and OSCin PINS With a Differential Source

CLKin and OSCin pins can be driven by differential signals. TI recommends setting the input mode to bipolar (CLKinX_BUF_TYPE = 0) when using differential reference clocks. The LMK04832 internally biases the input pins so the differential interface should be AC-coupled. The recommended circuits for driving the CLKin pins with either LVDS or LVPECL are shown in $\boxed{2}$ 21 and $\boxed{2}$ 22.



Copyright © 2017, Texas Instruments Incorporated

図 21. CLKinX/X* or OSCin Termination for an LVDS Reference Clock Source



☑ 22. CLKinX/X* or OSCin Termination for an LVPECL Reference Clock Source

Finally, a reference clock source that produces a differential sine wave output can drive the CLKin pins using the following circuit. Note: the signal level must conform to the requirements for the CLKin pins listed in the *Electrical Characteristics*.



Copyright © 2017, Texas Instruments Incorporated

図 23. CLKinX/X* or OSCin Termination for a Differential Sinewave Reference Clock Source

9.1.2.2 Driving CLKin Pins With a Single-Ended Source

The CLKin and OSCin pins of the LMK04832 can be driven using a single-ended reference clock source, for example, either a sine wave source or an LVCMOS/LVTTL source. CLKin supports both AC coupling or DC coupling. OSCin must use AC coupling. In the case of the sine wave source that is expecting a 50- Ω load, TI recommends using AC coupling as shown in \mathbb{Z} 24 with a 50- Ω termination.

注

The signal level must conform to the requirements for the CLKin or OSCin pins listed in the *Electrical Characteristics*.

To support LOS functionality, CLKinX_BUF_TYPE must be set to MOS mode (CLKinX_BUF_TYPE = 1) when AC-coupled. When AC coupling, if the 100- Ω termination is placed on the IC side of the blocking capacitors, then the LOS functionality will not be valid.



Copyright © 2017, Texas Instruments Incorporated

図 24. CLKinX/X* Single-Ended Termination

If the CLKin pins are being driven with a single-ended LVCMOS/LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, the CLKinX_BUF_TYPE should be set to MOS buffer mode (CLKinX_BUF_TYPE = 1) and the voltage swing of the source must meet the specifications for DC -oupled, MOS-mode clock inputs given in the *Electrical Characteristics*. If AC coupling is used, the CLKinX_BUF_TYPE should be set to the bipolar buffer mode (CLKinX_BUF_TYPE = 0). The voltage swing at the input pins must meet the specifications for AC-coupled, bipolar mode clock inputs given in the *Electrical Characteristics*. In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC-coupling capacitor is sufficient.



Copyright © 2017, Texas Instruments Incorporated

図 25. DC-Coupled LVCMOS/LVTTL Reference Clock

9.1.3 OSCin Doubler for Best Phase Noise Performance

PLL2 OSCin input path includes an on-chip Frequency Doubler. To have the best phase noise performance, it is recommended to maximize the PLL2 phase detector frequency. For example, using 122.88MHz VCXO, PLL2 phase detector frequency can be increased to 245.76MHz by setting PLL2_REF_2X_EN. Doubler path is a high performance path for OSCin clock. For configuration where doubler cannot be used, it is recommended to use Doubler and PLL2_RDIV=2. To have deterministic phase relationship between input clock and output clocks, 0-delay modes should be used (nested 0-delay mode for dual loop configuration instead of cascaded 0-delay mode).



9.2 Typical Application

This design example highlights using the available tools to design loop filters and create programming map for LMK04832.



図 26. Typical Application

9.2.1 Design Requirements

Clocks outputs:

- 1x 245.76-MHz clock for JESD204B ADC, LVPECL.
 - This clock requires the best performance in this example.
- 2x 2949.12-MHz clock for JESD204B DAC, CML.
- 1x 122.88-MHz clock for JESD204B FPGA block, LVDS
- 3x 10.24-MHz SYSREF for ADC (LVPECL), DAC (LVPECL), FPGA (LVDS).
- 2x 122.88-MHz clock for FPGA, LVDS

For best performance, the highest possible phase detector frequency is used at PLL2. As such, a 122.88-MHz VCXO is used.

9.2.2 Detailed Design Procedure

注 This information is current as of the date of the release of this datasheet. Design tools receive continuous improvements to add features and improve model accuracy. Refer to the software instructions or training for latest features.

9.2.2.1 Device Selection

Enter the required frequencies into the tools. In this design, the LMK04832 VCO0 and LMK04832 VCO1 both meet the design requirements. VCO0 offers a relatively improved VCO performance over VCO1. In this case, choose LMK04832_VCO0 for improved RMS jitter in the 12-kHz to 20-MHz integration range.

9.2.2.1.1 Clock Architect

Under the advanced tab of Clock Architect, filtering of specific parts can be done using regular expressions in the Part Filter box. [LMK04832.*] will filter for only the LMK04832 device (without brackets). More detailed filters can be given such as the entire part name LMK04832_VCO0 to force an LMK04832 using VCO0 solution if one is available.



Typical Application (continued)

9.2.2.2 Device Configuration and Simulation

The tools automatically configure the simulation to meet the input and output frequency requirements given, and make assumptions about other parameters to give some default simulations. However, the user may chose to make adjustments for more accurate simulations to their application. For example:

- Entering the VCO Gain of the external VCXO or possible external VCO used device.
- Adjust the charge pump current to help with loop filter component selection. Lower charge pump currents result in smaller components but may increase impacts of leakage and at the lowest values reduce PLL phase nosie performance.
- Clock Architect allows loading a custom phase noise plot for reference or VCXO block. Typically, a custom
 phase noise plot is entered for CLKin to match the reference phase noise to device; a phase noise plot for the
 VCXO can additionally be provided to match the performance of VCXO used. For improved accuracy in
 simulation and optimum loop filter design, be sure to load these custom noise profiles for use in application.
- PLLatinum Sim can also be used to design and simulate a loop filter.

9.2.2.3 Device Programming

Using the clock design tools configuration the TICS Pro software is manually updated with this information to meet the required application.

Frequency planning for assignment of outputs:

- To minimize crosstalk perform frequency planning / CLKout assignments to keep common frequencies on outputs close together.
- It is best to place common device clock output frequencies on outputs sharing the same V_{CC} group. For example, these outputs share Vcc4_CG2. Refer to *Pin Configuration and Functions* to see the V_{CC} groupings the clock outputs.

In this example, the 245.76-MHz ADC output needs the best performance. CLKout2 on the LMK04832 provides the best noise floor / performance. The 245.76 MHz is placed on CLKout2 with 10.24-MHz SYSREF on CLKout3.

- For best performance the input and output drive level bits may be set. Best noise floor performance is achieved with CLKout2_3_IDL = 1 and CLKout2_3_ODL = 1.
- The CLKoutX_Y_ODL bit has no impact on even clock outputs in high performance bypass mode.

In this example, the 983.04-MHz DAC output is placed on CLKout4 and CLKout6 with 10.24-MHz SYSREF on paired CLKout5 and CLKout7 outputs.

• These outputs share Vcc4_CG2.

In this example, the 122.88-MHz FPGA JESD204B output is placed on CLKout10 with 10.24-MHz SYSREF on paired CLKout11 output.

Additionally, the 122.88-MHz FPGA non-JESD204B outputs are placed on CLKout8 and CLKout9.

• When frequency planning, consider PLL2 as a clock output at the phase detector frequency. As such, these 122.88-MHz outputs have been placed on the outputs close to the PLL2 and Charge Pump power supplies.

Once the device programming is completed as desired in the TICS Pro software, it is possible to export the register settings from the Register tab for use in application.



Typical Application (continued)

9.2.3 Application Curves

The phase noise plots collected with loop filter values of C1 = open, C2 = 150 nF, R2 = 470 Ω .



LMK04832

JAJSFI6C - FEBRURAY 2017 - REVISED MAY 2018



www.tij.co.jp

Typical Application (continued)





Typical Application (continued)



9.3 Do's and Don'ts

9.3.1 Pin Connection Recommendations

- V_{cc} Pins and Decoupling: all V_{cc} pins must always be connected.
- Unused Clock Outputs: leave unused clock outputs floating and powered down.
- Unused Clock Inputs: unused clock inputs can be left floating.

10 Power Supply Recommendations

10.1 Current Consumption

TI recommends using the TICS Pro software to calculate the current consumption estimate based on programmed configuration.

LMK04832 JAJSFI6C – FEBRURAY 2017 – REVISED MAY 2018 Texas Instruments

www.tij.co.jp

11 Layout

11.1 Layout Guidelines

11.1.1 Thermal Management

Power consumption of the LMK04832 can be high enough to require attention from thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

11.2 Layout Example

	For any pins not connected, ensure that the exposed copper is of the same area as other pins to contribute to healthy solderdown joint	CLKouts/OSCouts – Differential signals should be routed tightly coupled to minimize PCB crosstalk. For LVPECL/LCPECL/CML place components			
П	For CLKout Vccs in JESD204B application, place ferrite beads then 1 μF capacitor. The 1 μF capacitor supports low frequency SYSREF switching/turning on.	resistors close to IC. OSCout shares pins with CLKin2 and is programmable for input or output			
	For CLKout Vccs in traditional applications, place ferrite bead on top layer close to pins to choke high frequency noise from via.	CLKin and OSCin – If differential input (preferred) route traces tightly coupled. If single ended, have at least 3 trace width (of CLKin/OSCin trace) separation from other RF traces.			
W	better. Place all resistors and caps close to IC.	Place terminations close to IC.			
		CLKin2 and OSCout share pins and is programmable for input or output.			

図 37. LMK04832 Layout Example, Top Layer



Layout Example (continued)





Expose copper under the PCB to provide direct copper to air interface to dissipate heat

Provide areas of connect copper to allow heat to escape from directly below PCB. Do not let components block all thermal escape from ground pad. A flexible termination / PCB layout for either CML requiring a pull-up to Vcc or LVPECL/LCPECL requiring a pull-down to ground, or for any other format is the H configuration as illustrated in layout above and schematic below. R1/R2 allow connection to Vcc or ground. When using CML with inductors (in position R3 and R4), R1 allows the use of an additional series resistor.



図 38. LMK04832 Layout Example, Bottom Layer



12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 Clock Architect

部品の選択、ループ・フィルタ設計、シミュレーション。

オンラインClock Architectツールを使用するには、www.ti.com/clockarchitectを参照してください。

12.1.1.2 PLLatinum Sim

ループ・フィルタ設計およびシミュレーションをサポートします。シミュレーションはいずれもシングル・ループ用であり、デュ アル・ループのシミュレーションを行うには、最初のPLLシミュレーションの結果を次のPLLシミュレーションのリファレンスとし てロードする必要があります。

PLLatinum Simツールをダウンロードするには、www.ti.com/tool/PLLATINUMSIM-SWを参照してください。

12.1.1.3 TICS Pro

EVMプログラミング・ソフトウェア。プログラミング用レジスタ・マップの作成や消費電流の推計にも使用できます。

TICS Proについては、www.ti.com/tool/TICSPRO-SWを参照してください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ TIのE2E (Engineer-to-Engineer)コミュニティ。エンジニア間の共同作 業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有 し、アイディアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることが できます。技術サポート用の連絡先情報も参照できます。

12.3 商標

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防 ▲ 止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。このデータは予告なく変更さ れることがあり、ドキュメントが改訂される場合もあります。



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LMK04832NKDR	Active	Production	WQFN (NKD) 64	2000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K04832NKD
LMK04832NKDR.A	Active	Production	WQFN (NKD) 64	2000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K04832NKD
LMK04832NKDT	Active	Production	WQFN (NKD) 64	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K04832NKD
LMK04832NKDT.A	Active	Production	WQFN (NKD) 64	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K04832NKD

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMK04832 :



www.ti.com

• Space : LMK04832-SP

NOTE: Qualified Version Definitions:

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NKD0064B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NKD0064B

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NKD0064B

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE



WQFN - 0.8 mm max height

WQFN



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NKD0064A

NKD0064A

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

WQFN



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



NKD0064A

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

WQFN



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みま す)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある 「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証 も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様 のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様の アプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任 を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツル メンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらの リソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権の ライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、 費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは 一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソ ースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありませ ん。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated