LMK00804B-Q1 1.5V～3.3V、1 入力 4 出力、高性能 LVCMOS ファンアウト・バッファ / レベル・シフタ

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1: -40°C～+125°C、T_A
- 1.5V～3.3V レベルをサポートする 4 つの LVCMOS/LVTTL 出力
  - 付加ジッタ:40MHz で RMS 0.1ps (標準値)
  - ノイズ・フロア:40MHz で -168dBc/Hz (標準値)
  - 出力周波数:350MHz (最大値)
  - 出力スキュー:35ps (最大値)
  - 部品間スキュー:550ps (最大値)
- 2 つの入力を選択可能
  - CLK_P、CLK_N ペアは LVPECL、LVDS、HCSL、SSTL、LVHSTL、LVCMOS/LVTTL に対応
  - LVCMOS_CLK は LVCMOS/LVTTL に対応
- 同期クロック・イネーブル
- コア / 出力電源
  - 3.3V/3.3V
  - 3.3V/2.5V
  - 3.3V/1.8V
  - 3.3V/1.5V
- パッケージ：16 ピン VQFN

2 アプリケーション

- 先進運転支援システム(ADAS)
  - 前方長距離レーダー
  - 中距離/短距離レーダー
  - 超短距離レーダー

3 概要

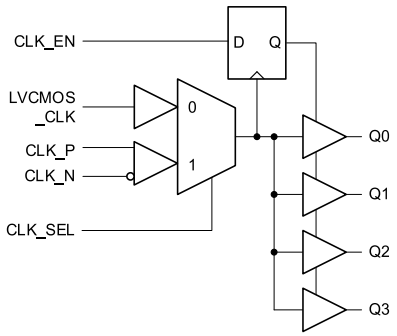
LMK00804B-Q1 は、差動またはシングルエンド入力に対応できる 2 つの選択可能な入力の 1 つから、最大 4 つの LVCMOS/LVTTL 出力 (3.3V、2.5V、1.8V、1.5V レベル) を分配できる高性能クロック・ファンアウト・バッファおよびレベル・シフタです。クロック・イネーブル入力は内部的に同期されており、クロック・イネーブル端子がアサートまたはアサート解除される際に、出力のラントやグリッチ・パルスが除去されます。クロックがディセーブルの場合、出力は論理 LOW 状態に保持されます。LMK00804B-Q1 はジッタの小さいクロックを 4 つのトランシーバ間に分配でき、カスケード接続されたミリ波レーダー・システムで、総合的なターゲット検出および分解能を向上できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMK00804B-Q1	VQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (June 2019) から Revision B に変更 **Page**

- 部品間スキューの最大値を 700ps から 550ps に変更 ... 1
- アプリケーションの「前面長距離レーダー」を「前方長距離レーダー」に変更 ... 1
- 「*概略回路図*」を変更 ... 1
- Changed pin 2 in the RGT package from: OE to: NC ... 3
- Changed the pin descriptions ... 3
- Changed Changed CDM ESD ratings from: +/-250 V to: +/-750 V ... 4
- Added the *Typical Characteristics* section back to the data sheet ... 8
- Changed *Differential Input Level* timing diagram ... 9
- Changed the *Overview* section ... 10
- Changed *Functional Block Diagram* ... 10
- Added the *Typical Connection Diagram* ... 12
- Changed the *Power Considerations* section to *Power Dissipation Calculations* ... 16
- Moved the *Thermal Management* section to *Do's and Don'ts* ... 16
- Changed the recommendations for unused output pins ... 17
- Changed the *Input Slew Rate Considerations* section ... 17
- Added content to the *Ground Planes* section ... 18
- Changed the *Layout Example* section ... 19

2019年3月発行のものから更新 **Page**

- データシートのステータスを「事前情報」から「量産データ」に変更 ... 1

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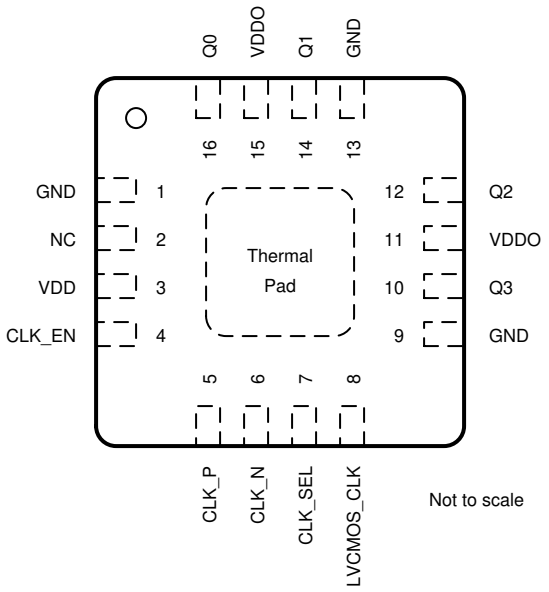
5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions(1)

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
CLK_EN	4	I, PU	Synchronous clock enable input. CLK_EN must be held low until a valid reference clock is provided. Typically connected to VDD with an external 1-kΩ pullup. When unused, leave floating. 0 = Outputs are forced to logic low state 1 = Outputs are enabled with LVCMOS/LVTTL levels
CLK_N	6	I, PD, PU	Inverting differential clock input with internal 51-kΩ (typ) pullup resistor to VDD and internal 51-kΩ (typ) pulldown resistor to GND. Typically connected to the inverting clock input. When unused, leave floating. Internally biased to $V_{DD}/2$ when left floating.
CLK_P	5	I, PD	Noninverting differential clock input with internal 51-kΩ (typ) pulldown resistor to GND. Typically connected to the noninverting clock input. A single-ended clock input can also be connected to CLK_P. When unused, leave floating.
CLK_SEL	7	I, PU	Clock select input. Typically connected to VDD with an external 1-kΩ pullup. When unused, leave floating. 0 = Select LVCMOS_CLK (pin 8) 1 = Select CLK_P, CLK_N (pins 5, 6)
GND	1, 9, 13	G	Power supply ground.
LVCMOS_CLK	8	I, PD	Single-ended clock input with internal 51-kΩ (typ) pulldown resistor to GND. Typically connected to a single-ended clock input. When unused, leave floating. Accepts LVCMOS/LVTTL levels.
NC	2	NC	No connect pin. Typically left floating. Do not connect to GND.
Q0	16	O	Single-ended clock outputs with LVCMOS/LVTTL levels at 7-Ω output impedance. Typically connected to a receiver with a 43-Ω series termination. When unused, leave floating.
Q1	14		
Q2	12		
Q3	10		

(1) See *Recommendations for Unused Input and Output Pins*, if applicable.
(2) G = Ground, I = Input, O = Output, P = Power, PU = 51-kΩ pullup, PD = 51-kΩ pulldown. NC = No connect

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Pin Functions[1] (continued)

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
VDD	3	P	Power supply terminal. Typically connected to a 3.3-V supply. The VDD pin is typically connected GND with an external 0.1-uF capacitor.
VDDO	11, 15	P	Output supply terminals. Typically connected to a 3.3-V, 2.5-V, 1.8-V, or 1.5-V supply. The VDDO pins are typically connected GND with external 0.1-uF capacitors.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{DD}	Supply input voltage		–0.3	3.6	V
V_{DDO}	Supply output voltage		–0.3	3.6	V
V_I	Input voltage	CLK_EN, CLK_SEL, CLK_P, CLK_N, LVCMOS_CLK	–0.3	V_{DD} + 0.3	V
	Input voltage	Q0, Q1, Q2, Q3	–0.3	V_{DDO} + 0.3	V
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply input voltage	3.135	3.3	3.465	V
V_{DDO}	Supply output voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
		1.71	1.8	1.89	
		1.425	1.5	1.575	
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		135	°C
f_{OUT}	Maximum output frequency[1]			350	MHz

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.

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6.4 Thermal Information

THERMAL METRIC(1)(2)		LMK00804B-Q1 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-K board).

6.5 Power Supply Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current through VDD			21	mA
I_{DDO}	Power supply current through VDDO			5	mA

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6.6 LVCMOS / LVTTL DC Electrical Characteristics

V_{DD} = 3.3 V ± 5%, V_{DDO} = 1.5 V ± 5%, 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	CLK_EN, CLK_SEL		2		V_{DD} + 0.3	V
		LVCMOS_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input low voltage	CLK_EN, CLK_SEL		–0.3		0.8	V
		LVCMOS_CLK		–0.3		1.3	
I_{IH}	Input high current	CLK_EN, CLK_SEL	V_{IH} = V_{DD}			15	µA
		LVCMOS_CLK	V_{DD} = 3.465 V, V_{IN} = 3.465 V			150	
I_{IL}	Input low current	CLK_EN, CLK_SEL	V_{IL} = GND	–150			µA
		LVCMOS_CLK	V_{DD} = 3.465 V, V_{IN} = 0 V	–150			
V_{OH}	Output high voltage(1)	V_{DDO} = 3.3 V ± 5%		2.64			V
		V_{DDO} = 2.5 V ± 5%		2			
		V_{DDO} = 1.8 V ± 5%		1.44			
		V_{DDO} = 1.5 V ± 5%		1.2			
V_{OL}	Output low voltage(1)	V_{DDO} = 3.3 V ± 5%				0.66	V
		V_{DDO} = 2.5 V ± 5%				0.5	
		V_{DDO} = 1.8 V ± 5%				0.36	
		V_{DDO} = 1.5 V ± 5%				0.3	
I_{OZL}	Output Hi-Z current low			–5			µA
I_{OZH}	Output Hi-Z current high					5	

(1) Outputs terminated with 50 Ω to V_{DDO}/2.

6.7 Differential Input DC Electrical Characteristics

V_{DD} = 3.3 V ± 5%, V_{DDO} = 1.5 V ± 5%, 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage swing, (V_{IH} – V_{IL})(1)			0.15		1.4	V
V_{IC}	Input common-mode voltage(1)(2)			0.5		V_{DD} – 0.85	V
I_{IH}	Input high current(3)	CLK_N, CLK_P	V_{DD} = 3.465 V, V_{IN} = 3.465 V			150	µA
I_{IL}	Input low current(3)	CLK_N, CLK_P	V_{DD} = 3.465 V , V_{IN} = 0 V	–150			µA

(1) V_{IL} should not be less than –0.3 V.
(2) Input common-mode voltage is defined as V_{IH}.
(3) For I_{IH} and I_{IL} measurements on CLK_Por CLK_N, one must comply with V_{ID} and V_{IC} specifications by using the appropriate bias on CLK_N or CLK.

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6.8 Switching Characteristics

V_{DD} = 3.3 V ± 5%, V_{DDO} = 1.5 V ± 5%, 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay, Low-to-high	LVCMOS_CLK(1), CLK_P/CLK_N(2)	–40°C to 125°C	1		2.5	ns
$t_{SK(O)}$	Output skew(3)(4)	Measured on rising edge				35	ps
$t_{SK(PP)}$	Part-to-part skew(4)(5)					550	ps
t_R/t_F	Output rise/fall time	20% to 80%, C_L= 5 pF		100	310	600	ps
t_{JIT}	Additive jitter(6)	f = 40 MHz, Input slew rate = 1.25 V/ns, 12-kHz to 20-MHz integration band			115	200	fs RMS
PN_{FLOOR}	Phase noise floor(7)	f = 40 MHz, Input slew rate = 1.25 V/ns	10-kHz offset		–151		dBc/Hz
			100-kHz offset		–160		
			1-MHz offset		–162		
			10-MHz offset		–162		
			20-MHz offset		–162		
D_O	Output duty cycle	REF = CLK_P/CLK_N, 50% input duty cycle, f < 166 MHz		45%		55%	
		REF = LVCMOS_CLK, 50% input duty cycle, f > 166 MHz		42%		58%	

(1) Measured from the V_{DD}/2 of the input to the V_{DDO}/2 of the output.
(2) Measured from the differential input crossing point to V_{DDO}/2 of the output.
(3) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at V_{DDO}/2 of the output.
(4) Parameter is defined in accordance with JEDEC Standard 65.
(5) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, various supply voltages, operating at the same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(6) Buffer additive jitter: $t_{JIT} = SQRT(t_{JIT\_SYS}^2 – t_{JIT\_SOURCE}^2)$, where t_{JIT_SYS} is the RMS jitter of the system output (source+buffer) and t_{JIT_SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.
(7) Buffer phase noise floor: PN_{FLOOR} (dBc/Hz) = 10 × log10[10^(PN_{SYSTEM}/10) – 10^(PN_{SOURCE}/10)], where PN_{SYSTEM} is the phase noise floor of the system output (source+buffer) and PN_{SOURCE} is the phase noise floor of the input source. Buffer Phase Noise Floor should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

6.9 Pin Characteristics

		MIN	TYP	MAX	UNIT
C_I	Input capacitance		1		pF
R_{PU}	Input pullup resistance		51		kΩ
R_{PD}	Input pulldown resistance		51		kΩ
C_{PD}	Power dissipation capacitance (per output)		2		pF
R_{OUT}	Output impedance		7		Ω

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6.10 Typical Characteristics

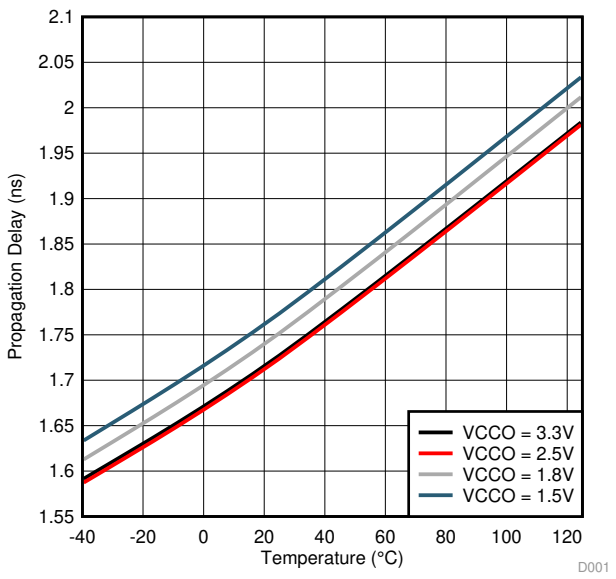

図 1. Propagation Delay vs. Temperature and Supply Voltage

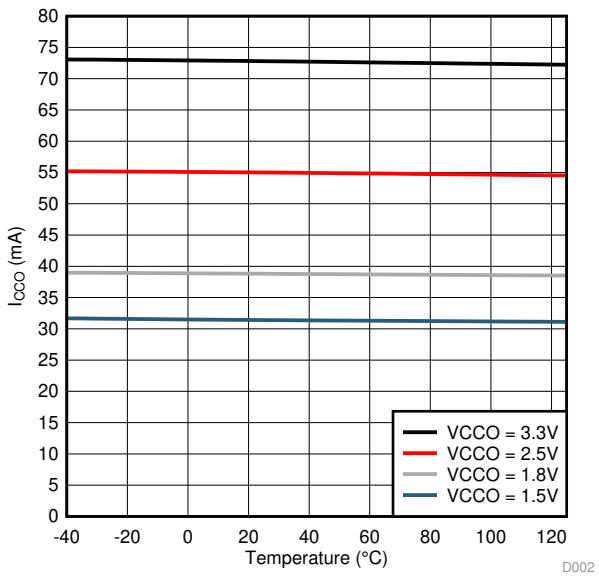

図 2. I_{CCO} vs. Temperature and Supply Voltage

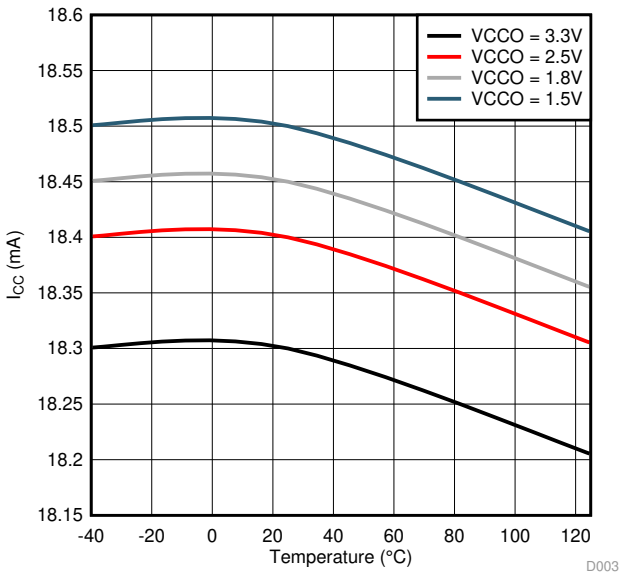

図 3. I_{CC} vs. Temperature and Supply Voltage

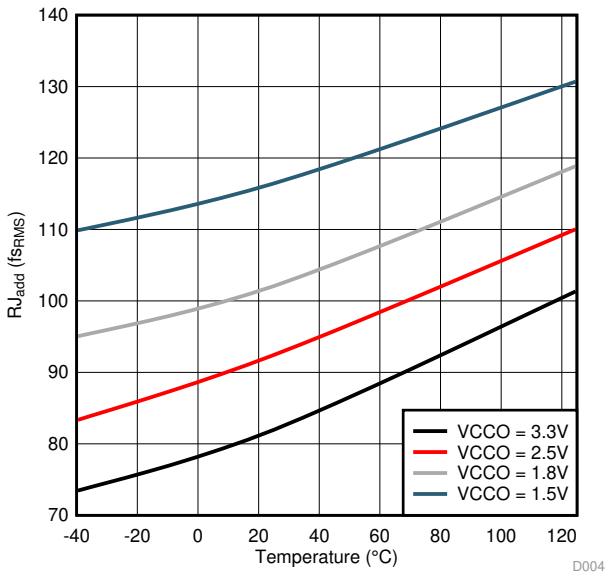

図 4. Additive Jitter vs. Temperature and Supply Voltage

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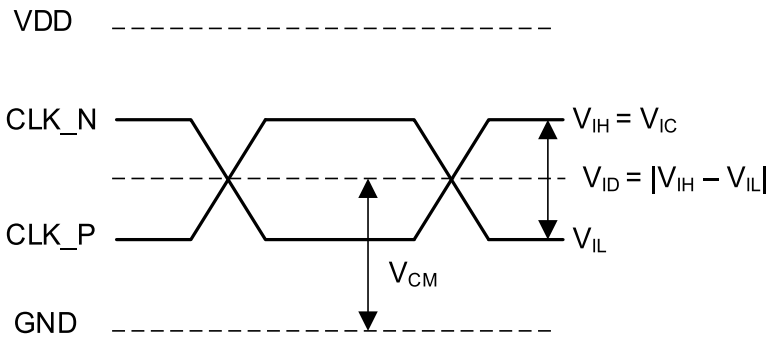
7 Parameter Measurement Information



NOTE: $V_{CM} = V_{IC} – V_{ID}/2 = (V_{IH} + V_{IL})/2$

図 5. Differential Input Level

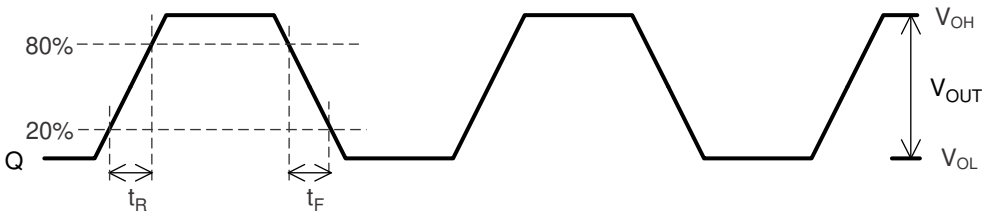


図 6. Output Voltage, and Rise and Fall Times

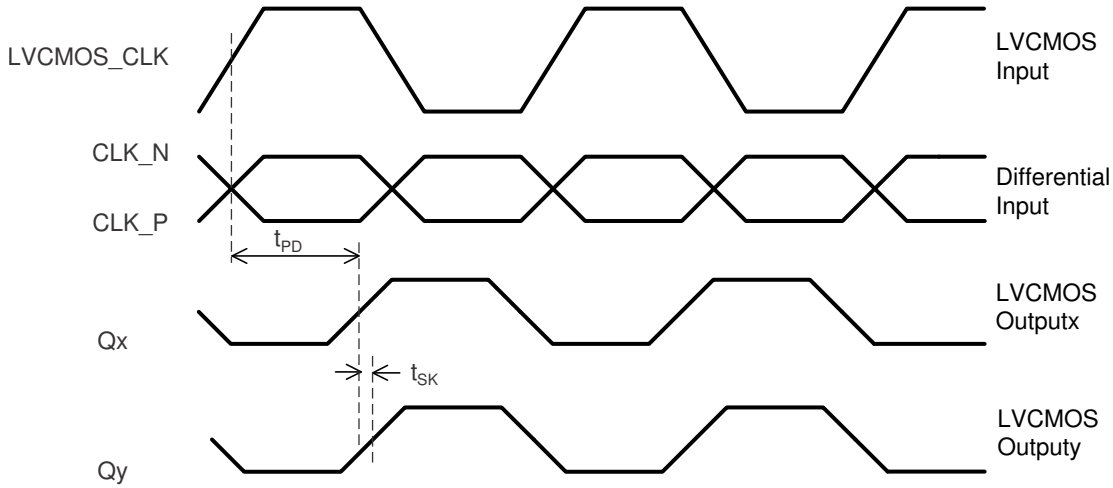


図 7. Output Skew and Propagation Delay

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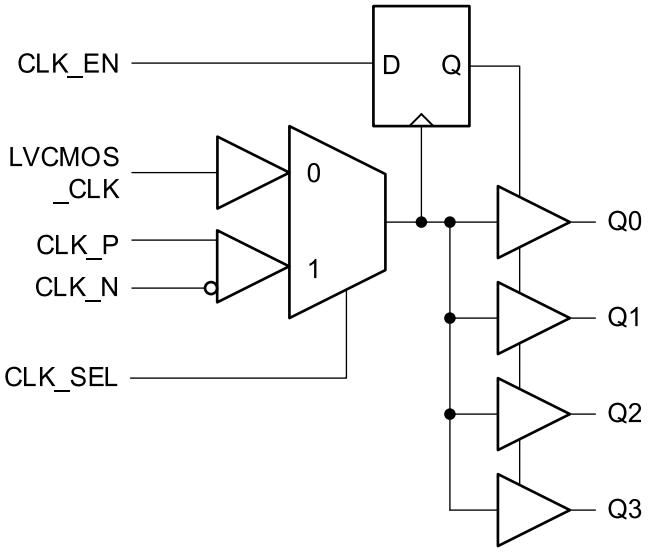
8 Detailed Description

8.1 Overview

The LMK00804B-Q1 is a clock fan-out buffer with two selectable clock inputs and four LVCMOS outputs. The LVCMOS_CLK input accepts a single-ended clock input, and the CLK_P/CLK_N input accepts a differential or single-ended clock input. The LMK00804B-Q1 has a synchronous clock enable feature that allows the device to synchronously enable or disable the outputs using the CLK_EN pin.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Clock Enable Timing

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in 図 8.

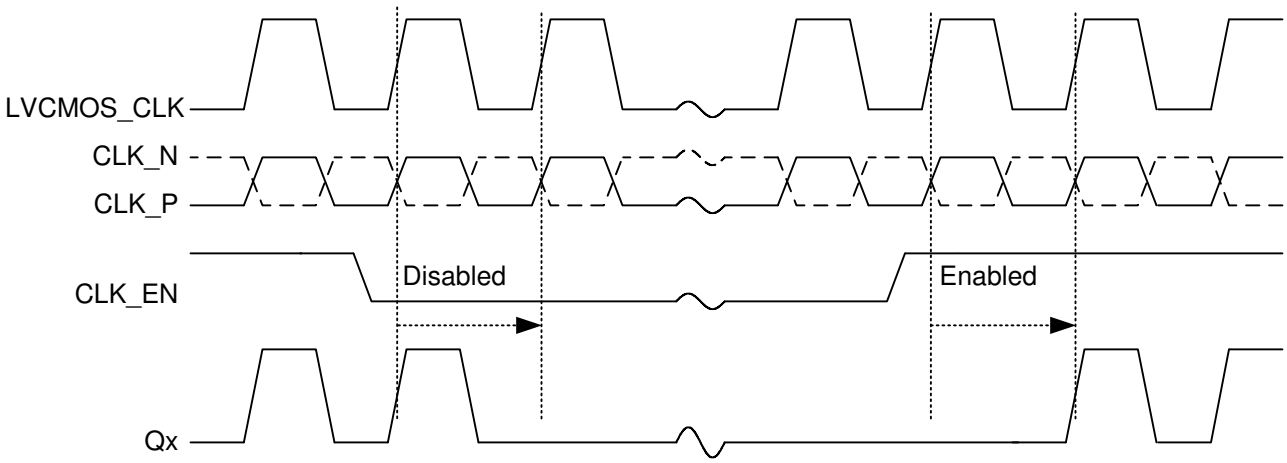

図 8. Clock Enable Timing Diagram

8.4 Device Functional Modes

The device can provide fan-out and level translation from a differential or single-ended input to a LVCMOS/LVTTL output where the output V_{OH} and V_{OL} levels are applied to the V_{DDO} pin and output load condition.

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9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMK00804B-Q1 enables the distribution of up to four LVCMOS copies of a low-noise source designed for general-purpose and high-performance applications. For best jitter performance, TI recommends to use the appropriate matching networks for the clock driver and receiver format, as detailed in the *Typical Applications* section. Practice good high-speed layout design outlined in the *High-speed Layout Guidelines* application report (SCAA082).

The LMK00804B-Q1 is designed to drive 50-Ω controlled-impedance traces. TI recommends to design these clock traces as 50-Ω, single-ended controlled impedance traces. Use a series 43-Ω resistor at the clock outputs Q[3:0] to match the driver impedance and series resistance to the trace impedance.

9.2 Typical Applications

Refer to the following sections for output clock and input clock interface circuits.

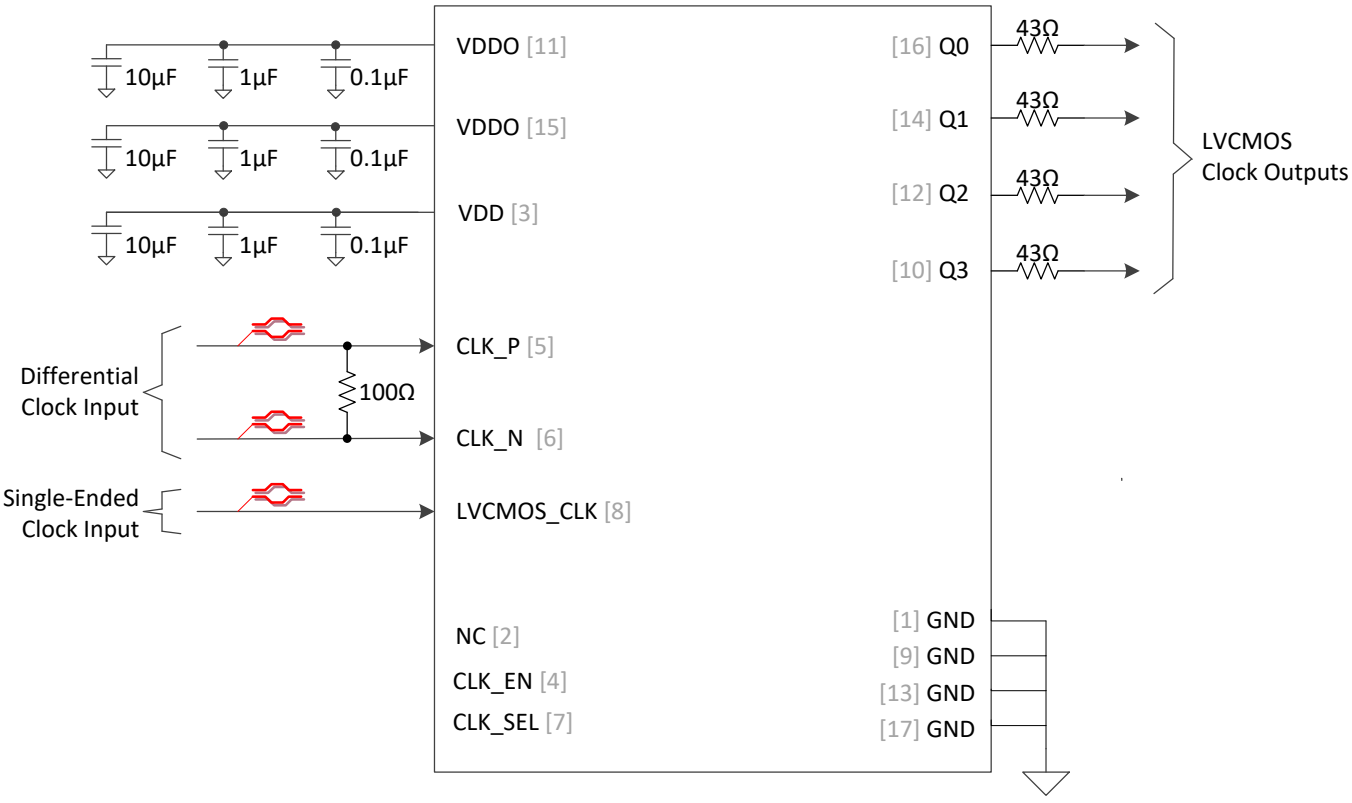

図 9. Typical Connection Diagram

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Typical Applications (continued)

9.2.1 Output Clock Interface Circuit

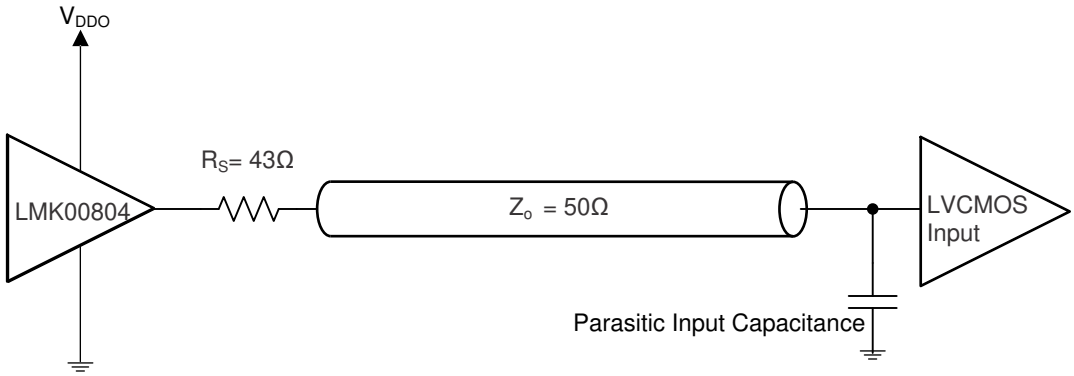

図 10. LVCMOS Output Configuration

9.2.1.1 Design Requirements

For high-performance devices, limitations of the equipment can affect phase-noise measurements. The noise floor of the equipment is often higher than the noise floor of the device. The real noise floor of the device is probably lower. It is important to understand that system-level phase noise measured at the DUT output is influenced by the input source and the measurement equipment.

For 図 11 and system-level phase noise plots, a Rohde & Schwarz SMA100A low-noise signal generator was cascaded with an Agilent 70429A K95 single-ended-to-differential converter block with ultra-low phase noise and fast-edge slew rate (>3 V/ns) to provide a low-noise clock input source to the LMK00804B-Q1. An Agilent E5052 source signal analyzer with an ultra-low measurement noise floor was used to measure the phase noise of the input source (SMA100A + 70429A K95) and system output (input source + LMK00804B-Q1). The light blue trace shows the input source phase noise, and the dark blue trace in 図 11 shows the system output phase noise.

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Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Use 式 1 to calculate the additive phase noise or noise floor of the buffer (PN_{FLOOR}):

$$PN_{FLOOR}\ (dBc/Hz) = 10 \times \log_{10}[10\text{^}(PN_{SYSTEM}/10) - 10\text{^}(PN_{SOURCE}/10)]$$

where

- PN_{SYSTEM} is the phase noise of the system output (source+buffer)
- PN_{SOURCE} is the phase noise of the input source

(1)

Use 式 2 to calculate the additive jitter of the buffer (t_{JIT}):

$$t_{JIT} = SQRT(t_{JIT\_SYS}^2 - t_{JIT\_SOURCE}^2)$$

where:

- t_{JIT_SYS} is the RMS jitter of the system output (source+buffer), integrated from 10 kHz to 20 MHz
- t_{JIT_SOURCE} is the RMS jitter of the input source, integrated from 10 kHz to 20 MHz

(2)

9.2.1.3 Application Curve

9.2.1.3.1 System-Level Phase Noise and Additive Jitter Measurement

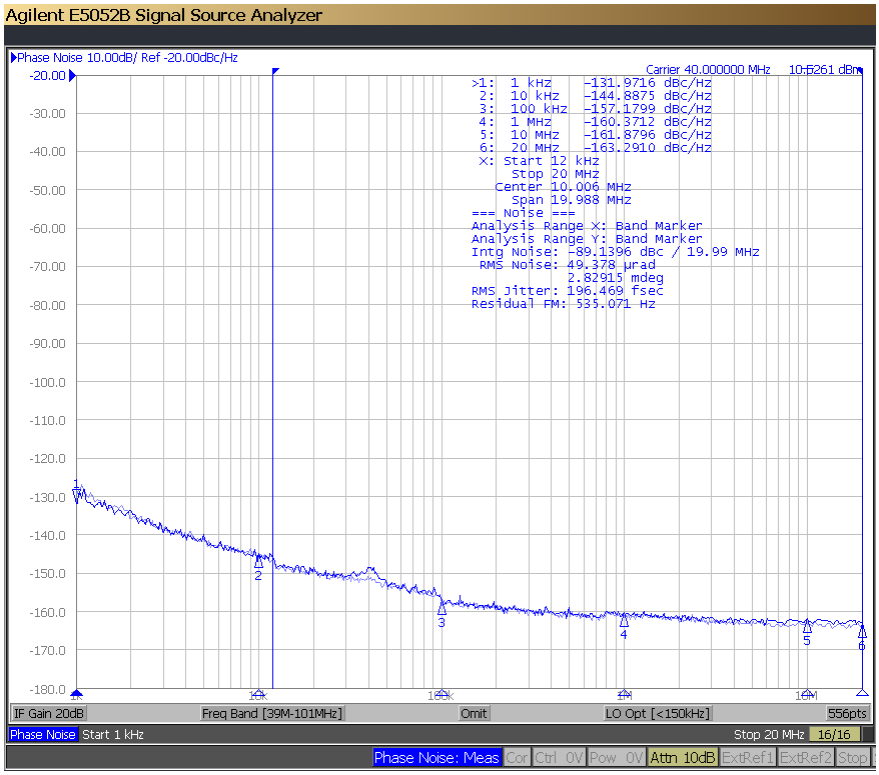

図 11. 40-MHz Input Phase Noise (181 fs rms, Light Blue), and Output Phase Noise (196 fs rms, Dark Blue), Additive Jitter = 77 fs rms

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Typical Applications (continued)

9.2.2 Input Detail

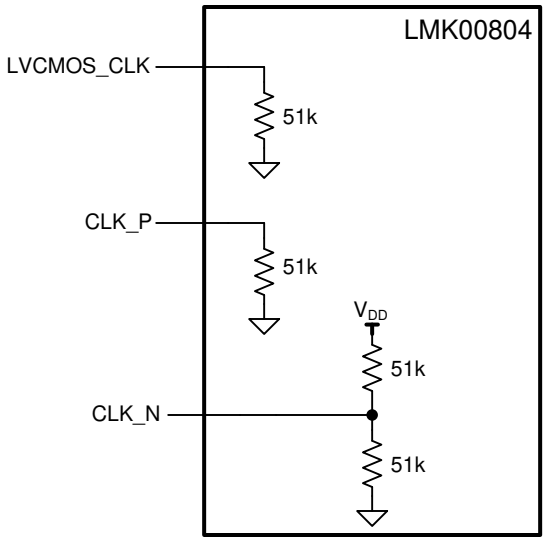


図 12. Clock Input Components

9.2.3 Input Clock Interface Circuits

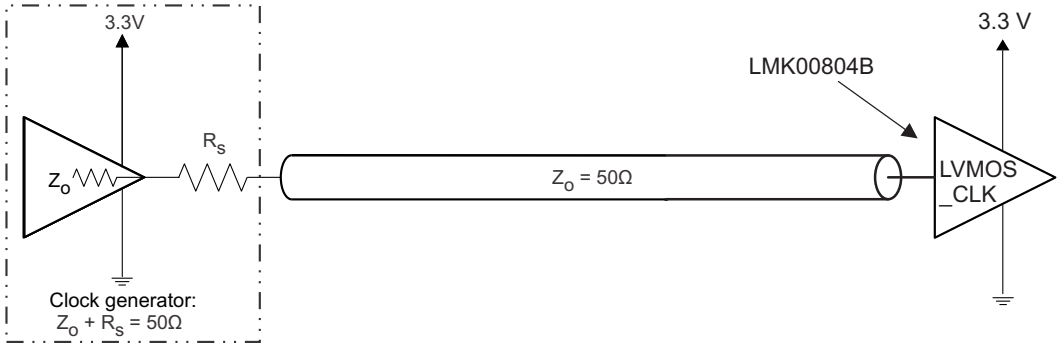
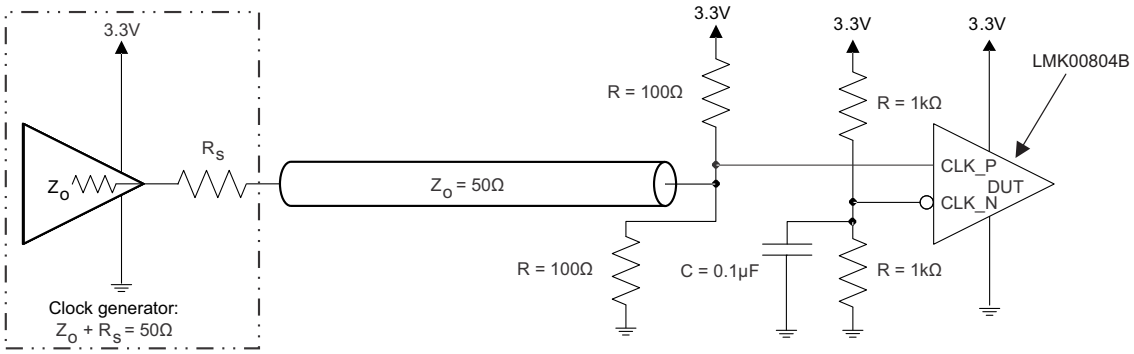


図 13. LVCMOS_CLK Input Configuration



(1) The Thevenin/split termination values (R = 100 Ω) at the CLK_P input may be adjusted to provide a small differential offset voltage (50 mV, for example) between the CLK_P and CLK_N inputs to prevent input chatter if the LVCMOS driver in a tri-state condition. For example, the engineer can use 105 Ω 1% to the 3.3-V rail and 97.6 Ω 1% to GND to receive a –60-mV offset voltage ($V_{CLK\_N} – V_{CLK\_P}$) . Ensure a logic low state if the LVCMOS driver enters a tri-state condition.

図 14. Single-Ended/LVCMOS Input DC Configuration

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9.3 Do's and Don'ts

9.3.1 Power Dissipation Calculations

The following power considerations refer to the device-consumed power consumption only. The device power consumption is the sum of static and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. Use 式 3 through 式 5 to calculate the power consumption of the device:

$$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload} \quad (3)$$

$$P_{stat} = (I_{DD} \times V_{DD}) + (I_{DDO} \times V_{DDO}) \quad (4)$$

$$P_{dyn} + P_{Cload} = (I_{DDO,dyn} + I_{DDO,Cload}) \times V_{DDO}$$

where:

- $I_{DDO,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
- $I_{DDO,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA] (5)

Example for power consumption of the LMK00804B-Q1: 4 outputs are switching, f = 100 MHz,

$V_{DD} = V_{DDO} = 3.465$ V and assuming $C_{load} = 5$ pF per output:

$$P_{Dev} = 90 \text{ mW} + 34 \text{ mW} = 124 \text{ mW} \quad (6)$$

$$P_{stat} = (21 \text{ mA} \times 3.465 \text{ V}) + (5 \text{ mA} \times 3.465 \text{ V}) = 90 \text{ mW} \quad (7)$$

$$P_{dyn} + P_{Cload} = (2.8 \text{ mA} + 6.9 \text{ mA}) \times 3.465 \text{ V} = 34 \text{ mW} \quad (8)$$

$$I_{DD,dyn} = 2 \text{ pF} \times 3.465 \text{ V} \times 100 \text{ MHz} \times 4 = 2.8 \text{ mA} \quad (9)$$

$$I_{DD,Cload} = 5 \text{ pF} \times 3.465 \text{ V} \times 100 \text{ MHz} \times 4 = 6.9 \text{ mA} \quad (10)$$

注

For dimensioning the power supply, consider the total power consumption. The total power consumption is the sum of device power consumption and the power consumption of the load.

9.3.2 Thermal Management

For reliability and performance reasons, limit the die temperature to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

Assuming the conditions in the *Power Dissipation Calculations* section and operating at an ambient temperature of 70°C with all outputs loaded, 式 11 shows the estimate of the LMK00804B-Q1 junction temperature:

$$T_J = T_A + P_{Total} \times R_{\theta JA} = 70°C + (124 \text{ mW} \times 48°C/W) = 70°C + 6.0°C = 76.0°C \quad (11)$$

Here are some recommendations to improve heat flow away from the die:

- Use multi-layer boards
- Specify a higher copper thickness for the board
- Increase the number of vias from the top level ground plane under and around the device to internal layers and to the bottom layer with as much copper area flow on each level as possible
- Apply air flow
- Leave unused outputs floating

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Do's and Don'ts (continued)

9.3.3 Recommendations for Unused Input and Output Pins

- **CLK_SEL and CLK_EN:** CLK_EN must be held low until a valid reference clock is provided before the engineer can use the pin to enable the outputs. These inputs both have an internal pullup (PU) according to 表 1. 表 1 shows the default floating state of these inputs:

表 1. Input Floating Default States

INPUT	FLOATING STATE SELECTION
CLK_SEL	CLK_P/CLK_N selected
CLK_EN	Synchronous outputs enable

- **CLK_P/CLK_N Inputs:** See 図 12 for the internal connections. When using a single-ended input, take note of the internal pullup and pulldown to make sure the unused input is properly biased. To interface a single-ended input to the CLK_P/CLK_N input, the configuration shown in 図 14 is recommended.
- **LVCMOS_CLK Input:** See 図 12 for the internal connection. The internal pulldown (PD) resistor ensures a low state when this input is left floating.
- **Outputs:** Any unused output may be left floating.

9.3.4 Input Slew Rate Considerations

LMK00804B-Q1 employs high-speed and low-latency circuit topology to allow ultra-low additive jitter/phase noise and high-frequency operation. To take advantage of these benefits in the system application, it is optimal for the input signal to have a high slew rate of 3 V/ns or greater. Driving the input with a slower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential signal input is recommended over a single-ended signal, because a differential signal typically provides a higher slew rate and common-mode-rejection.

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10 Power Supply Recommendations

10.1 Power Supply Considerations

While there is no strict power supply sequencing requirement, it is generally best practice to sequence the supply input voltage (V_{DD}) before the supply output voltage (V_{DDO}).

10.1.1 Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

The use of bypass capacitors eliminates the low-frequency noise from power supply, because they can provide a very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them close to the power supply terminals and lay out traces with short loops to minimize inductance. TI recommends that the engineer add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply terminals in the package. TI recommends that the engineer insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver. This would prevent leakage into the board supply. It is important to choose an appropriate ferrite bead with low DC resistance, because the bead must provide adequate isolation between the board supply and the chip supply. It is also important to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

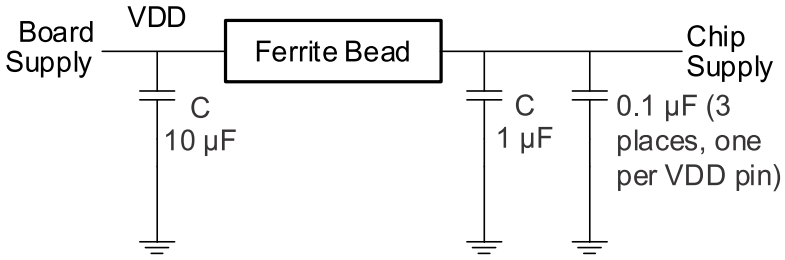

図 15. Power-Supply Decoupling

11 Layout

11.1 Layout Guidelines

11.1.1 Ground Planes

Solid ground planes are recommended because these planes provide a low-impedance return paths between the device and bypass capacitors, along with the clock source and destination devices.

LMK00804B-Q1 has a die attach pad (DAP) for enhanced thermal and electrical performance. Use five VIAs to connect the DAP to a solid GND plane. Full-through VIAs are preferred.

Avoid return paths of other system circuitry (for example, high-speed/digital logic, switching power supplies, and so forth) from passing through the local ground of the device to minimize noise coupling. Remember that noise coupling can lead to added jitter and spurious noise.

11.1.2 Power Supply Pins

Follow the power supply schematic and layout example described in *Power-Supply Filtering*.

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Layout Guidelines (continued)

11.1.3 Differential Input Termination

- Place input termination or biasing resistors as close to the CLK_P/CLK_N pins as possible.
- Avoid or minimize vias in the 50-Ω input traces to minimize impedance discontinuities. Intra-pair skew should also be minimized on the differential input traces.
- If not used, CLK_P/CLK_N inputs may be left as no connect.

11.1.4 LVCMOS Input Termination

- Input termination is not necessary when the LVCMOS_CLK input is driven from a LVCMOS driver that is series-terminated to match the characteristic impedance of the trace. Otherwise, place the input termination resistor as close to the LVCMOS_CLK input as possible.
- Avoid or minimize vias in the 50-Ω input trace to minimize impedance discontinuities.
- If not used, LVCMOS_CLK input may be left as no connect.

11.1.5 Output Termination

- Place 43-Ω series termination resistors close to the Qx outputs at the launch of the 50-Ω traces.
- Avoid or minimize vias in the 50-Ω input traces to minimize impedance discontinuities.
- If not used, any Qx output should be left as no connect.

11.2 Layout Example

図 16 shows the recommended PCB design for good electrical and thermal performance. To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Refer to the *Example Board Layout* in the *Package Option Addendum*.

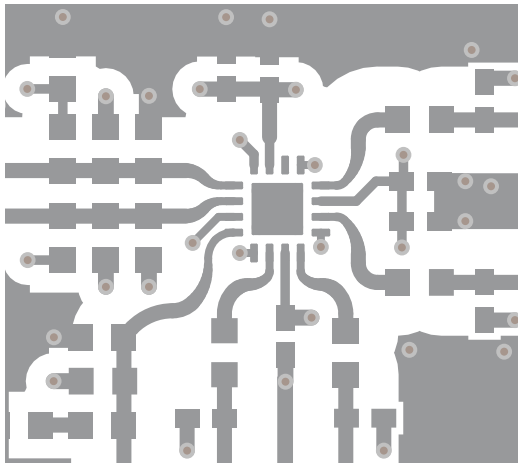

図 16. General PCB Ground Layout for Thermal Reliability

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『High-Speed Layout Guidelines』(SCAA082) (英語)

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK00804BQWRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	804BQ
LMK00804BQWRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	804BQ
LMK00804BQWRGTTQ1	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	804BQ
LMK00804BQWRGTTQ1.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	804BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LMK00804B-Q1 :

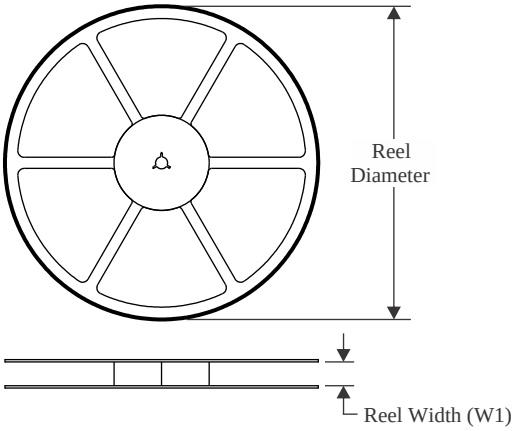
- Catalog : LMK00804B

NOTE: Qualified Version Definitions:

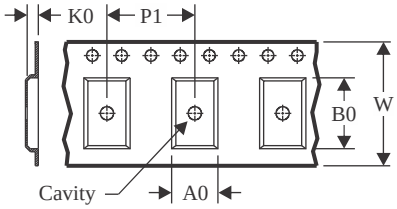
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

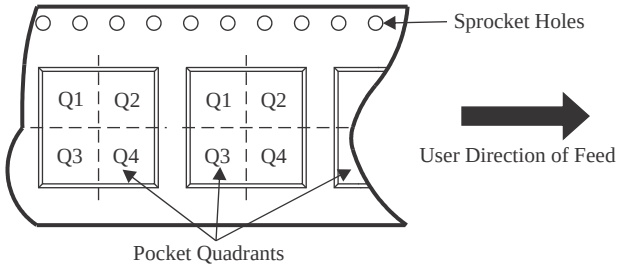


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

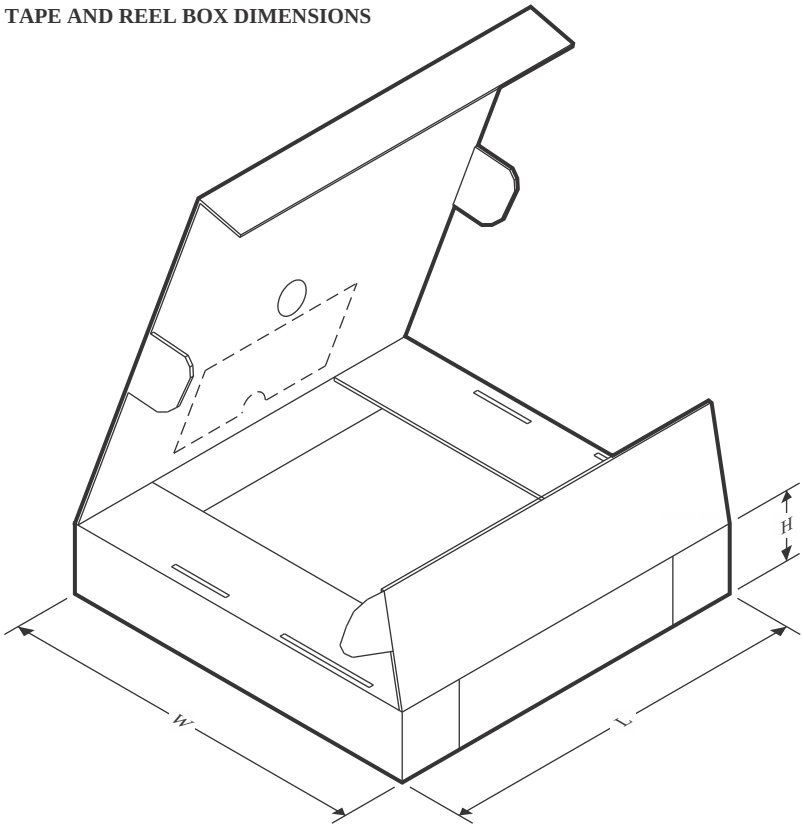
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00804BQWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK00804BQWRGTTQ1	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

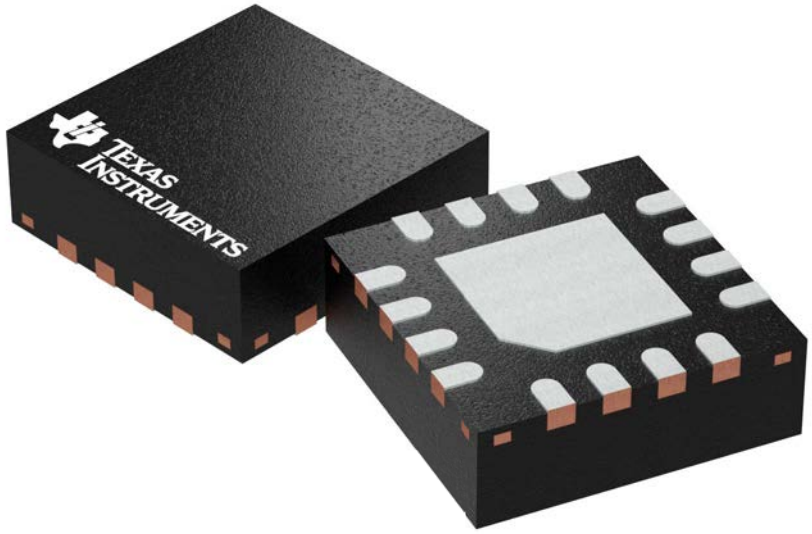


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00804BQWRGTRQ1	VQFN	RGT	16	3000	346.0	346.0	33.0
LMK00804BQWRGTTQ1	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



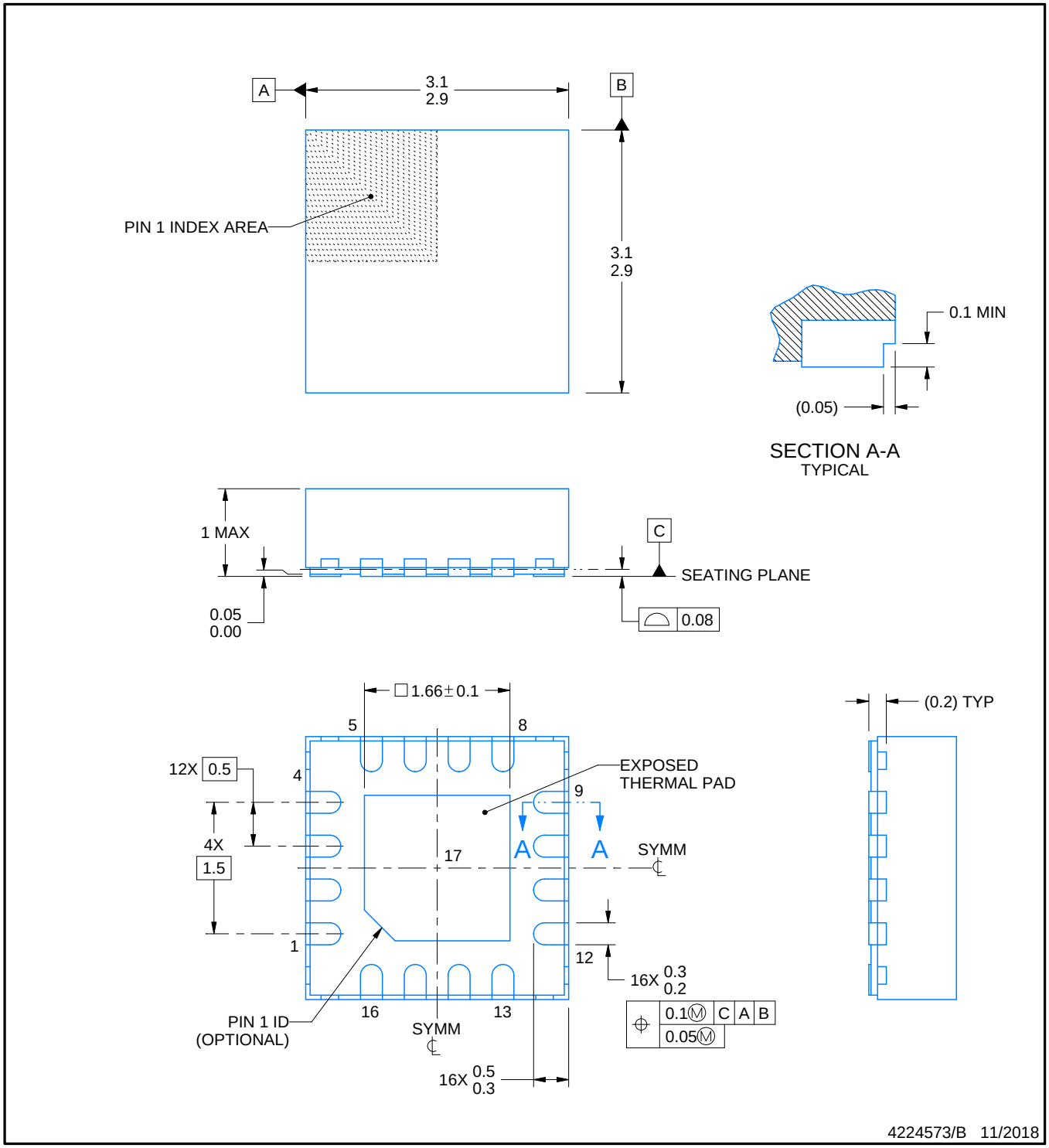
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016J

PACKAGE OUTLINE

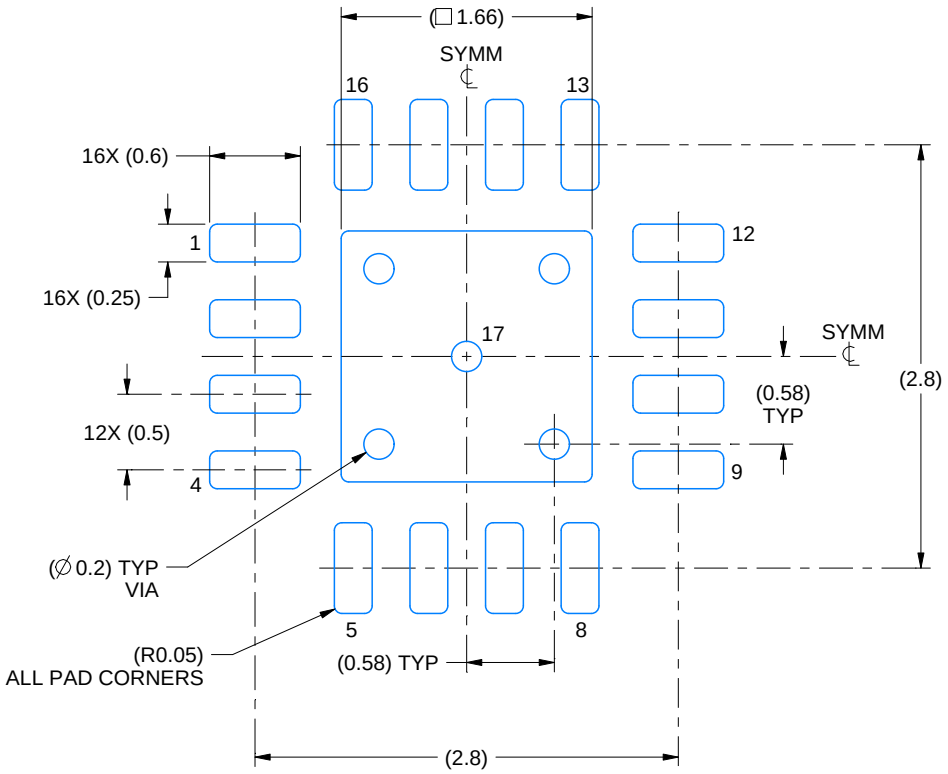
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

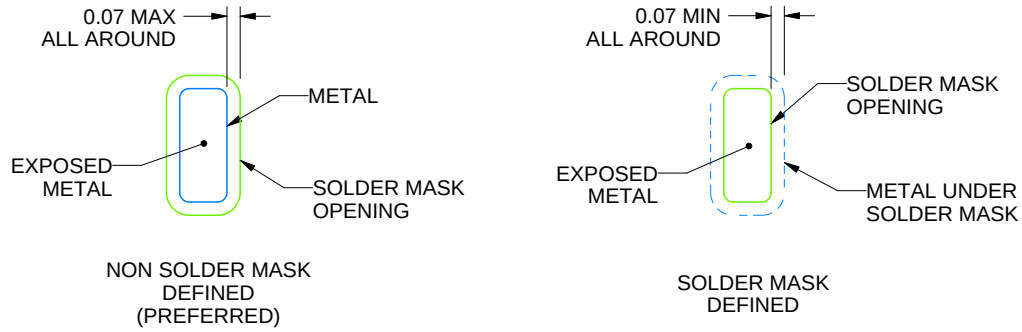


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

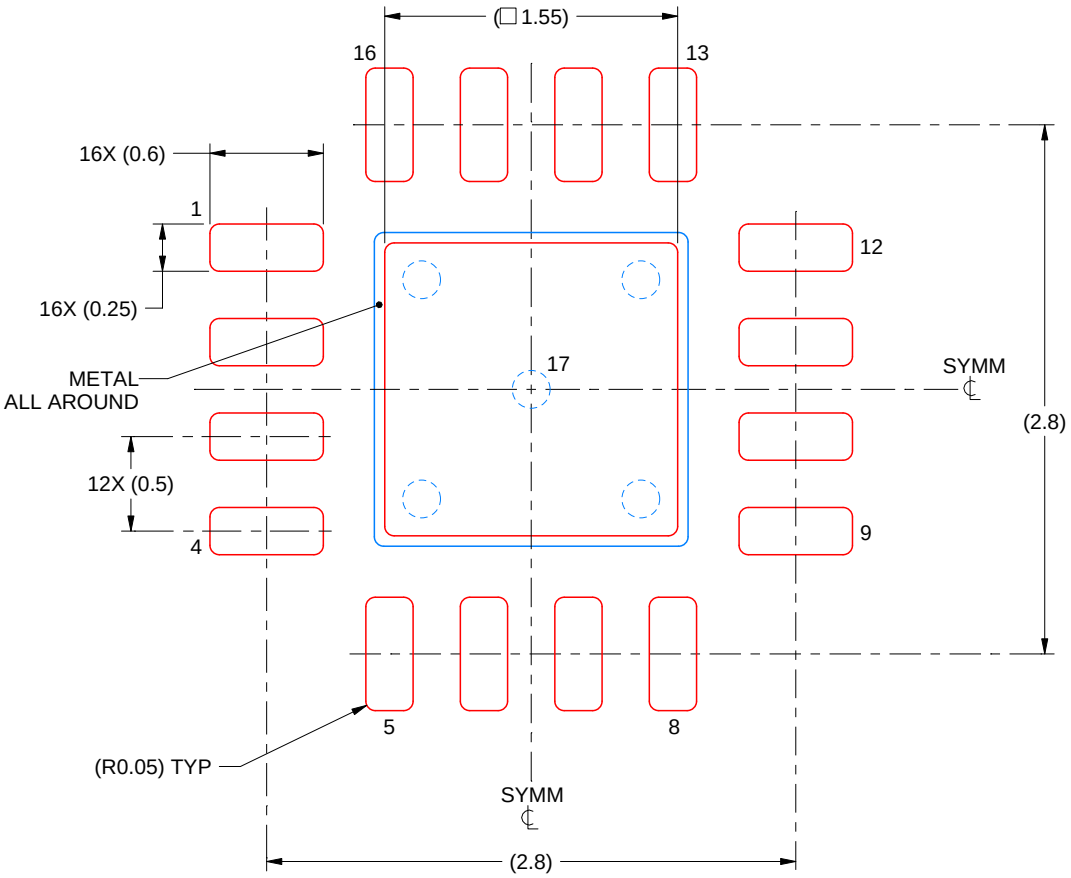


SOLDER MASK DETAILS

4224573/B 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 17:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224573/B 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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