

# LMK00334-Q1 PCIe Gen 1～Gen 5 向け 4 出力クロック・バッファおよびレベル変換器

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - デバイス温度グレード 2 :  $-40^{\circ}\text{C} \sim 105^{\circ}\text{C}$  の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
  - デバイス MM ESD 分類レベル M2
- 3 : 1 入力マルチプレクサ
  - 2 つの汎用入力は最高 400MHz で動作し、LVPECL、LVDS、CML、SSTL、HSTL、HCSL、シングルエンド・クロックに対応
  - 1 つの水晶振動子入力で、10 ~ 40MHz の水晶振動子またはシングルエンド・クロックに対応
- 2 バンクで、それぞれに 2 つの差動出力
  - HCSL または Hi-Z (選択可能)
  - 100MHz の PCIe Gen3/Gen4 用の付加 RMS 位相ジッタ
    - 30fs RMS (標準値)
- 高 PSRR :  $-72\text{dBc}$  (156.25MHz)
- 同期イネーブル入力付きの LVCMOS 出力
- 構成をピンで制御可能
- $V_{CC}$  コア電源 :  $3.3\text{V} \pm 5\%$
- 3 つの独立した  $V_{CCO}$  出力電源 :  $3.3\text{V}$ 、 $2.5\text{V} \pm 5\%$
- 産業用温度範囲 :  $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$
- 32 ピン WQFN (5mm × 5mm)

## 2 アプリケーション

- インフォテインメント : テレマティクス
- 制御ユニット・インフォテインメント : ヘッド・ユニット
- ADAS : 自律運転コントローラ

## 3 概要

LMK00334-Q1 デバイスは 4 出力の HCSL ファンアウト・バッファで、高周波数、低ジッタのクロック、データ分配、およびレベル変換を目的としています。本デバイスは、ADC、DAC、マルチ・ギガビット・イーサネット、XAUI、ファイバー・チャネル、SATA/SAS、SONET/SDH、CPRI、高周波バックプレーンのリファレンス・クロックを分配できます。

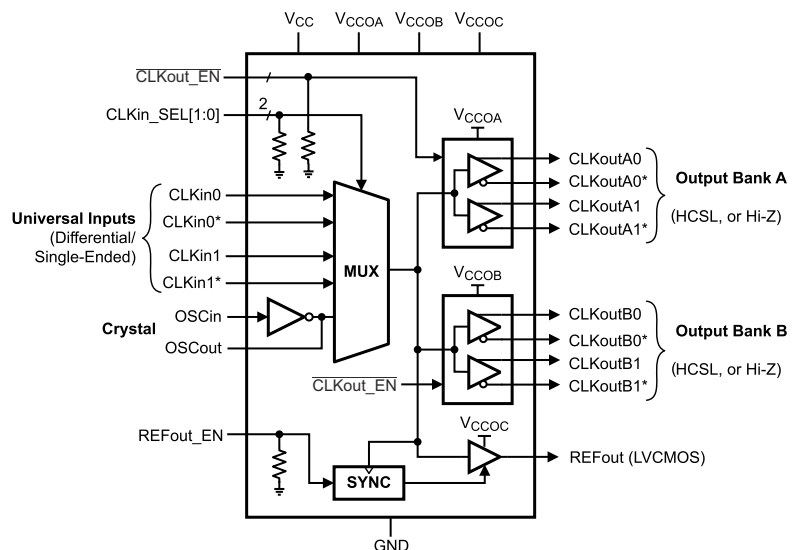
入力クロックは 2 つの汎用入力、または 1 つの水晶振動子入力から選択できます。選択された入力クロックは 2 つのバンクに分配され、それぞれのバンクには 2 つの HCSL 出力と 1 つの LVCMOS 出力があります。LVCMOS 出力には同期イネーブル入力があり、イネーブルまたはディスエーブル時にラント (微小) パルスなしの動作を実現できます。LMK00334-Q1 は 3.3V のコア電源、および 3 つの独立した 3.3V または 2.5V の出力電源で動作します。

LMK00334-Q1 は高性能、多用途、高い電力効率から、固定出力のバッファ・デバイスの代替品として理想的で、システムのタイミング・マージンを拡大できます。

### 製品情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
LMK00334-Q1	WQFN (32)	5.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



LMK00334-Q1 の機能ブロック図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2018) to Revision A (January 2022)	Page
• データシートのタイトルを変更.....	1
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• アプリケーション・セクションにリンクを追加.....	1
• 「概要」セクションに文章を追加.....	1
• Added example board layout to <i>Packaging Information</i> section.....	25

## 5 Pin Configuration and Functions

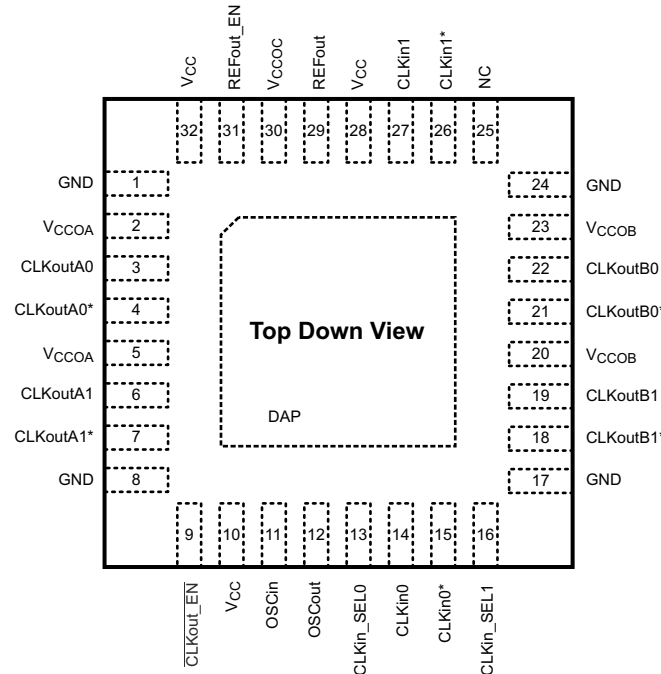


图 5-1. RTV Package 32-Pin WQFN Top View

表 5-1. Pin Functions<sup>(3)</sup>

PIN		I/O	DESCRIPTION
NAME	NO.		
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
CLKIn_SEL0	13	I	Clock input selection pins <sup>(2)</sup>
CLKIn_SEL1	16	I	Clock input selection pins <sup>(2)</sup>
CLKIn0	14	I	Universal clock input 0 (differential/single-ended)
CLKIn0*	15	I	Universal clock input 0 (differential/single-ended)
CLKIn1	27	I	Universal clock input 1 (differential/single-ended)
CLKIn1*	26	I	Universal clock input 1 (differential/single-ended)
CLKOut_EN	9	I	Bank A and Bank B low active output buffer enable. <sup>(2)</sup>
CLKOutA0	3	O	Differential clock output A0.
CLKOutA0*	4	O	Differential clock output A0.
CLKOutA1	6	O	Differential clock output A1.
CLKOutA1*	7	O	Differential clock output A1.
CLKOutB1	19	O	Differential clock output B1.
CLKOutB1*	18	O	Differential clock output B1.
CLKOutB0	22	O	Differential clock output B0.
CLKOutB0*	21	O	Differential clock output B0.
GND	1, 8 17, 24	GND	Ground
NC	25	—	Not connected internally. Pin may be floated, grounded, or otherwise tied to any potential within the Supply Voltage range stated in the <a href="#">Absolute Maximum Ratings</a> .
OSCin	11	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
OSCout	12	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
REFOut	29	O	LVCMOS reference output. Enable output by pulling REFOut_EN pin high.
REFOut_EN	31	I	REFOut enable input. Enable signal is internally synchronized to selected clock input. <sup>(2)</sup>

表 5-1. Pin Functions<sup>(3)</sup> (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V <sub>CC</sub>	10, 28, 32	PWR	Power supply for Core and Input Buffer blocks. The V <sub>CC</sub> supply operates from 3.3 V. Bypass with a 0.1-μF, low-ESR capacitor placed very close to each V <sub>CC</sub> pin.
V <sub>CCOA</sub>	2, 5	PWR	Power supply for Bank A Output buffers. V <sub>CCOA</sub> operates from 3.3 V or 2.5 V. The V <sub>CCOA</sub> pins are internally tied together. Bypass with a 0.1-μF, low-ESR capacitor placed very close to each V <sub>CCO</sub> pin. <sup>(1)</sup>
V <sub>CCOB</sub>	20, 23	PWR	Power supply for Bank B Output buffers. V <sub>CCOB</sub> operates from 3.3 V or 2.5 V. The V <sub>CCOB</sub> pins are internally tied together. Bypass with a 0.1-μF, low-ESR capacitor placed very close to each V <sub>CCO</sub> pin. <sup>(1)</sup>
V <sub>CCOC</sub>	30	PWR	Power supply for REFout buffer. V <sub>CCOC</sub> operates from 3.3 V or 2.5 V. Bypass with a 0.1-μF, low-ESR capacitor placed very close to each V <sub>CCO</sub> pin. <sup>(1)</sup>

- (1) The output supply voltages or pins (V<sub>CCOA</sub>, V<sub>CCOB</sub>, and V<sub>CCOC</sub>) will be called V<sub>CCO</sub> in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
- (2) CMOS control input with internal pulldown resistor.
- (3) Any unused output pins should be left floating with minimum copper length (see note in [Clock Outputs](#)), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See [Clock Outputs](#) for output configuration and [Termination and Use of Clock Drivers](#) for output interface and termination techniques.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub> , V <sub>CCO</sub>	Supply voltages	−0.3	3.6	V
V <sub>IN</sub>	Input voltage	−0.3	(V <sub>CC</sub> + 0.3)	V
T <sub>L</sub>	Lead temperature (solder 4 s)		260	°C
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750
		Machine model (MM)	±150

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
T <sub>A</sub>	Ambient temperature	–40	25	105	°C
T <sub>J</sub>	Junction temperature			125	°C
V <sub>CC</sub>	Core supply voltage	3.15	3.3	3.45	V
V <sub>CCO</sub>	Output supply voltage <sup>(1) (2)</sup>	3.3-V range	3.3	3.3 + 5%	V
		2.5-V range	2.5	2.5 + 5%	

- (1) The output supply voltages or pins (V<sub>CCOA</sub>, V<sub>CCOB</sub>, and V<sub>CCOC</sub>) will be called V<sub>CCO</sub> in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
- (2) V<sub>CCO</sub> for any output bank should be less than or equal to V<sub>CC</sub> (V<sub>CCO</sub> ≤ V<sub>CC</sub>).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMK00334-Q1 <sup>(2)</sup>	UNIT
		RTV (WQFN)	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	38.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	7.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	12	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	4.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Specification assumes 5 thermal vias connect the die attach pad (DAP) to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the package. TI recommends using the maximum number of vias in the board layout.

## 6.5 Electrical Characteristics

Unless otherwise specified: V<sub>CC</sub> = 3.3 V ± 5%, V<sub>CCO</sub> = 3.3 V ± 5%, 2.5 V ± 5%, –40°C ≤ T<sub>A</sub> ≤ 105°C, CLKIn driven differentially, input slew rate ≥ 3 V/ns. Typical values represent the most likely parametric norms at V<sub>CC</sub> = 3.3 V, V<sub>CCO</sub> = 3.3 V, T<sub>A</sub> = 25°C, and at the Recommended Operation Conditions at the time of product characterization; because of this, typical values are not ensured. <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION <sup>(1)</sup>							
ICC_CORE	Core supply current, all outputs disabled	CLKinX selected			8.5	10.5	mA
		OSCin selected			10	13.5	mA
ICC_HCSL					50	58.5	mA
ICC_CMOS					3.5	5.5	mA
ICCO_HCSL	Additive output supply current, HCSL banks enabled	Includes output bank bias and load currents for both banks, R <sub>T</sub> = 50 Ω on all outputs			65	81.5	mA
ICCO_CMOS	Additive output supply current, LVCMOS output enabled	200 MHz, C <sub>L</sub> = 5 pF	V <sub>CCO</sub> = 3.3 V ±5%		9	10	mA
			V <sub>CCO</sub> = 2.5V ± 5%		7	8	mA

Unless otherwise specified:  $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $V_{CCO} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , CLKIn driven differentially, input slew rate  $\geq 3\text{ V/ns}$ . Typical values represent the most likely parametric norms at  $V_{CC} = 3.3\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization; because of this, typical values are not ensured. <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY RIPPLE REJECTION (PSRR)							
PSRR <sub>HCSL</sub>	Ripple-induced phase spur level <sup>(2)</sup>	156.25 MHz		-72		dBc	
	Differential HCSL Output	312.5 MHz		-63			
CMOS CONTROL INPUTS (CLKin_SELn, CLKout_TYPEn, REFout_EN)							
V <sub>IH</sub>	High-level input voltage			1.6		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage			GND		0.4	V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CC</sub> , internal pulldown resistor				50	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V, internal pulldown resistor		-5	0.1		μA
CLOCK INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)							
f <sub>CLKin</sub>	Input frequency range <sup>(8)</sup>	Functional up to 400 MHz Output frequency range and timing specified per output type (refer to LVCMOS output specifications)		DC		400	MHz
V <sub>IHD</sub>	Differential input high voltage	CLKin driven differentially				V <sub>CC</sub>	V
V <sub>ILD</sub>	Differential input low voltage			GND			V
V <sub>ID</sub>	Differential input voltage swing <sup>(3)</sup>			0.15		1.3	V
V <sub>CMD</sub>	Differential input CMD common-mode voltage	V <sub>ID</sub> = 150 mV		0.25		V <sub>CC</sub> - 1.2	V
		V <sub>ID</sub> = 350 mV		0.25		V <sub>CC</sub> - 1.1	
		V <sub>ID</sub> = 800 mV		0.25		V <sub>CC</sub> - 0.9	
V <sub>IH</sub>	Single-ended input high voltage	CLKinX driven single-ended (AC- or DC-coupled), CLKinX* AC-coupled to GND or externally biased within V <sub>CM</sub> range				V <sub>CC</sub>	V
V <sub>IL</sub>	Single-ended input low voltage			GND			V
V <sub>I_SE</sub>	Single-ended input voltage swing <sup>(8)</sup>			0.3		2	V <sub>pp</sub>
V <sub>CM</sub>	Single-ended input CM common-mode voltage			0.25		V <sub>CC</sub> - 1.2	V
ISO <sub>MUX</sub>	Mux isolation, CLKin0 to CLKin1	f <sub>OFFSET</sub> > 50 kHz, P <sub>CLKinX</sub> = 0 dBm	f <sub>CLKin0</sub> = 100 MHz	-84		dBc	
			f <sub>CLKin0</sub> = 200 MHz	-82			
			f <sub>CLKin0</sub> = 500 MHz	-71			
			f <sub>CLKin0</sub> = 1000 MHz	-65			
CRYSTAL INTERFACE (OSCin, OSCout)							
F <sub>CLK</sub>	External clock frequency range <sup>(8)</sup>	OSCin driven single-ended, OSCout floating				250	MHz
F <sub>XTAL</sub>	Crystal frequency range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) <sup>(4)</sup>		10		40	MHz
C <sub>IN</sub>	OSCin input capacitance			1			pF

Unless otherwise specified:  $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $V_{CCO} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , CLKIn driven differentially, input slew rate  $\geq 3\text{ V/ns}$ . Typical values represent the most likely parametric norms at  $V_{CC} = 3.3\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization; because of this, typical values are not ensured. <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HCSL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f <sub>CLKout</sub>	Output frequency range <sup>(8)</sup>	R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		DC		400	MHz
Jitter <sub>ADD_PCIE</sub>	Additive RMS phase jitter for PCIe 5.0	PCIe Gen 5 filter	CLKin: 100 MHz, slew rate ≥ 0.5 V/ns	0.015		0.03	ps
Jitter <sub>ADD_PCIE</sub>	Additive RMS phase jitter for PCIe 4.0	PCIe Gen 4, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, slew rate ≥ 1.8 V/ns	0.03			ps
Jitter <sub>ADD_PCIE</sub>	Additive RMS phase jitter for PCIe 3.0	PCIe Gen 3, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, slew rate ≥ 0.6 V/ns	0.03			ps
Jitter <sub>ADD</sub>	Additive RMS jitter integration bandwidth 12 MHz to 20 MHz <sup>(5)</sup>	V <sub>CCO</sub> = 3.3 V, R <sub>T</sub> = 50 Ω to GND	CLKin: 100 MHz, slew rate ≥ 3 V/ns	77			fs
Noise Floor	Noise floor f <sub>OFFSET</sub> ≥ 10 MHz <sup>(6) (7)</sup>	V <sub>CCO</sub> = 3.3 V, R <sub>T</sub> = 50 Ω to GND	CLKin: 100 MHz, slew rate ≥ 3 V/ns	−161.3			dBc/Hz
DUTY	Duty cycle <sup>(8)</sup>	50% input clock duty cycle		45%		55%	
V <sub>OH</sub>	Output high voltage	T <sub>A</sub> = 25°C, DC measurement, R <sub>T</sub> = 50 Ω to GND		520	810	920	mV
V <sub>OL</sub>	Output low voltage			−150	0.5	150	mV
V <sub>CROSS</sub>	Absolute crossing voltage <sup>(9)</sup>	R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		350			mV
t <sub>R</sub>	Output rise time 20% to 80% <sup>(9) (12)</sup>	250 MHz, uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		225		400	ps
t <sub>F</sub>	Output fall time 80% to 20% <sup>(9) (12)</sup>			225		400	ps
LVCMOS OUTPUT (REFout)							
f <sub>CLKout</sub>	Output frequency range <sup>(8)</sup>	C <sub>L</sub> ≤ 5 pF		DC		250	MHz
Jitter <sub>ADD</sub>	Additive RMS jitter integration bandwidth 1 MHz to 20 MHz <sup>(5)</sup>	V <sub>CCO</sub> = 3.3 V, C <sub>L</sub> ≤ 5 pF	100 MHz, input slew rate ≥ 3 V/ns	95			fs
Noise Floor	Noise floor f <sub>OFFSET</sub> ≥ 10 MHz <sup>(6) (7)</sup>	V <sub>CCO</sub> = 3.3 V, C <sub>L</sub> ≤ 5 pF	100 MHz, input slew rate ≥ 3 V/ns	−159.3			dBc/Hz
DUTY	Duty cycle <sup>(8)</sup>	50% input clock duty cycle		45%		55%	
V <sub>OH</sub>	Output high voltage	1-mA load		V <sub>CCO</sub> − 0.1			V
V <sub>OL</sub>	Output low voltage			0.1			V
I <sub>OH</sub>	Output high current (source)	V <sub>O</sub> = V <sub>CCO</sub> / 2	V <sub>CCO</sub> = 3.3 V	28			mA
I <sub>OL</sub>	Output low current (sink)		V <sub>CCO</sub> = 2.5 V	20			
			V <sub>CCO</sub> = 3.3 V	28		mA	
			V <sub>CCO</sub> = 2.5 V	20			
t <sub>R</sub>	Output rise time 20% to 80% <sup>(9)</sup>	250 MHz, uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		225			ps
t <sub>F</sub>	Output fall time 80% to 20% <sup>(10)</sup>			225			ps
t <sub>EN</sub>	Output enable time <sup>(10)</sup>	C <sub>L</sub> ≤ 5 pF		3			cycles
t <sub>DIS</sub>	Output disable time <sup>(10)</sup>			3			cycles

- (1) See [Power Supply Recommendations](#) and [Thermal Management](#) for more information on current consumption and power dissipation calculations.
- (2) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the  $V_{CCO}$  supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:  $\text{DJ (ps pk-pk)} = [(2 \times 10^{(\text{PSRR}/20)}) / (\pi \times f_{\text{CLK}})] \times 1\text{E}12$
- (3) See [Differential Voltage Measurement Terminology](#) for definition of  $V_{\text{ID}}$  and  $V_{\text{OD}}$  voltages.
- (4) The ESR requirements stated must be met to ensure that the oscillator circuitry has no start-up issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to [Crystal Interface](#) for crystal drive level considerations.

- (5) For the 100-MHz and 156.25-MHz clock input conditions, Additive RMS Jitter ( $J_{ADD}$ ) is calculated using Method #1:  $J_{ADD} = \text{SQRT}(J_{OUT}^2 - J_{SOURCE}^2)$ , where  $J_{OUT}$  is the total RMS jitter measured at the output driver and  $J_{SOURCE}$  is the RMS jitter of the clock source applied to CLKIn. For the 625-MHz clock input condition, Additive RMS Jitter is approximated using Method #2:  $J_{ADD} = \text{SQRT}(2 \times 10^{\text{dBc}/10}) / (2 \times \pi \times f_{CLK})$ , where dBc is the phase noise power of the Output Noise Floor integrated from 12-kHz to 20-MHz bandwidth. The phase noise power can be calculated as:  $\text{dBc} = \text{Noise Floor} + 10 \times \log_{10}(20 \text{ MHz} - 12 \text{ kHz})$ .
- (6) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is  $\geq 10$  MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.
- (7) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common-mode noise rejection. However, TI recommends using the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.
- (8) Specification is ensured by characterization and is not tested in production.
- (9) AC timing parameters for HCSL or LVCMOS are dependent on output capacitive loading.
- (10) Output Enable Time is the number of input clock cycles it takes for the output to be enabled after REFout\_EN is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after REFout\_EN is pulled low. The REFout\_EN signal should have an edge transition much faster than that of the input clock period for accurate measurement.
- (11) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.
- (12) Parameter is specified by design, not tested in production.

## 6.6 Propagation Delay and Output Skew

			MIN	TYP	MAX	UNIT
$t_{PD\_HCSL}$	Propagation delay CLKIn-to-HCSL <sup>(1)</sup>	$R_T = 50 \Omega$ to GND, $C_L \leq 5 \text{ pF}$		590		ps
$t_{PD\_CMOS}$	Propagation delay CLKIn-to-LVCMOS <sup>(1)</sup>	$C_L \leq 5 \text{ pF}$		1475		ps
		$V_{CCO} = 3.3 \text{ V}$ $V_{CCO} = 2.5 \text{ V}$		1550		
$t_{SK(O)}$	Output skew <sup>(1) (9)</sup>	Skew specified between any two CLKouts. Load conditions are the same as propagation delay specifications.		30		ps
$t_{SK(PP)}$	Part-to-part output skew <sup>(1) (2)</sup>			80		ps

- (1) AC timing parameters for HCSL or LVCMOS are dependent on output capacitive loading.
- (2) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

## 6.7 Typical Characteristics

Unless otherwise specified:  $V_{CC} = 3.3\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , CLKIn driven differentially, input slew rate  $\geq 3\text{ V/ns}$ .

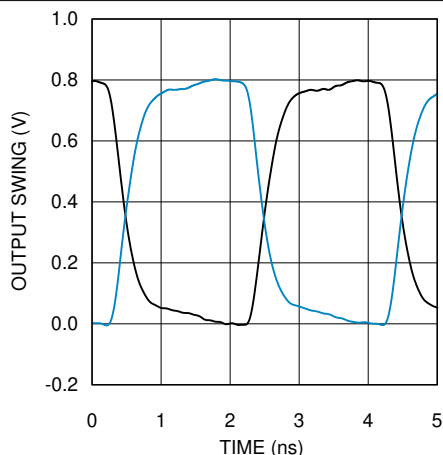


FIG 6-1. HCSL Output Swing at 250 MHz

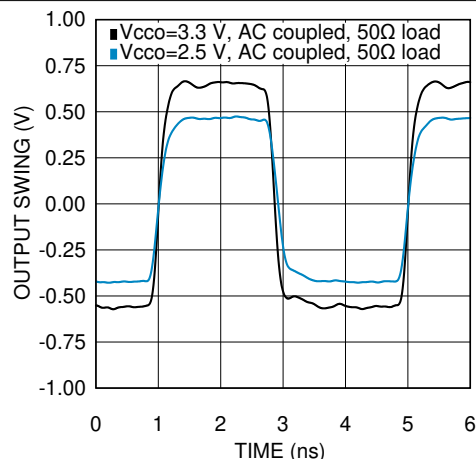


FIG 6-2. LVCMOS Output Swing at 250 MHz

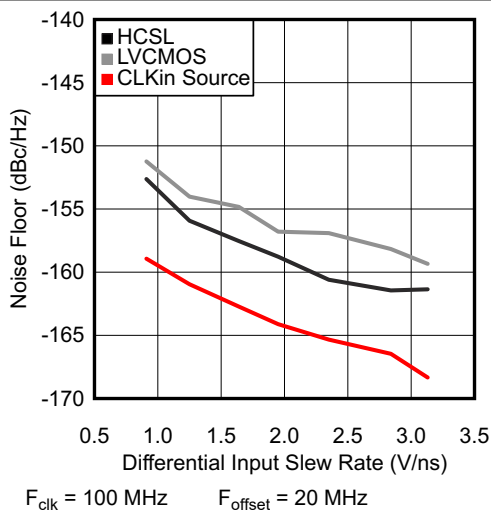


FIG 6-3. Noise Floor vs. CLKIn Slew Rate at 100 MHz

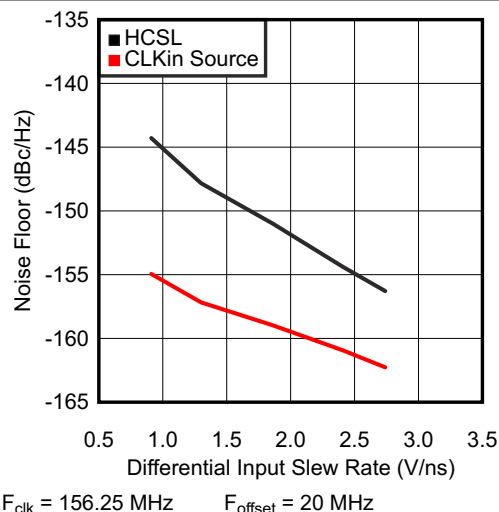


FIG 6-4. Noise Floor vs. CLKIn Slew Rate at 156.25 MHz

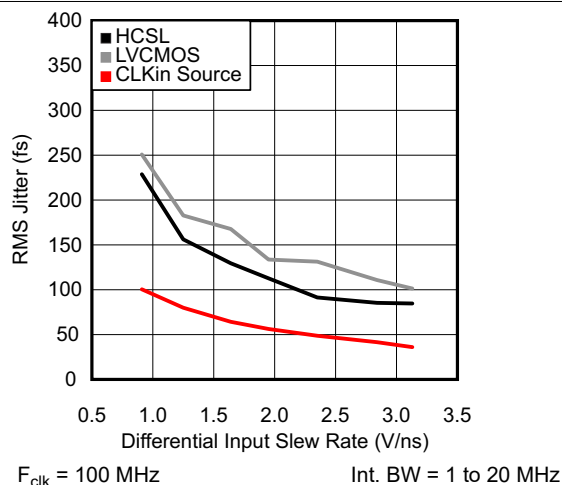


FIG 6-5. RMS Jitter vs. CLKIn Slew Rate at 100 MHz

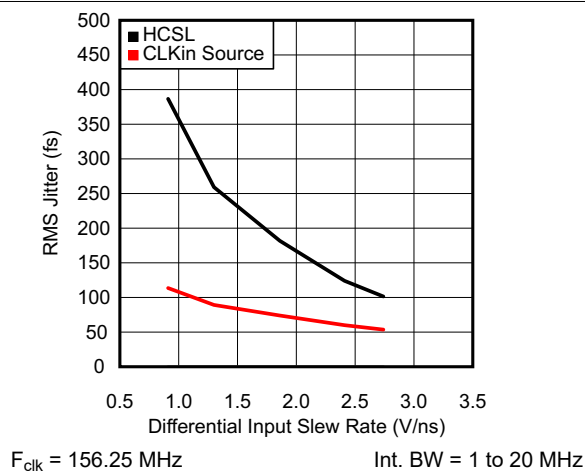
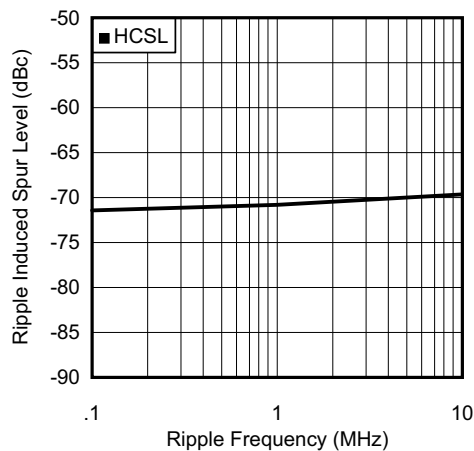


FIG 6-6. RMS Jitter vs. CLKIn Slew Rate at 156.25 MHz

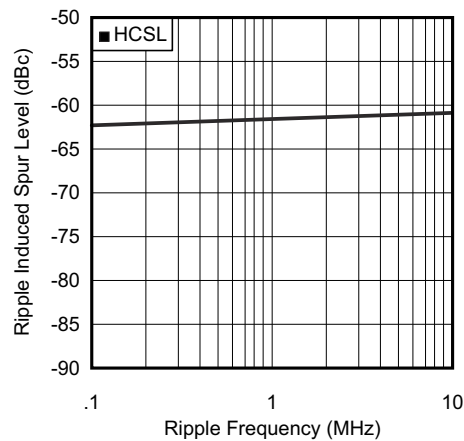
## 6.7 Typical Characteristics (continued)

Unless otherwise specified:  $V_{CC} = 3.3\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , CLKIn driven differentially, input slew rate  $\geq 3\text{ V/ns}$ .



$F_{\text{clk}} = 156.25\text{ MHz}$   $V_{\text{CCO}} \text{ Ripple} = 100\text{ mV}_{\text{pp}}$

FIG 6-7. PSRR vs. Ripple Frequency at 156.25 MHz



$F_{\text{clk}} = 312.5\text{ MHz}$   $V_{\text{CCO}} \text{ Ripple} = 100\text{ mV}_{\text{pp}}$

FIG 6-8. PSRR vs. Ripple Frequency at 312.5 MHz

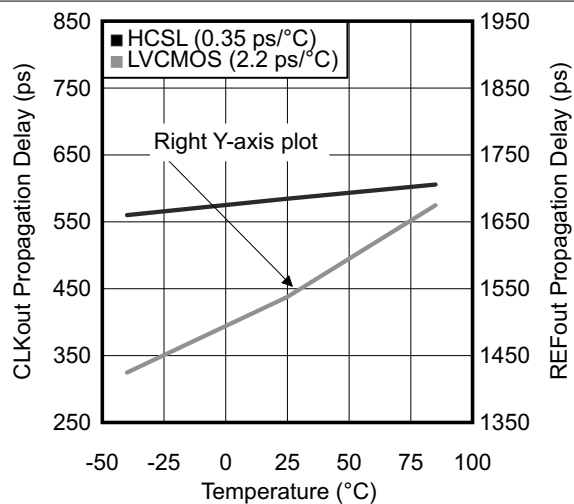


FIG 6-9. Propagation Delay vs. Temperature

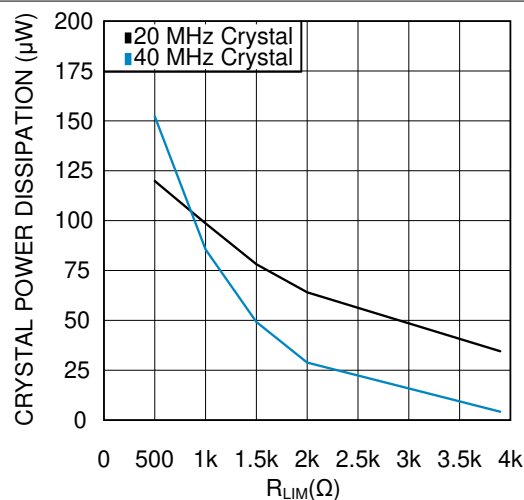


FIG 6-10. Crystal Power Dissipation vs.  $R_{\text{LIM}}$

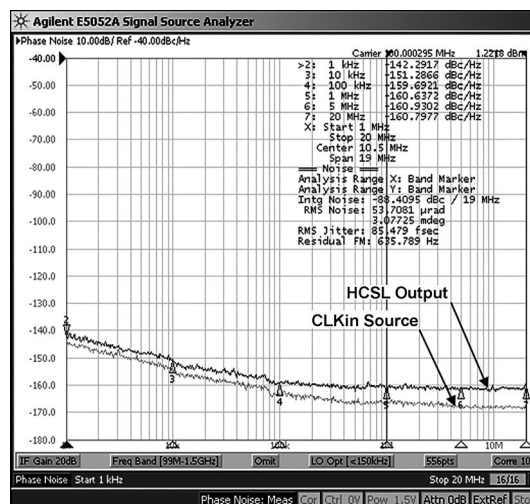


FIG 6-11. HCSL Phase Noise at 100 MHz

## 7 Parameter Measurement Information

### 7.1 Differential Voltage Measurement Terminology

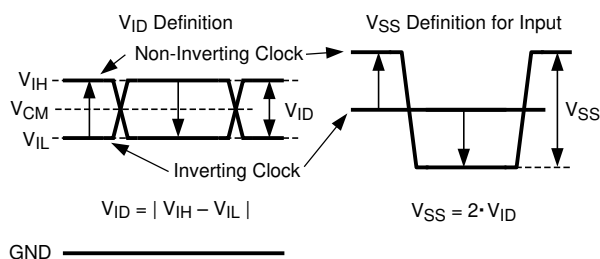
The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically  $V_{ID}$  or  $V_{OD}$  depending on if an input or output voltage is being described.

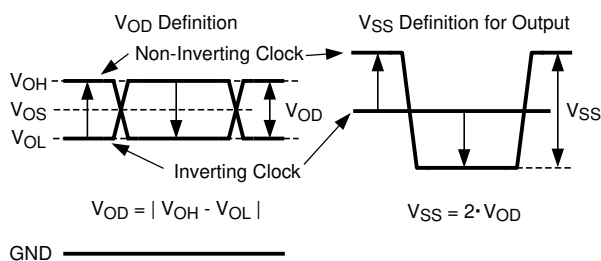
The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is  $V_{SS}$  and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground; it only exists in reference to its differential pair.  $V_{SS}$  can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of  $V_{OD}$  as described in the first description.

Figure 7-1 illustrates the two different definitions side-by-side for inputs and Figure 7-2 illustrates the two different definitions side-by-side for outputs. The  $V_{ID}$  (or  $V_{OD}$ ) definition shows the DC levels,  $V_{IH}$  and  $V_{OL}$  (or  $V_{OH}$  and  $V_{OL}$ ), that the noninverting and inverting signals toggle between with respect to ground.  $V_{SS}$  input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

$V_{ID}$  and  $V_{OD}$  are often defined as volts (V) and  $V_{SS}$  is often defined as volts peak-to-peak ( $V_{PP}$ ).



**Figure 7-1. Two Different Definitions for Differential Input Signals**



**Figure 7-2. Two Different Definitions for Differential Output Signals**

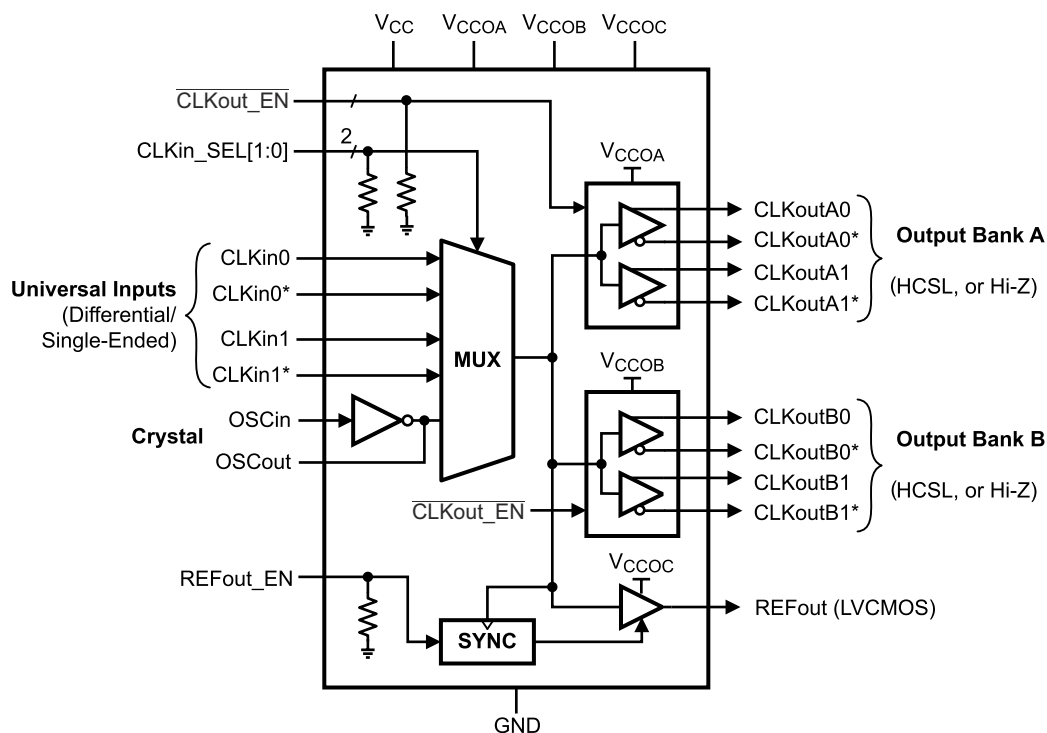
Refer to [Common Data Transmission Parameters and their Definitions](#) (SNLA036) for more information.

## 8 Detailed Description

### 8.1 Overview

The LMK00334-Q1 is a 4-output HCSL clock fanout buffer with low additive jitter that can operate up to 400 MHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of two HCSL outputs, one LVCMOS output, and three independent output buffer supplies. The input selection and output buffer modes are controlled through pin strapping. The device is offered in a 32-pin WQFN package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Crystal Power Dissipation vs. $R_{LIM}$

For [Figure 6-10](#), the following applies:

- The typical RMS jitter values in the plots show the total output RMS jitter ( $J_{OUT}$ ) for each output buffer type and the source clock RMS jitter ( $J_{SOURCE}$ ). From these values, the Additive RMS Jitter can be calculated as:  

$$J_{ADD} = \sqrt{J_{OUT}^2 - J_{SOURCE}^2}$$
- 20-MHz crystal characteristics: Abracon ABL series, AT cut,  $C_L = 18$  pF,  $C_0 = 4.4$  pF measured (7 pF maximum), ESR = 8.5  $\Omega$  measured (40  $\Omega$  maximum), and Drive Level = 1 mW maximum (100  $\mu$ W typical).
- 40-MHz crystal characteristics: Abracon ABLS2 series, AT cut,  $C_L = 18$  pF,  $C_0 = 5$  pF measured (7 pF maximum), ESR = 5  $\Omega$  measured (40  $\Omega$  maximum), and Drive Level = 1 mW maximum (100  $\mu$ W typical).

### 8.3.2 Clock Inputs

The input clock can be selected from CLKIn0/CLKIn0\*, CLKIn1/CLKIn1\*, or OSCIn. Clock input selection is controlled using the CLKIn\_SEL[1:0] inputs as shown in 表 8-1. Refer to [Driving the Clock Inputs](#) for clock input requirements. When CLKIn0 or CLKIn1 is selected, the crystal circuit is powered down. When OSCIn is selected, the crystal oscillator circuit will start up and its clock will be distributed to all outputs. Refer to [Crystal Interface](#) for more information. Alternatively, OSCIn may be driven by a single-ended clock (up to 250 MHz) instead of a crystal.

**表 8-1. Input Selection**

CLKIn_SEL1	CLKIn_SEL0	SELECTED INPUT
0	0	CLKIn0, CLKIn0*
0	1	CLKIn1, CLKIn1*
1	X	OSCIn

表 8-2 shows the output logic state vs. input state when either CLKIn0/CLKIn0\* or CLKIn1/CLKIn1\* is selected. When OSCIn is selected, the output state will be an inverted copy of the OSCIn input state.

**表 8-2. CLKIn Input vs. Output States**

STATE OF SELECTED CLKIn	STATE OF ENABLED OUTPUTS
CLKInX and CLKInX* inputs floating	Logic low
CLKInX and CLKInX* inputs shorted together	Logic low
CLKIn logic low	Logic low
CLKIn logic high	Logic high

### 8.3.3 Clock Outputs

The HCSL output buffer for both Bank A and B outputs are can be disabled to Hi-Z using the  $\overline{\text{CLKout\_EN}}$  [1:0] as shown in 表 8-3. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If all differential outputs are not used, TI recommends disabling (Hi-Z) the banks to reduce power. Refer to [Termination and Use of Clock Drivers](#) for more information on output interface and termination techniques.

#### Note

For best soldering practices, the minimum trace length for any unused pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

**表 8-3. Differential Output Buffer Type Selection**

CLKout_EN	CLKoutX BUFFER TYPE (BANK A AND B)
0	HCSL
1	Disabled (Hi-Z)

### 8.3.3.1 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the  $V_{CCO}$  voltage. REFout can be enabled or disabled using the enable input pin, REFout\_EN, as shown in [表 8-4](#).

**表 8-4. Reference Output Enable**

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

The REFout\_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout will be enabled within three cycles ( $t_{EN}$ ) of the input clock after REFout\_EN is toggled high. REFout will be disabled within three cycles ( $t_{DIS}$ ) of the input clock after REFout\_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1-k $\Omega$  load to ground, then the output will be pulled to low when disabled.

## 8.4 Device Functional Modes

### 8.4.1 $V_{CC}$ and $V_{CCO}$ Power Supplies

The LMK00334-Q1 has separate 3.3-V core supplies ( $V_{CC}$ ) and three independent 3.3-V or 2.5-V output power supplies ( $V_{CCOA}$ ,  $V_{CCOB}$ ,  $V_{CCOC}$ ). Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5-V receiver devices. The output levels for HCSL are relatively constant over the specified  $V_{CCO}$  range. Refer to [Power Supply Recommendations](#) for additional supply related considerations, such as power dissipation, power supply bypassing, and power supply ripple rejection (PSRR).

#### Note

Take care to ensure the  $V_{CCO}$  voltages do not exceed the  $V_{CC}$  voltage to prevent turning-on the internal ESD protection circuitry.

## 9 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

A common automotive PCIe application, such as ADAS (Advanced Driver Assistance Systems), requires several clocks and timing sources to drive the building blocks of the system. In a common ADAS system, the clock is distributed to an SoC, PCIe Switch, WiFi Controller, and Gigabit Ethernet to transmit high-speed video data from the IP-Based Cameras on the vehicle. The LMK00334-Q1 provides an automotive qualified solution that saves cost and space. When transmitting high-speed video data, the additive jitter of the buffer clock may noticeably impact performance. In order to optimize signal speed and cable length, system designs must account for this additive jitter. The LMK00334-Q1 is an ultra-low-jitter PCIe clock buffer suitable for current and future automotive PCIe applications.

### 9.2 Typical Application

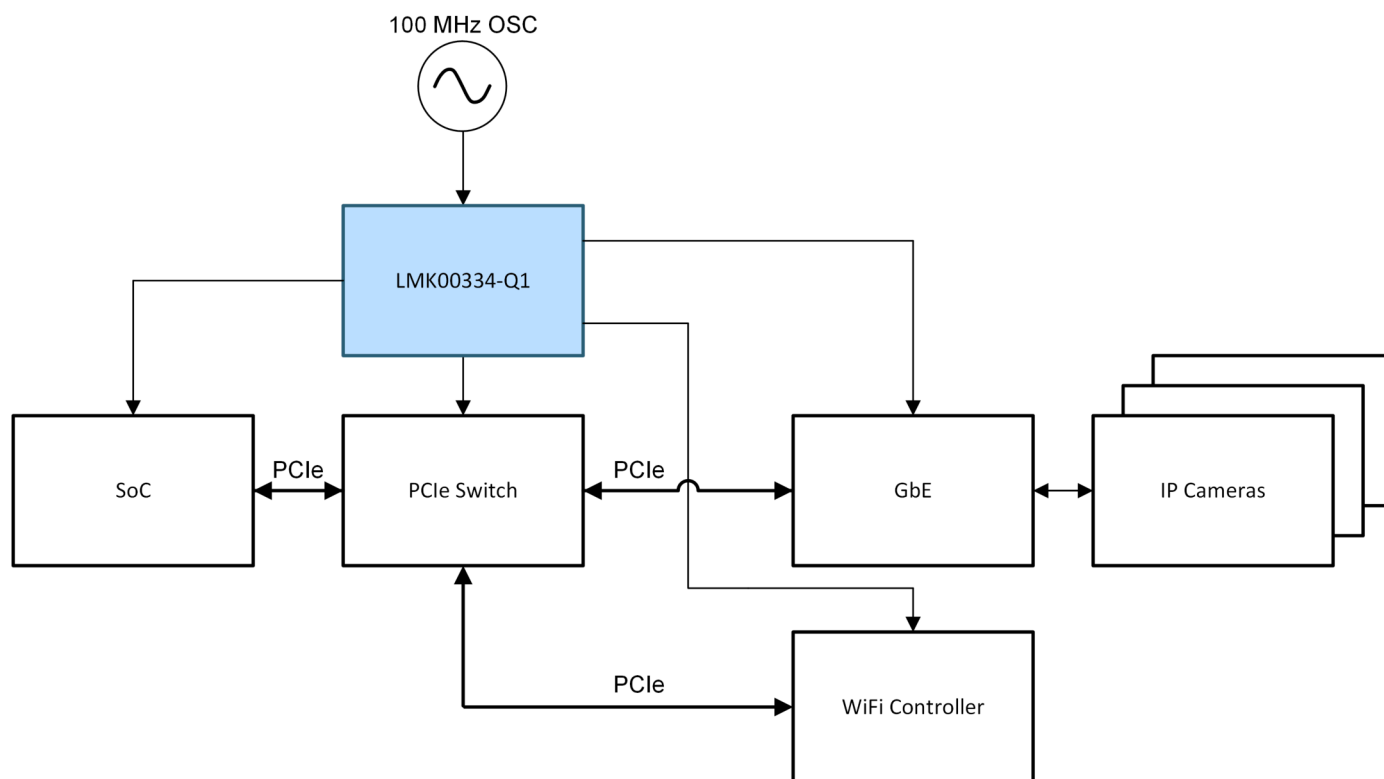


図 9-1. Example Automotive Application

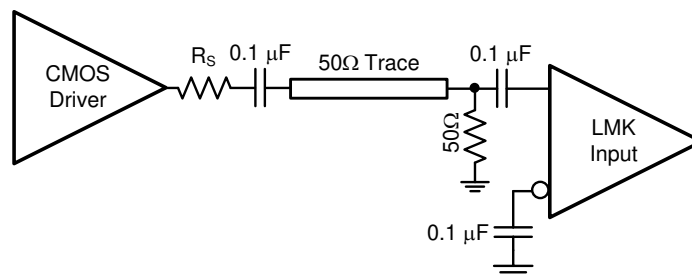
## 9.2.1 Design Requirements

### 9.2.1.1 Driving the Clock Inputs

The LMK00334-Q1 has two universal inputs (CLKin0/CLKin0\* and CLKin1/CLKin1\*) that can accept DC-coupled, 3.3-V or 2.5-V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in [Electrical Characteristics](#). The device can accept a wide range of signals due to its wide input common-mode voltage range ( $V_{CM}$ ) and input voltage swing ( $V_{ID}$ ) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the  $V_{CM}$  range. Refer to [Termination and Use of Clock Drivers](#) for signal interfacing and termination techniques.

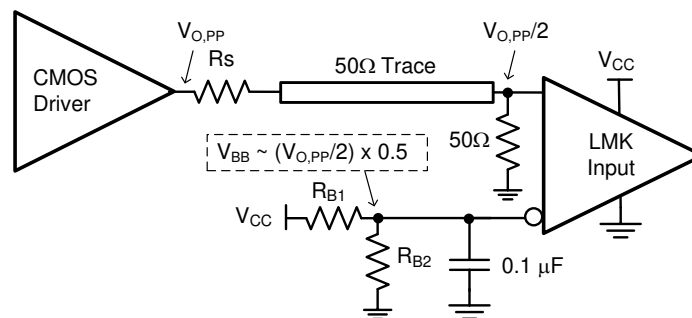
To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode rejection. Refer to the *Noise Floor vs. CLKin Slew Rate* and *RMS Jitter vs. CLKin Slew Rate* plots in [Typical Characteristics](#).

While TI recommends driving the CLKin/CLKin\* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the single-ended input specifications for CLKin pins listed in the [Electrical Characteristics](#). For large single-ended input signals, such as 3.3-V or 2.5-V LVCMOS, a 50-Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in [Figure 9-2](#). The output impedance of the LVCMOS driver plus  $R_s$  should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.



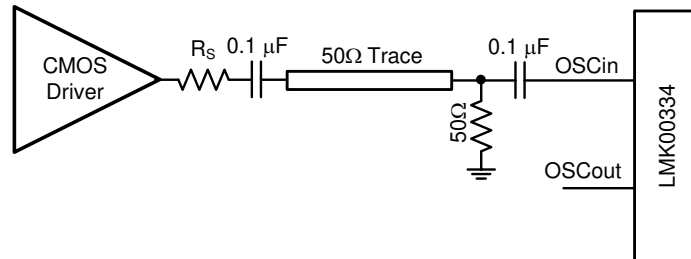
**Figure 9-2. Single-Ended LVCMOS Input, AC Coupling**

A single-ended clock may also be DC-coupled to CLKinX as shown in [Figure 9-3](#). A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ( $V_{O,PP} / 2$ ) drives CLKinX, CLKinX\* should be externally biased to the midpoint voltage of the attenuated input swing ( $(V_{O,PP} / 2) \times 0.5$ ). The external bias voltage should be within the specified input common voltage ( $V_{CM}$ ) range. This can be achieved using external biasing resistors in the kΩ range ( $R_{B1}$  and  $R_{B2}$ ) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.



**Figure 9-3. Single-Ended LVCMOS Input, DC Coupling With Common-Mode Biasing**

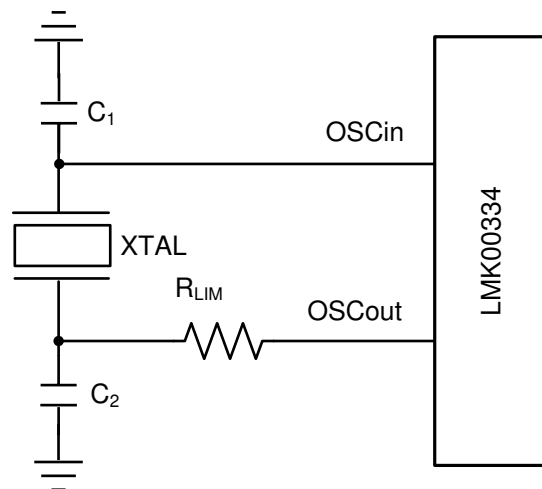
If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with a single-ended external clock as shown in 9-4. The input clock should be AC coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, TI recommends using either universal input (CLKinX) because it offers higher operating frequency, better common-mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.



9-4. Driving OSCin With a Single-Ended Input

### 9.2.1.2 Crystal Interface

The LMK00334-Q1 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in 9-5.



9-5. Crystal Interface

The load capacitance ( $C_L$ ) is specific to the crystal, but usually on the order of 18 to 20 pF. While  $C_L$  is specified for the crystal, the OSCin input capacitance ( $C_{IN} = 1$  pF typical) of the device and PCB stray capacitance ( $C_{STRAY}$  is approximately around 1 to 3 pF) can affect the discrete load capacitor values,  $C_1$  and  $C_2$ .

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically,  $C_1 = C_2$  for optimum symmetry, so 1 can be rewritten in terms of  $C_1$  only:

$$C_L = C_1^2 / (2 \times C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for  $C_1$ :

$$C_1 = (C_L - C_{IN} - C_{STRAY}) \times 2 \quad (3)$$

[Electrical Characteristics](#) provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer must ensure the crystal power dissipation

does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start up and maintain steady-state operation.

The power dissipated in the crystal,  $P_{XTAL}$ , can be computed by:

$$P_{XTAL} = I_{RMS}^2 \times R_{ESR} \times (1 + C_0/C_L)^2 \quad (4)$$

where

- $I_{RMS}$  is the RMS current through the crystal.
- $R_{ESR}$  is the maximum equivalent series resistance specified for the crystal
- $C_L$  is the load capacitance specified for the crystal
- $C_0$  is the minimum shunt capacitance specified for the crystal

$I_{RMS}$  can be measured using a current probe (Tektronix CT-6 or equivalent, for example) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in [Figure 9-5](#), an external resistor,  $R_{LIM}$ , can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with  $R_{LIM}$  shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with  $R_{LIM}$  shorted, then a zero value for  $R_{LIM}$  can be used. As a starting point, a suggested value for  $R_{LIM}$  is 1.5 k $\Omega$ .

## 9.2.2 Detailed Design Procedure

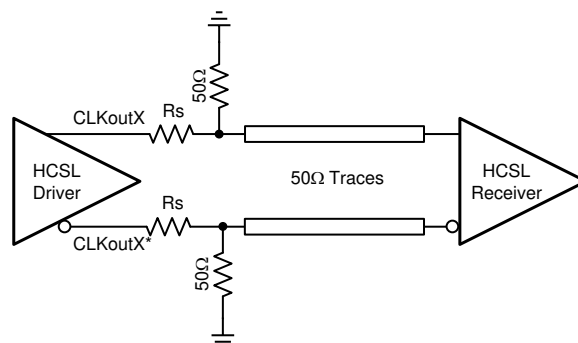
### 9.2.2.1 Termination and Use of Clock Drivers

When terminating clock drivers, keep these guidelines in mind for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - HCSL drivers are switched current outputs and require a DC path to ground through 50- $\Omega$  termination.
- Receivers should be presented with a signal biased to their specified DC bias level (common-mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

### 9.2.2.2 Termination for DC-Coupled Differential Operation

For DC-coupled operation of an HCSL driver, terminate with 50  $\Omega$  to ground near the driver output as shown in [Figure 9-6](#). Series resistors,  $R_s$ , may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50- $\Omega$  termination resistors.

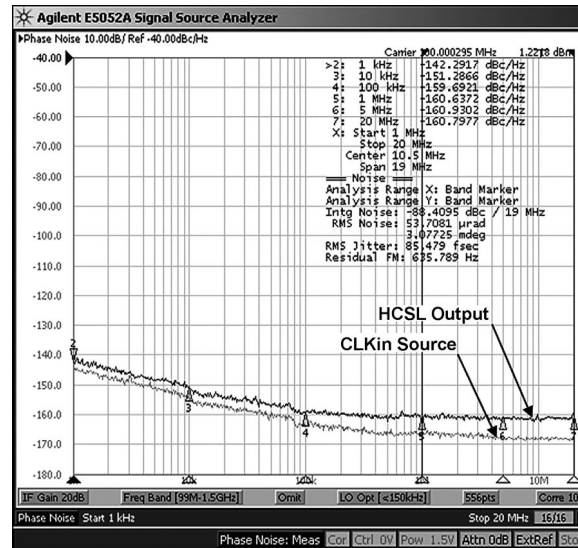


**Figure 9-6. HCSL Operation, DC Coupling**

### 9.2.2.3 Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common-mode voltage) when driving different receiver standards. Because AC-coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

### 9.2.3 Application Curve



9-7. HCSL Phase Noise at 100 MHz

## 10 Power Supply Recommendations

### 10.1 Current Consumption and Power Dissipation Calculations

The current consumption values specified in [Electrical Characteristics](#) can be used to calculate the total power dissipation and IC power dissipation for any device configuration. The total  $V_{CC}$  core supply current ( $I_{CC\_TOTAL}$ ) can be calculated using [式 5](#):

$$I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANKS} + I_{CC\_CMOS} \quad (5)$$

where

- $I_{CC\_CORE}$  is the  $V_{CC}$  current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- $I_{CC\_HCSL}$  is the  $V_{CC}$  current for Banks A and B
- $I_{CC\_CMOS}$  is the  $V_{CC}$  current for the LVCMOS output (or 0 mA if REFout is disabled).

Because the output supplies ( $V_{CCOA}$ ,  $V_{CCOB}$ ,  $V_{CCOC}$ ) can be powered from three independent voltages, the respective output supply currents ( $I_{CCO\_BANK\_A}$ ,  $I_{CCO\_BANK\_B}$ , and  $I_{CCO\_CMOS}$ ) should be calculated separately.

$I_{CCO\_BANK}$  for either Bank A or B may be taken as 50% of the corresponding output supply current specified for two banks ( $I_{CCO\_HCSL}$ ) **provided the output loading matches the specified conditions**. Otherwise,  $I_{CCO\_BANK}$  should be calculated per bank as shown in [式 6](#):

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N \times I_{OUT\_LOAD}) \quad (6)$$

where

- $I_{BANK\_BIAS}$  is the output bank bias current (fixed value).
- $I_{OUT\_LOAD}$  is the DC load current per loaded output pair.
- $N$  is the number of loaded output pairs ( $N = 0$  to 2).

[表 10-1](#) shows the typical  $I_{BANK\_BIAS}$  values and  $I_{OUT\_LOAD}$  expressions for HCSL.

**表 10-1. Typical Output Bank Bias and Load Currents**

CURRENT PARAMETER	HCSL
$I_{BANK\_BIAS}$	2.4 mA
$I_{OUT\_LOAD}$	$V_{OH}/R_T$

Once the current consumption is known for each supply, the total power dissipation ( $P_{TOTAL}$ ) can be calculated by [式 7](#):

$$P_{TOTAL} = (V_{CC} \times I_{CC\_TOTAL}) + (V_{CCOA} \times I_{CCO\_BANK}) + (V_{CCOB} \times I_{CCO\_BANK}) + (V_{CCOC} \times I_{CCO\_CMOS}) \quad (7)$$

If the device is configured with HCSL outputs, then it is also necessary to calculate the power dissipated in any termination resistors ( $P_{RT\_HCSL}$ ). The external power dissipation values can be calculated by [式 8](#):

$$P_{RT\_HCSL} \text{ (per HCSL pair)} = V_{OH}^2 / R_T \quad (8)$$

Finally, the IC power dissipation ( $P_{DEVICE}$ ) can be computed by subtracting the external power dissipation values from  $P_{TOTAL}$  as shown in [式 9](#):

$$P_{DEVICE} = P_{TOTAL} - N \times P_{RT\_HCSL} \quad (9)$$

where

- $N$  is the number of HCSL output pairs with termination resistors to GND.

### 10.1.1 Power Dissipation Example: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate **worst-case power dissipation**. In this case, the maximum supply voltage and supply current values specified in [Electrical Characteristics](#) are used:

- Max  $V_{CC} = V_{CCO} = 3.465\text{ V}$ . Max  $I_{CC}$  and  $I_{CCO}$  values.
- CLKIn0/CLKIn0\* input is selected.
- Banks A and B are enabled, and all outputs are terminated with  $50\ \Omega$  to GND.
- REFout is enabled with 5-pF load.
- $T_A = 105^\circ\text{C}$

Using the power calculations from the previous section and *maximum* supply current specifications, the user can compute  $P_{TOTAL}$  and  $P_{DEVICE}$ :

- From [式 5](#):  $I_{CC\_TOTAL} = 10.5\text{ mA} + 58.5\text{ mA} + 5.5\text{ mA} = 74.5\text{ mA}$
- From  $I_{CCO\_HCSL}$  max spec:  $I_{CCO\_BANK} = 50\%$  of  $I_{CCO\_HCSL} = 40.75\text{ mA}$
- From [式 7](#):  $P_{TOTAL} = (3.465\text{ V} \times 74.5\text{ mA}) + (3.465\text{ V} \times 40.75\text{ mA}) + (3.465\text{ V} \times 40.75\text{ mA}) + (3.465\text{ V} \times 10\text{ mA}) = 575.2\text{ mW}$
- From [式 8](#):  $P_{RT\_HCSL} = (0.92\text{ V})^2 / 50\ \Omega = 16.9\text{ mW}$  (per output pair)
- From [式 9](#):  $P_{DEVICE} = 575.2\text{ mW} - (4 \times 16.9\text{ mW}) = 510.4\text{ mW}$

In this worst-case example, the IC device will dissipate about 510.4 mW or 88.7% of the total power (575.2 mW), while the remaining 11.3% will be dissipated in the termination resistors (64.8 mW for 4 pairs). Based on  $R_{\theta JA}$  of  $38.1^\circ\text{C/W}$ , the estimate die junction temperature would be about  $19.4^\circ\text{C}$  above ambient, or  $104.4^\circ\text{C}$  when  $T_A = 85^\circ\text{C}$ .

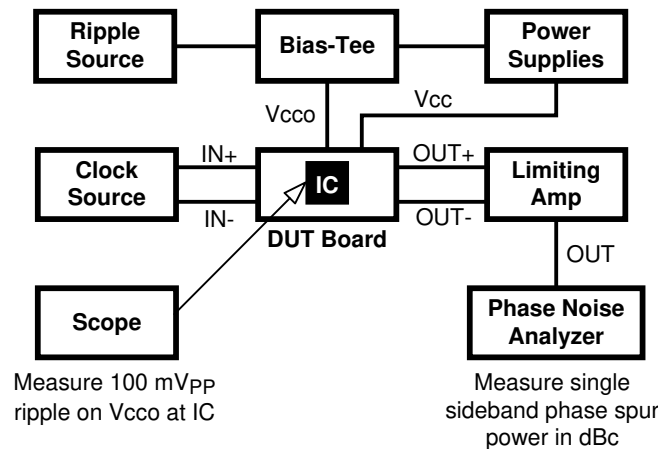
## 10.2 Power Supply Bypassing

The  $V_{CC}$  and  $V_{CCO}$  power supplies should have a high-frequency bypass capacitor, such as 0.1  $\mu\text{F}$  or 0.01  $\mu\text{F}$ , placed very close to each supply pin. 1- $\mu\text{F}$  to 10- $\mu\text{F}$  decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

### 10.2.1 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, and so forth. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00334-Q1, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00334-Q1, power supply ripple rejection, or PSRR, was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the  $V_{CCO}$  supply. The PSRR test setup is shown in [Figure 10-1](#).



**Figure 10-1. PSRR Test Setup**

A signal generator was used to inject a sinusoidal signal onto the  $V_{CCO}$  supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the  $V_{CCO}$  pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 156.25 MHz and 312.5 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on  $V_{CCO} = 2.5\text{ V}$
- Ripple frequencies: 100 kHz, 1 MHz, and 10 MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$\text{DJ (ps pk-pk)} = [(2 \times 10^{(\text{PSRR} / 20)}) / (\pi \times f_{\text{CLK}})] \times 10^{12} \quad (10)$$

The *PSRR vs. Ripple Frequency* plots in [Typical Characteristics](#) show the ripple-induced phase spur levels at 156.25 MHz and 312.5 MHz. The LMK00334-Q1 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range. The phase spur levels for HCSL are below  $-72\text{ dBc}$  at 156.25 MHz and below  $-63\text{ dBc}$  at 312.5 MHz. Using [Equation 10](#), these phase spur levels translate to Deterministic Jitter values of 1.02 ps pk-pk at 156.25 MHz and 1.44 ps pk-pk at 312.5 MHz. Testing has shown that the PSRR performance of the device improves for  $V_{CCO} = 3.3\text{ V}$  under the same ripple amplitude and frequency conditions.

## 11 Layout

### 11.1 Layout Guidelines

For this device, consider the following guidelines:

- For DC-coupled operation of an HCSL driver, terminate with 50  $\Omega$  to ground near the driver output as shown in [Figure 11-1](#).
- Keep the connections between the bypass capacitors and the power supply on the device as short as possible.
- Ground the other side of the capacitor using a low impedance connection to the ground plane.
- If the capacitors are mounted on the back side, 0402 components can be employed. However, soldering to the Thermal Dissipation Pad can be difficult.
- For component side mounting, use 0201 body size capacitors to facilitate signal routing.

### 11.2 Layout Example

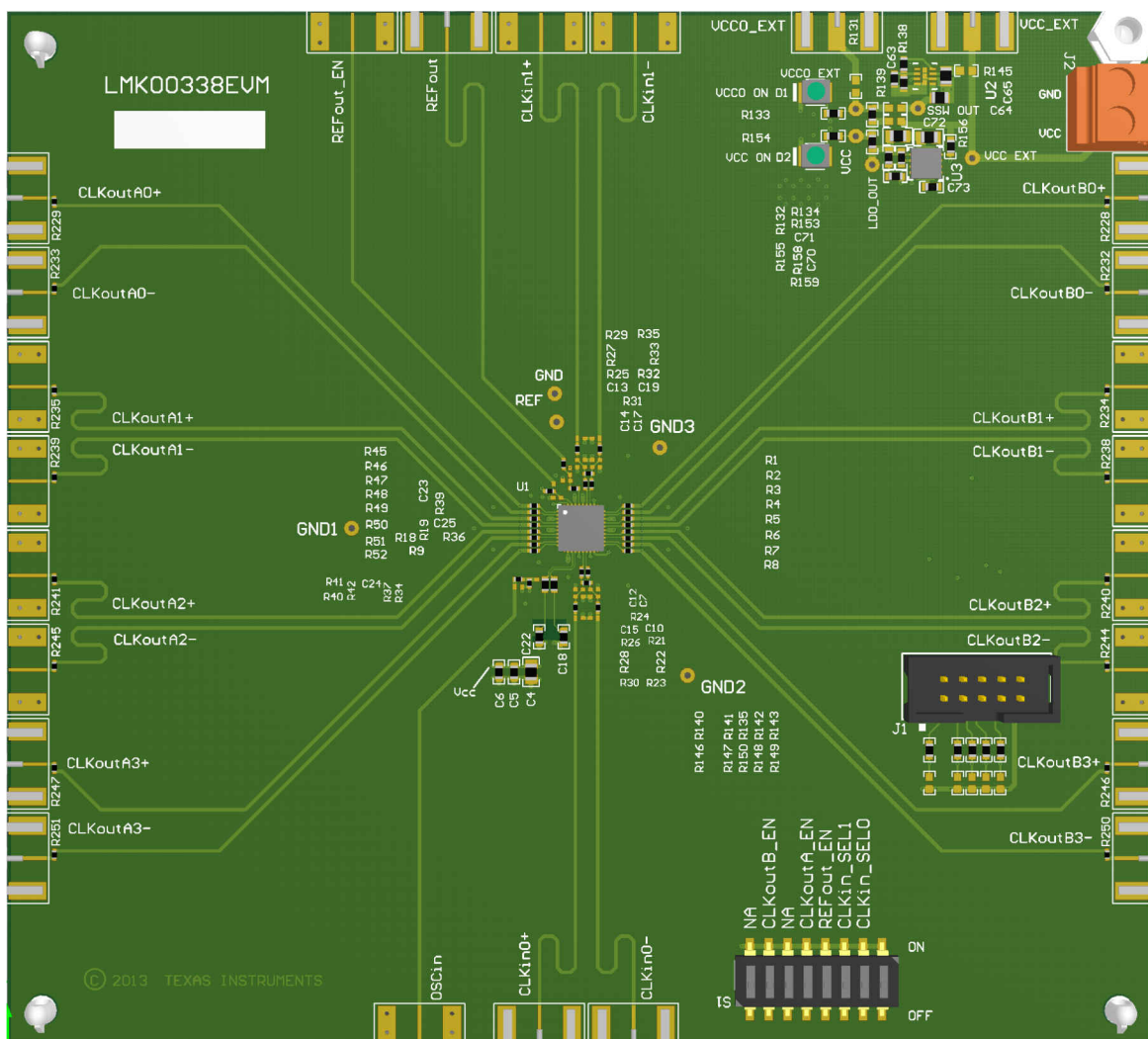


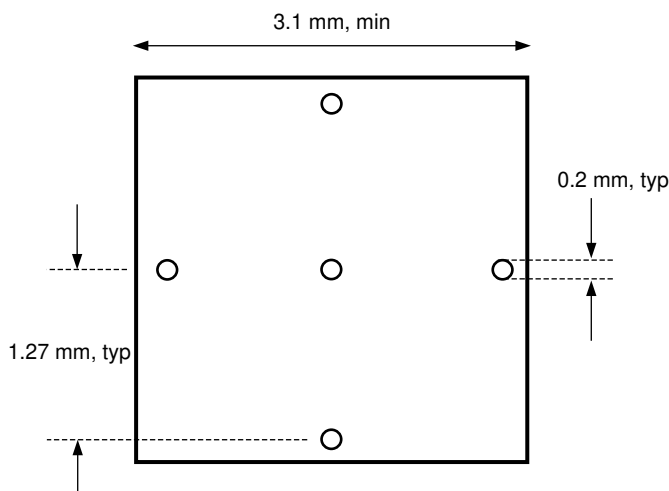
Figure 11-1. LMK00334-Q1 Layout Example

### 11.3 Thermal Management

Power dissipation in the LMK00334-Q1 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate,  $T_A$  (ambient temperature) plus device power dissipation times  $R_{\theta JA}$  should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed-circuit board. To maximize the removal of heat from the package, a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in [Figure 11-2](#). More information on soldering WQFN packages can be obtained at: <https://www.ti.com/packaging>.



**Figure 11-2. Recommended Land and Via Pattern**

To minimize junction temperature, TI recommends building a simple heat sink into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in [Figure 11-2](#) should connect these top and bottom copper layers and to the ground layer. These vias act as *heat pipes* to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documents, see the following:

- [Absolute Maximum Ratings for Soldering](#) (SNOA549)
- [Common Data Transmission Parameters and their Definitions](#) (SNLA036)
- ["How to Optimize Clock Distribution in PCIe Applications"](#) on the Texas Instruments E2E community forum
- [LMK00338EVM User's Guide](#) (SNAU155)
- [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 サポート・リソース

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#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMK00334RTVRQ1</a>	Active	Production	WQFN (RTV)   32	1000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	K00334Q
LMK00334RTVRQ1.A	Active	Production	WQFN (RTV)   32	1000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	K00334Q
<a href="#">LMK00334RTVTQ1</a>	Active	Production	WQFN (RTV)   32	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	K00334Q
LMK00334RTVTQ1.A	Active	Production	WQFN (RTV)   32	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	K00334Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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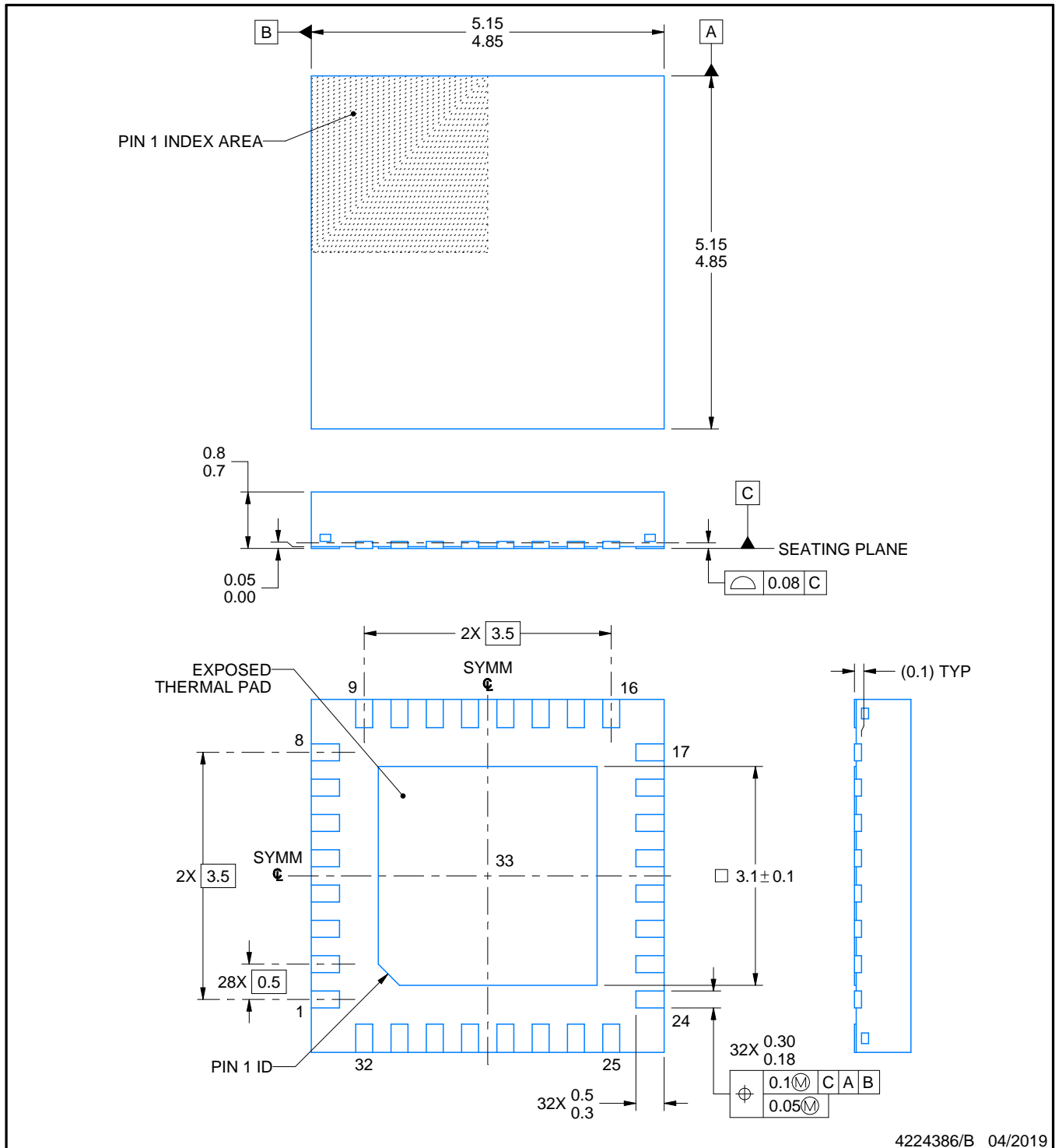
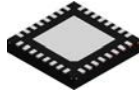
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMK00334-Q1 :**

- Catalog : [LMK00334](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



## NOTES:

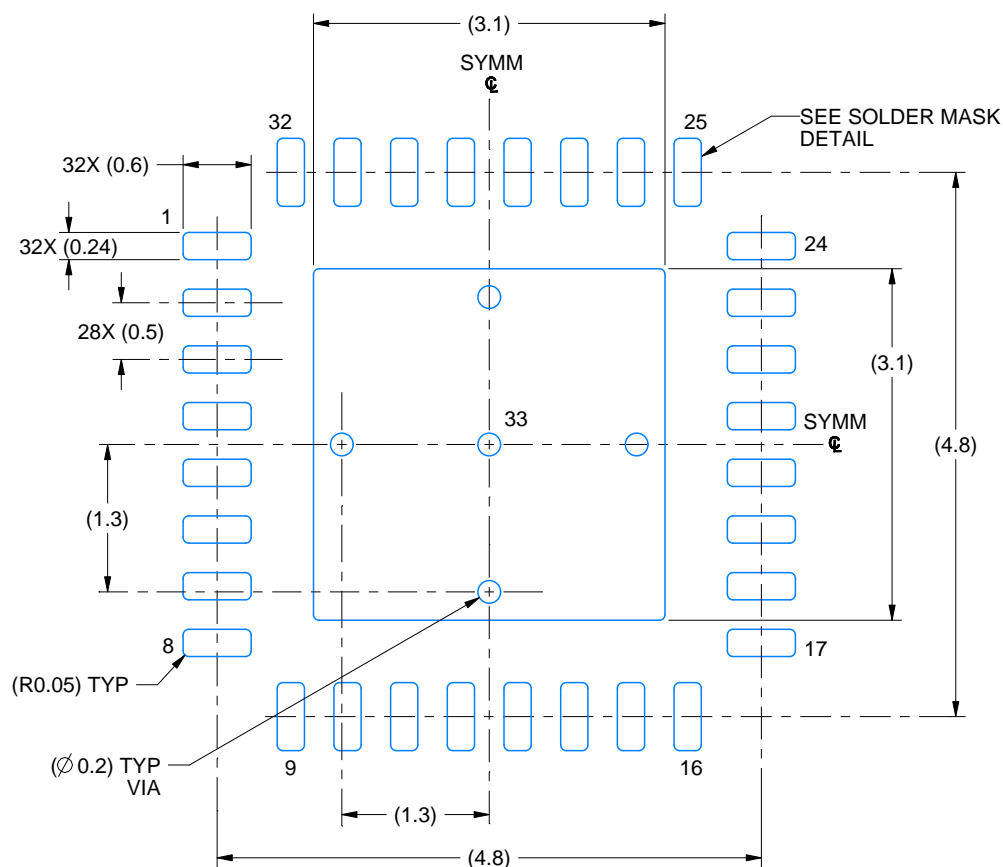
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

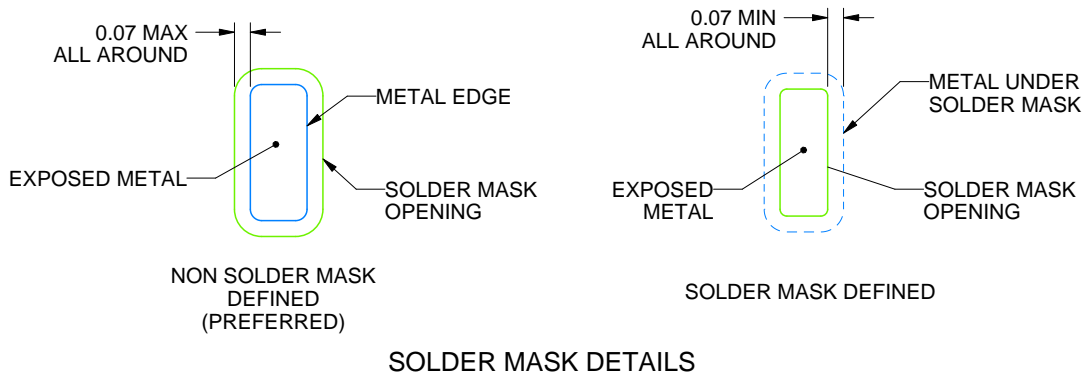
RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4224386/B 04/2019

NOTES: (continued)

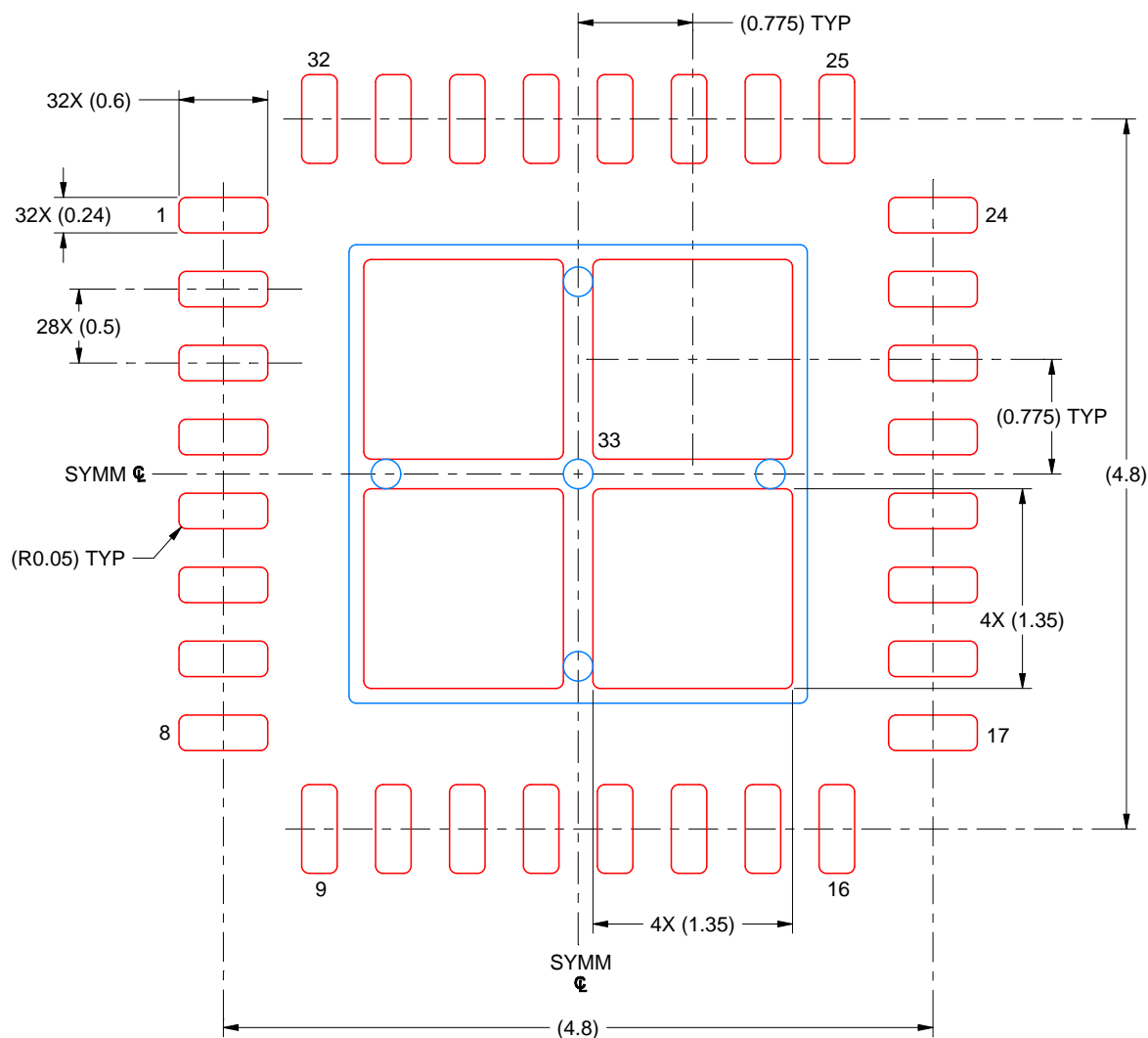
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 MM THICK STENCIL  
 SCALE: 20X

EXPOSED PAD 33  
 76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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