LMH9135 バラン内蔵 3.2～4.2GHz 差動～シングルエンド・アンプ

1 特長

- シングル・チャネル、狭帯域、差動入力シングルエンド出力、RF ゲイン・ブロック・アンプ
- 3.2～4.2GHz (標準値) の 1dB BW をサポート
- 18dB (標準値) のゲイン (帯域内)
- 3.8dB のノイズ指数
- 31.5dBm の OIP3
- 18dBm の出力 (P1dB)
- 395mW の消費電力 (+3.3V 単電源)
- 最高 T_A = 105℃の動作温度

2 アプリケーション

- GSPS DAC 用差動 DAC 出力ドライバ
- 差動→シングルエンド変換
- バランの代替品
- スモール・セルまたは m-MIMO 基地局
- 5G アクティブ・アンテナ・システム (AAS)
- 無線セルラー基地局

3 概要

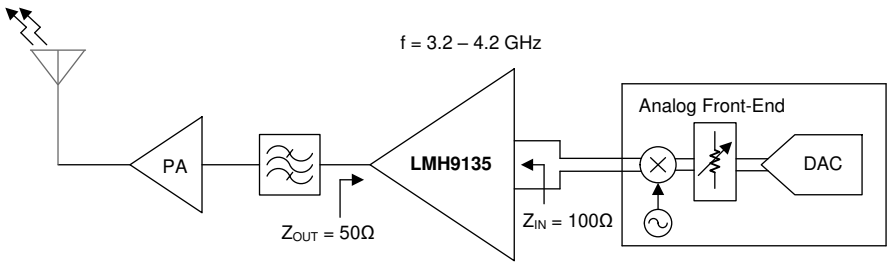
LMH9135 は、3.2～4.2GHz の周波数帯域をサポートする、高性能、シングル・チャネル、差動入力シングルエンド出力、送信無線周波数 (RF) ゲイン・ブロック・アンプです。このデバイスは、パワー・アンプ (PA) の入力を駆動すると同時に、次世代 5G アクティブ・アンテナ・システム (AAS) またはスモール・セル・アプリケーションの要件をサポートできます。この RF アンプは、18dB (標準値) のゲインと +31.5dBm の出力 IP3 という優れた直線性を備えている一方、1dB 帯域幅全体にわたって 4dB 未満のノイズ指数を維持します。このデバイスは、100Ω の差動入力インピーダンスに対して内部的に整合されているため、RF サンプリングまたはゼロ IF アナログ・フロント・エンド (AFE) を簡単に入力に接続できます。またこのデバイスは、ポスト・アンプ、表面弾性波 (SAW) フィルタ、パワー・アンプ (PA) と簡単に接続するために必要な 50Ω のシングルエンド出力インピーダンスに内部的に整合されています。

3.3V の単電源で動作するこのデバイスは、アクティブ消費電力が約 395mW (標準値) であるため、高密度 5G Massive MIMO アプリケーションに適しています。また、このデバイスは省スペースの 2mm × 2mm、12 ピン QFN パッケージで供給されます。このデバイスは最高 105℃の動作温度で定格が規定されているため、堅牢なシステム設計が可能です。時分割複信 (TDD) システムに適した、デバイスの高速な電源オン/オフに利用できる 1.8V JEDEC 準拠のパワー・ダウン・ピンを備えています。

製品情報 (1) (1 ページ)

型番	パッケージ	本体サイズ (公称)
LMH9135	WQFN (12)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



LMH9135：差動→シングルエンド・アンプ

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2020	*	Initial Release

5 Pin Configuration and Functions

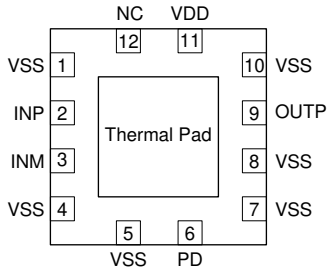


図 5-1. RRL Package 12-Pin WQFN Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VSS	Power	Ground
2	INP	Input	RF differential positive input into amplifier
3	INM	Power	RF differential negative input into amplifier
4	VSS	Power	Ground
5	VSS	Power	Ground
6	PD	Input	Power down connection. PD = 0 V = normal operation; PD = 1.8 V = power off mode
7	VSS	Power	Ground
8	VSS	Output	Ground
9	OUTP	Output	RF single-ended output from amplifier
10	VSS	Power	Ground
11	VDD	Power	Positive supply voltage (3.3 V)
12	NC	—	Do not connect this pin
Thermal Pad		—	Connect the thermal pad to Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	3.6	V
RF Pins	INP, INM, OUTP	–0.3	VDD	V
Digital Input PIN	PD	–0.3	VDD	V
Continuous wave (CW) input	T = 25 °C		18	dBm
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	3.15	3.3	3.45	V
T_C	Case (bottom) temperature	–40		105	°C
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE PKG DES (PKG FAM) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_A = +25°C, VDD = 3.3V, Frequency (f_{in}) = 3.5 GHz, Differential Input Impedance (Z_{IN}) = 100 Ω, Output Load (Z_{LOAD}) = 50 Ω (unless otherwise noted)

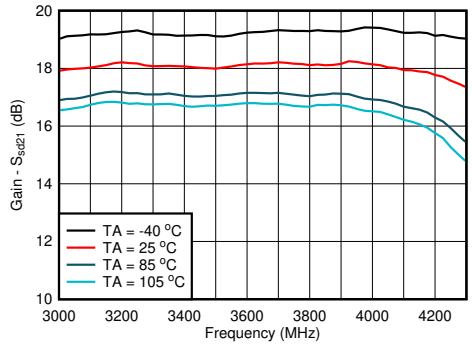
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF PERFORMANCE - LMH9135						
F_{RF}	RF frequency range		3200		4200	MHz
BW_{1dB}	1dB Bandwidth			1000		MHz
S21	Gain			18		dB
NF	Noise Figure	R_S = 100 Ω differential		3.8		dB
OP1dB	Output P1dB	Z_{LOAD} = 50 Ω		18		dBm
OIP3	Output IP3	f_{in} = 3.5 GHz ± 5 MHz Spacing, $P_{OUT/TONE}$ = 2 dBm		31.5		dBm
	Differential Input Gain Imbalance			±0.5		dB
	Differential Input Phase Imbalance			±4		degree
S11	Input return loss (1)	$_{fin}$ = 3.3 - 3.8 GHz		-10		dB
		$_{fin}$ = 3.3 - 4.2 GHz		-10		dB
S22	Output return loss (1)	$_{fin}$ = 3.3 - 3.8 GHz		-10		dB
		$_{fin}$ = 3.3 - 4.2 GHz		-10		dB
S12	Reverse isolation			35		dB
CMRR	Common Mode Rejection Ratio (2)			30		dB
Switching and Digital input characteristics						
t_{ON}	Turn-ON time	50% VPD to 90% RF		0.2		µs
t_{OFF}	Tun-OFF time	50% VPD to 10% RF		0.2		µs
V_{IH}	High-Level Input Voltage	PD pin	1.4			V
V_{IL}	Low-Level Input Voltage	PD pin			0.5	V
DC current and Power Consumption						
I_{VDD_ON}	Supply Current			120		mA
I_{VDD_PD}	Power Down Current			10		mA
P_{dis}	Power Dissipation			395		mW

(1) Reference impedance: Input = 100 Ω differential, Output = 50 Ω single-ended

(2) CMRR is calculated using $(S_{12} - S_{13})/(S_{12} + S_{13})$ for Transmit (1 is output port, 2 & 3 are differential input ports)

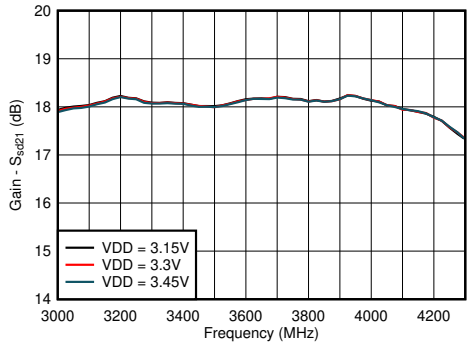
6.6 Typical Characteristics

At T_A = 25°C, VDD = 3.3 V, differential input impedance (Z_{IN}) = 100 Ω, single-ended output impedance (Z_{LOAD}) = 50 Ω (unless otherwise noted).



P_{OUT} = 2 dBm

図 6-1. Gain vs Frequency and Temperature



P_{OUT} = 2 dBm

図 6-2. Gain vs Frequency and Supply Voltage

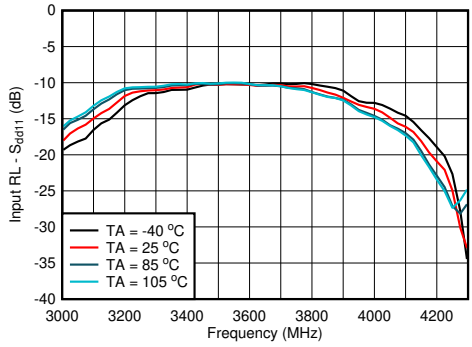


図 6-3. Input Return Loss vs Frequency

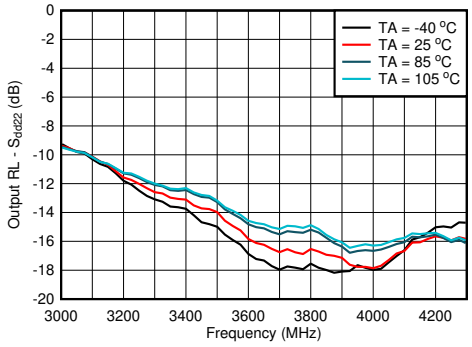


図 6-4. Output Return Loss vs Frequency

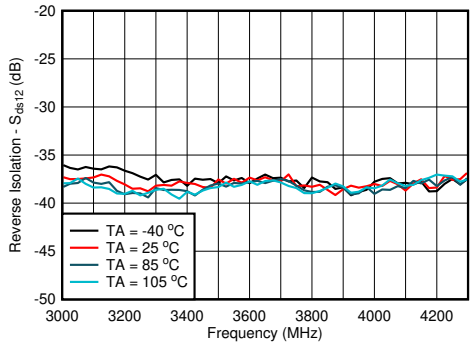
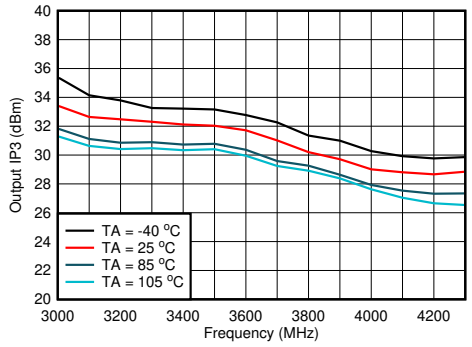
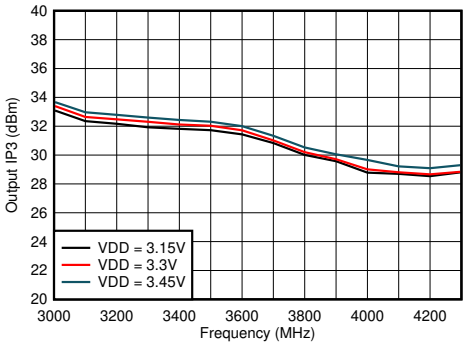


図 6-5. Reverse Isolation vs Frequency



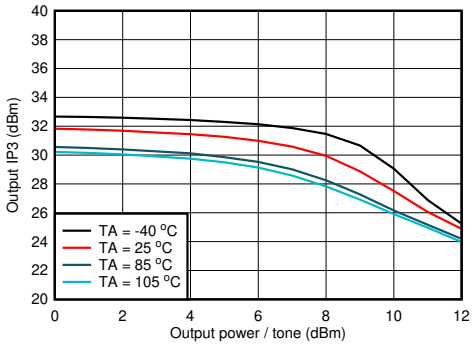
$P_{OUT/TONE}$ = 2 dBm, 10-MHz tone spacing

図 6-6. Output IP3 vs Frequency and Temperature



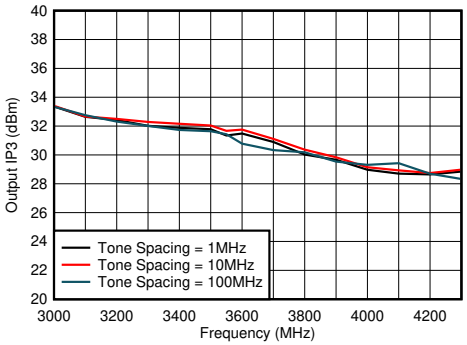
$P_{OUT/TONE}$ = 2 dBm, 10-MHz tone spacing

図 6-7. Output IP3 vs Frequency and Supply Voltage



f = 3.5 GHz, 10-MHz tone spacing

図 6-8. Output IP3 vs Output Power per Tone



$P_{OUT/TONE}$ = 2 dBm

図 6-9. Output IP3 vs Frequency and Tone Spacing

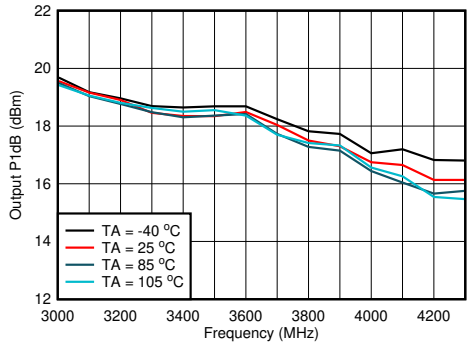


図 6-10. Output P1dB vs Frequency and Temperature

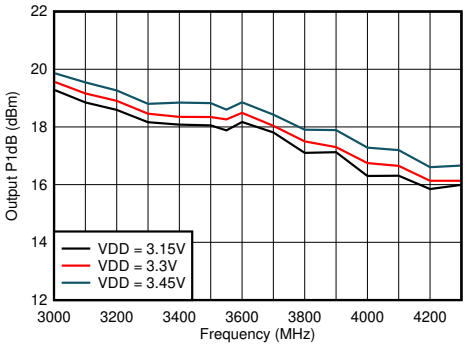
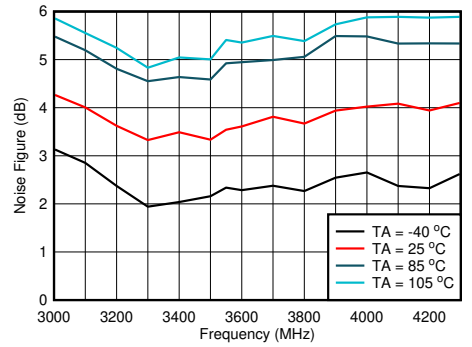


図 6-11. Output P1dB vs Frequency and Supply Voltage



Z_{SOURCE} = 100-Ω differential

図 6-12. Noise Figure vs Frequency and Temperature

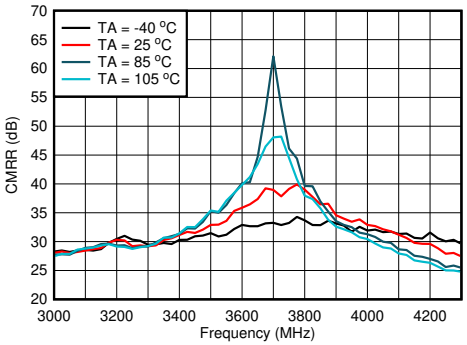


図 6-13. Common-mode Rejection Ratio vs Frequency

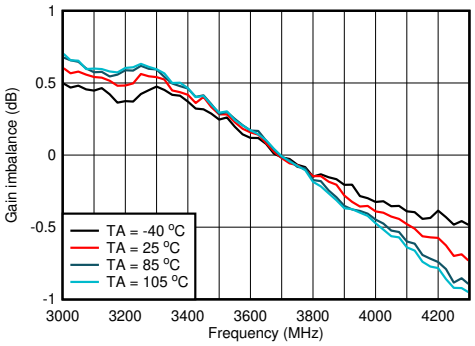


図 6-14. Gain Imbalance vs Frequency and Temperature

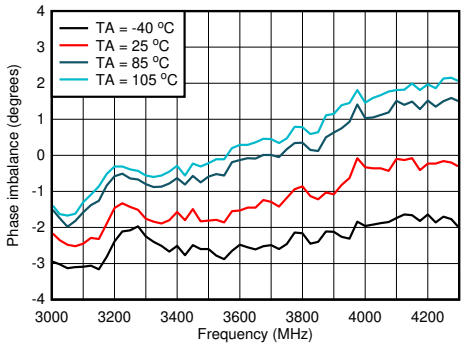


図 6-15. Phase Imbalance vs Frequency and Temperature

7 Detailed Description

7.1 Overview

The LMH9135 device is a differential input to single-ended output narrow-band RF amplifier used in transmitter applications. The device provides 18 dB fixed power gain with excellent linearity and noise performance across the frequency band 3.2 – 4.2 GHz. The device is internally matched for 100-Ω impedance at the differential input and 50-Ω impedance at the single-ended output, as shown in 図 7-1.

LMH9135 have on-chip active bias circuitry to maintain device performance over a wide temperature and supply voltage range. The included power down function allows the amplifier to shut down saving power when the amplifier is not needed. Fast shut down and start up enable the amplifier to be used in a host of time division duplex applications.

Operating on a single 3.3 V supply and 120 mA of typical supply current, the devices are available in a 2 mm x 2 mm 12-pin QFN package.

7.2 Functional Block Diagram

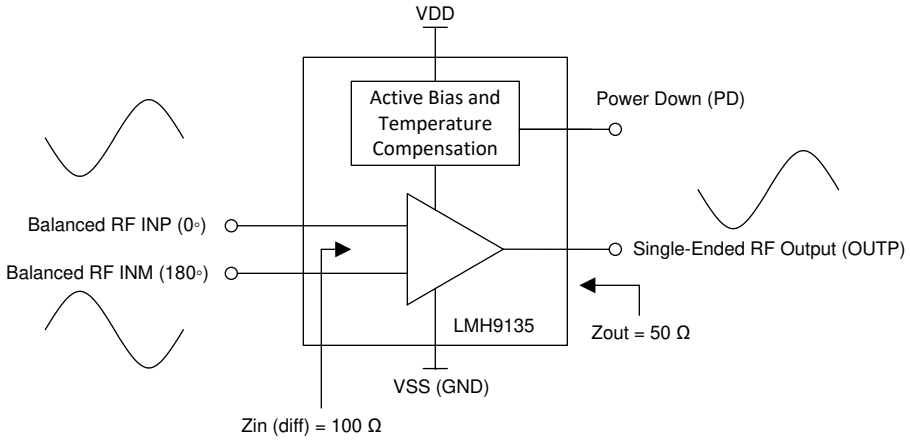


図 7-1. Functional Block Diagram

7.3 Feature Description

The LMH9135 device is a differential input to single-ended output RF amplifier for narrow band active balun implementation. The device integrates the functionality of a single-ended RF amplifier and passive balun in traditional transmitter applications achieving small form factor with comparable linearity and noise performance, as shown in 図 7-2.

The active balun implementation coupled with higher operating temperature of 105°C allows for more robust receiver system implementation compared to passive balun that is prone to reliability failures at high temperatures. The robust operation is achieved by the on-chip active bias circuitry which maintains device performance over a wide temperature and supply voltage range.

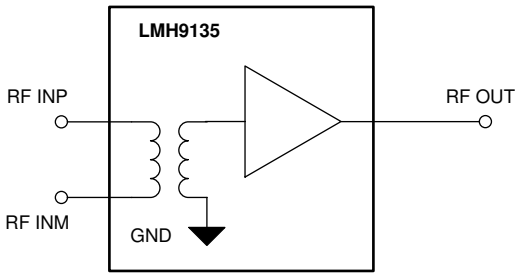


図 7-2. Differential Input to Single-Ended Output, Active Balun Implementation

7.4 Device Functional Modes

LMH9135 features a PD pin which should be connected to GND for normal operation. To power down the device, connect the PD pin to a logic high voltage of 1.8 V.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LMH9135 is a differential to single-ended RF gain block amplifier, which works as an active balun in the transmit path of a 3.3-GHz to 3.8-GHz 5G, TDD m-MIMO or small cell base station. The device replaces the traditional passive balun and single-ended RF amplifier offering a smaller footprint solution to the customer. TI recommends following good RF layout and grounding techniques to maximize the device performance.

8.2 Typical Application

LMH9135 is typically used in a four transmit and four receive (4T/4R) array of active antenna system for 5G, TDD, wireless base station applications. Such a system is shown in 図 8-1, where the LMH9135 is used in the transmit path as an active balun that converts differential DAC output from Tx AFE to single-ended signal. Also shown in the figure is the application of LMH9235 chip, which is the counter-part of LMH9135 in the Receive path.

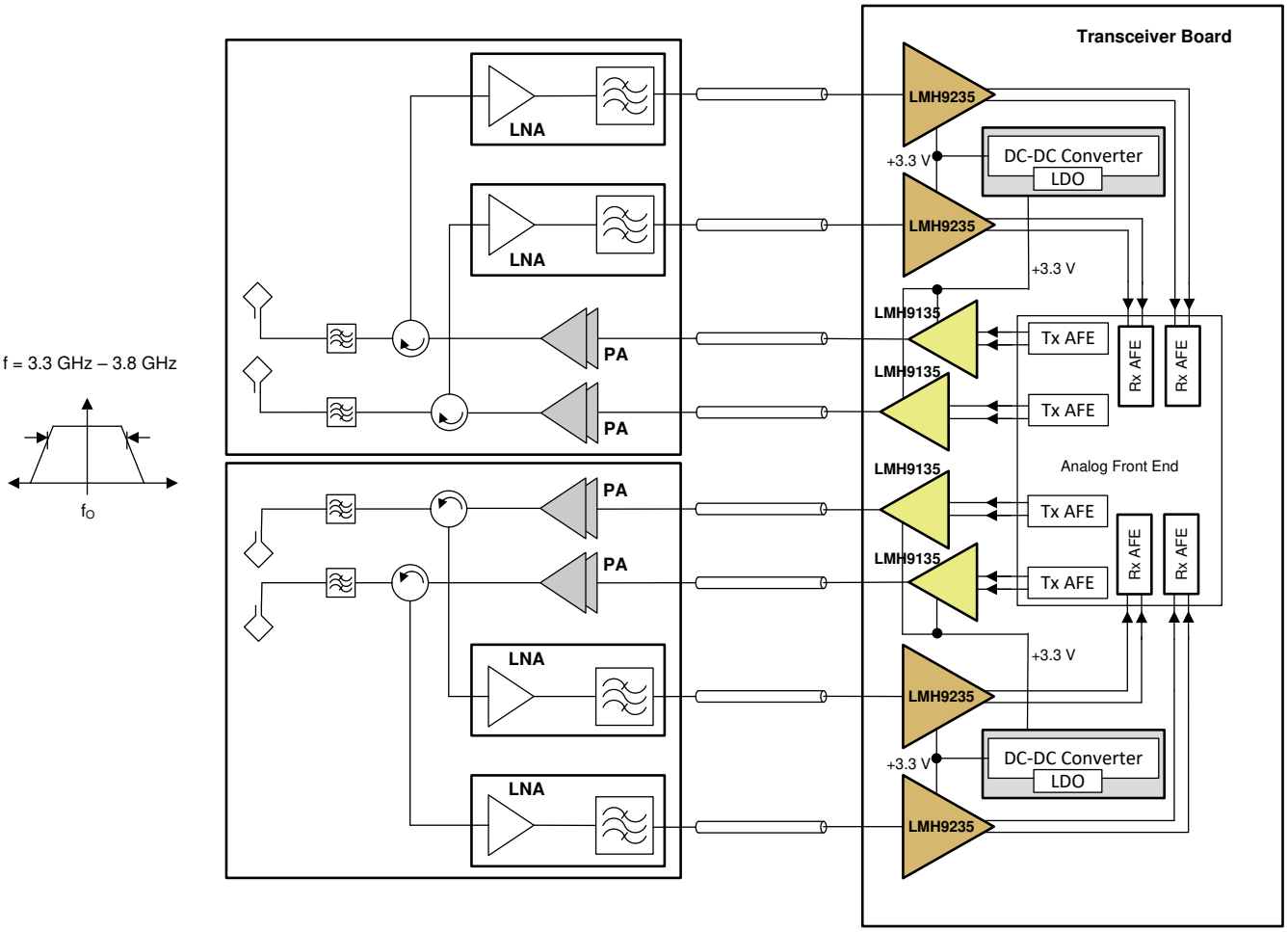


図 8-1. LMH9135 in a 4T/4R 5G Active Antenna System

The 4T/4R system can be scaled to 16T/16R, 64T/64R, or higher antenna arrays that result in proportional scaling of the overall system power dissipation. As a result of the proportional scaling factor for multiple channels in a system, the individual device power consumption must be reduced to dissipate less overall heat in the system. Operating on a single 3.3-V supply, the LMH9135 consumes only about 400 mW and therefore provides power saving to the customer. Multiple LMH9135 devices can be powered from a single DC/DC converter or a low-dropout regulator (LDO) operating on a 3.3-V supply. A DC/DC converter provides the most power efficient way of generating the 3.3-V supply. However, care must be taken when using the DC/DC converter to minimize the switching noise using inductor chokes and adequate isolation must be provided between the analog and digital power domains.

8.2.1 Design Requirements

Input of LMH9135 is matched to 100 Ω and therefore can be directly driven by a DAC that has 100 Ω source impedance without any external matching network. If a DAC with different impedance is used, then it should be appropriately matched to get the best RF performance.

The example in 図 8-2 shows how LMH9135 can be matched to a DAC that has 200-Ω differential termination.

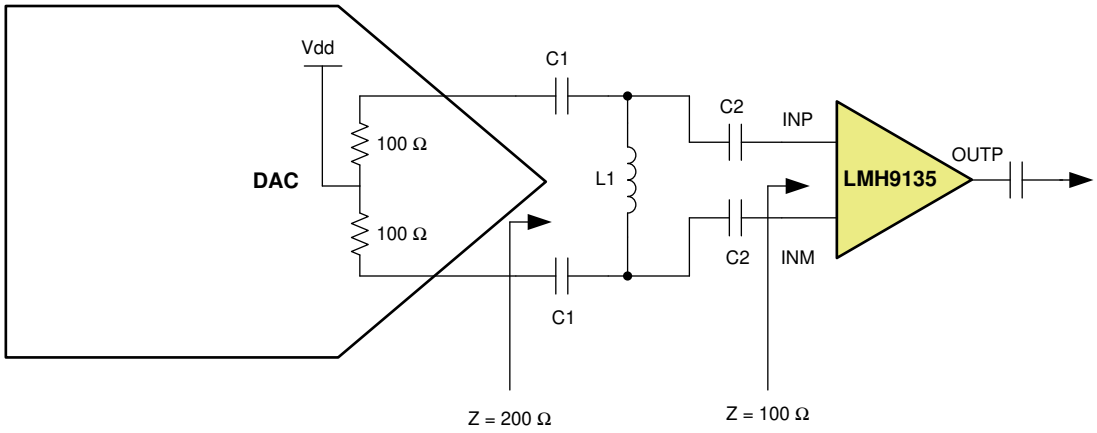


図 8-2. LMH9135 Driven by a DAC with 200-Ω Termination

8.2.2 Detailed Design Procedure

A simple differential LC network is used here as the matching network. In 図 8-2, shunt inductor L1 and series capacitors C2 form the matching network. The series capacitors C1 act as the DC-blocking capacitors. 表 8-1 shows the matching network component values.

表 8-1. Matching Network Component Values for 200-Ω Termination

COMPONENT	VALUE
C1	5.6 pF
L1	6.8 nH
C2	0.8 pF

8.2.3 Application Curves

The graphs given below show the gain, input return loss, and output return loss of the design with different DAC terminations.

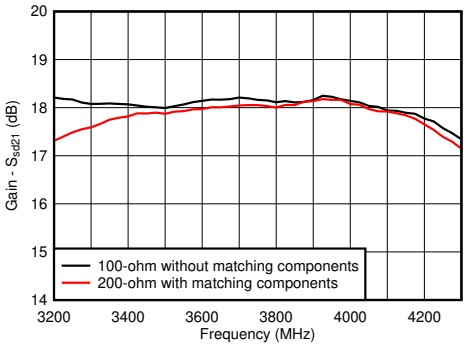


図 8-3. Gain vs Frequency for Different DAC Terminations

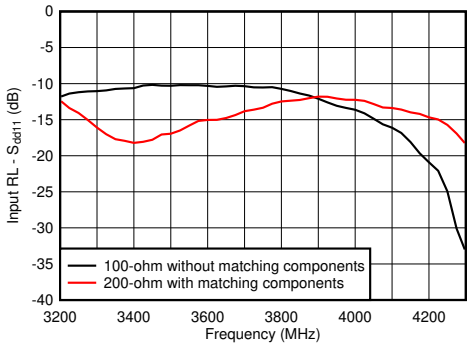


図 8-4. Input Return Loss vs Frequency for Different DAC Terminations

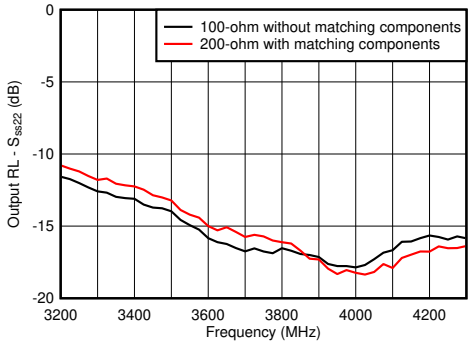


図 8-5. Output Return Loss vs Frequency for Different DAC Terminations

9 Power Supply Recommendations

The LMH9135 device operates on a common nominal 3.3 V supply voltage. It is recommended to isolate the supply voltage through decoupling capacitors placed close to the device. Select capacitors with self resonant frequency above the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.

10 Layout

10.1 Layout Guidelines

When designing with an RF amplifier operating in the frequency range 3 GHz to 4.2 GHz with relatively high gain, certain board layout precautions must be taken to ensure stability and optimum performance. TI recommends that the LMH9135 board be multi-layered to improve thermal performance, grounding, and power-supply decoupling. 図 10-1 shows a good layout example. In this figure, only the top signal layer is shown.

- Excellent electrical connection from the thermal pad to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include a solder mask under the pad.
- Connect the pad ground to the device terminal ground on the top board layer.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Design the two input and one output RF traces for 50-Ω impedance. TI recommends grounded coplanar waveguide (GCPW) type transmission lines for the RF traces. Use a PCB trace width calculator tool to design the transmission lines.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes.
- Place supply decoupling close to the device.
- The differential output traces must be symmetrical in order to achieve the best differential balance and linearity performance.

See the *LMH9135 Evaluation Module* user's guide for more details on board layout and design.

10.2 Layout Example

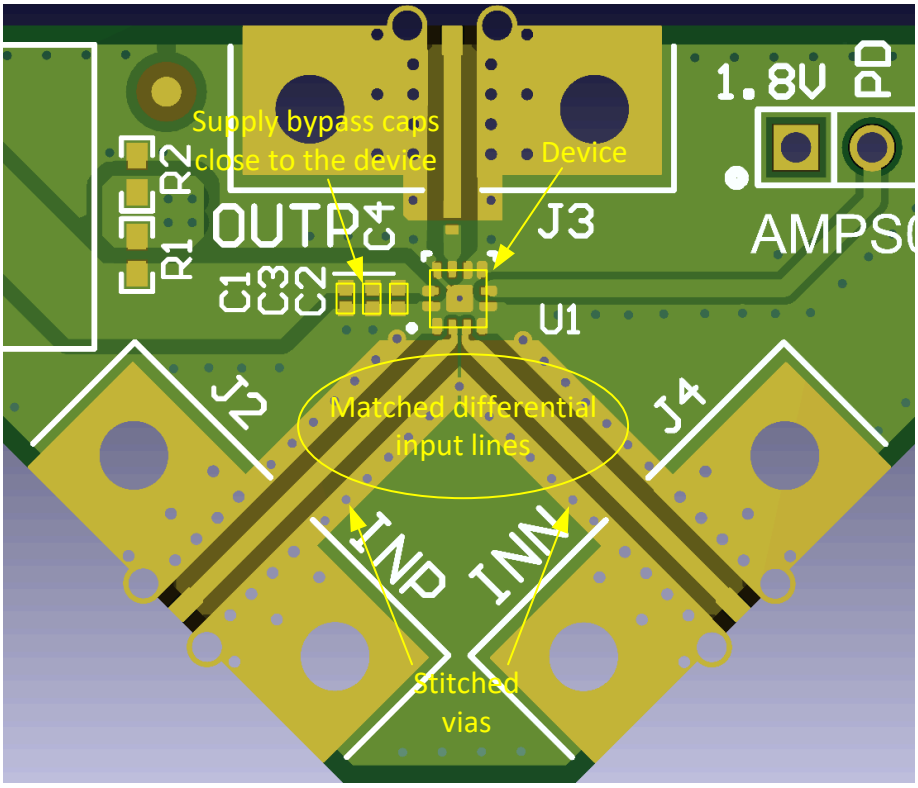


図 10-1. Layout Showing Matched Differential Traces and Supply Decoupling

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, LMH9135 Evaluation Module User's Guide
- Texas Instruments, LMH9135 S-parameter Models
- Texas Instruments, LMH9135RRLEVM EU Declaration of Conformity (DoC)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH9135IRRLR	Active	Production	WQFN (RRL) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	35AO
LMH9135IRRLR.B	Active	Production	WQFN (RRL) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	35AO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

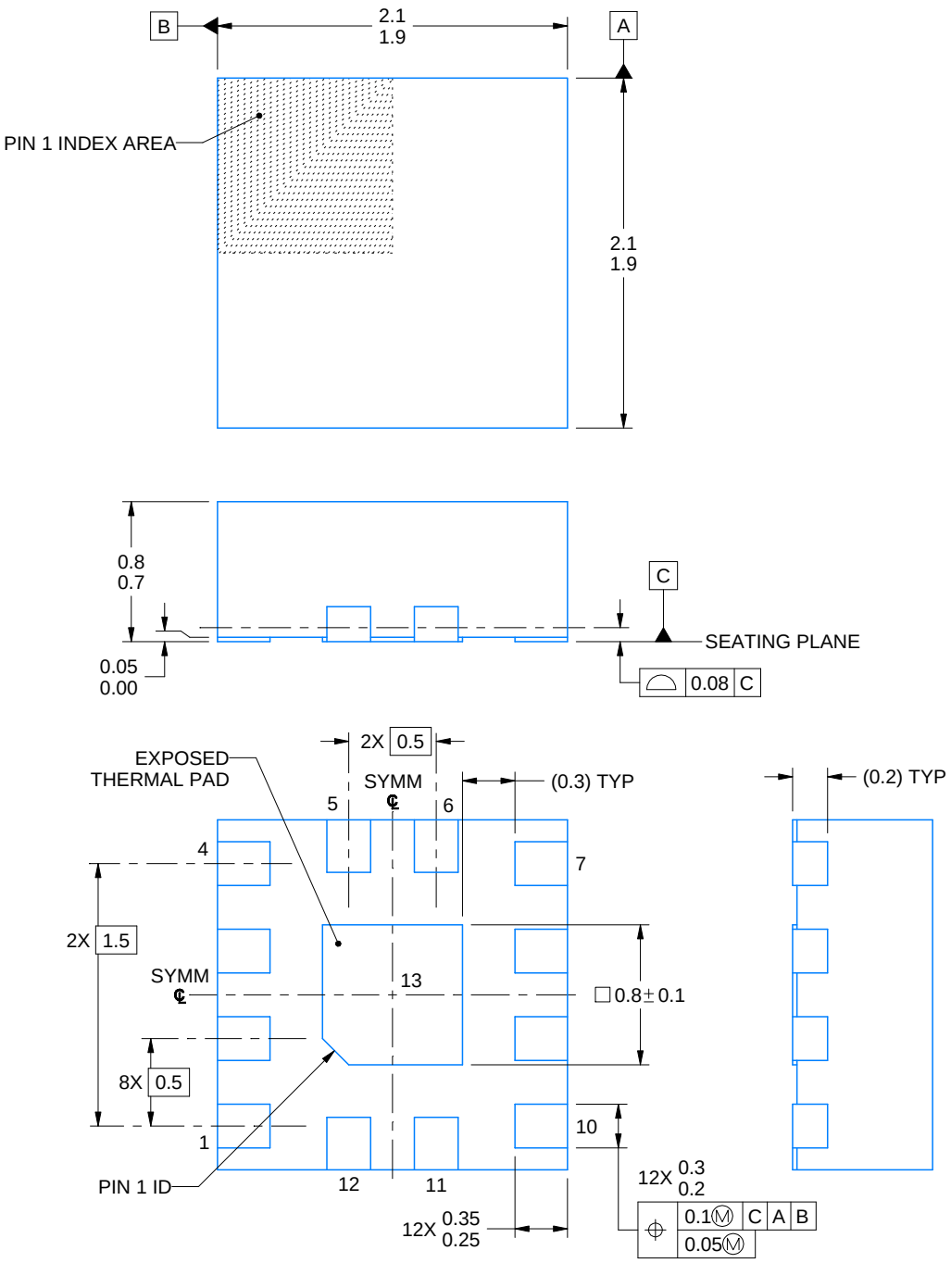
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

RRL0012A

PACKAGE OUTLINE

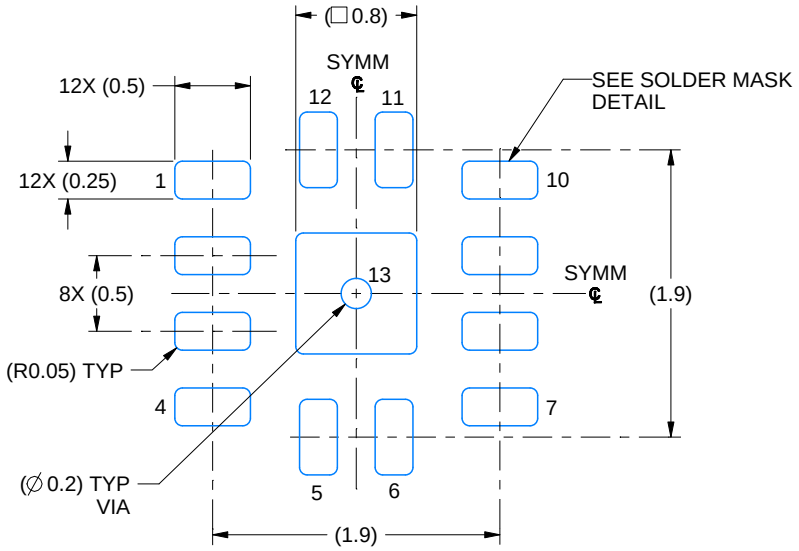
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

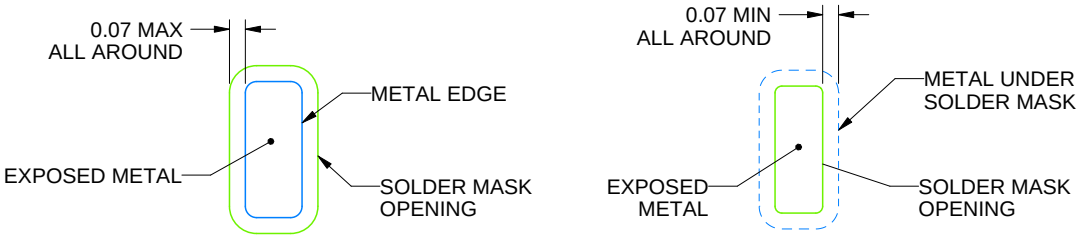


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

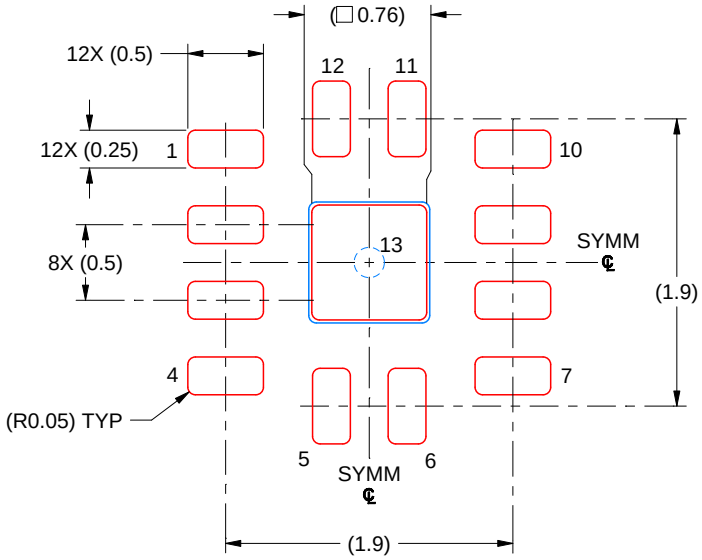
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224942/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224942/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265