



LMH6574 4:1高速ビデオ・マルチプレクサ

1 特長

- 500MHz、500mV -3dB帯域幅、 $A_V = 2$
- 400MHz、2V_{PP} -3dB帯域幅、 $A_V = 2$
- チャンルのスイッチング時間: 8ns
- 10MHzにおいてチャンネル間分離70dB
- 0.02%、0.05°の差動ゲイン、位相
- ゲイン・フラットネス: 150MHzまで0.1dB
- スルー・レート: 2200V/μs
- 広い電源電圧範囲: 6V (±3V)~12V (±6V)
- 5MHzにおいて-68dB HD2
- 5MHzにおいて-84dB HD3

2 アプリケーション

- ビデオ・ルータ
- 複数の入力ビデオ・モニタ
- 計装/テスト機器
- 受信機のIFダイバーシティ・スイッチ
- マルチチャンネルA/Dドライバ
- ピクチャー・イン・ピクチャーのビデオ・スイッチ

3 概要

LMH6574は高性能のアナログ・マルチプレクサで、プロフェッショナル・グレードのビデオや、他の高忠実度、高帯域幅のアナログ・アプリケーション用に最適化されています。出力アンプは、2つのアドレス・ビットの状態に基づき、4つのバッファ付き入力信号のどれでも選択できます。LMH6574は、2V_{PP}の出力信号レベルで400MHzの帯域幅を提供します。150MHzの0.1dB帯域幅と2200V/μsのスルー・レートを特長とするLMH6574は、マルチメディアおよび高精細テレビ(HDTV)アプリケーションに最適です。

LMH6574は、コンポジット・ビデオ・アプリケーションをサポートし、NTSCおよびPALビデオ信号で0.02%および0.05°の差動ゲイン誤差と位相誤差を実現し、単一のバック終端の75Ω負荷を駆動します。80mAのリニア出力電流によって複数のビデオ負荷アプリケーションを駆動できます。

LMH6574のゲインは外付けのフィードバックおよびゲイン設定抵抗により設定されるため、最大の柔軟性が得られます。

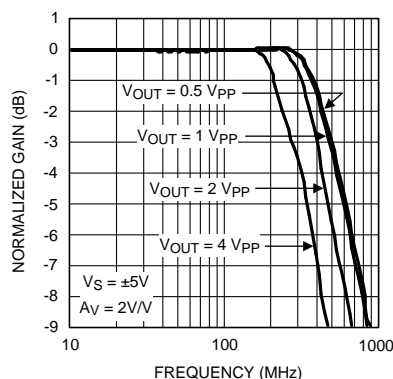
LMH6574は14ピンのSOICパッケージで供給されます。

製品情報⁽¹⁾

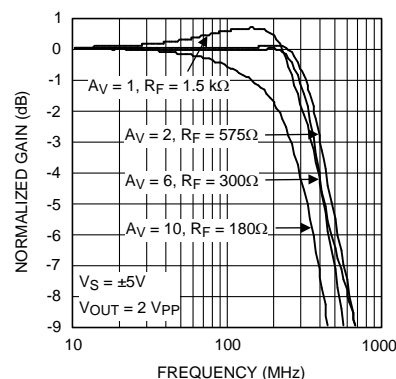
| 型番 | パッケージ | 本体サイズ(公称) |
|---------|-----------|---------------|
| LMH6574 | SOIC (14) | 8.65mm×3.91mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

周波数応答とV_{OUT}との関係



周波数応答とゲインとの関係



目次

| | | | | | |
|-----|--|----|------|---|----|
| 1 | 特長 | 1 | 7.3 | Device Functional Modes..... | 16 |
| 2 | アプリケーション | 1 | 8 | Application and Implementation | 17 |
| 3 | 概要 | 1 | 8.1 | Application Information..... | 17 |
| 4 | 改訂履歴..... | 2 | 9 | Power Supply Recommendations | 21 |
| 5 | Pin Configuration and Functions | 3 | 9.1 | Power Dissipation | 21 |
| 6 | Specifications | 4 | 10 | Layout | 21 |
| 6.1 | Absolute Maximum Ratings | 4 | 10.1 | Layout Guidelines | 21 |
| 6.2 | ESD Ratings..... | 4 | 11 | デバイスおよびドキュメントのサポート | 22 |
| 6.3 | Recommended Operating Conditions..... | 4 | 11.1 | ドキュメントのサポート | 22 |
| 6.4 | Thermal Information | 4 | 11.2 | ドキュメントの更新通知を受け取る方法..... | 22 |
| 6.5 | Electrical Characteristics ± 5 V | 5 | 11.3 | コミュニティ・リソース | 22 |
| 6.6 | Electrical Characteristics ± 3.3 V | 7 | 11.4 | 商標 | 22 |
| 6.7 | Typical Characteristics | 8 | 11.5 | 静電気放電に関する注意事項 | 22 |
| 7 | Detailed Description | 13 | 11.6 | Glossary | 22 |
| 7.1 | Functional Block Diagram | 13 | 12 | メカニカル、パッケージ、および注文情報 | 22 |
| 7.2 | Feature Description..... | 13 | | | |

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (December 2014) から Revision E に変更

Page

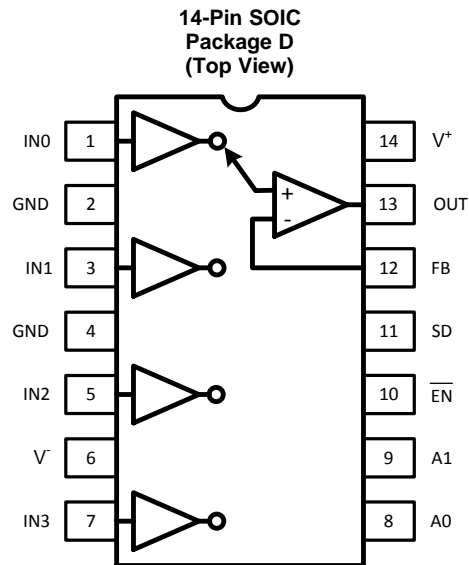
| | | |
|---|--|----|
| • | Changed IBN parameter maximum specifications from $\pm 5 \mu\text{A}$ to $\pm 5.2 \mu\text{A}$ and from $\pm 5.6 \mu\text{A}$ to $\pm 5.8 \mu\text{A}$ | 5 |
| • | Changed PSRR parameter minimum specifications from 47 dB to 43 dB and from 45 dB to 41 dB | 5 |
| • | Changed <i>Supply Current Disabled</i> parameter maximum specifications from 5.8 mA to 6.2 mA and from 5.9 mA to 6.3 mA | 6 |
| • | Changed I _{IL} parameter minimum specifications from $-2.9 \mu\text{A}$ to $-3.3 \mu\text{A}$ and from $-8.5 \mu\text{A}$ to $-9 \mu\text{A}$ | 6 |
| • | Added <i>Feature Description</i> and <i>Device Functional Modes</i> sections | 13 |

Revision C (November 2012) から Revision D に変更

Page

| | | |
|---|---|----|
| • | 次のセクションを追加、更新、または修正: 「ピン構成と機能」、「仕様」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」..... | 1 |
| • | Revised text in <i>Application and Implementation</i> section, formerly titled "Application Notes" | 17 |
| • | Revised text in <i>Multiplexer Expansion</i> section. Added Figure 31 , Figure 32 , and Figure 33 | 17 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------------------------|-----|-----------------------|
| NO. | NAME | | |
| 1 | IN0 | I | Input Channel 0 |
| 2 | GND | — | Ground |
| 3 | IN1 | I | Input Channel 1 |
| 4 | GND | — | Ground |
| 5 | IN2 | I | Input Channel 2 |
| 6 | V ⁻ | I | V ⁻ Supply |
| 7 | IN3 | I | Input Channel 3 |
| 8 | A0 | I | Select Pin A0 |
| 9 | A1 | I | Select Pin A1 |
| 10 | $\overline{\text{EN}}$ | I | Enable |
| 11 | SD | I | Shutdown |
| 12 | FB | I | Feedback |
| 13 | OUT | O | Output |
| 14 | V ⁺ | I | V ⁺ Supply |

Truth Table

| A1 | A0 | $\overline{\text{EN}}$ | SD | OUT |
|----|----|------------------------|----|----------|
| 1 | 1 | 0 | 0 | CH 3 |
| 1 | 0 | 0 | 0 | CH2 |
| 0 | 1 | 0 | 0 | CH1 |
| 0 | 0 | 0 | 0 | CH 0 |
| X | X | 1 | 0 | Disable |
| X | X | X | 1 | Shutdown |

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | MIN | MAX | UNIT |
|----------------------------------|-----|----------------|------|
| Supply Voltage ($V^+ - V^-$) | | 13.2 | V |
| $I_{OUT}^{(3)}$ | | 130 | mA |
| Signal & Logic Input Pin Voltage | | $\pm(V_S+0.6)$ | V |
| Signal & Logic Input Pin Current | | ± 20 | mA |
| Maximum Junction Temperature | | +150 | °C |
| Storage Temperature | -65 | +150 | °C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics \$\pm 5\$ V](#) tables
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the [Power Dissipation](#) for more details. A short circuit condition should be limited to 5 seconds or less.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--|---|------------|------|
| $V_{(ESD)}$ Electrostatic discharge ⁽¹⁾ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾ | ± 2000 | V |
| | Machine model (MM) | ± 200 | |

- (1) Human Body model, 1.5 k Ω in series with 100 pF. Machine model, 0 Ω in series with 200 pF.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ± 200 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | NOM | MAX | UNIT |
|-----------------------|-----|-----|-----|------|
| Operating Temperature | -40 | | 85 | °C |
| Supply Voltage | 6 | | 12 | V |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics \$\pm 5\$ V](#) tables

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D | UNIT |
|-------------------------------|---|---------|------|
| | | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 130 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 40 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics ± 5 V

$V_S = \pm 5$ V, $R_L = 100 \Omega$, $A_V = 2$ V/V, $R_F = 575 \Omega$, $T_J = 25^\circ\text{C}$, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|---|--|---------------|---------------|------------------------------|
| FREQUENCY DOMAIN PERFORMANCE | | | | | | |
| SSBW | –3 dB Bandwidth | $V_{OUT} = 0.5 V_{PP}$ | | 500 | | MHz |
| LSBW | –3 dB Bandwidth | $V_{OUT} = 2 V_{PP}$ | | 400 | | MHz |
| .1 dBBW | 0.1 dB Bandwidth | $V_{OUT} = 0.25 V_{PP}$ | | 150 | | MHz |
| DG | Differential Gain | $R_L = 150 \Omega$, $f = 4.43$ MHz | | 0.02% | | |
| DP | Differential Phase | $R_L = 150 \Omega$, $f = 4.43$ MHz | | 0.05 | | deg |
| XTLK | Channel to Channel Crosstalk | All Hostile, 5 MHz | | –85 | | dB |
| TIME DOMAIN RESPONSE | | | | | | |
| TRS | Channel to Channel Switching Time | Logic Transition to 90% Output | | 8 | | ns |
| | Enable and Disable Times | Logic Transition to 90% or 10% Output | | 10 | | ns |
| TRL | Rise and Fall Time | 4-V Step | | 2.4 | | ns |
| TSS | Settling Time to 0.05% | 2-V Step | | 17 | | ns |
| OS | Overshoot | 2-V Step | | 5% | | |
| SR | Slew Rate | 4-V Step | | 2200 | | V/ μ s |
| DISTORTION | | | | | | |
| HD2 | 2 nd Harmonic Distortion | 2 V_{PP} , 5 MHz | | –68 | | dBc |
| HD3 | 3 rd Harmonic Distortion | 2 V_{PP} , 5 MHz | | –84 | | dBc |
| IMD | 3 rd Order Intermodulation Products | 10 MHz, Two Tones 2 V_{PP} at Output | | –80 | | dBc |
| EQUIVALENT INPUT NOISE | | | | | | |
| VN | Voltage | >1 MHz, Input Referred | | 5 | | nV/ $\sqrt{\text{Hz}}$ |
| ICN | Current | >1 MHz, Input Referred | | 5 | | pA/ $\sqrt{\text{Hz}}$ |
| STATIC, DC PERFORMANCE | | | | | | |
| CHGM | Channel to Channel Gain Difference | DC, Difference in Gain Between Channels | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | $\pm 0.005\%$ | $\pm 0.032\%$ | |
| VIO | Input Offset Voltage ⁽²⁾ | $V_{IN} = 0$ V | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | 1 | ± 20 | mV |
| DVIO | Offset Voltage Drift | | | 30 | | $\mu\text{V}/^\circ\text{C}$ |
| IBN | Input Bias Current ⁽²⁾⁽³⁾ | $V_{IN} = 0$ V | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | –3 | ± 5.2 | μA |
| DIBN | Bias Current Drift | | | 11 | | nA/ $^\circ\text{C}$ |
| | Inverting Input Bias Current | Pin 12, Feedback Point, $V_{IN} = 0$ V | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | –7 | ± 10 | |
| PSRR | Power Supply Rejection Ratio ⁽²⁾ | DC, Input Referred | | 43 | 54 | dB |
| | | | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | 41 | | |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See [Application and Implementation](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
- (2) Parameters guaranteed by electrical testing at 25°C .
- (3) Positive Value is current into device.

LMH6574

JAJ5FX7E – NOVEMBER 2004 – REVISED AUGUST 2018

www.ti.com
Electrical Characteristics ± 5 V (continued)
 $V_S = \pm 5$ V, $R_L = 100\ \Omega$, $A_V = 2$ V/V, $R_F = 575\ \Omega$, $T_J = 25\ ^\circ\text{C}$, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|---------------------------|---|--|-------------------------------|-------|------|------|------|
| ICC | Supply Current ⁽²⁾ | No Load | | | 13 | 16 | mA |
| | | | -40°C ≤ T _J ≤ 85°C | | | 18 | |
| | Supply Current Disabled ⁽²⁾ | $\overline{\text{ENABLE}} > 2 \text{ V}$ | | | 4.7 | 6.2 | mA |
| | | | -40°C ≤ T _J ≤ 85°C | | | 6.3 | |
| | Supply Current Shutdown | SHUTDOWN > 2 V | | | 1.8 | 2.5 | mA |
| | | | -40°C ≤ T _J ≤ 85°C | | | 2.6 | |
| VIH | Logic High Threshold ⁽²⁾ | Select & Enable Pins (SD & $\overline{\text{EN}}$) | | 2.0 | | | V |
| VIL | Logic Low Threshold ⁽²⁾ | Select & Enable Pins (SD & $\overline{\text{EN}}$) | | | | 0.8 | V |
| II _L | Logic Pin Input Current Low ⁽³⁾ | Logic Input = 0 V Select & Enable Pins (SD & $\overline{\text{EN}}$) | | -3.3 | -1 | | μA |
| | | | -40°C ≤ T _J ≤ 85°C | -9 | | | |
| II _H | Logic Pin Input Current High ⁽³⁾ | Logic Input = 2.0 V, Select & Enable Pins (SD & $\overline{\text{EN}}$) | | | 47 | 68 | μA |
| | | | -40°C ≤ T _J ≤ 85°C | | | 72.5 | |
| MISCELLANEOUS PERFORMANCE | | | | | | | |
| RIN+ | Input Resistance | | | | 5 | | kΩ |
| CIN | Input Capacitance | | | | 0.8 | | pF |
| ROUT | Output Resistance | Output Active, ($\overline{\text{EN}}$ and SD < 0.8 V) | | | 0.04 | | Ω |
| ROUT | Output Resistance | Output Disabled, ($\overline{\text{EN}}$ or SD > 2 V) | | | 3000 | | Ω |
| COUT | Output Capacitance | Output Disabled, ($\overline{\text{EN}}$ or SD > 2 V) | | | 3.1 | | pF |
| VO | Output Voltage Range | No Load | | ±3.54 | ±3.7 | | V |
| | | | -40°C ≤ T _J ≤ 85°C | ±3.53 | | | |
| VOL | Output Voltage Range | R _L = 100 Ω | | ±3.18 | ±3.5 | | V |
| | | | -40°C ≤ T _J ≤ 85°C | ±3.17 | | | |
| CMIR | Input Voltage Range | | | ±2.5 | ±2.6 | | V |
| IO | Linear Output Current ⁽²⁾⁽³⁾ | V _{IN} = 0 V | | +60 | | | mA |
| | | | | -70 | | | |
| | | | -40°C ≤ T _J ≤ 85°C | +50 | ±80 | | |
| | | | -40°C ≤ T _J ≤ 85°C | -60 | | | |
| ISC | Short Circuit Current ⁽⁴⁾ | V _{IN} = ±2 V, Output Shorted to Ground | | | ±230 | | mA |

(4) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the [Power Dissipation](#) for more details. A short circuit condition should be limited to 5 seconds or less.

6.6 Electrical Characteristics ± 3.3 V

$V_S = \pm 3.3$ V, $R_L = 100\ \Omega$, $A_V = 2$ V/V, $R_F = 575\ \Omega$; unless otherwise specified.

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|-------------------------------------|-------------------------------------|--|-----|-----------|-----|------------|
| FREQUENCY DOMAIN PERFORMANCE | | | | | | |
| SSBW | –3 dB Bandwidth | $V_{OUT} = 0.5\ V_{PP}$ | | 475 | | MHz |
| LSBW | –3 dB Bandwidth | $V_{OUT} = 2.0\ V_{PP}$ | | 375 | | MHz |
| 0.1 dBBW | 0.1 dB Bandwidth | $V_{OUT} = 0.5\ V_{PP}$ | | 100 | | MHz |
| GFP | Peaking | DC to 200 MHz | | 0.4 | | dB |
| XTLK | Channel to Channel Crosstalk | All Hostile, $f = 5$ MHz | | –85 | | dBc |
| TIME DOMAIN RESPONSE | | | | | | |
| TRL | Rise and Fall Time | 2-V Step | | 2 | | ns |
| TSS | Settling Time to 0.05% | 2-V Step | | 20 | | ns |
| OS | Overshoot | 2-V Step | | 5% | | |
| SR | Slew Rate | 2-V Step | | 1400 | | V/ μ s |
| DISTORTION | | | | | | |
| HD2 | 2 nd Harmonic Distortion | $2\ V_{PP}$, 10 MHz | | –67 | | dBc |
| HD3 | 3 rd Harmonic Distortion | $2\ V_{PP}$, 10 MHz | | –87 | | dBc |
| STATIC, DC PERFORMANCE | | | | | | |
| VIO | Input Offset Voltage | $V_{IN} = 0$ V | | –5 | | mV |
| IBN | Input Bias Current ⁽²⁾ | $V_{IN} = 0$ V | | –3 | | μ A |
| PSRR | Power Supply Rejection Ratio | DC, Input Referred | | 49 | | dB |
| ICC | Supply Current | No Load | | 12 | | mA |
| VIH | Logic High Threshold | Select & Enable Pins (SD & \overline{EN}) | 1.3 | | | V |
| VIL | Logic Low Threshold | Select & Enable Pins (SD & \overline{EN}) | | | 0.4 | V |
| MISCELLANEOUS PERFORMANCE | | | | | | |
| RIN+ | Input Resistance | | | 5 | | k Ω |
| CIN | Input Capacitance | | | 0.8 | | pF |
| ROUT | Output Resistance | | | 0.06 | | Ω |
| VO | Output Voltage Range | No Load | | ± 2 | | V |
| VOL | | $R_L = 100\ \Omega$ | | ± 1.8 | | V |
| CMIR | Input Voltage Range | | | ± 1.2 | | V |
| IO | Linear Output Current | $V_{IN} = 0$ V | | ± 60 | | mA |
| ISC | Short Circuit Current | $V_{IN} = \pm 1$ V, Output Shorted to Ground | | ± 150 | | mA |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See [Application and Implementation](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

6.7 Typical Characteristics

$V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $A_V = 2$, $R_F = R_G = 575\ \Omega$, unless otherwise specified.

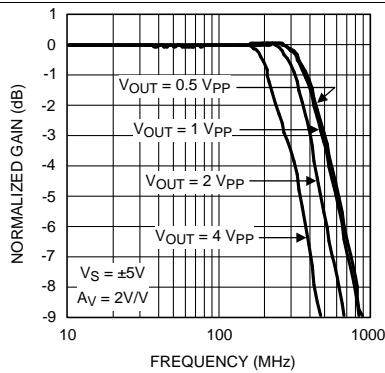


Figure 1. Frequency Response vs V_{OUT}

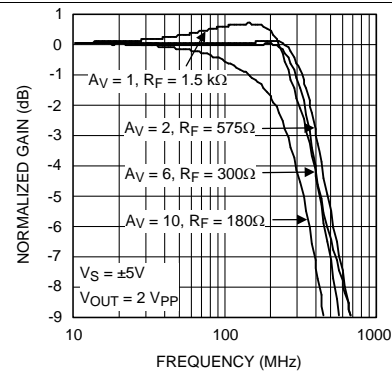


Figure 2. Frequency Response vs Gain

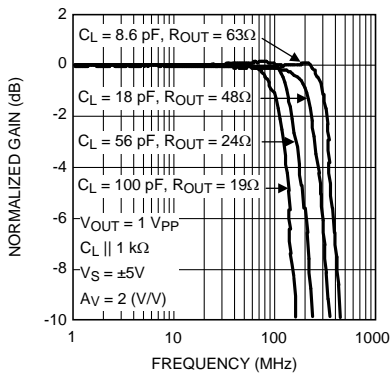


Figure 3. Frequency Response vs Capacitive Load

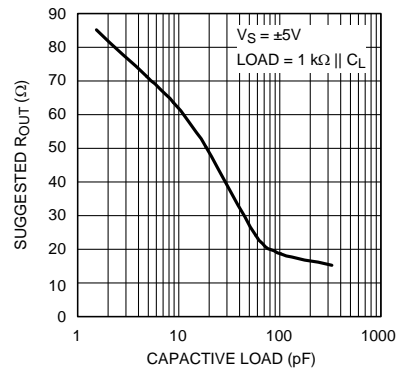


Figure 4. Suggested R_{OUT} vs Capacitive Load

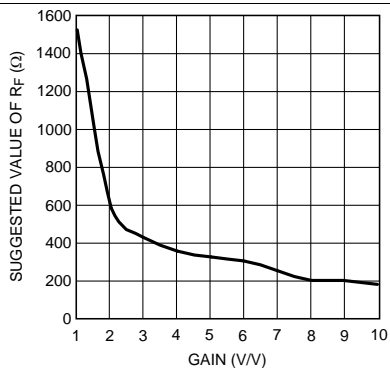


Figure 5. Suggested Value of R_F vs Gain

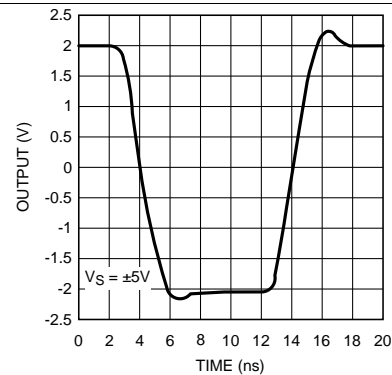


Figure 6. Pulse Response $4V_{PP}$

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $A_V = 2$, $R_F = R_G = 575\ \Omega$, unless otherwise specified.

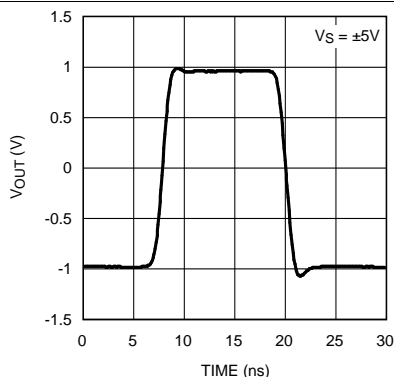


Figure 7. Pulse Response 2V_{pp}

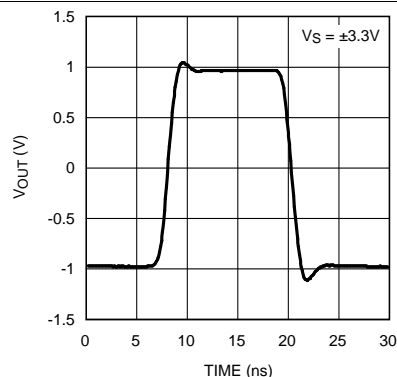


Figure 8. Pulse Response 2V_{pp}

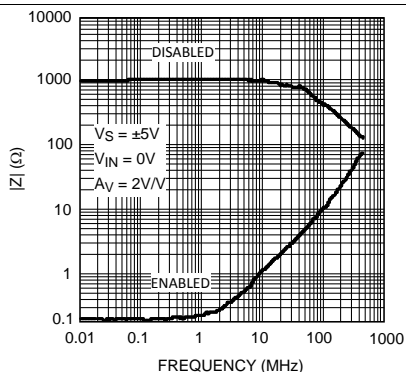


Figure 9. Closed Loop Output Impedance

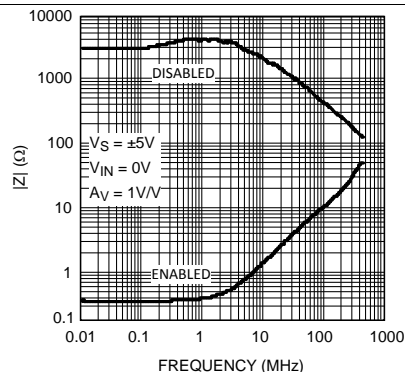


Figure 10. Closed Loop Output Impedance

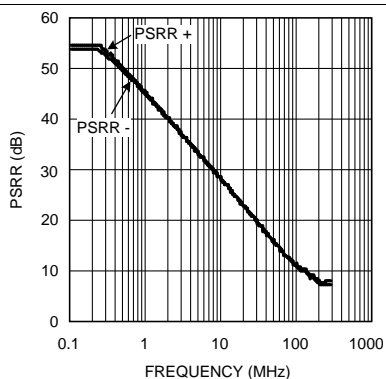


Figure 11. PSRR vs Frequency

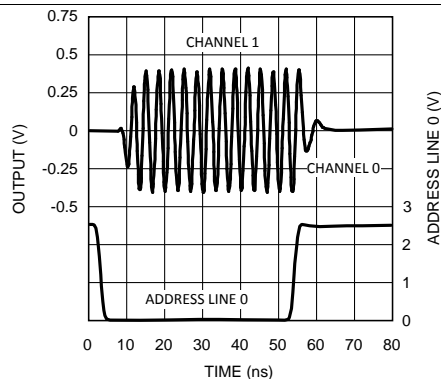


Figure 12. Channel Switching

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $A_V = 2$, $R_F = R_G = 575\ \Omega$, unless otherwise specified.

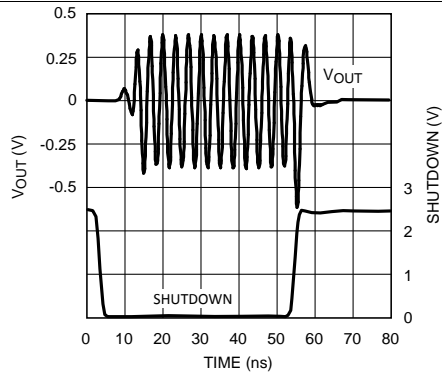


Figure 13. SHUTDOWN Switching

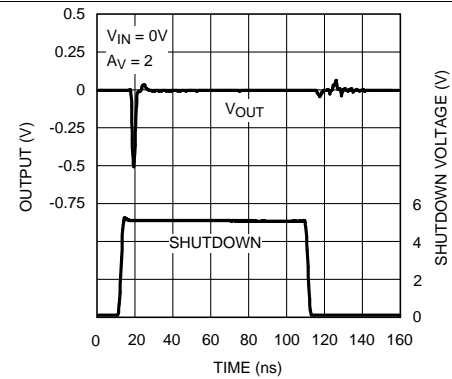


Figure 14. Shutdown Glitch

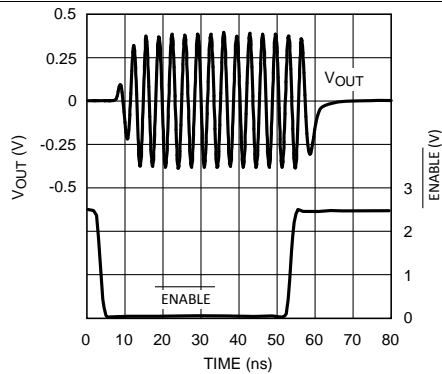


Figure 15. $\overline{\text{ENABLE}}$ Switching

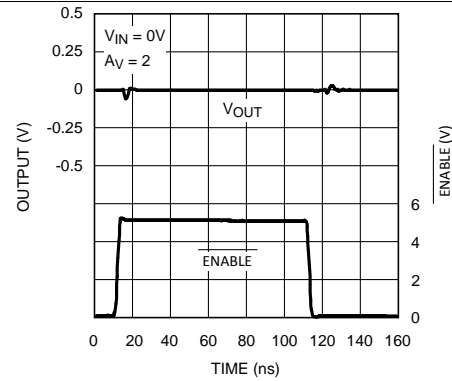


Figure 16. Disable Glitch

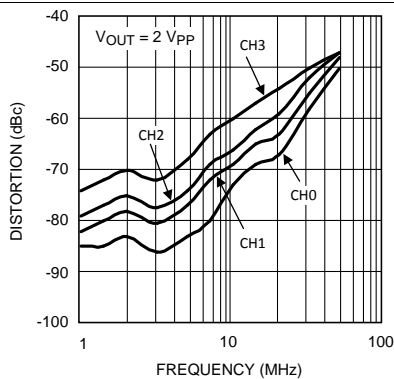


Figure 17. HD2 vs Frequency

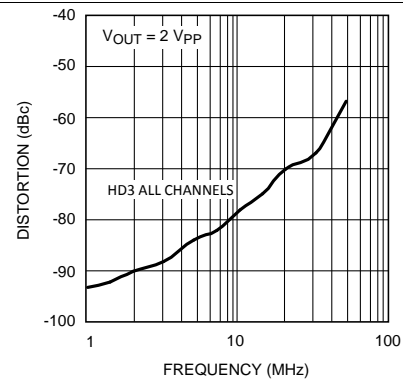


Figure 18. HD3 vs Frequency

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $A_V = 2$, $R_F = R_G = 575\ \Omega$, unless otherwise specified.

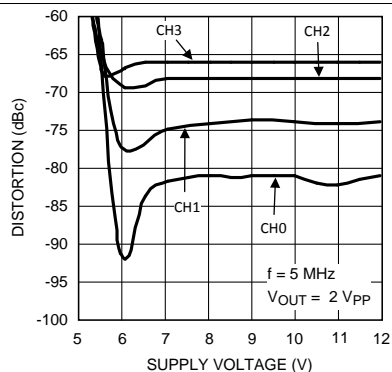


Figure 19. HD2 vs V_S

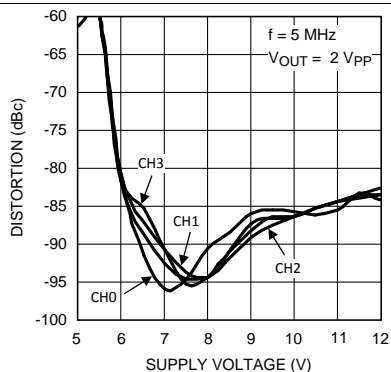


Figure 20. HD3 vs V_S

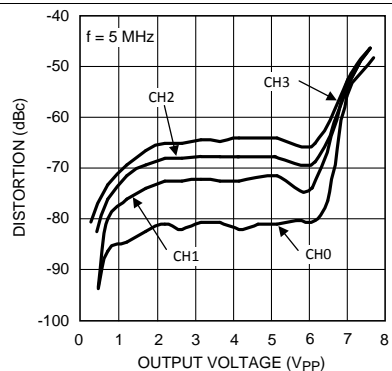


Figure 21. HD2 vs V_{OUT}

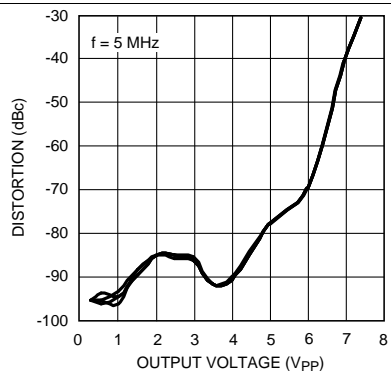
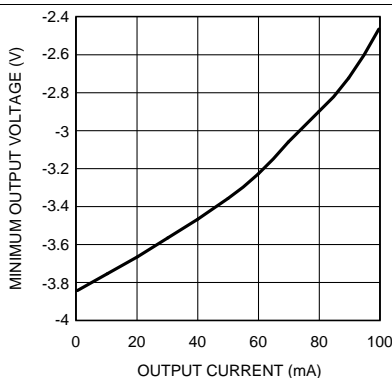
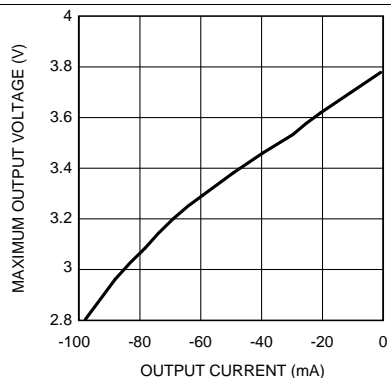


Figure 22. HD3 vs V_{OUT}



Positive Value is current into device

Figure 23. Minimum V_{OUT} vs I_{OUT}



Positive Value is current into device

Figure 24. Maximum V_{OUT} vs I_{OUT}

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $A_V = 2$, $R_F = R_G = 575\ \Omega$, unless otherwise specified.

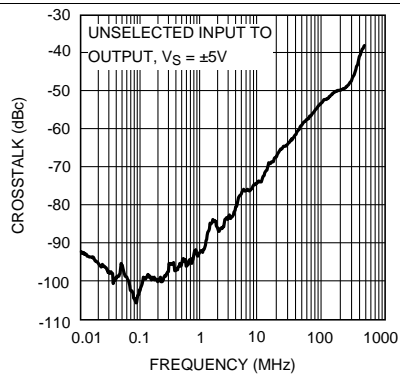


Figure 25. Crosstalk vs Frequency

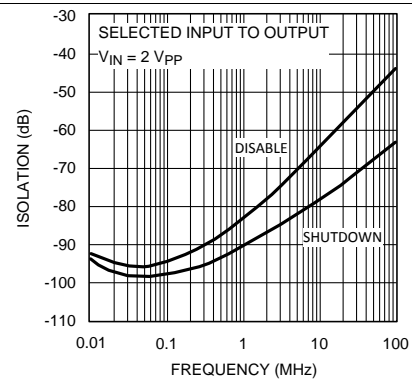
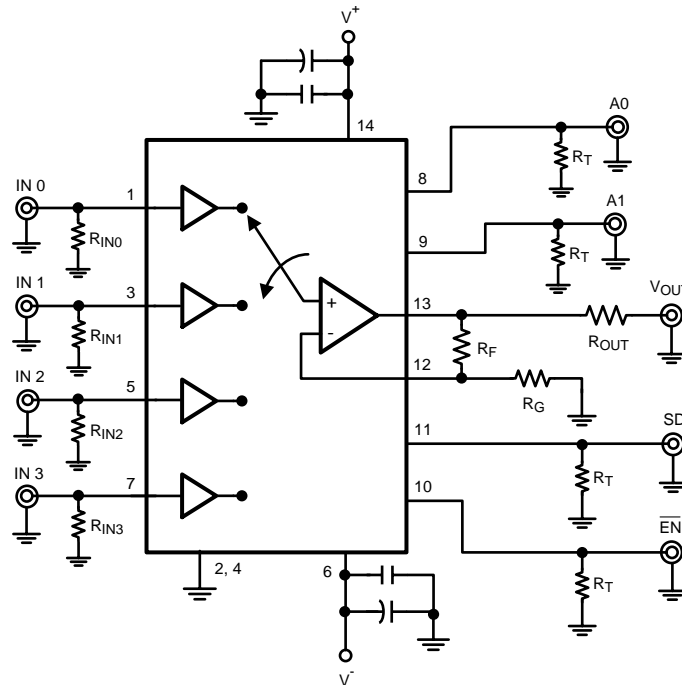


Figure 26. Off Isolation

7 Detailed Description

7.1 Functional Block Diagram



7.2 Feature Description

7.2.1 Video Performance

The LMH6574 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks other parasitic capacitances from the amplifier output stage. The [Functional Block Diagram](#) shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

7.2.2 Feedback Resistor Selection

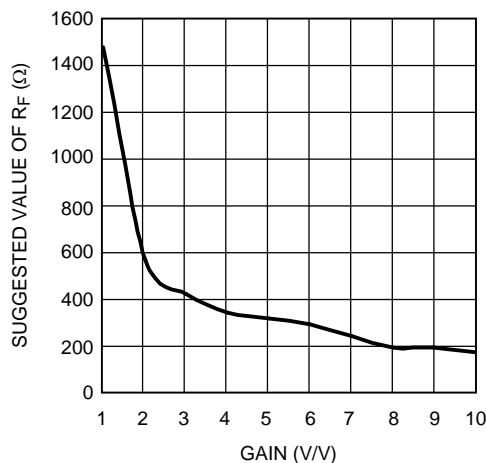


Figure 27. Suggested R_F vs Gain

Feature Description (continued)

The LMH6574 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F . For a gain of 2 V/V, the recommended value of R_F is 575 Ω . For other gains see [Figure 27](#). Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 ([SNOA366](#)), which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 12 is approximately 20 Ω . This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6574 will exhibit a “gain bandwidth product” similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 ([SNOSA39](#)) to provide additional gain.

7.2.3 Other Applications

The LMH6574 could support a multi antenna receiver with up to four separate antennas. Monitoring the signal strength of all 4 antennas and connecting the strongest signal to the final IF stage would provide effective spacial diversity.

For direction finding, the LMH6574 could be used to provide high speed sampling of four separate antennas to a single DSP which would use the information to calculate the direction of the received signal.

Feature Description (continued)

7.2.4 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT} . Figure 28 shows the use of a series output resistor, R_{OUT} , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 29 provides a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

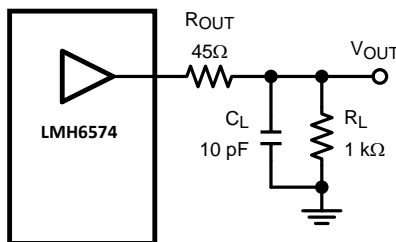


Figure 28. Decoupling Capacitive Loads

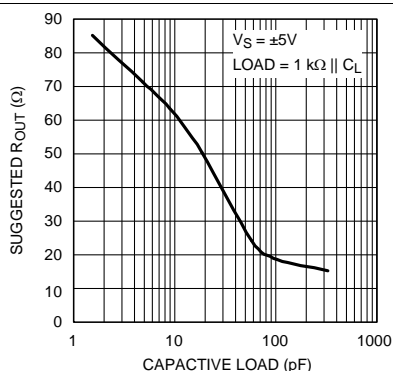


Figure 29. Suggested R_{OUT} vs Capacitive Load

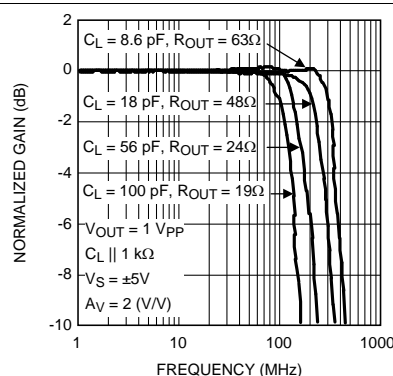


Figure 30. Frequency Response vs Capacitive Load

7.2.5 ESD Protection

The LMH6574 is protected against electrostatic discharge (ESD) on all pins. The LMH6574 will survive 2000-V Human Body model and 200-V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6574 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

7.3 Device Functional Modes

7.3.1 SD vs $\overline{\text{EN}}$

The LMH6574 has both shutdown and disable capability. The shutdown feature affects the entire chip, whereas the disable function only affects the output buffer. When in shutdown mode, minimal power is consumed. The shutdown function is very fast, but causes a very brief spike of about 400 mV to appear on the output. When in shutdown mode the LMH6574 consumes only 1.8 mA of supply current. For maximum input to output isolation use the shutdown function.

The $\overline{\text{EN}}$ pin only disables the output buffer which results in a substantially reduced output glitch of only 50 mV. While disabled the chip consumes 4.7 mA, considerably more than when shutdown. This is because the input buffers are still active. For minimal output glitch use the $\overline{\text{EN}}$ pin. Also, care should be taken to ensure that, while in the disabled state, the voltage differential between the active input buffer (the one selected by pins A0 and A1) and the output pin stays less than 2V. As the voltage differential increases, input to output isolation decreases. Normally this is not an issue. See [Multiplexer Expansion](#) for further details.

To reduce the output glitch when using the SD pin, switch the $\overline{\text{EN}}$ pin at least 10 ns before switching the SD pin. This can be accomplished by using an RC delay circuit between the two pins if only one control signal is available.

Logic inputs "SD" and " $\overline{\text{EN}}$ " will revert to the "High", while "A₀" and "A₁" will revert to the "Low" state when left floating.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH6574 is a high-speed 4:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6574 is ideally suited for switching high resolution, presentation grade video signals. The LMH6574 has no internal ground reference. Single or split supply configurations are both possible. The LMH6574 features very high speed channel switching and disable times. When disabled the LMH6574 output is high impedance making MUX expansion possible by combining multiple devices. See [Multiplexer Expansion](#).

8.1.1 Multiplexer Expansion

It is possible to use multiple LMH6574 devices to expand the number of inputs that can be selected for output. [Figure 31](#) shows an 8:1 MUX using two LMH6574 devices.

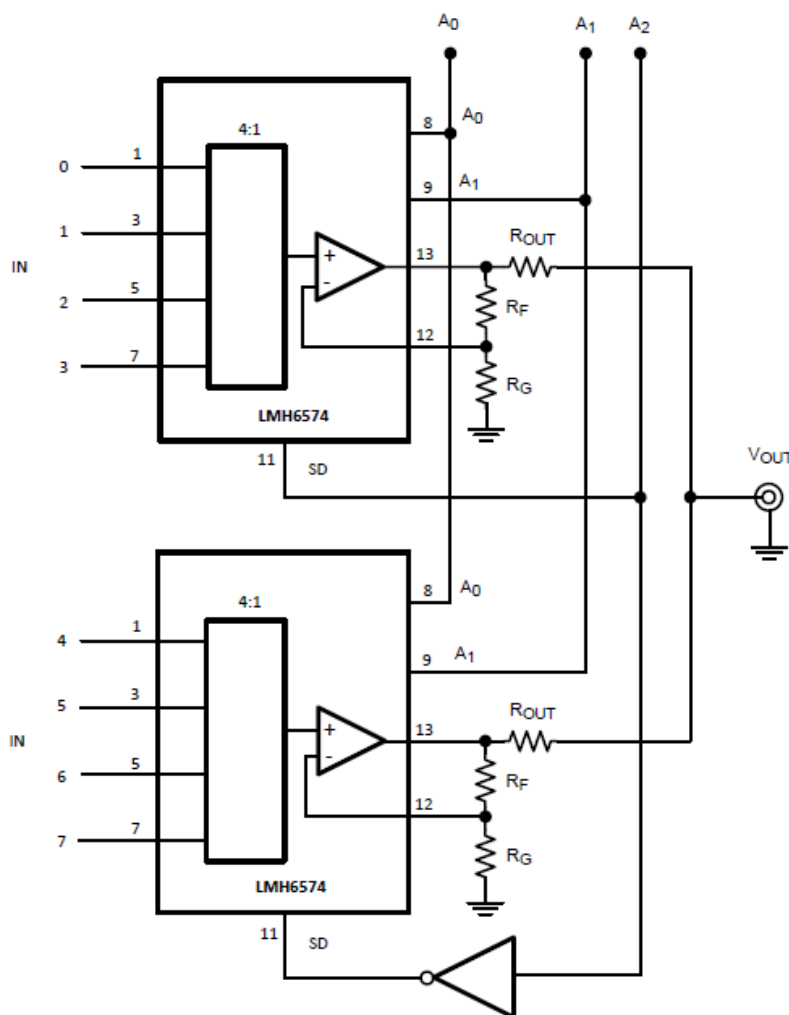


Figure 31. 8:1 MUX Using Two LMH6574 Devices

Application Information (continued)

In such an application, the output settling may be longer than the LMH6574 switching specifications (~20ns), while switching between two separate LMH6574 devices. The switching time limiting factor occurs when one LMH6574 is turned off and another one is turned on, using the SD (shutdown) pin. The output settling time consists of the time needed for the first LMH6574 to enter high impedance state plus the time required for the second LMH6574 output to dissipate the left-over output charge of the first device (limited by the output current capability of the second device) and the time needed to settle to the final voltage value.

While [Figure 31](#) MUX expansion benefits from more isolation, originating from the parasitic loading of the unselected channels on the selected channel, afforded by individual R_{OUT} on each multiplexer output, this configuration does not produce the fastest transition between individual LMH6574 devices. For the fastest transition, the configuration of [Figure 32](#) can be used where the LMH6574 output pins are all shorted together.

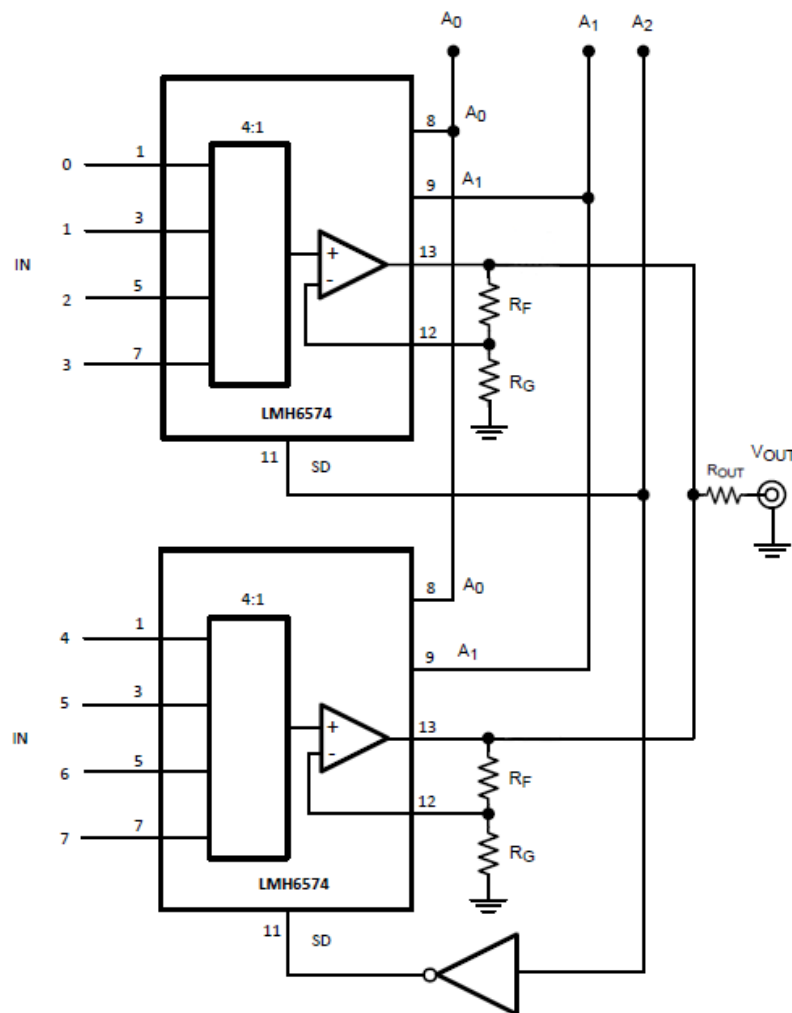


Figure 32. Alternate 8:1 MUX Expansion Schematic (for Faster SD Switching)

Application Information (continued)

Figure 33 shows typical transition waveforms and shows that SD pin switching settles in less than 145 ns.

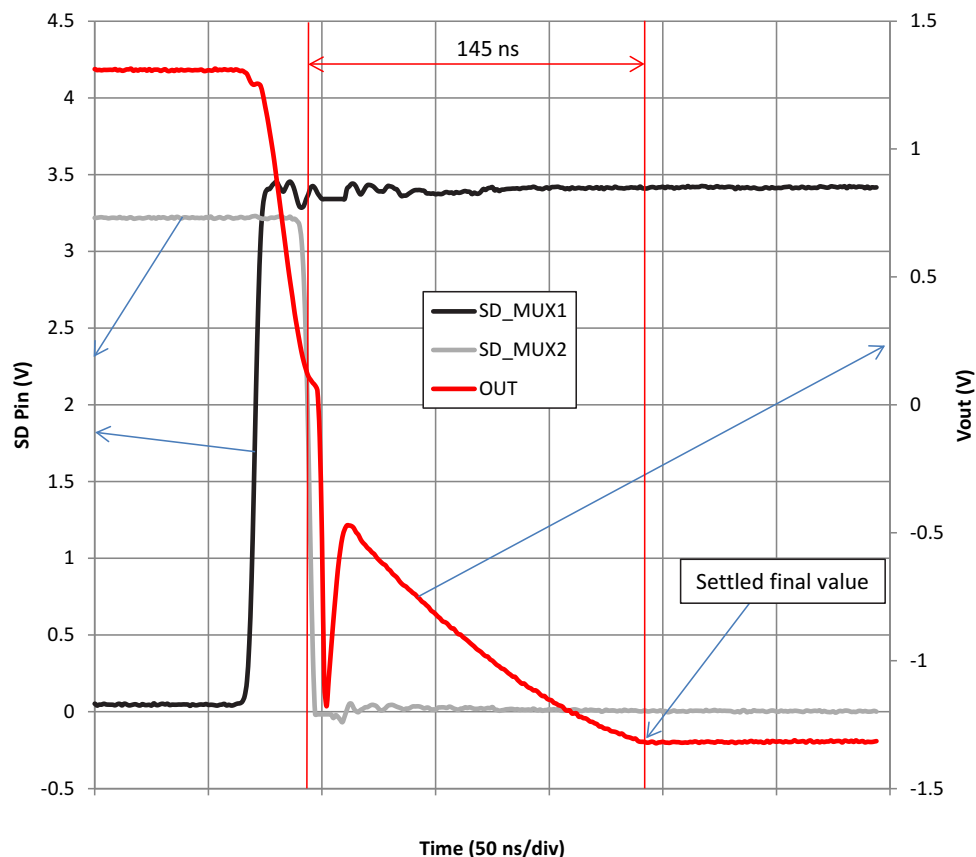


Figure 33. SD Pin Switching Waveform and Output Settling

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. Figure 34 shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions (R_1 and C_1 decay) but will not delay its L to H transition. R_2 should be kept small compared to R_1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

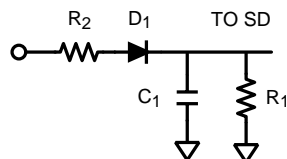


Figure 34. Delay Circuit Implementation

Application Information (continued)

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6574's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 35 shows how to compensate for this effect. For the 16:1 MUX function shown in Figure 35, the gain error would be about -0.8 dB, or about 9%. In the circuit in Figure 35, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

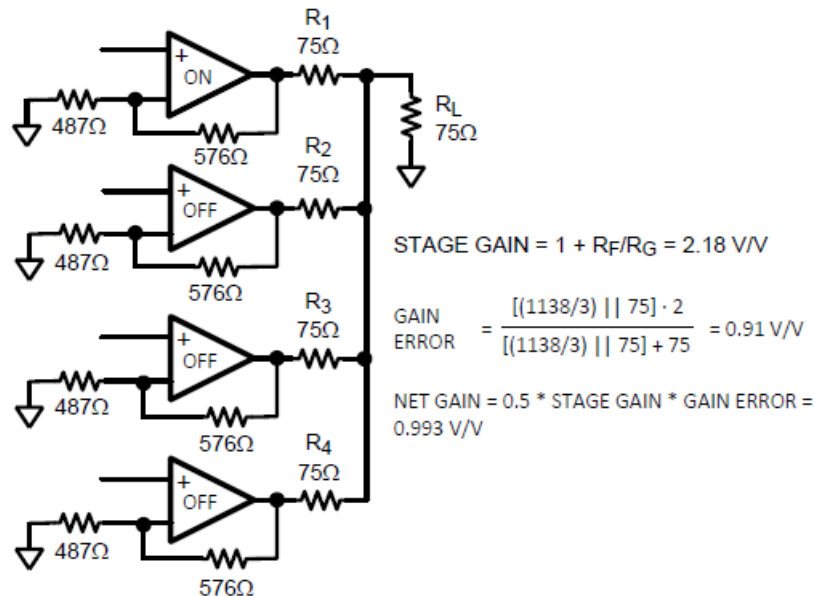


Figure 35. Multiplexer Gain Compensation

NOTE

Disabling of the LMH6574 using the EN pin is not recommended for use when doing multiplexer expansion. While disabled, if the voltage between the selected input and the chip output exceeds approximately 2V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

9 Power Supply Recommendations

9.1 Power Dissipation

The LMH6574 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6574:

1. Calculate the quiescent (no-load) power.

$$P_{AMP} = I_{CC} * (V_S)$$

where

- $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (rms) = rms ((V_S - V_{OUT}) * I_{OUT})$$

where

- V_{OUT} is the voltage across the external load
- I_{OUT} is the current through the external load
- V_S is the total supply voltage (2)

3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6574 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^\circ - T_{AMB})/R_{\theta JA}$$

where

- T_{AMB} = Ambient temperature ($^\circ\text{C}$)
- $R_{\theta JA}$ = Thermal resistance, from junction to ambient, for a given package ($^\circ\text{C/W}$) (3)

For the SOIC package $R_{\theta JA}$ is 130 $^\circ\text{C/W}$.

10 Layout

10.1 Layout Guidelines

Whenever questions about layout arise, use the evaluation board [LMH730276](#) as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In the [Functional Block Diagram](#), the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

詳細情報については、以下を参照してください。

- 『電流フィードバック・ループのゲイン分析と性能向上』アプリケーション・ノートOA-13
- 『ICパッケージの熱指標』アプリケーション・レポート
- 『LMH730276 4:1マルチプレクサ評価ボード』

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LMH6574MA/NOPB | Active | Production | SOIC (D) 14 | 55 TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LMH65 74MA |
| LMH6574MA/NOPB.A | Active | Production | SOIC (D) 14 | 55 TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LMH65 74MA |
| LMH6574MAX/NOPB | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LMH65 74MA |
| LMH6574MAX/NOPB.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LMH65 74MA |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH6574MAX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH6574MAX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LMH6574MA/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LMH6574MA/NOPB.A | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated