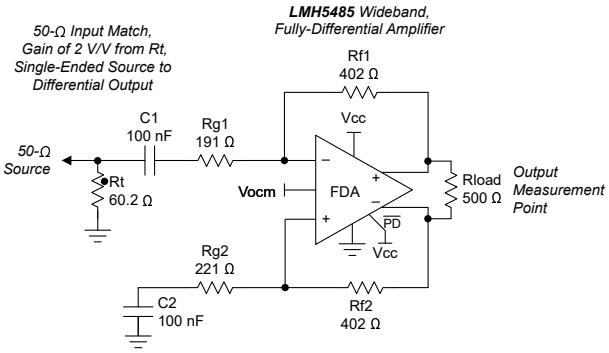
LMH5485-SP 放射線 Hardened 耐性保証 (RHA)、負レール入力、レール・ツー・レール出力、高精度、850MHz 完全差動アンプ

1 特長

- QMLV (QML Class V) MIL-PRF-38535 認定済み、SMD 5962R1920401VXC
  - 吸収線量 (TID) 100krad (Si) までの放射線耐性保証 (RHA)
  - 単一イベント・ラッチアップ (SEL) 耐性: LET = 85MeV-cm2/mg
  - 軍用温度範囲全体で認定: –55℃～125℃
- 完全差動アンプ (FDA) アーキテクチャ
- 帯域幅: 490MHz (G = 2V/V)
- ゲイン帯域幅積 (GBWP): 850MHz
- スルーレート: 1400V/µs
- HD2、HD3: -79dBc、-97dBc (10MHz、$2V_{PP}$)
- 入力電圧ノイズ: 2.4nV/√Hz (f > 100kHz)
- 入力オフセット電圧、ドリフト: ±100µV、±0.5µV/℃
- 負レール入力 (NRI)、レール・ツー・レール出力 (RRO)
- 出力同相モード制御
- 電源:
  - 電源電圧範囲: 2.7V～5.1V
  - 静止時電流: 10.1mA (5V 電源)
  - パワーダウン機能: 2µA (標準値)

2 アプリケーション

- 低消費電力、高性能の ADC ドライバ:
  - SAR、ΔΣ、パイプライン
- 差動 DAC 出力ドライバ
- コマンドとデータの処理
- 自動車起動システム
- 宇宙用画像処理システム:
  - 光学画像処理のペイロード
  - レーダー画像処理ペイロード
  - 熱画像処理カメラ



概略回路図

3 概要

LMH5485-SP は、負レールよりも低い入力同相範囲とレール・ツー・レール出力を備え、放射線をした低消費電力、電圧帰還、完全差動アンプ (FDA) です。高性能 A/D コンバータ (ADC) または D/A コンバータ (DAC) インターフェイス設計の高密度化が非常に重要な、電力の制約が厳しいデータ・アクイジション・システム向けに設計されています。

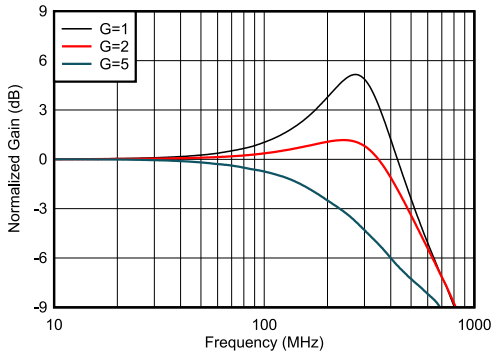
LMH5485-SP は、DC 結合、グランド中心の信号源と接続する際に必要な負レール入力を備えています。この負レール入力とレール・ツー・レール出力を使うことで、シングルエンド、グランド・リファレンスのバイポーラ信号源と各種 ADC (逐次比較レジスタ (SAR)、デルタ・シグマ (ΔΣ)、パイプライン) を 2.7V～5.1V の単一電源を使って簡単に接続できます。LMH5485-SP また、このような ADC 駆動アプリケーションに適した非常に優れた DC 精度も備えており、–55℃～+125℃の広い温度範囲で動作が規定されています。

製品情報

部品番号(1)	グレード	パッケージ
5962R1920401VXC	放射線耐性保証 (RHA)	セラミック CFP HKX (8) 6.5mm × 6.5mm
5962-1920401VXC	QMLV	
LMH5485HKX/EM	エンジニアリング・サンプル(2)	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

(2) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフローに従って処理されています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。部品は、MIL に規定されている温度範囲全体 (–55℃～125℃) にわたる性能も動作寿命全体にわたる性能も保証されていません。



シングルから差動までのゲイン：2、100mV_{PP} 出力

ADVANCE INFORMATION

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2021) to Revision A (December 2021)	Page
• Added clarifying text to note 1 in Pin Functions table	3
• Changed 0.9 V to 0.91 V in second paragraph of *セクション 9.1* section	17
• Changed 0.9 V to 0.91 V in first paragraph of *セクション 9.4.1.1* section	21

5 Device Comparison Table

DEVICE	RAD TOLERANCE	GBWP (MHz)	I_Q (mA)	HD2 / HD3 (dBc) 2 V_{PP} AT 10 MHz	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL
LMH5485-SP	100 kRad TID	850	10.1	–79 / –97	2.4	NRI/Out
LMH5485-SEP	30 kRad TID	850	10.1	–90 / –102	2.4	NRI/Out
THS4513-SP	150 kRad TID	3000	37.7	–106 / –108	2.2	No
LMH5401-SP	100 kRad TID	6500	60	–99 / –100	1.25	No

6 Pin Configuration and Functions

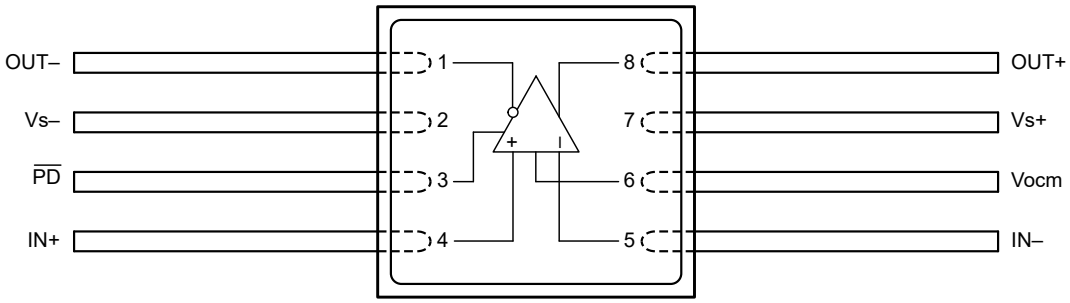

図 6-1. Top View
HKX Package
8-Pin CFP

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN+	4	I	Noninverting (positive) amplifier input
IN–	5	I	Inverting (negative) amplifier input
OUT+	8	O	Noninverted (positive) amplifier output
OUT–	1	O	Inverted (negative) amplifier output
$\overline{PD}$	3	I	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
Vocm	6	I	Common-mode voltage input
Vs+	7	P	Positive power-supply input
Vs–	2	P	Negative power-supply input

(1) I = input, O = output, P = power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, (Vs+) – Vs–		5.25	V
	Input-output voltage range	(Vs–) – 0.5	(Vs+) + 0.5	V
	Differential input voltage		±1	V
Current	Continuous input current		±20	mA
	Continuous output current		±80	mA
	Continuous power dissipation	See *Thermal Information* table and *Thermal Analysis* section		
Temperature	Maximum junction temperature		150	°C
	Operating free-air temperature range	–55	125	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	TBD	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs+	Single-supply voltage	2.7	5	5.1	V
T_A	Ambient temperature	–55	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMH5485-SP HKX (CFP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	128.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	61.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	55.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: $V_{S+} – V_{S–}$ = 5 V

The specifications shown below correspond to the respectively identified subgroup temperature (see セクション 7.7), unless otherwise noted. VOCM = open (defaults midsupply), V_{OUT} = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted. See 図 8-1 for an AC-coupled gain of a 2-V/V test circuit, and 図 8-3 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS		SUBGROUP(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1				530		MHz
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 2				490		MHz
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 5				240		MHz
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 10				125		MHz
GBWP	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20				850		MHz
	Large-signal bandwidth	Vout = 2 V_{PP}				315		MHz
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}				50		MHz
	Slew rate(2)	Vout = 2-V_{PP}, FPBW				1400		V/µs
	Rise/fall time	Vout = 2-V step, input ≤ 0.5 ns t_r				1.4		ns
	Settling time	Vout = 2-V step, t_r = 2 ns	To 1%			5.4		ns
			To 0.1%			10		ns
	Overshoot and undershoot	Vout = 2-V step, input ≤ 0.3 ns t_r				24%		
	100-kHz harmonic distortion	Vout = 2 V_{PP}	HD2			–111		dBc
			HD3			–149		dBc
	10-MHz harmonic distortion	Vout = 2 V_{PP}	HD2			–79		dBc
			HD3			–97		dBc
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone)				–90		dBc
	3rd-order intermodulation distortion					–85		dBc
	Input voltage noise	f > 100 kHz				2.4		nV/√Hz
	Input current noise	f > 1 MHz				1.9		pA/√Hz
	Overdrive recovery time	2x output overdrive, either polarity				20		ns
	Closed-loop output impedance	f = 10 MHz (differential)				0.1		Ω
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			[1, 2, 3]	97	119		dB
	Input-referred offset voltage			[1, 2, 3]	–900	±100	900	µV
	Input offset voltage drift(3)				–2.5	±0.5	2.5	µV/°C
	Input bias current	Positive out of node		[1, 2, 3]	1.7	10	15	µA
	Input bias current drift(3)					6	15	nA/°C
	Input offset current			[1, 2, 3]	–650	±150	650	nA
	Input offset current drift(3)				–1.5	±0.3	1.5	nA/°C
INPUT								
	Common-mode input low	< 3-dB degradation in CMRR from midsupply		[1, 2, 3]		(Vs–) – 0.2	Vs–	V
	Common-mode input high	< 3-dB degradation in CMRR from midsupply		[1, 2, 3]	(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at midsupply		[1, 2, 3]	82	100		dB
	Input impedance differential mode	Input pins at midsupply				110 || 1.25		kΩ || pF

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7.5 Electrical Characteristics: $V_{S+} – V_{S–}$ = 5 V (continued)

The specifications shown below correspond to the respectively identified subgroup temperature (see セクション 7.7), unless otherwise noted. VOCM = open (defaults midsupply), V_{OUT} = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted. See 図 8-1 for an AC-coupled gain of a 2-V/V test circuit, and 図 8-3 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
OUTPUT							
	Output voltage low		[1, 2, 3]		(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high		[1, 2, 3]	(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive		[1, 2, 3]	±75	±100		mA
POWER SUPPLY							
	Specified operating voltage		[1, 2, 3]	2.7	5	5.1	V
	Quiescent operating current		[1, 2, 3]	9.2	10.1	11	mA
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout	[1, 2, 3]	82	100		dB
POWER DOWN							
	Enable voltage threshold		[1, 2, 3]	(Vs–) + 1.7			V
	Disable voltage threshold		[1, 2, 3]			(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+	[1, 2, 3]		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V	[1, 2, 3]		6	30	µA
		$\overline{PD}$ = Vs–	[1, 2, 3]		2	8	µA
	Turnon-time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value			100		ns
	Turnoff time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value			60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)							
	Small-signal bandwidth	Vocm = 100 mV_{PP}			150		MHz
	Slew rate(2)	Vocm = 2-V step			400		V/µs
	Gain		[1, 2, 3]	0.975	0.982	0.995	V/V
	Input bias current	Considered positive out of node	[1, 2, 3]	–0.8	0.1	0.8	µA
	Input impedance	Vocm input driven to midsupply			47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	Vocm pin open	[1, 2, 3]	–45	±8	45	mV
CM Vos	Common-mode offset voltage	Vocm input driven to midsupply	[1, 2, 3]	–8	±2	8	mV
	CM V_{OS} drift(3)	Vocm input driven to midsupply		–20	±4	+20	mV/°C
	Common-mode loop supply headroom to negative supply	< ±15-mV shift from midsupply CM Vos	[1, 2, 3]	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15-mV shift from midsupply CM Vos	[1, 2, 3]	1.2			V

(1) For subgroup definitions, please see セクション 7.7
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_P / \sqrt{2}) \cdot 2\pi \cdot f_{-3dB}$.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range.
(4) Specifications are from the input Vocm pin to the differential output average voltage.

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7.6 Electrical Characteristics: $V_{S+} – V_{S–} = 3$ V

The specifications shown below correspond to the respectively identified subgroup temperature (see セクション 7.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted. See 図 8-1 for an AC-coupled gain of a 2-V/V test circuit, and 図 8-3 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS		SUBGROUP(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1				510		MHz
		Vout = 100 mV_{PP}, G = 2				475		MHz
		Vout = 100 mV_{PP}, G = 5				240		MHz
GBWP	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20				850		MHz
	Large-signal bandwidth	Vout = 2 V_{PP}				300		MHz
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}				50		MHz
	Slew rate(2)	Vout = 2-V step, FPBW				1200		V/µs
	Rise/fall time	Vout = 2-V step, input ≤ 0.5 ns t_r				1.6		ns
	Settling time	Vout = 2-V step, t_r = 2 ns	To 1%			5		ns
			To 0.1%			9		ns
	Overshoot and undershoot	Vout = 2-V step, input ≤ 0.3 ns t_r				25%		
	100-kHz harmonic distortion	Vout = 2 V_{PP}	HD2			–111		dBc
			HD3			–150		dBc
	10-MHz harmonic distortion	Vout = 2 V_{PP}	HD2			–80		dBc
			HD3			–96		dBc
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone)				–89		dBc
	3rd-order intermodulation distortion					–87		dBc
	Input voltage noise	f > 100 kHz				2.4		nV/√Hz
	Input current noise	f > 1 MHz				1.9		pA/√Hz
	Overdrive recovery time	2X output overdrive, either polarity				20		ns
	Closed-loop output impedance	f = 10 MHz (differential)				0.1		Ω
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			[1, 2, 3]	97	119		dB
	Input-referred offset voltage			[1, 2, 3]	–900	±100	900	µV
	Input offset voltage drift(3)				–2.5	±0.5	2.5	µV/°C
	Input bias current	Positive out of node		[1, 2, 3]	1.7	9	15	µA
	Input bias current drift(3)					5	15	nA/°C
	Input offset current			[1, 2, 3]	–650	±150	650	nA
	Input offset current drift(3)				–1.5	±0.3	1.5	nA/°C
INPUT								
	Common-mode input low	< 3-dB degradation in CMRR from midsupply		[1, 2, 3]		(Vs–) – 0.2	Vs–	V
	Common-mode input high	< 3-dB degradation in CMRR from midsupply		[1, 2, 3]	(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at midsupply		[1, 2, 3]	82	100		dB
	Input impedance differential mode	Input pins at midsupply				110 || 1.25		kΩ || pF

ADVANCE INFORMATION

7.6 Electrical Characteristics: $V_{S+} – V_{S–}$ = 3 V (continued)

The specifications shown below correspond to the respectively identified subgroup temperature (see セクション 7.7), unless otherwise noted. Vocm = open (defaults midsupply), V_{OUT} = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted. See 図 8-1 for an AC-coupled gain of a 2-V/V test circuit, and 図 8-3 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
OUTPUT							
	Output voltage low		[1, 2, 3]		(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high		[1, 2, 3]	(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive		[1, 2, 3]	±55	±60		mA
POWER SUPPLY							
	Specified operating voltage		[1, 2, 3]	2.7	3	5.1	V
	Quiescent operating current		[1, 2, 3]	9	9.7	10.6	mA
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout	[1, 2, 3]	82	100		dB
POWER DOWN							
	Enable voltage threshold		[1, 2, 3]	(Vs–) + 1.7			V
	Disable voltage threshold		[1, 2, 3]			(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+	[1, 2, 3]		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V	[1, 2, 3]		2	30	µA
		$\overline{PD}$ = Vs–	[1, 2, 3]		1	8	µA
	Turnon-time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value			100		ns
	Turnoff time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value			60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)							
	Small-signal bandwidth	Vocm = 100 mV_{PP}			140		MHz
	Slew rate(2)	Vocm = 1-V step			350		V/µs
	Gain		[1, 2, 3]	0.975	0.987	0.990	V/V
	Input bias current	Considered positive out of node	[1, 2, 3]	–0.7	0.1	0.7	µA
	Input impedance	Vocm input driven to midsupply			47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	Vocm pin open	[1, 2, 3]	–45	±10	45	mV
CM Vos	Common-mode offset voltage	Vocm input driven to midsupply	[1, 2, 3]	–8	±2	8	mV
	CM V_{OS} drift(3)	Vocm input driven to midsupply		–20	±4	20	mV/°C
	Common-mode loop supply headroom to negative supply	< ±15-mV shift from midsupply CM Vos	[1, 2, 3]	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15-mV shift from midsupply CM Vos	[1, 2, 3]	1.2			V

(1) For subgroup definitions, please see セクション 7.7
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_P / \sqrt{2}) \cdot 2\pi \cdot f_{-3dB}$.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range. Maximum drift set by distribution of a large sampling of devices. Drift is not specified by test or QA sample test.
(4) Specifications are from input Vocm pin to differential output average voltage.

ADVANCE INFORMATION

7.7 Quality Conformance Inspection

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55

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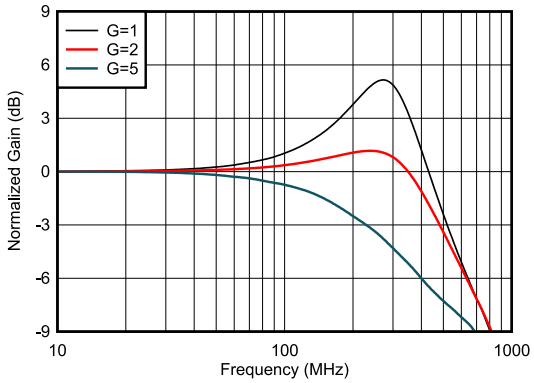
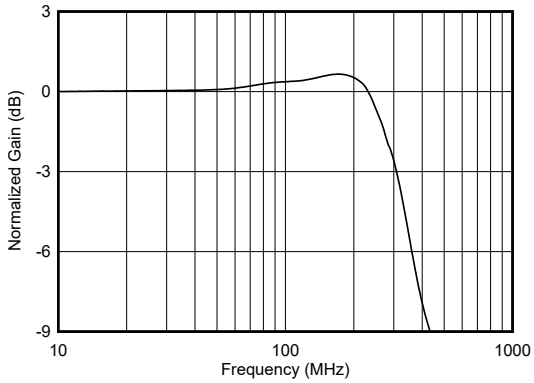
7.8 Typical Characteristics: 5 V Single Supply

at Vs+ = 5 V, Vs– = GND, R_F= 402 Ω, Vocm is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



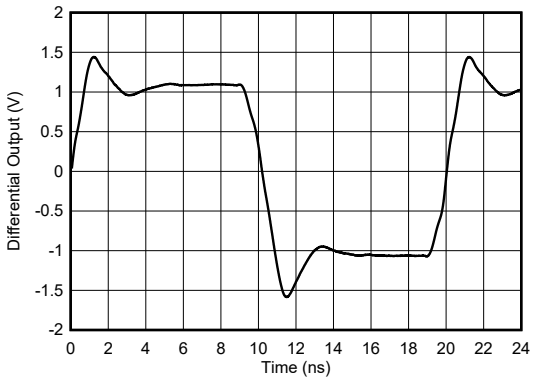
Vo = 100 mVpp, see 図 8-1 and 表 9-1 for resistor values

図 7-1. Small-Signal Frequency Response vs Gain



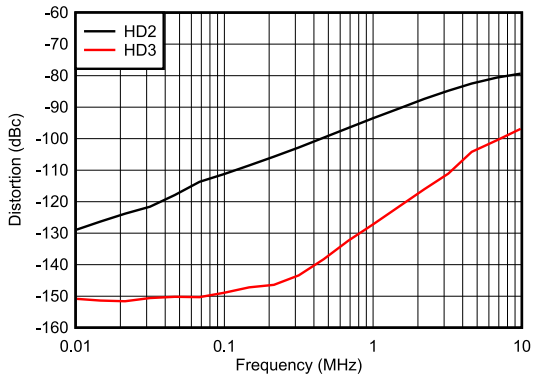
V_O = 2 Vpp, see 図 8-1 and 表 9-1 for resistor values

図 7-2. Large-Signal Frequency Response



50 MHz input, 0.5-ns input edge rate, single-ended to differential output, split supply, DC-coupled, see 図 8-3

図 7-3. Large-Signal Step Response

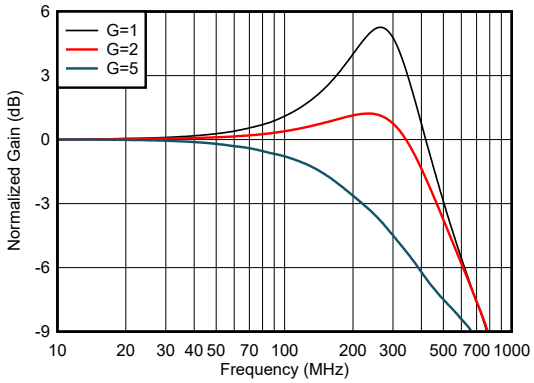


2 V_{PP} output, see 図 8-1

図 7-4. Harmonic Distortion Over Frequency

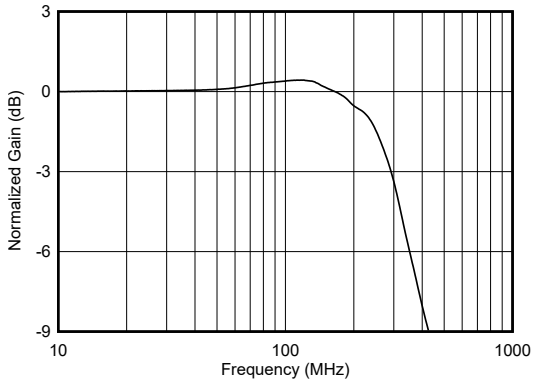
7.9 Typical Characteristics: 3 V Single Supply

at Vs+ = 3 V, Vs– = GND, Vocm is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



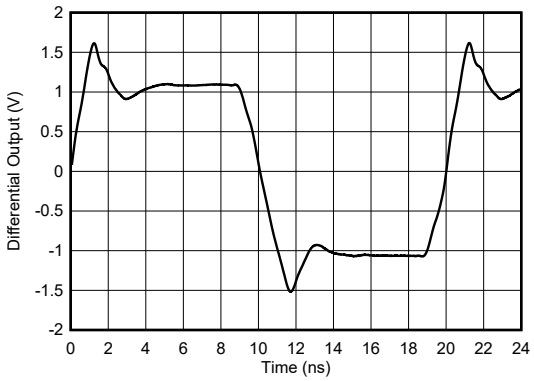
Rf = 402 Ω, Vout = 100 mV_{PP}, see 図 8-1 and 表 9-1 for resistor values

図 7-5. Small-Signal Frequency Response vs Gain



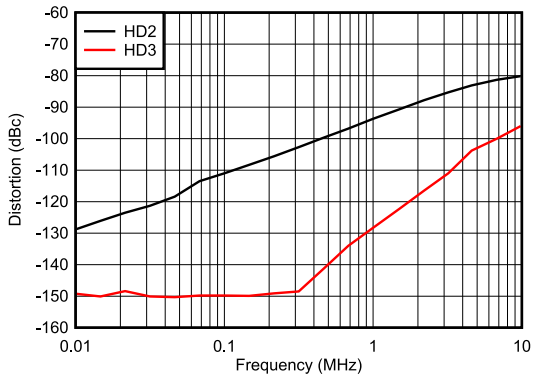
Rf = 402 Ω, Vout = 2 V_{PP}, see 図 8-1 and 表 9-1 for resistor values

図 7-6. Large-Signal Frequency Response



50 MHz input, 0.5-ns input edge rate, single-ended input to differential output, split supply, DC coupled, see 図 8-3

図 7-7. Large-Signal Step Response



2 V_{PP} output, see 図 8-1 with Vs+ = 3 V, Vocm = 1.5 V

図 7-8. Harmonic Distortion Over Frequency

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7.10 Typical Characteristics: 3 V to 5 V Supply Range

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

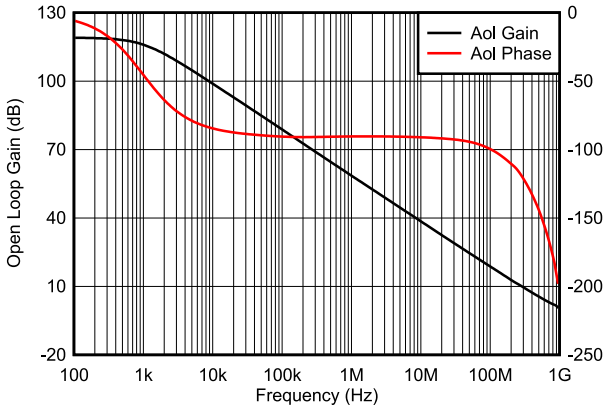
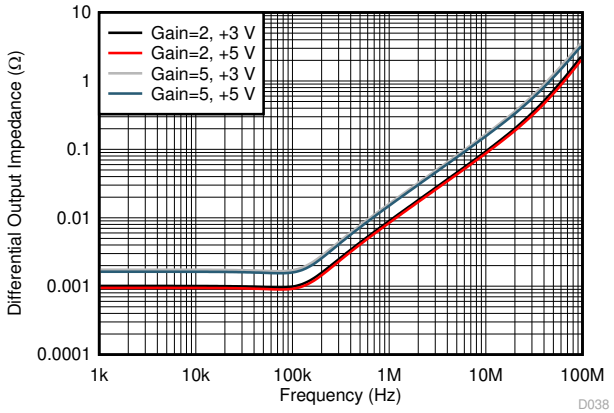


図 7-9. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Single-ended input to differential output, simulated differential output impedance, see 図 8-1

図 7-10. Closed-Loop Output Impedance

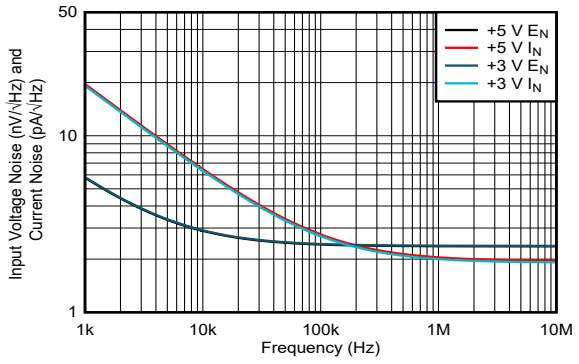
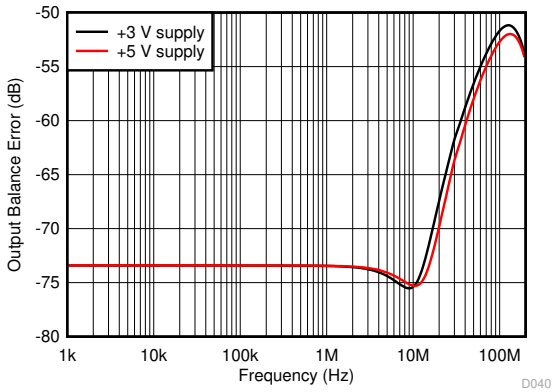
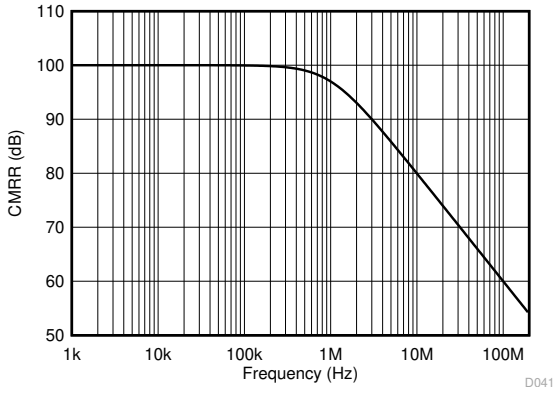


図 7-11. Input Spot Noise Over Frequency



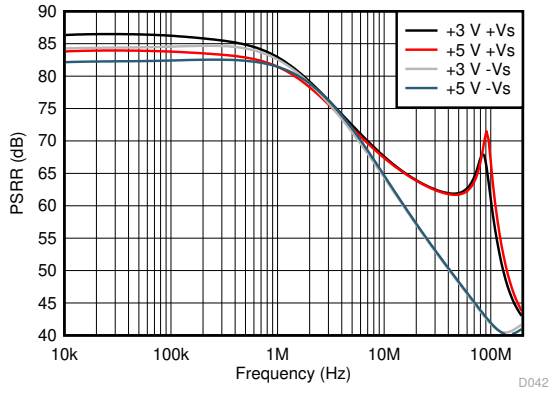
Single-ended input to differential output, gain of 2 (see 図 8-1), simulated with 1% resistor, worst-case mismatch

図 7-12. Output Balance Error Over Frequency



Common-mode in to differential out, gain of 2 simulation

図 7-13. CMRR Over Frequency

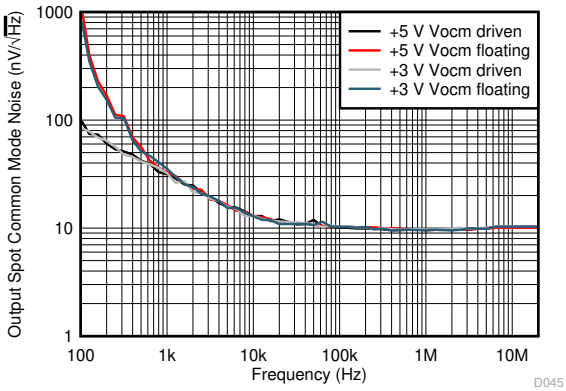


Single-ended to differential, gain of 2 (see 図 8-1) PSRR simulated to differential output

図 7-14. PSRR Over Frequency

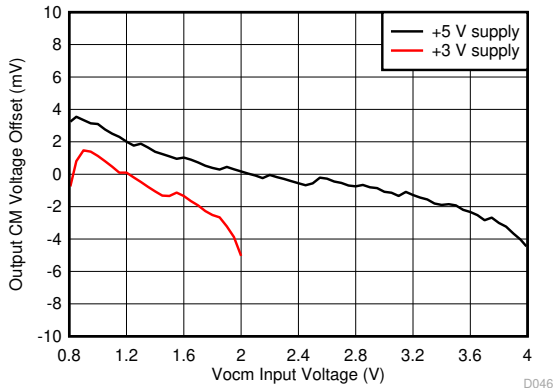
7.10 Typical Characteristics: 3 V to 5 V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



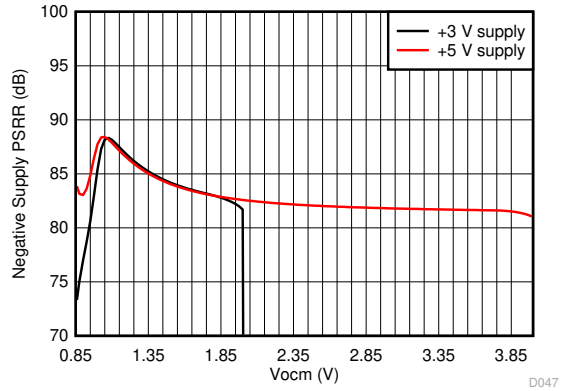
Vocm input either driven to mid-supply by low impedance source, or allowed to float and default to mid-supply

図 7-15. Output Common-Mode Noise



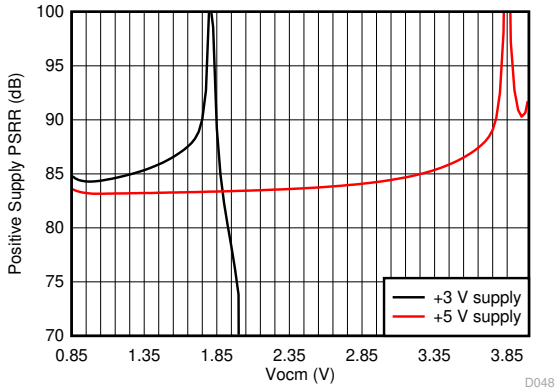
Average Vocm output offset of 37 units, Standard deviation < 2.5 mV, see 図 8-3

図 7-16. Vocm Offset vs Vocm Setting



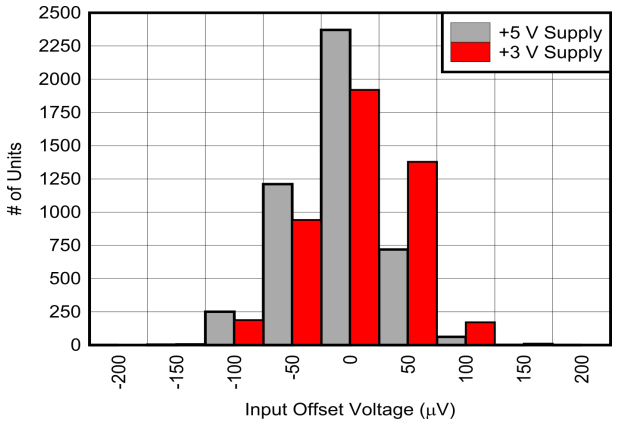
Single-ended to differential gain of 2 (see 図 8-1), PSRR for negative supply to differential output (1-kHz simulation)

図 7-17. –PSRR vs Vocm Approaching Vs–



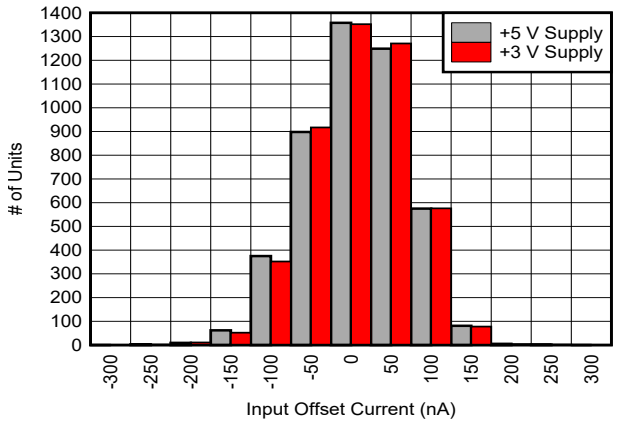
Single-ended to differential gain of 2 (see 図 8-1), PSRR for positive supply to differential output (1-kHz simulation)

図 7-18. +PSRR vs Vocm Approaching Vs+



Total of 4618 units for each supply. For Vs = 5 V: μ = -35.1 μV, σ = 38.9 μV

図 7-19. Input Offset Voltage



Total of 4618 units for each supply. For Vs = 5 V: μ = 16.7 nA, σ = 62.3 nA

図 7-20. Input Offset Current

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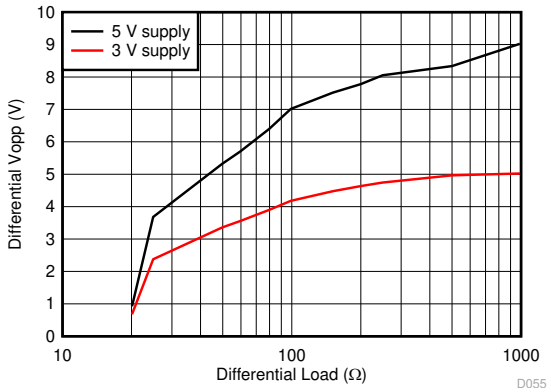
7.10 Typical Characteristics: 3 V to 5 V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



Maximum differential output swing, Vocm at mid-supply

図 7-21. Maximum Vopp vs Rload

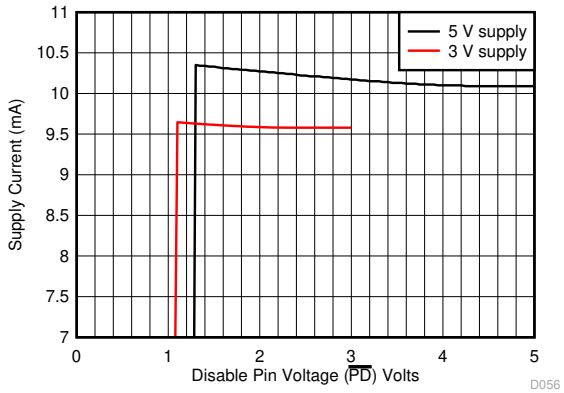
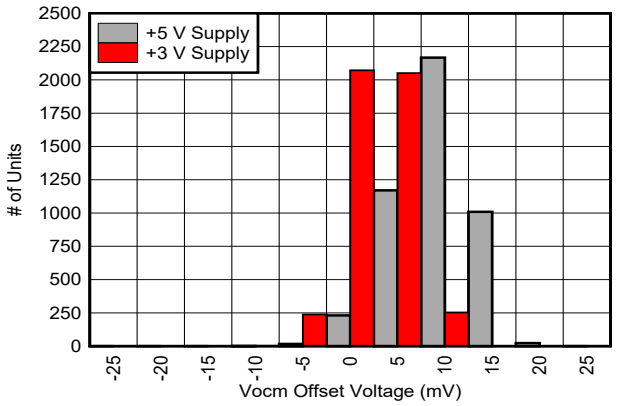
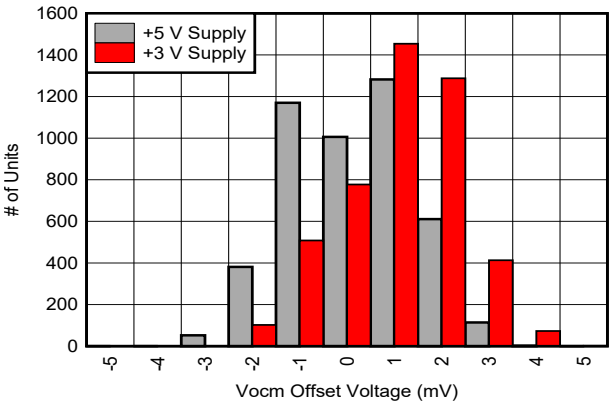


図 7-22. Supply Current vs PD Voltage



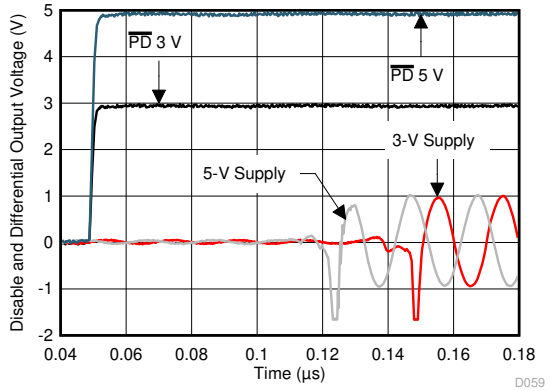
Vocm input floating. Total of 4618 units for each supply. For Vs = 5 V: μ = 6.8 mV, σ = 3.9 mV

図 7-23. Common-Mode Output Offset from Vs+ / 2 Default Value



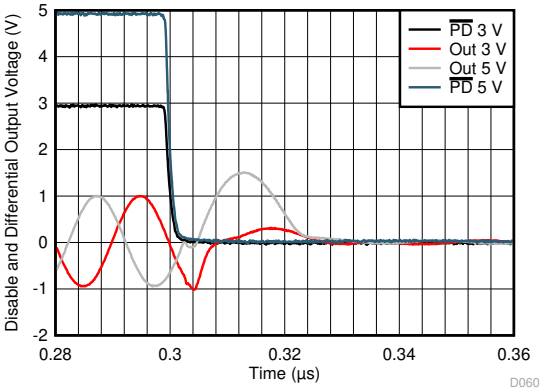
Total of 4618 units for each supply. For Vs = 5 V: μ = 0.3 mV, σ = 1.3 mV

図 7-24. Common-Mode Output Offset from Driven Vocm



10 MHz, 1 Vpp input single to differential gain of 2, see 図 8-3

図 7-25. PD Turn On Waveform



10 MHz, 1 V_{PP} input single to differential gain of 2, see 図 8-3

図 7-26. PD Turn Off Waveform

8 Parameter Measurement Information

8.1 Example Characterization Circuits

The LMH5485-SP offers the advantages of a fully differential amplifier (FDA) design, with the trimmed input offset voltage of a precision op amp. The FDA is an extremely flexible device that provides a purely differential output signal centered on a settable output common-mode level. The primary options revolve around the choices of single-ended or differential inputs, AC-coupled or DC-coupled signal paths, gain targets, and resistor Value selections. Differential sources can certainly be supported and are often simpler to both implement and analyze.

Because most lab equipment is single-ended, the characterization circuits typically operate with a single-ended, matched, 50 Ω input termination to a differential output at the FDA output pins. That output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled, step-response testing uses two 50 Ω scope inputs with trace math. The starting point for any single-ended-to-differential, AC-coupled characterization plot is shown in 図 8-1.

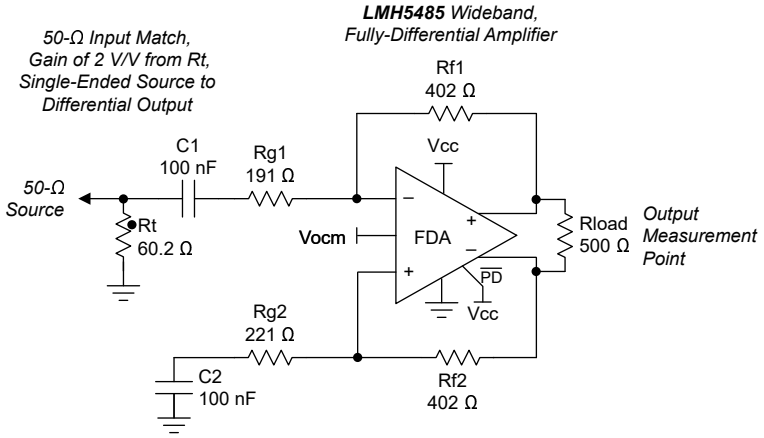


図 8-1. AC-Coupled, Single-Ended Source to a Differential Gain of a 2 V/V Test Circuit

図 8-1 shows how most characterization plots fix the R_f (R_{f1} = R_{f2}) value at 402 Ω. This element value is completely flexible in application, but the 402 Ω provides a good compromise for the parasitic issues linked to this value, specifically:

- Added output loading. The FDA appears like an inverting op amp design with both feedback resistors as an added load across the outputs (approximate total differential load in 図 8-1 is 500 Ω || 804 Ω = 308 Ω).
- Noise contributions because of the resistor values. The resistors contribute both a 4kTR term and provide gain for the input current noise.
- Parasitic feedback pole at the input summing nodes. This pole created by the feedback R value and the 1.25-pF 0.9-pF differential input capacitance (as well as any board layout parasitic) introduces a zero in the noise gain, decreasing the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot. The 402 Ω value selected does degrade the phase margin slightly over a lower value, but does not decrease the loading significantly from the nominal 500 Ω value across the output pins.

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The frequency domain characterization curves start with the selections of 図 8-1. Then, various elements are modified to show their impact over a range of design targets, specifically:

- Gain setting is changed by adjusting R_t and the $2 – R_g$ elements (holding a 50 Ω input match).
- Output loading, including both resistive and capacitive load testing.
- Power-supply settings. Most often, a single +5 V test uses a ±2.5 V supply, and a +3 V test uses ±1.5 V supplies.
- The disable control pin is tied to Vs+ for any active channel test.

Because most network and spectrum analyzers are a single-ended input, the output network on the LMH5485-SP characterization tests typically show the desired load connected through a balun to a single-ended, 50 Ω load, while presenting a 50 Ω source from the balun output back into the balun. For instance, 図 8-2 shows a wideband MA/Com balun used for 図 8-1. This network shows a 500 Ω differential load to the LMH5485-SP, but an AC-coupled, 50 Ω source to the network analyzer. Distortion testing typically uses a lower-frequency, DC-isolated balun (such as the TT1-6T) that is rotated 90° from the wider band interface of 図 8-2.

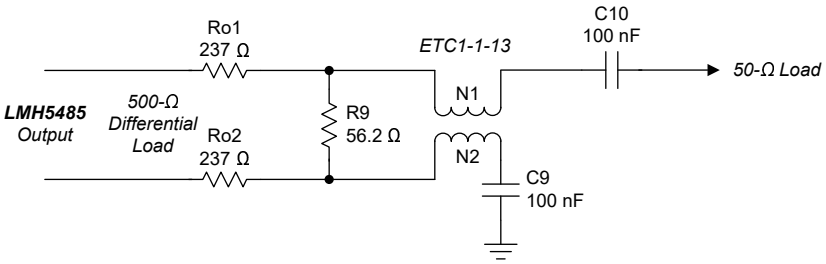

図 8-2. Example 500 Ω Load to a Single-Ended, Doubly-Terminated, AC-Coupled, 50 Ω Interface

This approach allows a higher differential load, but with a wideband 50 Ω output match at the cost of considerable signal-path insertion loss. This loss is acceptable for characterization, and is normalized out to show the characterization curves.

図 8-3 shows the circuit used as a starting point for time-domain or DC-coupled testing.

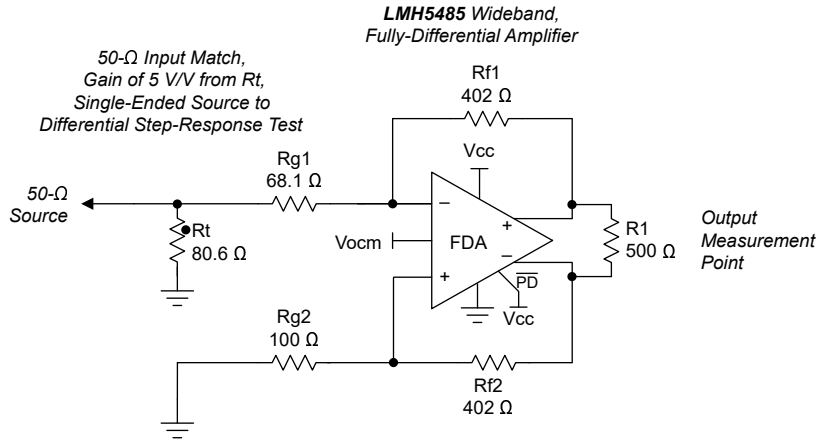

図 8-3. DC-Coupled, Single-Ended-to-Differential, Basic Test Circuit Set for a Gain of 5 V/V

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In this case, the input is DC-coupled, showing a 50 Ω input match to the source, gain of 5 V/V to a differential output, again driving a nominal 500 Ω load. Using a single supply, the Vocm control input can either be floated (defaulting to mid-supply) or be driven within the allowed range for the Vocm loop (see the headroom limits on Vocm in the *Electrical Characteristics: VS+ −VS = 5 V* tables). To use this circuit for step-response measurements, load each of the two outputs with a 250 Ω network, translating to a 50 Ω source impedance driving into two 50 Ω scope inputs. Then, difference the scope inputs to generate the step responses. 図 8-4 shows the output interface circuit. This grounded interface pulls a DC load current from the output Vocm voltage for single-supply operation. Running this test with balanced bipolar power supplies eliminates this DC load current and gives similar waveform results.

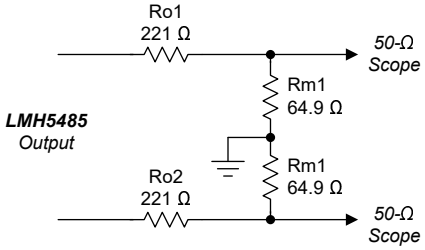

図 8-4. Example 500 Ω Load to Differential, Doubly-Terminated, DC-Coupled 50 Ω Scope Interface

9 Detailed Description

9.1 Overview

The LMH5485-SP is a voltage-feedback (VFA) based, fully-differential amplifier (FDA) offering greater than 490 MHz, small-signal bandwidth at a gain of 2 V/V with trimmed supply current and input offset voltage. The core differential amplifier is a slightly decompensated voltage-feedback design with a high slew-rate, precision input stage. This design gives the 490 495 MHz gain of 2 V/V small-signal bandwidth shown in the characterization curves, with a 1400 1300 V/µs slew rate, yielding approximately a 315 295 MHz, 2 V_{PP}, large-signal bandwidth in the same circuit configuration.

The outputs offer near rail-to-rail output swing (0.2 V headroom to either supply), while the device inputs are negative rail inputs with approximately 1.2 V of headroom required to the positive supply. 図 8-3 shows how this negative rail input directly supports a bipolar input around ground in a DC-coupled, single-supply design. Similar to all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the Vocm input pin that can be either floated to default near mid-supply or driven to a desired output common-mode voltage. The Vocm range extends from a very low 0.91 V above the negative supply to 1.1 V below the positive supply, supporting a wide range of modern analog-to-digital converter (ADC) input common-mode requirements using a single 2.7 V to 5.1 V supply range for the LMH5485-SP.

A power-down pin ($\overline{PD}$) is included. Pull the $\overline{PD}$ pin voltage to the negative supply to turn the device off, putting the LMH5485-SP into a very-low quiescent current state. For normal operation, the $\overline{PD}$ pin must be asserted high. When the device is disabled, remember that the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH5485-SP still appear at the outputs at some level through this passive resistor path as they would for any disabled FDA device.

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9.1.1 Terminology and Application Assumptions

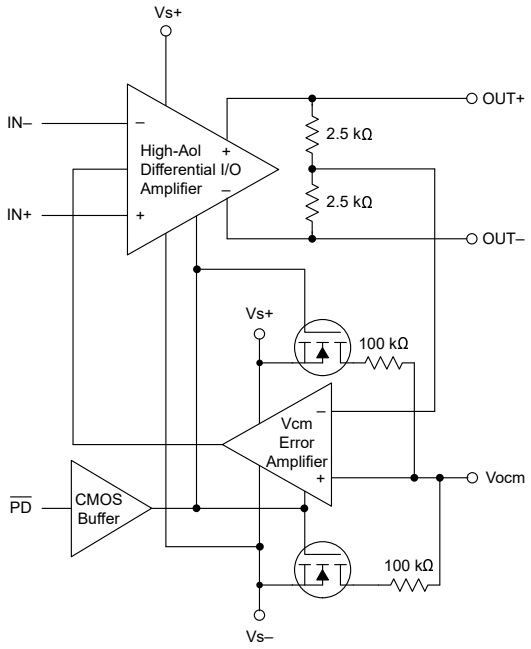
Like all widely-used devices, numerous common terms have developed that are unique to this type of device. These terms include:

- Fully differential amplifier (FDA)—In this document, this term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not high-impedance input) and includes a second internal control-loop setting the output average voltage (Vocm) to a default or set point. This second loop interacts with the differential loop in some configurations.
- The desired output signal at the two output pins is a *differential* signal swinging symmetrically around a *common-mode* voltage where that is the average voltage for the two outputs.
- Single-ended to differential—always use the outputs differentially in an FDA; however, the source signal can be either a single-ended source or differential, with a variety of implementation details for either. When the FDA operation is single-ended to differential, only one of the two input resistors receives the source signal with the other input resistor connected to a DC reference (often ground) or through a capacitor to ground.

To simplify, several features in the application of the LMH5485-SP are not explicitly stated, but are necessary for correct operation. These requirements include:

- Although not always stated, make sure to tie the power disable pin to the positive supply when only an enabled channel is desired.
- Virtually all AC characterization equipment expects a 50 Ω termination from the 50 Ω source, and a 50 Ω single-ended source impedance from the device outputs to the 50 Ω sensing termination. This termination is achieved in all characterizations (often with some insertion loss), but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the LMH5485-SP, and on to an ADC input do not require doubly-terminated lines or filter designs; the exception is if the source requires a defined termination impedance for correct operation (for example, a SAW filter source).
- External element values are normally assumed to be accurate and matched. In an FDA, match the feedback resistor values and also match the (DC and AC) impedance from the summing junctions to the source on one side and the reference or ground on the other side. Unbalancing these values introduces nonidealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides create a common-mode to differential conversion. Also, mismatched Rf values and feedback ratios create some added differential output error terms from any common-mode DC, ac signal, or noise terms. Snapping to standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Mismatched resistors or ratios do not in themselves degrade harmonic distortion. If there is meaningful CM noise or distortion coming in, those errors are converted to a differential error through element or ratio mismatch.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Differential I/O

The LMH5485-SP combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage with a dominant pole at approximately 900 Hz. This voltage feedback structure projects a single-pole, unity-gain Aol at 850 MHz (gain bandwidth product). The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the Vocm pin. If floated, this reference is at half the total supply voltage across the device using two 100-kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the Vocm pin. The bandwidth of this error amplifier is approximately the same bandwidth as the main differential I/O amplifier.

The differential outputs are collector outputs to obtain the rail-to-rail output swing. These outputs are relatively high-impedance, open-loop sources; however, closing the loop provides a very low output impedance for load driving. No output current limit or thermal shutdown features are provided in this lower-power device. The differential inputs are PNP inputs to provide a negative-rail input range.

To operate the LMH5485-SP connect the OUT– pin to the IN+ pin through an Rf, and the OUT+ pin to the IN– pin through the same value of Rf. Bring in the inputs through additional resistors to the IN+ and IN– pins. The differential I/O op amp operates similarly to an inverting op amp structure where the source must drive the input resistor and the gain is the ratio of the feedback to the input resistor.

9.3.2 Power-Down Control Pin ($\overline{PD}$)

The LMH5485-SP includes a power-down control pin, $\overline{PD}$. This pin must be asserted high for correct amplifier operation. The $\overline{PD}$ pin cannot be floated because there is no internal pullup or pulldown resistor on this pin to reduce disabled power consumption. Asserting this pin low (within 0.7 V of the negative supply) puts the LMH5485-SP into a very low quiescent state (approximately 2 µA). Switches in the default Vocm resistor string open to eliminate the fixed bias current (25 µA) across the supply in this 200-kΩ voltage divider to mid-supply.

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9.3.2.1 Operating the Power Shutdown Feature

When the $\overline{PD}$ pin is asserted high, close to the positive supply, the device will be in normal active mode of operation. To disable the device for reduced power consumption, $\overline{PD}$ pin must be asserted low, close to the negative supply. 図 7-22 shows the $\overline{PD}$ pin voltage and the corresponding quiescent current drawn. For applications that require the device to only be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

The disable operation is referenced from the negative supply (normally, ground). For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the LMH5485-SP off when the negative supply exceeds –0.7 V.

For single-supply operation, a minimum of 1.7 V above the negative supply (ground, in this case) is required to assure operation. This minimum logic-high level allows for direct operation from 1.8 V supply logic.

9.3.3 Input Overdrive Operation

The LMH5485-SP input stage architecture is intrinsically robust to input overdrives with the series input resistor required by all applications. High input overdrives cause the outputs to limit into their maximum swings with the remaining input current through the Rg resistors absorbed by internal, back-to-back protection diodes across the two inputs. These diodes are normally off in application, and only turn on to absorb the currents that a large input overdrive might produce through the source impedance and or the series Rg elements required by all designs.

The internal input diodes can safely absorb up to ±15 mA in an overdrive condition. For designs that require more current to be absorbed, consider adding an external protection diode such as BAV99.

9.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than (Vs–) + 1.7 V or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops the correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The Vocm control pin sets the output average voltage. Left open, Vocm defaults to an internal mid-supply value. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal Vcm error amplifier.

9.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the Rg value. This input active impedance issue applies to both AC- and DC-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in the following subsections.

9.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be AC-coupled, the DC biasing for the LMH5485-SP becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The AC-coupling issue can be separated for the input and output sides of an FDA design. The input can be AC coupled and the output DC coupled, or the output can be AC coupled and the input DC coupled, or they can both be AC coupled. One situation where the output might be DC coupled (for an AC-coupled input), is when driving directly into an ADC where the Vocm control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. In any case, the design starts by setting the desired Vocm. When an AC-coupled path follows the output pins, the best linearity is achieved by operating Vocm at mid-supply. The Vocm voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91 V greater than the negative supply and 1.1 V less than the positive supply). If the output path is also AC coupled, simply letting the Vocm control pin float is usually preferred in order to get a mid-supply default Vocm bias with minimal elements. To limit noise, place a 0.1 µF decoupling capacitor on the Vocm pin to ground.

After Vocm is defined, check the target output voltage swing to ensure that the Vocm plus the positive or negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as Vopp, divide by 4 to obtain the ±Vp swing around Vocm at each of the two output pins (each pin operates 180° out of phase with the other). Check that Vocm ±Vp does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the nonsignal input side are DC blocked (see 図 8-1), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher Vocm voltages. Because the input Vicm is the output Vocm for AC-coupled sources, the 1.2 V minimum headroom for the input pins to the positive supply overrides the 1.1 V headroom limit for the output Vocm. Also, the input signal moves this input Vicm around the DC bias point, as described in the *Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA* section.

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9.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the AC-coupled design. Again, the input can be DC-coupled while the output is AC-coupled. A DC-coupled input with an AC-coupled output might have some advantages to move the input Vicm down if the source is ground referenced. 図 8-3 shows how when the source is DC-coupled into the LMH5485-SP, both sides of the input circuit must be DC coupled to retain differential balance. Normally, the nonsignal input side has an Rg element biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around Vocm at the outputs. Often, Rg2 is simply grounded for DC-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source is swinging around ground. If the source swings from ground to some positive voltage, grounding Rg2 gives a unipolar output differential swing from both outputs at Vocm (when the input is at ground) to one polarity of swing. Biasing Rg2 to an expected midpoint for the input signal creates a differential output swing around Vocm.

One significant consideration for a DC-coupled input is that Vocm sets up a common-mode bias current from the output back through Rf and Rg to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this DC current. After the input signal range and biasing on the other Rg element is set, check that the voltage divider from Vocm to Vin through Rf and Rg (and possibly Rs) establishes an input Vicm at the device input pins that is in range. If the average source is at ground, the negative rail input stage for the LMH5485-SP is in range for applications using a single positive supply and a positive output Vocm setting because this DC current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

9.4.1.3 Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA

The design equations for setting the resistors around an FDA to convert from a single-ended input signal to differential output can be approached from several directions. Here, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and set equal on the two sides.
- The DC and AC impedances from the summing junctions back to the signal source and ground (or a bias voltage on the nonsignal input side) are set equal to retain feedback divider balance on each side of the FDA

Both of these assumptions are typical and aimed to delivering the best dynamic range through the FDA signal path.

図 8-1 and 図 8-3 shows how after the feedback resistor values are chosen, the aim is to solve for the Rt (a termination resistor to ground on the signal input side), Rg1 (the input gain resistor for the signal path), and Rg2 (the matching gain resistor on the nonsignal input side). The same resistor solutions can be applied to either AC- or DC-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. 図 8-1 shows how adding these blocking capacitors after the Rt element has the advantage of removing any DC currents in the feedback path from the output Vocm to ground.

Earlier approaches to the solutions for Rt and Rg1 (when the input must be matched to a source impedance, Rs) follow an iterative approach. This complexity arises from the active input impedance at the Rg1 input. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the Rg2 element. 式 1shows a more recent solution, where a quadratic in Rt can be solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are the following:

1. The selected Rf value.
2. The target voltage gain (Av) from the input of Rt to the differential output voltage.
3. The desired input impedance at the junction of Rt and Rg1 to match Rs.

As 式 1 shows, solving this quadratic for Rt starts the solution sequence.

$$Rt^2 - Rt\frac{2Rs\left(2Rf + \frac{Rs}{2}Av^2\right)}{2Rf\left(2 + Av\right) - RsAv(4 + Av)} - \frac{2RfRs^2Av}{2Rf\left(2 + Av\right) - RsAv(4 + Av)} = 0 \quad (1)$$

Being a quadratic, there are limits to the range of solutions. Specifically, after Rf and Rs are chosen, there is physically a maximum gain beyond which 式 1 starts to solve for negative Rt values (if input matching is a requirement). With Rf selected, use 式 2 to verify that the maximum gain is greater than the desired gain.

$$Av_{max} = \left(\frac{Rf}{Rs} - 2\right) \bullet \left[1 + \sqrt{1 + \frac{4\frac{Rf}{Rs}}{\left(\frac{Rf}{Rs} - 2\right)^2}}\right] \quad (2)$$

If the achievable Av_{max} is less than desired, increase the Rf value. After Rt is derived from 式 1, the Rg1 element is given by 式 3:

$$Rg1 = \frac{2\frac{Rf}{Av} - Rs}{1 + \frac{Rs}{Rt}} \quad (3)$$

Then, the simplest approach is to use a single Rg2 = Rt || Rs + Rg1 on the nonsignal input side. Often, this approach is shown as the separate Rg1 and Rs elements. Using these separate elements provide a better divider match on the two feedback paths, but a single Rg2 is often acceptable. A direct solution for Rg2 is given as 式 4:

$$Rg2 = \frac{2\frac{Rf}{Av}}{1 + \frac{Rs}{Rt}} \quad (4)$$

This design proceeds from a target input impedance matched to Rs, signal gain Av from the matched input to the differential output voltage, and a selected Rf value. The nominal Rf value chosen for the LMH5485-SP characterization is 402 Ω. As discussed previously, going lower improves noise and phase margin, but reduces the total output load impedance possibly degrading harmonic distortion. Going higher increases the output noise, and might reduce the loop-phase margin because of the feedback pole to the input capacitance, but reduces the total loading on the outputs. Using 式 2 to 式 4 to sweep the target gain from 1 to Av_{max} < 14.3 V/V gives 表 9-1, which shows exact values for Rt, Rg1, and Rg2, where a 50 Ω source must be matched while setting the two feedback resistors to 402 Ω. One possible solution for 1% standard values is shown along with the resulting actual input impedance and gain with % errors to the targets in 表 9-1.

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表 9-1. Required Resistors for a Single-Ended to Differential FDA Design Stepping Gain from 1 V/V to 14 V/V

Av(1)	Rt, EXACT (Ω)	Rt 1%	Rg1, EXACT (Ω)	Rg1 1%	Rg2, EXACT (Ω)	Rg2 1%	ACTUAL Z_{IN}	%ERR TO Rs	ACTUAL GAIN	%ERR TO Av
1	55.2	54.9	395	392	421	422	49.731	–0.54%	1.006	0.62%
2	60.1	60.4	193	191	220	221	50.171	0.34%	2.014	0.72%
3	65.6	64.9	123	124	151	150	49.572	–0.86%	2.983	–0.57%
4	72.0	71.5	88.9	88.7	118	118	49.704	–0.59%	4.005	0.14%
5	79.7	80.6	68.4	68.1	99.2	100	50.451	0.90%	5.014	0.28%
6	89.1	88.7	53.7	53.6	85.7	86.6	49.909	–0.18%	6.008	0.14%
7	101	102	43.5	43.2	77.1	76.8	50.179	0.36%	7.029	0.42%
8	117	118	35.5	35.7	70.6	69.8	50.246	0.49%	7.974	–0.32%
9	138	137	28.8	28.7	65.4	64.9	49.605	–0.79%	9.016	0.18%
10	170	169	23.5	23.7	62.0	61.9	50.009	0.02%	9.961	–0.39%
11	220	221	18.8	18.7	59.6	59.0	49.815	–0.37%	11.024	0.22%
12	313	316	14.7	14.7	57.9	57.6	50.051	0.10%	11.995	–0.04%
13	545	549	10.9	11.0	56.7	56.2	49.926	–0.15%	12.967	–0.25%
14	2209	2210	7.26	7.32	56.2	56.2	50.079	0.16%	13.986	–0.10%

(1) Rf = 402 Ω, Rs = 50 Ω, and Av_{MAX} = 14.32 V/V.

These equations and design flow apply to any FDA. Using the feedback resistor value as a starting point is particularly useful for current-feedback-based FDAs such as the LMH6554, where the value of these feedback resistors determines the frequency response flatness. Similar tables can be built using the equations provided here for other source impedances, Rf values, and gain ranges.

Note the extremely low Rg1 values at the higher gains. For instance, at a gain of 14 V/V, that 7.32 Ω standard value is transformed by the action of the common-mode loop moving the input common-mode voltage to appear like a 50 Ω input match. This active input impedance provides an improved input-referred noise at higher gains. The TINA model correctly shows this actively-set input impedance in the single-ended to differential configuration, and is a good tool to validate the gains, input impedances, response shapes, and noise issues.

9.4.1.4 Input Impedance for the Single-Ended to Differential FDA Configuration

The designs so far have included a source impedance, Rs, that must be matched by Rt and Rg1. The total impedance at the junction of Rt and Rg1 for the circuit of 図 8-3 is the parallel combination of Rt to ground, and the ZA (active impedance) presented by Rg1. The expression for ZA, assuming Rg2 is set to obtain the differential divider balance, is given by 式 5:

$$ZA = Rg1\frac{\left(1+\frac{Rg1}{Rg2}\right)\left(1+\frac{Rf}{Rg1}\right)}{2+\frac{Rf}{Rg2}} \quad (5)$$

For designs that do not need impedance matching, but instead come from the low impedance output of another amplifier for instance, Rg1 = Rg2 is the single-to-differential design used without an Rt to ground. Setting Rg1 = Rg2 = Rg in 式 5 gives the input impedance of a simple input FDA driving from a low-impedance, single-ended source to a differential output as shown in 式 6:

$$ZA = 2Rg\frac{1+\frac{Rf}{Rg}}{2+\frac{Rf}{Rg}} \quad (6)$$

In this case, setting a target gain as Rf / Rg ≡ α, and then setting the desired input impedance, allows the Rg element to be resolved first, and then the required Rf to get the gain. For example, targeting an input impedance of 200 Ω with a gain of 4 V/V, 式 7 gives the physical Rg element. Multiplying this required Rg value by a gain of 4 gives the Rf value and the design of 図 9-1.

$$Rg = ZA\frac{2+\alpha}{2(1+\alpha)} \tag{7}$$

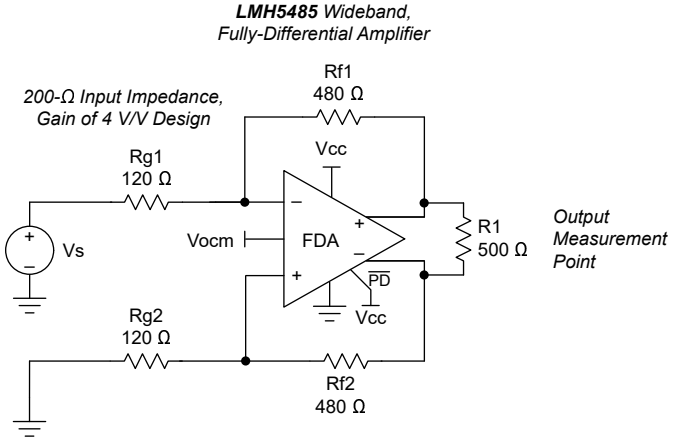

図 9-1. 200 Ω Input Impedance, Single-Ended to Differential DC-Coupled Design with Gain of 4 V/V

After being designed, this circuit can also be AC-coupled by adding blocking caps in series with the two 120 Ω Rg resistors. This active input impedance has the advantage of increasing the apparent load to the prior stage using lower resistors values, leading to lower output noise for a given gain target.

9.4.2 Differential-Input to Differential-Output Operation

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming the two sides of the circuit are balanced with equal Rf and Rg elements, the differential input impedance is now just the sum of the two Rg elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be DC biased in the allowable range for the input pins with consideration given to the voltage headroom required from each supply. Slightly different considerations apply to AC- or DC-coupled, differential-in to differential-out designs, as described in the following sections.

9.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the LMH5485-SP with an AC-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). 図 9-2 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (Rm) is included in this design. This Rm element allows the input Rg resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the Rg elements sum to show a 200 Ω differential impedance, while the Rm element combines in parallel to give a net 100 Ω, AC-coupled, differential impedance to the source. Again, the design proceeds ideally by selecting the Rf element values, then the Rg to set the differential gain, then an Rm element (if needed) to achieve a target input impedance. Alternatively, the Rm element can be eliminated, the Rg elements set to the desired input impedance, and Rf set to the get the differential gain (= Rf / Rg).

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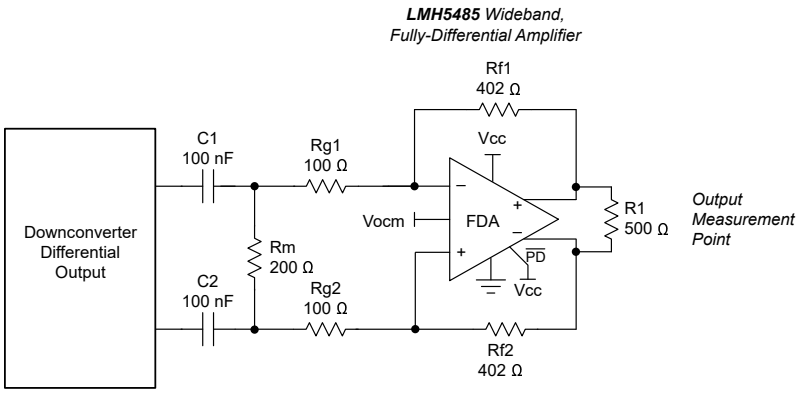

図 9-2. Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the LMH5485-SP

The DC biasing here is very simple. The output Vocm is set by the input control voltage. Because there is no DC current path for the output common-mode voltage, that DC bias also sets the input pins common-mode operating points.

Transformer input coupling allows either a single-ended or differential source to be coupled into the LMH5485-SP, which also improves the input-referred noise figure. These designs assume a source impedance that must be matched in the balun interface. 図 9-3 shows the simplest approach where an example 1:2 turns ratio step-up transformer is used from a 50 Ω source.

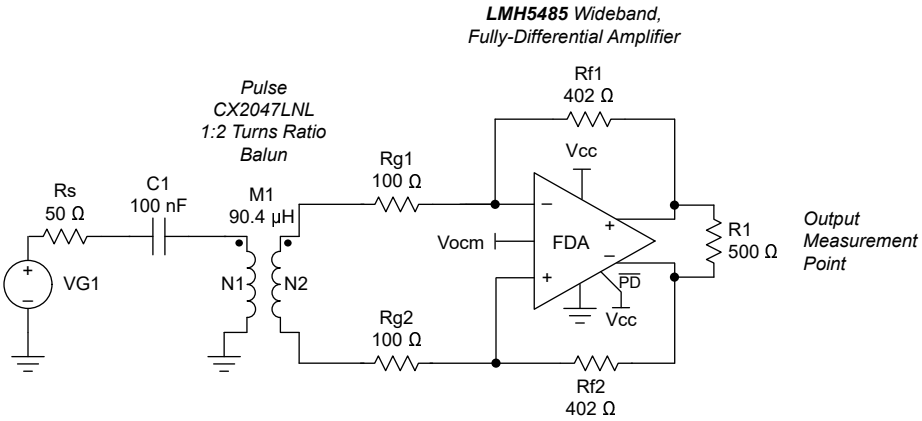

図 9-3. Input Balun Interface Delivers a Differential Input to the LMH5485-SP

In this example, this 1:2 turns ratio step-up transformer provides a source and load match from the 50 Ω source if the secondary is terminated in 200 Ω (turns-ratio squared is the impedance ratio across a balun). The two Rg elements provide that termination as they sum to the differential virtual ground at the FDA summing junctions. The input blocking cap (C1) is optional and included only to eliminate DC shorts to ground from the source. This solution often improves the input-referred noise figure more so than just the FDA using this passive (zero power dissipation) input balun. Defining a few ratios allows a noise figure expression to be written as 式 8:

$$NF = 10 \cdot \mathrm{Log}\left(1 + \frac{(1+\beta^2)}{\beta^2} + \frac{8}{\alpha\beta^2} + \frac{4}{(\alpha\beta)^2} + \frac{\left(\frac{e_{ni}}{\beta n} \cdot \left(\frac{1}{2} + \frac{1}{\alpha}\right)\right)^2 + \frac{1}{2}\frac{(n \cdot i_n \cdot Rs)^2}{\beta^2}}{kTRs}\right) \quad (8)$$

where

- n ≡ turns ratio (the ohms ratio is then n^2)
- α ≡ differential gain in the FDA = Rf / Rg
- β ≡ transformer insertion loss in V/V (from a dB insertion loss, convert to linear attenuation = β)
- kT = 4e-21J at 290 K (17°C)

One way to use 式 8 is to fix the input balun selection, and then sweep the FDA gain by stepping up the Rf value. The lowest-noise method uses just the two Rg elements for termination matching (no Rm element, such as in 図 9-3) and sweep the Rf values up to assess the resulting input-referred noise figure. While this method can be used with all FDAs and a wide range of input baluns, relatively low-frequency input baluns are an appropriate choice here because the LMH5485-SP holds exceptional SFDR for less than 40 MHz applications. Two representative selections, with their typical measured spans and resulting model elements, are shown in 表 9-2. For these two selections, the critical inputs for the noise figures are the turns ratio and the insertion loss (the 0.2 dB for the CX2014LNL becomes a β = 0.977 in the NF expression).

表 9-2. Example Input Step-Up Baluns and Associated Parameters

PART NUMBER	Rs (Ω)	–1-dB FREQUENCY (MHz)		INSERTION LOSS (dB)	MFR	NO. OF DECADES		–3-dB FREQUENCY (MHz)		TURNS RATIO	MODEL ELEMENTS			
		MIN	MAX			–1-dB POINTS	–3-dB POINTS	MIN	MAX		L1 (µH)	L2 (µH)	k	M (µH)
ADT2-1T	50	0.1	463	0.3	MiniCircuits	3.67	4.22	0.05	825	1.41	79.57747	158.50797	0.99988	112.19064
CX2047LNL	50	0.083	270	0.2	Pulse Eng	3.51	3.93	0.044	372	2	90.42894	361.71578	0.99976	180.81512

Using the typical input referred noise terms for the LMH5485-SP (e_{ni} = 2.2 nV and i_n = 1.9 pA) and sweeping the total gain from the input of the balun to the differential output over a 10-dB to 24-dB span, gives the input noise figure shown in 図 9-4.

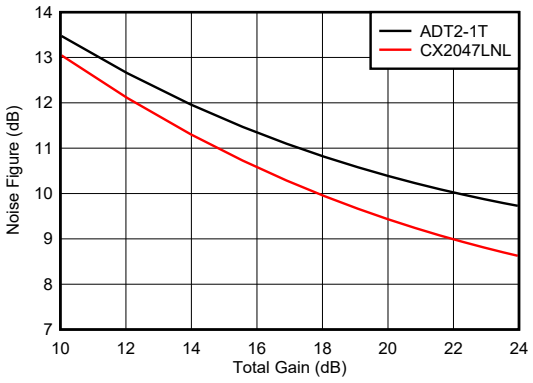

図 9-4. Noise Figure vs Total Gain with the Two Input Baluns of Table 9-2

The 50 Ω referred noise figure estimates show a decreasing input-referred noise for either balun as the gain increases through 24 dB. The only elements changing in these sweeps are the feedback-resistor values, to achieve the total target gain after the step up from the input balun. The example of 図 9-3 is a gain of 7.86 V/V, or a 17.9-dB gain where a 10.0-dB input noise figure is predicted from 図 9-4. Another advantage for this method is that the effective noise gain (NG) is reduced by the source impedance appearing as part of the total Rg element in the design. The example of 図 9-3 operates with a NG = 1 + 402 / (100 + 100) = 3 V/V, giving greater than 300 MHz SSBW in the LMH5485-SP portion of the design. Combining that with the 372 MHz in the balun itself gives greater than 200 MHz in this 18-dB gain stage; or an equivalent greater than 1.6-GHz gain bandwidth product in a low-power, high dynamic range interface.

Added features and considerations for the balun input of 図 9-3 include:

- Many of these baluns offer a secondary centertap. Leave the centertap unconnected for the best HD2 suppression and DC biasing (do not include a capacitor from this centertap to ground).

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- With a floating secondary centertap, the input pins common-mode voltage again equals the output Vocm setting because there is no DC path for the output common-mode voltage to create a common-mode current (I_{CM}).

10 Power Supply Recommendations

The LMH5485-SP is principally intended to operate with a nominal single-supply voltage of +3 V to +5 V. Supply decoupling is required, as described in the *Layout Guidelines*. The amplifier signal path is flexible for single or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used, as long as the total supply across the LMH5485-SP is less than 5.25 V and the required input, output, and common-mode pin headrooms to each supply are observed. Left open, the Vocm pin defaults to near mid-supply for any combination of split or single supplies used. The disable pin is negative-rail referenced. Using a negative supply requires the disable pin to be pulled down to within 0.7 V of the negative supply to disable the amplifier.

11 Layout

11.1 Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with a close attention to board layout. The LMH5485-SP evaluation module (EVM) shows a good example of high frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that may not apply to some applications. General high-speed, signal-path layout suggestions include the following:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, ground and power planes around the capacitive sensitive input and output device pins should be open. After the signal is sent into a resistor, the parasitic capacitance becomes more of a band limiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. A supply decoupling capacitor across the two power supplies (for bipolar operation) should also be added. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- For each LMH5485-SP, attach a separate 0.1 µF capacitor to a nearby ground plane. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor is often useful to the local high-frequency decoupling capacitor.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Connect any Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the Rg elements can have more trace length if needed to the source or to ground.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Design for a Wideband, Differential Transimpedance DAC Output* application report
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide
- Texas Instruments, *LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier* data sheet
- Texas Instruments, *LMH5485-SP-EVM* user guide
- Texas Instruments, *Maximizing the dynamic range of analog front ends having a transimpedance amplifier* technical brief

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

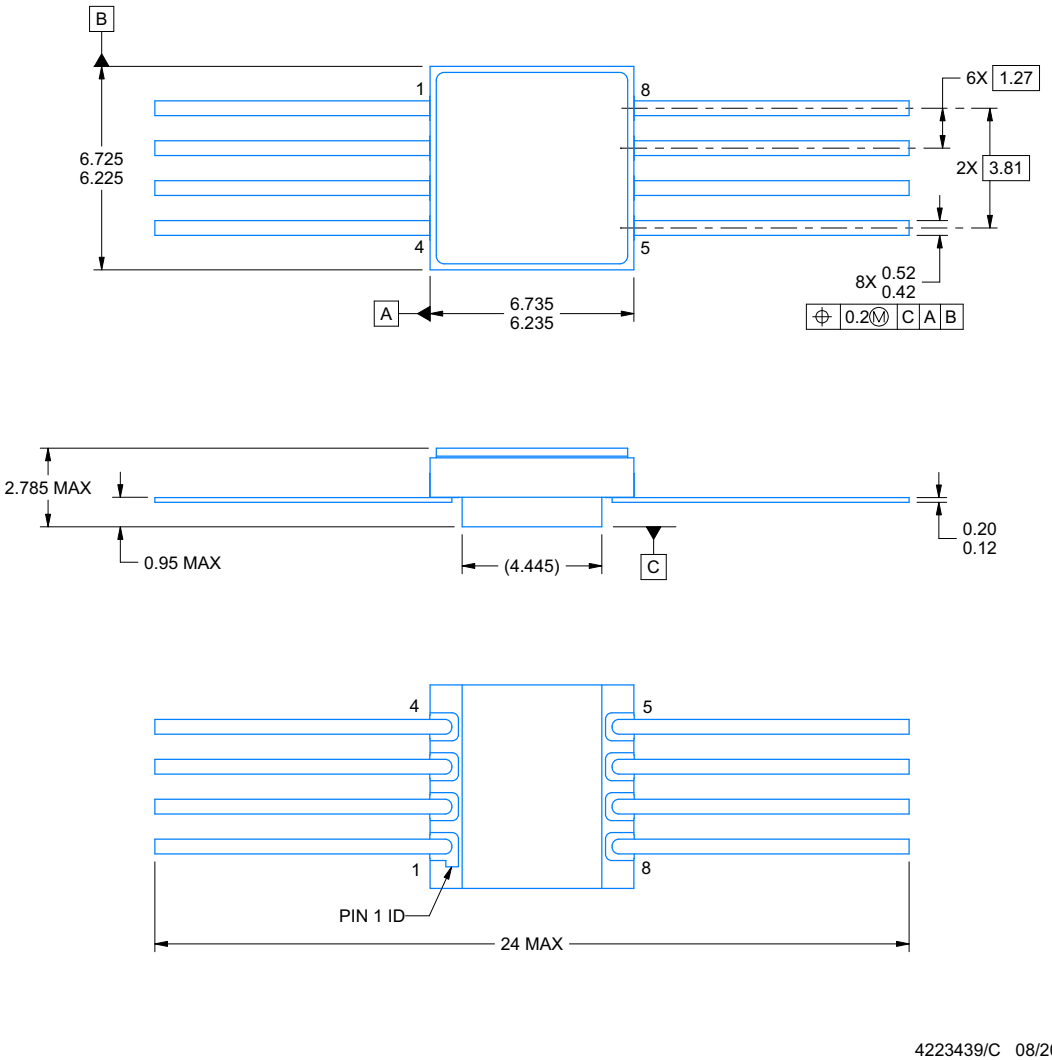
ADVANCE INFORMATION

PACKAGE OUTLINE

HKX0008A

CFP - 2.785 mm max height

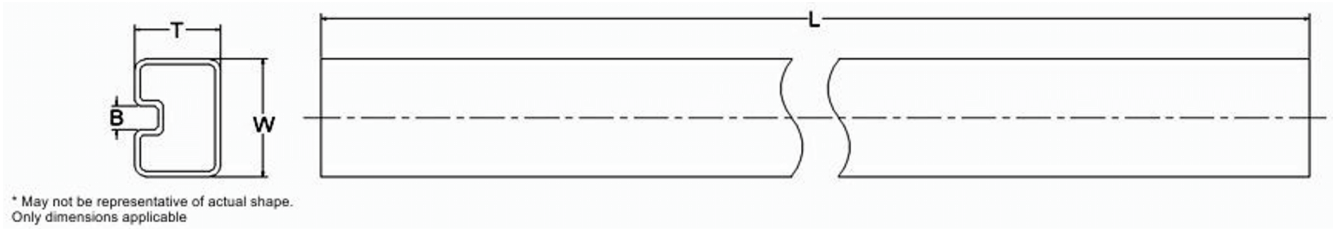
CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated.

13.1 Tube Information



* May not be representative of actual shape.
Only dimensions applicable

Device	Package Type	Package Name	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH5485HKX/EM	CFP	HKX	8	1	506.98	26.16	6220	NA

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLMH5485HKX/EM	Active	Preproduction	CFP (HKX) | 8	25 | TUBE	-	Call TI	Call TI	25 to 25	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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