

LME49743 Quad High Performance, High Fidelity Audio Operational Amplifier

Check for Samples: [LME49743](#)

FEATURES

- Easily Drives 600Ω Loads
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection
- 98dB (Typ) PSRR and 106dB (Typ) CMRR
- TSSOP Package

APPLICATIONS

- Audio Amplifiers and Preamplifiers
- Professional Audio
- Equalization and Crossover Networks
- Line Drivers and Receivers
- Active Filters

DESCRIPTION

The LME49743 is a low distortion, low noise, high slew rate operational amplifier optimized and fully specified for high performance, high fidelity applications. The LME49743 audio operational amplifier delivers superior audio signal amplification for outstanding audio performance. The LME49743 combines low voltage noise density (3.5nV/√Hz) and THD+N (0.0001%) to easily satisfy demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49743 has a slew rate of ±12V/μs and an output current capability of ±21mA.

The LME49743's outstanding CMRR(106dB), PSRR(98dB), and V_{OS} (±0.15mV) give the amplifier excellent operational amplifier DC performance.

The LME49743 has a wide supply range of ±4.0V to ±17V. Over this supply range the LME49743's input circuitry maintains excellent common-mode, power supply rejection, and low input bias current. The LME49743 is unity gain stable.

The LME49743 is available in 14-lead TSSOP.

Table 1. Key Specifications

		VALUE	UNIT
Power Supply Voltage Range		±4.0V to ±17	V
THD+N ($A_V = 1$, $V_{OUT} = 3V_{RMS}$, $f_{IN} = 1kHz$)	$R_L = 2k\Omega$	0.0001	% (typ)
	$R_L = 600\Omega$	0.0001	% (typ)
Input Noise Density		3.5	nV/√Hz (typ)
Slew Rate		±12	V/μs (typ)
Gain Bandwidth Product		30	MHz (typ)
Open Loop Gain ($R_L = 600\Omega$)		110	dB (typ)
Input Bias Current		190	nA (typ)
Input Offset Voltage		±0.15	mV (typ)



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Connection Diagram

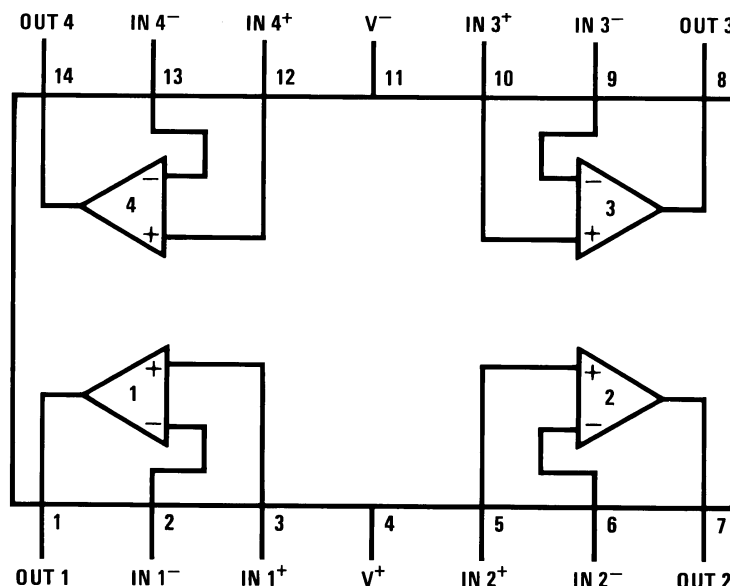


Figure 1. TSSOP Package
See Package Number PW0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾⁽³⁾

Power Supply Voltage	$(V_S = V^+ - V^-)$	36V
Storage Temperature		-65°C to 150°C
Input Voltage		$(V^-) - 0.7V$ to $(V^+) + 0.7V$
Output Short Circuit ⁽⁴⁾		Continuous
Power Dissipation		Internally Limited
ESD Susceptibility ⁽⁵⁾		750V
ESD Susceptibility ⁽⁶⁾		175V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (MT)	140°C/W
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ 85°C
Supply Voltage Range		$\pm 4.0V \leq V_S \leq \pm 17V$

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
- (2) *Operating Ratings* indicate conditions for which the device is functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (3) If Military/Aerospace specifications are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) Amplifier output connected to GND, any number of amplifiers within a package.
- (5) Human body model, 100pF discharged through a 1.5kΩ resistor.
- (6) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $R_L = 2k\Omega$, $f_{IN} = 1kHz$, and $T_A = 25^\circ C$, unless otherwise specified. ⁽¹⁾⁽²⁾

Parameter		Test Conditions	LME49743		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾⁽⁵⁾	
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$, $V_{OUT} = 3V_{RMS}$ $R_L = 2k\Omega$ $R_L = 600\Omega$	0.0001 0.0001	0.0002	% (max)
IMD	Intermodulation Distortion	$A_V = 1$, $V_{OUT} = 3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1	0.0005		% (max)
GBWP	Gain Bandwidth Product		30	25	MHz (min)
SR	Slew Rate		12	9.5	V/ μs (min)
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}$, -3dB referenced to output magnitude at $f = 1kHz$	10		MHz
t_s	Settling time	$A_V = 1$, 10V step, $C_L = 100pF$ 0.1% error range	1.2		μs
e_n	Equivalent Input Noise Voltage	$f_{BW} = 20Hz$ to 20kHz	0.48	0.65	μV_{RMS}
	Equivalent Input Noise Density	$f = 1kHz$ $f = 10Hz$	3.5 6.4	4.5	$nV/\sqrt{Hz}$ (max) $nV/\sqrt{Hz}$
i_n	Current Noise Density	$f = 1kHz$	1.6		$pA/\sqrt{Hz}$
		$f = 10Hz$	3.1		$pA/\sqrt{Hz}$
V_{OS}	Offset Voltage		± 0.15	± 1.0	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	$40^\circ C \leq T_A \leq 85^\circ C$	0.05		$\mu V/^\circ C$
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	$\Delta V_S = 20V^{(6)}$	98	94	dB (min)
ISO _{CH-CH}	Channel-to-Channel Isolation	$f_{IN} = 1kHz$	118		dB
		$f_{IN} = 20kHz$	112		dB
I_B	Input Bias Current	$V_{CM} = 0V$	190	250	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	$-40^\circ C \leq T_A \leq 85^\circ C$	0.05		nA/ $^\circ C$
I_{OS}	Input Offset Current	$V_{CM} = 0V$	7	40	nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		± 13.2	(V+)-2.0 (V-)+2.0	V (min) V (min)
CMRR	Common-Mode Rejection	$-10V < V_{CM} < 10V$	106	98	dB (min)
Z_{IN}	Differential Input Impedance		30		k Ω
	Common Mode Input Impedance	$-10V < V_{CM} < 10V$	1000		M Ω
A_{VOL}	Open Loop Voltage Gain	$-10V < V_{OUT} < 10V$, $R_L = 600\Omega$	110		dB (min)
		$-10V < V_{OUT} < 10V$, $R_L = 2k\Omega$	110		dB (min)
		$-10V < V_{OUT} < 10V$, $R_L = 10k\Omega$	110	100	dB (min)
V_{OUTMAX}	Maximum Output Voltage Swing	$R_L = 600\Omega$	± 12.4	± 12.0	V (min)
		$R_L = 2k\Omega$	± 13.0		V (min)
		$R_L = 10k\Omega$	± 13.0		V (min)
I_{OUT}	Output Current	$R_L = 600\Omega$, $V_S = \pm 17V$	± 21	± 20	mA (min)
I_{OUT-CC}	Short Circuit Current		+30 -38		mA mA

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.

(2) Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(3) Typical specifications are specified at $+25^\circ C$ and represent the most likely parametric norm.

(4) Tested limits are ensured to Texas Instrument's AOQL (Average Outgoing Quality Level).

(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

(6) PSRR is measured as follows: V_{OS} is measured at two supply voltages, $\pm 5V$ and $\pm 15V$. $PSRR = |20\log(\Delta V_{OS}/\Delta V_S)|$.

Electrical Characteristics (continued)

The following specifications apply for $V_S = \pm 15V$, $R_L = 2k\Omega$, $f_{IN} = 1kHz$, and $T_A = 25C$, unless otherwise specified.⁽¹⁾⁽²⁾

Parameter		Test Conditions	LME49743		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾⁽⁵⁾	
R_{OUT}	Output Impedance	$f_{IN} = 10kHz$ Closed-Loop Open-Loop	0.01 13		Ω Ω
C_{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I_S	Total Quiescent Current	$I_{OUT} = 0mA$	10	14	mA (max)

Typical Performance Characteristics

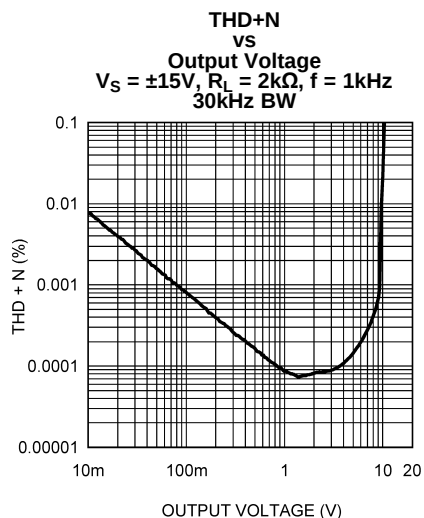


Figure 2.

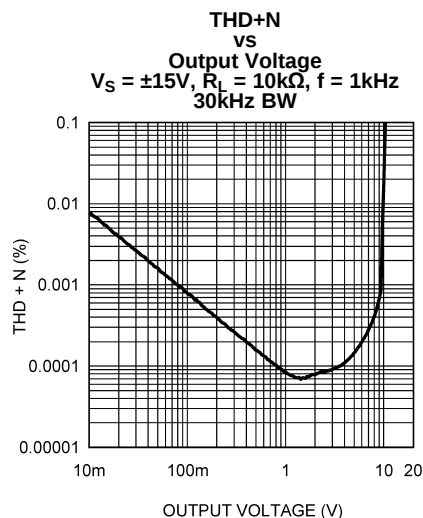


Figure 3.

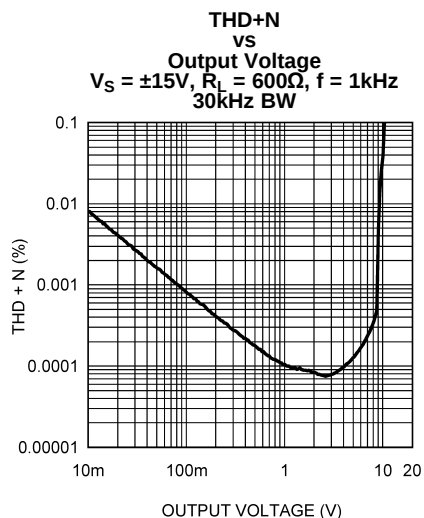


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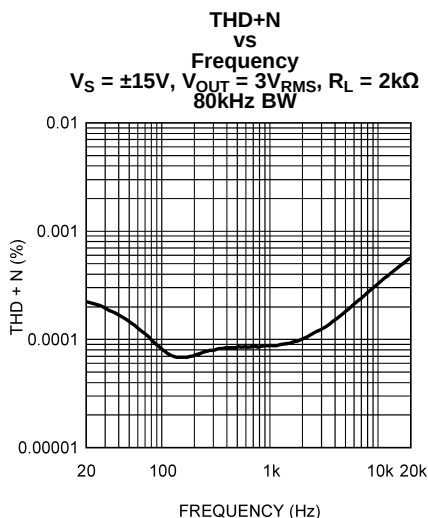


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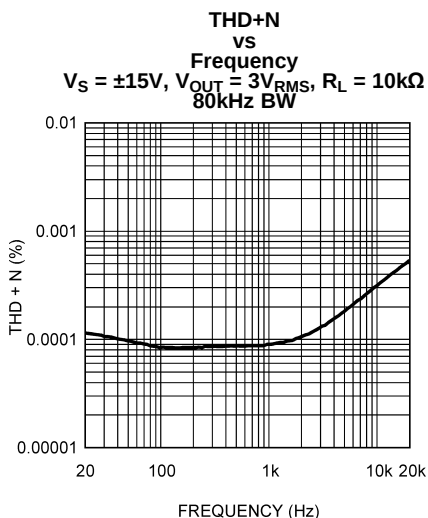


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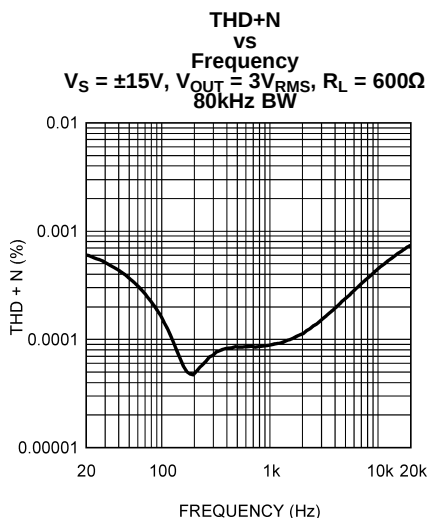


Figure 7.

Typical Performance Characteristics (continued)

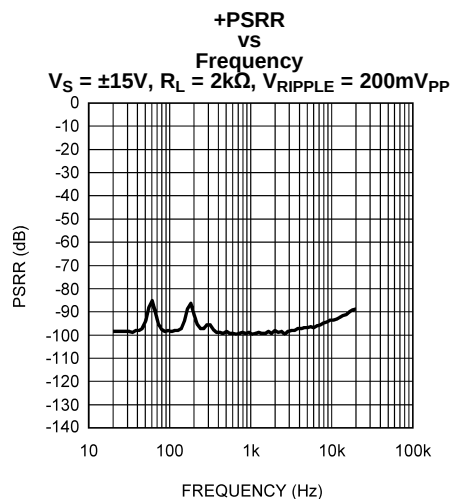


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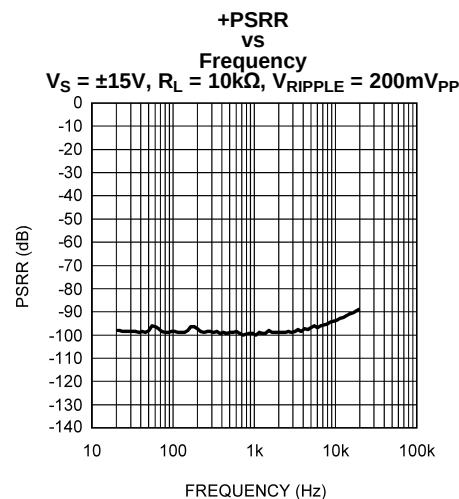


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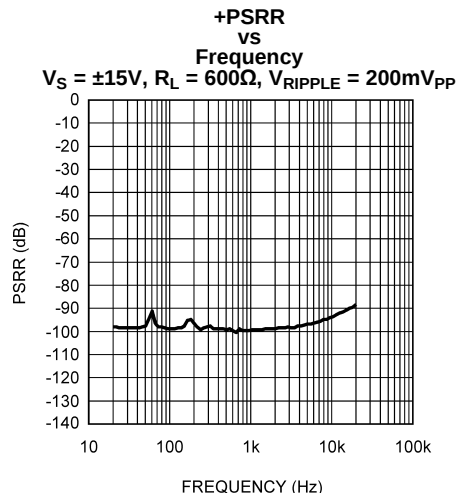


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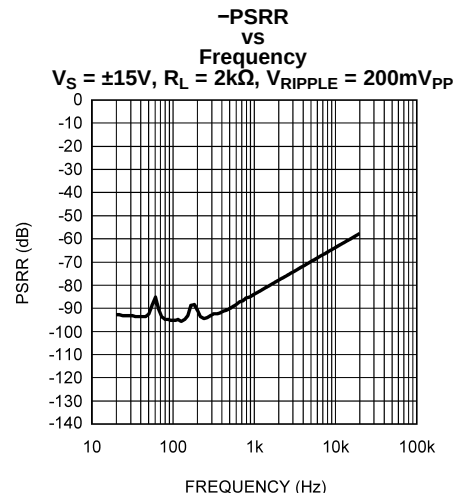


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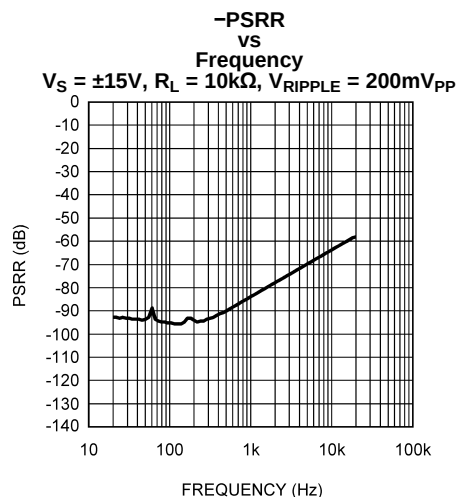


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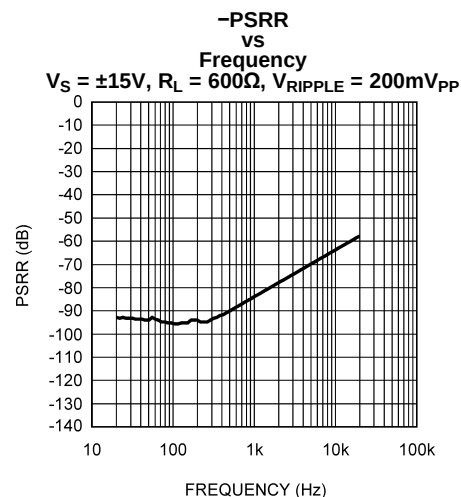


Figure 13.

Typical Performance Characteristics (continued)

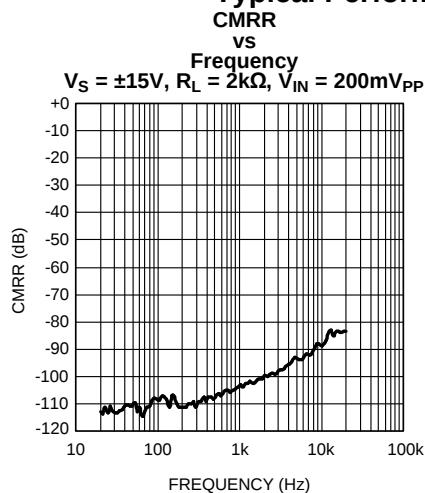


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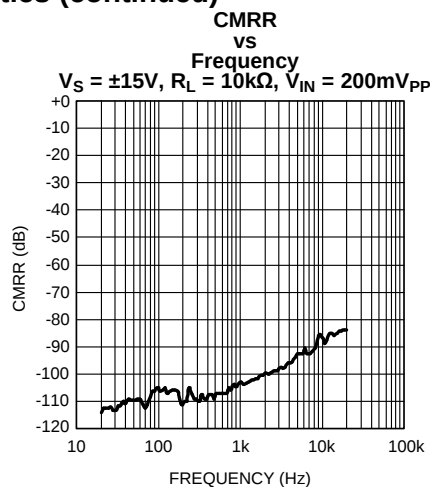


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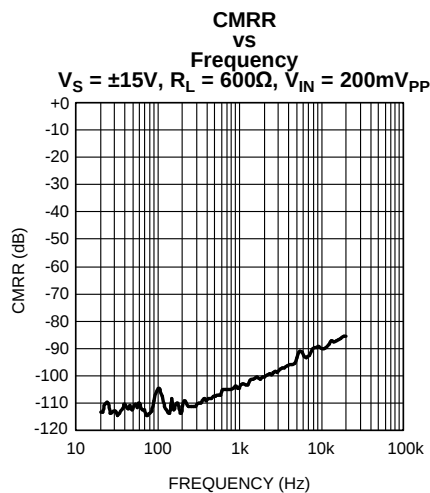


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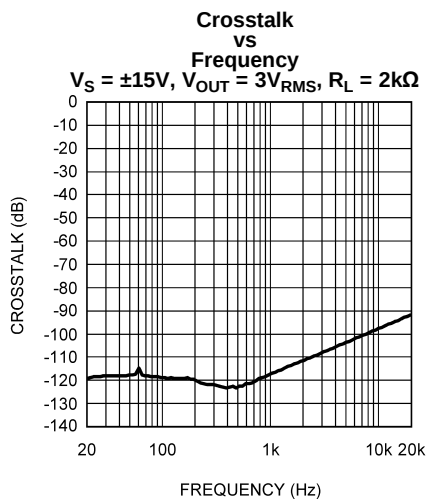


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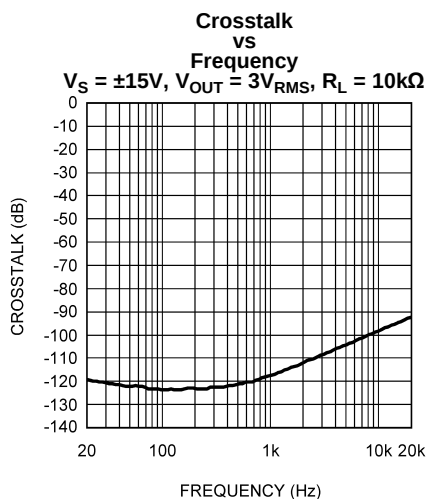


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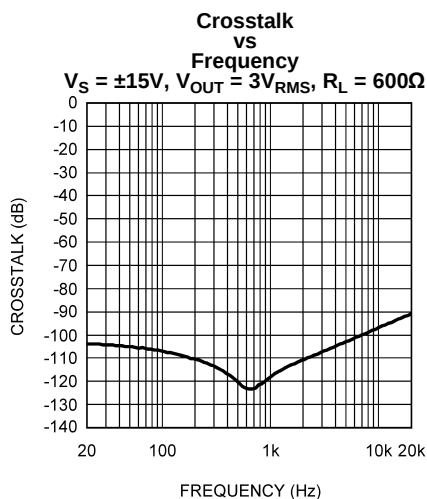


Figure 19.

Typical Performance Characteristics (continued)

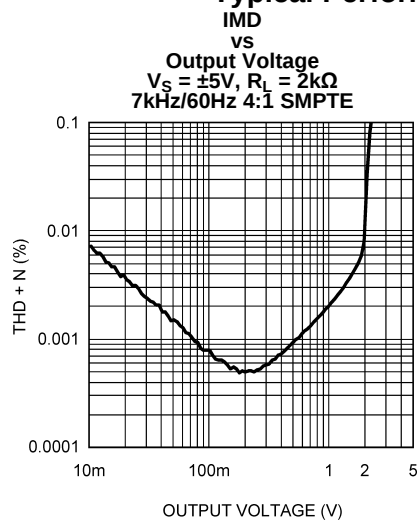


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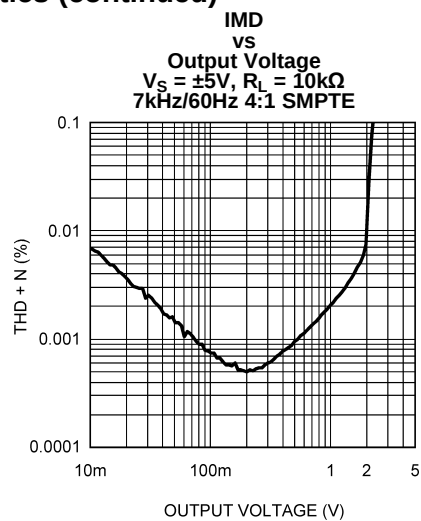


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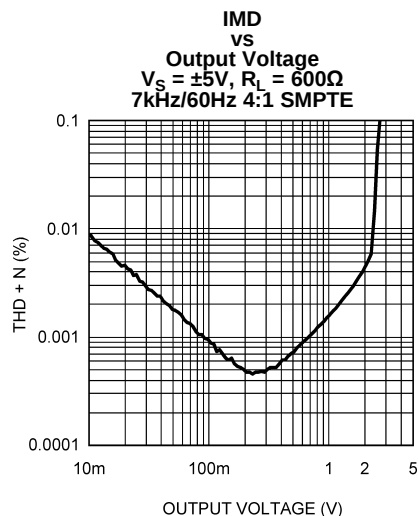


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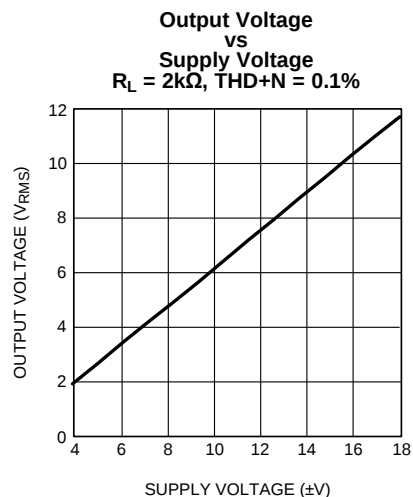


Figure 23.

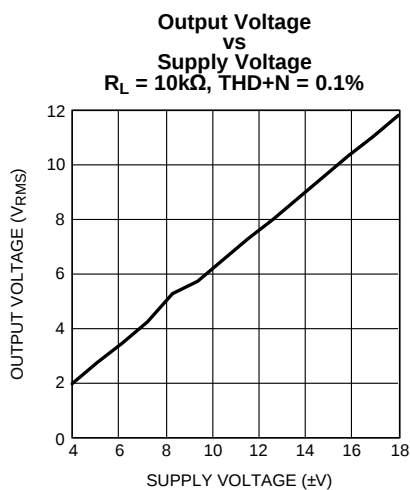


Figure 24.

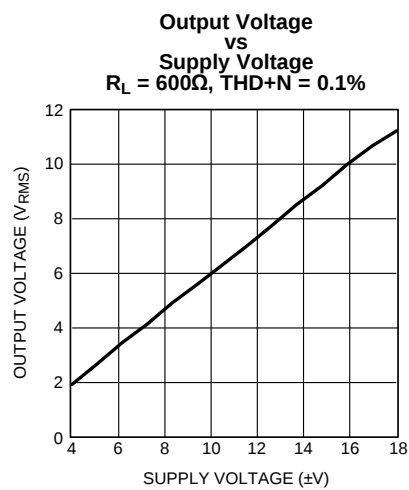


Figure 25.

Typical Performance Characteristics (continued)

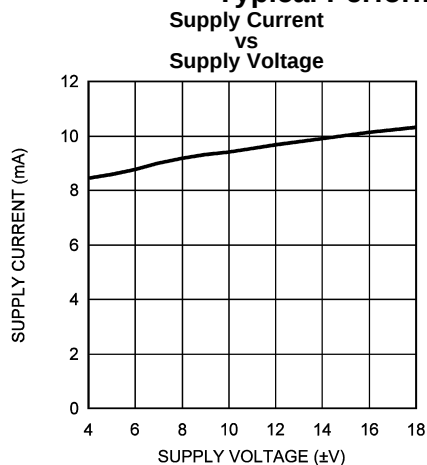


Figure 26.

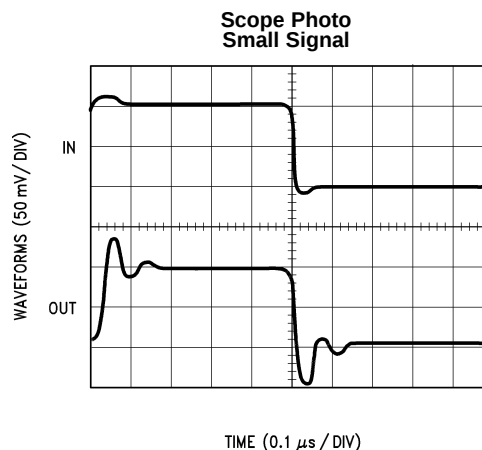


Figure 27.

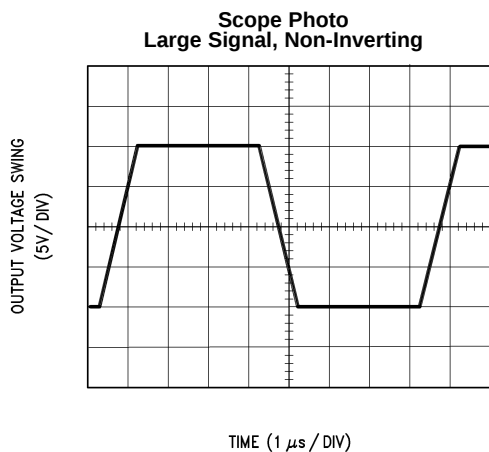


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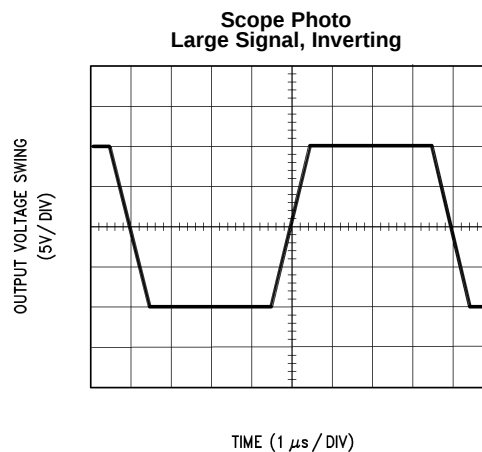


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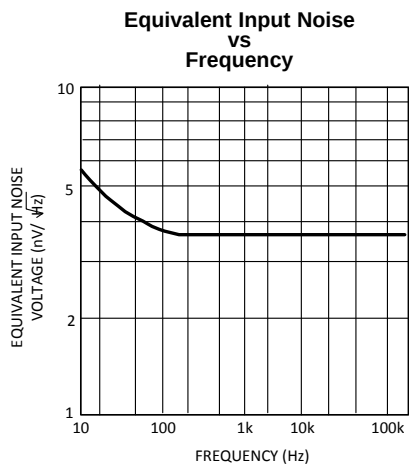


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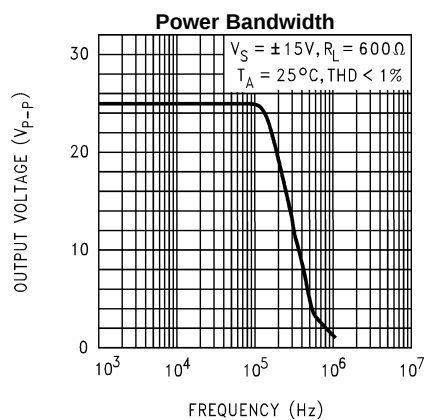


Figure 31.

Typical Performance Characteristics (continued)

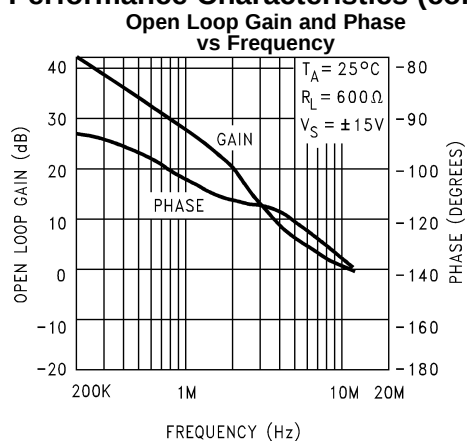


Figure 32.

APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49743 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49743's low residual distortion is an input referred internal error. As shown in Figure 33, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 33.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

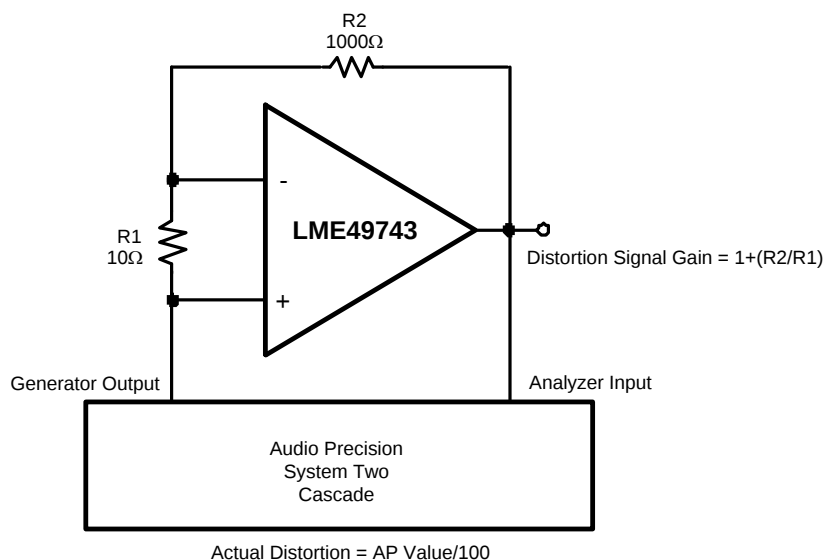


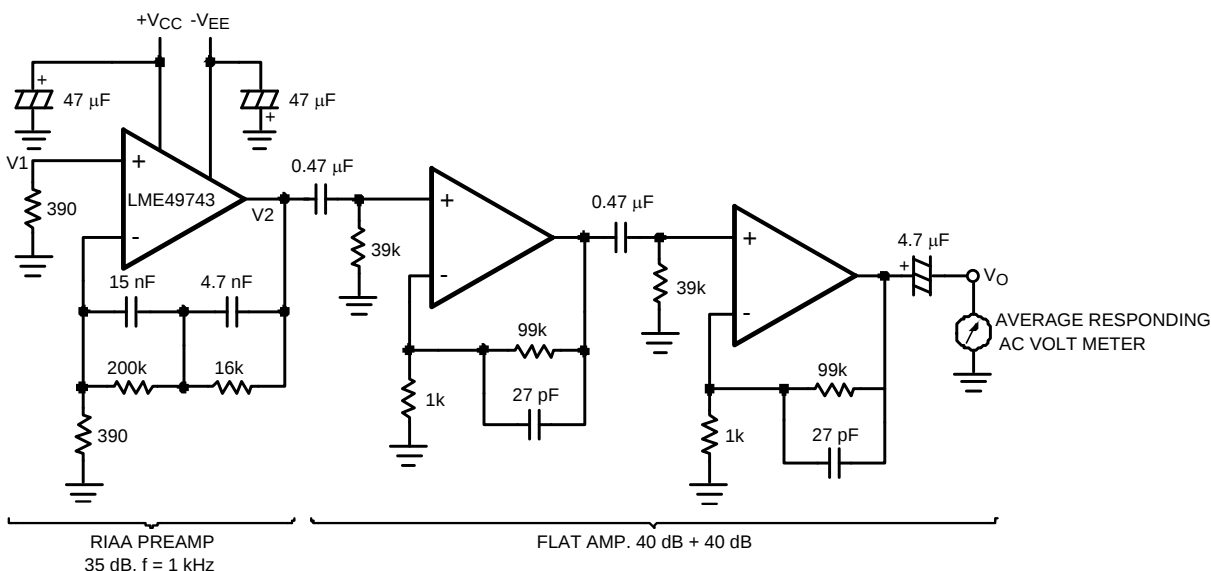
Figure 33. THD+N and IMD Distortion Test Circuit

Application Hints

The LME49743 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit



- (1) Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.
- (2) Total Gain: 115 dB at $f = 1$ kHz
- (3) Input Referred Noise Voltage: $e_n = V_O/560,000$ (V)

Figure 34.

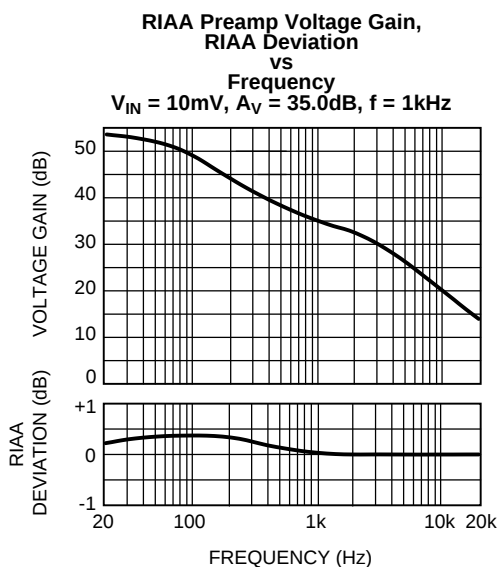


Figure 35.

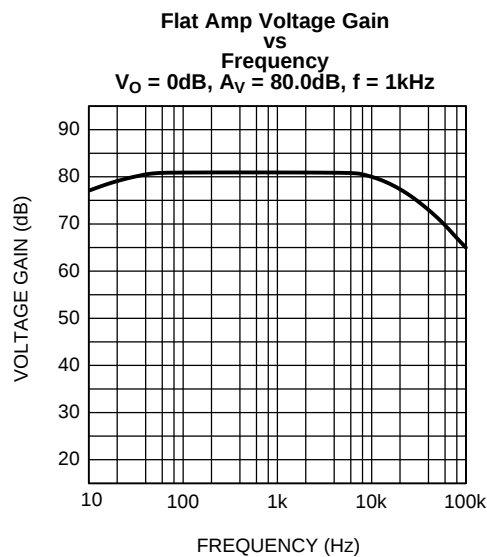
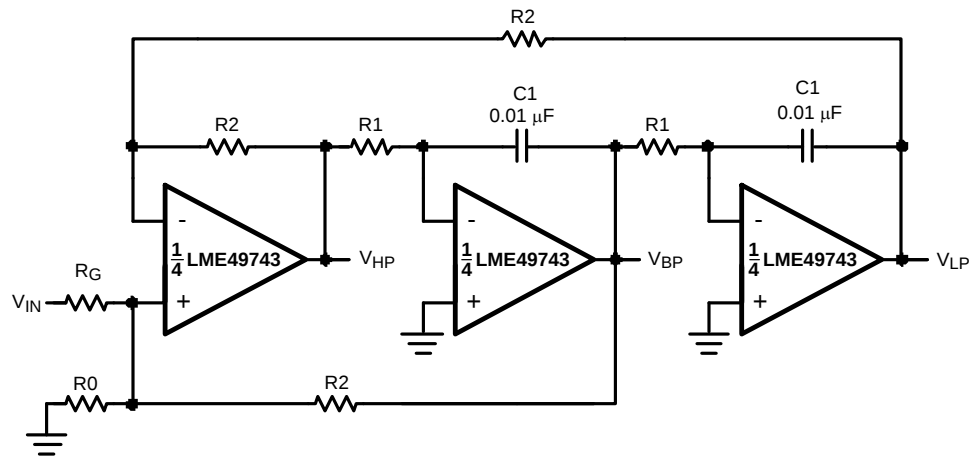


Figure 36.

Typical Applications



$$f_0 = \frac{1}{2\pi C_1 R_1}, Q = \frac{1}{2} \left(1 + \frac{R_2}{R_0} + \frac{R_2}{R_G} \right), A_{BP} = Q A_{LP} = Q A_{LH} = \frac{R_2}{R_G}$$

Figure 37. State Variable Filter

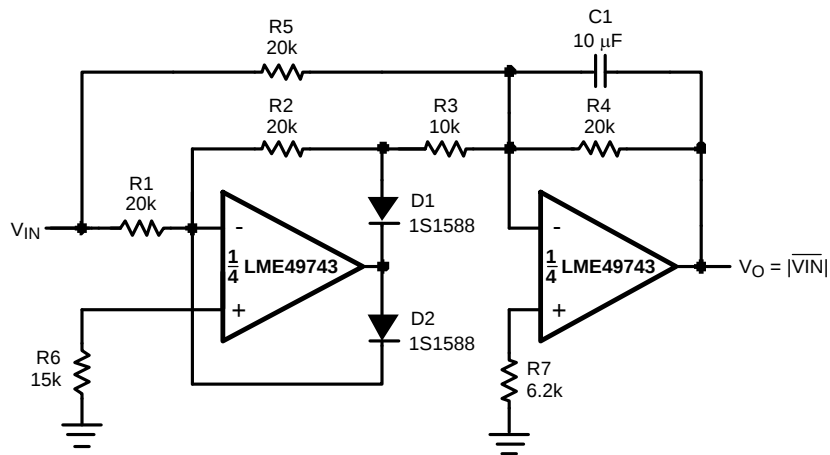


Figure 38. AC-DC Converter

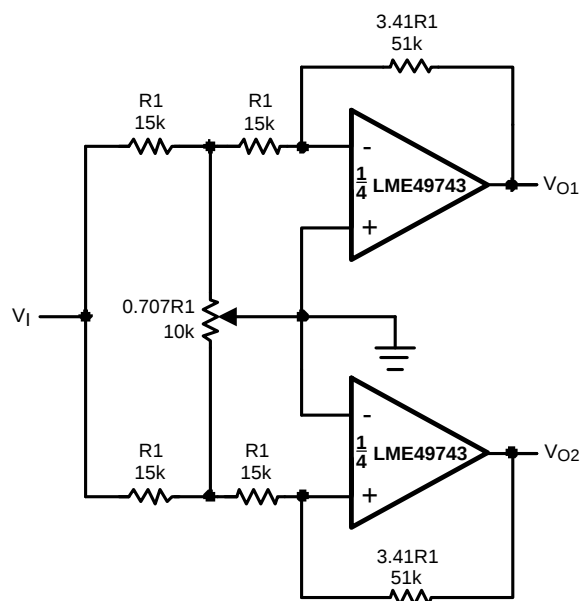


Figure 39. 2 Channel Panning Circuit (Pan Pot)

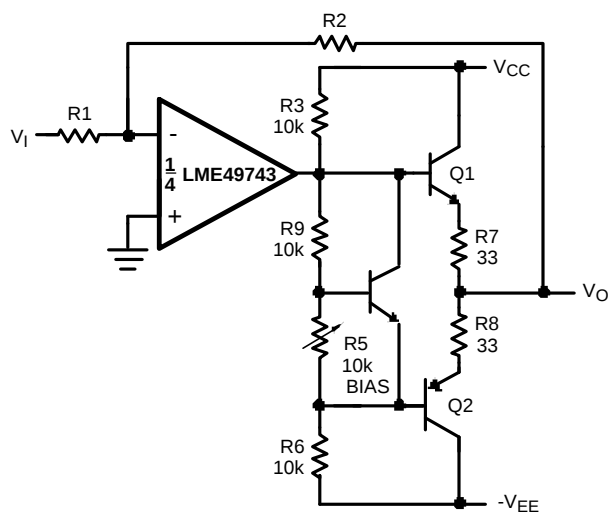
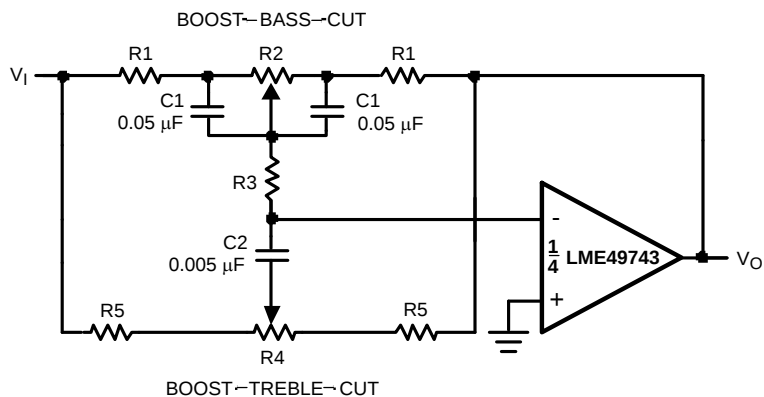


Figure 40. Line Driver



$$f_L = \frac{1}{2\pi R_2 C_1}, f_{LB} = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_5 C_2}, f_{HB} = \frac{1}{2\pi (R_1 + R_5 + 2R_3) C_2}$$

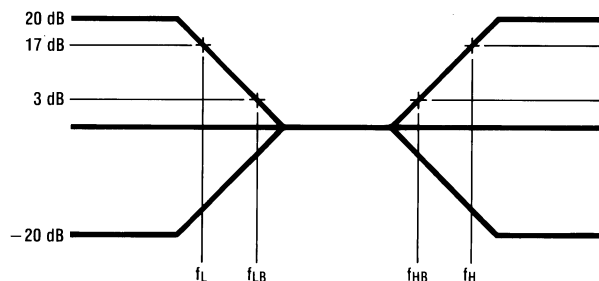
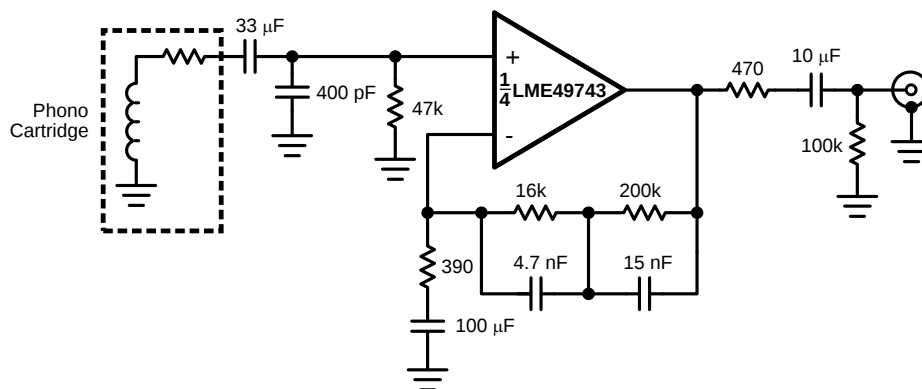
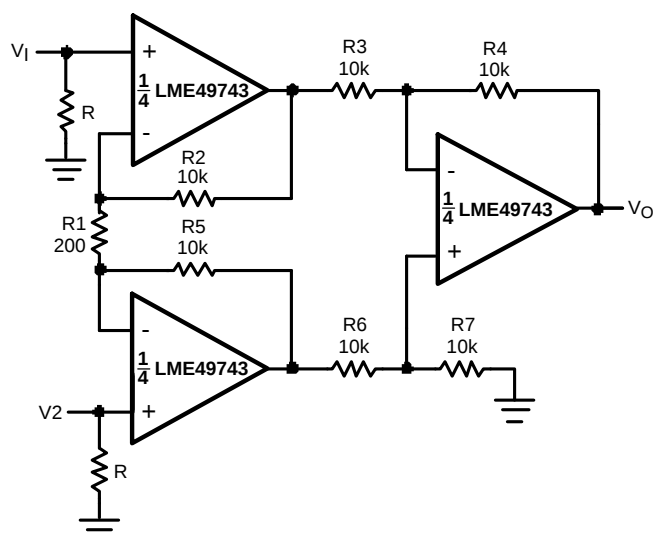


Figure 41. Tone Control



$A_v = 35 \text{ dB}$
 $E_n = 0.33 \text{ } \mu\text{V}$
 $S/N = 90 \text{ dB}$
 $f = 1 \text{ kHz}$
 A Weighted
 A Weighted, $V_{IN} = 10 \text{ mV}$
 at $f = 1 \text{ kHz}$

Figure 42. RIAA Preamp



If $R_2 = R_5$, $R_3 = R_6$, $R_4 = R_7$

$$V_O = \left(1 + \frac{2R_2}{R_1}\right) \frac{R_4}{R_3} (V_2 - V_1)$$

Illustration is:

$$V_O = 101(V_2 - V_1)$$

Figure 43. Balanced Input Mic Amp

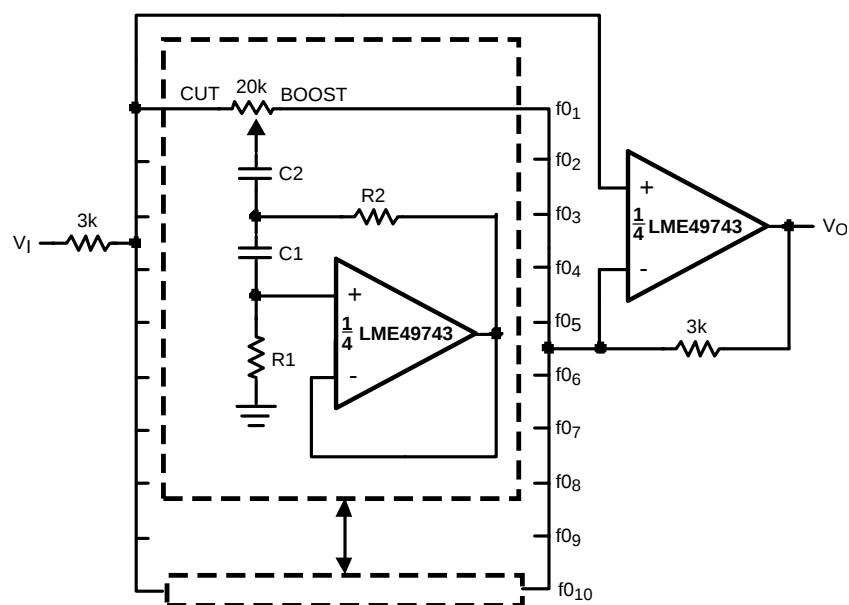


Figure 44. 10 Band Graphic Equalizer

fo (Hz)	C ₁	C ₂	R ₁	R ₂
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

NOTE

At volume of change = ±12 dB

 Q = 1.7

REVISION HISTORY

Rev	Date	Description
1.0	03/26/08	Initial release.
1.01	01/12/09	Fixed a typo.
B	04/04/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LME49743MTX/NOPB	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	L49743 MT
LME49743MTX/NOPB.B	Active	Production	TSSOP (PW) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L49743 MT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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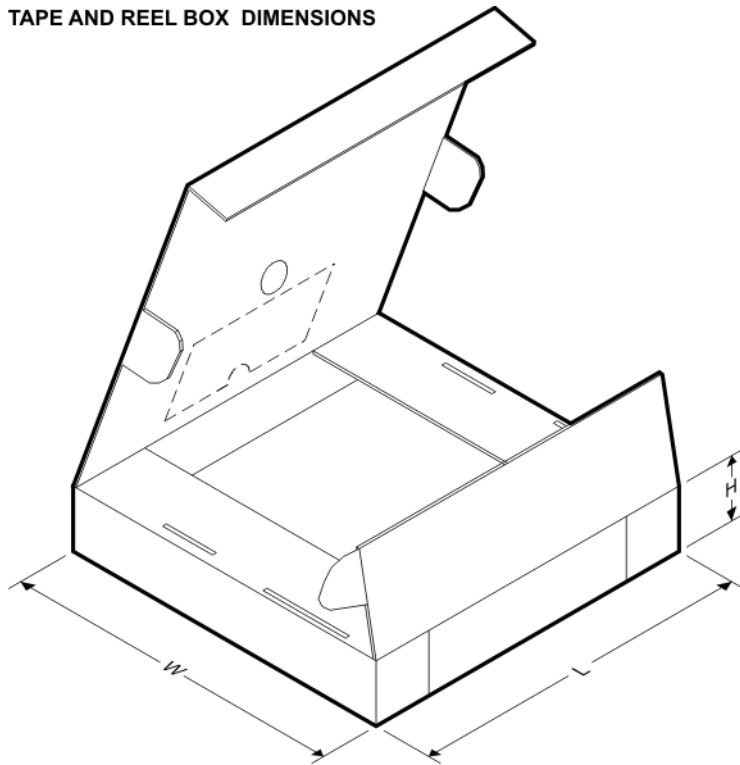
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

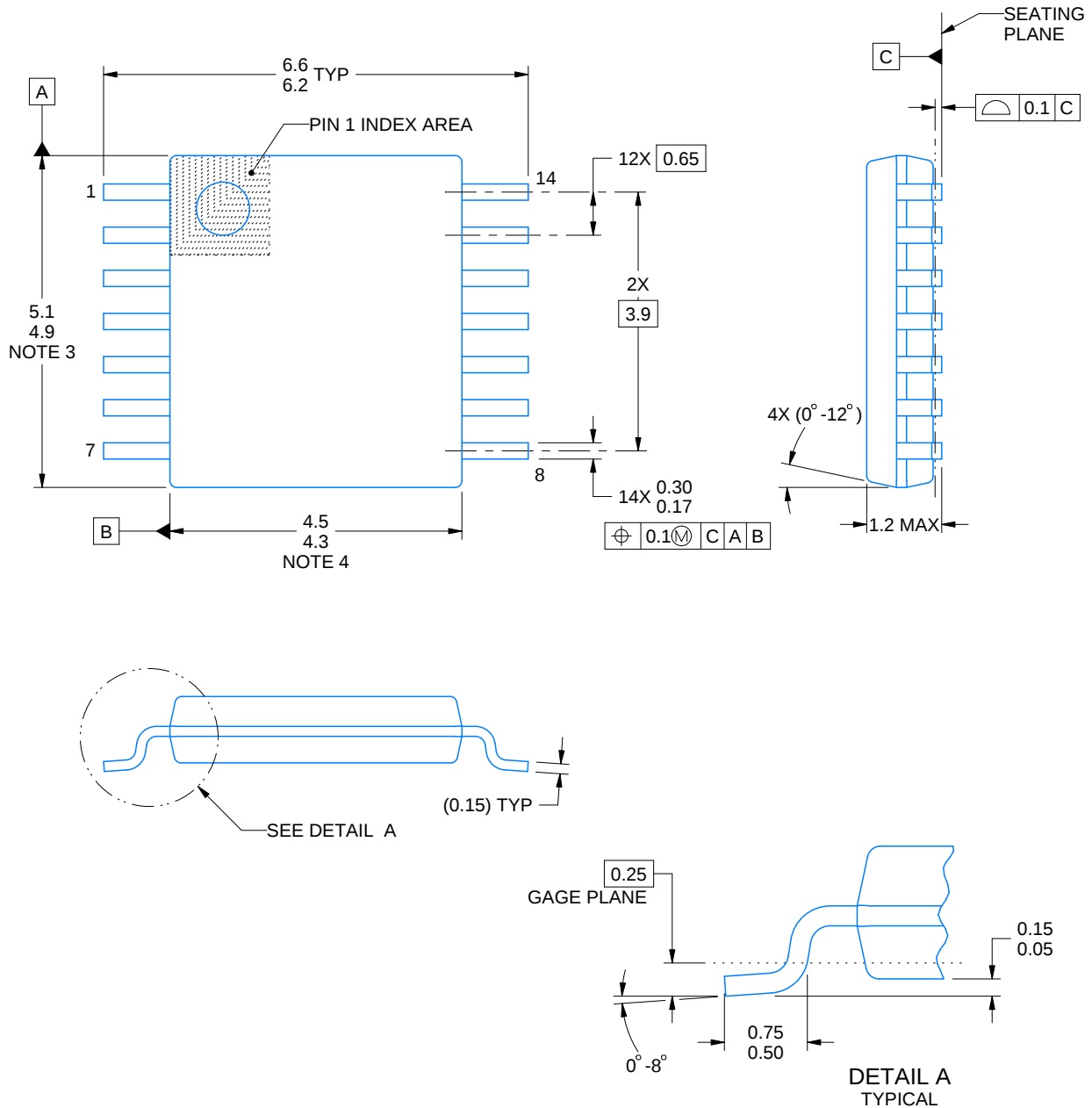
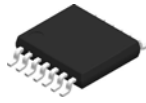
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49743MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49743MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0



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NOTES:

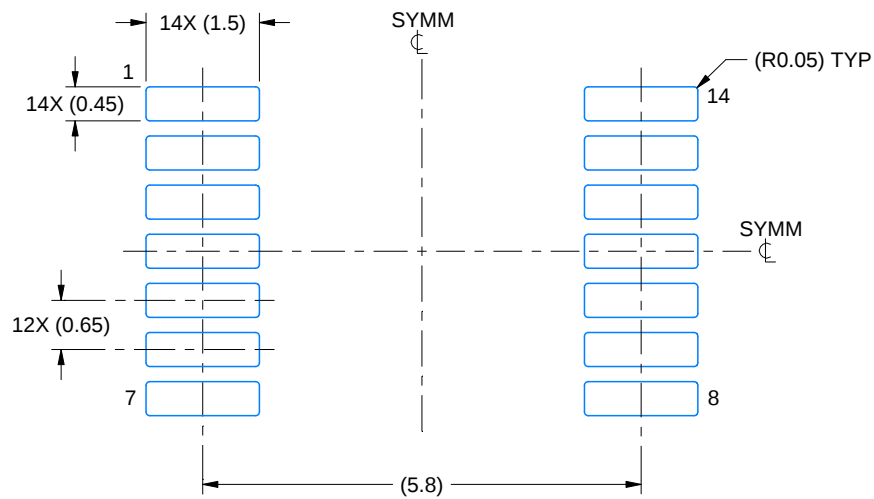
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

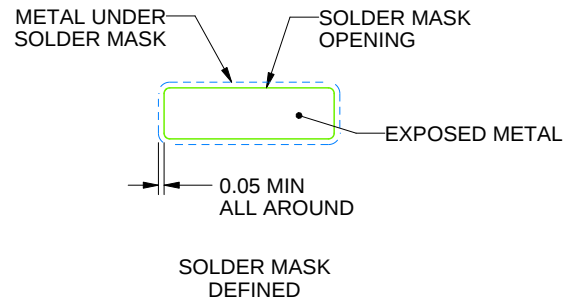
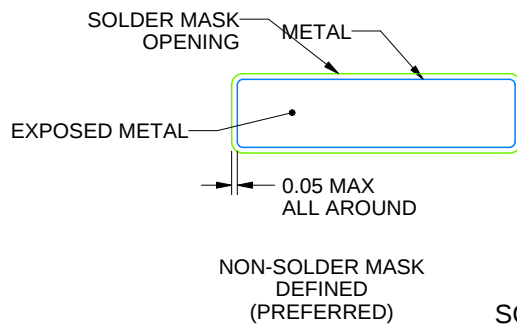
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

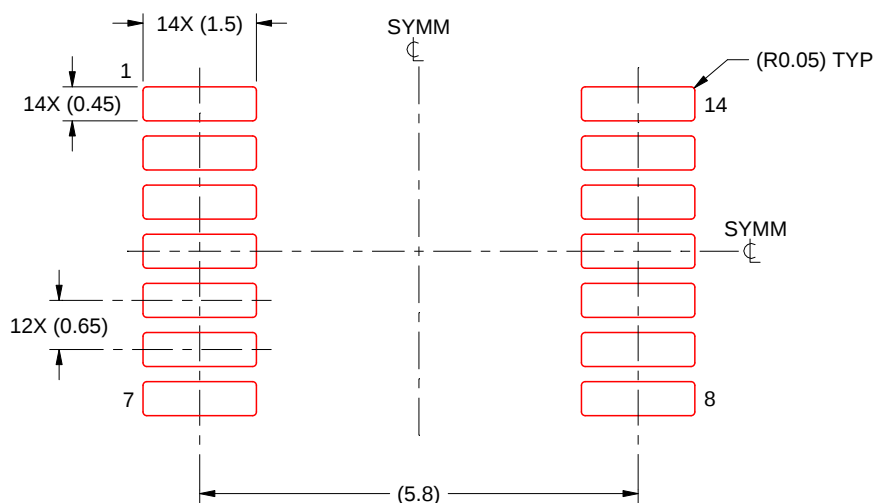
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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