LM8272 Dual RRIO, High Output Current & Unlimited Cap Load Op Amp in Miniature Package

1 Features

(V_S = 12V, T_A = 25°C, Typical values unless specified).

- GBWP 15MHz
- Wide supply voltage range 2.5 V to 24 V
- Slew rate 15 V/µs
- Supply current/channel 0.95 mA
- Cap load tolerance Unlimited
- Output short circuit current ±13 0mA
- Output current (1 V from rails) ±65 mA
- Input common mode voltage 0.3 V beyond rails
- Input voltage noise 15 nV/√Hz
- Input current noise 1.4 pA/√Hz

2 Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

3 Description

The LM8272 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, and unlimited capacitive load drive capability, while requiring only 0.95mA/channel supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50 dB of Common Mode Rejection allows high side and low side sensing among many applications without concerns for exceeding the range and with no compromise in accuracy. An exceptionally wide operating supply voltage range of 2.5 V to 24 V removes any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations. This design enhancement is yet another step in simplifying its usage.

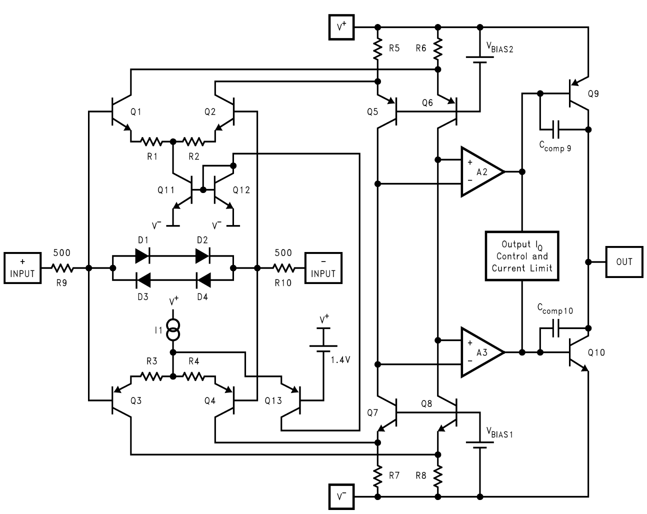
The LM8272 is offered in the 8-pin VSSOP package.

Device Information(1)

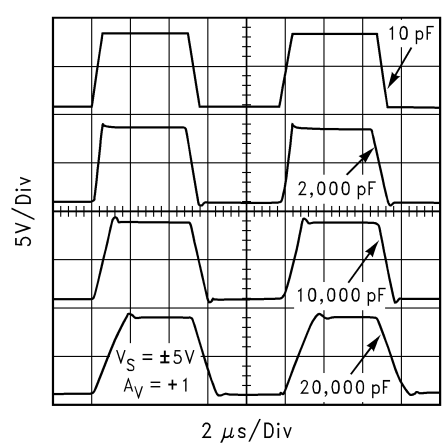
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM8272	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Large Signal Step Response for Various Cap. Load



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2014) to Revision F — **Page**

- Changed pin 5 From: -IN B To: +IN B Non-Inverting Input B in the *Pin Functions* table ... 3
- Changed pin 6 From: +IN B To: -IN B Inverting Input B in the *Pin Functions* table ... 3
- Moved "Storage temperature range" to the *Absolute Maximum Ratings*[(1)(2)] ... 4
- Changed *Handling Ratings* To: *ESD Ratings* ... 4

Changes from Revision D (March 2013) to Revision E — **Page**

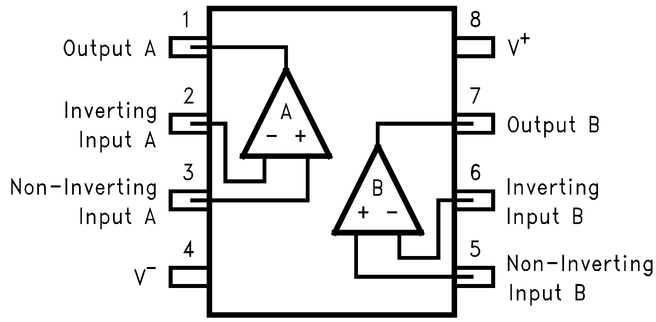
- Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Mechanical, Packaging, and Ordering Information. ... 1
- Deleted T_J = 25°C ... 5
- Deleted T_J = 25°C ... 6

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 18

5 Pin Configuration and Functions

**8-Pin VSSOP
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	Output A
2	-IN A	I	Inverting Input A
3	+IN A	I	Non-Inverting Input A
4	V-	I	Negative Supply
5	+IN B	I	Non-Inverting Input B
6	-IN B	I	Inverting Input B
7	OUT B	O	Output B
8	V+	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN} Differential			+/−10	V
Output Short Circuit Duration			See[3][4]	
Supply Voltage (V^+ - V^-)			27	V
Voltage at Input/Output pins			V^+ +0.3, V^- −0.3	V
Junction Temperature[5]			+150	°C
Storage temperature range, T_{stg}		−65	+150	°C
Soldering Information:	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Output short circuit duration is infinite for VS ≤ 6 V at room temperature and below. For VS > 6 V, allowable short circuit duration is 1.5 ms.
(5) The maximum power dissipation is a function of TJ(max), $R_{θJA,}$ and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ $R_{θJA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]	±2000	V
		Machine Model (MM)[3]	±200	

(1) Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 0 Ω is series with 200 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V^+ - V^-)	2.5		24	V
Operating Temperature Range[1]	−40		+85	°C

(1) The maximum power dissipation is a function of TJ(max), $R_{θJA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ $R_{θJA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC[1]		DGK	UNIT
		8 Pins	
$R_{θJA}$	Junction-to-ambient thermal resistance[2]	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of TJ(max), $R_{θJA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ $R_{θJA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 5V Electrical Characteristics

Unless otherwise specified, all limited ensured for V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 4.5V	+/−0.7	+/−5 **+/− 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 4.5V(3)	+/−2	—	µV/°C
I_B	Input Bias Current	See (4)	—	±2.00 **±2.70**	µA max
I_{OS}	Input Offset Current		20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 5V	80	64 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V	100	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10kΩ to V^+/2	80	64 **60**	dB min
V_O	Output Swing High	R_L = 10kΩ to V^-	4.93	4.85	V min
		I_{SOURCE} = 5mA	4.85	4.70	
	Output Swing Low	R_L = 10kΩ to V^+	215	250	mV max
		I_{SINK} = 5mA	300	350	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV(5)	100	—	mA
		Sinking to V^+ V_{ID} = −200mV(5)	100	—	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±55	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.8	2.3 **2.8**	mA max
SR	Slew Rate(6)	A_V = +1, V_I = $5V_{PP}$	12	—	V/µs
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2KΩ to V^+/2	7.5	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	13	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	55	—	deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	nV/√Hz
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	pA/√Hz
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to V^+/2	700	—	kHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(6) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.6 12V Electrical Characteristics

Unless otherwise specified, all limited ensured for V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 11.5V	+/−0.7	+/−7 **+/− 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 11.5V(3)	+/−2	—	µV/°C
I_B	Input Bias Current	See (4)	—	±2.00 **±2.80**	µA max
I_{OS}	Input Offset Current		30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 12V	88	74 **72**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V, V_{CM} = 0.5V	100	78 **74**	dB min
−PSRR	Negative Power Supply Rejection Ratio		85	—	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0**	V max
			12.3	12.1 **12.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 11V R_L = 10kΩ to V^+/2	83	74 **70**	dB min
V_O	Output Swing High	R_L 10kΩ to V^+/2	11.8	11.7	V min
		I_{SOURCE} = 5mA	11.6	11.5	
	Output Swing Low	R_L = 10kΩ to V^+/2	0.25	0.3	V max
		I_{SINK} = 5mA	.40	.45	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)	130	110	mA min
		Sinking to V^+ V_{ID} = 200mV (5)	130	110	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±65	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.9	2.4 **2.9**	mA max
SR	Slew Rate(6)	A_V = +1, V_I = 10V_{PP}, C_L = 10pF	15	—	V/µs
		A_V = +1, V_I = 10V_{PP}, C_L = 0.1µF	1	—	
R_{OUT}	Close Loop Output Resistance	A_V = +1, f = 100KHz	3	—	Ω
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2kΩ to V^+/2	8	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	15	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	57	—	Deg
GM	Gain Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	20	—	dB
−3dB BW	Small Signal -3db Bandwidth	A_V = +1, R_L = 2kΩ to V^+/2	12.5	—	MHz
		A_V = +1, R_L = 600Ω to V^+/2	10.5	—	
		A_V = +10, R_L = 600Ω to V^+/2	1.0	—	

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test. Output short circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS > 6V, allowable short circuit duration is 1.5ms.
(6) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

12V Electrical Characteristics (continued)

Unless otherwise specified, all limited ensured for V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP (1)	LIMIT (2)	UNIT
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	nV/√Hz
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	pA/√Hz
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to $V^+/2$	300	—	kHz
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 2kΩ to $V^+/2$ V_O = 8V_{PP}, V_S = ±5V	0.02%	—	
CT Rej.	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ to $V^+/2$	68	—	dB

6.7 Typical Performance Characteristics

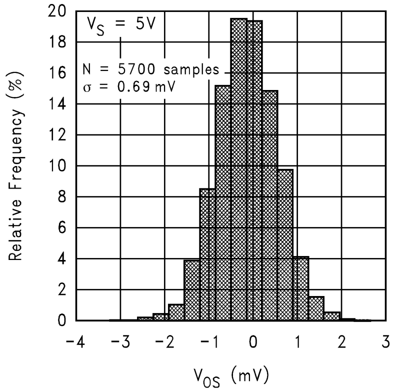


Figure 1. V_{OS} Distribution

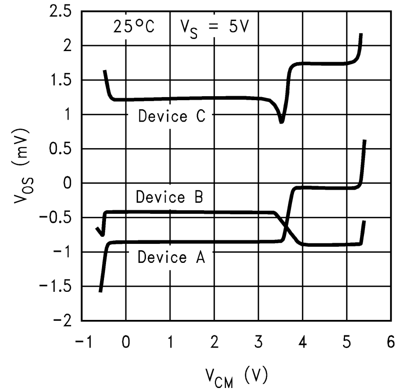


Figure 2. V_{OS} vs. V_{CM} for 3 Representative Units

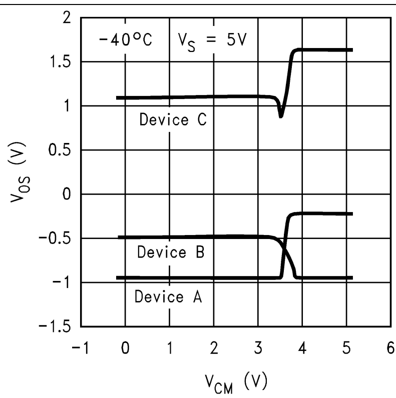


Figure 3. V_{OS} vs. V_{CM} for 3 Representative Units

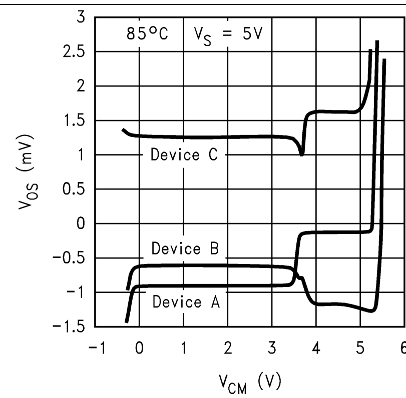


Figure 4. V_{OS} vs. V_{CM} for 3 Representative Units

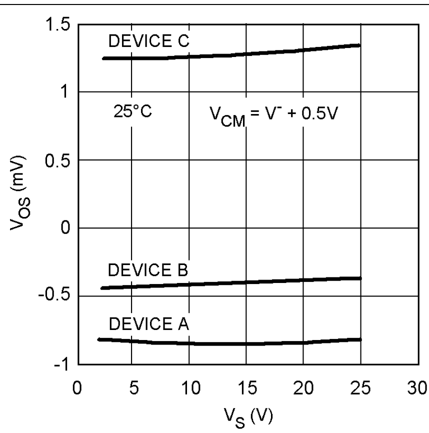


Figure 5. V_{OS} vs. V_S for 3 Representative Units

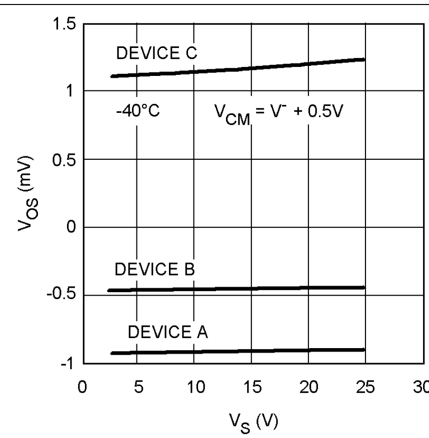


Figure 6. V_{OS} vs. V_S for 3 Representative Units

Typical Performance Characteristics (continued)

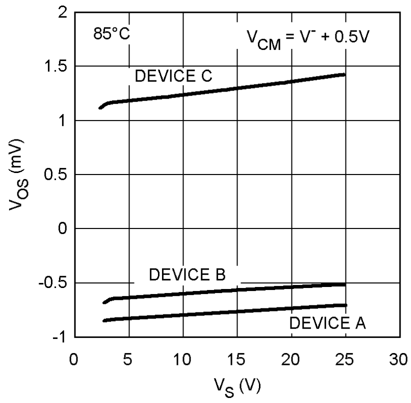


Figure 7. V_{OS} vs. V_S for 3 Representative Units

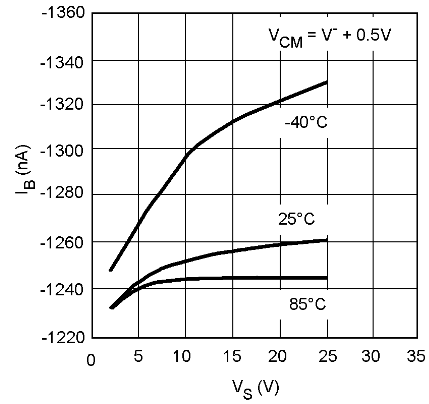


Figure 8. I_B vs. V_S

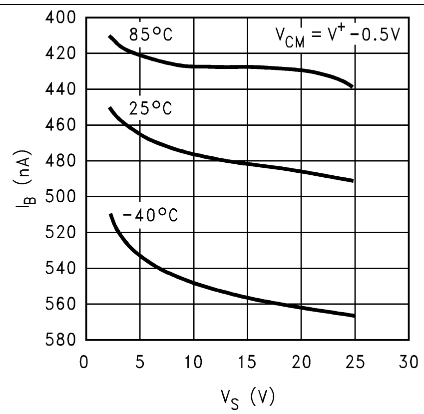


Figure 9. I_B vs. V_S

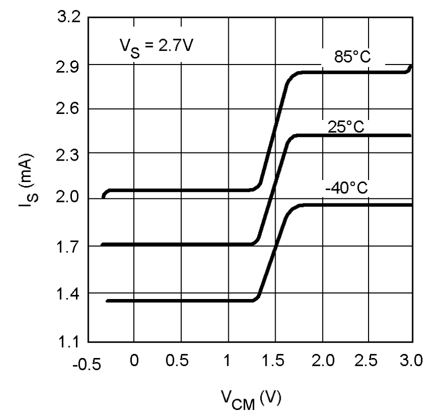


Figure 10. I_S vs. V_{CM}

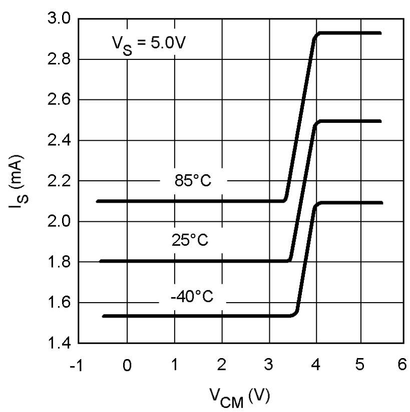


Figure 11. I_S vs. V_{CM}

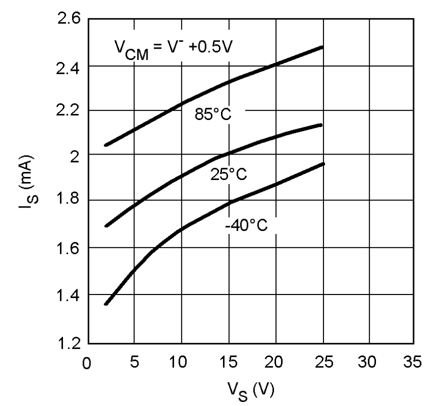


Figure 12. I_S vs. V_S

Typical Performance Characteristics (continued)

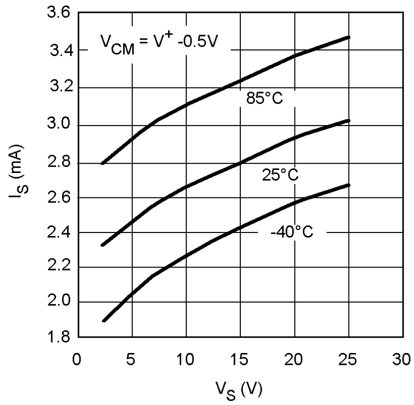


Figure 13. I_S vs. V_S

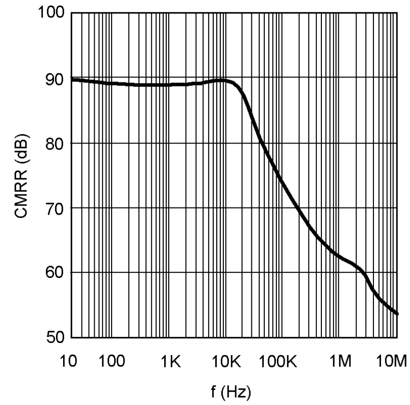


Figure 14. CMRR vs. Frequency

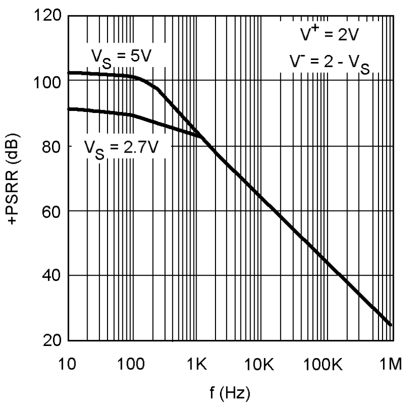


Figure 15. +PSRR vs. Frequency

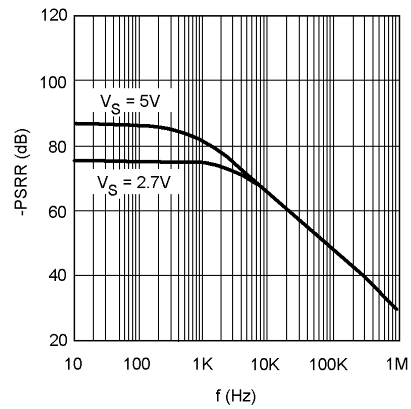


Figure 16. −PSRR vs. Frequency

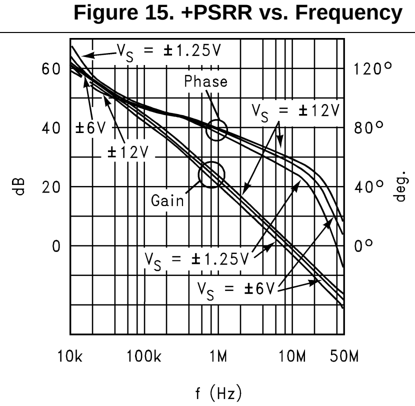


Figure 17. Open Loop Gain/Phase for Various Supplies

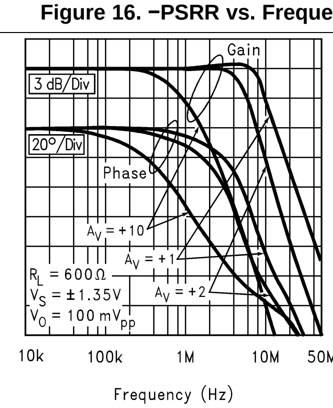


Figure 18. Closed Loop Frequency Response for Various Gains

Typical Performance Characteristics (continued)

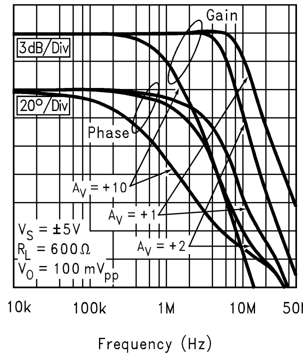


Figure 19. Closed Loop Frequency Response for Various Gains

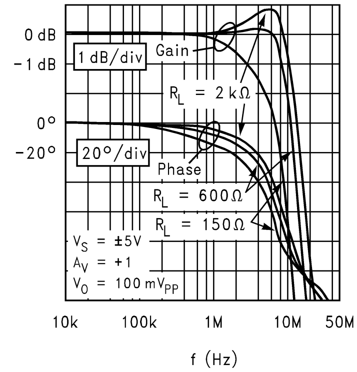


Figure 20. Closed Loop Frequency Response for Various R_L

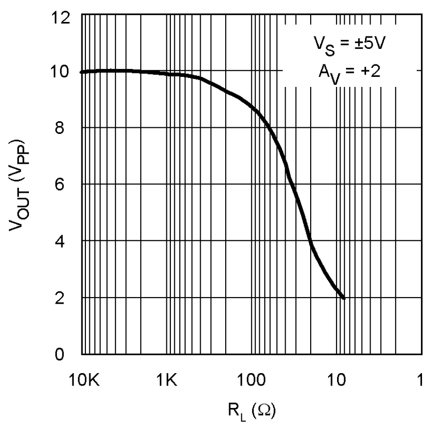


Figure 21. Maximum Output Swing vs. Load (1% Distortion)

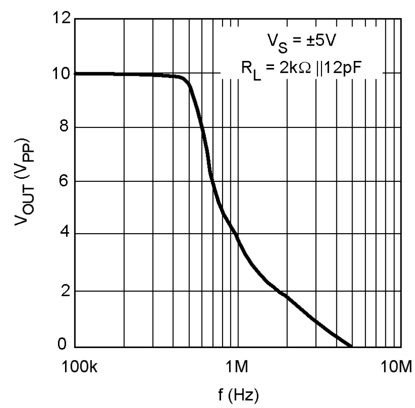


Figure 22. Maximum Output Swing vs. Frequency (1% Distortion)

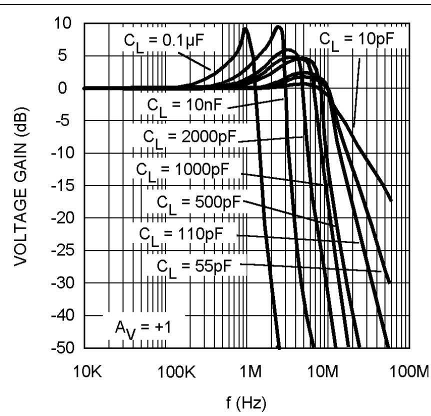


Figure 23. Closed Loop Small Signal Frequency Response for Various C_L

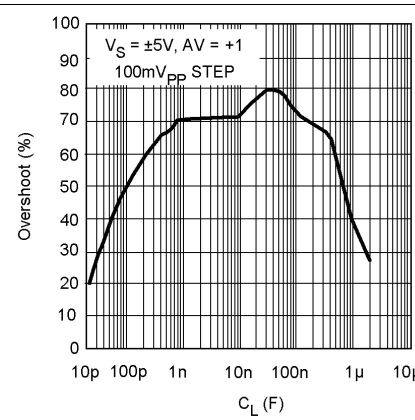


Figure 24. Overshoot vs. Cap Load

Typical Performance Characteristics (continued)

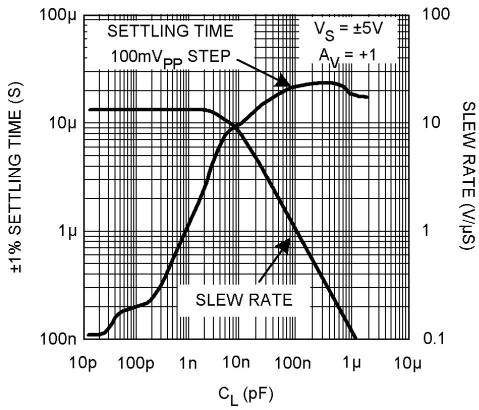


Figure 25. Settling Time (±1%) & Slew Rate vs. Cap Load

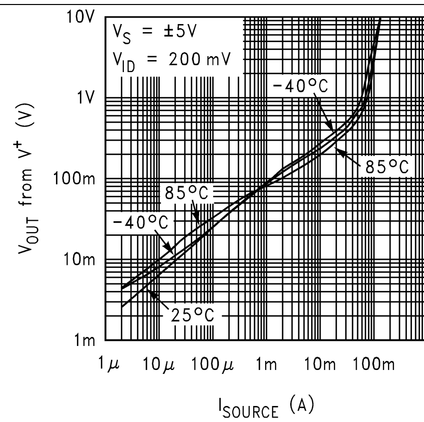


Figure 26. V_{OUT} from V^+ vs. I_{SOURCE}

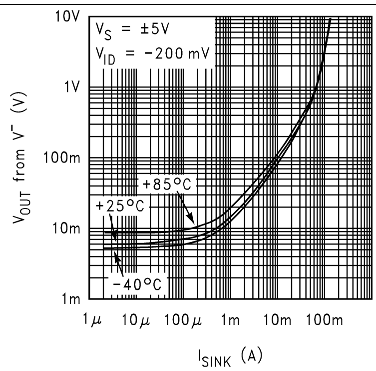


Figure 27. V_{OUT} from V^- vs. I_{SINK}

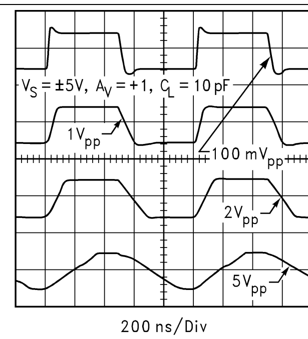


Figure 28. Step Response for Various Amplitudes

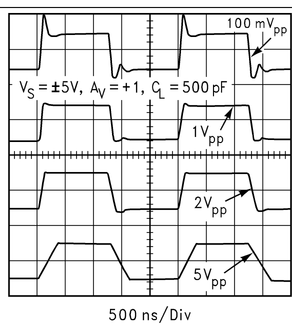


Figure 29. Step Response for Various Amplitudes

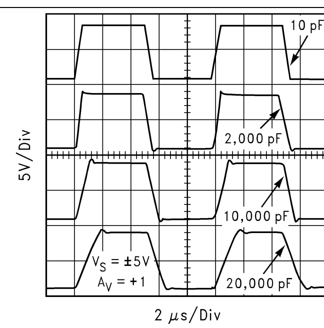


Figure 30. Large Signal Step Response for Various Cap Loads

Typical Performance Characteristics (continued)

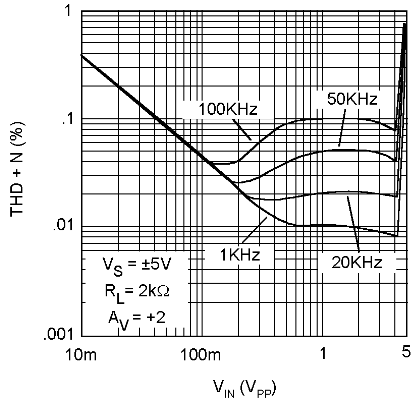


Figure 31. THD+N vs. Input Amplitude for Various Frequency

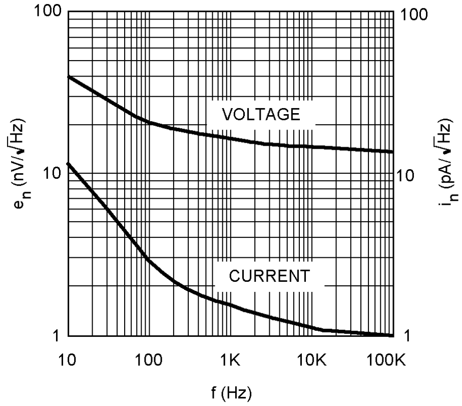


Figure 32. Input Referred Noise Density

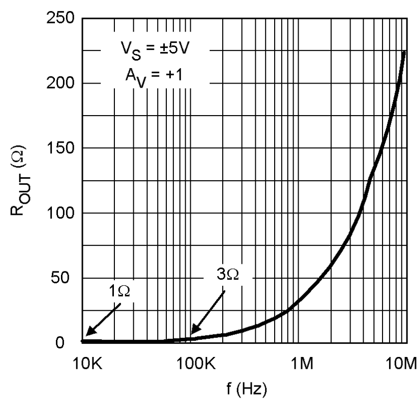


Figure 33. Closed Loop Output Impedance vs. Frequency

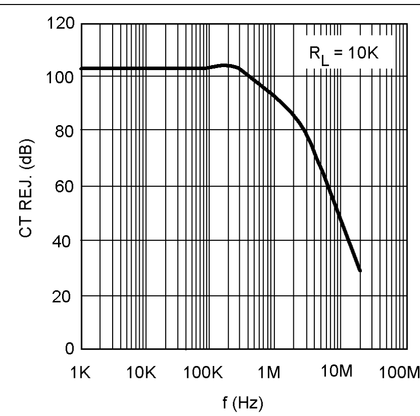


Figure 34. Crosstalk Rejection vs. Frequency

7 Application and Implementation

7.1 Block Diagram and Operational Description

A) Input Stage:

As seen in Figure 35, the input stage consists of two distinct differential pairs (Q1-Q2 and Q3-Q4) in order to accommodate the full Rail-to-Rail input common mode voltage range. The voltage drop across R5, R6, R7 and R8 is kept to less than 200 mV in order to allow the input to exceed the supply rails. Q13 acts as a switch to steer current away from Q3-Q4 and into Q1-Q2, as the input increases beyond 1.4 of V^+. This in turn shifts the signal path from the bottom stage differential pair to the top one and causes a subsequent increase in the supply current.

In transitioning from one stage to another, certain input stage parameters (V_{OS}, I_b, I_{OS}, e_n, and i_n) are determined based on which differential pair is "on" at the time. Input Bias current, I_b, will change in value and polarity as the input crosses the transition region. In addition, parameter such as PSRR and CMRR which involve the input offset voltage will also be effected by changes in V_{CM} across the differential pair transition region.

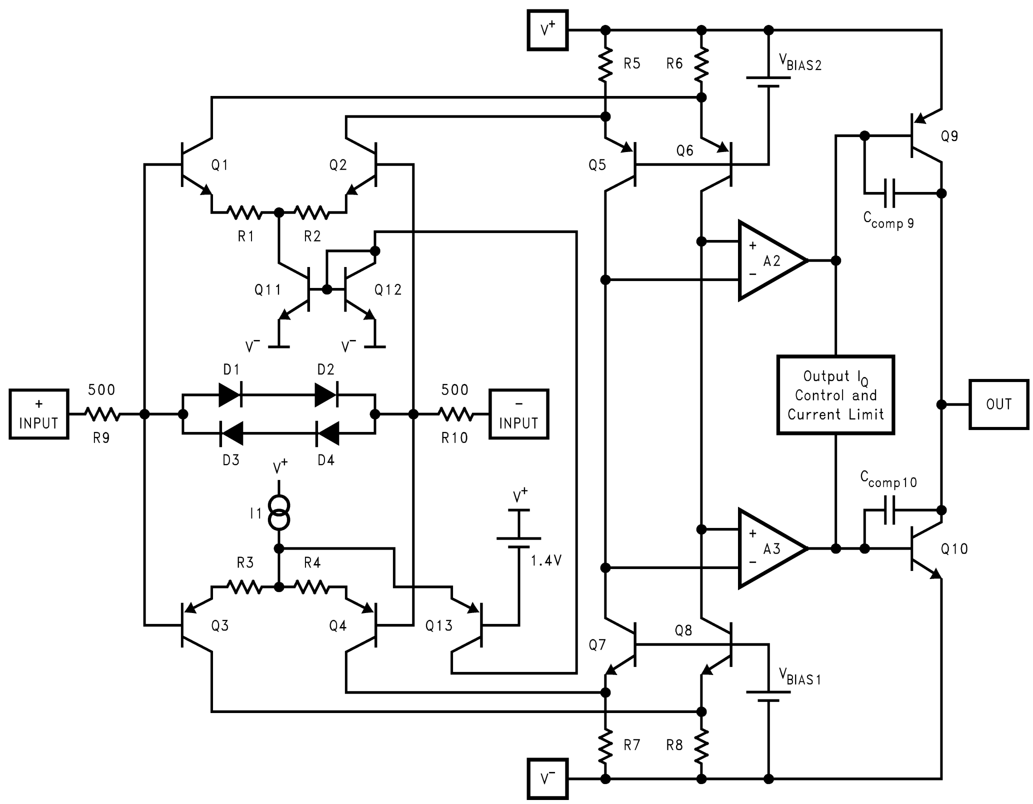


Figure 35. Simplified Schematic Diagram

Block Diagram and Operational Description
A) Input Stage: (continued)

The input stage is protected with the combination of R9-R10 and D1, D2, D3 and D4 against differential input over-voltages. This fault condition could otherwise harm the differential pairs or cause offset voltage shift in case of prolonged over voltage. As shown in Figure 36, if this voltage reaches approximately ±1.4V at 25°C, the diodes turn on and current flow is limited by the internal series resistors (R9 and R10). The Absolute Maximum Rating of ±10V differential on V_{IN} still needs to be observed. With temperature variation, the point were the diodes turn on will change at the rate of 5mV/°C

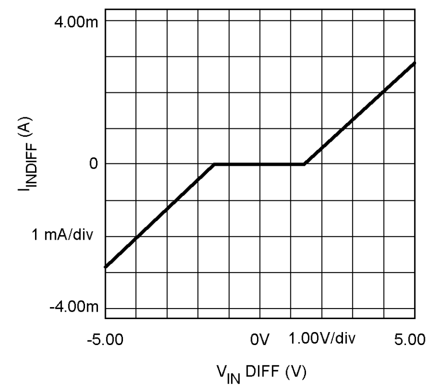


Figure 36. Input Stage Current vs. Differential Input Voltage

7.2 B) Output Stage:

The output stage (see Figure 35) is comprised of complimentary NPN and PNP common-emitter stages to permit voltage swing to within a $V_{ce(sat)}$ of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{ce} of Q9 and Q10. Using this approach to current limiting alleviates the drawback to the conventional scheme which requires one V_{be} reduction in output swing.

The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (see Figure 35, C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance - the internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than 0dB when the phase shift around the feedback loop is more than 180°, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough. Hence the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

7.3 C) Output Voltage Swing Close to V^-:

The LM8272's output stage design allows voltage swings to within millivolts of either supply rail for maximum flexibility and improved useful range. Because of this design architecture, as can be seen from Figure 35 diagram, with Output approaching either supply rail, either Q9 or Q10 Collector-Base junction reverse bias will decrease. With output less than a V_{be} from either rail, the corresponding output transistor operates near saturation. In this mode of operation, the transistor will exhibit higher junction capacitance and lower f_t which will reduce Phase Margin. With the Noise Gain (NG = 1 + Rf/Rg, Rf & Rg are external gain setting resistors) of 2 or higher, there is sufficient Phase Margin that this reduction (in Phase Margin) is of no consequence. However, with lower Noise Gain (<2) and with less than 150mV voltage to the supply rail, if the output loading is light, the Phase Margin reduction could result in unwanted oscillations.

C) Output Voltage Swing Close to V⁻: (continued)

In the case of the LM8272, due to inherent architectural specifics, the oscillation occurs only with respect to Q10 when output swings to within 150mV of V^-. However, if Q10 collector current is larger than its idle value of a few microamps, the Phase Margin loss becomes insignificant. In this case, 300µA is the required Q10 collector current to remedy this situation. Therefore, when all the aforementioned critical conditions are present at the same time (NG < 2, V_{OUT} < 150mV from supply rails, & output load is light) it is possible to ensure stability by adding a load resistor to the output to provide the necessary Q10 minimum Collector Current (300µA).

For 12V (or ±6V) operation, for example, add a 39kΩ resistor from the output to V^+ to cause 300µA output sinking current and ensure stability. This is equivalent to about 15% increase in total quiescent power dissipation.

7.4 Driving Capacitive Loads:

The LM8272 is specifically designed to drive unlimited capacitive loads without oscillations (see Figure 25). In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads (Settling Time and Slew Rate vs. Cap Load plot). The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to Figure 25, two distinct regions can be identified. Below about 10,000pF, the output Slew Rate is solely determined by the Op Amp's compensation capacitor value and available current into that capacitor. Beyond 10nF, the Slew Rate is determined by the Op Amp's available output current. An estimate of positive and negative slew rates for loads larger than 100nF can be made by dividing the short circuit current value by the capacitor.

7.5 Estimating the Output Voltage Swing

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, Figure 37 and Figure 38 plots can be used to predict the output swing. These plots also show several load lines corresponding to loads tied between the output and ground. In each case, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 600-Ω load can accommodate an output swing to within 100mV of V^- and to 250mV of V^+ (V_S = ±5V) corresponding to a typical 9.65V_{PP} unclipped swing.

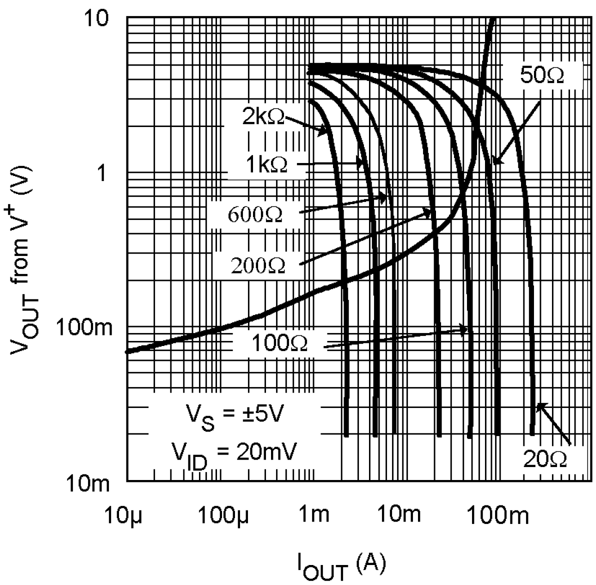


Figure 37. Steady State Output Sourcing Characteristics with Load Lines

Estimating the Output Voltage Swing (continued)

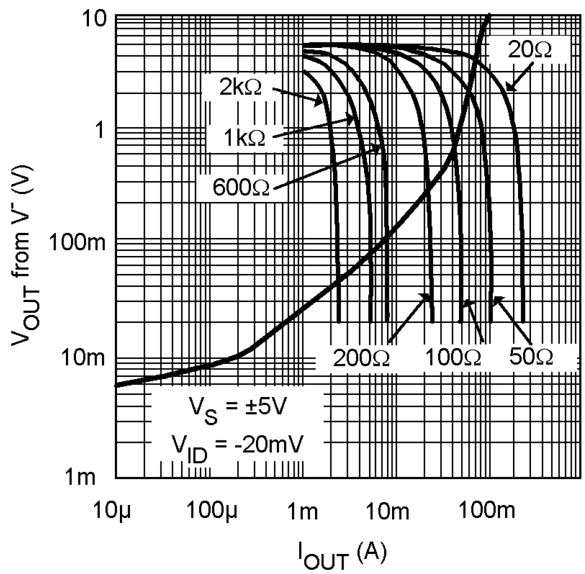


Figure 38. Steady State Output Sinking Characteristics with Load Lines

7.6 Output Short Circuit Current and Dissipation Issues:

The LM8272 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, output short circuit condition can be tolerated indefinitely.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or if the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$$P_{total} = P_Q + P_{DC} + P_{AC} \quad (1)$$

$$P_Q = I_S \cdot V_S \text{ (Op Amp Quiescent Power Dissipation)} \quad (2)$$

$$P_{DC} = I_O \cdot (V_r - V_o) \text{ (DC Load Power)} \quad (3)$$

P_{AC} = See Table 1 below (AC Load Power)

where:

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)
- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
SINUSOIDAL	TRIANGULAR	SQUARE
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [24^2/600] = 45.0mW \quad (4)$$

7.7 Other Application Hints:

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge “bucket” for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

7.8 LM8272 Advantages:

Compared to other Rail-to-Rail Input/Output devices, the LM8272 offers several advantages such as:

- Improved cross over distortion
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Nearly constant Unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM8272MM/NOPB	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	A60
LM8272MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A60
LM8272MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A60

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

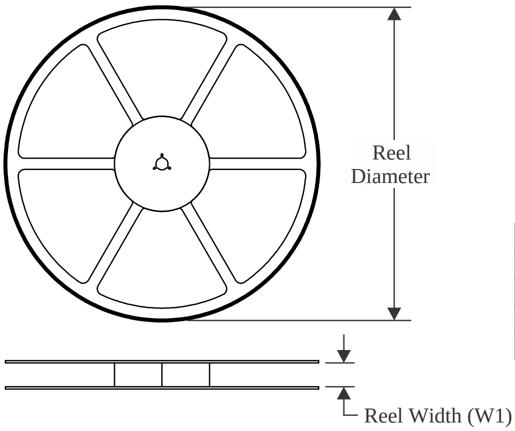
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

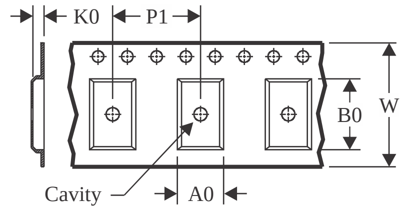
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

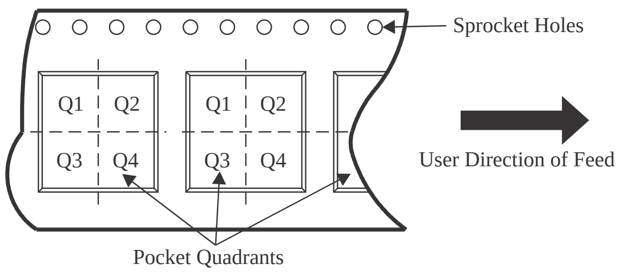


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

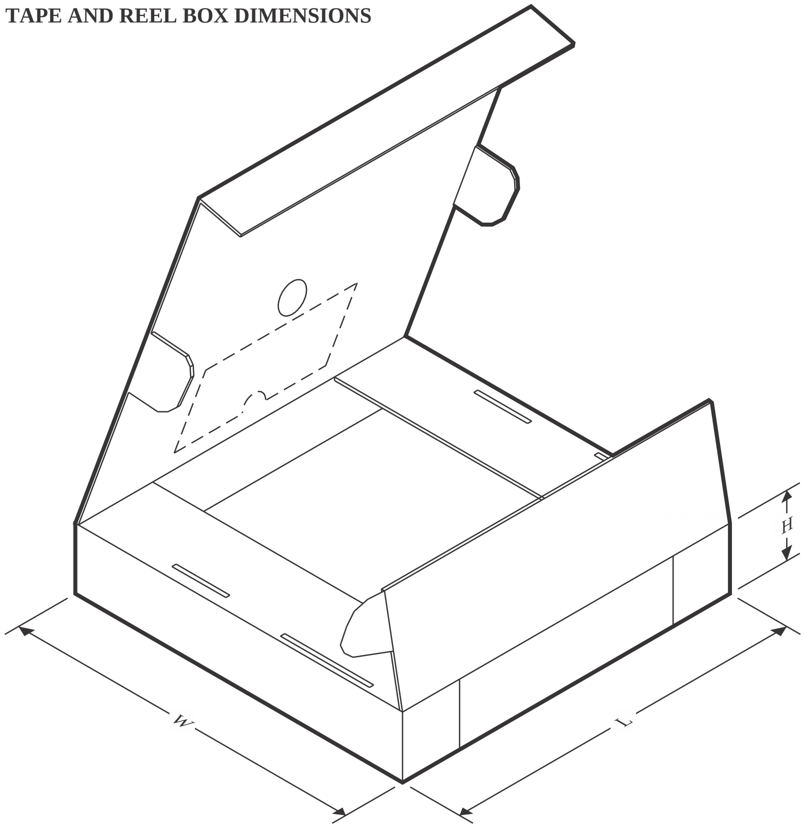
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

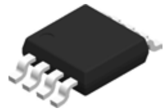
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8272MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8272MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

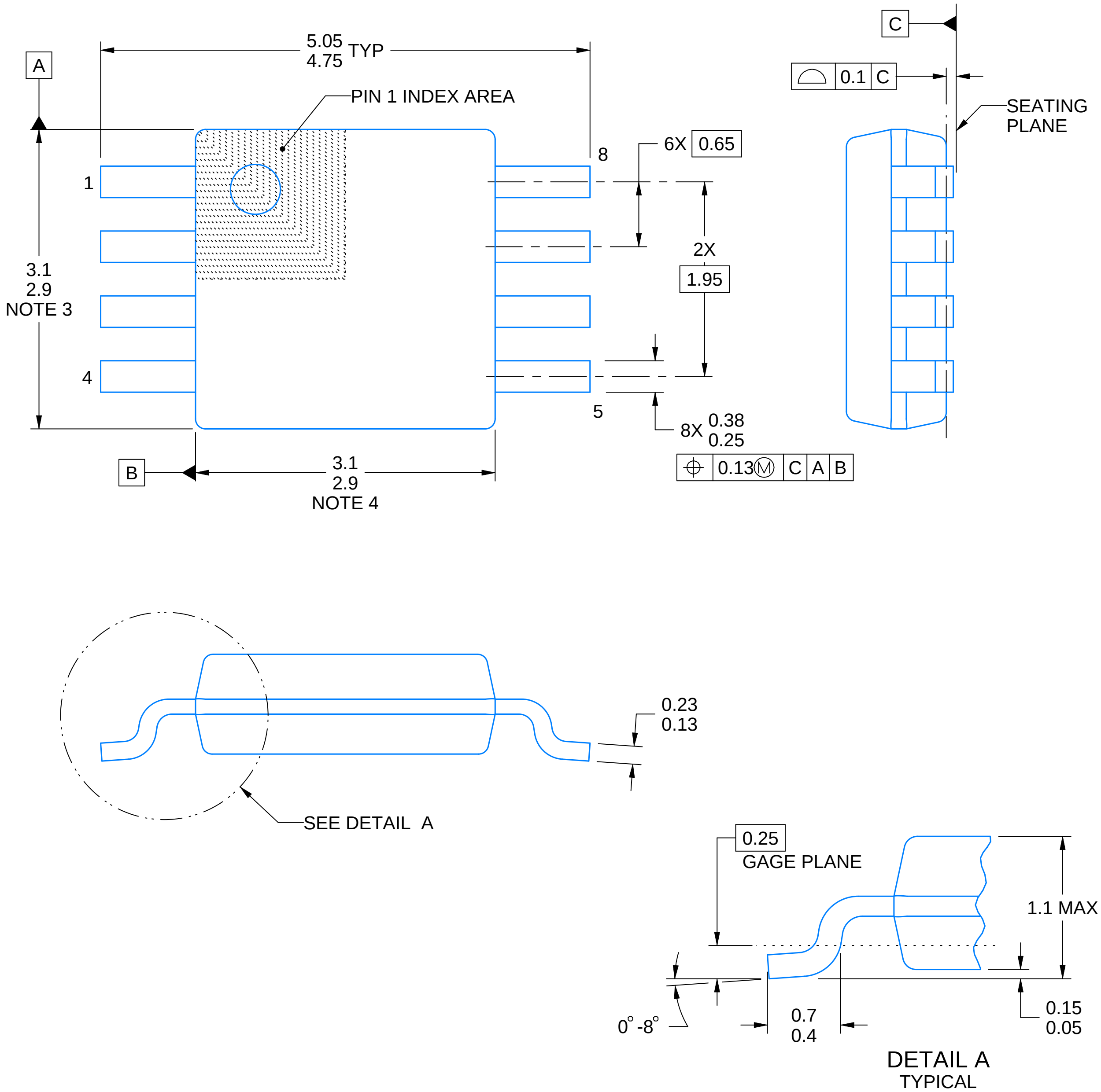
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8272MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM8272MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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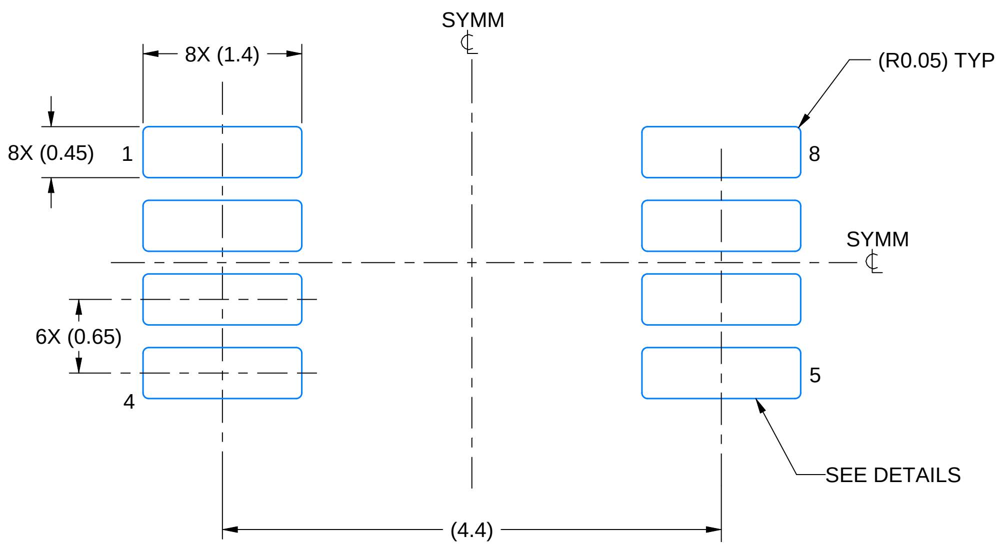
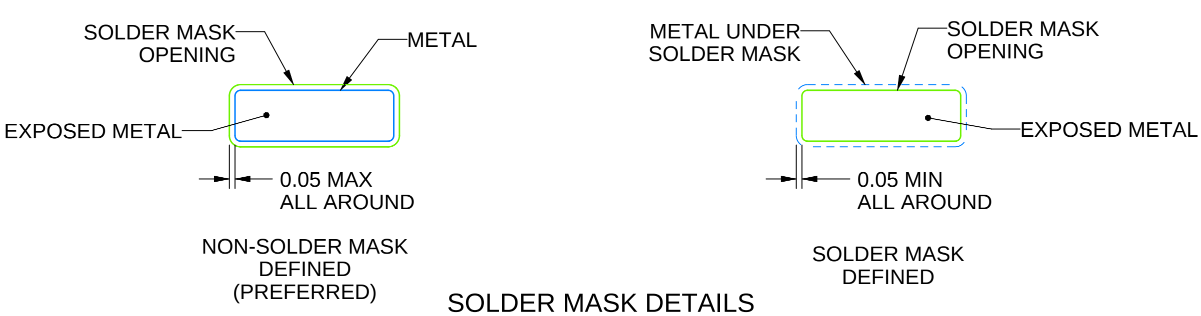
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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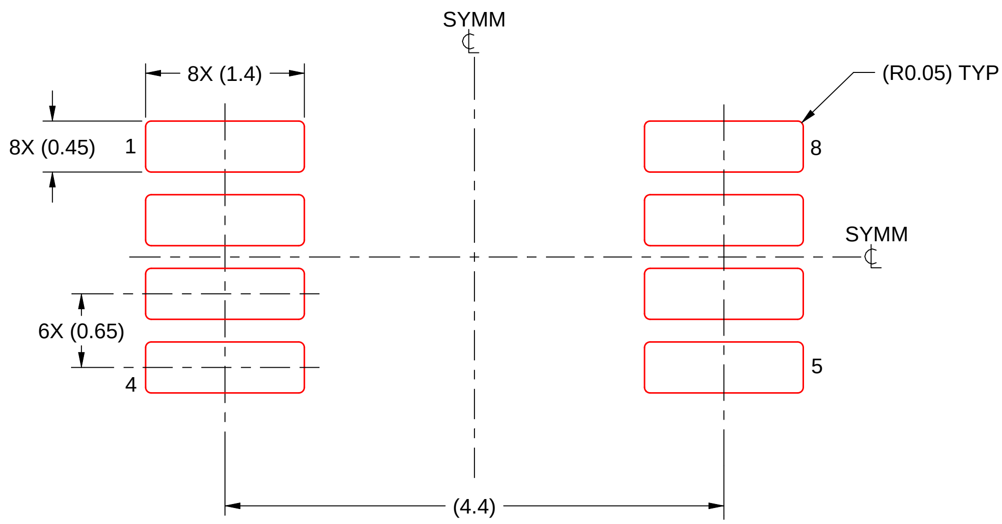
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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