LM76202-Q1 過電圧 / 過電流保護機能搭載 60V、2.2A 統合型理想ダイオード

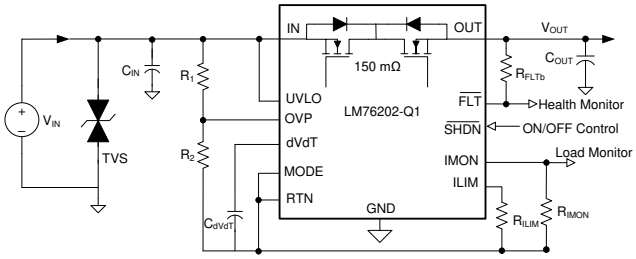
1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - 温度グレード 1:-40°C ≤ T_A ≤ +125°C
  - AEC-Q100-012 短絡信頼性グレード A
  - HBM ESD 分類レベル 2
  - CDM ESD 分類レベル C6
- 動作電圧：4.2V～60V、絶対最大定格 62V
- –60V までの入力逆極性保護機能内蔵
- バック・ツー・バック MOSFET を内蔵し、合計 RON 150mΩ
- 過渡耐性：最大 65V
- 電流制限を 0.1A～ 2.23A に調整可能 (1A において ±5% 精度)
- ISO7637 および ISO16750-2 試験時の負荷保護
- バッテリへの短絡と GND への短絡から保護
- 逆電流ブロックにより出力のバッテリ短絡から保護
- IMON 電流インジケータ出力 (±8.5% 精度)
- 低い静止電流：動作時 285µA、シャットダウン時 16µA
- 可変 UVLO、OVP カットオフ、突入電流制御
- 38V 過電圧クランプ・オプションを出荷時に設定
- 電流を制限するフォルトへの応答オプションを選択可能 (自動再試行、ラッチオフ、サーキット・ブレーカー・モード)
- 使いやすい 16 ピンの HTSSOP パッケージで供給

2 アプリケーション

- フロント・カメラ、リア・カメラ
- 運転支援 ECU
- テレマティクス制御ユニット
- 携帯電話/スマートフォン・モジュールのアセット・トラッキング

概略回路図



3 概要

LM76202-Q1 は、各種保護機能を備えた小型で機能豊富な 60V の統合型理想ダイオードです。入力電源電圧範囲が広いため、12V および 24V の車載用バッテリで動作するアプリケーションを制御できます。このデバイスは最大 ±60V の正負の電源電圧に耐え、負荷を保護できます。負荷、入力電源、デバイスの保護機能は、過電流、突入電流制御、過電圧、低電圧スレッショルドを含めて多くの機能をプログラム可能です。内蔵の堅牢な保護制御ブロックと 60V の定格により、ISO 規格パルス試験を考慮したシステム設計が簡単になります。

シャットダウン・ピンを使うと内蔵 FET のイネーブル/ディセーブルを外部的に制御でき、デバイスを低電流のシャットダウン・モードに移行させることもできます。システム状態の監視と下流負荷の制御のため、フォルト出力と高精度の電流監視出力を備えています。MODE ピンにより、電流を制限する 3 種類のフォルト応答 (サーキット・ブレーカー、ラッチオフ、自動再試行モード) のどれにでも柔軟にデバイスを構成できます。$V_{(IN)}$ および $V_{(OUT)}$ を監視し、V(IN) < (V(OUT)-10mV) のときに逆電流保護を行います。この機能は、出力がバッテリに短絡した障害時に過電圧からシステム・バスを保護し、電力障害およびブラウンアウト状況での電圧ホールドアップ要件を満たすためにも役立ちます。

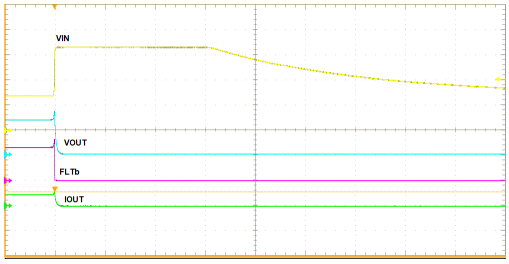
このデバイスは 5mm × 4.4mm の 16 ピン HTSSOP で供給され、–40℃～+125℃の温度範囲で完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM76202-Q1	HTSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

24V での ISO16750-2 ロードダンプ・パルス 5b 性能



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4 改訂履歴

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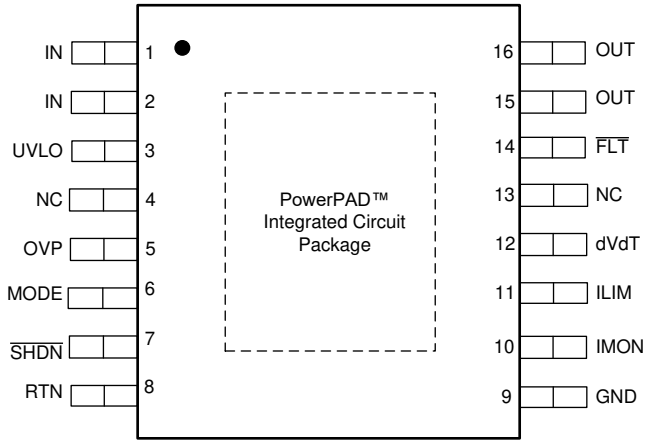
5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 2	IN	P	Input supply voltage. See *IN, OUT, RTN and GND Pins* section.
3	UVLO	I	Input for setting the programmable Undervoltage Lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{\text{FLT}}$ to indicate power failure. If the Undervoltage Lockout function is not needed, the UVLO terminal must be connected to the IN terminal. See *Undervoltage Lockout (UVLO)* section.
4, 13	NC	—	No internal connection. These pins can be connected to RTN for enhanced thermal performance.
5	OVP	I	Input for setting the programmable Overvoltage Protection threshold. An overvoltage event turns off the internal FET and asserts $\overline{\text{FLT}}$ to indicate the overvoltage fault. For fixed overvoltage clamp response connect OVP to RTN externally. See *Overvoltage Protection (OVP)* section.
6	MODE	I	Mode selection pin for overload fault response. See the *Device Functional Modes* section.
7	$\overline{\text{SHDN}}$	I	Shutdown pin. Pulling $\overline{\text{SHDN}}$ low enters the device into low-power shutdown mode. Cycling $\overline{\text{SHDN}}$ pin voltage resets the device that has latched off due to a fault condition. See *Low Current Shutdown Control ($\overline{\text{SHDN}}$)* section.
8	RTN	—	Reference for device internal control circuits. If reverse input polarity protection is not required, this pin can be connected to GND. See *IN, OUT, RTN and GND Pins* section.
9	GND	—	Connect GND to system ground. See *IN, OUT, RTN and GND Pins* section.
10	IMON	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to RTN converts current to proportional voltage. If pin is unused, leave pin floating. See *Current Monitoring* section.
11	ILIM	I/O	A resistor from this pin to RTN sets the overload and short-circuit current limit. See the *Overload and Short Circuit Protection* section.
12	dVdT	I/O	A capacitor from this pin to RTN sets output voltage slew rate. See the *Hot Plug-In and In-Rush Current Control* section.
14	$\overline{\text{FLT}}$	O	Fault event indicator. Indicator is an open drain output. If indicator is unused, leave indicator floating. See *FAULT Response* section.
15,16	OUT	P	Power output of the device. See *IN, OUT, RTN and GND Pins* section.
PowerPAD		—	PowerPAD integrated circuit package must be connected to RTN plane on PCB using multiple vias for enhanced thermal performance. PowerPAD is not internally connected to RTN. Do not use the PowerPAD as the only electrical connection to RTN.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
IN, IN-OUT		-62	62	V
IN, IN-OUT (350ms transient), T_A = 25°C		-65	65	
[IN, OUT, $\overline{FLT}$, UVLO, $\overline{SHDN}$] to RTN		-0.3	62	
[OVP, dVdT, ILIM, IMON, MODE] to RTN		-0.3	5	
RTN		-62	0.3	
$I_{\overline{FLT}}$, I_{dVdT}, $I_{\overline{SHDN}}$	Sink current	10		mA
I_{dVdT}, I_{ILIM}, I_{IMON}	Source Current	Internally limited	Internally limited	
T_J	Operating junction temperature	-40	150	°C
	Transient junction temperature	-65	$T_{(TSD)}$	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage range	-60		60	V
UVLO, OUT, $\overline{FLT}$		0		60	
OVP, dVdT, ILIM, IMON, $\overline{SHDN}$		0		4	
ILIM	Resistance	5.36		120	kΩ
IMON		1			
IN, OUT	External capacitance	0.1	1		µF
dVdT		10			nF
T_J	Operating junction temperature range	-40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LM76202-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	18	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(SHDN)}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN.
(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$	Operating input voltage		4.2		60	V
V_{PORR}	Internal POR Threshold, Rising		3.89	4	4.14	V
V_{PORHys}	Internal POR Hysteresis		55	275	305	mV
IQ_{ON}	Supply Current with device enabled	VIN = 24V, Enabled: $V_{(\overline{SHDN})}$ = 2 V		300	398	µA
IQ_{ON}	Supply Current with device enabled	VIN = 12V Enabled: $V_{(\overline{SHDN})}$ = 2 V,		285	390	µA
IQ_{OFF}	Supply Current with device disabled	VIN = 24V, $V_{(\overline{SHDN})}$ = 0 V		18	35	µA
IQ_{OFF}	Supply Current with device disabled	VIN = 12V, $V_{(\overline{SHDN})}$ = 0 V		16	32	µA
I_{VINR}	Reverse Input supply current	$V_{(IN)}$ = -60 V, $V_{(OUT)}$ = 0 V			66	µA
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO Threshold Voltage, Rising		1.175	1.19	1.25	V
$V_{(UVLOR)}$	UVLO Threshold Voltage, Falling		1.08	1.1	1.126	V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 60 V	–100		100	nA
LOW IQ SHUTDOWN (SHDNb) INPUT						
$V_{(\overline{SHDN})}$	Output voltage	$I_{(\overline{SHDN})}$ = 0.1µA	2	2.7	3.4	V
$V_{(SHUTF)}$	$\overline{SHDN}$ Threshold Voltage for Low IQ Shutdown, Falling		0.45			V
$V_{(SHUTFR)}$	$\overline{SHDN}$ Threshold, Rising				0.96	V
$I_{(\overline{SHDN})}$	Input current	$V_{(\overline{SHDN})}$ = 0.4 V	-10			µA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(SEL_OVP)}$	Factory Set OV Clamp Select Threshold		180	200	240	mV
V_{OVC}	Internal Over voltage clamp	$V_{(IN)}$ > 42 V, $I_{(OUT)}$=10mA $V_{(OVP)}$ = 0 V	36	37.5	40	V
$V_{(OVPR)}$	Over-Voltage Threshold Voltage, Rising		1.175	1.19	1.225	V
$V_{(OVPF)}$	Over-Voltage Threshold Voltage, Falling		1.085		1.125	
$I_{(OVP)}$	OVP Input Leakage Current	0V ≤ $V_{(OVP)}$ ≤ 4V	–100	0	100	nA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT Charging Current	$V_{(dVdT)}$ = 0 V	4	4.7	5.82	µA
$R_{(dVdT)}$	dVdT Discharging Resistance	$\overline{SHDN}$ = 0 V, with $I_{(dVdT)}$ = 10mA sinking		28		Ω
$GAIN_{(dVdT)}$	dVdT to OUT Gain	$\Delta V_{(OUT)} / \Delta V_{(dVdT)}$	23.75	24.63	25.5	V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$V_{(ILIM)}$	ILIM Bias Voltage			1		V
$I_{(OL)}$	Overload Current Limit	$R_{(ILIM)}$ = 120 kΩ, $V_{(IN)}$-$V_{(OUT)}$=1V	0.085	0.1	0.115	A
		$R_{(ILIM)}$ = 12 kΩ, $V_{(IN)}$-$V_{(OUT)}$=1V	0.95	1	1.05	
		$R_{(ILIM)}$ = 8 kΩ, $V_{(IN)}$-$V_{(OUT)}$=1V	1.425	1.5	1.575	
		$R_{(ILIM)}$ = 5.36 kΩ, $V_{(IN)}$-$V_{(OUT)}$=1V	2.11	2.23	2.35	
$I_{(OL_R\text{-}OPEN)}$		$R_{(ILIM)}$= OPEN, Open Resistor Current Limit		0.055		
$I_{(OL_R\text{-}SHORT)}$		$R_{(ILIM)}$= SHORT, Shorted Resistor Current Limit		0.095		
$I_{(CB)}$	Circuit breaker detection threshold	$R_{(ILIM)}$ = 120 kΩ, MODE = open	0.045	0.073	0.11	A
$I_{(CB)}$	Circuit breaker detection threshold	$R_{(ILIM)}$ = 5.36 kΩ, MODE = open	2	2.21	2.4	A

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Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(SHDN)}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN.

(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SCL)}$	Short-Circuit Current Limit	$R_{(ILIM)}$ = 120 kΩ, $V_{(IN)}$-$V_{(OUT)}$=5V	0.08	0.1	0.12	A
		$R_{(ILIM)}$ = 8 kΩ, $V_{(IN)}$-$V_{(OUT)}$=5V	1.425	1.5	1.575	A
		$R_{(ILIM)}$ = 5.36 kΩ, $V_{(IN)}$-$V_{(OUT)}$=5V	2.11	2.23	2.35	A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			1.87 x $I_{(OL)}$ + 0.015		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain Factor $I_{(IMON)}$:$I_{(OUT)}$	0.1A ≤ $I_{(OUT)}$ ≤ 2A	72	78.28	85	µA/A
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT Total ON Resistance	0.1A ≤ $I_{(OUT)}$ ≤ 2A,T_J = 25°C	130	150	168	mΩ
		0.1A ≤ $I_{(OUT)}$ ≤ 2A, -40°C ≤ T_J ≤ 85°C		150	220	
		0.1A ≤ $I_{(OUT)}$ ≤ 2A, -40°C ≤ T_J ≤ 125°C	78	150	265	
$I_{lkg(OUT)}$	OUT Leakage Current in Off State	$V_{(IN)}$ = 60 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, Sourcing			12	µA
$I_{lkg(OUT)}$	OUT Leakage Current in Off State	$V_{(IN)}$ = 0 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 24 V, Sinking	-11		11	µA
		$V_{(IN)}$ = -60 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, Sinking	-40	-18	50	
$V_{(REVTH)}$	$V_{(IN)}$-$V_{(OUT)}$ Threshold for Reverse Protection Comparator, Falling		-16.2	-10	-5	mV
$V_{(FWDTH)}$	$V_{(IN)}$-$V_{(OUT)}$ Threshold for Reverse Protection Comparator, Rising		85	96	110	mV
FAULT FLAG (FLTb): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-Down Resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5mA sinking		350		Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input Leakage Current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–200		200	nA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD Threshold, rising			157		°C
	TSD hysteresis			10.1		°C
MODE						
MODE_SEL	Thermal fault mode selection	MODE = 402 kΩ to RTN	Current limiting with latch			
		MODE = Open	Circuit breaker mode with auto-retry			
		MODE = Short to RTN	Current limiting with auto-retry			

6.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(SHDN)}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN.

(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT						
UVLO Turn On Delay	UVLO_$t_{ON(dly)}$	UVLO↑ (100mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100mV, $C_{(dvdt)}$ = Open		80		µs
	UVLO_$t_{ON(dly)}$	UVLO↑ (100mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100mV, $C_{(dvdt)}$ ≥ 10 nF, [$C_{(dvdt)}$ in nF]		80+14.5 x $C_{(dvdt)}$		
UVLO Turn-Off delay	UVLO_$t_{off(dly)}$	UVLO↓ (100mV below $V_{(UVLOF)}$) to $\overline{FLT}$ ↓		9		µs
SHUTDOWN INPUT						

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Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 12 V, $V_{(SHDN)}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN.

(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SHUTDOWN Exit delay	SHDN_$t_{on(dly)}$	$\overline{SHDN}$ ↑ (above $V_{(SHUTR)}$ to $V_{(OUT)}$ = 100mV, $C_{(dvdt)}$ ≥ 10 nF, [$C_{(dvdt)}$ in nF]		350+14 .5 x $C_{(dvdt)}$		µs
	SHDN_$t_{on(dly)}$	$\overline{SHDN}$ ↑ (above $V_{(SHUTR)}$ to $V_{(OUT)}$ = 100mV, $C_{(dvdt)}$= Open		355		
SHUTDOWN Entry delay	SHDN_$t_{off(dly)}$	$\overline{SHDN}$ ↓ (below $V_{(SHUTF)}$ to $\overline{FLT}$ ↓		10		µs
OVP INPUT						
OVP Exit delay	$t_{OVP(dly)}$	OVP ↓(20mV below $V_{(OVPF)}$) to $V_{(OUT)}$ = 100mV		205		µs
OVP Disable delay	$t_{OVP(dly)}$	OVP↑ (20mV above $V_{(OVPR)}$) to $\overline{FLT}$ ↓		2		µs
OVP clamp delay	$t_{OVC(dly)}$	$V_{(IN)}$ step from 24V to 60V in 50µs, Iload: 10mA, C_L: 0.1uF. OVP connected to RTN		3		µs
CURRENT LIMIT						
Fast-Trip Comparator Delay	$t_{FASTTRIP(dly)}$	$I_{(OUT)}$ = 1.5x $I_{(FASTRIP)}$		170		ns
REVERSE CURRENT BLOCKING COMPARATOR						
RCB comparator delay	$t_{REV(dly)}$	($V_{(IN)}$-$V_{(OUT)}$) ↓ (100mV overdrive below $V_{(REVTH)}$) to internal FET OFF		1.29		µs
		($V_{(IN)}$-$V_{(OUT)}$) ↓ (10mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$ ↓		40		µs
	$t_{FWD(dly)}$	($V_{(IN)}$-$V_{(OUT)}$) ↑ (10mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$ ↑		60		µs
THERMAL SHUTDOWN						
Retry Delay in TSD	t_{retry}			540		ms
OUTPUT RAMP TIME						
Output Ramp Time	t_{dVdT}	$\overline{SHDN}$↑ to $V_{(OUT)}$ = $V_{(IN)}$		1.6		ms
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = $V_{(IN)}$, with $C_{(dVdT)}$ = 47nF		10		ms
FAULT FLAG						
FLT assertion delay in circuit breaker mode	$t_{CB(dly)}$	MODE = OPEN,Delay from $I_{(out)}$>$I_{(lim)}$ to $\overline{FLT}$ ↓(and internal FET turned off)		4		ms
Retry Delay in circuit breaker mode	$t_{CBretry(dly)}$	MODE= OPEN, $C_{(dVdT)}$ = Open. $I_{(out)}$>$I_{(lim)}$. Delay from $\overline{FLT}$ ↓ to $V_{(dVdT)}$ = 50mV (Rising)		540		ms
PGOOD delay time	t_{PGOODR}	Delay for rising $\overline{FLT}$ edge		1.8		ms
	t_{PGOODF}	Delay for falling $\overline{FLT}$ edge		900		µs

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6.7 Typical Characteristics

T_A = 25 °C, $V_{(IN)}$ = 12 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless otherwise noted)

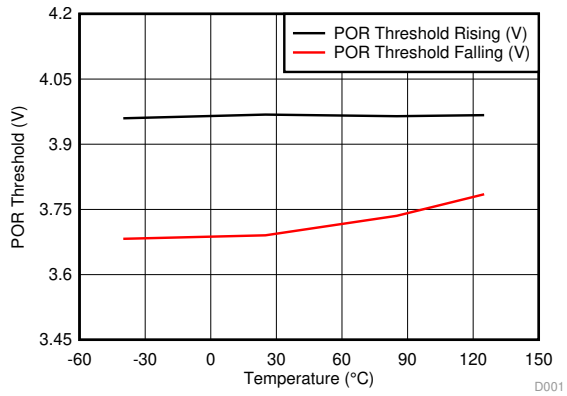

図 1. POR Threshold (V_{POR}) vs Temperature

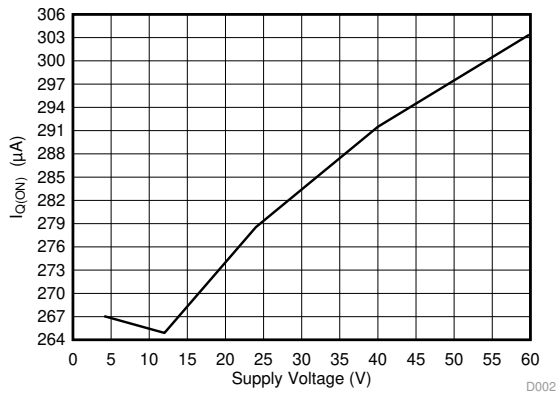

図 2. Supply Current ON (IQ_{ON}) vs Supply Voltage (V_{IN})

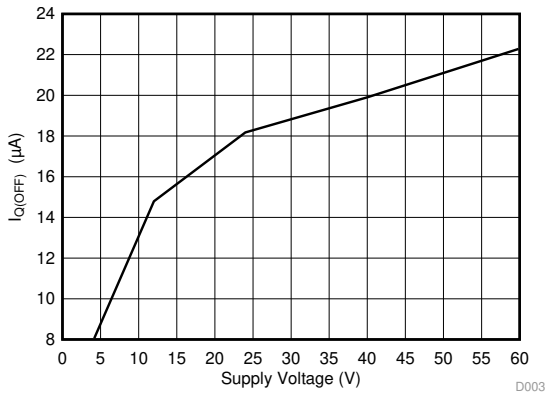

図 3. Supply Current OFF (IQ_{OFF}) vs Supply Voltage (V_{IN})

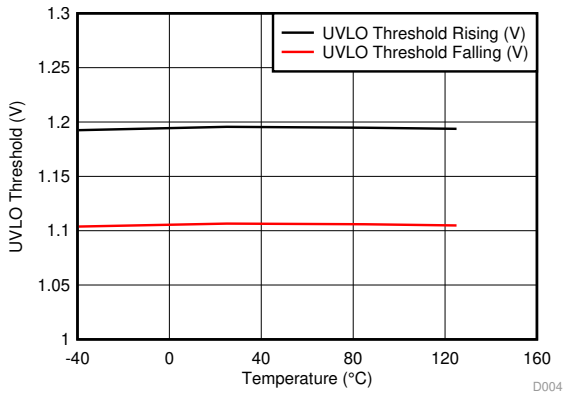

図 4. UVLO Thresholds (V_{UVLOR}, V_{UVLOF}) vs Temperature

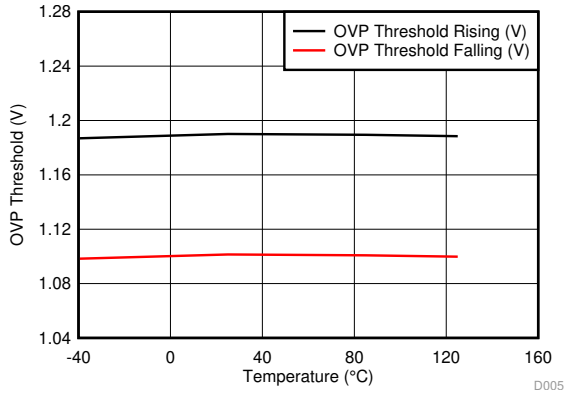

図 5. OVP Thresholds (V_{OVPR}, V_{OVPF}) vs Temperature

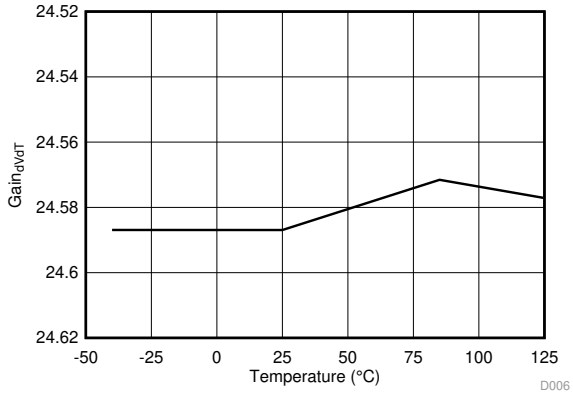

図 6. $GAIN_{(dVdT)}$ vs Temperature

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Typical Characteristics (continued)

T_A = 25 °C, $V_{(IN)}$ = 12 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless otherwise noted)

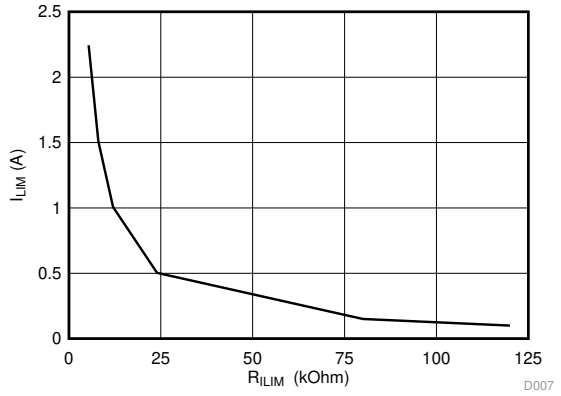
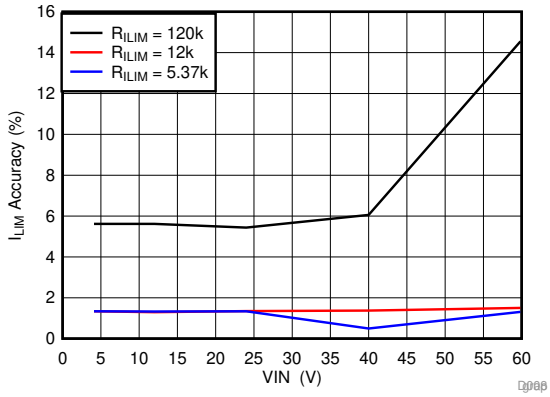


図 7. I_{LIM} vs R_{ILIM}



T_A = -40 to 125 °C

図 8. I_{LIM} Accuracy vs Supply Voltage

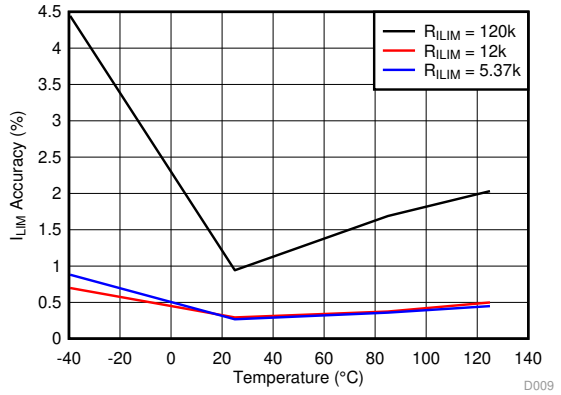


図 9. I_{LIM} Accuracy vs Temperature with V_{IN} = 12 V

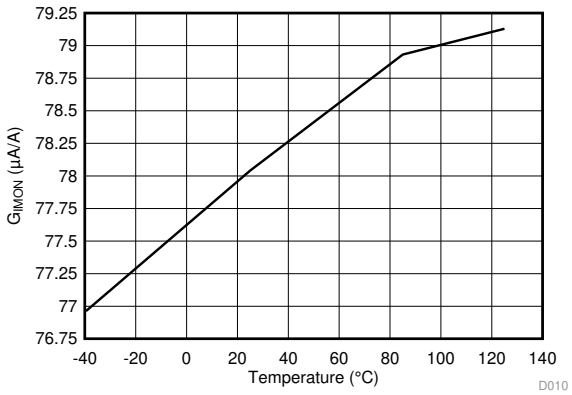


図 10. $GAIN_{(IMON)}$ vs Temperature

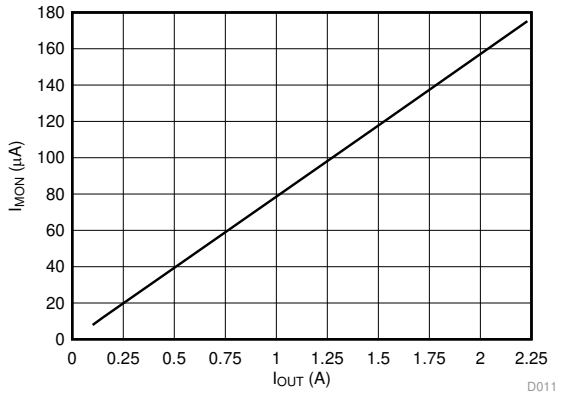


図 11. I_{MON} vs I_{OUT}

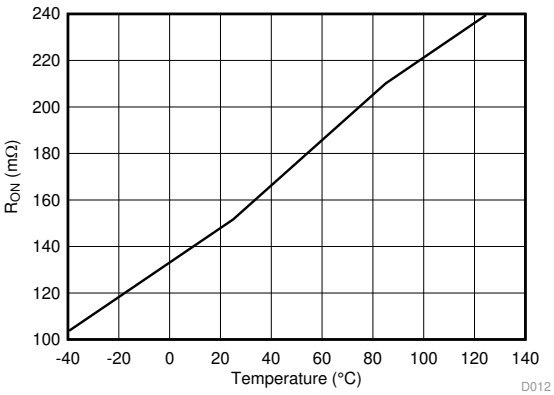
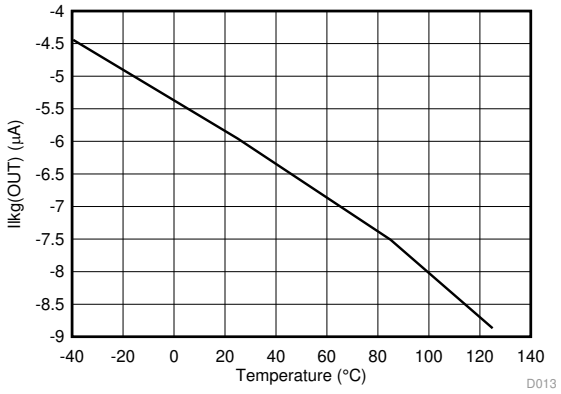


図 12. R_{ON} vs Temperature

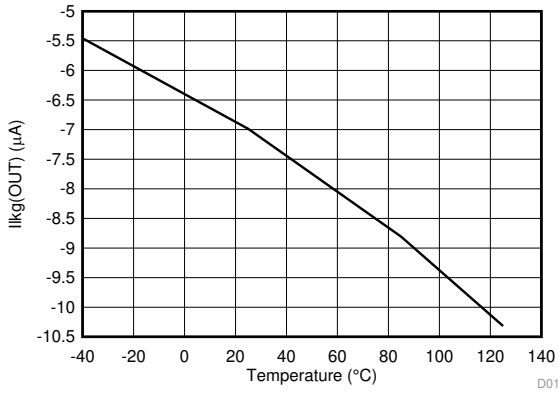
Typical Characteristics (continued)

T_A = 25 °C, $V_{(IN)}$ = 12 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(IN)}$ = 0.1 µF, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless otherwise noted)



$V_{(OUT)}$ = 24 V $V_{(IN)}$ = 0 V $V_{\overline{SHDN}}$ = 0 V

図 13. $I_{lkg(OUT)}$ vs Temperature with V_{IN} = 0 V



$V_{(OUT)}$ = 0 V $V_{(IN)}$ = –24 V $V_{\overline{SHDN}}$ = 0 V

図 14. $I_{lkg(OUT)}$ vs Temperature with V_{IN} = –24 V

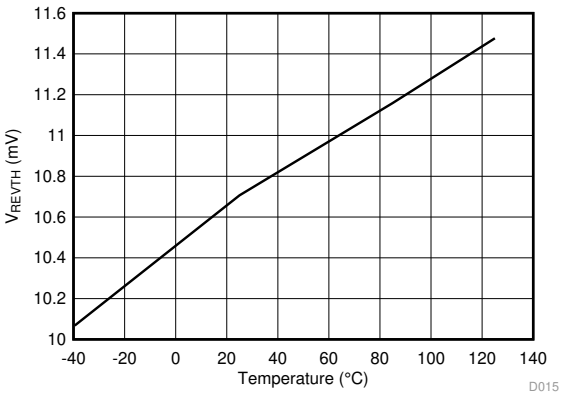


図 15. V_{REVTH} vs Temperature

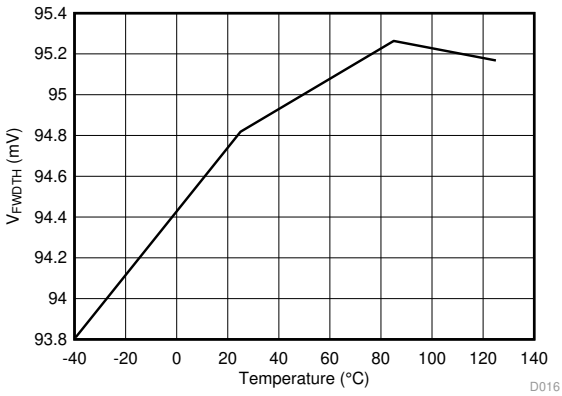


図 16. V_{FWDTH} vs Temperature

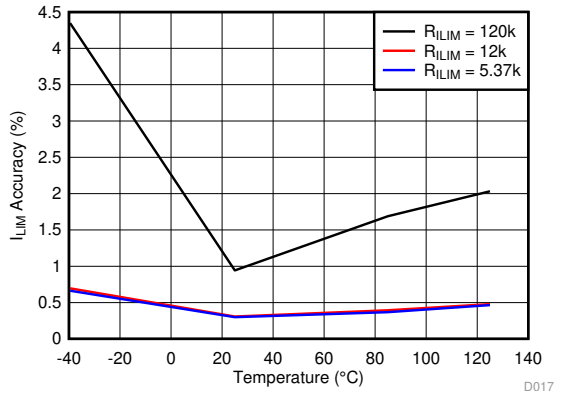
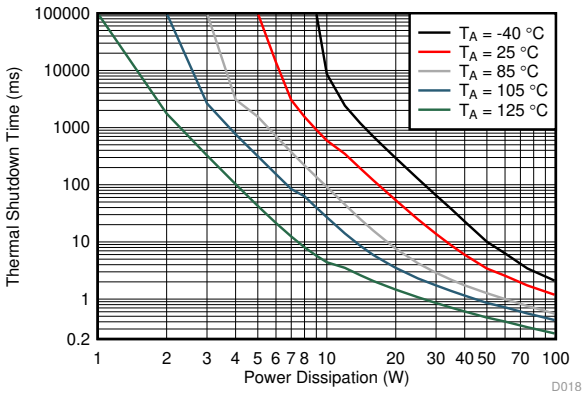


図 17. I_{LIM} Accuracy vs Temperature with V_{IN} = 24 V



Taken on 2-layer PCB with 0.07-mm thick copper and copper area of 10.5 cm^2 connected to PowerPAD.

図 18. Thermal Shutdown Time vs Power Dissipation

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7 Parameter Measurement Information

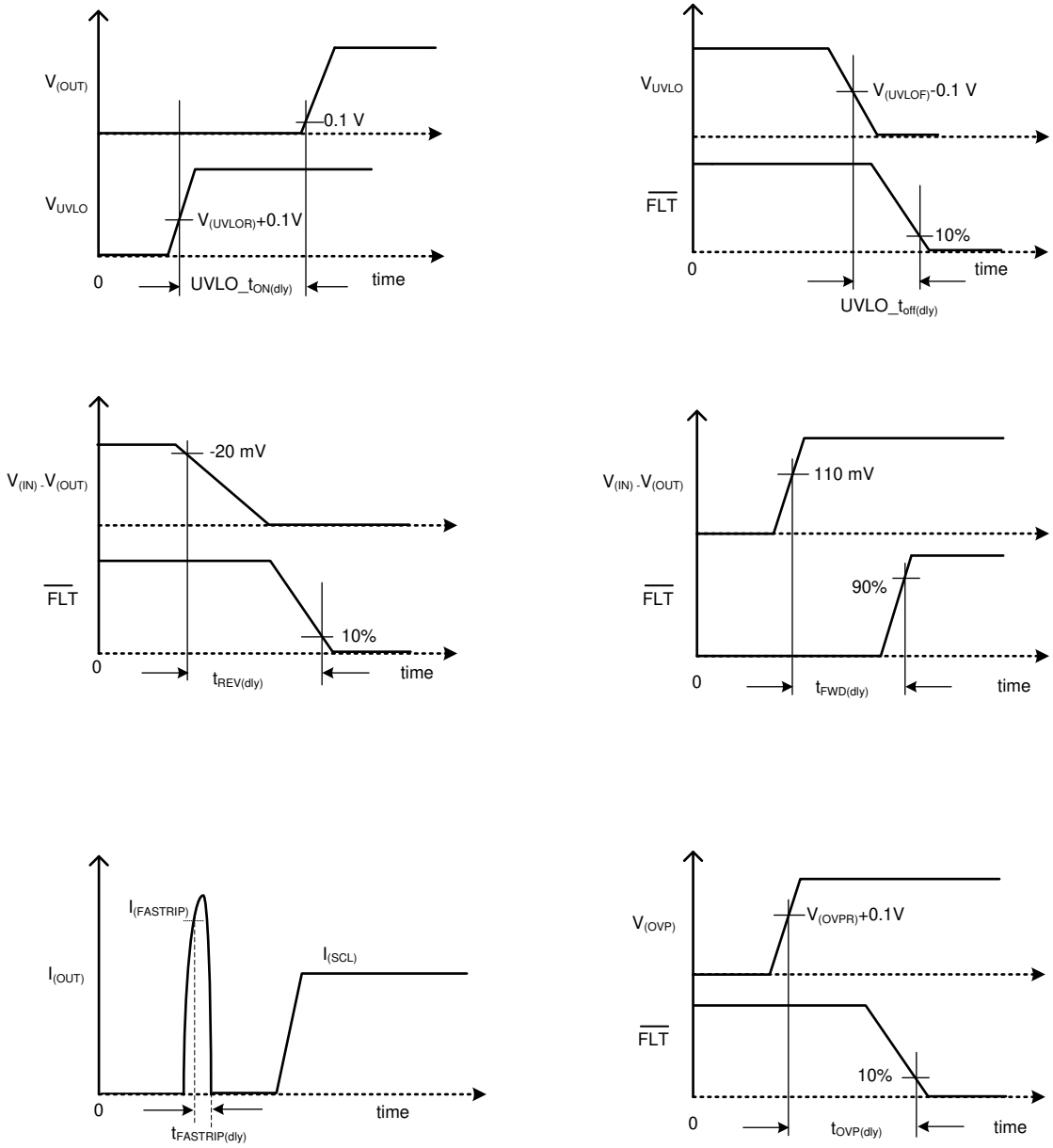

図 19. Timing Waveforms

8 Detailed Description

8.1 Overview

LM76202-Q1 is an ideal diode with integrated back-to-back FETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 4.2 V to 60 V. The device integrates reverse battery input, reverse current, overvoltage, undervoltage, overcurrent and short circuit protection. The precision overcurrent limit (±5% at 1A) helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.1 A and 2.23 A with an external resistor. The device monitors the bus voltage for brown-out and overvoltage protection, asserting the FLTb pin to notify downstream systems.

The device is designed to protect systems such as ADAS camera supplies against sudden output short to battery events. The device monitors V(IN) and V(OUT) to provide true reverse blocking from output when output short to battery fault condition or input power fail condition is detected. The internal robust protection control blocks of the LM76202-Q1 device along with its ±60 V rating helps to simplify the system designs for the various ISO and LV124 compliance ensuring complete protection of the load and the device.

The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The LM76202-Q1 device is also designed to control redundant power supply systems.

Additional features of the LM76202-Q1 device include:

- Reverse input battery protection
- Reverse current blocking
- Current monitor output for health monitoring of the system
- Electronic circuit breaker operation with overload timeout using MODE pin
- A choice of latch off or automatic restart mode response during current limit fault using MODE pin
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for brown-out and overvoltage faults
- Look ahead overload current fault indication (see the *Look Ahead Overload Current Fault Indicator* section)

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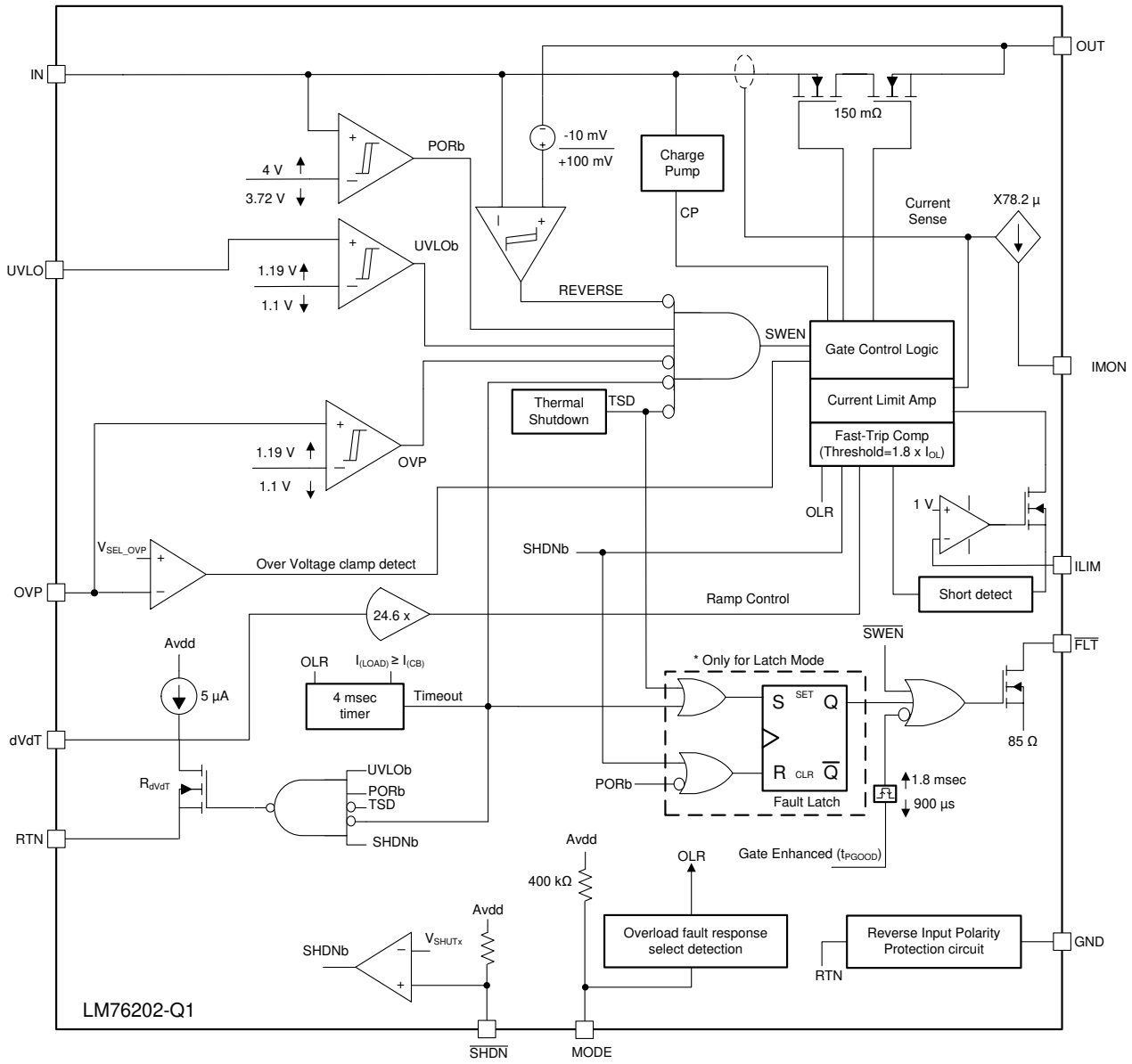
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

This section describes the undervoltage comparator input. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input power fail or input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 90 mV. To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to RTN as shown in 図 20.

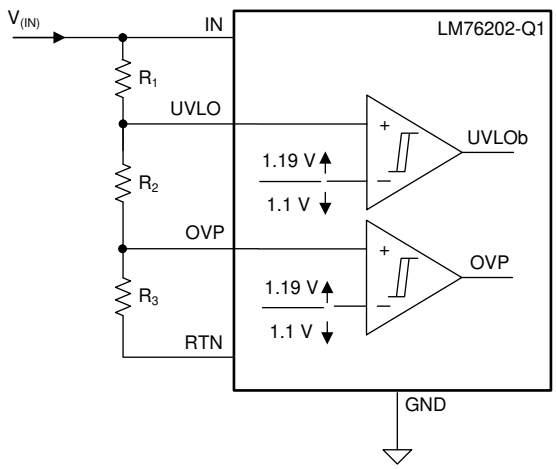


図 20. UVLO and OVP Thresholds Set by R_1, R_2 and R_3

If the undervoltage lockout (UVLO) function is not needed, the UVLO terminal must be connected to the IN terminal. UVLO terminal must not be left floating.

The device also implements an internal power ON reset (POR) function on the IN terminal. The device disables the internal circuitry when the IN terminal voltage falls below internal POR threshold $V_{(PORF)}$. The internal POR threshold has a hysteresis of 275 mV.

8.3.2 Overvoltage Protection (OVP)

The device incorporates circuitry to protect the system during overvoltage conditions. This device features an overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold, connect a resistor divider from IN supply to OVP terminal to RTN as shown in 図 21. OVP Overvoltage Cut-off response is shown in 図 22. OVP pin must not be left floating. If OVP pin could be floating due to dry soldering, an additional zener diode at the output will be required for protection from over voltage.

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Feature Description (continued)

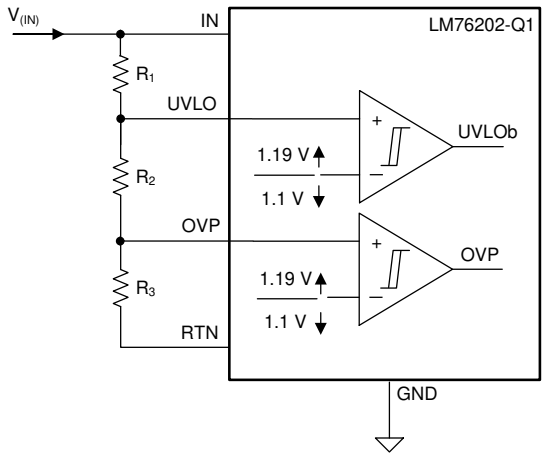

図 21. OVP Threshold Setting

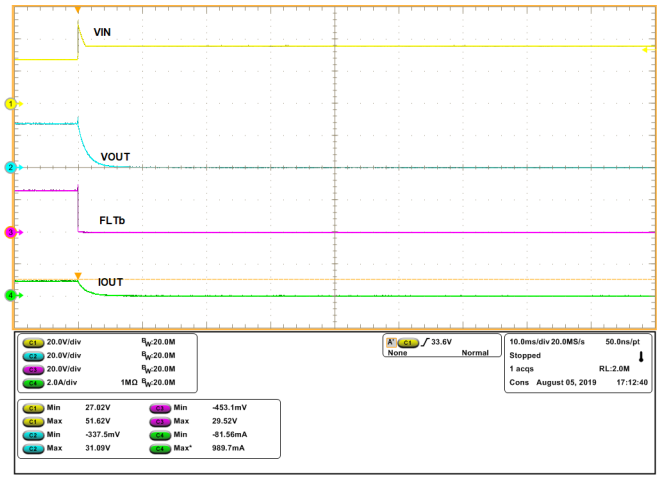

図 22. OVP Overvoltage Cut-Off

Programmable overvoltage clamp can also be achieved using LM76202-Q1 by connecting the resistor ladder from Vout to OVP to RTN as shown in 図 23 . This results in clamping of output voltage close to OVP set-point by resistors R1 and R2. as shown in 図 24. This scheme will also help in achieving minimal system Iq during off state. For this OVP configurataion, use R1 > 90 kΩ.

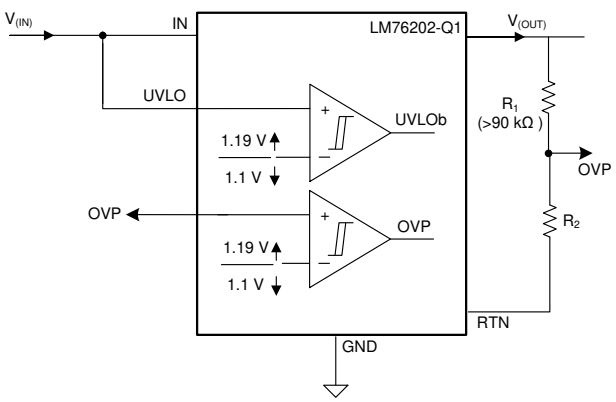

図 23. Programmable OV Clamp

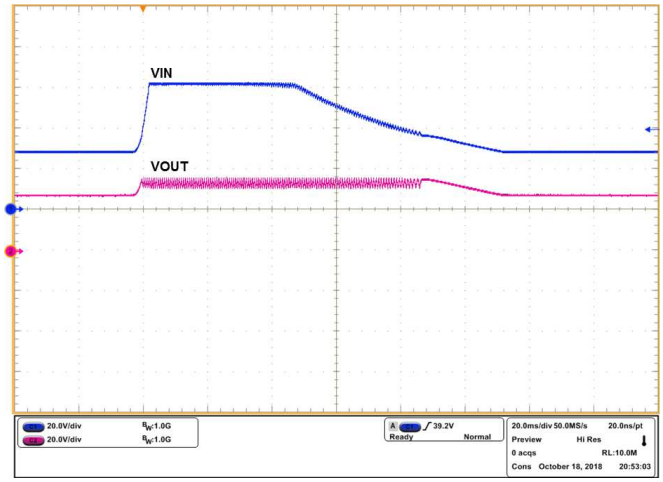

図 24. Programmable Overvoltage Clamp Response

The LM76202-Q1 device also features an internally fixed 38 V overvoltage clamp (V_{OVC}) functionality. The OVP terminal of theLM76202-Q1 device must be connected to the RTN terminal directly as shown in 図 25. The LM76202-Q1 clamps the output voltage to V_{OVC}, when the input voltage exceeds 38 V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is $P_D = (V_{IN} - V_{OVC}) \times I_{OUT}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown. 図 26 illustrates the overvoltage clamp functionality.

Feature Description (continued)

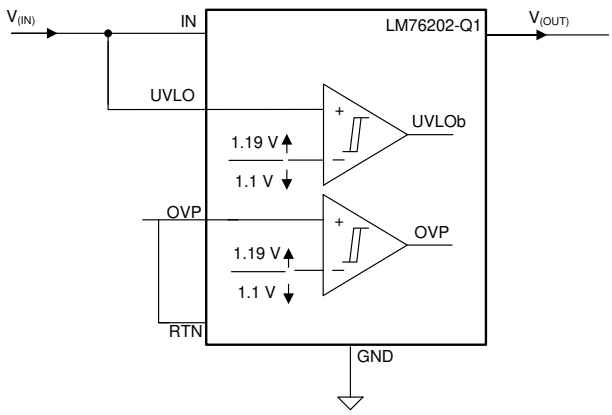

図 25. Internal Fixed OV Clamp Setting

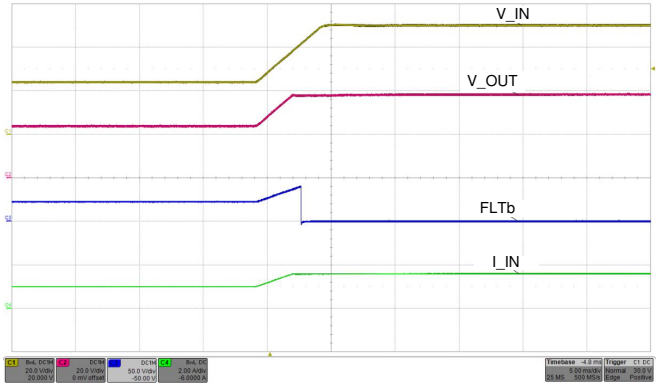

図 26. Internal OV Clamp Response

8.3.3 Reverse Battery Protection

To protect the electronic systems from reverse battery voltage due to miswiring, often a power component like a schottky diode is added in series with the supply line as shown in 図 27. These additional discretes result in a lossy and bulky protection solution. The LM76202-Q1 devices feature fully integrated reverse input supply protection and does not need an additional diode. These devices can withstand a reverse voltage of –60 V without damage. 図 28 illustrates the reverse input polarity protection functionality.

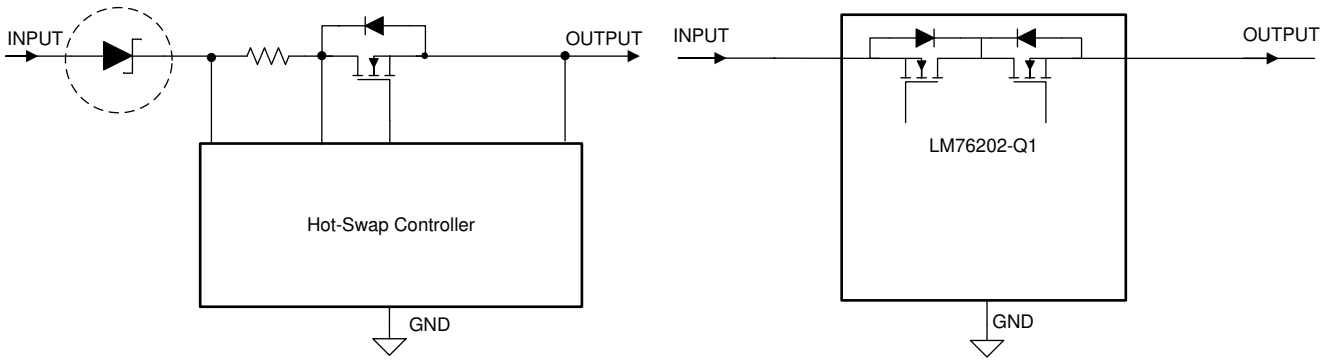

図 27. Reverse Battery Protection Circuits - Discrete vs LM76202-Q1

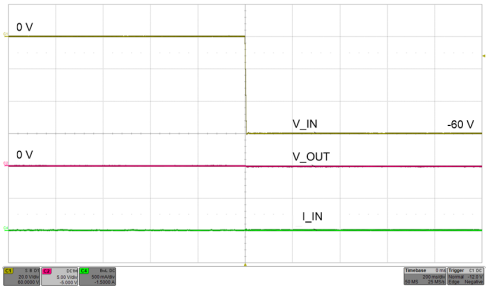

図 28. Reverse Input Supply Protection at –60 V

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Feature Description (continued)

8.3.4 Hot Plug-In and In-Rush Current Control

The device is designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to RTN defines the slew rate of the output voltage at power-on as shown in 図 29 and 図 30.

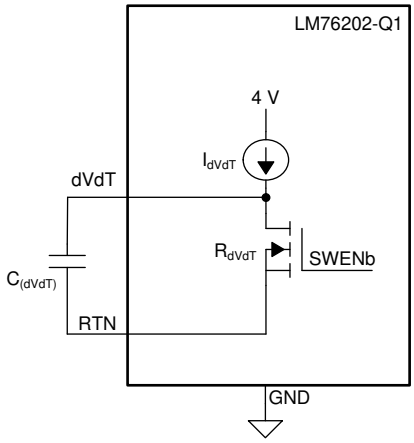


図 29. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When the terminal is left floating, the devices set an internal output voltage ramp rate of 23.9 V / 1.6 ms. A capacitor can be connected from dVdT pin to RTN to program the output voltage slew rate slower than 23.9 V / 1.6 ms. Use 式 1 and 式 2 to calculate the external $C_{(dVdT)}$ capacitance.

式 1 governs slew rate at start-up.

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{Gain_{(dVdT)}}\right) \times \left(\frac{dV_{(OUT)}}{dt}\right)$$

where

- $I_{(dVdT)}$ = 4.7 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$
- $Gain_{(dVdT)}$ = dVdT to V_{OUT} gain = 24.6 (1)

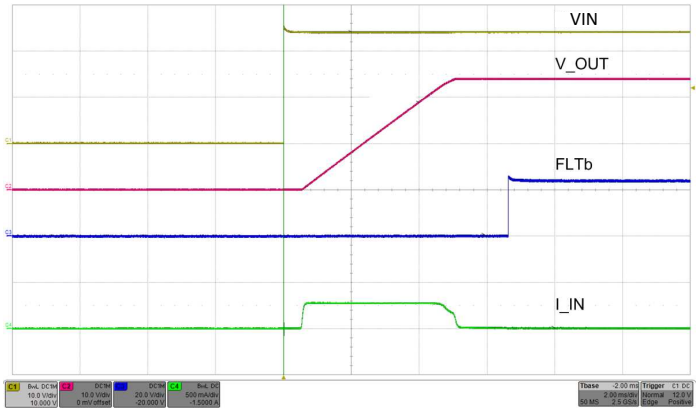
The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using 式 2.

$$t_{dVdT} = 8.7 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

The inrush current can be calculated by 式 3

$$I_{INRUSH} = C_{OUT}/[8.7 \times 10^3 \times C_{dVdT}] \quad (3)$$

Feature Description (continued)



C_{dVdT} = 22 nF C_{OUT} = 47 µF R_{ILIM} = 5.36 kΩ

図 30. Hot Plug-In and In-Rush Current Control at 24-V Input

8.3.5 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

8.3.5.1 Overload Protection

The device offers following choices for the overload protection fault response:

- Active current limiting (Auto-retry and Latch-off modes)
- Electronic Circuit Breaker with overload timeout (Auto-retry mode)

See the configurations in 表 1 to select a specific overload fault response.

表 1. Overload Fault Response Configuration

MODE Pin Configuration	Overload Protection Type
Open	Electronic circuit breaker with auto-retry
Shorted to RTN	Active current limiting with auto-retry
A 402-kΩ resistor across MODE pin to RTN pin	Active current limiting with latch-off

8.3.5.1.1 Active Current Limiting

When the active current limiting mode is selected, during overload events, the device continuously regulates the load current to the overcurrent limit $I_{(OL)}$ programmed by the $R_{(ILIM)}$ resistor as shown in 式 4.

$$I_{OL} = \frac{12}{R_{(ILIM)}}$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ (4)

During an overload condition, the internal current-limit amplifier regulates the output current to $I_{(LIM)}$. The $\overline{FLT}$ signal assert after a delay of t_{PGOODF}. The output voltage droops during the current regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turn off. The device configured in latch-off mode stays latched off until it is reset by either of the following conditions:

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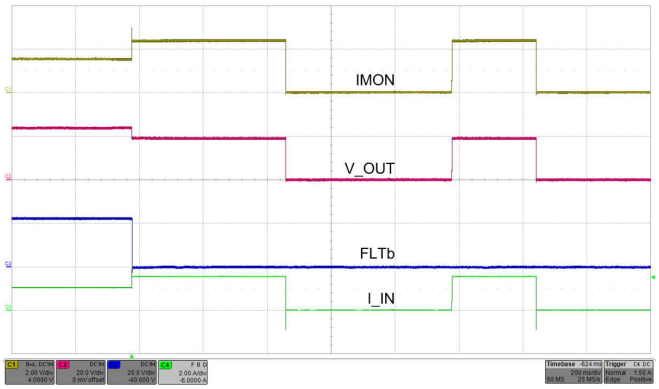
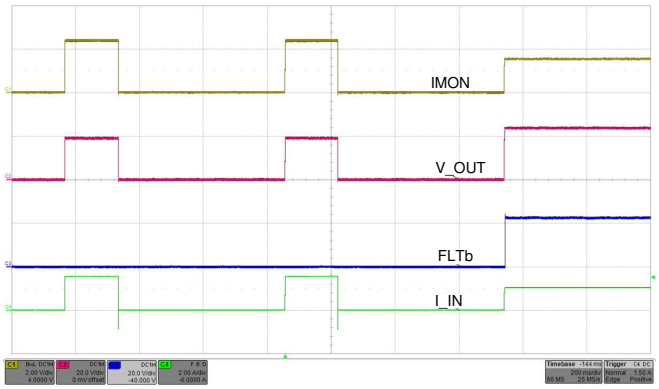
- Cycling $V_{(IN)}$ below $V_{(PORF)}$
- Toggling $\overline{SHDN}$

When the device is configured in auto-retry mode, it commences an auto-retry cycle $t_{CBretry(dly)}$ ms after T_J < [$T_{(TSD)}$ – 10°C]. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. 図 31 and 図 32 illustrates the behavior of the system during current limiting with auto-retry functionality.



Load transition from 22 Ω to 12 Ω
R_{ILIM} = 8 kΩ
MODE pin connected to RTN

図 31. Auto-Retry MODE Fault Behavior



R_{ILIM} = 5.36 kΩ

図 32. Response During Coming Out of Overload Fault

8.3.5.1.2 Electronic Circuit Breaker with Overload Timeout, MODE = OPEN

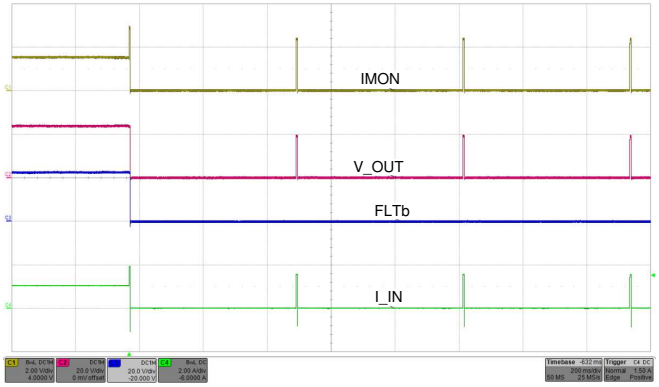
In this mode, during overload events, the device allows the overload current to flow through the device until $I_{(LOAD)}$ < $I_{(FASTRIP)}$. The circuit breaker threshold $I_{(CB)}$ can be programmed using the $R_{(ILIM)}$ resistor, as shown in 式 5.

$$I_{(CB)} = \frac{12}{R_{(ILIM)}} + 0.03A$$

where

- $I_{(CB)}$ is circuit breaker current threshold in A
- $R_{(ILIM)}$ is the current limit resistor in kΩ (5)

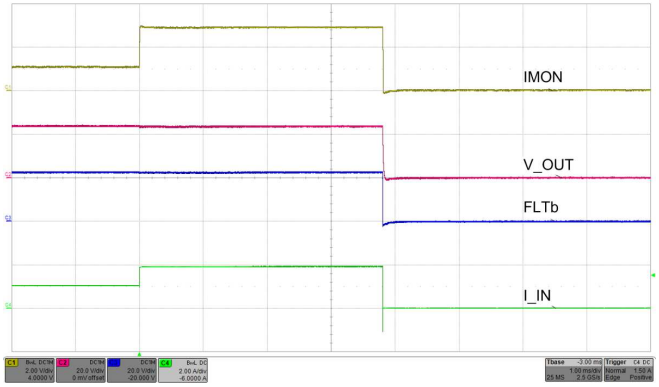
The device commences an auto-retry cycle after a delay of $t_{CBretry(dly)}$. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. 図 33 and 図 34 illustrate behavior of the system during electronic circuit breaker with auto-retry functionality.



MODE left floating
R_{ILIM} = 8 kΩ

Load Transition from 22 Ω to 12 Ω

図 33. Circuit Breaker Functionality

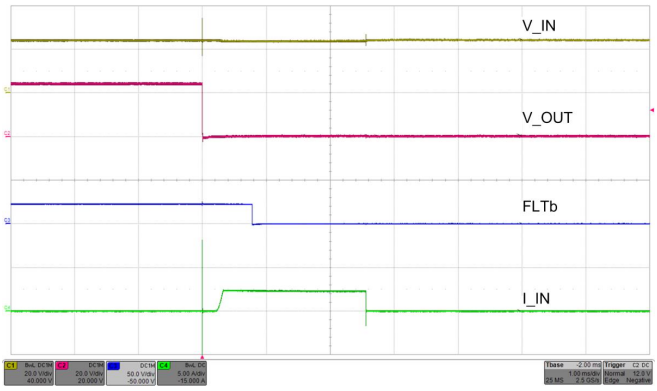


Load Transition from 22 Ω to 12 Ω , R_{ILIM} = 8 kΩ

図 34. Zoomed at the Instance of Load Step

8.3.5.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases very rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. The fast-trip comparator turns off the internal FET after a duration of $t_{FASTTRIP(dly)}$, when the current through the FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The fast-trip threshold is internally set to 87% higher than the programmed overload current limit ($I_{(FASTRIP)} = 1.87 \times I_{(OL)} + 0.015$). The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device behaves similar to overload condition. 図 35 and 図 36 illustrate the behavior of the system when the current exceeds the fast-trip threshold.



VIN = 24 V, R_{ILIM} = 5.36 kΩ

図 35. Output Hot Short Functionality at 24-V Input

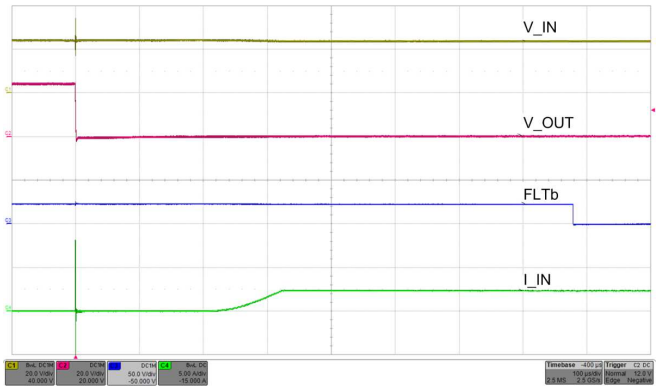


図 36. Zoomed at the Instance of Output Short

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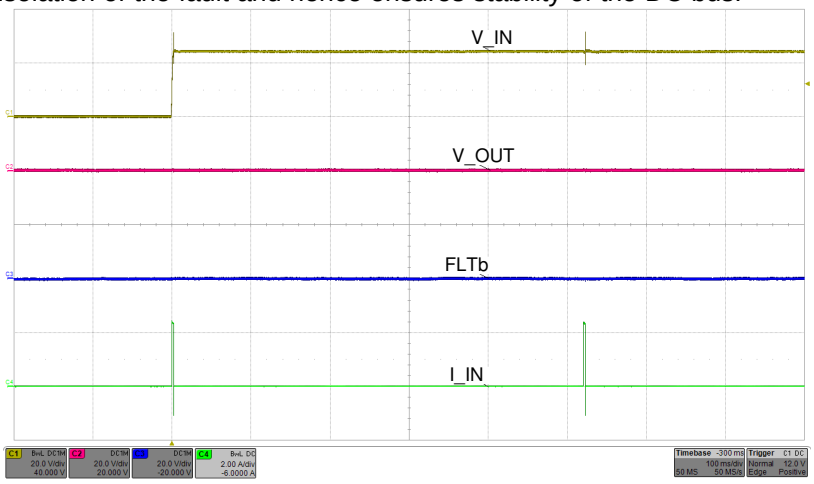
8.3.5.2.1 Start-Up With Short-Circuit On Output

When the device is started with a short-circuit on the output end, it limits the load current to the current limit $I_{(OL)}$, and behaves similarly to the overload condition. 図 37 illustrates the behavior of the device in this condition. This feature helps in quick isolation of the fault and hence ensures stability of the DC bus.



MODE pin connected to RTN

VIN = 24 V R_{ILIM} = 5.36 kΩ

図 37. Start-Up With Short on Output

8.3.5.3 FAULT Response

The $\overline{FLT}$ open-drain output asserts (active low) under following conditions:

- Fault events such as undervoltage, overvoltage, overload, reverse current and thermal shutdown conditions
- When the device enters low current shutdown mode when $\overline{SHDN}$ is pulled low
- During start-up when the internal FET GATE is not fully enhanced (for example: V_{OUT} has not reached V_{IN}).

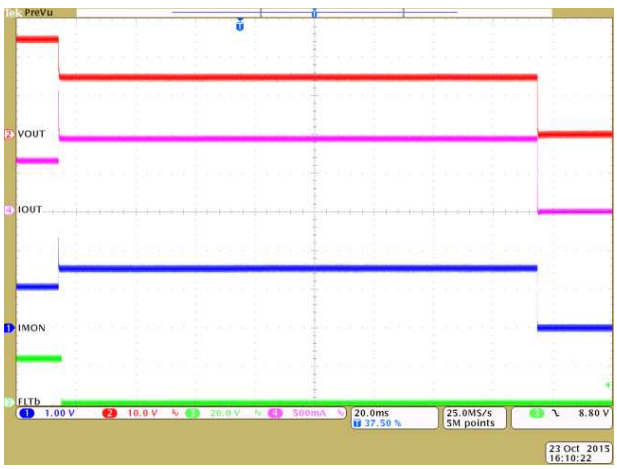
The $\overline{FLT}$ output does not assert in the event of reverse voltage on Input.

The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry.

The $\overline{FLT}$ signal can also be used as Power Good indicator to the downstream loads like DC-DC converters. An internal Power Good (PGOOD) signal is OR'd with the fault logic. During start-up, when the device is operating in dVdT mode, PGOOD and $\overline{FLT}$ remains low and is de-asserted after the dVdT mode is completed and the internal FET is fully enhanced and V_{OUT} has reached V_{IN}. The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by the downstream converters. Rising deglitch delay is determined by $t_{PGOOD(degl)}$ = Maximum {(900 + 20 × $C_{(dVdT)}$), t_{PGOODR}}, where $C_{(dVdT)}$ is in nF and $t_{PGOOD(degl)}$ is in µs. $\overline{FLT}$ can be left open or connected to RTN when not used. $V_{(IN)}$ falling below $V_{(PORF)}$ resets $\overline{FLT}$.

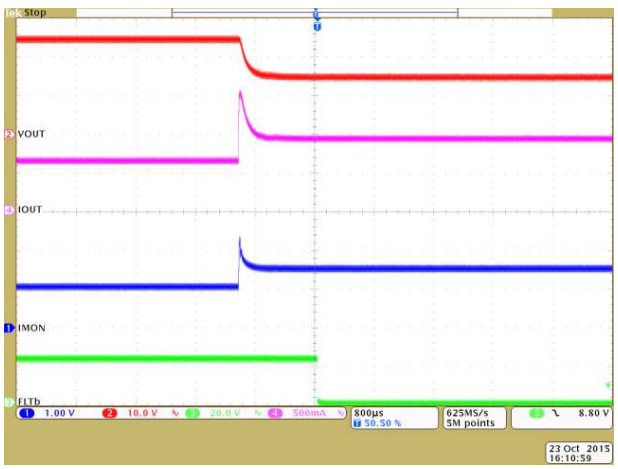
8.3.5.3.1 *Look Ahead* Overload Current Fault Indicator

With the device configured in current limit operation and when the overload condition exists for more than t_{PGOODF}, the $\overline{FLT}$ asserts to warn of impending turnoff of the internal FETs due to the subsequent thermal shutdown event. 図 38 and 図 39 depict this behavior. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation.



R_{ILIM} = 12 kΩ MODE pin connected to RTN Load transient event from 37 Ω to 15 Ω

図 38. Look Ahead Overload Current Fault Indication



R_{ILIM} = 12 kΩ MODE pin connected to RTN Load transient event from 37 Ω to 15 Ω

図 39. Output Turnoff Due to Thermal Shutdown With $\overline{FLT}$ Asserted in Advance

8.3.5.4 Current Monitoring

The current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to RTN terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage range ($V_{(IMONmax)}$) for monitoring the current is limited to minimum of ([$V_{(IN)}$ – 1.5 V, 4 V]) to ensure linear output. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by 式 6.

$$R_{(IMONmax)} = \frac{\text{Min}\,[(V_{(IN)} - 1.5),\ 4\ V]}{1.8 \times I_{(LIM)} \times GAIN_{(IMON)}} \tag{6}$$

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The output voltage at IMON terminal is calculated using 式 7 and 式 8.

For I_{OUT} > 50 mA,

$$V(IMON) = \left[I(OUT) \times GAIN(IMON)\right] \times R(IMON)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$
- $I_{(OUT)}$ is the load current
- $I_{(MON_OS)}$ = 2 µA (Typical) (7)

For I_{OUT} < 50 mA (typical), IMON output current is close to $I_{(MON_OS)}$ and 式 8 provides the voltage output with R_{IMON}.

$$V(IMON) = \left(I(IMON_OS)\right) \times R(IMON) \quad (8)$$

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

In case of reverse input polarity fault, an external 100-kΩ resistor is recommended between IMON pin and ADC input to limit the current through the ESD protection structures of the ADC.

8.3.5.5 IN, OUT, RTN and GND Pins

The device has two pins for input (IN) and output (OUT). All IN pins must be connected together and to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended input operating voltage range is 4.2 V to 60 V. Similarly all OUT pins must be connected together and to the load. $V_{(OUT)}$, in the ON condition, is calculated using 式 9.

$$V(OUT) = V(IN) - \left(RON \times I(OUT)\right)$$

Where,

- R_{ON} is the total ON resistance of the internal FETs. (9)

The GND pin must be connected to the system ground. RTN is the device ground reference for all the internal control blocks. Connect the device support components: $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, $R_{(MODE)}$ and resistors for UVLO and OVP with respect to the RTN pin. Internally, the device has reverse input polarity protection block between RTN and the GND terminal. Connecting RTN pin to GND pin disables the reverse input polarity protection feature. if negative input voltage is applied on IN pins with RTN pin connected to GND, the device can get damaged.

8.3.5.6 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FETs, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches off or commences an auto-retry cycle 540 ms after T_J < [$T_{(TSD)}$ – 10°C]. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

8.3.5.7 Low Current Shutdown Control ($\overline{SHDN}$)

The internal FETs and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below $V_{(SHUTF)}$ threshold with a micro-controller GPIO pin as shown in 図 40. The device quiescent current reduces to 16 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{SHDN}$ must be pulled up to $V_{(SHUTR)}$ threshold. Once the device is enabled, the internal FETs turns on with dVdT mode.

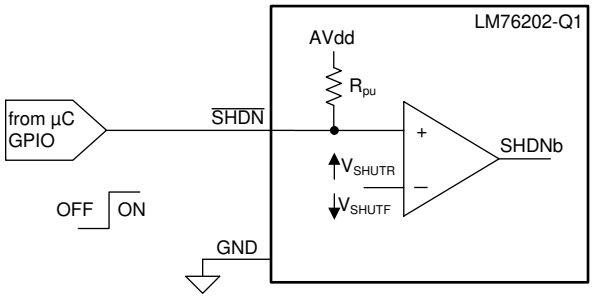

図 40. Shutdown Control

8.4 Device Functional Modes

The device responds differently to overload and short circuit conditions. The operational differences are explained in 表 2.

表 2. Device Operational Differences Under Different MODE Configurations

Mode Pin Configuration	Mode Connected To RTN (Current Limit With Auto-Retry)	A 402-KΩ Resistor Connected Between Mode And RTN Pins (Current Limit With Latchoff)	Mode Pin = Open
Start-up	Inrush current controlled by dVdT		
	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$
			Fault timer runs when current is limited to $I_{(OL)}$
			Fault timer expires after $t_{CB(dly)}$ causing the FETs to turnoff
	If $T_J > T_{(TSD)}$, device turns off	If $T_J > T_{(TSD)}$, device turns off	Device turns off if $T_J > T_{(TSD)}$ before timer expires
Overcurrent response	Current is limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Current is limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Current is allowed through the device if $I_{(LOAD)} < I_{(FASTTRIP)}$
	Power dissipation increases as $V_{(IN)} – V_{(OUT)}$ increases	Power dissipation increases as $V_{(IN)} – V_{(OUT)}$ increases	Fault timer runs when the current increases above $I_{(OL)}$
			Fault timer expires after $t_{CB(dly)}$ causing the FETs to turnoff
	Device turns off when $T_J > T_{(TSD)}$	Device turns off when $T_J > T_{(TSD)}$	Device turns off if $T_J > T_{(TSD)}$ before timer expires
	Device attempts restart 540 ms after $T_J < [T_{(TSD)} – 10°C]$	Device remains off	Device attempts restart 540 ms after $T_J < [T_{(TSD)} – 10°C]$.
Short-circuit response	Fast turnoff when $I_{(LOAD)} > I_{(FASTRIP)}$		
	Quick restart and current limited to $I_{(OL)}$, follows standard start-up		

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9 Application and Implementation

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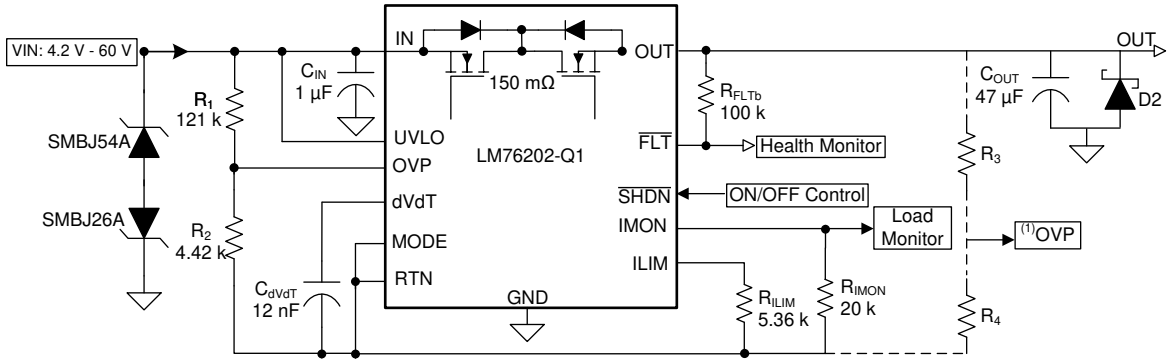
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is an automotive ideal diode, typically used for load protection in automotive applications. It can operate from 24-V battery with programmable current limit, overvoltage, undervoltage and reverse polarity protections. The device provides robust protection against reverse current and transients (such as ISO 7637-2 Pulse 1 and ISO 16750-2 Pulse 5b) due to cables and switches in different automotive systems such as an ECU. The device also provides robust protection for output short to battery, output short to GND, reverse battery and input overvoltage.

The *Detailed Design Procedure* section can be used to select component values for the device.

9.2 Typical Application



(1) OVP connection for Programmable over voltage clamp. See *Overvoltage Protection (OVP)*.

図 41. 24-V, 2-A Ideal Diode Load Protection Circuit for Automotive ECU

9.2.1 Design Requirements

表 3 shows the Design Requirements for LM76202-Q1. In addition to below requirements, the circuit is designed to provide protection for transients as per ISO 7637-2 Pulse 1 and ISO 16750-2 Pulse 5b.

表 3. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	4.2 to 60 V
$V_{(UV)}$	Undervoltage lockout set point	4 V
$V_{(OV)}$	Overvoltage cutoff set point	33.8 V
$I_{(LIM)}$	Current limit	2.23 A
$C_{(OUT)}$	Load capacitance	47 µF
$I_{(LOAD)}$	Load current	2 A

9.2.2 Detailed Design Procedure

9.2.2.1 Step by Step Design Procedure

To begin the design process, the designer must know the following parameters:

- Operating voltage range

- Maximum output capacitance
- Start-up time
- Maximum current limit
- Transient voltage levels

9.2.2.2 Setting Undervoltage Lockout and Overvoltage Set Point for Operating Voltage Range

To provide operation in cold crank conditions for automotive batteries, the UVLO is set to POR value (4 V) by connecting UVLO to IN pin and OVP threshold is set from resistors connected from IN pins to provide protection from transient during ISO 16750 Pulse 5b. During the ISO 16750 5b transient, output voltage is cut-off at 33.8 V and provides protection to load from high input voltage during the transient. The overvoltage threshold is calculated by 式 10.

$V_{OVPR} = R_2/(R_1 + R_2) \times V_{OV}$

where

- Overvoltage threshold rising, V_{OVPR} = 1.19 V
- V_{OV} is overvoltage protection voltage (= 33.8 V) (10)

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{23})$ must be chosen to be 20x greater than the leakage current of OVP pin.

9.2.2.3 Programming the Current-Limit Threshold—$R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using 式 4.

$R_{(ILIM)}$ = 5.36 kΩ was selected to set I_{LIM} to 2.23 A.

9.2.2.4 Programming Current Monitoring Resistor—R_{IMON}

The voltage at IMON pin $V_{(IMON)}$ represents the voltage proportional to the load current. This can be connected to an ADC of the downstream system for health monitoring of the system. The $R_{(IMON)}$ must be configured based on the maximum input voltage range of the ADC used. $R_{(IMON)}$ is set using 式 11.

$$R(IMON) = \frac{V(IMON\,max)}{I(LIM) \times 75 \times 10^{-6}} \tag{11}$$

For current monitoring up-to a current of 2.2 A, and considering the operating input voltage range of ADC from 0 V to 4 V, $V_{(IMONmax)}$ is 4 V and $R_{(IMON)}$ is selected as 20 kΩ.

9.2.2.5 Limiting the Inrush Current

To limit the inrush current and power dissipation during start-up, an appropriate value of C_{dVdT} must be selected. The inrush current during start-up is estimated by 式 12. A 12nF capacitance is selected for C_{dVdT} to keep inrush current less than 0.5 A.

$I_{INRUSH} = C_{OUT} / [8.7 \times 10^3 \times C_{dVdt}]$ (12)

9.2.2.5.1 Selection of Input TVS for Transient Protection

To protect the device and the load from input transients exceeding the absolute maximum ratings of the device, a TVS diode is required at input of the device. To meet the requirements of protection for ISO 16750 pulse 5b and ISO 7637 pulse 1 as per 表 4, SMBJ54A and SMBJ26A are selected for protection from transients.

表 4. Input TVS Selection for Transients

Parameter	ISO 16750 Pulse 5b	ISO 7637 Pulse 1 and Reverse Battery	
Maximum Transient Voltage of Pulse (V_T)	65 V	-600V	A bidirectional TVS is required to protect from positive and negative transients
Pulse Current through TVS (I_{Pulse})	$(V_T - V_C)/(R_i)$	$(V_T - V_C)/(R_i)$	R_i = Source impedance. For ISO 16750 Pulse 5b; R_i = 1Ω For ISO 7637 Pulse 1;R_i = 50 Ω

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表 4. Input TVS Selection for Transients (continued)

Parameter	ISO 16750 Pulse 5b	ISO 7637 Pulse 1 and Reverse Battery	
Clamping voltage of TVS (V_C) at Pulse current I_{Pulse}	< 65 V	> –(65 - $V_{OUT-Max}$) V	To keep input voltage below absolute maximum rating of the device. See 式 13 for V_C
Breakdown voltage of TVS (V_{BR})	> 60V	> 28V	To operate with maximum operating input voltage and to protect from maximum reverse battery voltage

$V_C = V_{BR} + I_{Pulse} \times [V_{Clamp-max} - V_{BR}]/[I_{PP} - I_T]$

where

- V_C is the clamping voltage of TVS at I_{Pulse} current through it.
- V_{BR} is break down voltage of TVS with I_T test current through it.
- $V_{Clamp-max}$ is maximum clamping voltage of TVS at peak pulse current I_{PP}
- V_{BR}, I_T, $V_{Clamp-max}$ and I_{PP} are the specifications of the TVS diode. (13)

9.2.3 Application Curves

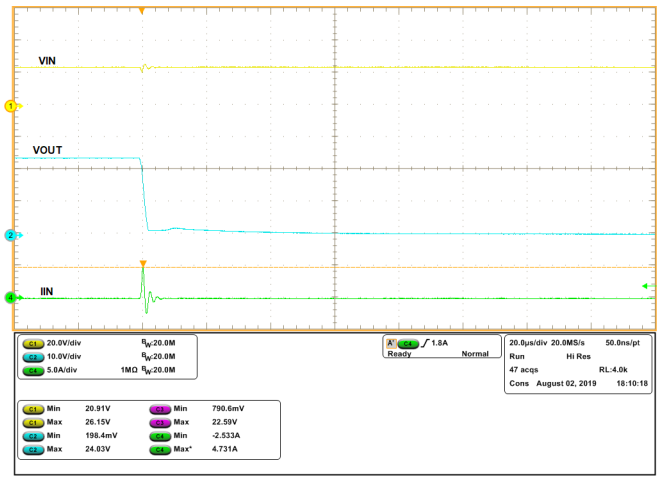

図 42. Protection from Output Short to GND [V_{IN} = 24 V, ILIM = 2.23 A, MODE = RTN]

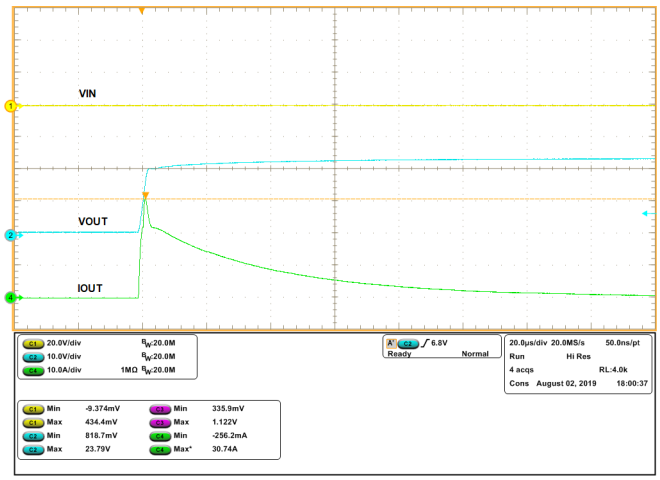

図 43. Protection from Output short to Battery [V_{IN} = Floating, V_{OUT} = 24 V, ILIM = 2.23 A, MODE = RTN]

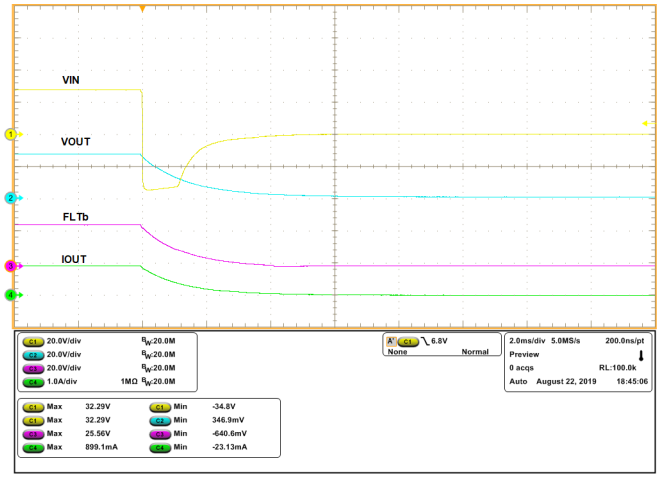

図 44. Protection from ISO 7637-2 Pulse 1 [24 V Battery, Transient Voltage = –600 V , R_{LOAD} = 28 Ω]

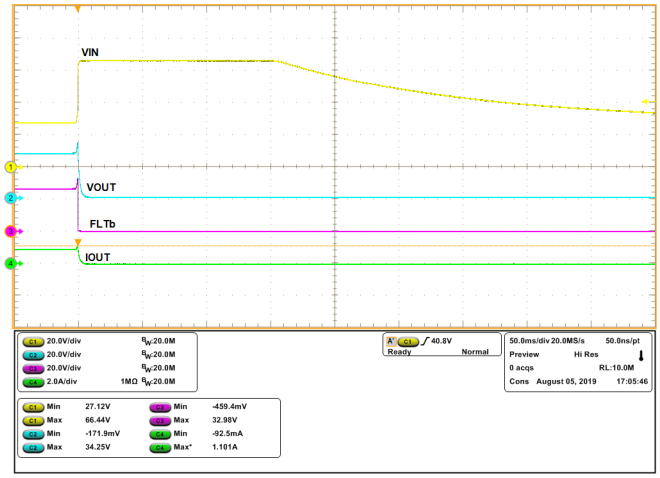

図 45. Protection from ISO 16750-2 Pulse 5b [24 V Battery, Transient Voltage = 65 V , R_{LOAD} = 28 Ω]

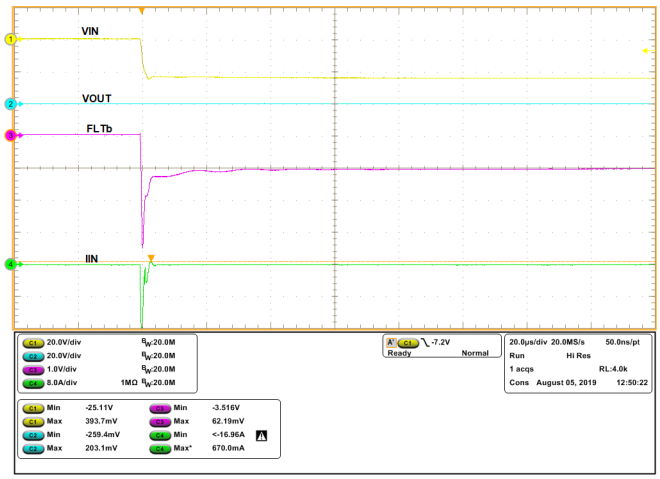

図 46. Protection from Reverse Battery [V_{IN} = -24 V, V_{OUT} = 0 V, ILIM = 2.23 A]

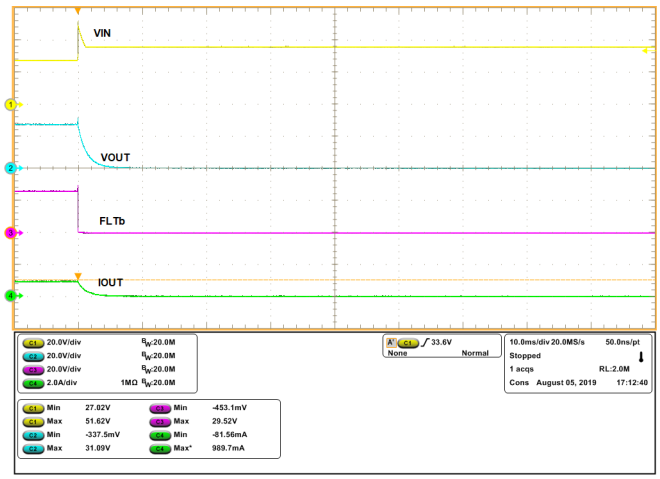

図 47. Protection from OverVoltage at Input [V_{IN} = 36 V, R_{LOAD} = 28 Ω, ILIM = 2.23 A]

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10 Power Supply Recommendations

The device is designed for the supply voltage range of 4.2 V ≤ V_{IN} ≤ 60 V. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A ceramic capacitor at input ($C_{(IN)}$) with value more than 1µF to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with 式 14.

$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}}$$

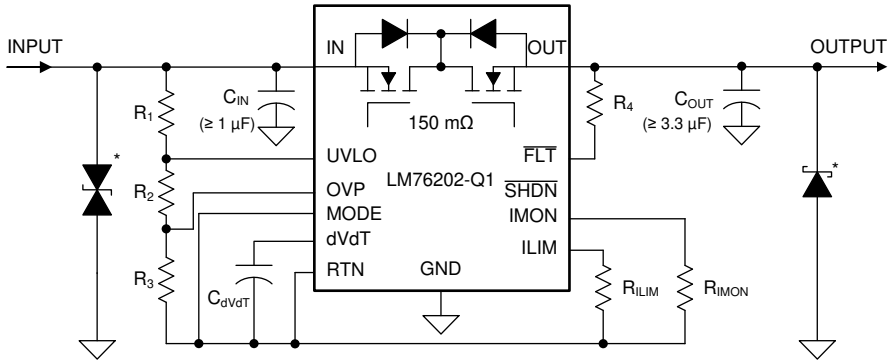
where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

(14)

Automotive applications could require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients include ISO 7637 Pulse 1, Output short to battery, Output short to GND and reverse battery at input.

The circuit implementation with optional protection components (TVS Diode at Input and schottky diode at output) is shown in 図 48. For protection from automotive transients similar to ISO 7637 Pulse 1, Output short to battery , output short to GND and reverse battery, use C_{IN} ≥ 1 µF and C_{OUT} ≥ 3.3 µF. For selection of TVS diode and other components, see *Application Information*.



* Optional components needed for suppression of transients

図 48. Circuit Implementation for Automotive Transient Protection

11 Layout

11.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND. Use C_{IN} ≥ 1 µF for automotive transient protection. See *Transient Protection*.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the device. See 図 49 for PCB layout example with HTSSOP package.
- High current carrying power path connections must be as short as possible and must be sized to carry atleast twice the full-load current.
- RTN, which is the reference ground for the device must be a copper plane or island.
- Locate all the device support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, and MODE, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the RTN with shortest trace length.
- The trace routing for the R_{ILIM} and $R_{(IMON)}$ components to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board RTN plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Designs that do not need reverse input polarity protection can have RTN, GND and PowerPAD connected together. PowerPAD in these designs can be connected to the PCB ground plane.

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11.2 Layout Example

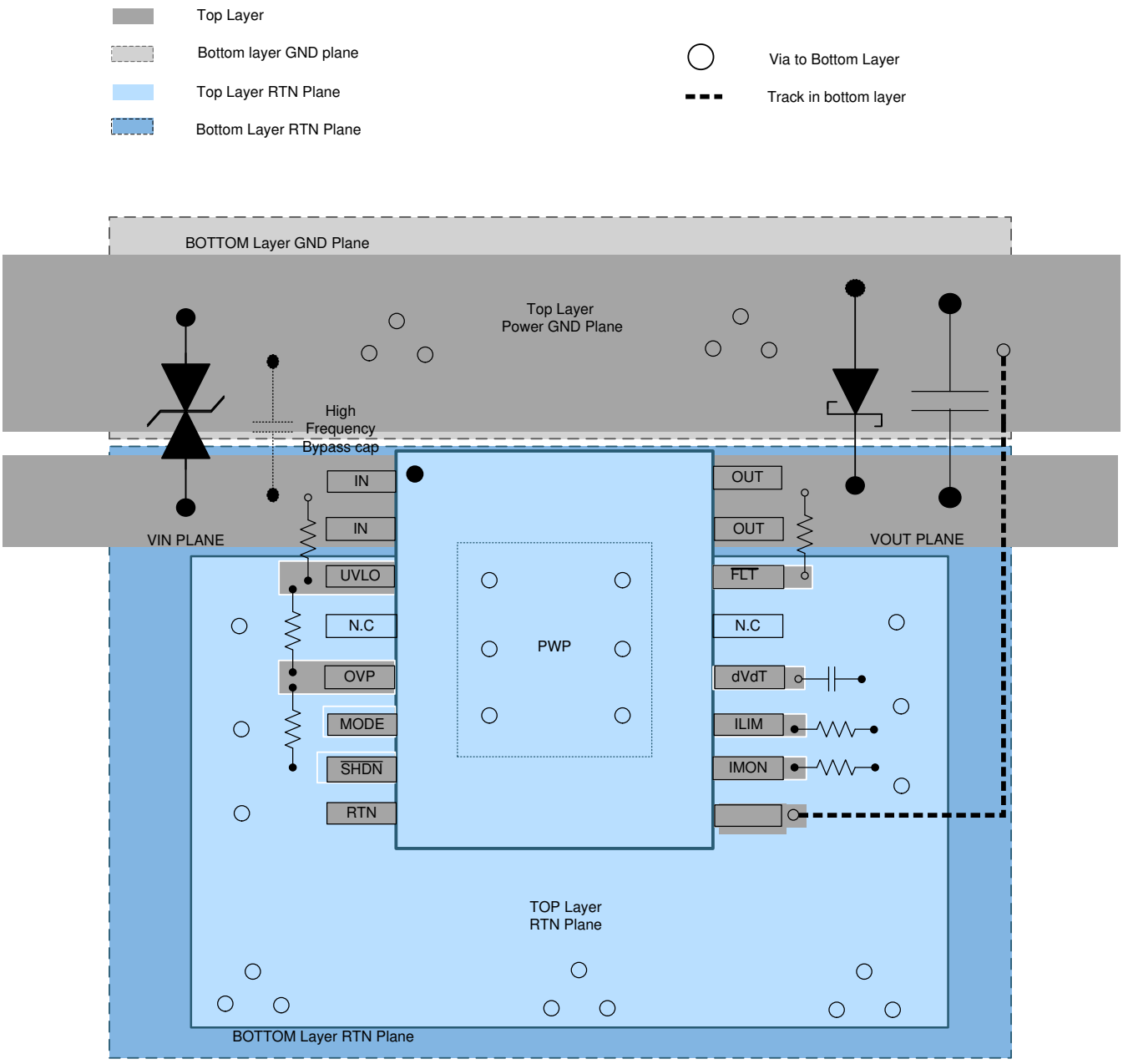

図 49. Typical PCB Layout Example With HTSSOP Package With a 2-Layer PCB

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『LM76202-Q1 EVMユーザー・ガイド』*

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM76202QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M76202Q
LM76202QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M76202Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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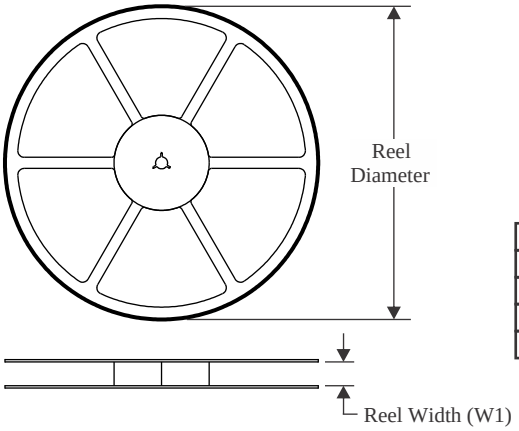
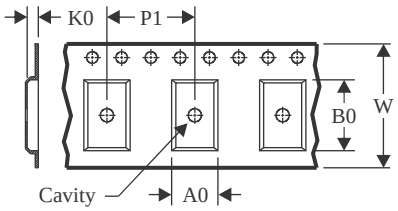
TAPE AND REEL INFORMATION

REEL DIMENSIONS

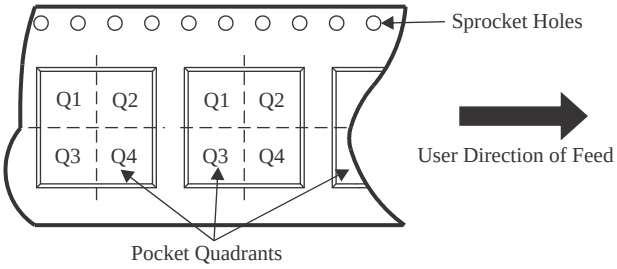


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

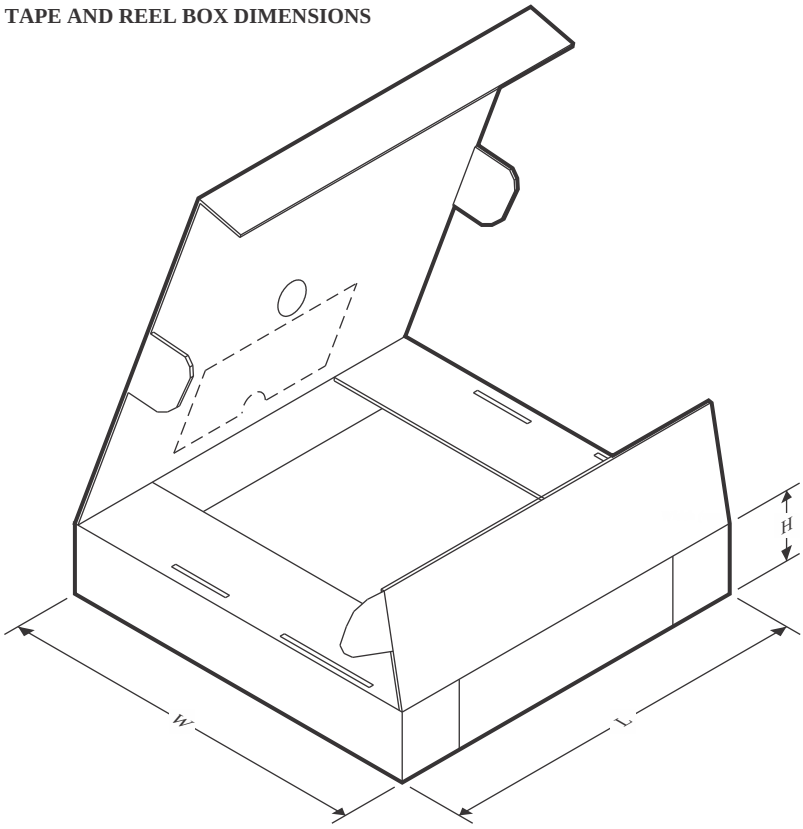
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM76202QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM76202QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

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