LM7480 3V～65V、バック・ツー・バック NFET 駆動、理想ダイオード・コントローラ

1 特長

- 拡張温度アプリケーション向けに認定済み
  - デバイス温度:
    -55℃～+125℃の動作時周囲温度範囲
- 3V～65V の入力範囲
- 最低 -65V までの逆入力保護
- 共通ドレインと共通ソースの構成で外付けのバック・ツー・バック N チャネル MOSFET を駆動
- アノードからカソードへ 10.5mV の順方向電圧降下レギュレーションを行う理想ダイオード動作 (LM74800)
- 低いスレッショルド (-4.5mV) と高速応答 (0.5µs) の逆電流検出
- 20mA のピーク・ゲート (DGATE) ターンオン電流
- 2.6A のピーク DGATE ターンオフ電流
- 調整可能な過電圧保護機能
- 低シャットダウン電流 (EN/UVLO = Low):2.87µA
- 省スペースの 12 ピン WSON パッケージで供給

2 アプリケーション

- アビオニクス入力の逆極性保護
  - センサ
  - 画像処理
  - レーダー
- 冗長化電源用のアクティブ OR

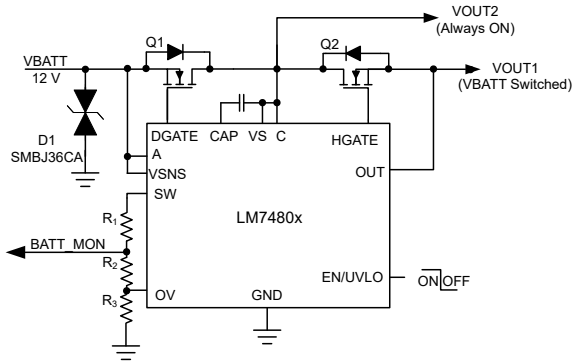
3 概要

LM7480 理想ダイオード・コントローラは外付けのバック・ツー・バック N チャネル MOSFET を駆動および制御して、電力パスの ON/OFF 制御と過電圧保護を備えた理想ダイオード整流器をエミュレートします。入力電源電圧範囲が 3V～65V と広いため、12V および 24V 入力電源システムを保護および制御できます。このデバイスは最低 -65V の負の電源電圧に耐え、この電圧から負荷を保護できます。内蔵の理想ダイオード・コントローラ (DGATE) は第 1 の MOSFET を駆動し、逆電流保護および出力電圧保持用のショットキー・ダイオードを置き換えます。電力パスの第 2 の MOSFET により、HGATE 制御を使用した負荷の切断 (ON/OFF 制御) と過電圧保護が可能です。このデバイスには可変の過電圧カットオフ保護機能があります。LM7480 には、LM74800 と LM74801 の 2 つのバリエーションがあります。LM74800 は、リニア・レギュレーションおよびコンパレータ方式を使用した逆電流ブロックを採用しています。一方、LM74801 はコンパレータに基づく方式をサポートしています。共通ドレイン構成のパワー MOSFET の場合、もう 1 つの理想ダイオードを使用した OR 接続設計のために中間点を利用できます。LM7480 は 65V の最大電圧定格を持っています。本デバイスと外付け MOSFET を共通ソース・トポロジに構成することで、24V バッテリ・システムの 200V 非抑制負荷ダンプのような大きな過電圧過渡からも負荷を保護できます。

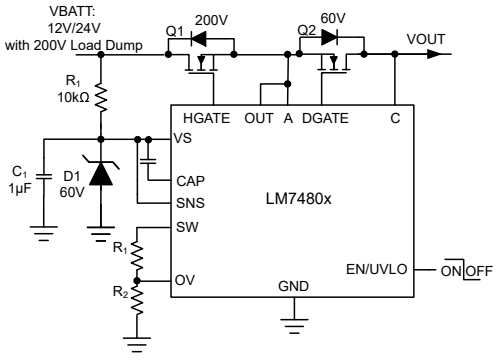
パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM74800	WSON (12)	3.00mm × 3.00mm
LM74801		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



スイッチ出力を備えた理想ダイオード



200V 負荷ダンプ保護機能を備えた理想ダイオード

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Device Comparison Table

	LM74800	LM74801
Reverse Current Blocking	$V_{(A-C)}$ linear regulation and comparator	$V_{(A-C)}$ comparator only

6 Pin Configuration and Functions

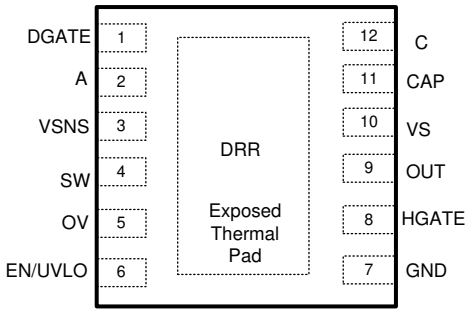


図 6-1. DRR Package, 12-Pin WSON (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	LM7480 DRR-12 (WSON)		
DGATE	1	O	Diode Controller Gate Drive Output. Connect to the GATE of the external MOSFET.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET.
VSNS	3	I	Voltage sensing input.
SW	4	I	Voltage sensing disconnect switch terminal. VSNS and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN/UVLO is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used then short them together and connect to VS pin.
OV	5	I	Adjustable overvoltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OVP exceeds the overvoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OVP falling threshold.
EN/UVLO	6	I	EN/UVLO Input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling it low below $V_{(ENF)}$ makes the device enter into low Iq shutdown mode. For UVLO, connect an external resistor ladder to EN/UVLO to GND.
GND	7	G	Connect to the system ground plane.
HGATE	8	O	GATE driver output for the HSFET. Connect to the GATE of the external FET.
OUT	9	I	Connect to the output rail (external MOSFET source).
VS	10	I	Input power supply to the IC. Connect VS to middle point of the common drain back to back MOSFET configuration. Connect a 100-nF capacitor across VS and GND pins.
CAP	11	O	Charge pump output. Connect a 100-nF capacitor across CAP and VS pins.
C	12	I	Cathode of the ideal diode. Connect to the drain of the external MOSFET.
RTN	Thermal Pad	—	Leave exposed pad floating. Do Not connect to GND plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	–65	70	V
	VS to GND	–1	70	
	VSNS, SW, EN/UVLO, C, OV, OUT to GND, $V_{(A)}$ > 0 V	–0.3	70	
	VSNS, SW, EN/UVLO, C, OV, OUT to GND, $V_{(A)}$ ≤ 0 V	$V_{(A)}$	(70 + $V_{(A)}$)	
	RTN to GND	–65	0.3	
	I_{VSNS}, I_{SW}	–1	10	mA
	$I_{EN/UVLO}$, I_{OV}, $V_{(A)}$ > 0 V	–1		mA
	$I_{EN/UVLO}$, I_{OV}, $V_{(A)}$ ≤ 0 V	Internally limited		
Output Pins	OUT to VS	–65	16.5	V
Output Pins	CAP to VS	–0.3	15	V
	CAP to A	–0.3	85	
	DGATE to A	–0.3	15	
	HGATE to OUT	–0.3	15	
Output to Input Pins	C to A	–5	85	
Operating junction temperature, T_j (2)		–55	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JEDEC JS-001(1)		±2000	V
		Charged device model (CDM), V per JEDEC JS-002(2)	Corner pins (DGATE, OV, and C)	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
	VS to GND	0		65	V
	EN/UVLO to GND	0		65	V
External Capacitance	CAP to A, VS to GND, A to GND	0.1			µF
External MOSFET max VGS rating	DGATE to A and HGATE to OUT	15			V
Tj	Operating Junction temperature(2)	–55		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		LM7480x DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –55°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = $V_{(VSNS)}$ = 12 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3		65	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.4	2.6	2.85	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		1.9	2.1	2.3	V
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V		2.87	5	µA
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		397		µA
		$V_{(A)}$ = $V_{(VS)}$ = 24 V, $V_{(EN/UVLO)}$ = 2 V		413	530	µA
$I_{(REV)}$	$I_{(A)}$ leakage current during Reverse Polarity,	0 V ≤ $V_{(A)}$ ≤ – 65 V		10	112	µA
	$I_{(OUT)}$ leakage current during Reverse Polarity				1	µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	EN/UVLO threshold voltage, rising		1.195	1.231	1.267	V
$V_{(UVLOF)}$	EN/UVLO threshold voltage, falling		1.091	1.132	1.159	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3	0.67	0.93	V
$V_{(EN\_Hys)}$	Enable Hysteresis		37	72	95	mV
$I_{(EN/UVLO)}$		0 V ≤ $V_{(EN/UVLO)}$ ≤ 65 V		55	200	nA
OVERVOLTAGE PROTECTION AND BATTERY SENSING (VSNS, SW, OV) INPUT						
$R_{(SW)}$	Battery sensing disconnect switch resistance	3 V ≤ $V_{(SNS)}$ ≤ 65 V	10	19.5	46	Ω
$V_{(OVR)}$	Overvoltage threshold input, rising		1.195	1.231	1.267	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.091	1.13	1.159	V
$I_{(OV)}$	OV Input leakage current	0 V ≤ $V_{(OV)}$ ≤ 65 V		53	200	nA
CHARGE PUMP (CAP)						
$I_{(CAP)}$	Charge Pump source current (Charge pump on)	$V_{(CAP)}$ – $V_{(A)}$ = 7 V, 6 V ≤ $V_{(S)}$ ≤ 65 V	1.3	2.7		mA
VCAP – VS	Charge Pump Turn ON voltage		11	12.2	13.2	V
	Charge Pump Turnoff voltage		11.9	13.2	14.1	V

7.5 Electrical Characteristics (continued)

T_J = –55°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = $V_{(VSNS)}$ = 12 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CAP\ UVLO)}$	Charge Pump UVLO voltage threshold, rising		5.4	6.6	7.9	V
	Charge Pump UVLO voltage threshold, falling		4.4	5.5	6.6	V
IDEAL DIODE (A, C, DGATE)						
$V_{(A\_PORR)}$	$V_{(A)}$ POR threshold, rising		2.2	2.35	2.6	V
$V_{(A\_PORF)}$	$V_{(A)}$ POR threshold, falling		2	2.2	2.4	V
$V_{(AC\_REG)}$	Regulated Forward $V_{(A)}$–$V_{(C)}$ Threshold	For LM74800 Only	6.8	10	13.4	mV
$V_{(AC\_REV)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Fast Reverse Current Blocking		–6.5	–5.5	–1.3	mV
$V_{(AC\_FWD)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Reverse to Forward transition		150	177	220	mV
$V_{(DGATE)} – V_{(A)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.5	13	V
$I_{(DGATE)}$	Peak Gate Source current	$V_{(A)} – V_{(C)}$ = 100 mV, $V_{(DGATE)} – V_{(A)}$ = 1 V		20		mA
	Peak Gate Sink current	$V_{(A)} – V_{(C)}$ = –12 mV, $V_{(DGATE)} – V_{(A)}$ = 11 V		2670		mA
	Regulation sink current	$V_{(A)} – V_{(C)}$ = 0 V, $V_{(DGATE)} – V_{(A)}$ = 11 V, LM74800 Only	7.2	12.3		µA
$I_{(C)}$	Cathode leakage Current	$V_{(A)}$ = –14 V, $V_{(C)}$ = 12 V, LM74801	0.1	2.84	15	µA
		$V_{(A)}$ = –14 V, $V_{(C)}$ = 12 V, LM74800	4	8.77	32	µA
HIGH SIDE CONTROLLER (HGATE, OUT, SNS, SW, OV)						
$V_{(HGATE)} – V_{(OUT)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.1	14.5	V
$I_{(HGATE)}$	Source Current		39	55	75	µA
	Sink Current	$V_{(OV)}$ > $V_{(OVR)}$	168	260		mA

7.6 Switching Characteristics

T_J = –55°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGATE\_OFF(dly)}$	DGATE Turnoff Delay during reverse voltage detection	$V_{(A)} – V_{(C)}$ = +30 mV to –100 mV to $V_{(DGATE–A)}$ < 1 V, $C_{(DGATE–A)}$ = 10 nF		0.5	0.875	µs
$t_{DGATE\_ON(dly)}$	DGATE Turnon Delay during forward voltage detection	$V_{(A)} – V_{(C)}$ = –20 mV to +700 mV to $V_{(DGATE-A)}$ > 5 V, $C_{(DGATE-A)}$ = 10 nF		2.8	3.8	µs
$t_{EN(dly)\_DGATE}$	DGATE Turnon Delay during EN/UVLO	EN/UVLO ↑ to $V_{(DGATE-A)}$ > 5V, $C_{(DGATE-A)}$ = 10 nF	98	175	270	µs
$t_{EN\_OFF(deg)\_DGATE}$	DGATE Turnoff Deglitch during EN/UVLO	EN/UVLO ↓ to DGATE ↓		8.1		µs
$t_{EN\_OFF(deg)\_HGATE}$	HGATE Turnoff Deglitch during EN/UVLO	EN/UVLO ↓ to HGATE ↓	3	4.6	6	µs
$t_{OVP\_OFF(deg)\_HGATE}$	HGATE Turnoff Deglitch during OV	OV ↑ to HGATE ↓, For LM74800 only		3.98	5.4	µs
		OV ↑ to HGATE ↓, For LM74801 only		3.2	4.7	µs

7.6 Switching Characteristics (continued)

T_J = –55°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OVP\_ON(deg)\_HGATE}$	HGATE Turnon Deglitch during OV	OV ↓ to HGATE ↑		2.95		µs

7.7 Typical Characteristics

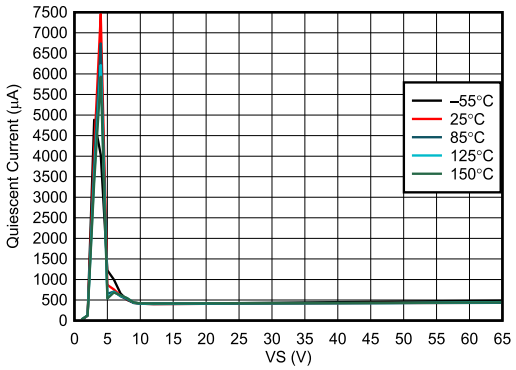


図 7-1. Operating Quiescent Current vs Supply Voltage

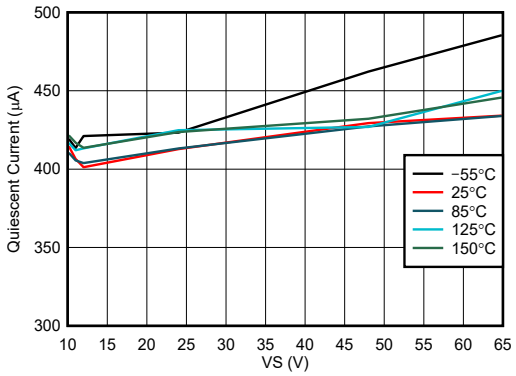


図 7-2. Operating Quiescent Current vs Supply Voltage (> 10 V)

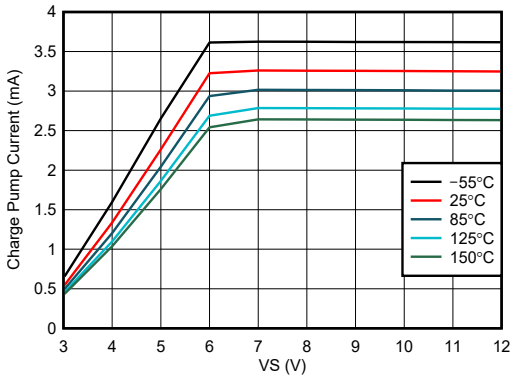


図 7-3. Charge Pump Current vs Supply Voltage at CAP = 6 V

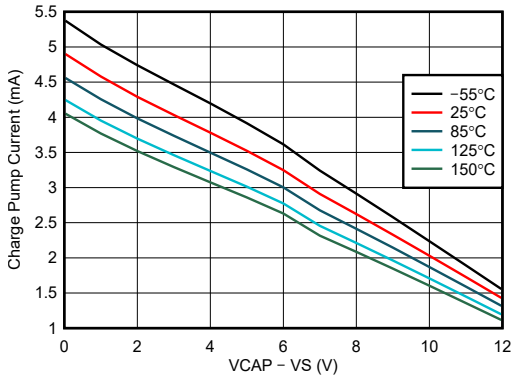


図 7-4. Charge Pump V-I Characteristics at VS ≥ 12 V

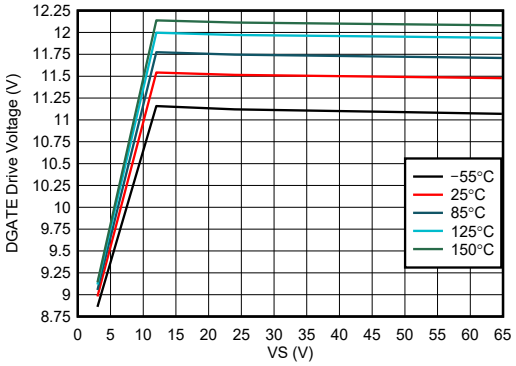


図 7-5. DGATE Drive Voltage vs Supply Voltage

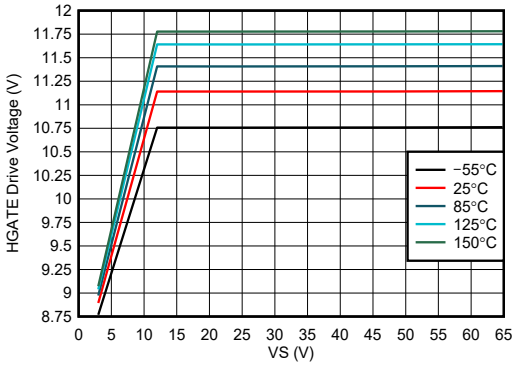


図 7-6. HGATE Drive Voltage vs Supply Voltage

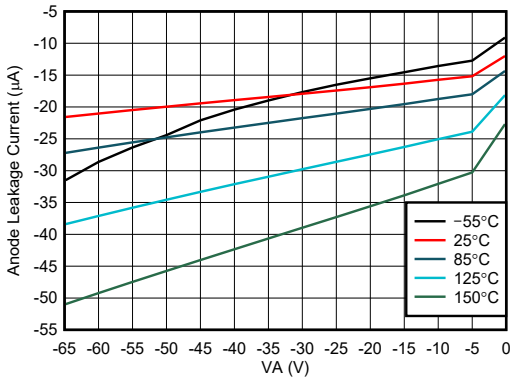


図 7-7. ANODE Leakage Current vs Reverse ANODE Voltage

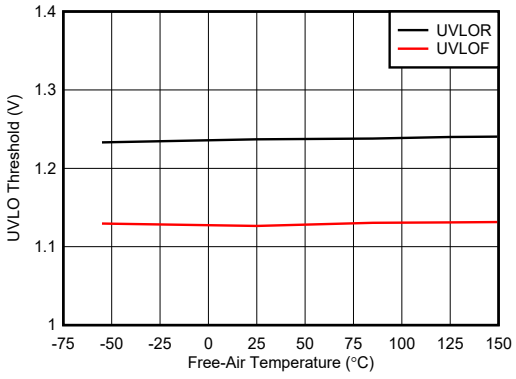


図 7-8. UVLO Thresholds vs Temperature

7.7 Typical Characteristics (continued)

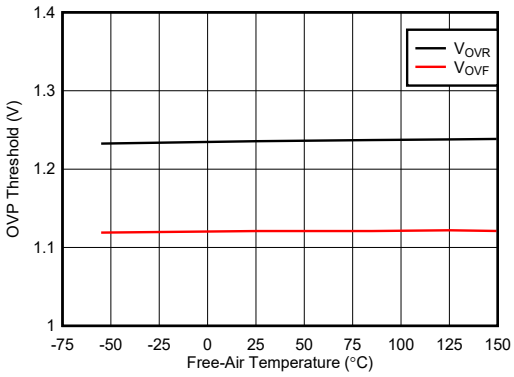


図 7-9. OVP Thresholds vs Temperature

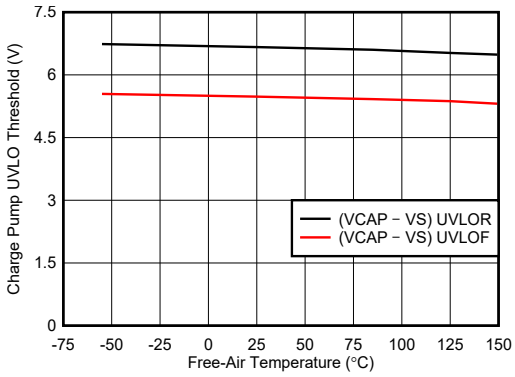


図 7-10. Charge Pump UVLO Threshold vs Temperature

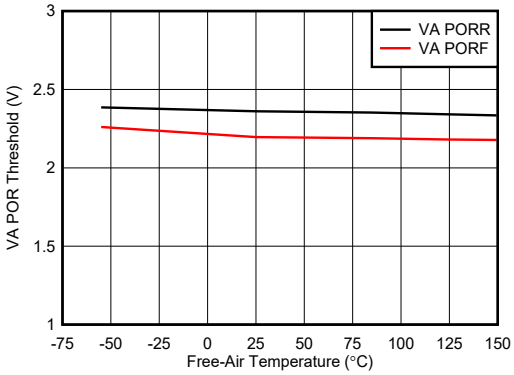


図 7-11. VA POR Threshold vs Temperature

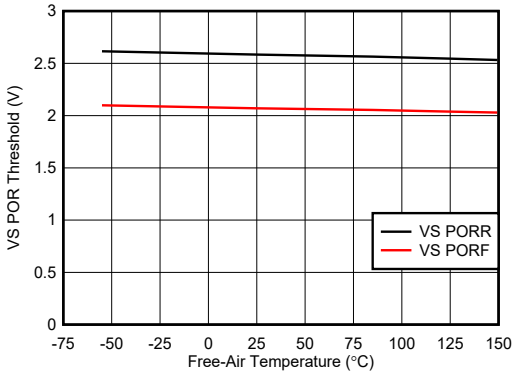


図 7-12. VS POR Threshold vs Temperature

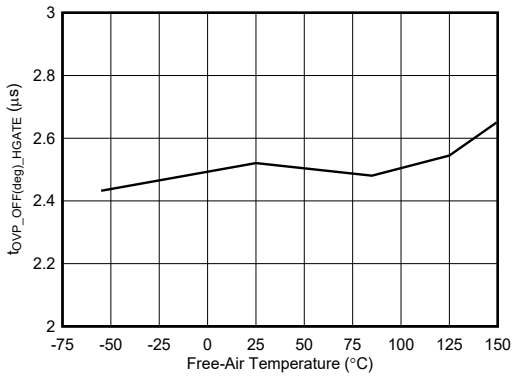


図 7-13. HGATE Turn OFF Delay During OV

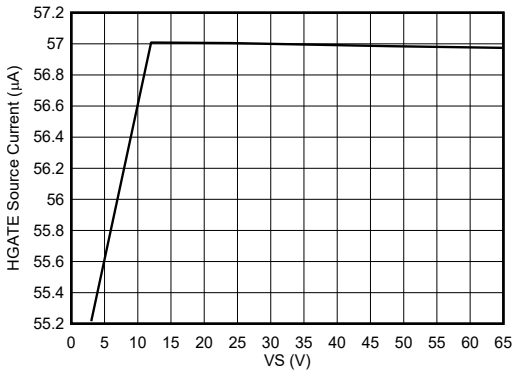


図 7-14. HGATE Current (IHGATE) vs Supply Voltage

8 Parameter Measurement Information

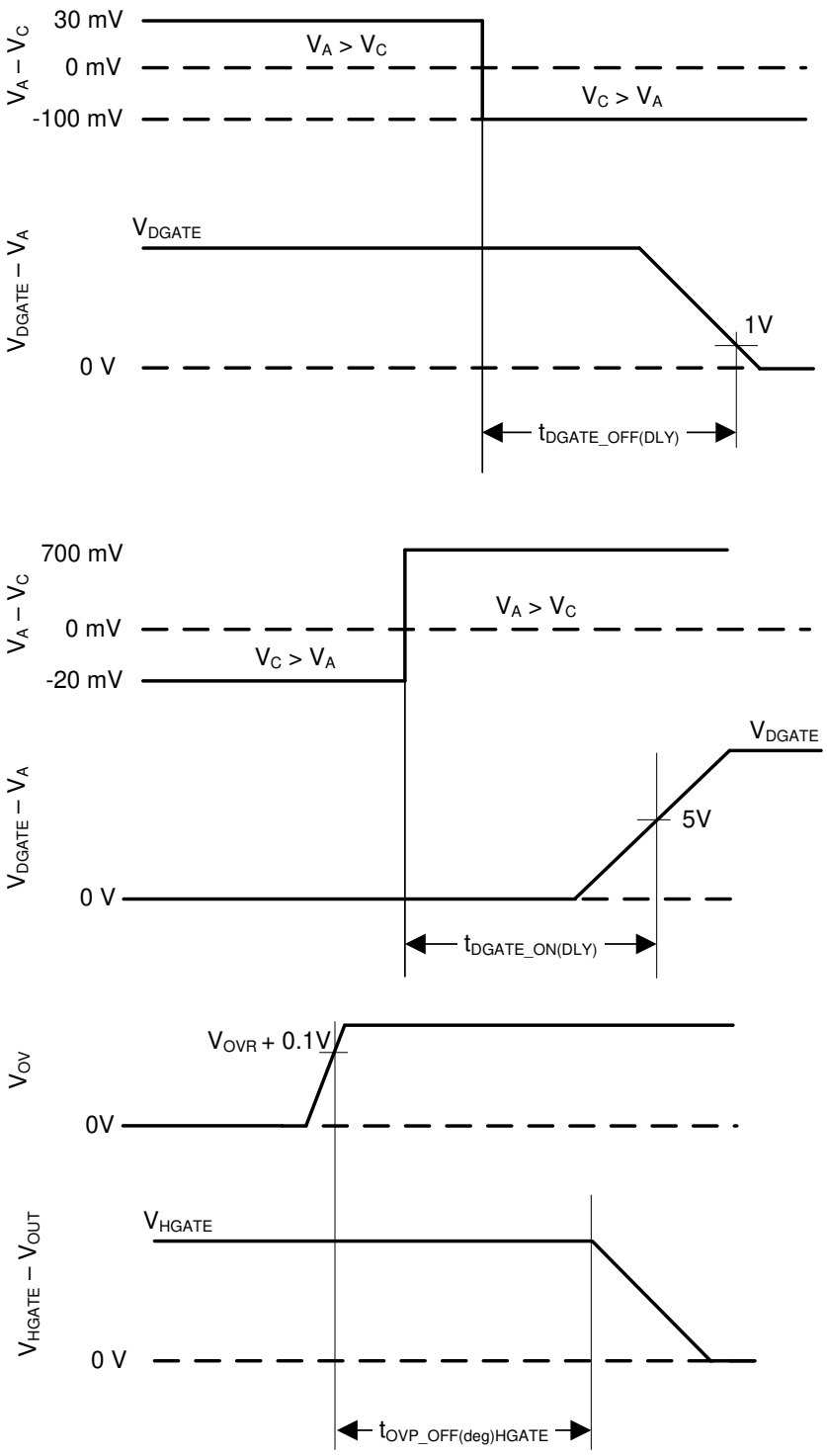


図 8-1. Timing Waveforms

9 Detailed Description

9.1 Overview

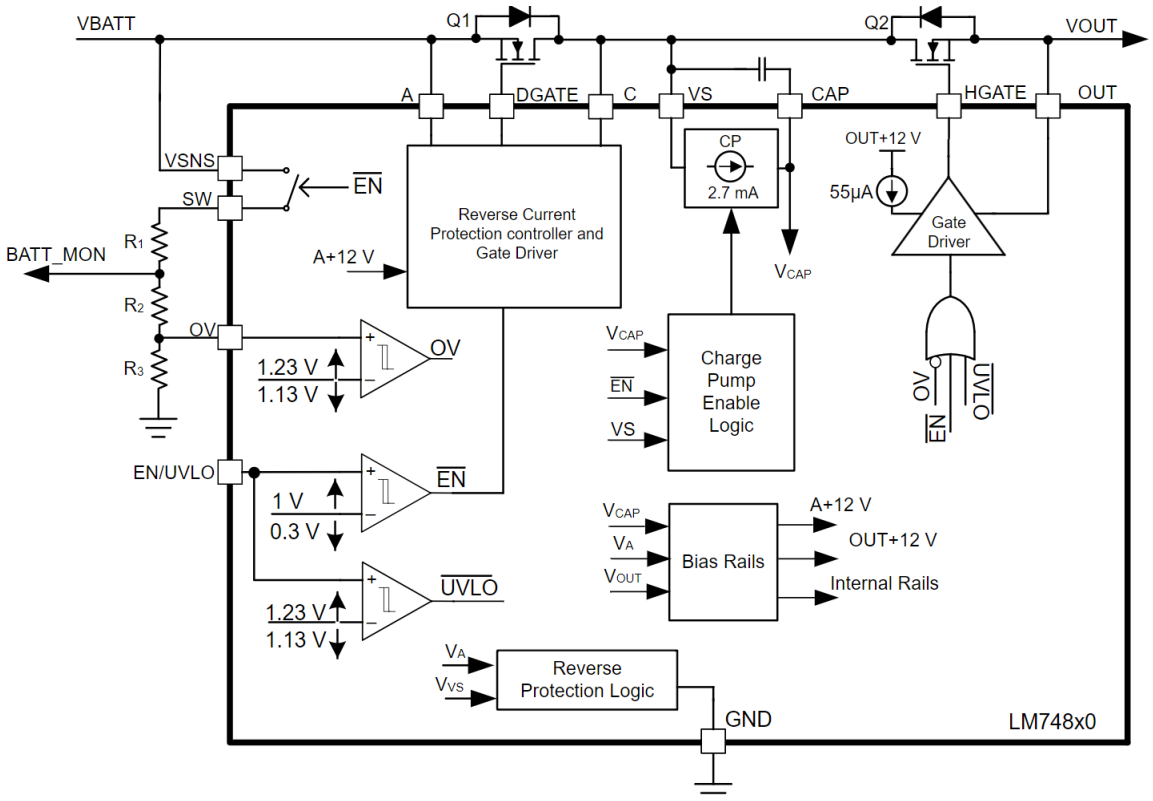
The LM7480 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control, inrush current limiting and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong charge pump with 20-mA peak GATE source current driver stage and short turn ON and turn OFF delay times ensures fast transient response ensuring robust performance during automotive testing such as ISO16750 or LV124 where an ECU is subjected to AC superimpose input signals. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and overvoltage protection using HGATE control. The device features an adjustable overvoltage cut-off protection feature using a programming resistor across SW and OVP terminal.

The LM7480 controller can drive the external MOSFETs in common drain and common source configurations. With common drain configuration of the power MOSFETs, the mid-point can be utilized for OR-ing designs using an another ideal diode. The LM7480 has a maximum voltage rating of 65 V. The loads can be protected from extended overvoltage transients like 200-V unsuppressed load dumps in 24-V battery systems by configuring the device with external MOSFETs in common source topology.

The LM74800 controls the DGATE of the MOSFET to regulate the forward voltage drop at 10.5 mV. The linear regulation scheme in these devices enables graceful control of the GATE voltage and turns off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. The LM74801 features a comparator based scheme to turn ON/OFF the MOSFET GATE.

The device features enable control. With the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low 2.87 µA of current. The high voltage rating of LM7480 helps to simplify the system designs for automotive ISO7637 protection. The LM74800 is also suitable for ORing applications.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the EN/UVLO pin voltage must be above the specified input high threshold, $V_{(ENR)}$. When enabled the charge pump sources a charging current of 2.7-mA typical. If EN/UVLO pin is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the CAP to VS voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use 式 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 175\mu s + C_{(CAP)} x \frac{V_{(CAP\_UVLOR)}}{2.7mA} \quad (1)$$

where

- $C_{(CAP)}$ is the charge pump capacitance connected across VS and CAP pins
- $V_{(CAP\_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive approximately 1 V of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the CAP to VS voltage reaches 13.2 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the CAP to VS voltage is below to 12.2 V typically at which point the charge pump is enabled. The voltage between CAP and VS continue to charge and discharge between 12.2 V and 13.2 V as shown in 図 9-1. By enabling and disabling the charge pump, the operating quiescent current of the LM7480 is reduced. When the charge pump is disabled it sinks 15 µA.

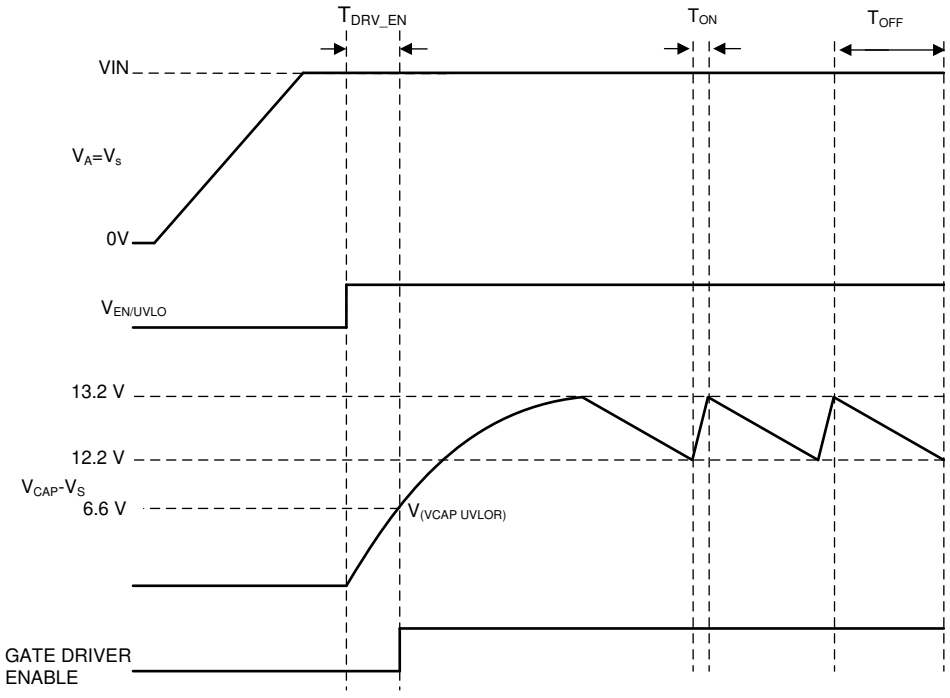


図 9-1. Charge Pump Operation

9.3.2 Dual Gate Control (DGATE, HGATE)

The LM7480x feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs.

9.3.2.1 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises of Ideal Diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to DGATE. The LM7480x has integrated reverse input protection down to –65 V.

Before the DGATE driver is enabled, following conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at A pin must be greater than VA POR Rising threshold.
- Voltage at Vs pin must be greater than Vs POR Rising thershold.

If the above conditions are not achieved, then the DGATE pin is internally connected to the A pin, assuring that the external MOSFET is disabled.

In LM74800 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 10.5 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74800 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches V(AC_REV) threshold then the DGATE goes low within 0.5-µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits V(AC_FWD) threshold within 2.8 µs (typ).

In LM74801, reverse current blocking is by fast reverse voltage comparator only. When the voltage drop across A and C reaches V(AC_REV) threshold then the DGATE goes low within 0.5 µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input LM7480 micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits V(AC_FWD) threshold within 2.8 µs (typ).

For Ideal Diode only designs, connect LM7480x as shown in 図 9-2.

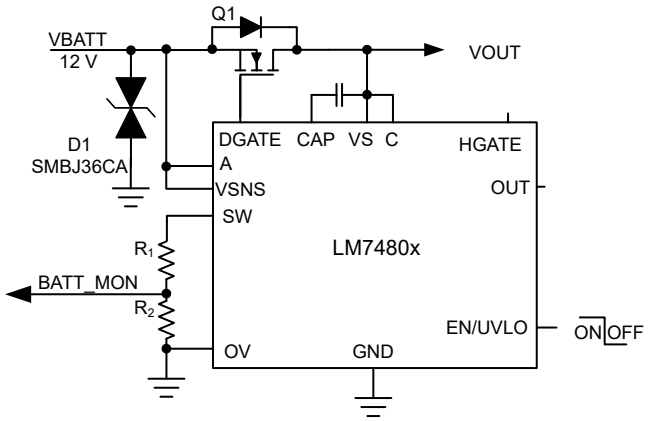


図 9-2. Configuring LM7480x-Q1 for Ideal Diode Only

9.3.2.2 Load Disconnect Switch Control (HGATE, OUT)

HGATE and OUT comprises of Load disconnect switch control stage. Connect the Source of the external MOSFET to OUT and Gate to HGATE.

Before the HGATE driver is enabled, following conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.

- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at Vs pin must be greater than Vs POR Rising thershold.

If the above conditions are not achieved, then the HGATE pin is internally connected to the OUT pin, assuring that the external MOSFET is disabled.

For Inrush Current limiting, connect C_{dVdT} capacitor and R_1 as shown in 図 9-3.

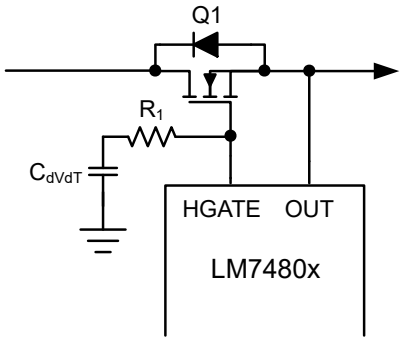


図 9-3. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use 式 2 to calculate C_{dVdT} capacitance value.

$$C_{dVdT} = \frac{I_{HGATE\_DRV}}{I_{INRUSH}} xC_{OUT} \quad (2)$$

where I_{HATE_DRV} is 55 µA (typ), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn off time.

9.3.3 Overvoltage Protection and Battery Voltage Sensing (VSNS, SW, OV)

Connect a resistor ladder as shown in 図 9-4 for overvoltage threshold programming.

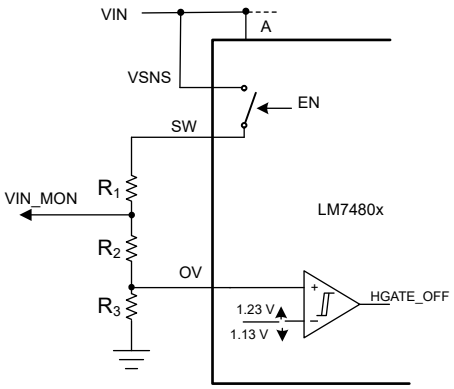


図 9-4. Programming Overvoltage Threshold and Battery Sensing

A disconnect switch is integrated between VSNS and SW pins. This switch is turned OFF when EN/UVLO pin is pulled low. This helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

LM7480-Q1 OV pin can also be used as a control input to turn off HGATE drive to achieve load disconnect functionality. When OV pin is driven high ($V_{OV} > V_{OVR}$), device pulls down HGATE to OUT thus turning off the load disconnect MOSFET. When OV pin is pulled low ($V_{OV} < V_{OVF}$) HGATE drive is again enabled to trun on the

load disconnect MOSFET. When OV pin is used as a control input to turn on/off load disconnect MOSFET, ensure device EN/UVLO pin is high ($V_{EN/UVLO}$ > V_{ENR}) and SW/VSNS pin voltage is higher than OV pin voltage.

9.3.4 Low Iq Shutdown and Under Voltage Lockout (EN/UVLO)

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in Charge Pump section. If EN/UVLO pin voltage is less than the input low threshold, $V_{(ENF)}$, the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM7480 in shutdown mode. If $V_{(ENF)}$ < $V_{(EN/UVLO)}$ < $V_{(UVLOF)}$ then only HGATE is disabled disconnecting the load from the supply, DGATE remains ON. The EN/UVLO pin can withstand a maximum voltage of 65 V. For always ON operation connect EN/UVLO pin to VS.

9.4 Device Functional Modes

Shutdown Mode

The LM7480 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold $V_{(ENF)}$. Both the gate drivers and the charge pump are disabled in shutdown mode. During shutdown mode the LM7480 enters low IQ operation with a total input quiescent consumption of 2.87 µA (typ). When the LM7480 is in shutdown mode, forward current flow to always ON loads connected to the common drain point of the back to back MOSFETs is not interrupted but is conducted through the MOSFET's body diode.

9.5 Application Examples

9.5.1 Redundant Supply OR-ing with Inrush Current Limiting, Overvoltage Protection and ON/OFF Control

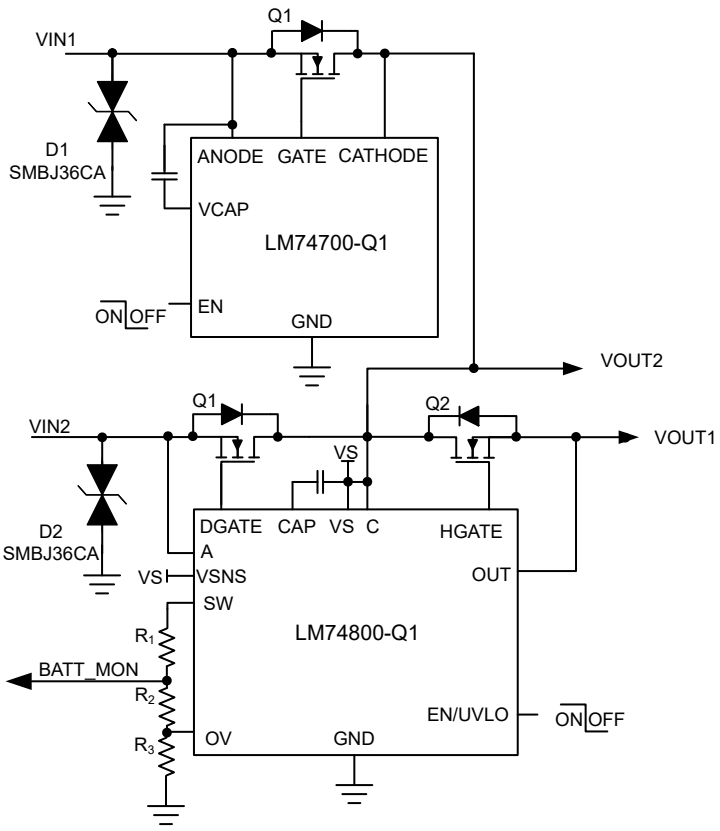


図 9-5. Redundant Supply OR-ing with Overvoltage Protection and ON/OFF Control

図 9-5 shows the implementation of Dual OR-ing with Inrush Current Limiting, overvoltage Protection and power path ON/OFF control. The input side SMBJ36CA TVS across the ideal diodes is required for ISO7637 Pulse 1 transient suppression to limit the input voltage within the device max voltage rating of –65V.

R1 and R2 are the programming resistors for over voltage protection (OVP) threshold. When the voltage at OV pin exceeds OV cut-off reference threshold then the HGATE driver turns OFF the FET Q3, disconnecting the power path and protecting the downstream load. HGATE goes high once the OVP pin voltage goes below the OVP falling hysteresis threshold. Use 0.1-µF to 1-µF capacitor across VS to CAP pins of the LM7480. This is the charge pump capacitor and acts as the supply for both the DGATE and HGATE driver stages. The DGATE driver of the LM7480 is equipped with 20-mA peak source current and 2.6-A peak sink current capability resulting in fast and efficient transient responses during the ISO16750 or LV124 short interruptions as well as AC superimpose testing.

Pull EN low during the sleep/standby mode. With EN low, both the DGATE and HGATE drivers are pulled low turning OFF both the power FETs. VOUT1 gets disconnected from the input supply rail reducing the system I_Q. VOUT2 is gets power through the body diode of the MOSFET Q2 and this supply can be utilized for always ON loads. The LM7480 draws a 2.87-µA (typ) current during this mode.

9.5.2 Ideal Diode With Unsuppressed Load Dump Protection

An extended overvoltage protection support above 65 V can be achieved by configuring the device with external back to back MOSFETs in common source topology as shown in 図 9-6. Place a resistor R1 and a zener clamp across VS pin to GND to limit the voltage below 65 V. The load gets protected from overvoltages transients like unsuppressed load dumps with the help of overvoltage protection feature. Use R2 and R3 for setting the overvoltage protection threshold. When voltage at OV pin exceeds the set OV threshold then the HGATE turns OFF. This results in power path disconnection between input and output.

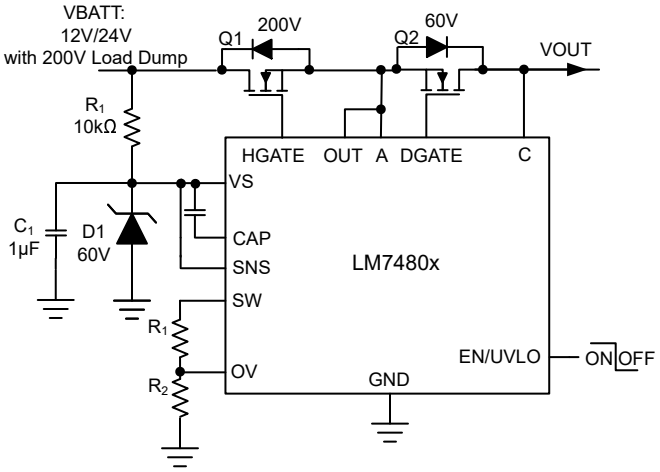


図 9-6. Ideal Diode With 200-V Unsupressed Load Dump Protection

10 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

LM7480 controls two N-channel power MOSFETs with DGATE used to control diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during an overvoltage protection. HGATE controlled MOSFET can be used to clamp the output during overvoltage or load dump conditions. LM7480 can be placed into low quiescent current mode using EN/UVLO, where both DGATE and HGATE are turned OFF.

The device has a separate supply input pin (Vs). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM7480 device offers flexibility in system design architectures and enables circuit design with various power path control topologies like common drain, common source, ORing and Power MUXing. With these various topologies, the system designers can design the front-end power system to meet various system design requirements. For more information, see the *Six System Architectures With Robust Reverse Battery Protection Using an Ideal Diode Controller* Application Report.

10.2 Typical 12-V Reverse Battery Protection Application

A typical application circuit of LM74800 configured in **common-drain topology** to provide reverse battery protection with overvoltage protection is shown in 図 10-1.

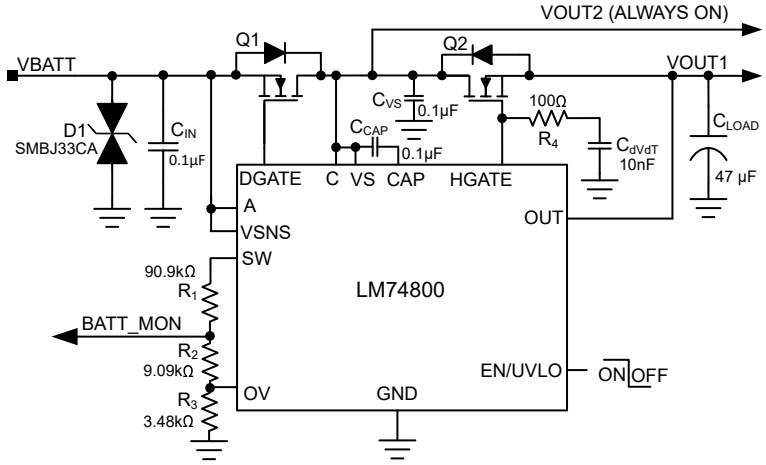


図 10-1. Typical Application Circuit: 12-V Reverse Battery Protection and Overvoltage Protection

10.2.1 Design Requirements for 12-V Battery Protection

The system design requirements are listed in 表 10-1.

表 10-1. Design Parameters for 12-V Reverse Battery Protection and Overvoltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output Power	50 W
Output Current Range	4-A nominal, 5-A maximum
Input Capacitance	0.1-µF minimum
Output Capacitance	0.1-µF minimum (optional hold-up capacitor of 47 µF)
Overvoltage Cut-off	37 V, output cut-off > 37 V
Battery Monitor Ratio	8:1

10.2.2 Automotive Reverse Battery Protection

The LM7480 feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs. This enables LM7480 to provide comprehensive immunity with robust system protection during various automotive transient tests as per ISO 7637-2 and ISO 16750-2 standard as well as other automotive OEM standards. For more information, see the *Automotive EMC-compliant reverse-battery protection with ideal-diode controllers* article.

LM7480 gate drive output DGATE controls MOSFET Q1 to provide reverse battery protection and true reverse current blocking functionality. HGATE controls MOSFET Q2 to turn off the power path during input overvoltage condition. Resistor network R1, R2 and R3 connected to OV and SW can be configured for overvoltage protection and also for battery monitoring under normal operating conditions as well as reverse battery conditions. Bi-directional TVS D1 clamps the automotive transient input voltages on the 12-V battery, both positive and negative transients, to voltage levels safe for MOSFET Q1 and LM7480.

Fast reverse current blocking response and quick reverse recovery enables LM7480 to turn ON/OFF MOSFET Q1 during AC super imposed input and provide active rectification of the AC input superimposed on DC battery voltage. Fast reverse current blocking response of LM7480 helps to turn off MOSFET Q1 during negative transients inputs and input micro short interruption conditions where input can fall to 0-V for short duration.

10.2.3 Detailed Design Procedure

10.2.3.1 Design Considerations

表 10-1 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with overvoltage cut-off. During power up, inrush current through MOSFET Q2 needs to be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2 and maximum operating voltage determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q2 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple and ISO 7637-2 pulse 1 requirements. overvoltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2 and LM7480.

10.2.3.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capactiance of Q2 $C_{ISS(MOSFET)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET\_Q1)}$ + $C_{ISS(MOSFET\_Q2)}$) (µF)

10.2.3.3 Input and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

10.2.3.4 Hold-Up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM7480 is based on the UVLO settings of downstream DC-DC converters. For this design, 2.5-V drop in output voltage for 100 µs is considered and the minimum hold-up capacitance required is calculated by

$$C_{HOLD\_UP\_MIN} = \frac{I_{LOAD\_MAX}}{dV_{OUT}} x100\mu s \tag{3}$$

Minimum hold-up capacitance required for 2.5-V drop in 100 µs is 200 µF. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

10.2.3.5 Overvoltage Protection and Battery Monitor

Resistors R_1, R_2 and R_3 connected in series are used to program the overvoltage threshold and battery monitor ratio. The resistor values required for setting the overvoltage threshold V_{OV} to 37.0 V and battery monitor ratio V_{BATT_MON} : V_{BATT} to 1:8 are calculated by solving Equation 3 and Equation 4.

$$V_{OVR} = \frac{R_3}{R_1 + R_2 + R_3} xV_{OV} \tag{4}$$

$$V_{BAT\_MON} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} xV_{BATT} \tag{5}$$

For minimizing the input current drawn from the battery through resistors R_1, R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current

through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_1 + R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{OVR} is 1.23 V and battery monitor ratio (V_{BATT_MON} / V_{BATT}) is designed for a ratio of 1/8. To limit (R_1 + R_2 + R_3) < 120 kΩ, select (R_1 + R_2) = 100 kΩ. Solving Equation 3 gives R_3 = 3.45 kΩ. Solving Equation 4 for R2 using (R_1 + R_2) = 100 kΩ and R_3 = 3.45 kΩ, gives R_2 = 9.48 kΩ and R_1 = 90.52 kΩ.

Standard 1% resistor values closest to the calculated resistor values are R1 = 90.9 kΩ, R2 = 9.09 kΩ and R3 = 3.48 kΩ.

10.2.4 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include all the automotive transient events and any anticipated fault conditions. It is recommended to use MOSFETs with V_{DS} voltage rating of 60 V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back-back at the input.

The maximum V_{GS} LM7480 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level, but this would result in increased I_Q current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM7480's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point.

For active rectification of AC super imposed ripple on the battery supply voltage, gate-source charge Q_{GS} of Q1 must be selected to meet the required AC ripple frequency. Maximum gate-source charge Q_{GS} (at 4.5-V V_{GS}) for active rectification every cycle is

$$Q_{GS\_MAX} = \frac{1.3mA}{F_{AC\_RIPPLE}} \quad (6)$$

Where 1.3 mA is minimum charge pump current at 7-V V_{DGATE}-V_A, F_{AC_RIPPLE} is frequency of the AC ripple superimposed on the battery and Q_{GS_MAX} is the Q_{GS} value specified in manufacturer datasheet at 6-V V_{GS}. For active rectification at F_{AC_RIPPLE} = 30 KHz, Q_{GS_MAX} = 43 nC.

Based on the design requirements, BUK7Y4R8-60E MOSFET is selected and its ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 5.0-mΩ typical at 5-V V_{GS} and 2.9-mΩ rated at 10-V V_{GS}
- MOSFET Q_{GS} 17.4 nC

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

10.2.5 MOSFET Selection: Hot-Swap MOSFET Q2

The V_{DS} rating of the MOSFET Q2 should be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12-V design, transient overvoltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2 A 50 V for 50 µs. Further, ISO 7637-2 Pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors and the maximum voltage on the 12-V battery can be limited to < 40 V the minimum recommended input capacitance of 0.1 µF. The 50-V

SO 7637-2 Pulse 2 A can also be absorbed by input and output capacitors and its amplitude could be reduced to 40-V peak by placing sufficient amount of capacitance at input and output. However for this 12-V design, maximum system voltage is 50 V and a 60-V V_{DS} rated MOSFET is selected.

The VGS rating of the MOSFET Q2 should be higher than that maximum HGATE-OUT voltage 15 V.

Inrush current through the MOSFET during input hot-plug into the 12-V battery is determined by output capacitance. External capacitor on HGATE, C_{DVDT} is used to limit the inrush current during input hot-plug or startup. The value of inrush current determined by 式 2 need to be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA). To limit inrush current to 250 mA, value of C_{DVDT} is 10.43 nF, closest standard value of 10.0 nF is chosen.

Duration of inrush current is calculated by

$$dT_{INRUSH} = \frac{12}{I_{INRUSH}} xC_{OUT} \tag{7}$$

Calculated inrush current duration is 2.36 ms with 250-mA inrush current.

MOSFET BUK7Y4R8-60E having 60-V V_{DS} and ±20-V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET's safe operating area (SOA).

10.2.6 TVS Selection

A 600-W SMBJ TVS such as SMBJ33CA is recommended for input transient clamping and protection. For detailed explanation on TVS selection for 12-V battery systems, refer to *TVS Selection for 12-V Battery Systems*.

10.2.7 Application Curves

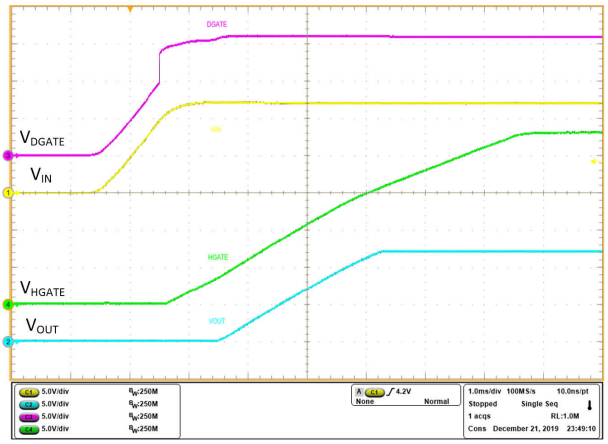


図 10-2. Startup 12 V with EN Pulled to VIN

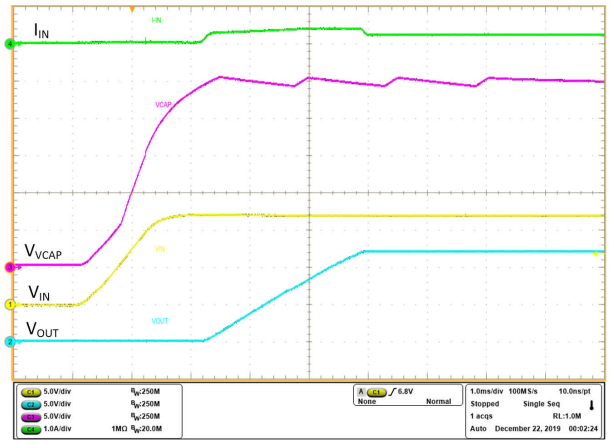


図 10-3. Startup 12 V showing Charge Pump VCAP

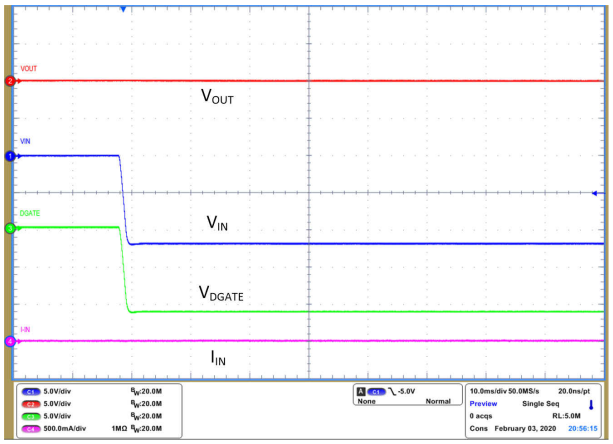


図 10-4. Reverse Input Voltage –14 V

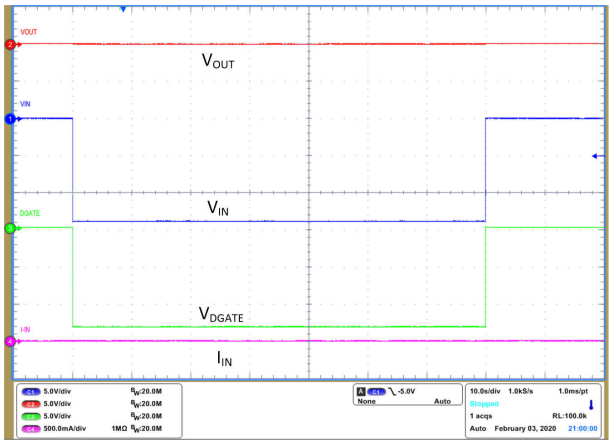


図 10-5. Reverse Input Voltage –14 V for 60 s

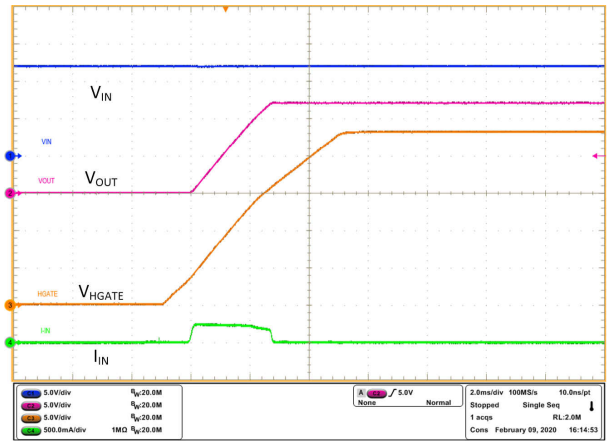


図 10-6. Inrush Current with no Load at Output

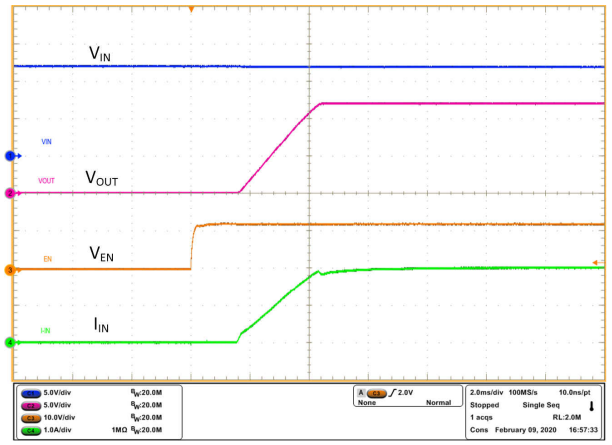


図 10-7. Inrush Current with 60-Ω Load

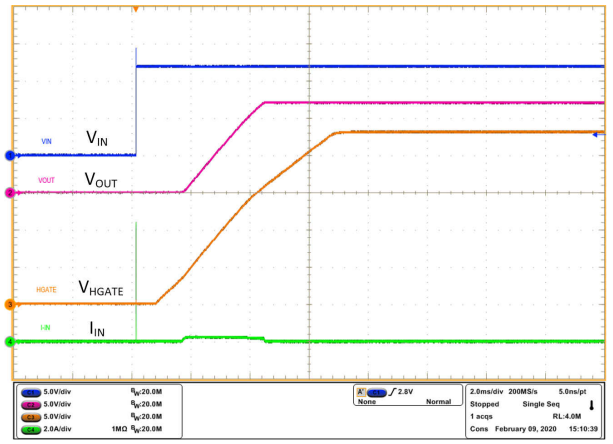


図 10-8. Hot-Plug into 12 V

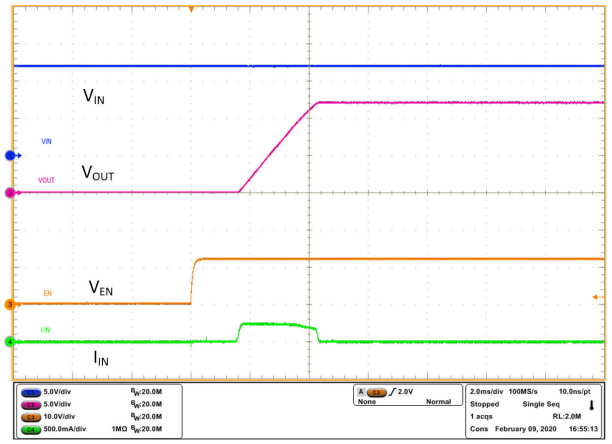


図 10-9. Output Turn ON with Enable

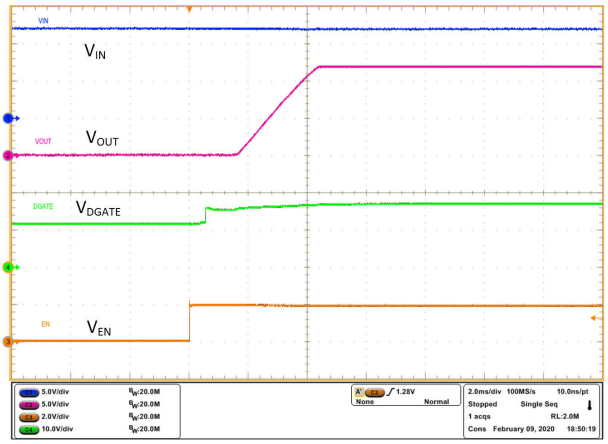


図 10-10. DGATE Turn ON with Enable

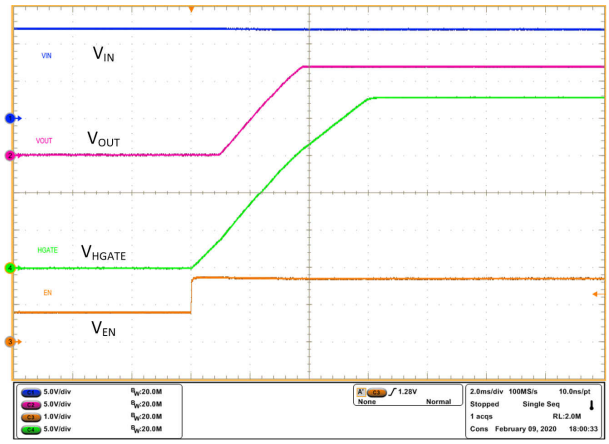


図 10-11. Turn ON with VCAP ON - EN rising from 0.8 V

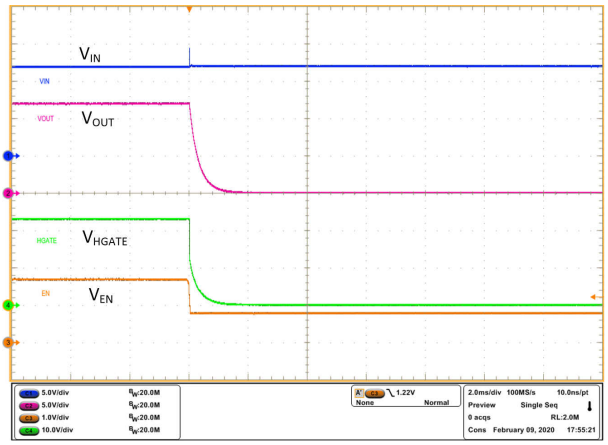


図 10-12. Turn OFF with Enable Control

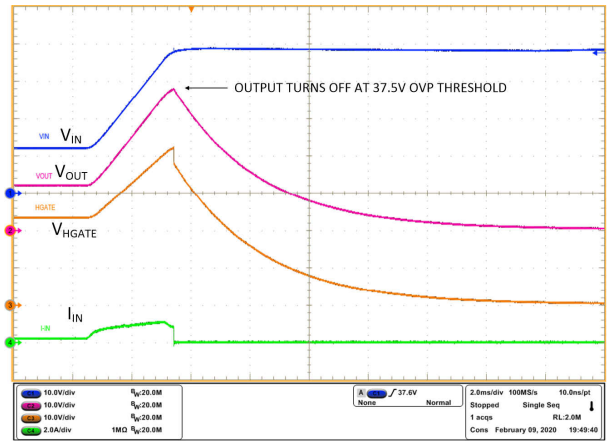


図 10-13. Overvoltage Protection

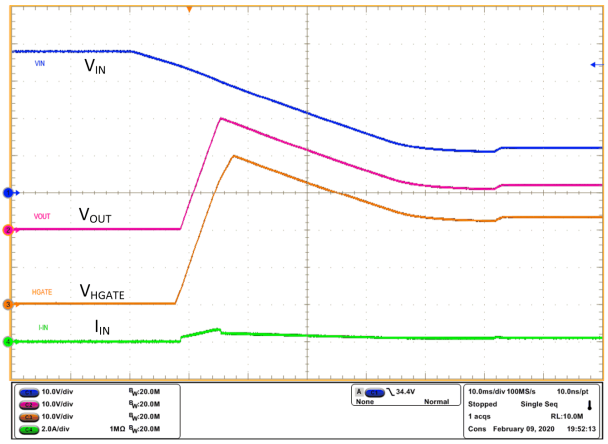


図 10-14. Overvoltage Recovery

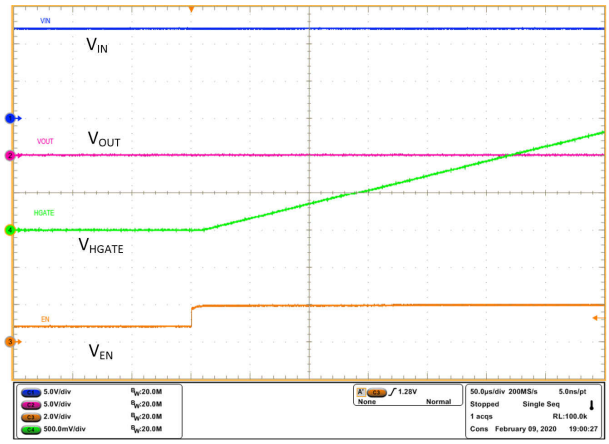


図 10-15. Turn ON delay - HGATE

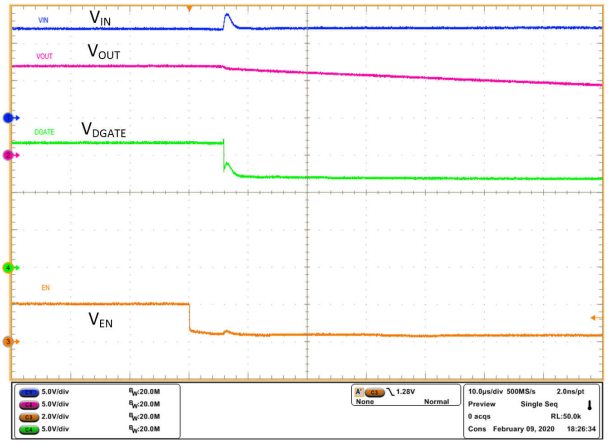


図 10-16. Turn OFF Delay - DGATE

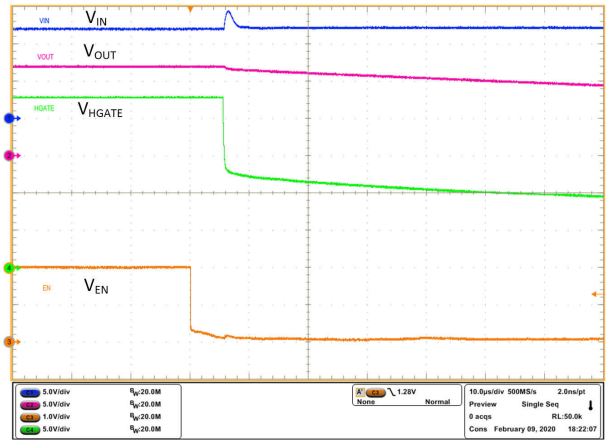


図 10-17. Turn OFF Delay - HGATE

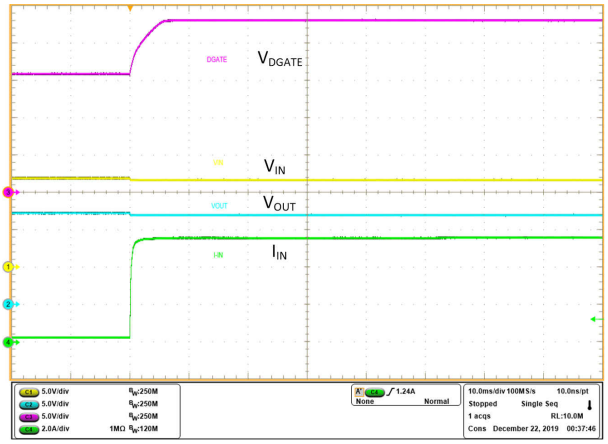


図 10-18. Load Transient 100 mA to 5 A

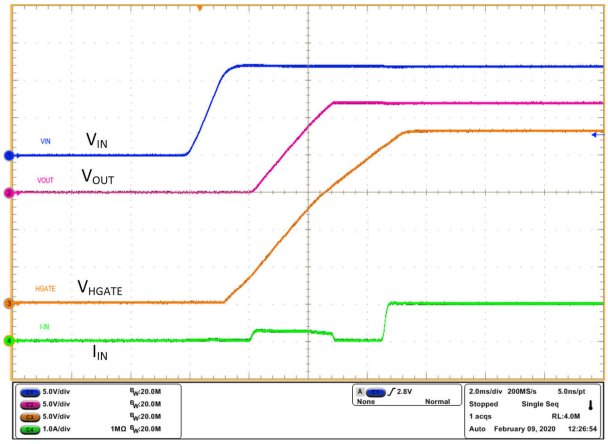


図 10-19. Startup 1-A Load 1 ms After Output Powers Up

10.3 200-V Unsuppressed Load Dump Protection Application

Independent gate drive topology of LM74800-Q1 enables to configure the LM74800-Q1 in to provide unsuppressed load dump or surge protection along with reverse battery protection. LM74800-Q1 configured in **common-source topology** to provide 200-V unsuppressed load dump protection with reverse battery protection is 図 10-20.

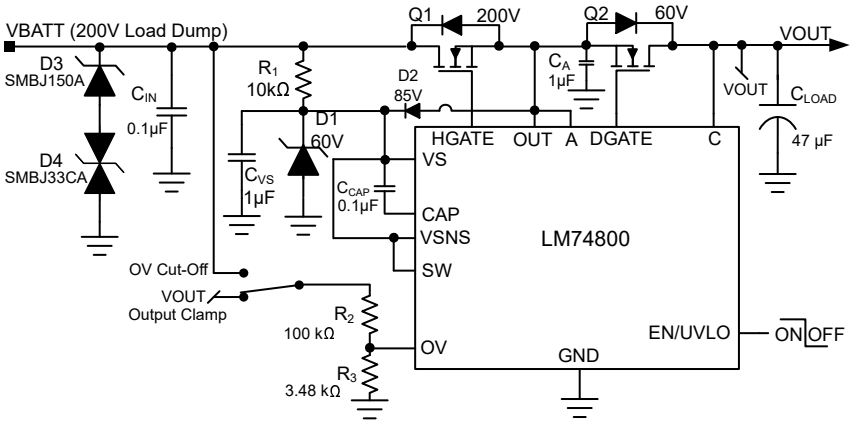


図 10-20. Typical Application Circuit: 200-V Unsuppressed Load Dump Protection With Reverse Battery Protection

10.3.1 Design Requirements for 200-V Unsuppressed Load Dump Protection

表 10-2. Design Parameters for 24-V Unsuppressed Load Dump Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	24-V battery, 6 V during cold crank 200-V unsuppressed load lump
Output Voltage	6 V during cold crank and 37 V during load dump
Output Power	25 W
Output Current Range	2-A nominal, 2.5-A peak
Input Capacitance	0.1-µF minimum
Output Capacitance	0.1-µF minimum, 220-µF typical hold-up capacitance
Overvoltage Cut-Off Threshold	37 V
Overvoltage Clamp	Output clamped between 34.5 V and 37.5 V
Automotive Transient Immunity Compliance	ISO 7637-2 and ISO 16750-2 including 200-V unsuppressed load dump Pulse 5 A and –600-V 50-Ω ISO-7637 Pulse 1

10.3.2 Design Procedure

Load dump transients occurs on loads connected to the alternator when a discharged battery is disconnected from alternator while it is still generating charging current. Load dump amplitude and duration depends on alternator speed and field current into the rotor. The pulse shape and parameter are specified in ISO 7637-2 5A where a 200-V pulse lasts maximum 350 ms on 24-V battery system. Circuit topology and MOSFET ratings are important when designing a 200-V unsuppressed load dump protection circuit using LM74800-Q1. Dual gate drive enables LM74800-Q1 to be configured in common source topology in 図 10-20 where MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and LM74800-Q1 from 200 V. Note that only the V_S pin is exposed to 200 V through a 10-kΩ resistor. A 60-V rated zener diode is used to clamp and protect the V_S pin. Rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level. MOSFET Q1 selection, input TVS selection and MOSFET Q2 selection for ISO 7637-2 and ISO 16750-2 compliance are discussed in this section.

10.3.2.1 Boost Converter Components (C2, C3, L1)

Place a minimum of 1-µF capacitor across drain of the FET to GND (C2) and across CAP pin of LM7472x-Q1 to drain of the FET (C3). Use a 100-µH inductor (L1) with saturation current rating > 175 mA (for example, XPL2010-104ML from coil craft).

10.3.2.2 Input and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

10.3.2.3 V_S Capacitance, Resistor, and Zener Clamp

Minimum of 1-µF C_{VS} capacitance is required. During 200-V load dump, resistor R_1 and Zener diode D_1 are used to protect VS pin from exceeding the maximum ratings by clamping V_{VS} to 60 V. Choosing R_1 = 10 kΩ, the peak power dissipated in Zener diode D1 = 60 V × (200 V – 60 V) / 10 kΩ = 0.840 W of peak power dissipation. SMA package diode such as BZG03B62-M can handle 840-mW peak power dissipation. Peak power dissipated in R1 = (200 V – 60 V)^2 / 10 kΩ = 1.96 W. One 10-kΩ resistor in 1210 package with 0.5-W DC power rating and 200-V rating can withstand 200-V load dump for 350 ms.

10.3.2.4 Overvoltage Protection and Output Clamp

Resistors R_2 and R_3 connected in series is used to program the overvoltage threshold. Connecting R2 to VBATT provides overvoltage cut-off and switching the connection to VOUT provides overvoltage clamp. The resistor values required for setting the overvoltage threshold V_{OV} to 37.0 V is calculated by solving Equation 7.

$$V_{OVR} = \frac{R_3}{R_2 + R_3} x V_{OV} \tag{8}$$

For minimizing the input current drawn from the battery through resistors R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{OVR} is 1.233V V. To limit (R_2 + R_3) < 120 kΩ, select (R_2) = 100 kΩ. Solving Equation 7 gives R_3 = 3.45 kΩ.

Closest standard 1% resistor values are R2 = 100 kΩ and R3 = 3.48 kΩ.

10.3.2.5 MOSFET Q1 Selection

The V_{DS} rating of the MOSFET Q1 should be minimum 200 V for a output cutoff design where output can reach 0 V while the load dump transient is present and should be a minimum of 164.5 V when output is clamped to 37 V (±1.5 V). The V_{GS} rating is based on HGATE-OUT maximum voltage of 15 V. A 20-V V_{GS} rated MOSFET is recommended.

Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET need to be considered with sufficient design margin for reliable operation.

10.3.2.6 Input TVS Selection

Two TVS diodes D3 and D4 are required at the input. The breakdown voltage of TVS in the positive side should be higher than the maximum system voltage 200 V. On the negative side clamping, diode D4 is used to clamp ISO 7637-2 pulse 1 and its selection is similar to procedure in *TVS selection for 24-V Battery Systems*. SMBJ150A for D3 and SMBJ33CA for D4 are recommended.

10.3.2.7 MOSFET Q2 Selection

Design requirements for selecting Q2 is similar to MOSFET Q1 selection in 表 10-1 and hence the procedure for selecting MOSFET Q2 is same as outlined in *MOSFET Selection: Blocking MOSFET Q1*. MOSFET BUK7Y4R8-60E is selected based on the design requirements.

10.3.3 Application Curves

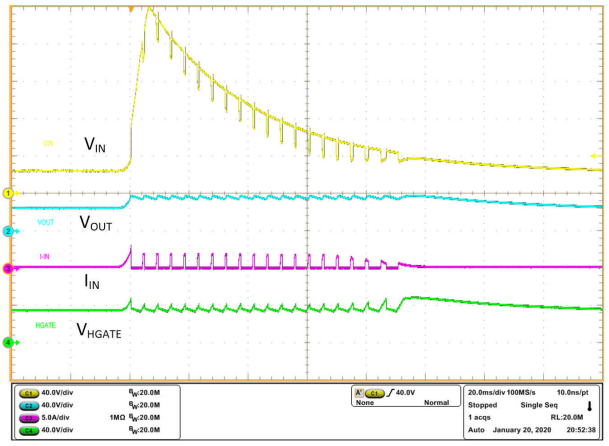


図 10-21. Unsuppressed Load Dump 200 V - Output Clamp

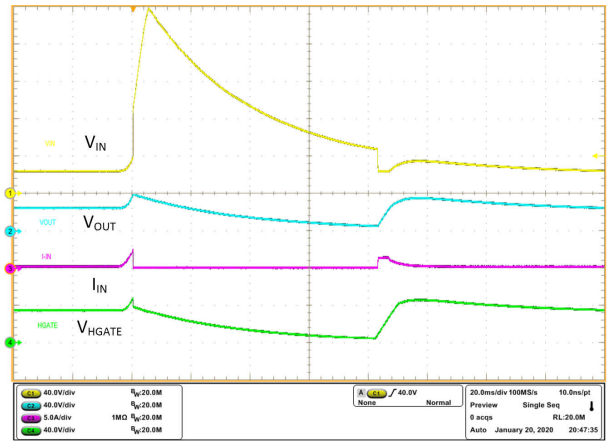


図 10-22. Unsuppressed Load Dump 200 V - Output Cut-off

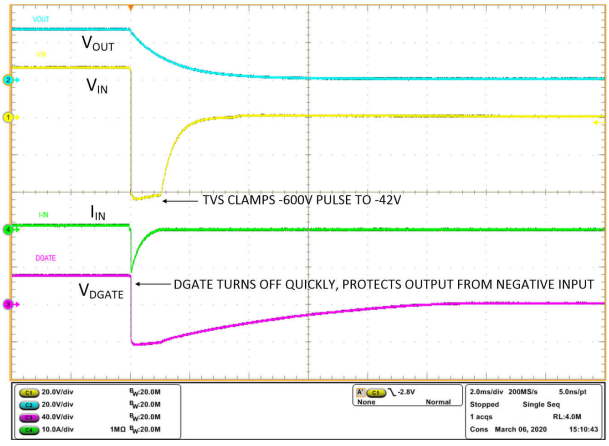


図 10-23. ISO 7637-2 Pulse 1 –600 V 50 Ω

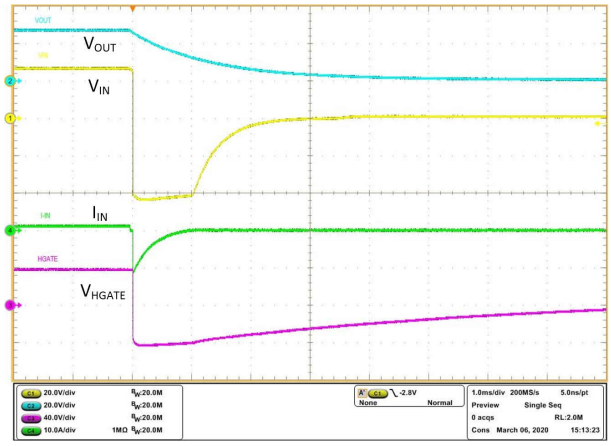


図 10-24. ISO 7637-2 Pulse 1 –600 V 50 Ω

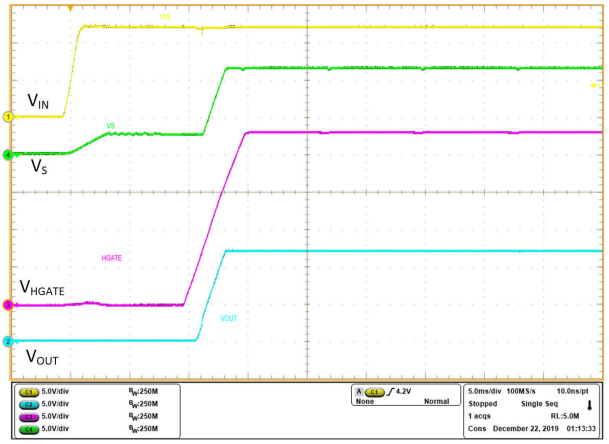


図 10-25. Power up 12 V - HGATE and Output

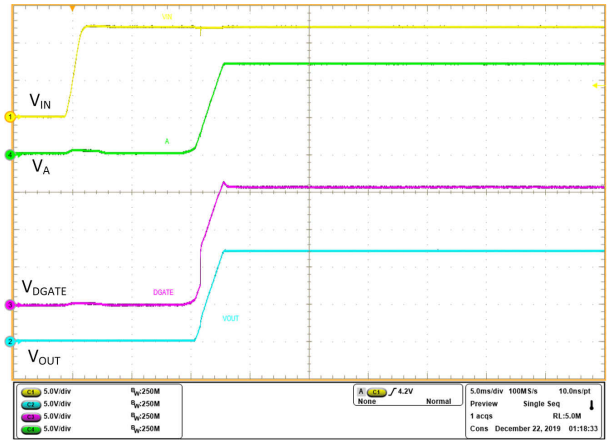


図 10-26. Power up 12 V - DGATE and A

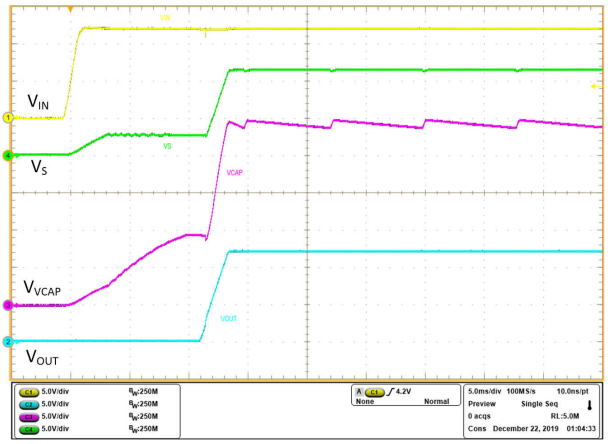


図 10-27. Power up 12 V - Charge Pump VCAP

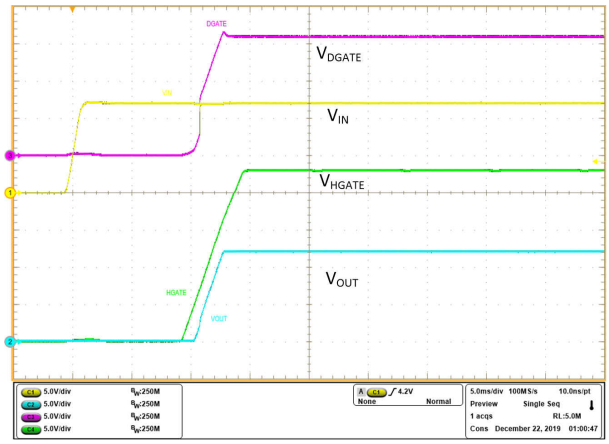


図 10-28. Power up 12 V - DGATE and HGATE

10.4 Do's and Don'ts

- Leave the exposed pad (RTN) of the IC floating. Do not connect the exposed pad to the GND plane. Connecting RTN to GND disables the reverse polarity protection feature.
- Connect a limiting resistor R_{PD} in series with the PD pin in the system application designs with input voltage above 48 V. This resistor value can be chosen in the range of 270 Ω to 330 Ω.

10.5 Power Supply Recommendations

10.5.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as overvoltage cut-off, reverse current blocking, EN/UVLO causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device.
- Using large PCB GND plane.
- Use of a Schottky diode across the output and GND to absorb negative spikes.
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 8.

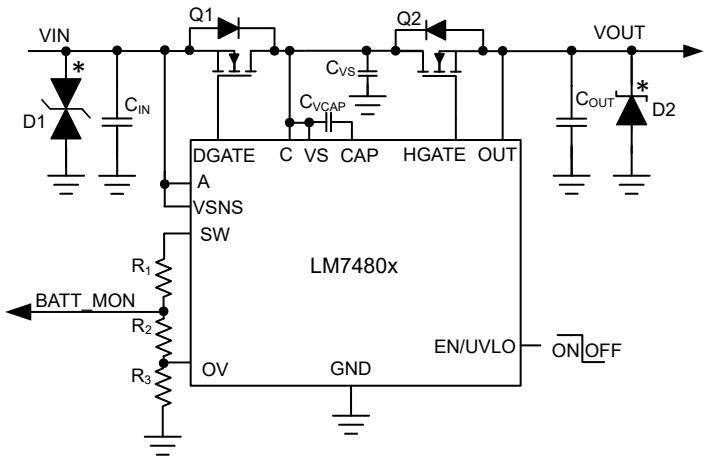
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (9)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in 図 10-29



* Optional components needed for suppression of transients

図 10-29. Circuit Implementation with Optional Protection Components for LM7480

10.5.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM7480 (65 V). The breakdown voltage of TVS- should be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM7480 (85 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM7480 is pulled down by the ISO pulse, clamped by TVS- and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- should not exceed, (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current as shown in and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS' are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

10.5.3 TVS Selection for 24-V Battery Systems

For 24-V battery protection application, the TVS and MOSFET in 図 10-1 needs to be changed to suit 24-V battery requirements.

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM7480 (70 V) and should withstand 65-V suppressed load dump.

The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12-A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (- TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- should not exceed, 85 V – 32 V = 53 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65V, maximum clamping voltage is ≤ 53 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ28A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ28A and SMBJ58A connected back-back at the input.

10.6 Layout

10.6.1 Layout Guidelines

- For the ideal diode stage, connect A, GATE and C pins of LM74720-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path of for this solution is through the MOSFET; therefore, it is important to use thick and short traces for source and drain of the MOSFET to minimize resistive losses.
- The GATE pin of the LM74720-Q1 must be connected to the MOSFET GATE with short trace.
- Boost converter switching currents flow into LX, CAP, GND pins and C3 (across DRAIN of the FET to GND). The loops formed by capacitor across CAP pin and DRAIN of the FET and C3 to GND must be minimized by placing these capacitors as close as possible. Keep the GND side of the C3 capacitor close to GND pin of LM74720-Q1.
- Place transient suppression components like input TVS and output Schottky close to LM74720-Q1.

10.6.2 Layout Example

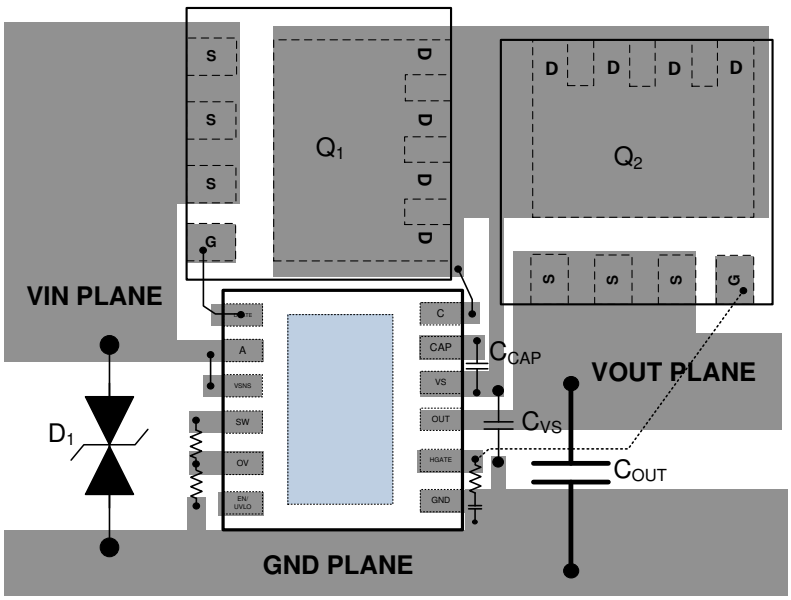


図 10-30. PCB Layout Example for Common Drain Configuration

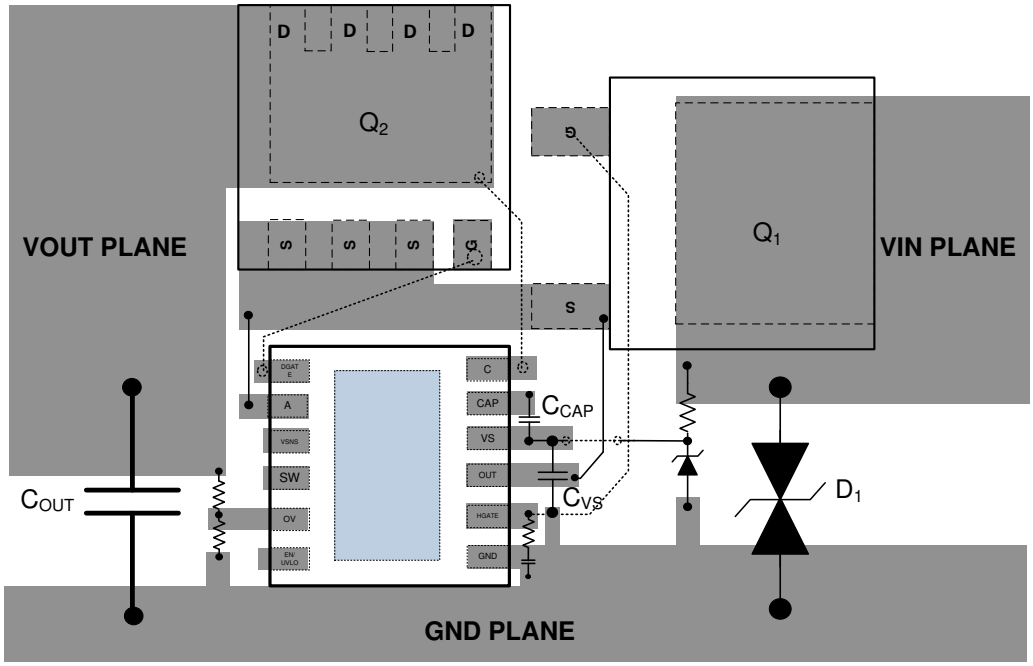


図 10-31. PCB Layout Example for Common Source Configuration

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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11.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM74800MDRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ET7480
LM74800MDRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ET7480
LM74801MDRRR	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T74801
LM74801MDRRR.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T74801

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM7480 :

- Automotive : LM7480-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

GENERIC PACKAGE VIEW

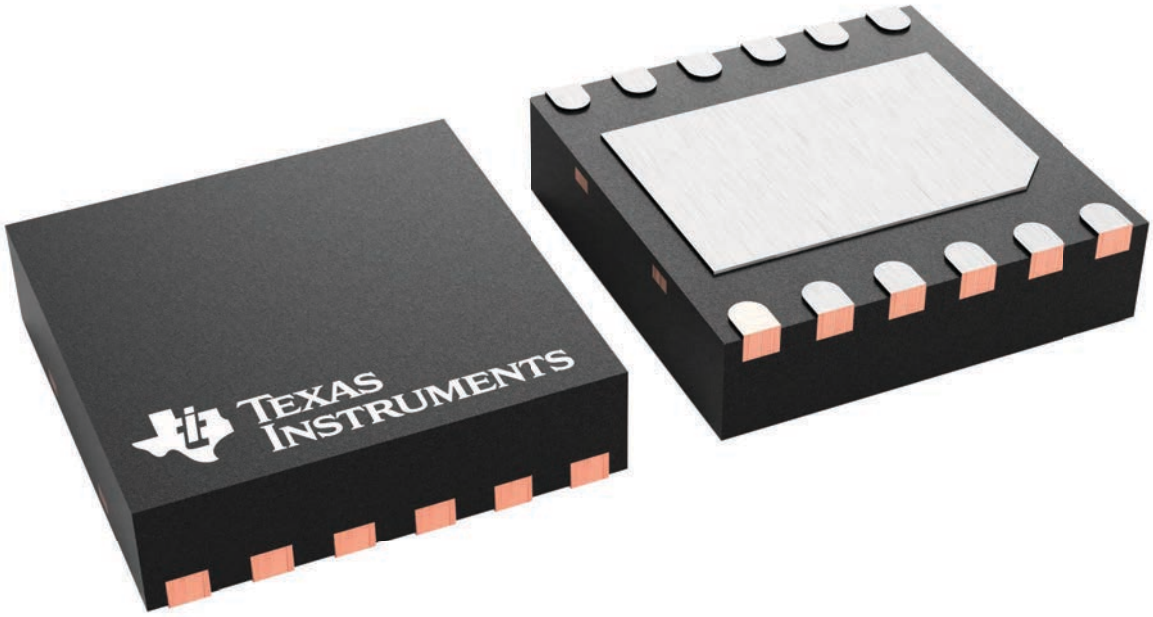
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



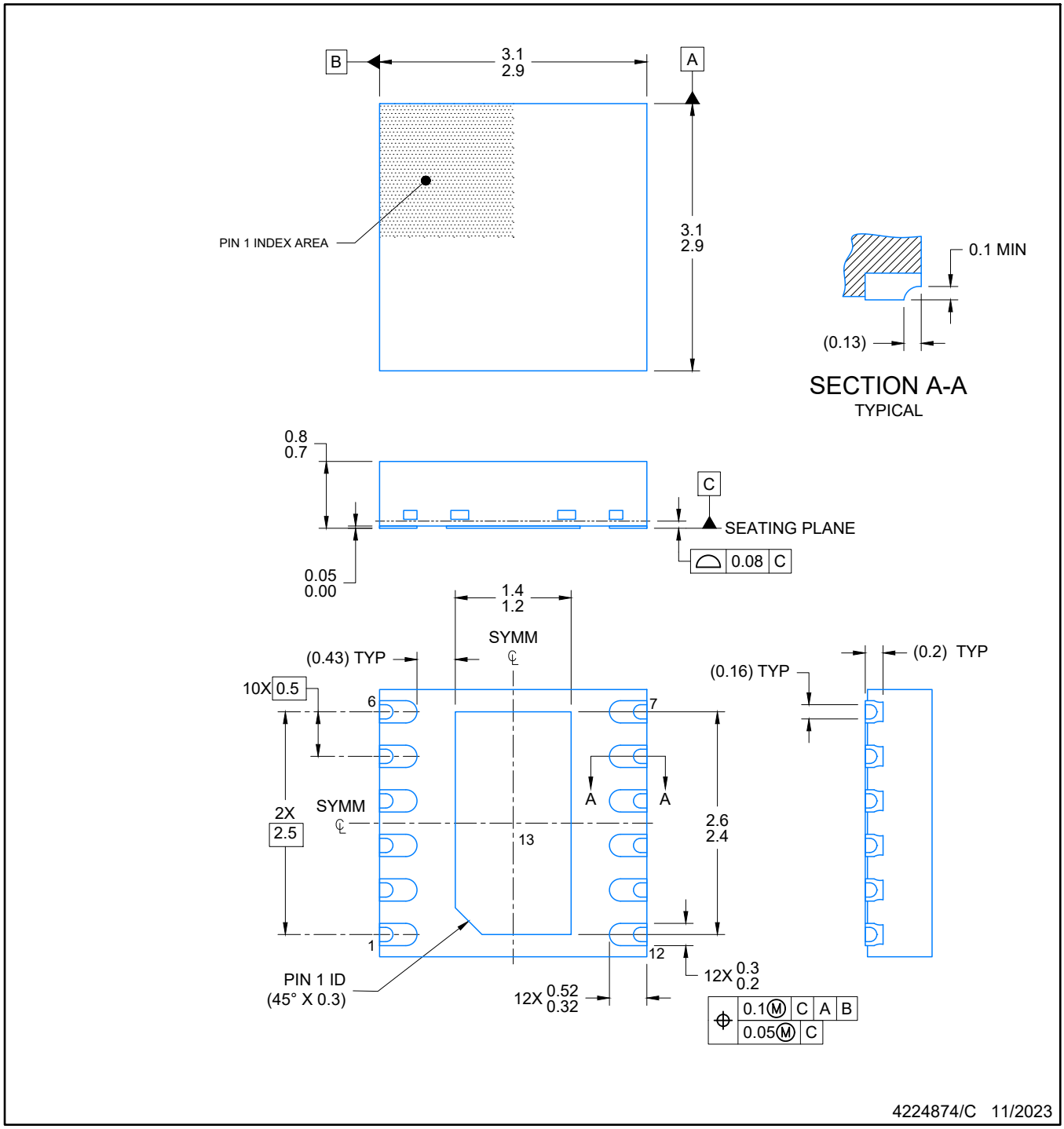
4223490/B

PACKAGE OUTLINE

DRR0012E

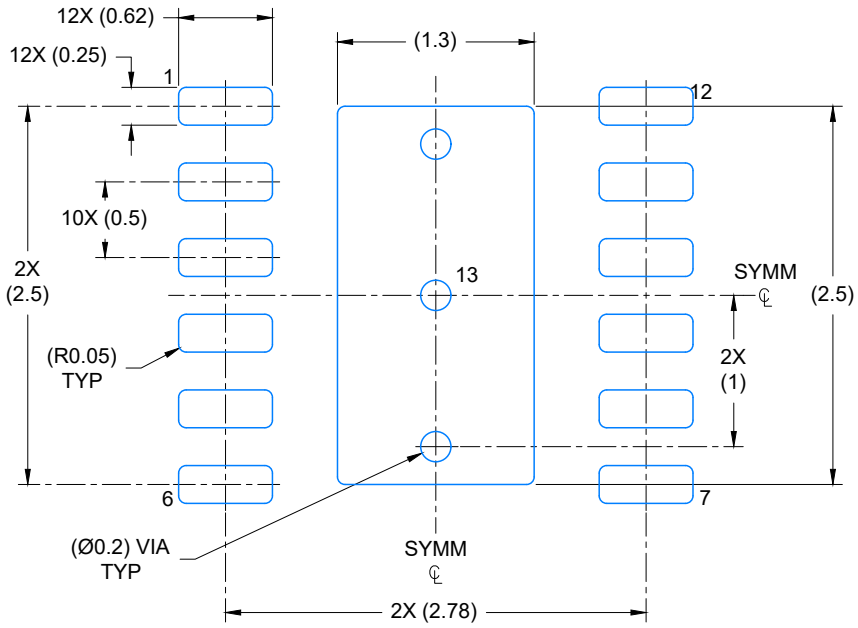
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

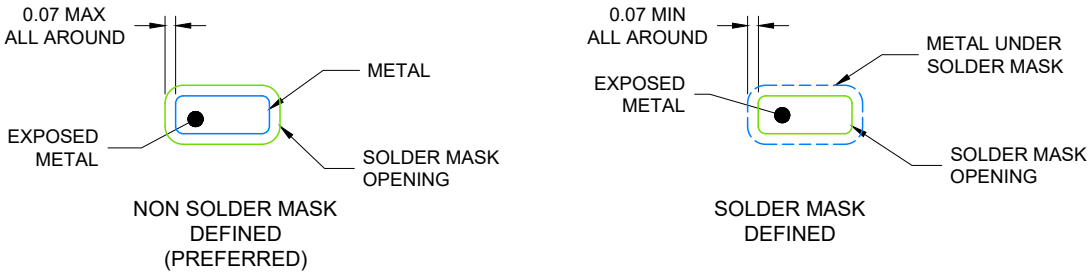


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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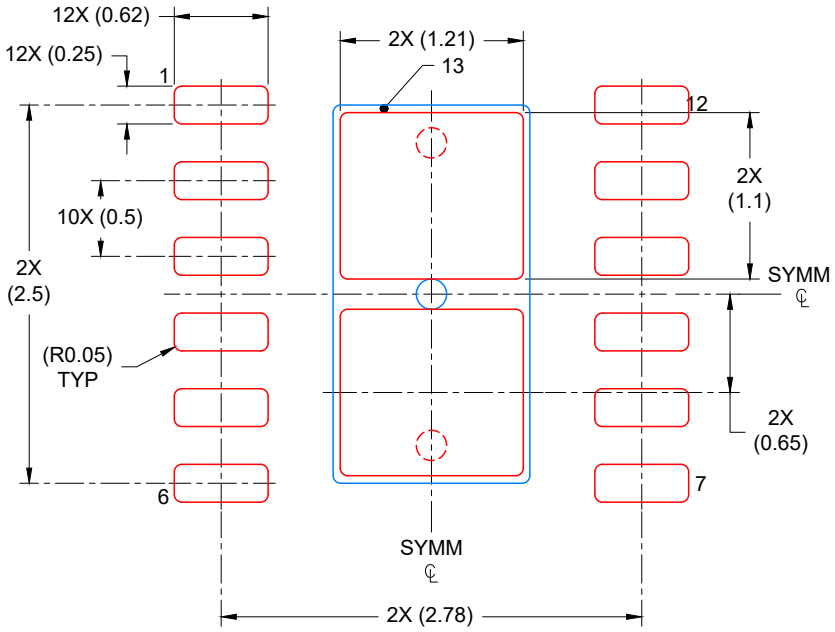
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月