TEXAS INSTRUMENTS
LM7171
JAJS842D – MAY 1999 – REVISED FEBRUARY 2024

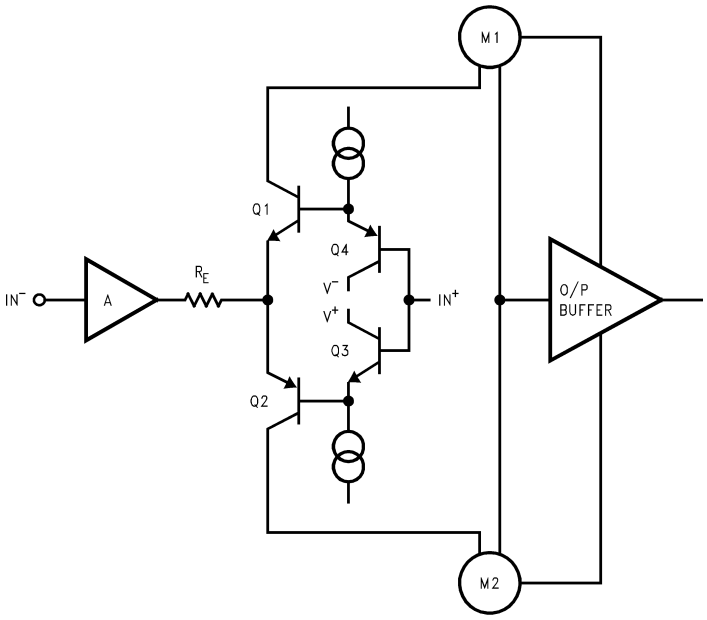
# LM7171 超高速、大出力電流、電圧帰還型アンプ

## 1 特長

- 特に記述のない限り標準値
- 使いやすい電圧帰還トポロジ
- 非常に高いスルーレート:4100V/µs
- 広いユニティ ゲイン帯域幅:200MHz
- $A_V$ = +2 での -3dB 周波数:220MHz
- 低い消費電流:6.5mA
- 高いオープン ループ ゲイン:85dB
- 大出力電流:100mA
- 差動ゲインおよび位相:0.01%、0.02º
- ±15V および ±5V での動作を規定

## 2 アプリケーション

- HDSL および ADSL ドライバ
- マルチメディア放送システム
- プロフェッショナル ビデオ カメラ
- ビデオ アンプ
- コピー機、スキャナ、ファックス
- HDTV アンプ
- パルス アンプおよびピーク検出器
- CATV および光ファイバー信号処理




**注:**M1 と M2 は電流ミラーです。

**概略回路図**

## 3 概要

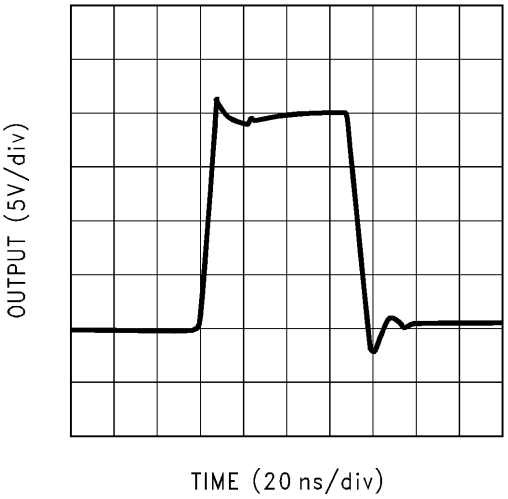
LM7171 は、電流帰還アンプと同様のスルーイング特性を持つ高速電圧帰還アンプですが、従来のすべての電圧帰還アンプ構成に使用できます。LM7171 は +2 倍 または -1 倍 の低いゲインで安定です。LM6171 は、わずか 6.5mA の消費電流で、4100V/µs の高速なスルーレートと 200MHz の広いユニティ ゲイン帯域幅を実現します。LM7171 は、HDSL やパルスアンプなどのビデオおよび高速信号処理アプリケーションに最適です。100mA の出力電流があるので、LM7171 はビデオ配信、トランスドライバ、またはレーザー ダイオード ドライバとして使用できます。

±15V 電源での動作により、大きな信号スイングが可能で、ダイナミック レンジと信号対雑音比 (SNR) が向上します。LM7171 は SFDR と THD が低く、ADC/DAC システムに最適です。さらに、LM7171 は、携帯機器のアプリケーション向けに ±5V での動作が規定されています。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| LM7171 | D (SOIC、8) | 4.90mm × 6mm |
| | P (PDIP、8) | 9.81mm × 9.43mm |

(1) 詳細については、セクション 9 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




**大信号パルス応答 $A_V$ = +2、$V_S$ = ±15V**

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## 4 Pin Configuration and Functions

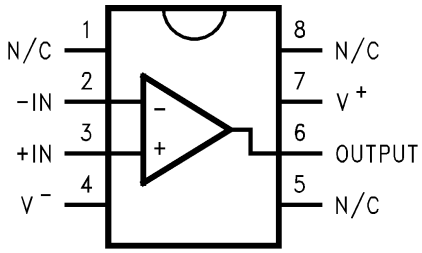



**図 4-1. D Package, 8-Pin SOIC (Top View)**

**表 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | NC | — | No connection |
| 2 | –IN | Input | Inverting power supply |
| 3 | +IN | Input | Noninverting power supply |
| 4 | V– | Input | Supply voltage |
| 5 | NC | — | No connection |
| 6 | OUTPUT | Output | Output |
| 7 | V+ | Input | Supply voltage |
| 8 | NC | — | No connection |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage ($V^+ – V^–$) | | 36 | V |
| VI | Differential input voltage(2) | | ±10 | V |
| $I_{SC}$ | Output current short to ground(3) | | Continuous | A |
| $T_J$ | Junction temperature(4) | | 150 | ℃ |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input differential voltage is applied at $V_S$ = ±15V.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A)/R_{θJA}$. All numbers apply for packages soldered directly into a PC board.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | V |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 2500V HBM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage | 5.5 | | 36 | V |
| $T_A$ | Ambient temperature | −40 | | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | LM7171 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) A Version | D (SOIC) B Version | P (PDIP) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 122.5 | 172 | 108 | ℃/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 64.7 | 62.4 | 52.4 | ℃/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 65.9 | 55.7 | 51.9 | ℃/W |
| $Ψ_{JT}$ | Junction-to-top characterization parameter | 17.6 | 16.5 | 6.8 | ℃/W |
| $Ψ_{JB}$ | Junction-to-board characterization parameter | 65.1 | 55.1 | 51.1 | ℃/W |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | ℃/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics: ±15V

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | LM7171A | | | 0.2 | 1 | mV |
| | | | $T_A$ = –40°C to +85°C | | | 4 | |
| | | LM7171B | | | 0.2 | 3 | |
| | | | $T_A$ = –40°C to +85°C | | | 7 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 35 | | µV/°C |
| $I_B$ | Input bias current | | | | 2.7 | 10 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 12 | |
| $I_{OS}$ | Input offset current | | | | 0.1 | 4 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 6 | |
| $R_{IN}$ | Input resistance | Common mode | | | 320 | | MΩ |
| | | Differential mode | | | 18 | | |
| $R_O$ | Open-loop output resistance | | | | 19 | | Ω |
| CMRR | Common-mode rejection ratio | LM7171A | $V_{CM}$ = ±10V | 85 | 105 | | dB |
| | | | $V_{CM}$ = ±10V, $T_A$ = –40°C to +85°C | 80 | | | |
| | | LM7171B | $V_{CM}$ = ±10V | 75 | 105 | | |
| | | | $V_{CM}$ = ±10V, $T_A$ = –40°C to +85°C | 70 | | | |
| PSRR | Power supply rejection ratio | LM7171A | $V_S$ = ±15V | 85 | 90 | | dB |
| | | | $V_S$ = ±15V, $T_A$ = –40°C to +85°C | 80 | | | |
| | | LM7171B | $V_S$ = ±15V | | | | |
| | | | $V_S$ = ±15V, $T_A$ = –40°C to +85°C | | | | |
| $V_{CM}$ | Input common-mode voltage | CMRR > 60dB | | | ±13.35 | | V |
| $A_V$ | Large-signal voltage gain | LM7171A | $R_L$ = 1kΩ, $V_{OUT}$ = ±5V | 80 | 85 | | dB |
| | | | $R_L$ = 1kΩ, $V_{OUT}$ = ±5V, $T_A$ = –40°C to +85°C | 75 | | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±5V | 75 | 81 | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±5V, $T_A$ = –40°C to +85°C | 70 | | | |
| | | LM7171B | $R_L$ = 1kΩ, $V_{OUT}$ = ±5V | 75 | 85 | | |
| | | | $R_L$ = 1kΩ, $V_{OUT}$ = ±5V, $T_A$ = –40°C to +85°C | 70 | | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±5V | 70 | 81 | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±5V, $T_A$ = –40°C to +85°C | 66 | | | |
| $V_O$ | Output swing | $R_L$ = 1kΩ | | 13 | 13.3 | | V |
| | | | $T_A$ = –40°C to +85°C | 12.7 | | | |
| | | $R_L$ = 1kΩ | | –13 | –13.2 | | |
| | | | $T_A$ = –40°C to +85°C | –12.7 | | | |
| | | $R_L$ = 100Ω | | 10.5 | 11.8 | | |
| | | | $T_A$ = –40°C to +85°C | 9.5 | | | |
| | | $R_L$ = 100Ω | | –9.5 | –10.5 | | |
| | | | $T_A$ = –40°C to +85°C | –9 | | | |

## 5.5 Electrical Characteristics: ±15V (続き)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Output current (open loop) | Sourcing, $R_L$ = 100Ω | | 105 | 118 | | mA |
| | | | $T_A$ = –40°C to +85°C | 95 | | | |
| | | Sinking, $R_L$ = 100Ω | | 95 | 105 | | |
| | | | $T_A$ = –40°C to +85°C | 90 | | | |
| | Output current (in linear region) | Sourcing, $R_L$ = 100Ω | | | 100 | | |
| | | Sinking, $R_L$ = 100Ω | | | 100 | | |
| $I_{SC}$ | Output short-circuit current | Sourcing | | | 140 | | |
| | | Sinking | | | 135 | | |
| $I_S$ | Supply current | | | | 6.5 | 8.5 | |
| | | | | | | 9.5 | |
| SR | Slew rate | $A_V$ = +2, $V_{IN}$ = 13$V_{PP}$ | | | 4100 | | V/µs |
| | | $A_V$ = +2, $V_{IN}$ = 10$V_{PP}$ | | | 3100 | | |
| | Unity-gain bandwidth | LM7171A | | | 160 | | MHz |
| | | LM7171B | | | 200 | | |
| | −3dB frequency | $A_V$ = +2 | | | 220 | | MHz |
| $\varphi_m$ | Phase margin | | | | 50 | | Deg |
| $t_s$ | Settling time (0.1%) | $A_V$ = −1, $V_{OUT}$ = ±5V, $R_L$ = 500Ω | LM7171A | | 16 | | ns |
| | | | LM7171B | | 42 | | ns |
| $t_p$ | Propagation delay | $A_V$ = −2, $V_{IN}$ = ±1V, $R_L$ = 500Ω | | | 5 | | ns |
| HD2 | Second harmonic distortion | LM7171A | $f_{IN}$ = 10kHz | | –123 | | dBc |
| | | | $f_{IN}$ = 5MHz | | –75 | | |
| | | LM7171B | $f_{IN}$ = 10kHz | | –110 | | |
| | | | $f_{IN}$ = 5MHz | | –75 | | |
| HD3 | Third harmonic distortion | LM7171A | $f_{IN}$ = 10kHz | | –133 | | dBc |
| | | | $f_{IN}$ = 5MHz | | –88 | | |
| | | LM7171B | $f_{IN}$ = 10kHz | | –115 | | |
| | | | $f_{IN}$ = 5MHz | | –55 | | |
| $e_n$ | Input-referred voltage noise | f = 10kHz | LM7171A | | 8.5 | | nV/√Hz |
| | | | LM7171B | | 14 | | |
| $i_n$ | Input-referred current noise | f = 10kHz | LM7171A | | 1 | | pA/√Hz |
| | | | LM7171B | | 1.5 | | |

## 5.6 Electrical Characteristics: ±5V

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | LM7171A | | | 0.3 | 1.5 | mV |
| | | | $T_A$ = –40°C to +85°C | | | 4 | |
| | | LM7171B | | | 0.3 | 3.5 | |
| | | | $T_A$ = –40°C to +85°C | | | 7 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 35 | | µV/°C |
| $I_B$ | Input bias current | | | | 3.3 | 10 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 12 | |
| $I_{OS}$ | Input offset current | | | | 0.1 | 4 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 6 | |
| $R_{IN}$ | Input resistance | Common mode | | | 250 | | MΩ |
| | | Differential mode | | | 18 | | |
| $R_O$ | Open-loop output resistance | | | | 18 | | Ω |
| CMRR | Common-mode rejection ratio | LM7171A | $V_{CM}$ = ±2.5V | 80 | 104 | | dB |
| | | | $V_{CM}$ = ±2.5V, $T_A$ = –40°C to +85°C | 75 | | | |
| | | LM7171B | $V_{CM}$ = ±2.5V | 70 | 104 | | |
| | | | $V_{CM}$ = ±2.5V, $T_A$ = –40°C to +85°C | 65 | | | |
| PSRR | Power supply rejection ratio | LM7171A | $V_S$ = ±5V | 85 | 90 | | dB |
| | | | $V_S$ = ±5V, $T_A$ = –40°C to +85°C | 80 | | | |
| | | LM7171B | $V_S$ = ±5V | 75 | 90 | | |
| | | | $V_S$ = ±5V, $T_A$ = –40°C to +85°C | 70 | | | |
| $V_{CM}$ | Input common-mode voltage range | CMRR > 60dB | | | ±3.2 | | V |
| $A_V$ | Large-signal voltage gain | LM7171A | $R_L$ = 1kΩ, $V_{OUT}$ = ±1V | 75 | 78 | | dB |
| | | | $R_L$ = 1kΩ, $V_{OUT}$ = ±1V, $T_A$ = –40°C to +85°C | 70 | | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±1V | 72 | 76 | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±1V, $T_A$ = –40°C to +85°C | 67 | | | |
| | | LM7171B | $R_L$ = 1kΩ, $V_{OUT}$ = ±1V | 70 | 78 | | |
| | | | $R_L$ = 1kΩ, $V_{OUT}$ = ±1V, $T_A$ = –40°C to +85°C | 65 | | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±1V | 68 | 76 | | |
| | | | $R_L$ = 100Ω, $V_{OUT}$ = ±1V, $T_A$ = –40°C to +85°C | 63 | | | |
| $V_O$ | Output swing | $R_L$ = 1kΩ | | 3.2 | 3.4 | | V |
| | | | | –3.2 | –3.4 | | |
| | | | $T_A$ = –40°C to +85°C | 3 | | | |
| | | | | –3 | | | |
| | | $R_L$ = 100Ω | | 2.9 | 3.1 | | |
| | | | | –2.9 | –3 | | |
| | | | $T_A$ = –40°C to +85°C | 2.8 | | | |
| | | | | –2.8 | | | |

## 5.6 Electrical Characteristics: ±5V (続き)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Output current (open loop) | Sourcing, $R_L$ = 100Ω | | 29 | 31 | | mA |
| | | | $T_A$ = –40°C to +85°C | 28 | | | |
| | | Sinking, $R_L$ = 100Ω | | 29 | 30 | | |
| | | | $T_A$ = –40°C to +85°C | 28 | | | |
| | Output current (in linear region) | Sourcing, $R_L$ = 100Ω | | | 30 | | mA |
| | | Sinking, $R_L$ = 100Ω | | | 31 | | |
| $I_{SC}$ | Output short-circuit current | Sourcing | | | 135 | | mA |
| | | Sinking | | | 100 | | |
| $I_S$ | Supply current | | | | 6.2 | 8 | mA |
| | | $T_A$ = –40°C to +85°C | | | | 9 | |
| SR | Slew rate | $A_V$ = +2, $V_{IN}$ = 3.2$V_{PP}$ | LM7171A | | 1200 | | V/µs |
| | | | LM7171B | | 950 | | |
| | Unity-gain bandwidth | LM7171A | | | 125 | | MHz |
| | | LM7171B | | | 125 | | |
| | −3dB frequency | $A_V$ = +2 | LM7171A | | 140 | | MHz |
| | | | LM7171B | | 140 | | |
| $\varphi_m$ | Phase margin | LM7171A | | | 68 | | Deg |
| | | LM7171B | | | 57 | | |
| $t_s$ | Settling time (0.1%) | $A_V$ = −1, $V_{OUT}$ = ±1V, $R_L$ = 500Ω | LM7171A | | 15 | | ns |
| | | | LM7171B | | 56 | | |
| $t_p$ | Propagation delay | $A_V$ = −2, $V_{IN}$ = ±1V, $R_L$ = 500Ω | LM7171A | | 2.5 | | ns |
| | | | LM7171B | | 6 | | |
| HD2 | Second harmonic distortion | LM7171A | $f_{IN}$ = 10kHz | | –125 | | dBc |
| | | | $f_{IN}$ = 5MHz | | –72 | | |
| | | LM7171B | $f_{IN}$ = 10kHz | | –102 | | |
| | | | $f_{IN}$ = 5MHz | | –70 | | |
| HD3 | Third harmonic distortion | LM7171A | $f_{IN}$ = 10kHz | | –129 | | dBc |
| | | | $f_{IN}$ = 5MHz | | –81 | | |
| | | LM7171B | $f_{IN}$ = 10kHz | | –110 | | |
| | | | $f_{IN}$ = 5MHz | | –51 | | |
| $e_n$ | Input-referred voltage noise | f = 10kHz | LM7171A | | 8.5 | | nV/√Hz |
| | | | LM7171B | | 14 | | |
| $i_n$ | Input-referred current noise | f = 10kHz | LM7171A | | 1 | | pA/√Hz |
| | | | LM7171B | | 1.8 | | |

## 5.7 Typical Characteristics: LM7171A

at $T_A$= 25°C (unless otherwise noted)

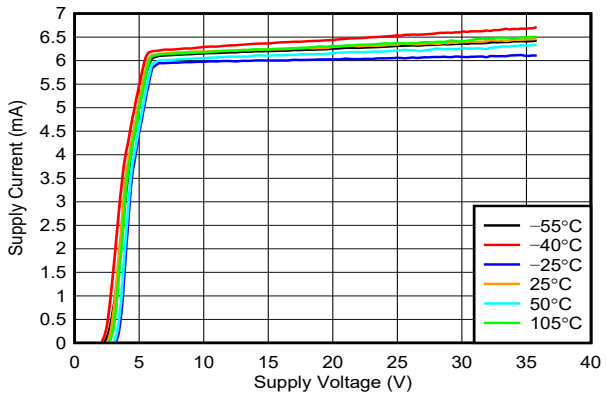



**図 5-1. Supply Current vs Supply Voltage**

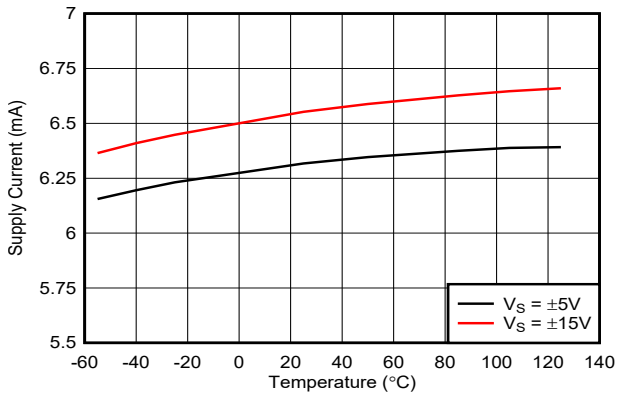



**図 5-2. Supply Current vs Temperature**

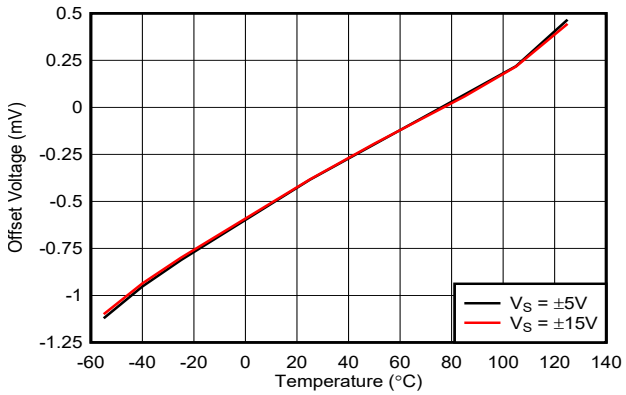



**図 5-3. Input Offset Voltage vs Temperature**

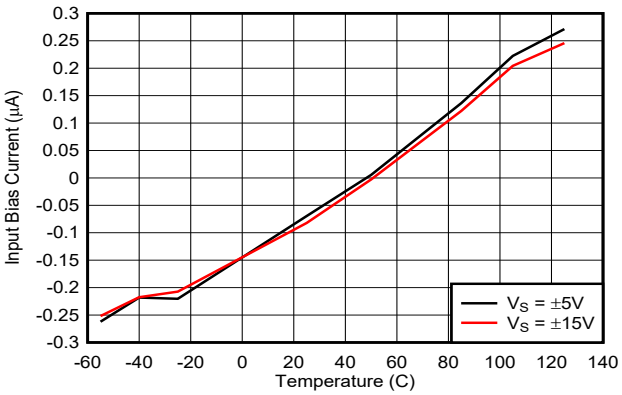



**図 5-4. Input Bias Current vs Temperature**

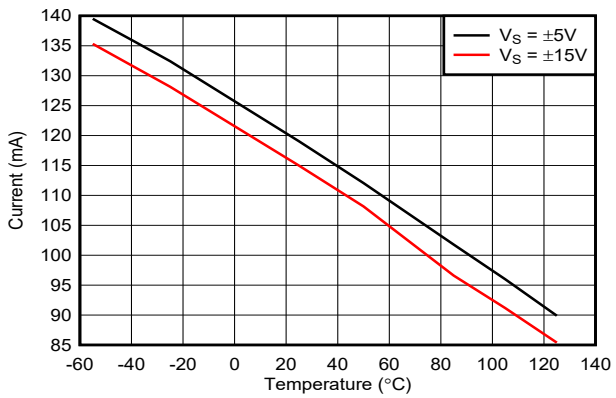



**図 5-5. Short Circuit Current vs Temperature (Sourcing)**

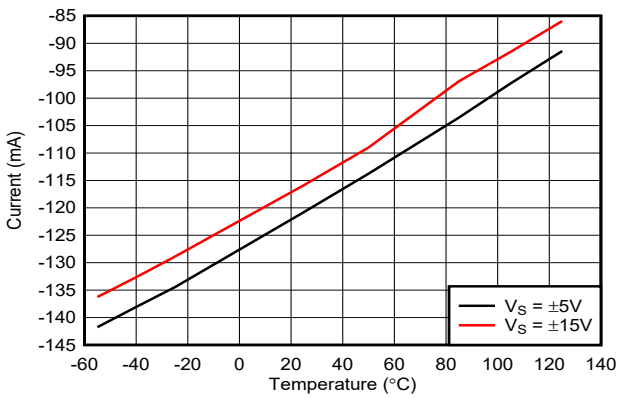
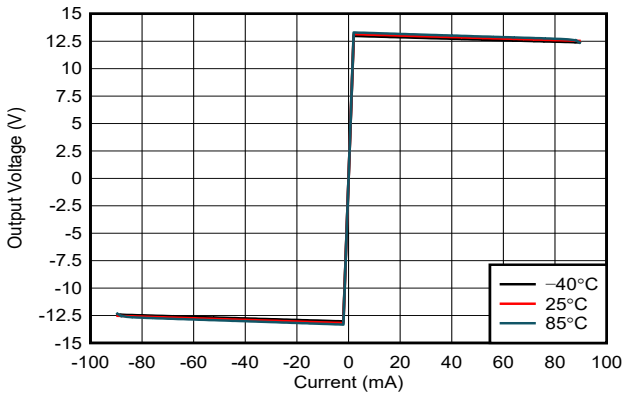



**図 5-6. Short Circuit Current vs Temperature (Sinking)**

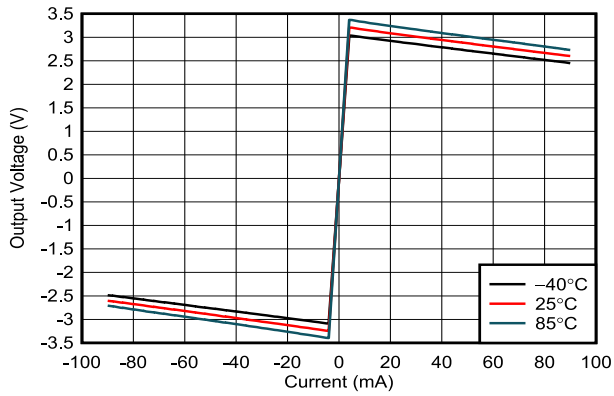
## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)




$V_S$ = ±15V

**図 5-7. Output Voltage vs Output Current**




$V_S$ = ±5V

**図 5-8. Output Voltage vs Output Current**

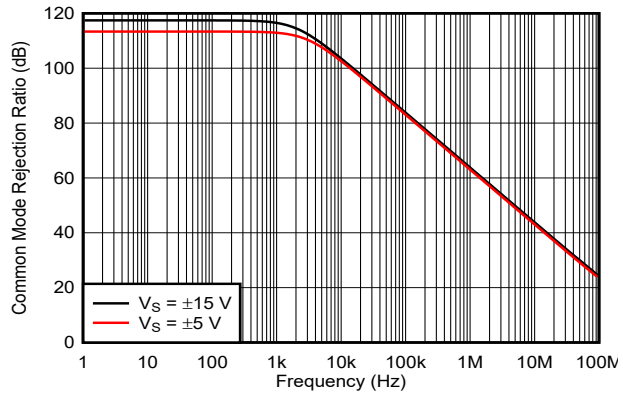
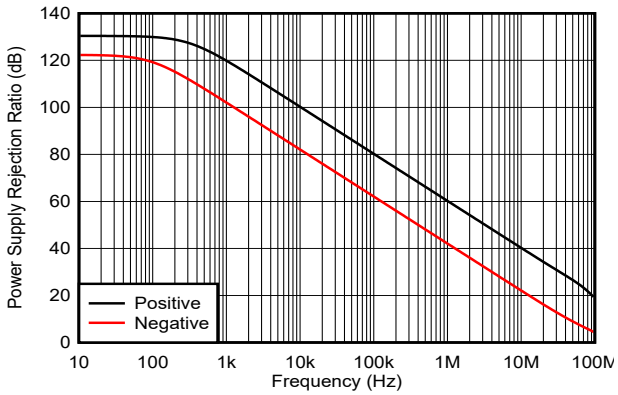
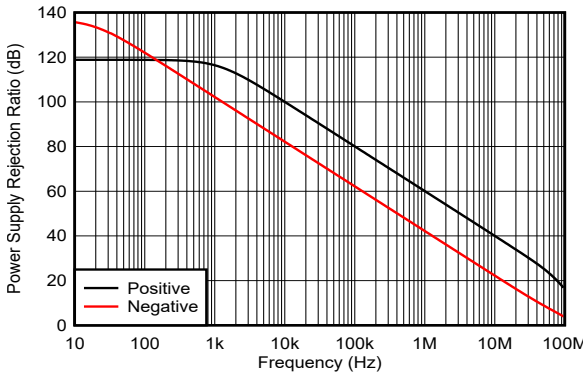



**図 5-9. CMRR vs Frequency**



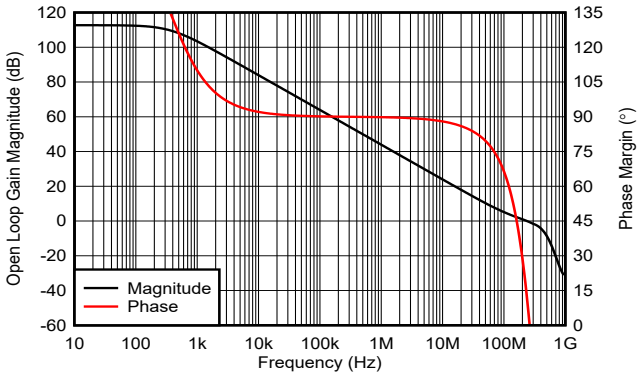

$V_S$ = 30V

**図 5-10. PSRR vs Frequency**




$V_S$ = 10V

**図 5-11. PSRR vs Frequency**

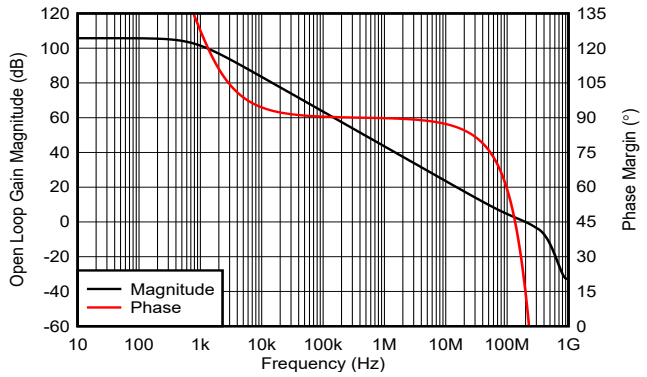



$V_S$ = ±15V

**図 5-12. Open Loop Frequency Response**

## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)




$V_S$ = ±5V

**図 5-13. Open Loop Frequency Response**

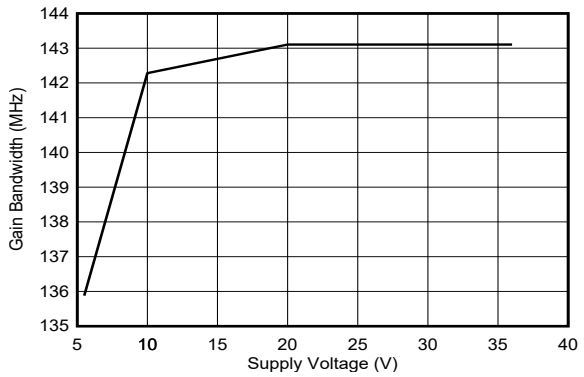



**図 5-14. Gain-Bandwidth Product vs Supply Voltage**

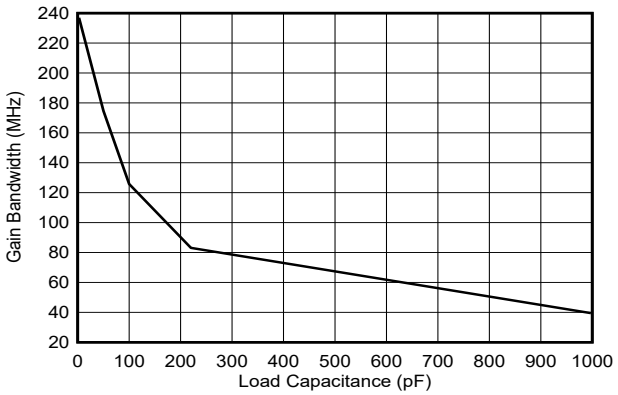



**図 5-15. Gain-Bandwidth Product vs Load Capacitance**

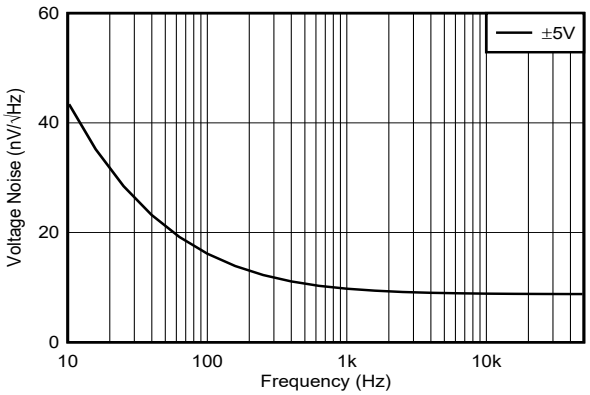



**図 5-16. Input Voltage Noise vs Frequency**

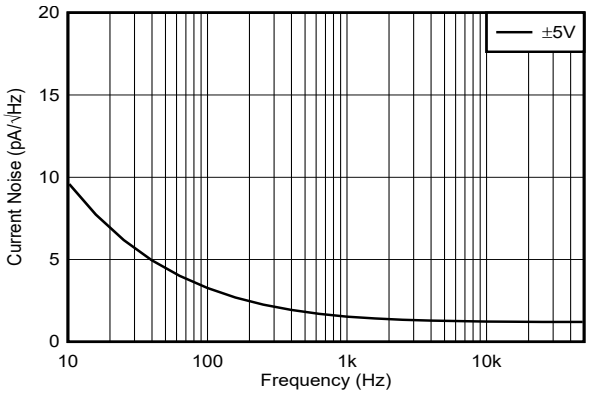



**図 5-17. Input Current Noise vs Frequency**

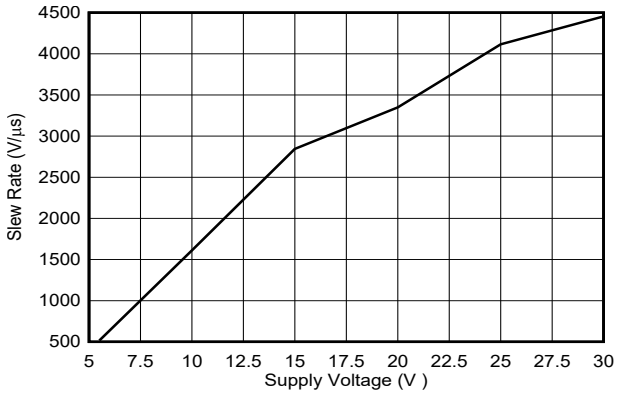



**図 5-18. Slew Rate vs Supply Voltage**

## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)

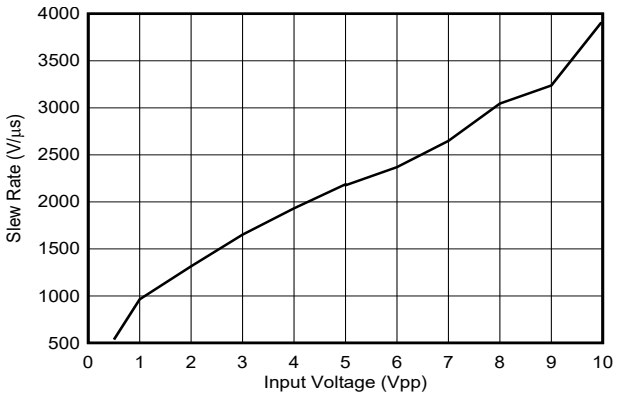



**図 5-19. Slew Rate vs Input Voltage**

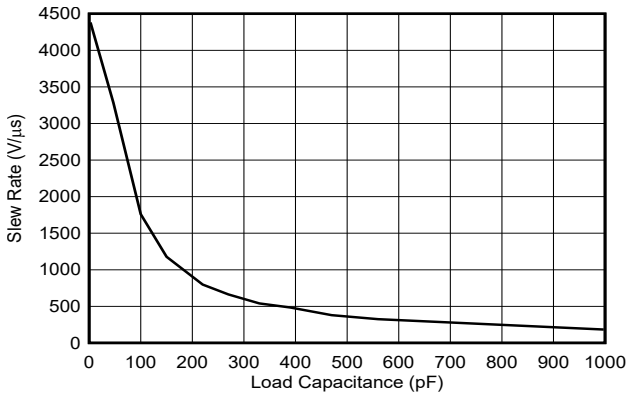
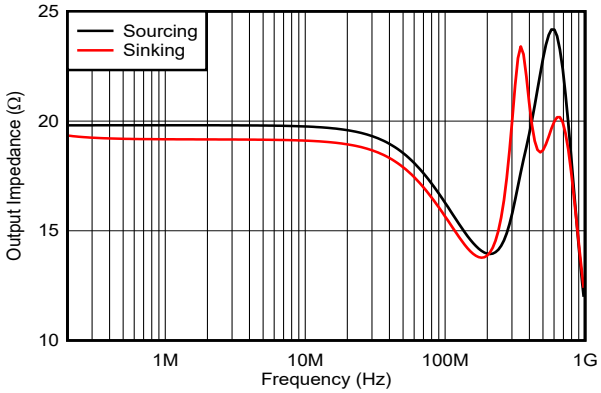
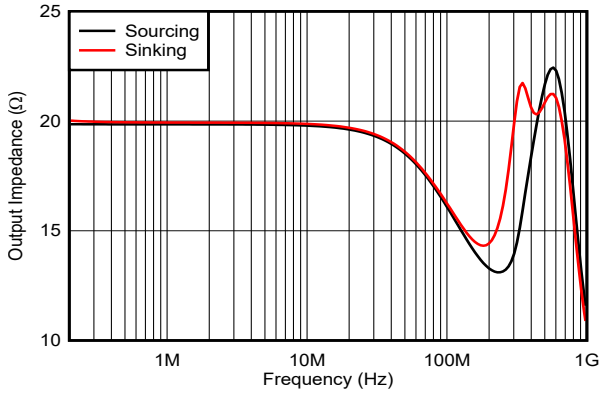



**図 5-20. Slew Rate vs Load Capacitance**



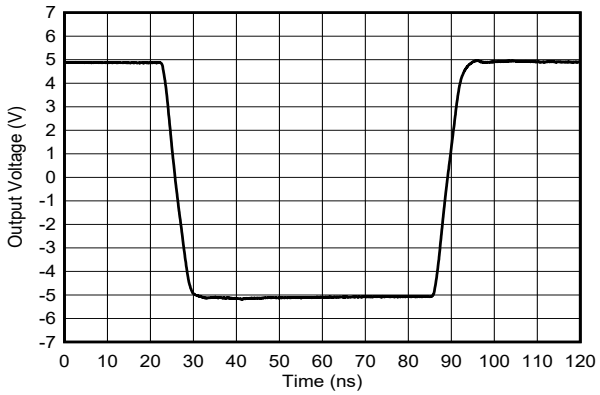

$V_S$ = ±15V

**図 5-21. Open Loop Output Impedance vs Frequency**



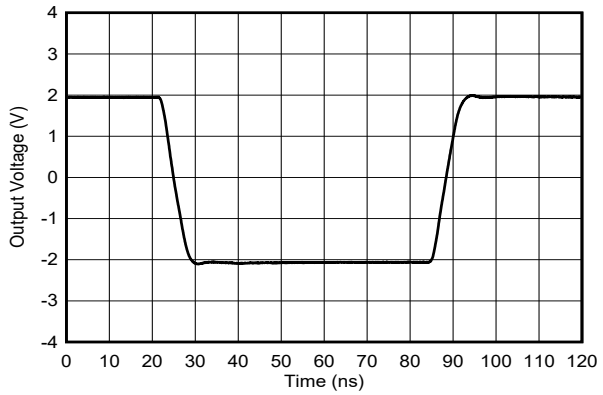

$V_S$ = ±5V

**図 5-22. Open Loop Output Impedance vs Frequency**




$A_V$ = −1 $V_S$ = ±15V

**図 5-23. Large-Signal Pulse Response**

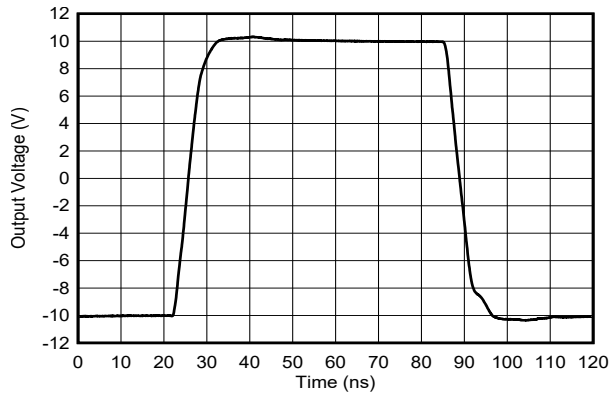



$A_V$ = −1 $V_S$ = ±5V

**図 5-24. Large-Signal Pulse Response**

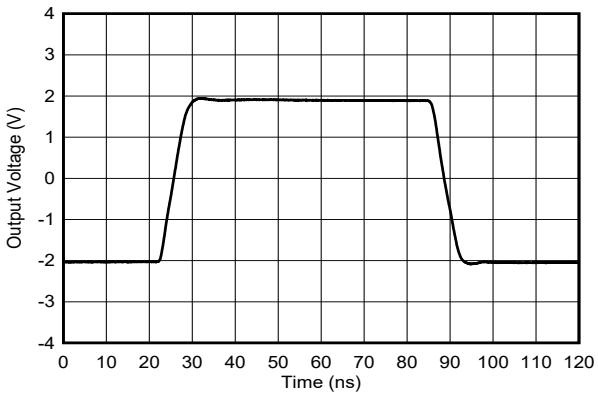
## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)



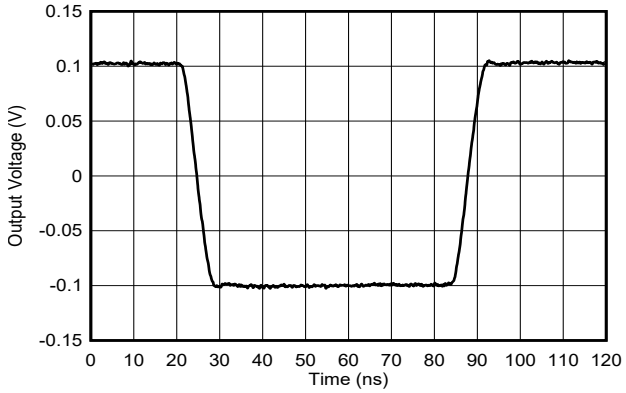

$A_V$ = +2 $V_S$ = ±15V

**図 5-25. Large-Signal Pulse Response**



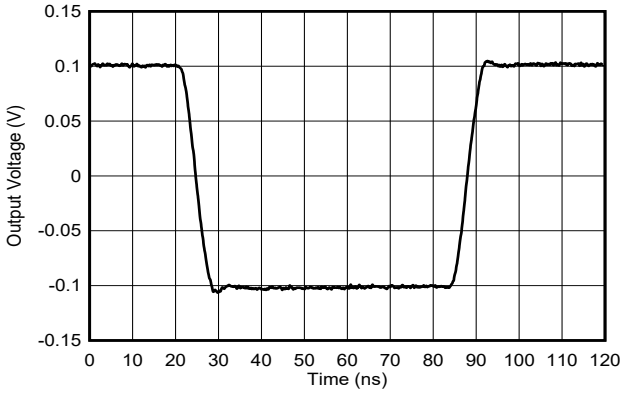

$A_V$ = +2 $V_S$ = ±5V

**図 5-26. Large-Signal Pulse Response**



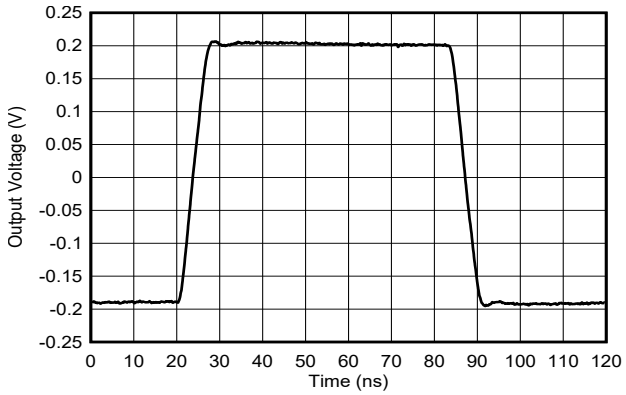

$A_V$ = −1 $V_S$ = ±15V

**図 5-27. Small-Signal Pulse Response**



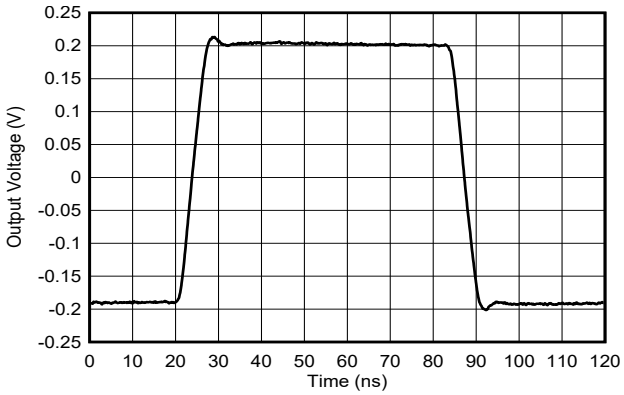

$A_V$ = −1 $V_S$ = ±5V

**図 5-28. Small-Signal Pulse Response**




$A_V$ = +2 $V_S$ = ±15V

**図 5-29. Small-Signal Pulse Response**

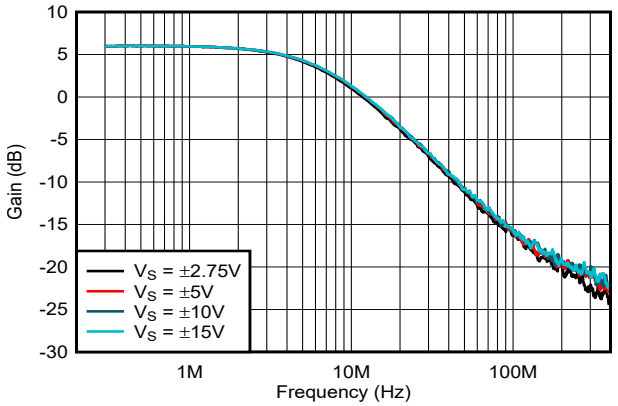



$A_V$ = +2 $V_S$ = ±5V

**図 5-30. Small-Signal Pulse Response**

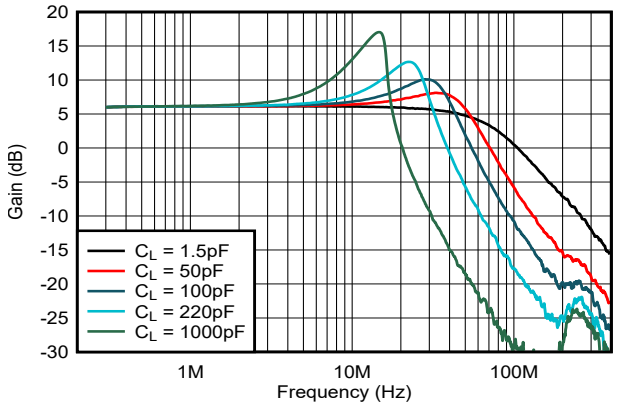
## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)



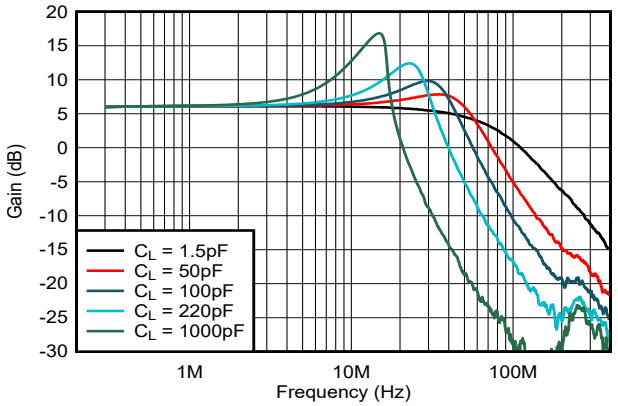

$A_V$ = +2

**図 5-31. Closed-Loop Frequency Response vs Supply Voltage**



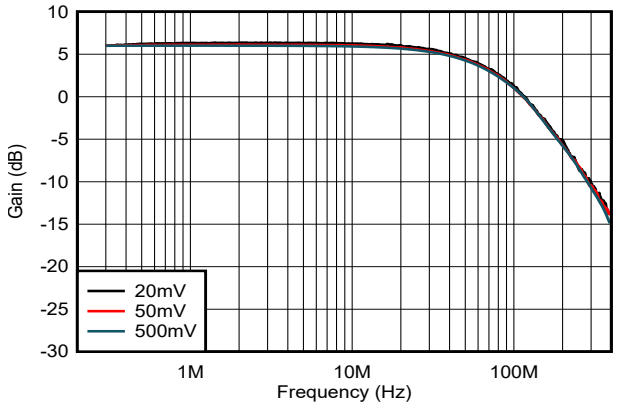

$A_V$ = +2 $V_S$ = ±5V

**図 5-32. Closed-Loop Frequency Response vs Capacitive Load**



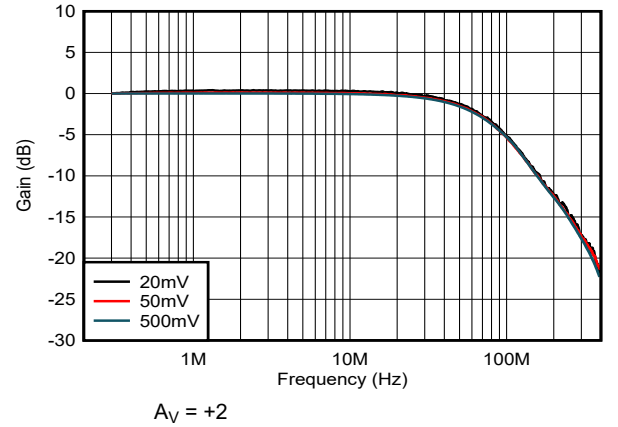

$A_V$ = +2 $V_S$ = ±15V

**図 5-33. Closed-Loop Frequency Response vs Capacitive Load**



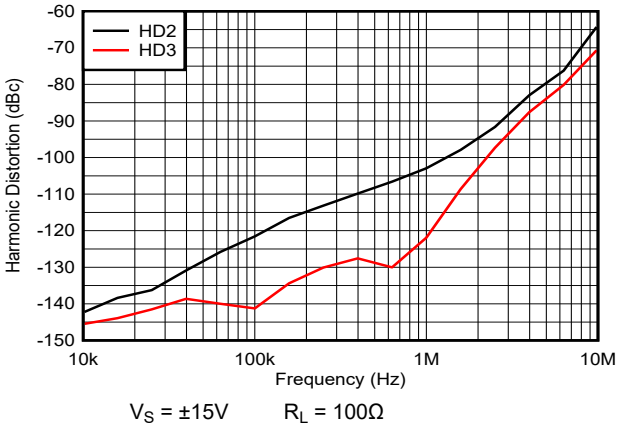

$A_V$ = +2

**図 5-34. Closed-Loop Frequency Response vs Input Signal Level**




$A_V$ = +2

**図 5-35. Closed-Loop Frequency Response vs Input Signal Level**

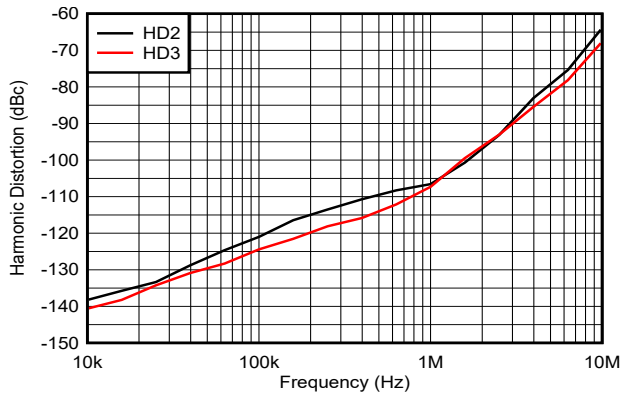



$V_S$ = ±15V $R_L$ = 100Ω

**図 5-36. Total Harmonic Distortion vs Frequency**

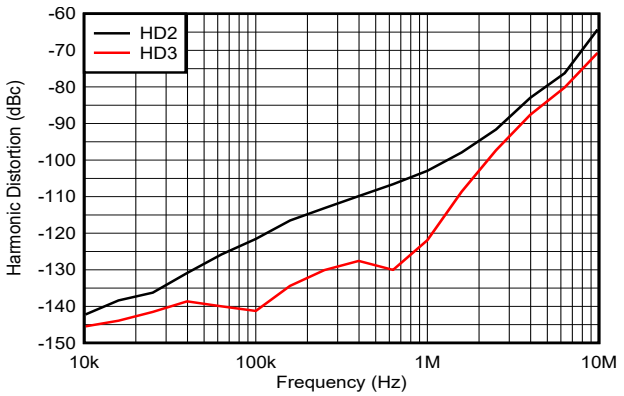
## 5.7 Typical Characteristics: LM7171A (continued)

at $T_A$= 25°C (unless otherwise noted)



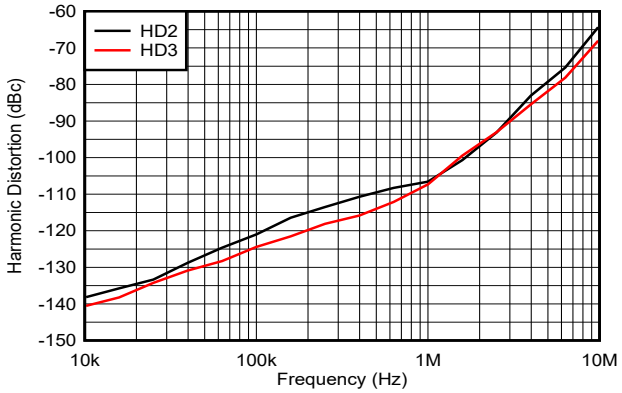

$V_S$ = ±5V $R_L$ = 100Ω

**図 5-37. Total Harmonic Distortion vs Frequency**




$V_S$ = ±15V $R_L$ = 2.5kΩ

**図 5-38. Harmonic Distortion vs Frequency**




$V_S$ = ±5V $R_L$ = 2.5kΩ

**図 5-39. Harmonic Distortion vs Frequency**

## 5.8 Typical Characteristics: LM7171B

at $T_A$= 25°C (unless otherwise noted)

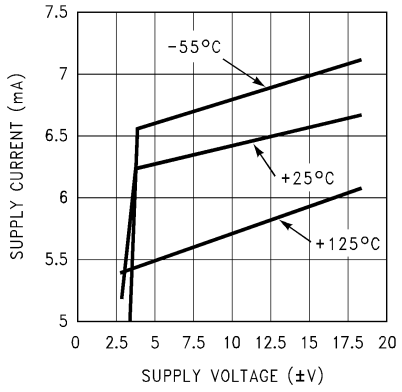



**図 5-40. Supply Current vs Supply Voltage**

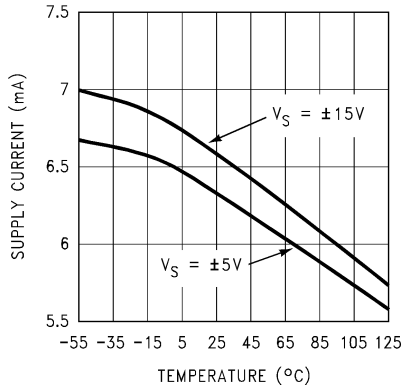



**図 5-41. Supply Current vs Temperature**

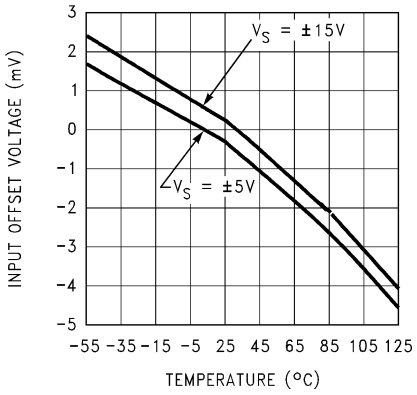



**図 5-42. Input Offset Voltage vs Temperature**

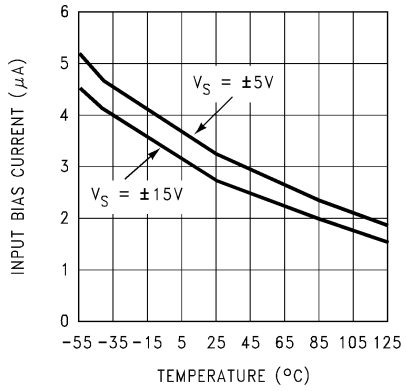



**図 5-43. Input Bias Current vs Temperature**

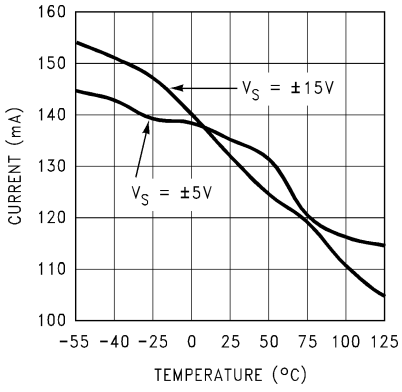



**図 5-44. Short Circuit Current vs Temperature (Sourcing)**

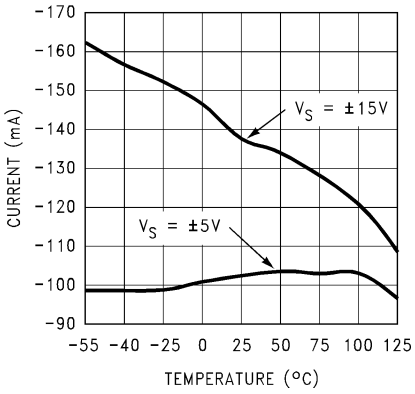



**図 5-45. Short Circuit Current vs Temperature (Sinking)**

## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)

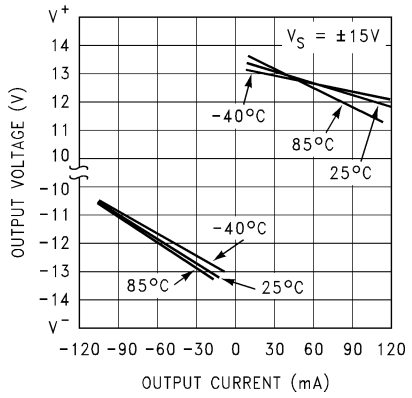



**図 5-46. Output Voltage vs Output Current**

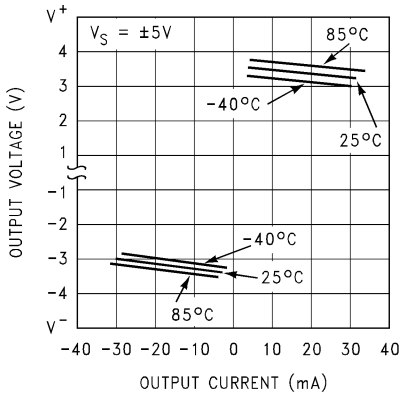



**図 5-47. Output Voltage vs Output Current**

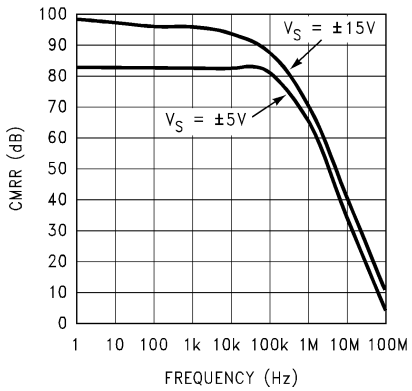



**図 5-48. CMRR vs Frequency**

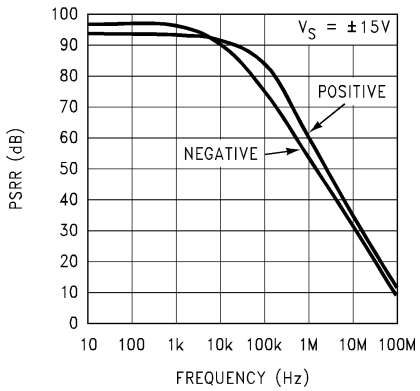



**図 5-49. PSRR vs Frequency**

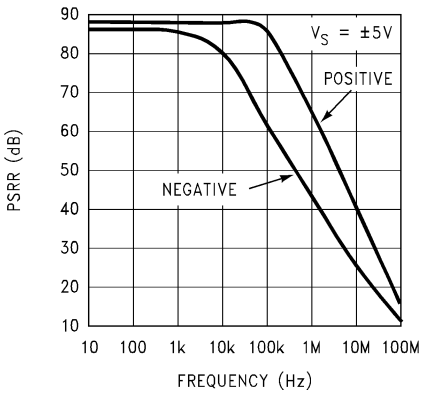



**図 5-50. PSRR vs Frequency**

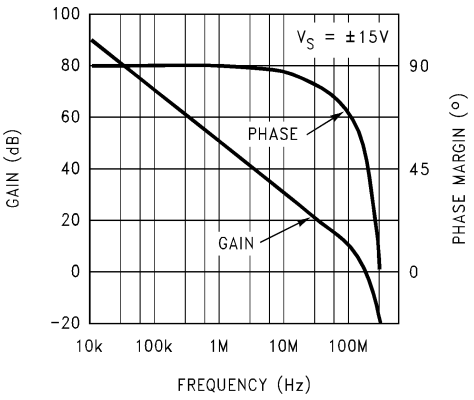



**図 5-51. Open Loop Frequency Response**

## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)

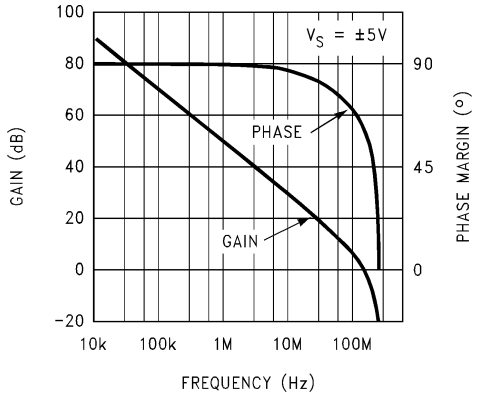



**図 5-52. Open Loop Frequency Response**

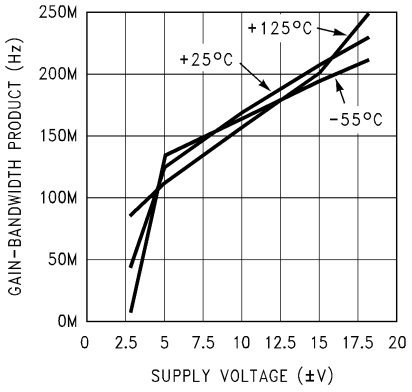



**図 5-53. Gain-Bandwidth Product vs Supply Voltage**

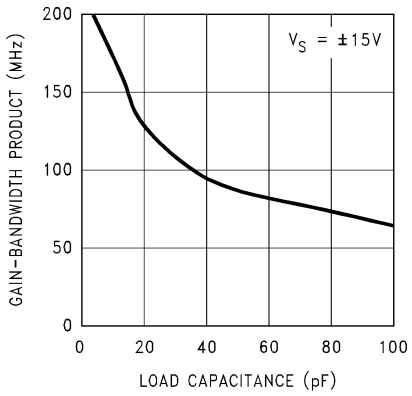



**図 5-54. Gain-Bandwidth Product vs Load Capacitance**

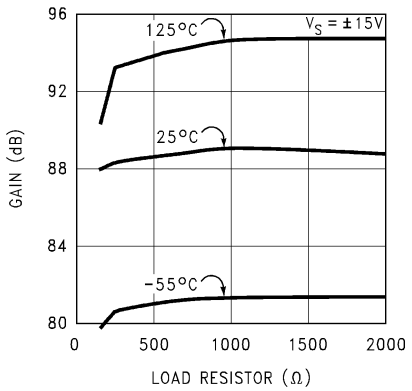



**図 5-55. Large Signal Voltage Gain vs Load**

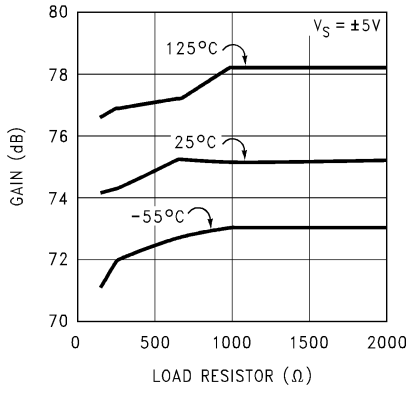



**図 5-56. Large Signal Voltage Gain vs Load**

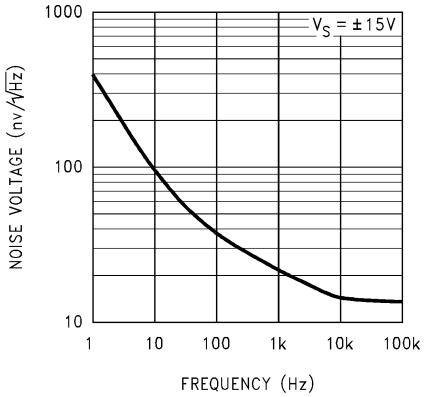



**図 5-57. Input Voltage Noise vs Frequency**

## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)

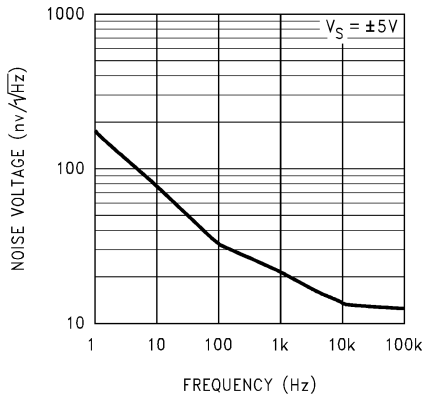



**図 5-58. Input Voltage Noise vs Frequency**

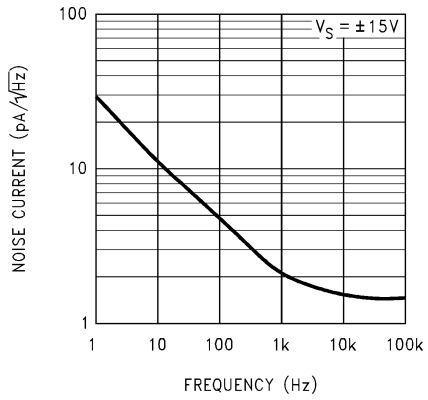



**図 5-59. Input Current Noise vs Frequency**

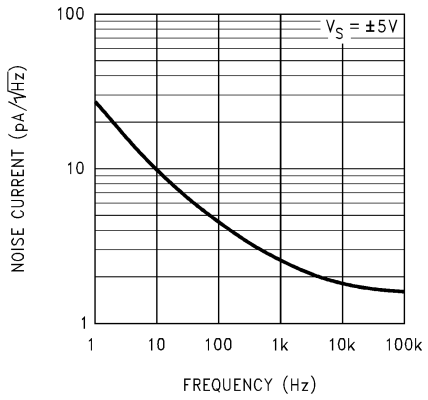



**図 5-60. Input Current Noise vs Frequency**

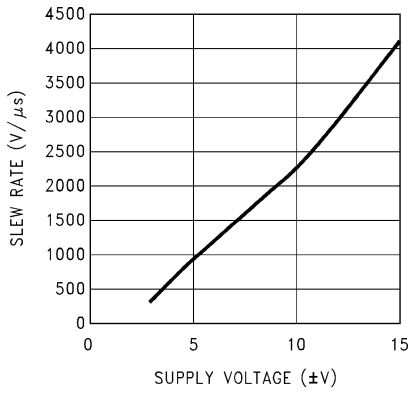



**図 5-61. Slew Rate vs Supply Voltage**

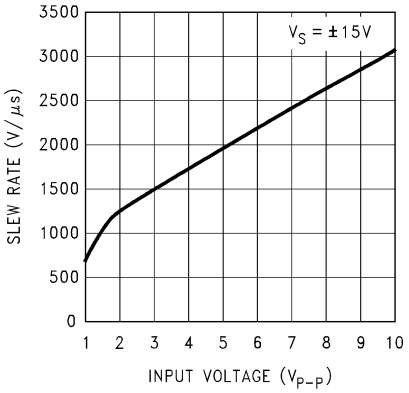



**図 5-62. Slew Rate vs Input Voltage**

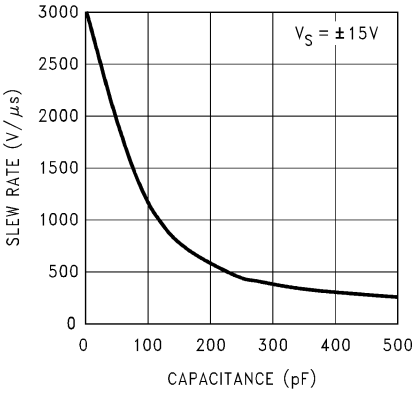



**図 5-63. Slew Rate vs Load Capacitance**

## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)

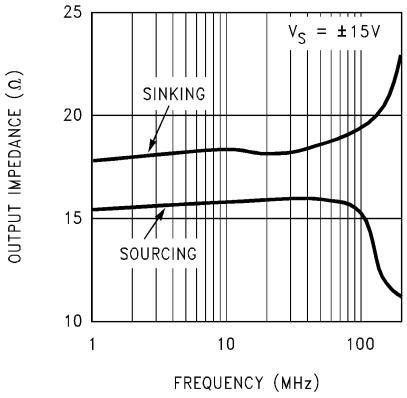



**図 5-64. Open Loop Output Impedance vs Frequency**

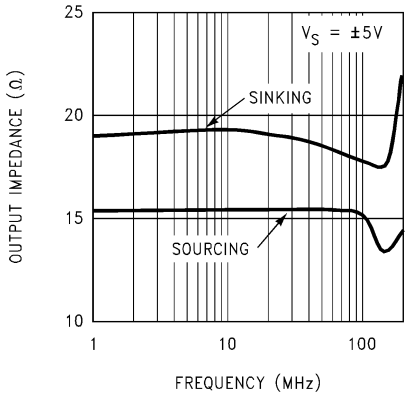
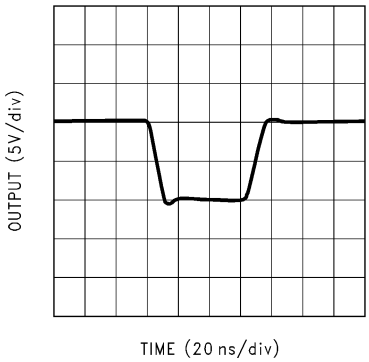
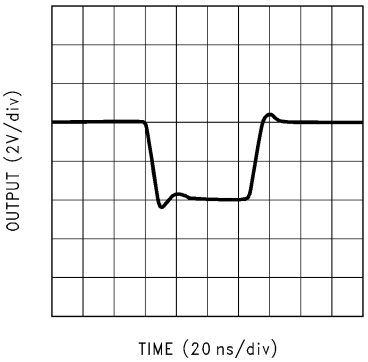



**図 5-65. Open Loop Output Impedance vs Frequency**



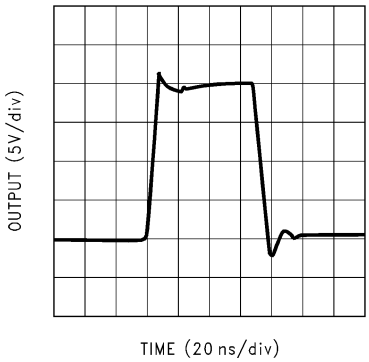

$A_V$ = –1 $V_S$ = ±15V

**図 5-66. Large-Signal Pulse Response**



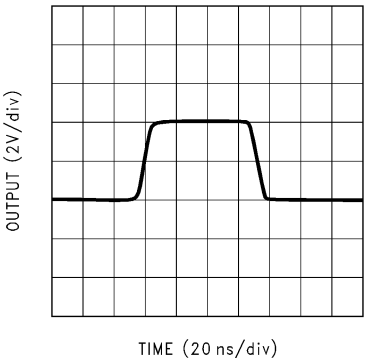

$A_V$ = –1 $V_S$ = ±5V

**図 5-67. Large-Signal Pulse Response**




$A_V$ = +2 $V_S$ = ±15V

**図 5-68. Large-Signal Pulse Response**

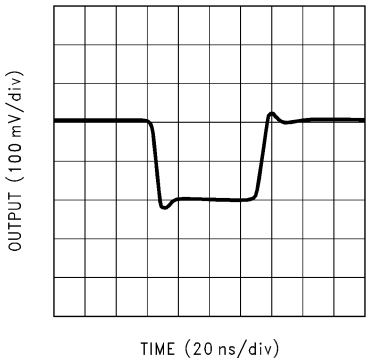



$A_V$ = +2 $V_S$ = ±5V

**図 5-69. Large-Signal Pulse Response**

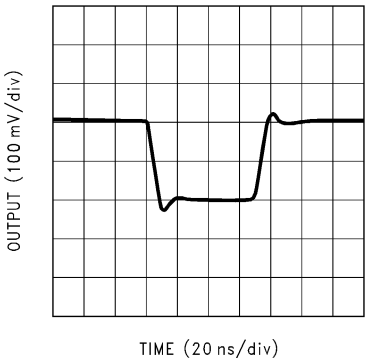
## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)



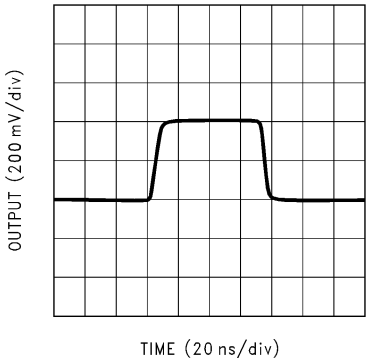

$A_V$ = –1 $V_S$ = ±15V

**図 5-70. Small-Signal Pulse Response**



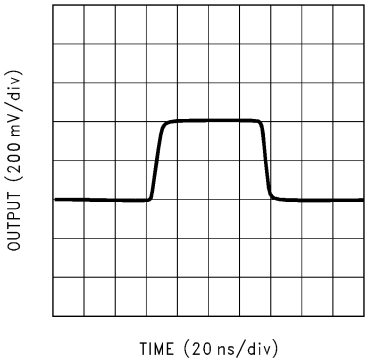

$A_V$ = –1 $V_S$ = ±5V

**図 5-71. Small-Signal Pulse Response**



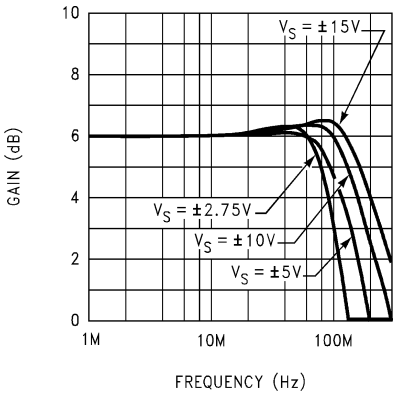

$A_V$ = +2 $V_S$ = ±15V

**図 5-72. Small-Signal Pulse Response**



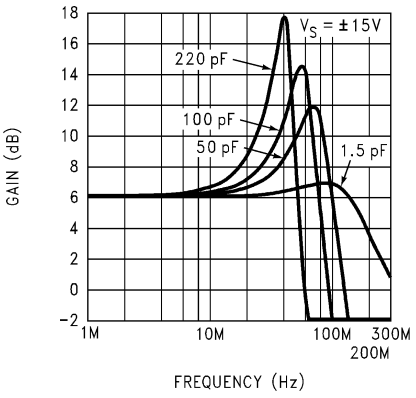

$A_V$ = +2 $V_S$ = ±5V

**図 5-73. Small-Signal Pulse Response**




$A_V$ = +2

**図 5-74. Closed-Loop Frequency Response vs Supply Voltage**

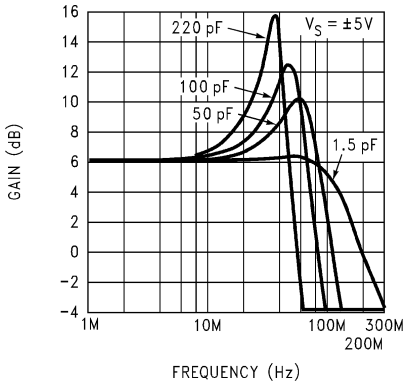



$A_V$ = +2

**図 5-75. Closed-Loop Frequency Response vs Capacitive Load**

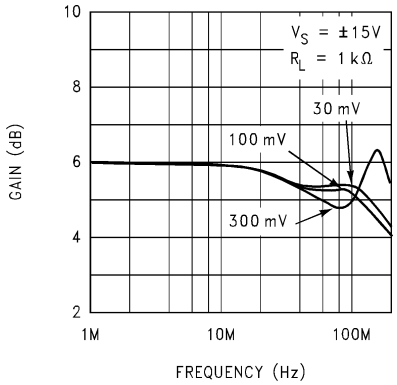
## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)



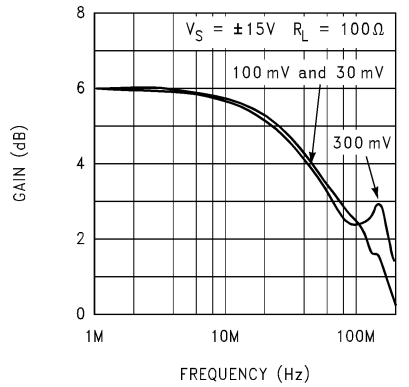

$A_V$ = +2

**図 5-76. Closed-Loop Frequency Response vs Capacitive Load**



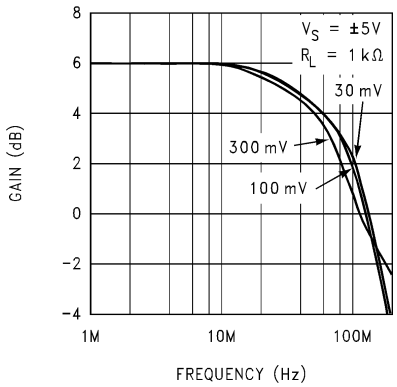

$A_V$ = +2

**図 5-77. Closed-Loop Frequency Response vs Input Signal Level**



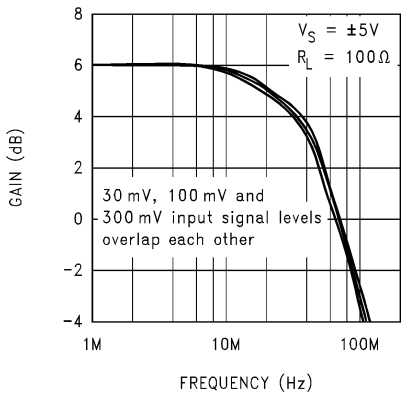

$A_V$ = +2

**図 5-78. Closed-Loop Frequency Response vs Input Signal Level**



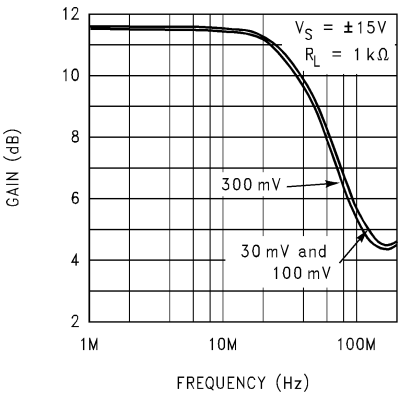

$A_V$ = +2

**図 5-79. Closed-Loop Frequency Response vs Input Signal Level**




$A_V$ = +2

**図 5-80. Closed-Loop Frequency Response vs Input Signal Level**

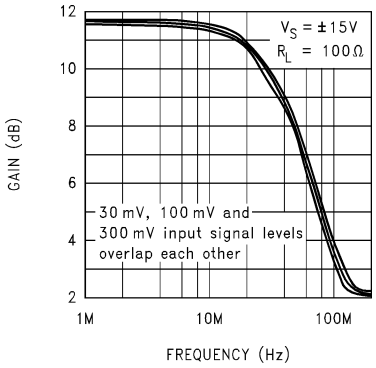



$A_V$ = +4

**図 5-81. Closed-Loop Frequency Response vs Input Signal Level**

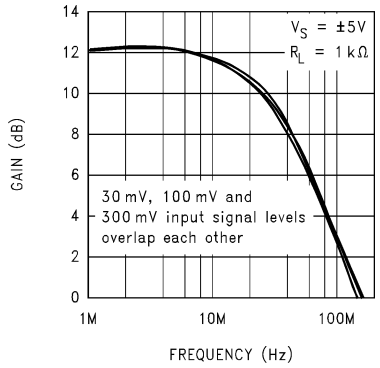
## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)



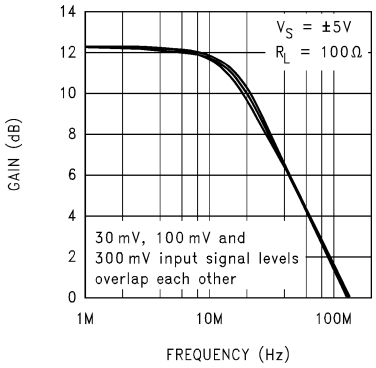

$A_V$ = +4

**図 5-82. Closed-Loop Frequency Response vs Input Signal Level**



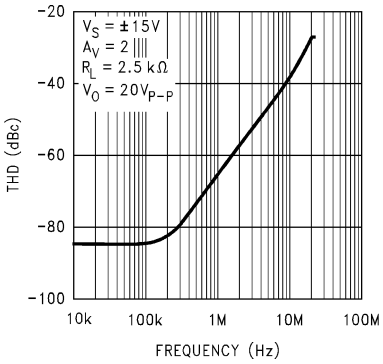

$A_V$ = +4

**図 5-83. Closed-Loop Frequency Response vs Input Signal Level**



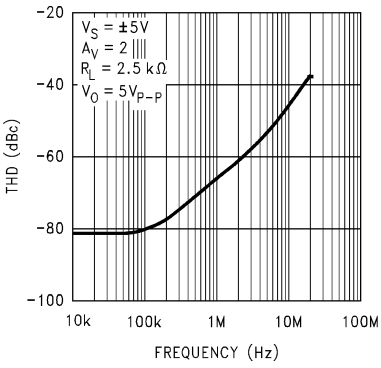

$A_V$ = +4

**図 5-84. Closed-Loop Frequency Response vs Input Signal Level**




THD measurement at low frequency limited by test instrument

**図 5-85. Total Harmonic Distortion vs Frequency**




THD measurement at low frequency limited by test instrument

**図 5-86. Total Harmonic Distortion vs Frequency**

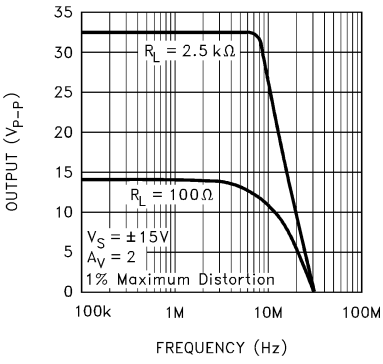



**図 5-87. Undistorted Output Swing vs Frequency**

## 5.8 Typical Characteristics: LM7171B (continued)

at $T_A$= 25°C (unless otherwise noted)

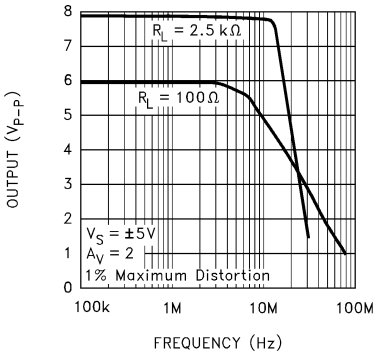



**図 5-88. Undistorted Output Swing vs Frequency**

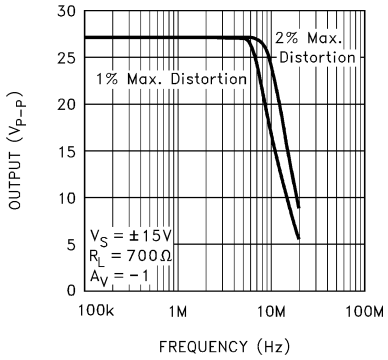
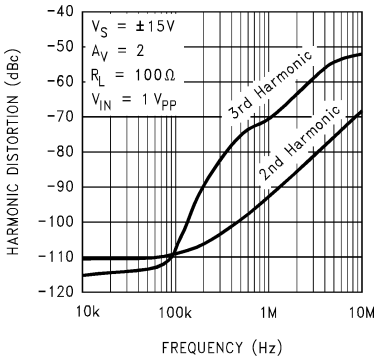
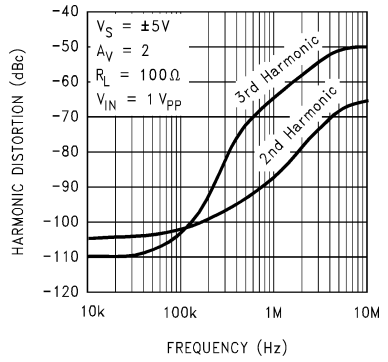



**図 5-89. Undistorted Output Swing vs Frequency**




THD measurement at low frequency limited by test instrument

**図 5-90. Harmonic Distortion vs Frequency**




THD measurement at low frequency limited by test instrument

**図 5-91. Harmonic Distortion vs Frequency**

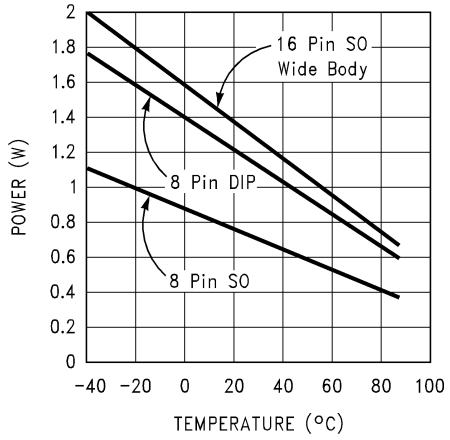



**図 5-92. Maximum Power Dissipation vs Ambient Temperature**

# 6 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 6.1 Application Information

The LM7171 is a very high-speed, voltage-feedback amplifier (VFA). This device consumes only 6.5mA of supply current while providing a unity-gain bandwidth of 200MHz and a slew rate of 4100V/µs. The LM7171 also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true VFA. Unlike a current-feedback amplifier (CFA) with a low inverting input impedance and a high noninverting input impedance, both inputs of a VFA have high-impedance nodes. The low-impedance inverting input of a CFA and a feedback capacitor create an additional pole that leads to instability. As a result, CFAs cannot be used in traditional op-amp circuits such as photodiode amplifiers, I-to-V converters, and integrators, where a feedback capacitor is required.

### 6.1.1 Circuit Operation

The class AB input stage in LM7171 is fully symmetrical and has a similar slewing characteristic to a CFA. In the LM7171 simplified schematic, Q1 through Q4 form the equivalent of the current-feedback input buffer, $R_E$ the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

### 6.1.2 Slew Rate Characteristic

The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor $R_E$. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in *セクション 5.8*.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1kΩ in series with the input of LM7171, the bandwidth is reduced to help lower the overshoot.

#### *6.1.2.1 Slew-Rate Limitation*

If the amplifier input signal amplitude is too large and the frequency too high, the amplifier is slew-rate limited. This limiting can cause ringing in the time domain and peaking in the frequency domain at the output of the amplifier.

For the $A_V$ = +2 curves, slight peaking occurs. This peaking at high frequency (> 100MHz) is due to a large input signal at a high enough frequency that exceeds the amplifier slew rate. The peaking in the frequency response does not limit the pulse response in the time domain, and the LM7171 is stable with a noise gain of ≥ +2.

### 6.1.3 Compensation for Input Capacitance

The combination of an amplifier input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value of

$$C_F > (R_G \times C_{IN}) / R_F \quad (1)$$

can be used to cancel that pole. For LM7171, a feedback capacitor of 2pF is recommended. 図 6-1 illustrates the compensation circuit.

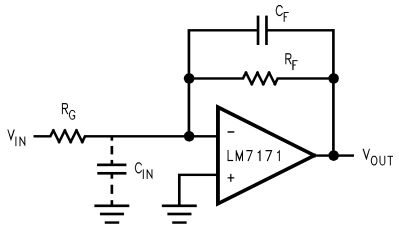



**図 6-1. Compensating for Input Capacitance**

## 6.2 Typical Applications

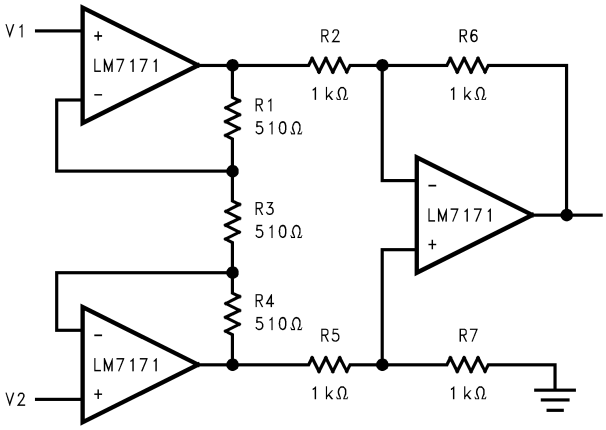



**図 6-2. Fast Instrumentation Amplifier**

$$V_{IN} = V_2 - V_1$$

if R6 = R2, R7 = R5, and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

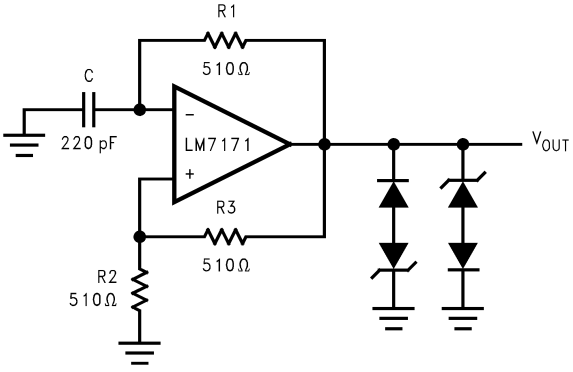



**図 6-3. Multivibrator**

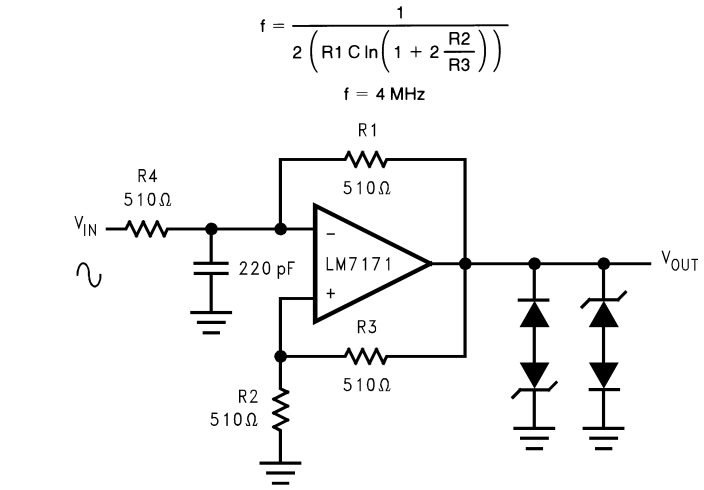



**図 6-4. Pulse Width Modulator**

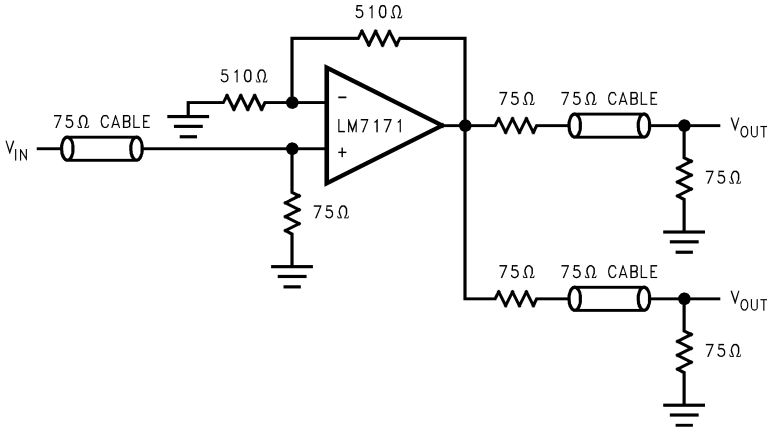



**図 6-5. Video Line Driver**

## 6.3 Power Supply Recommendations

### 6.3.1 Power-Supply Bypassing

Bypassing the power supply is necessary to maintain low power-supply impedance across frequency. To bypass both positive and negative power supplies individually, place 0.01µF ceramic capacitors directly to the power-supply pins, and 2.2µF tantalum capacitors close to the power-supply pins.

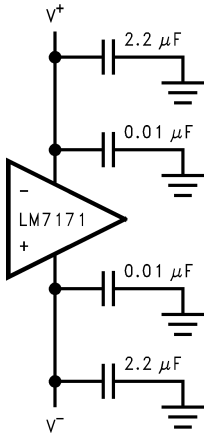



**図 6-6. Power-Supply Bypassing**

### 6.3.2 Termination

In high-frequency applications, reflections occur if signals are not properly terminated. 図 6-7 shows a properly terminated signal while 図 6-8 shows an improperly terminated signal.

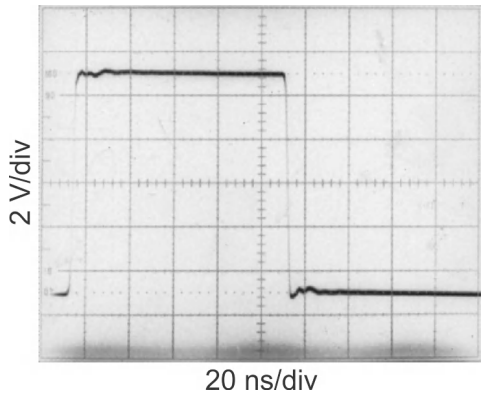



**図 6-7. Properly Terminated Signal**

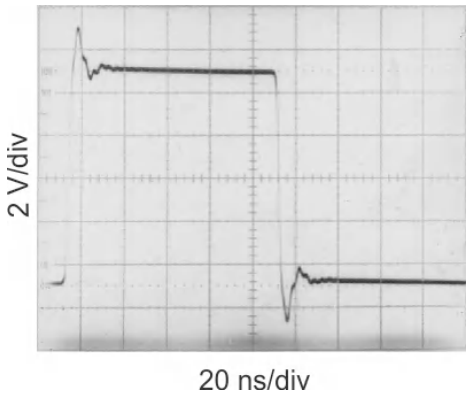



**図 6-8. Improperly Terminated Signal**

To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same-value terminator or resistor. For commonly used cables, RG59 has a 75Ω characteristic impedance, and RG58 has a 50Ω characteristic impedance.

### 6.3.3 Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in 図 6-9. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. 図 6-10 shows the LM7171 driving a 150pF load with the 50Ω isolation resistor.

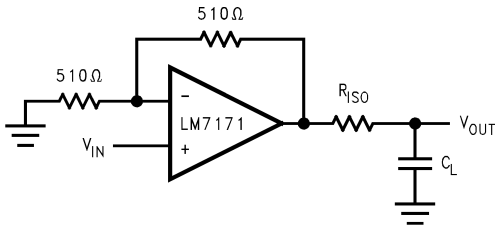



**図 6-9. Isolation Resistor Used to Drive Capacitive Load**

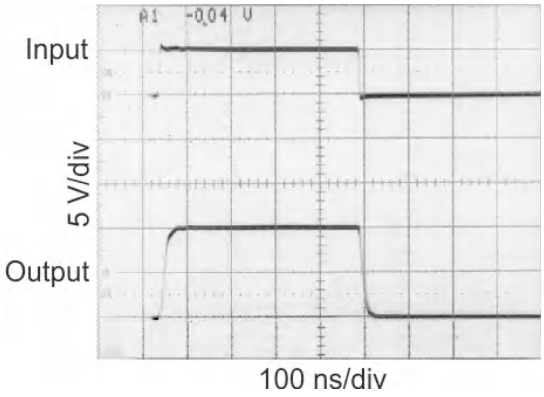



**図 6-10. The LM7171 Driving a 150pF Load With a 50Ω Isolation Resistor**

### 6.3.4 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

where

- $P_D$ is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- $T_A$ is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of a particular package

For example, for the LM7171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730mW.

Thermal resistance, $R_{\theta JA}$, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher $R_{\theta JA}$ becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- $P_Q$ is the quiescent power dissipated in a device with no load connected at the output. $P_L$ is the power dissipated in the device with a load connected at the output; $P_L$ is not the power dissipated by the load.

  Furthermore,
- $P_Q$ is the supply current × total supply voltage with no load
- $P_L$ is the output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage)

For example, the total power dissipated by the LM7171 with $V_S$ = ±15V and output voltage of 10V into 1kΩ is

$$P_D = P_Q + P_L \quad (4)$$

$$= (6.5mA) \times (30V) + (10mA) \times (15V - 10V) \quad (5)$$

$$= 195mW + 50mW \quad (6)$$

$$= 245mW \quad (7)$$

## 6.4 Layout

### 6.4.1 Layout Guidelines

#### *6.4.1.1 Printed Circuit Board and High-Speed Op Amps*

There are many things to consider when designing printed circuit boards (PCBs) for high-speed op amps. Without proper caution, excessive ringing, oscillation, and other degraded ac performance can easily occur in high-speed circuits. As a rule, keep signal traces short and wide to provide low inductance and low impedance paths. Ground any unused board space to reduce stray signal pickup. Ground critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high-frequency performance. Soldering the amplifier directly into the PCB without using any socket is better.

#### *6.4.1.2 Using Probes*

Active (FET) probes are an excellent choice for taking high-frequency measurements because of the wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

#### *6.4.1.3 Component Selection and Feedback Resistor*

In high-speed applications, keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects. such as ringing or oscillation in high-speed amplifiers. For LM7171, a feedback resistor of 510Ω gives optimized performance.

# 7 Device and Documentation Support

## 7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 7.2 サポート・リソース

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## 7.4 静電気放電に関する注意事項

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## 7.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (September 2014) to Revision D (February 2024) | Page |
|---|---|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • パッケージ情報を更新 | 1 |
| • Deleted footnote from *Recommended Operating Conditions* | 3 |
| • Changed DC and AC specifications tables to *Electrical Characteristics: ±15V* | 4 |
| • Changed LM7171A unity-gain bandwidth from 200MHz to 160MHz | 4 |
| • Changed LM7171A settling time from 42ns to 16ns | 4 |
| • Changed LM7171 A Input-referred voltage noise from 14nV/√Hz to 8.5nV/√Hz | 4 |
| • Changed LM7171 A Input-referred current noise from 1.5pA/√Hz to 1pA/√Hz | 4 |
| • Changed DC and AC specifications tables to *Electrical Characteristics: ±5V* | 6 |
| • Changed LM7171A slew rate from 950V/µs to 1200V/µs | 6 |
| • Changed LM7171A phase margin from 57° to 68° | 6 |
| • Changed LM7171A settling time from 56ns to 15ns | 6 |
| • Changed LM7171A propagation delay from 6ns to 2.5ns | 6 |
| • Changed LM7171A input-referred voltage noise from 14nV/√Hz to 8.5nV/√Hz | 6 |
| • Changed LM7171A input-referred current noise from 1.8pA/√Hz to 1pA/√Hz | 6 |
| • Added new *Typical Characteristics* section for LM7171A | 8 |
| • Deleted second paragraph in *Slew-Rate Limitation* | 24 |

| Changes from Revision B (March 2013) to Revision C (September 2014) | Page |
|---|---|
| • 新しい TI 標準に合わせてデータシートのフローとレイアウトを変更。以下のセクションを追加:「製品情報」表、「アプリケーションと実装」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション | 1 |

| Changes from Revision A (March 2013) to Revision B (March 2013) | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 25 |

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM7171AIM/NOPB | Obsolete | Production | SOIC (D) \| 8 | - | - | Call TI | Call TI | -40 to 85 | LM71<br>71AIM |
| LM7171AIMX/NOPB | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (L71AIM, LM71)<br>71AIM |
| LM7171AIMX/NOPB.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (L71AIM, LM71)<br>71AIM |
| LM7171BIM/NOPB | Obsolete | Production | SOIC (D) \| 8 | - | - | Call TI | Call TI | -40 to 85 | LM71<br>71BIM |
| LM7171BIMX/NOPB | Obsolete | Production | SOIC (D) \| 8 | - | - | Call TI | Call TI | -40 to 85 | LM71<br>71BIM |
| LM7171BIN/NOPB | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM7171<br>BIN |
| LM7171BIN/NOPB.A | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM7171<br>BIN |
| LM7171BIN/NOPB.B | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM7171<br>BIN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

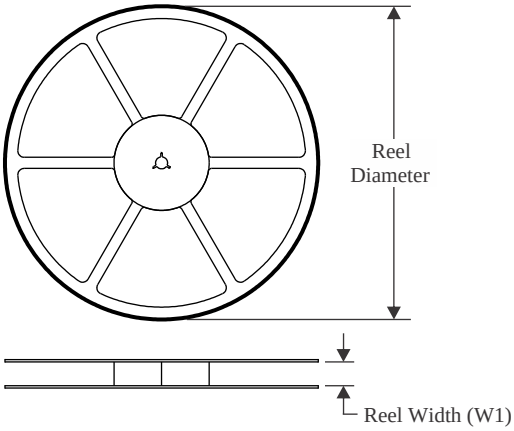
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

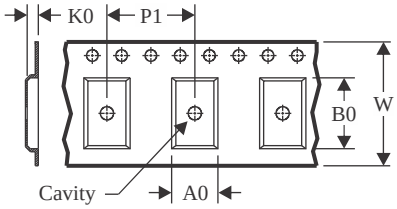
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

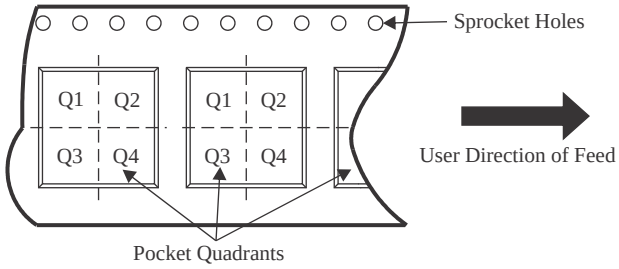



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

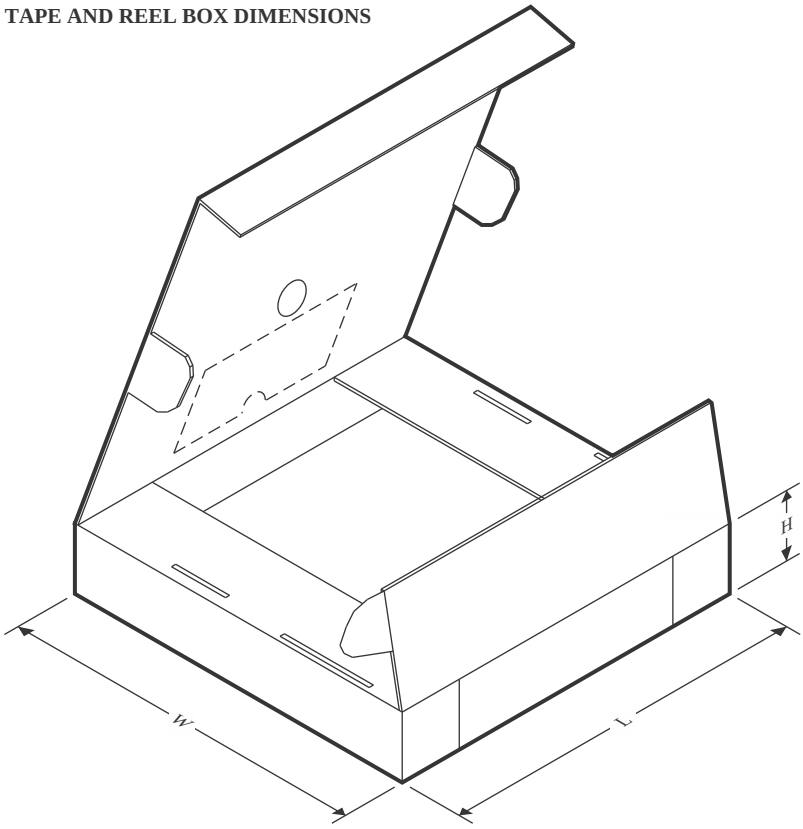
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM7171AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

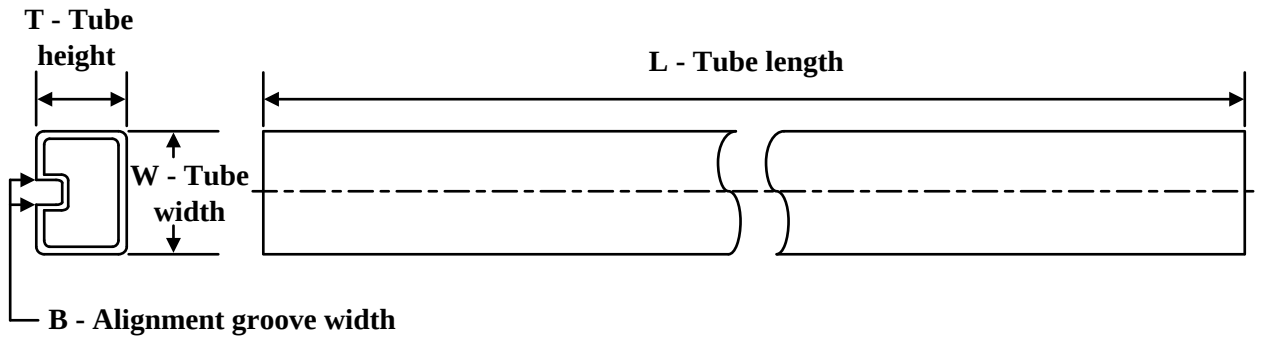
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

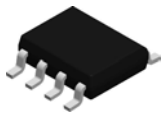
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM7171AIMX/NOPB | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM7171BIN/NOPB | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LM7171BIN/NOPB.A | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LM7171BIN/NOPB.B | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |

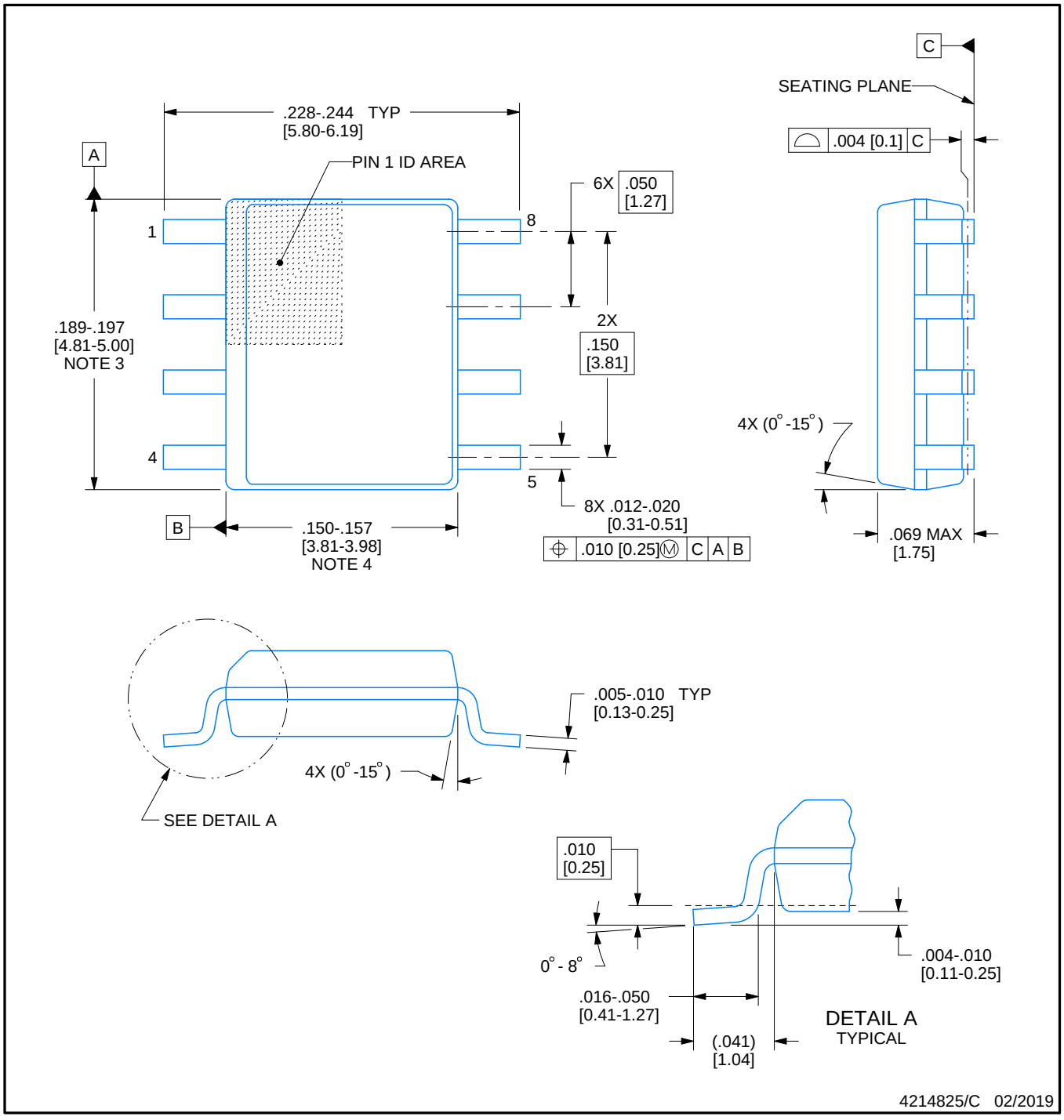


# PACKAGE OUTLINE

## D0008A

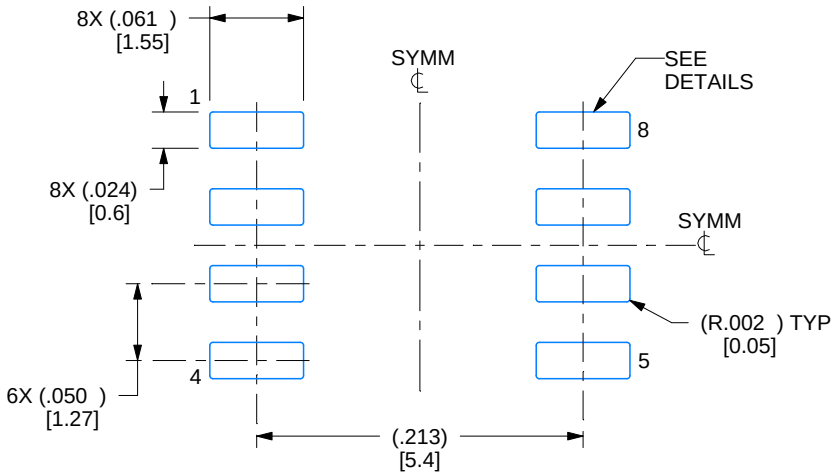
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

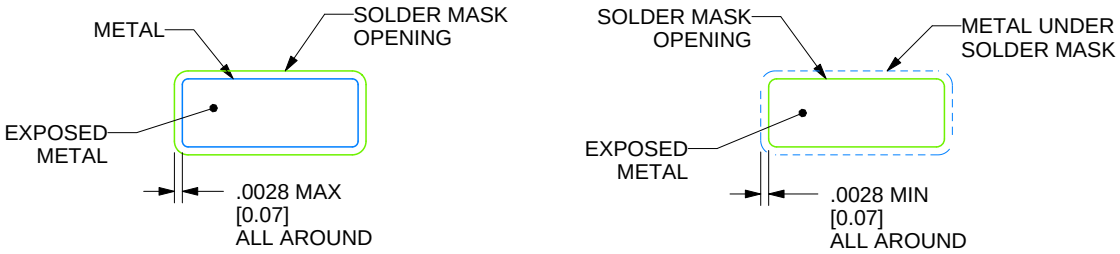



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

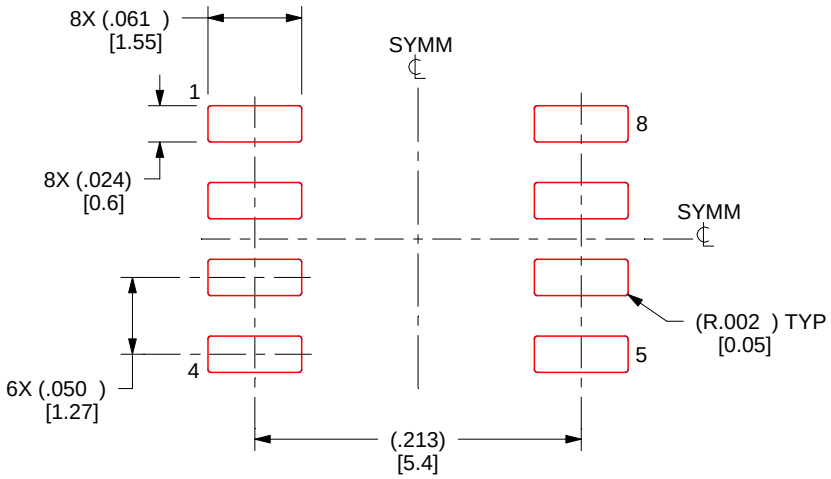
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



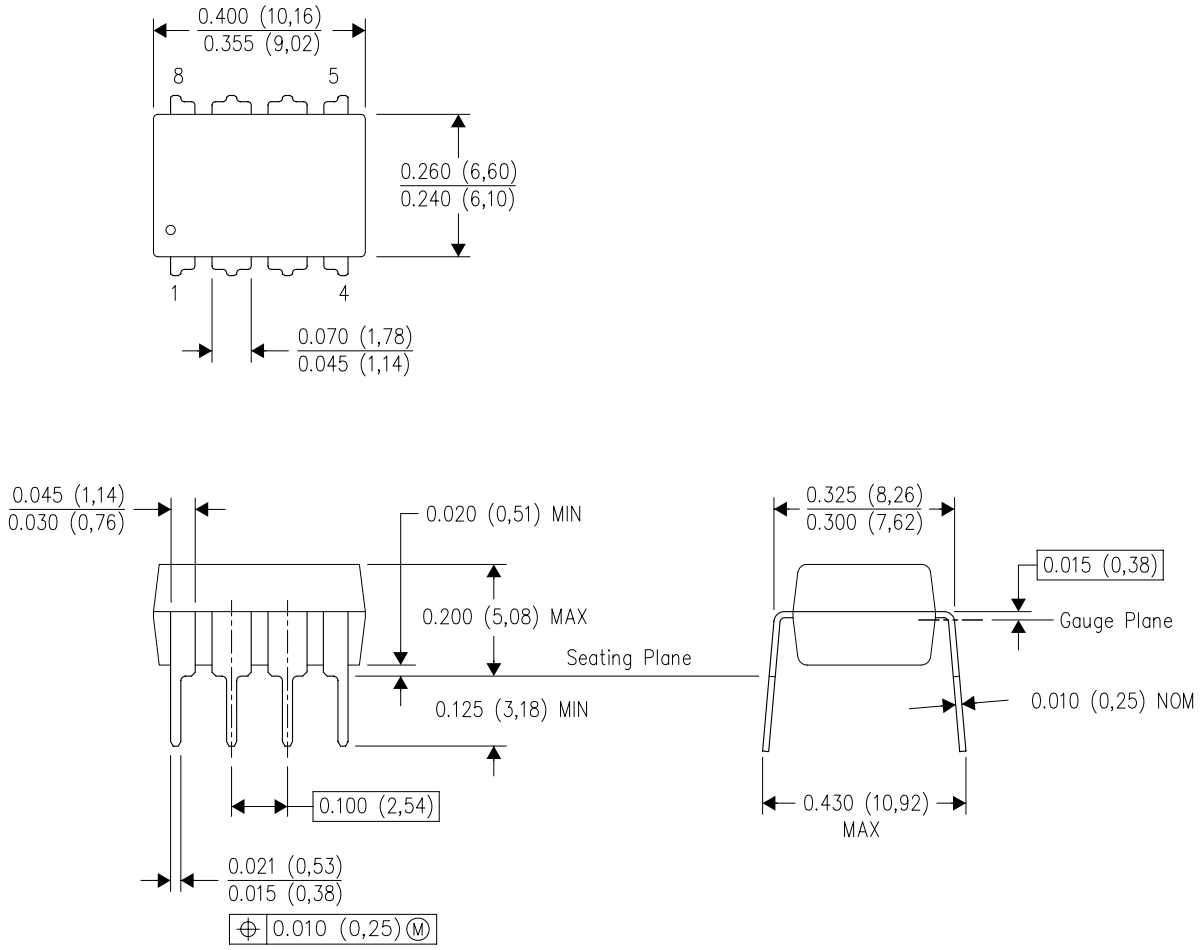

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265