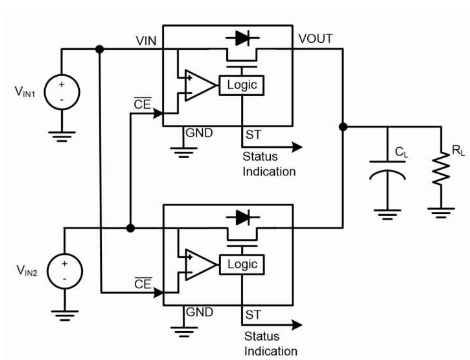
LM66100-Q1 5.5V、1.5A、79mΩ、車載用、低静止電流 (IQ) の理想ダイオード、入力極性保護付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～125℃の動作時周囲温度範囲
- 広い動作電圧範囲:1.5V～5.5V
- VIN の逆電圧スタンドオフ:–6V (絶対最大値)
- 最大連続電流 (I_{MAX}):1.5A
- オン抵抗 (R_{ON}):
  - 5V V_{IN}:79mΩ (標準値)
  - 3.6V V_{IN}:91mΩ (標準値)
  - 1.8V V_{IN}:141mΩ (標準値)
- コンパレータのチップ・イネーブル ($\overline{CE}$)
- チャネルのステータス表示 (ST)
- 低消費電流:
  - 3.6V V_{IN} 時のシャットダウン電流 ($I_{SD,VIN}$):120nA (標準値)
  - 3.6V V_{IN} 時の静止電流 ($I_{Q,\ VIN}$):150nA (標準値)

2 アプリケーション

- インフォテインメントおよびクラスタ・ヘッド・ユニット
- 車載対応、クラスタ・ディスプレイ
- ADAS サラウンド・ビュー・システムの ECU
- ボディ・コントロール・モジュールおよびゲートウェイ



代表的なアプリケーション

3 概要

LM66100-Q1 は、各種アプリケーションに適した単一入力、単一出力 (SISO) の集積化理想ダイオードです。このデバイスは、1.5V～5.5V の入力電圧範囲で動作でき、最大 1.5A の連続電流をサポートできる P チャネル MOSFET を内蔵しています。

チップ・イネーブルは、$\overline{CE}$ ピンの電圧を入力電圧と比較することで動作します。$\overline{CE}$ ピンの電圧が VIN より高い場合、デバイスはディセーブルで、MOSFET はオフです。$\overline{CE}$ ピンの電圧の方が低い場合、MOSFET はオンです。LM66100-Q1 には逆極性保護 (RPP) 機能もあり、バッテリの逆接続など入力の誤配線からデバイスを保護します。

デュアル・ダイオードの OR 実装のように、2 つの LM66100-Q1 デバイスを OR 構成で使用することもできます。この構成では、極めて高い入力電圧を出力に伝達しながら、逆電流が入力電源に流れ込むのを阻止できます。これらのデバイスは内部電圧コンパレータで入力と出力の電圧を比較し、逆電流がブロックされるようにします。

LM66100-Q1 は標準の SC-70 パッケージで供給され、–40℃～150℃の接合部温度範囲で仕様が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LM66100-Q1	SC-70 (6)	2.1mm × 2.0mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2021) to Revision A (March 2022)	**Page**
• データシートのステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

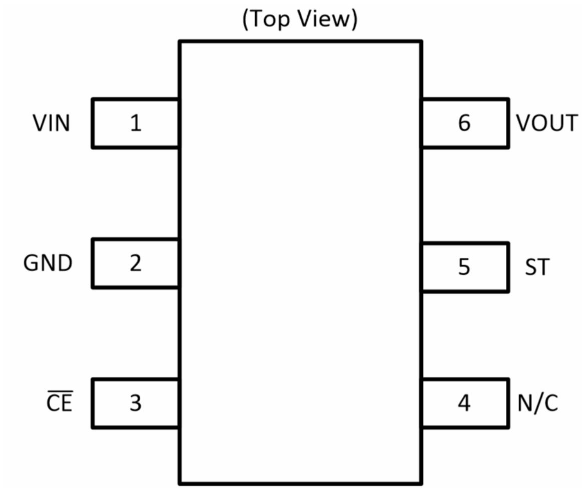


図 5-1. DCK Package 6-Pin SC-70 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Device input
2	GND	—	Device ground
3	$\overline{\text{CE}}$	I	Active-low chip enable. Can be connected to VOUT for reverse current protection. Do not leave floating.
4	N/C	—	Not internally connected, can be tied to GND or left floating.
5	ST	O	Active-low open-drain output, pulled low when the chip is disabled. Hi-Z when the chip is enabled. Connect to GND if not required.
6	VOUT	O	Device output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–6	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
$V_{\overline{CE}}$	Maximum $\overline{CE}$ Pin Voltage	–0.3	6	V
V_{ST}	Maximum ST Pin Voltage	–0.3	6	V
$I_{SW, MAX}$	Maximum Continuous Switch Current		1.5	A
$I_{SW, PLS}$	Maximum Pulsed Switch Current (≤120 ms, 2% Duty Cycle)		2.5	A
$I_{D, PLS}$	Maximum Pulsed Body Diode Current (≤0.1 ms, 0.2% Duty Cycle)		2.5	A
$I_{\overline{CE}}$	Maximum $\overline{CE}$ Pin Current	–1		mA
I_{ST}	Maximum ST Pin Current	–1		mA
T_J	Junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4A	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.5		5.5	V
V_{OUT}	Output Voltage Range	1		5.5	V
$V_{\overline{CE}}$	$\overline{CE}$ Pin Voltage Range	0		5.5	V
V_{ST}	ST Pin Voltage Range	0		5.5	V

6.4 Thermal Information

THERMAL METRIC[(1)]		LM66100 DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	34	°C/W

THERMAL METRIC[(1)]		LM66100 DCK (SC-70) 6 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	52	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values are at 25°C with an input voltage of 3.6V. Maximum and minimum values are across the entire operating voltage range, from 1.5V to 5.5V. (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input Supply (VIN)								
$I_{SD,VIN}$	VIN Shutdown Current	VOUT = VIN V$\overline{\text{CE}}$ > VIN + 80 mV I_{OUT} = 0 A (VOUT = open)		25°C		0.12	0.3	µA
				–40°C to 125°C			0.3	µA
$I_{Q,VIN}$	VIN Quiescent Current	VOUT = VIN V$\overline{\text{CE}}$ < VIN – 250 mV I_{OUT} = 0 A (VOUT = open)		25°C		0.15	0.3	µA
				–40°C to 125°C			0.3	µA
$I_{OUT, OFF}$	OUT to IN Leakage Current (Current out of VIN)	VOUT – VIN ≤ 5.5 V V$\overline{\text{CE}}$ > VIN + 80 mV		25°C		0.2	0.5	µA
				–40°C to 85°C			2.7	µA
				–40°C to 125°C			8	µA
		VOUT – VIN ≤ 4.5 V V$\overline{\text{CE}}$ > VIN + 80 mV		–40°C to 85°C			1.7	µA
				–40°C to 125°C			5.1	µA
		VOUT – VIN ≤ 1.0 V V$\overline{\text{CE}}$ > VIN + 80 mV		–40°C to 85°C			0.7	µA
				–40°C to 125°C			2.1	µA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	I_{OUT} = –200 mA	VIN = 5 V	25°C		79	95	mΩ
				–40°C to 85°C			110	
				–40°C to 125°C			120	
R_{ON}	ON-State Resistance	I_{OUT} = –200 mA	VIN = 3.6 V	25°C		91	110	mΩ
				–40°C to 85°C			125	
				–40°C to 125°C			140	
R_{ON}	ON-State Resistance	I_{OUT} = –200 mA	VIN = 1.8 V	25°C		141	180	mΩ
				–40°C to 85°C			210	
				–40°C to 125°C			230	
Comparator Chip Enable (CE)								
V_{ON}	Turn ON Threshold	V$\overline{\text{CE}}$ – VIN		–40°C to 125°C	–250	–150	–80	mV
V_{OFF}	Turn OFF Threshold	V$\overline{\text{CE}}$ – VIN		–40°C to 125°C	0	35	80	mV
$I_{\overline{CE}}$	$\overline{\text{CE}}$ Pin Leakage Current	VCE < VIN – 250 mV		–40°C to 125°C	0	160	300	nA
$I_{\overline{CE}}$	$\overline{\text{CE}}$ Pin Leakage Current	V$\overline{\text{CE}}$ > VIN + 80 mV		–40°C to 125°C	0	400	610	nA
Reverse Current Blocking (RCB) and Body Diode Characteristics								
I_{RCB}	Reverse Activation Current	V$\overline{\text{CE}}$ = VOUT		–40°C to 125°C		0.5	1	A
V_{FWD}	Body Diode Forward Voltage	I_{OUT} = 10 mA V$\overline{\text{CE}}$ > VIN + 80 mV		–40°C to 125°C	0.1	0.5	1.1	V
Status Indication (ST)								
$V_{OL, ST}$	Output Low Voltage	IST = 1 mA		–40°C to 125°C			0.1	V
t_{ST}	Status Delay Time	V$\overline{\text{CE}}$ transitions from low to high		–40°C to 125°C		1		µs

6.5 Electrical Characteristics (continued)

Typical values are at 25°C with an input voltage of 3.6V. Maximum and minimum values are across the entire operating voltage range, from 1.5V to 5.5V. (unless otherwise noted)

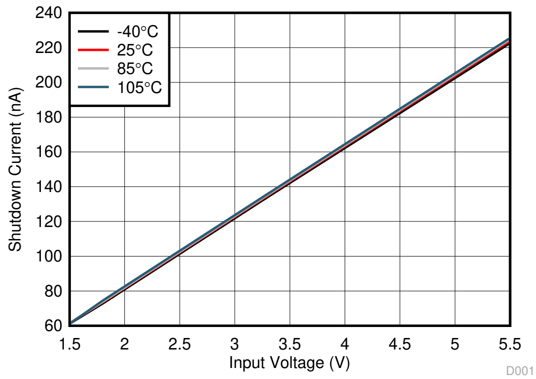
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{ST}	ST Pin Leakage Current	$\overline{VCE}$ < VIN – 250 mV	–40°C to 125°C	–20		20	nA

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended operating voltage at an ambient temperature of 25°C and a load of C_L = 100 nF and R_L = 1 kΩ

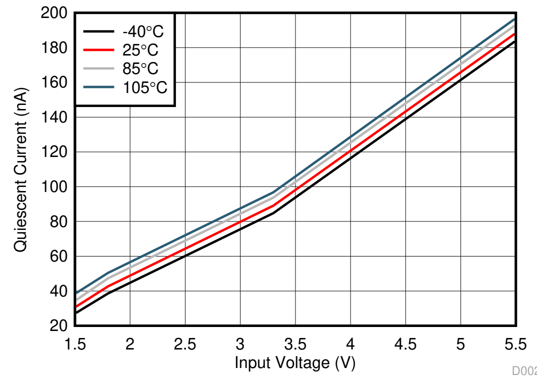
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	VIN = 1.8 V		90		µs
		VIN = 3.6 V		40		µs
		VIN = 5 V		27		µs
t_{OFF}	Turn OFF Time	VIN = 1.8 V		2		µs
		VIN = 3.6 V		2		µs
		VIN = 5 V		2		µs
t_{FALL}	Output Fall Time	VIN = 1.8 V		20		µs
		VIN = 3.6 V		10		µs
		VIN = 5 V		7.5		µs

6.7 Typical Characteristics



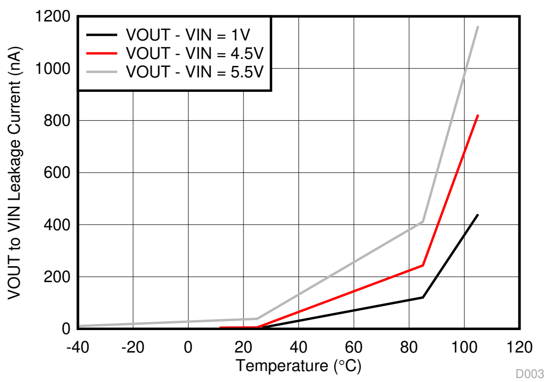
$V_{\overline{CE}} > V_{IN}$

図 6-1. Shutdown Current vs Input Voltage



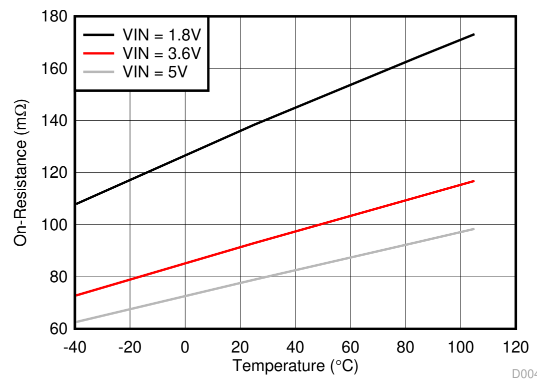
$V_{\overline{CE}} < V_{IN}$

図 6-2. Quiescent Current vs Input Voltage



$V_{\overline{CE}} > V_{IN}$

図 6-3. Reverse Leakage Current vs Junction Temperature



$V_{\overline{CE}} < V_{IN}$ I_{OUT} = 200 mA

図 6-4. On-Resistance vs Junction Temperature

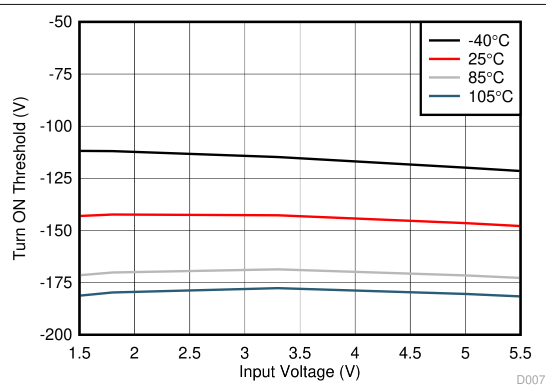


図 6-5. Turn ON Threshold vs Input Voltage

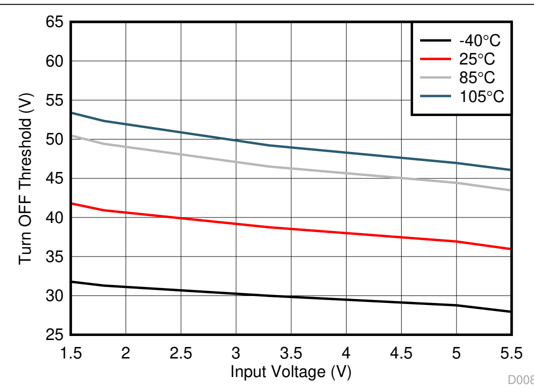
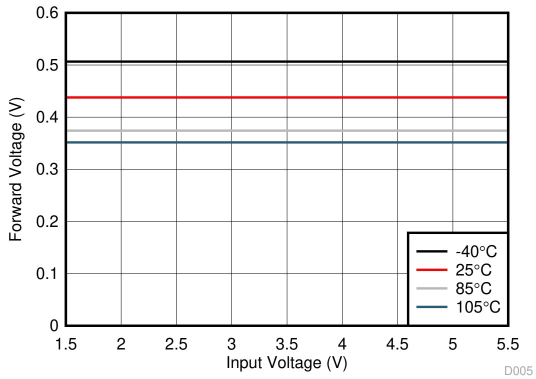


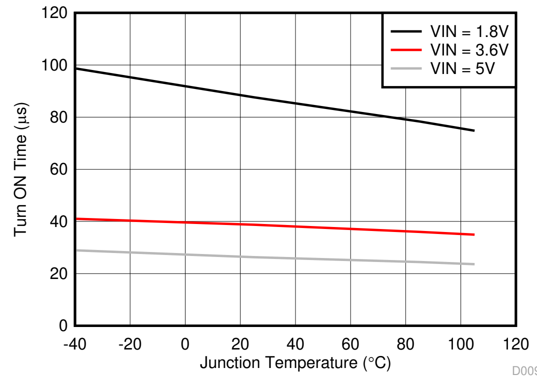
図 6-6. Turn OFF Threshold vs Input Voltage

6.7 Typical Characteristics (continued)



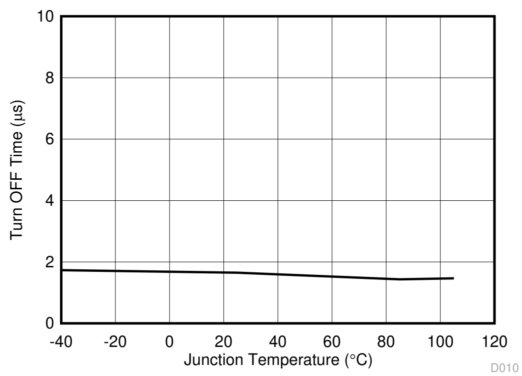
$V_{\overline{CE}} > V_{IN}$ I_{OUT} = 10 mA

図 6-7. Body Diode Forward Voltage vs Input Voltage



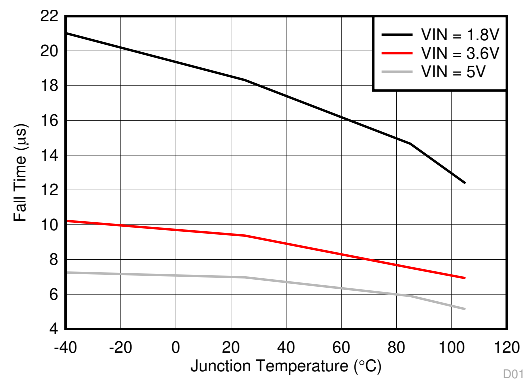
C_L = 100 nF R_L = 1 kΩ

図 6-8. Turn ON Time vs Junction Temperature



C_L = 100nF R_L = 1 kΩ V_{IN} = 1.8 V to 5 V

図 6-9. Turn OFF Time vs Junction Temperature



C_L = 100 nF R_L = 1 kΩ

図 6-10. Fall Time vs Junction Temperature

7 Parameter Measurement Information

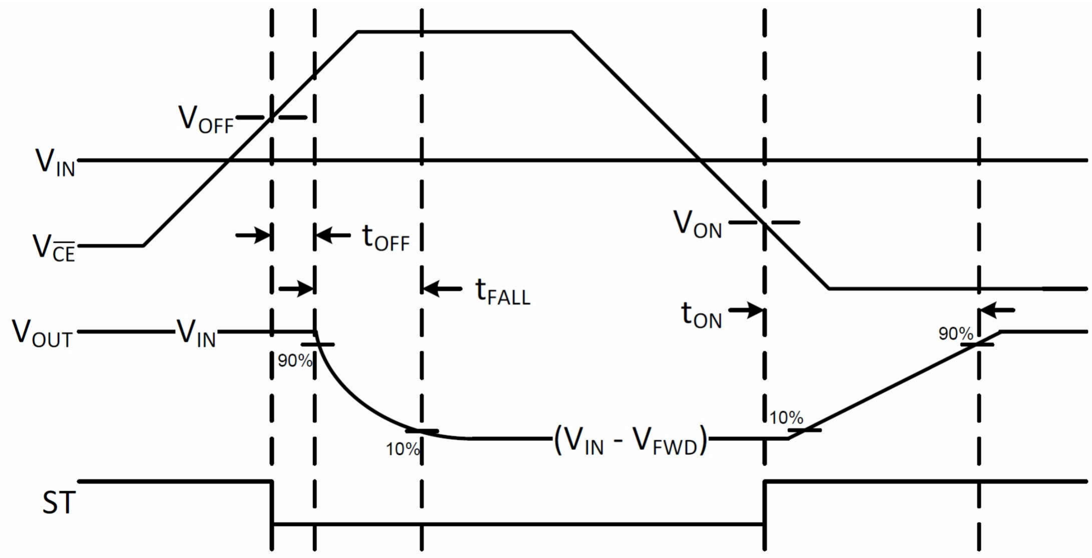


図 7-1. Timing Diagram

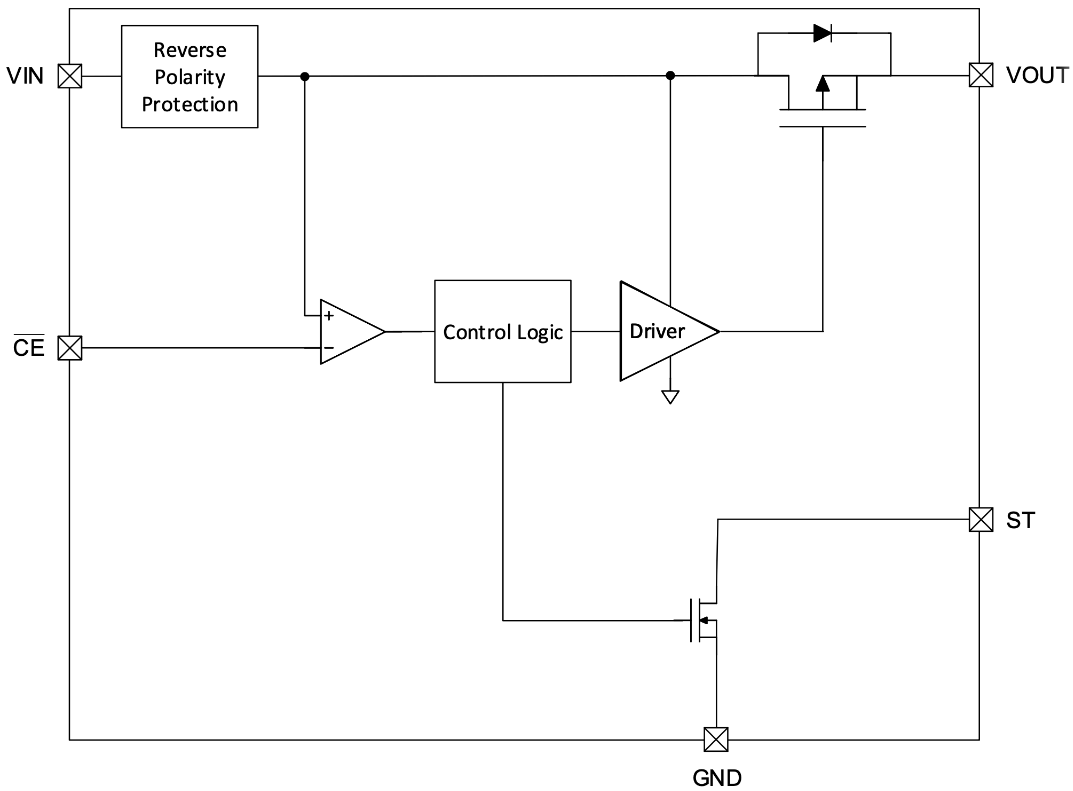
8 Detailed Description

8.1 Overview

The LM66100-Q1 is a Single-Input, Single-Output (SISO) integrated ideal diode that contains a P-channel MOSFET to minimize the voltage drop from input to output. The LM66100-Q1 can operate over an input voltage range of 1.5 V to 5.5 V and support a maximum continuous current of 1.5 A.

The chip enable works by comparing the $\overline{CE}$ pin voltage to the input voltage. When the $\overline{CE}$ pin voltage is higher than VIN by 80 mV, the device is disabled and the MOSFET is off. When the $\overline{CE}$ pin voltage is lower than V_{IN} by 250 mV, the MOSFET is on. The LM66100-Q1 also comes with reverse polarity protection (RPP) that protects against events where the VIN and GND terminals are swapped.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reverse Polarity Protection (RPP)

In the event a negative input voltage is applied, the ideal diode stays off and prevent current flow to protect the system load. For a stand-alone, always on application, $\overline{CE}$ can be tied to GND so it does not go negative with respect to GND. See 図 8-1.

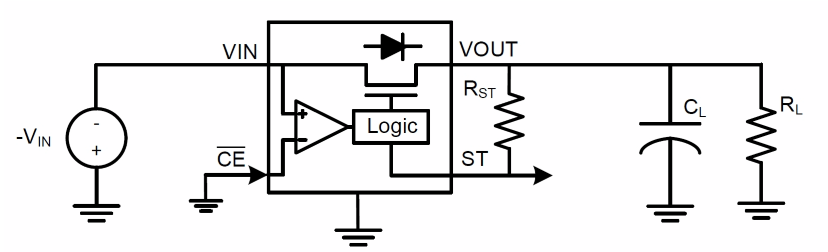


図 8-1. RPP Protection Circuit

8.3.2 Always-ON Reverse Current Blocking (RCB)

By connecting the $\overline{CE}$ pin to VOUT, this allows the comparator to detect reverse current flow through the switch. If the output is forced above the selected input by V_{OFF}, the channel switches off to stop the reverse current I_{RCB} within t_{OFF}. Once the output falls below V_{IN} by V_{ON}, the device turns back on.

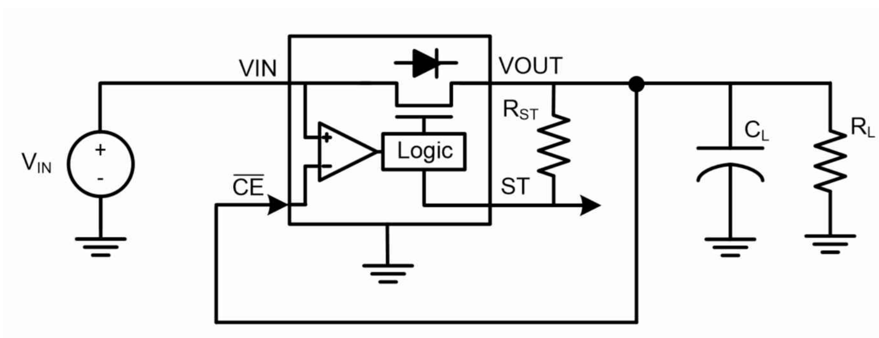


図 8-2. RCB Circuit

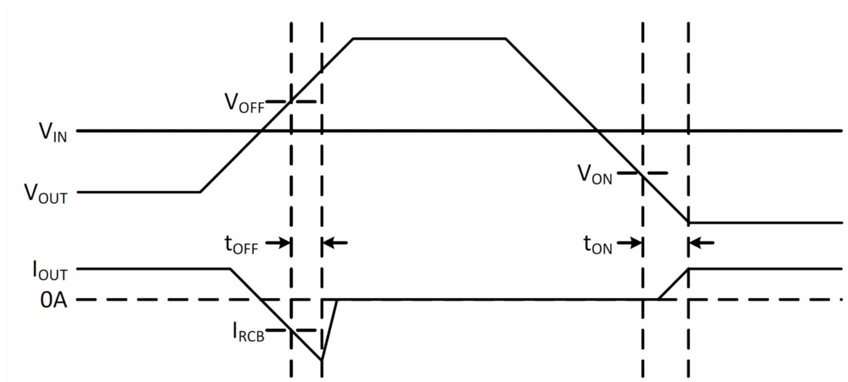


図 8-3. RCB Waveforms

8.4 Device Functional Modes

表 8-1 summarizes the Device Functional Modes:

表 8-1. Device Functional Modes

State	IN-to-OUT	Power Dissipation	ST State
OFF	Diode	$I_{OUT} \times V_{FWD}$	L
ON	Switch	$I_{OUT}{}^{2} \times R_{ON}$	H

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM66100-Q1 Ideal Diode can be used in a variety of stand-alone and multi-channel applications.

9.2 Typical Applications

9.2.1 Dual Ideal Diode ORing

Two LM66100-Q1 Ideal Diodes can be used together for ORing between two power supplies.

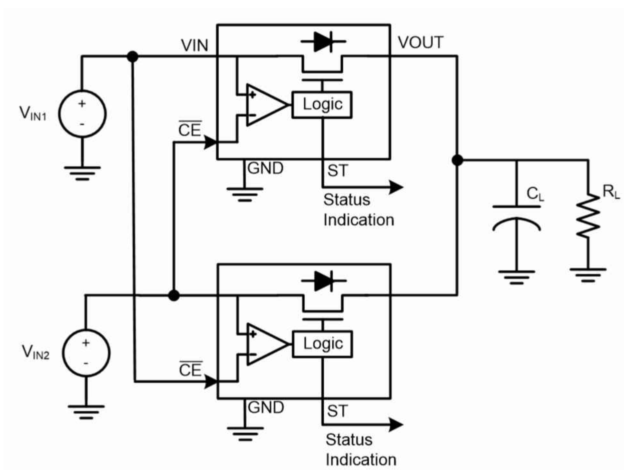


図 9-1. Dual Ideal Diode ORing

9.2.1.1 Design Requirements

Design a circuit that allows the highest input voltage to power a downstream system while providing reverse current protection.

9.2.1.2 Detailed Design Procedure

This circuit ties the $\overline{CE}$ of each device to the opposite power source. In this configuration, the highest supply is always selected using a make-before-break logic. This selection prevents any reverse current flow between the supplies and avoids the need of a dedicated reverse current blocking comparator. For ORing applications that need RPP, TI recommends to use a series resistor ($R_{\overline{CE}}$) to limit the current into the $\overline{CE}$ pin during a negative voltage event.

9.2.1.3 Application Curves

The below scope shot shows the output voltage (VOUT) being initially powered by VIN1. When VIN2 is applied, it powers VOUT because it is a higher voltage. When VIN2 is removed, VOUT is once again powered by VIN1.

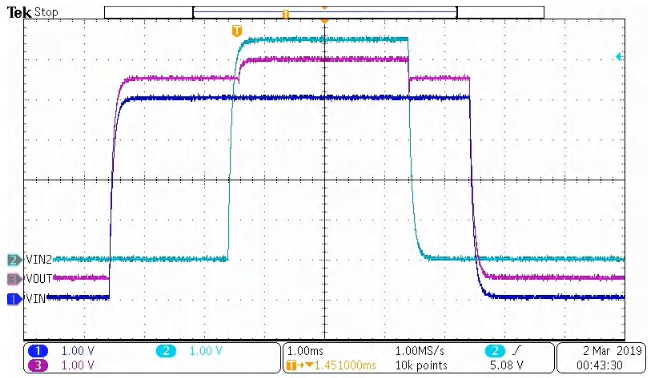


図 9-2. Dual Ideal Diode ORing Behavior

9.2.2 Dual Ideal Diode ORing for Continuous Output Power

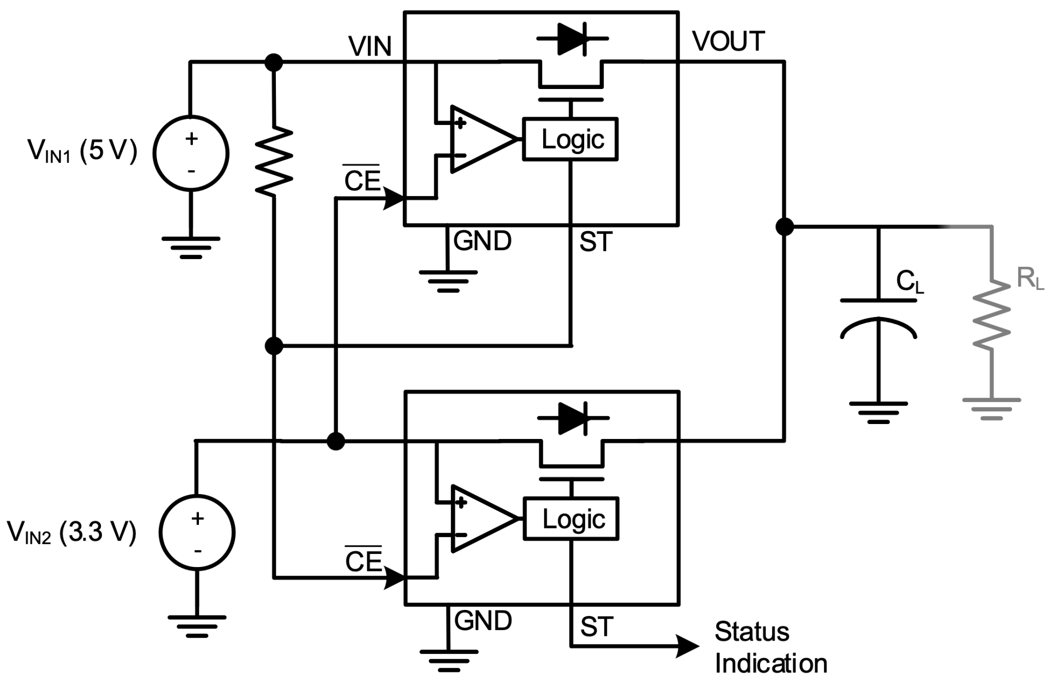


図 9-3. Dual Ideal Diode ORing for Continuous Output Power

9.2.2.1 Design Requirements

The shortcoming of the previous implementation happens when both input voltages are the same for a long period of time. Then, both devices completely turn off, powering down the output load. To avoid this case, use the status output from the priority supply and a pullup resistor, causing both devices to switchover at the same time. For ORing applications that need RPP, TI recommends to use a series resistor ($R_{\overline{CE}}$) to limit the current into the $\overline{CE}$ pin during a negative voltage event.

9.2.2.2 Application Curves

The figures below show the switchover performance between VIN1 and VIN2.

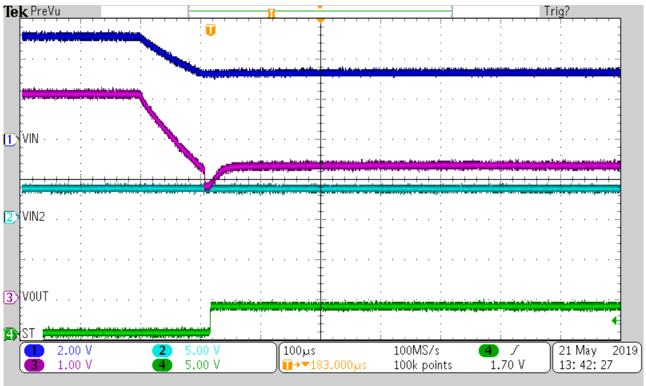


図 9-4. Switchover From VIN1 (5 V) to VIN2 (3.3 V)

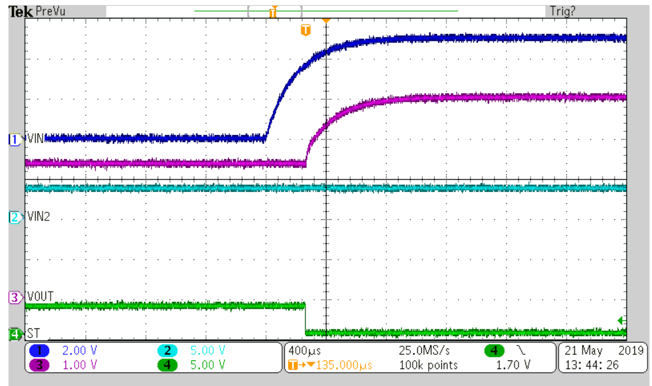


図 9-5. Switchover From VIN2 (3.3 V) to VIN1 (5 V)

9.2.3 ORing with Discrete MOSFET

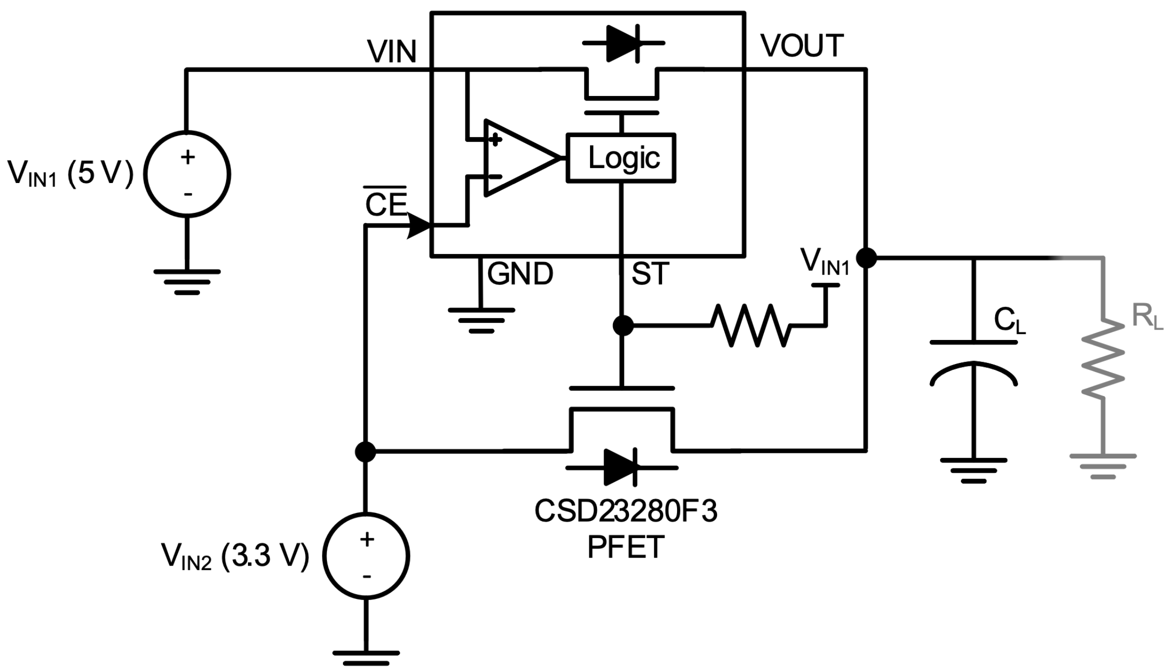


図 9-6. ORing with a Discrete MOSFET

9.2.3.1 Design Requirements

Similar to the Dual Ideal Diode circuit, the Status Output can also be used to control a discrete P-Channel MOSFET. This action can be useful in applications that want to minimize the leakage current on the secondary supply, such as battery backup systems. This configuration can also be used on systems that require a lower RON on the secondary rail, useful for higher current applications.

When the Ideal Diode path is enabled, the status is Hi-Z and pulls up the gate of the external PFET to keep it off. When the main supply (VIN1) drops such that backup supply (VIN2) is higher than VIN1, the ideal diode is disabled and pulls the ST pin and the PFET gate low to turn on the discrete MOSFET path.

9.2.3.2 Application Curves

The figures below show the switchover performance between VIN1 and VIN2.

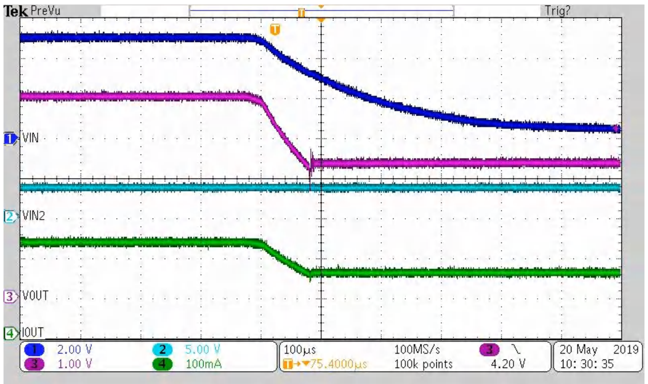


図 9-7. Switchover From VIN1 5 V to VIN2 3.3 V

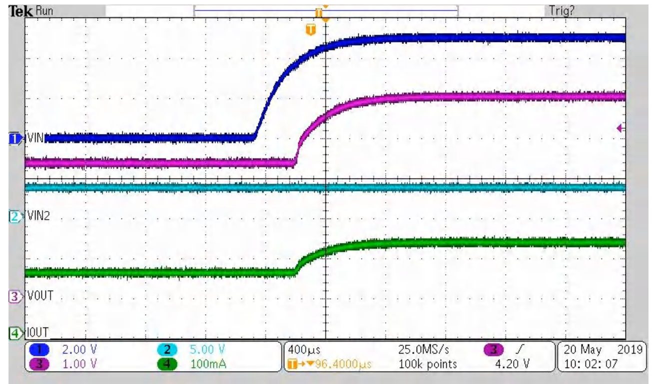


図 9-8. Switchover From VIN2 3.3 V to VIN1 5 V

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.5 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

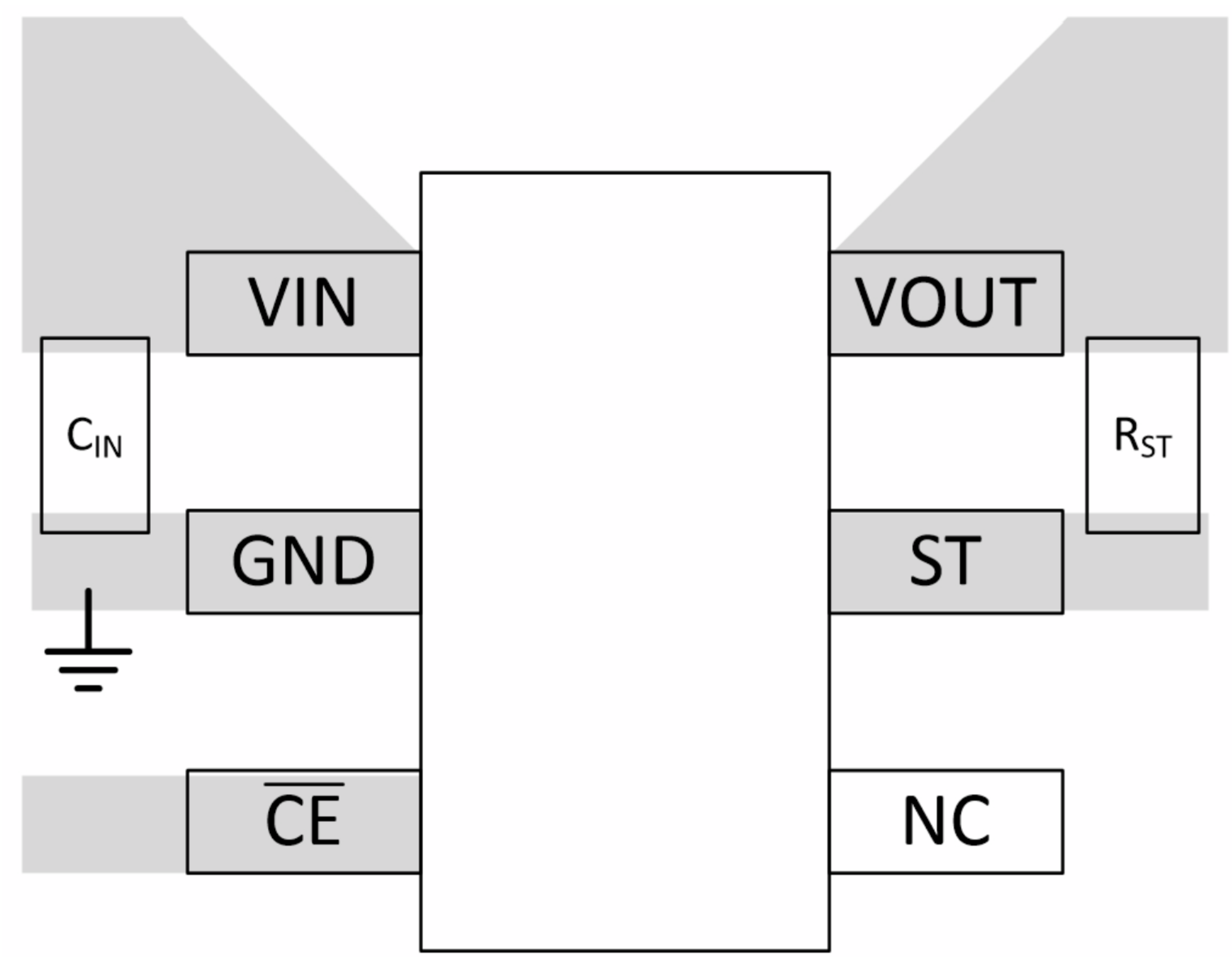


図 11-1. LM66100-Q1 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM66100QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IW
LM66100QDCKRQ1.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

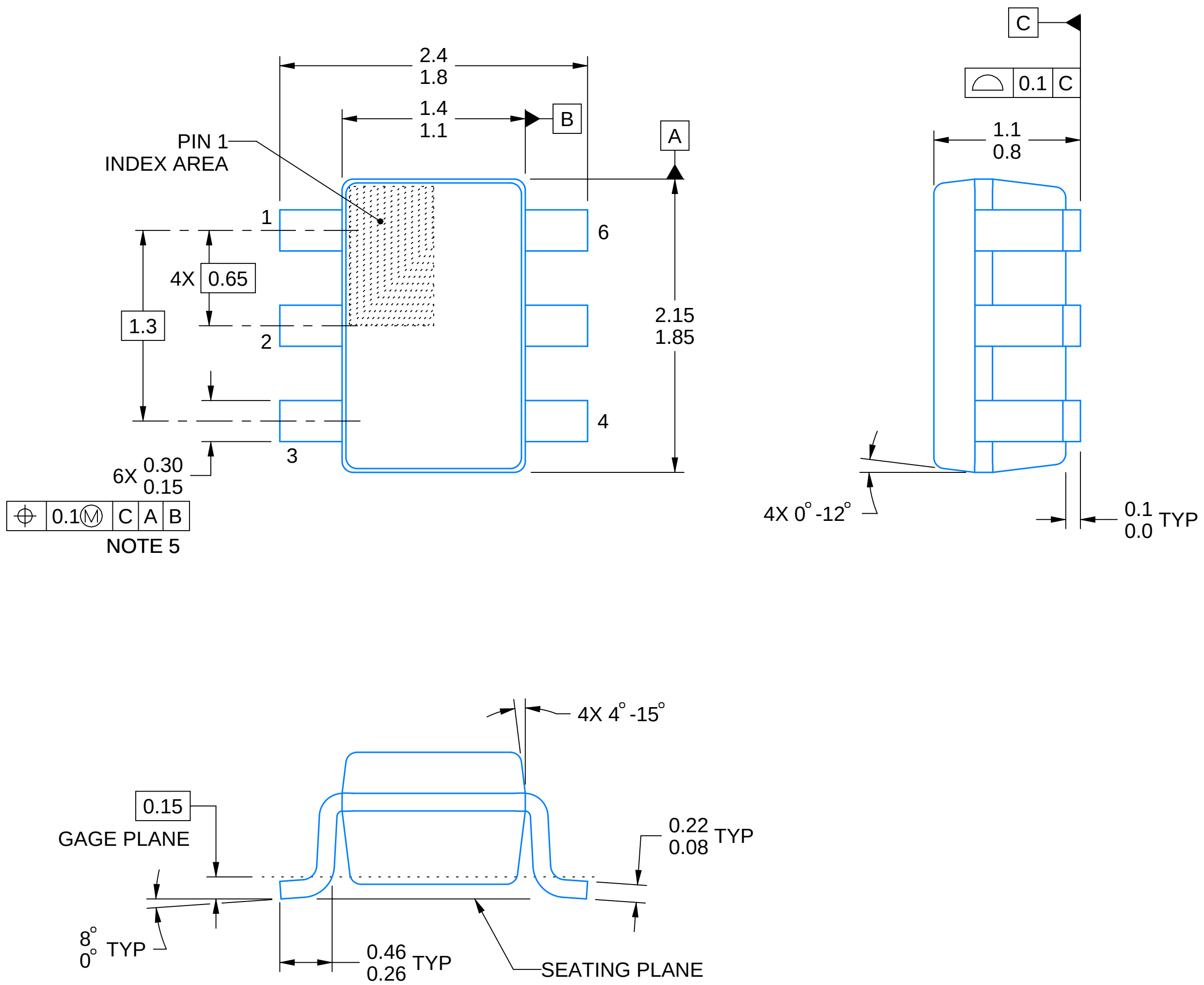
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM66100-Q1 :

- Catalog : LM66100

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



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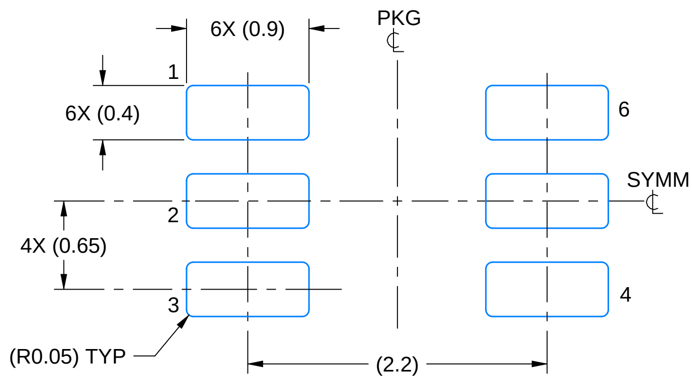
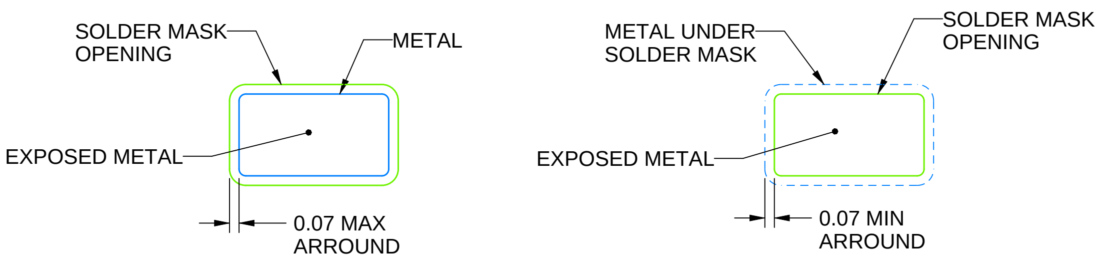
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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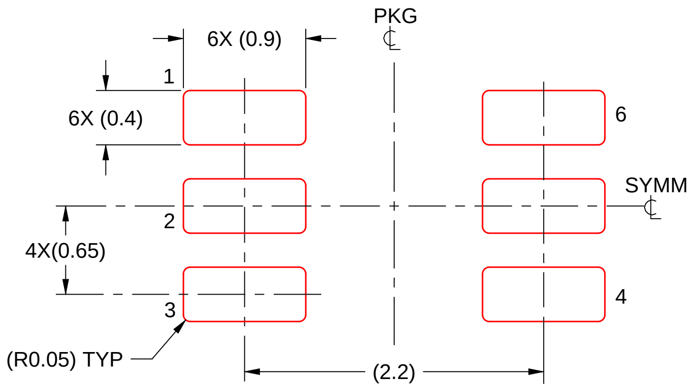
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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